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week

DRAM AND NAND PERIPHERY TRANSISTORS DEVICE LEARNING

ROMAIN RITZENTHALER, ON BEHALF OF LOGIC FOR MEMORY TEAM

LOGIC DEVICES

F203

NOW IN COURSE:

DRAM AND NAND PERIPHERY TRANSISTORS DEVICE LEARNING

ROMAIN RITZENTHALER

THIS PRESENTATION IS OPEN TO:

CORE PARTNERS, APPLE, SOCIONEXT

AMAT, ASM, BASF, SCREEN, KLA-TENCOR, KULEUVEN, LAM, SYNOPSYS, RIBER, COVENTOR, NOVA, THERMOFISHER, PARK SYSTEMS, SOITEC, KURITA, KOKUSAI, SILTRONIC, AIR LIQUIDE, EBARA, GLOBALTCADSOL, VERSUMMATERIALS, HPSP, ASML, MERCK, HITACHI, TEL, SHINETSU

imec partner technical week

PROJECT STATUS: CURRENT PTW VS. PREVIOUS PTW

PTW 2019H2 F304 | **THIS PTW (2020H1)**

DRAM peripheral devices

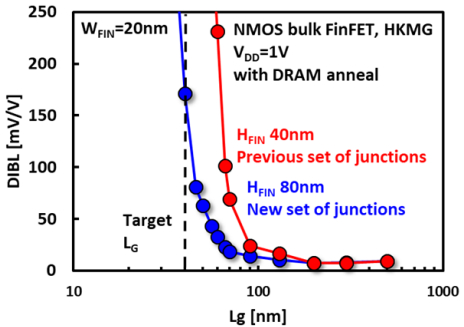
- H_{FIN} 80nm device demonstration.
- Introduction of new junctions.

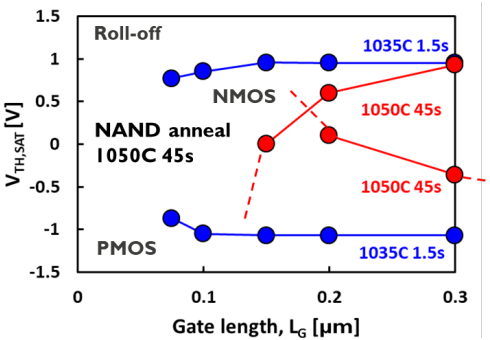
- Demonstration of Epi S/D with H_{FIN} 80nm.
- Device analysis for gate stack FinFET D&GR.

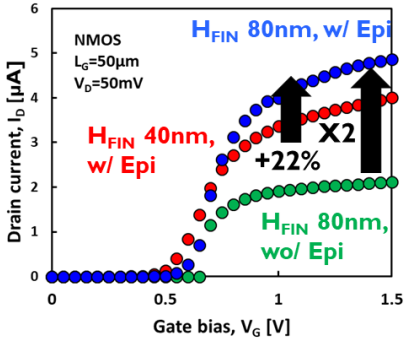
NAND peripheral devices

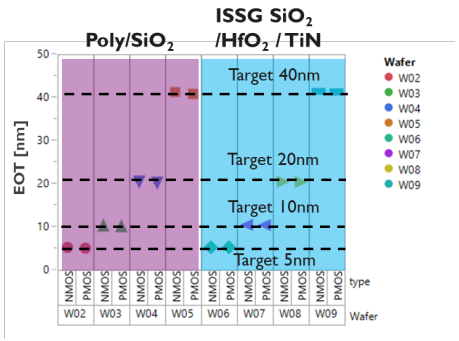
- TCAD preparatory work: NAND anneal and junctions.

- Device analysis: integration options, NAND anneal effect, and junctions analysis.









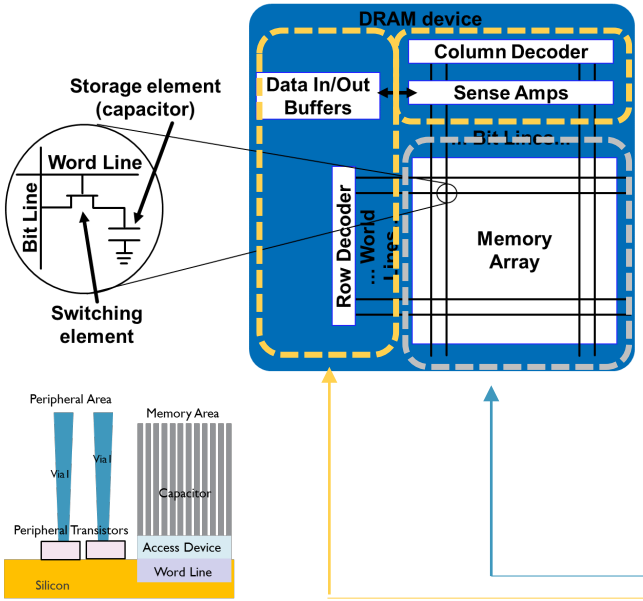
OUTLINE

- Introduction
- **DRAM peripheral devices**
- NAND peripheral devices
- Conclusions

TRANSISTORS USED IN DRAM MEMORY CHIP

Courtesy A. Spessot

- In DRAM technologies, transistors are used as access devices and in the peripheral circuitry.
- Peripheral transistors serve several purposes: address decoders, sense amplifiers, output buffers, control circuitry



	Cell Transistor	Periphery Transistor		
Type of transistor	**Access Device**	**Regular Logic Transistor**	**Sense/Amplifier**	**Row Decoder**
Applied Voltage	VPP (~3.0V)	VDD (1.5V)	Vcore (1.0V~1.3V)	VPP (~3.0V)
Gate Oxide thickness	THICK (>=6nm)	thin (<2.5nm)	thin (<2.5nm)	THICK (>=5nm)
Gate Length	Minimum Feature size	Larger than Cell (~50nm)	Longer Lg within pitched layout (e.g.: ~100nm)	Longer Lg within pitched layout (e.g.: ~120nm)
Key features/Attentio	Junction Leakage Short Channel	Speed Short Channel	Local Variation (mismatch)	Reliability

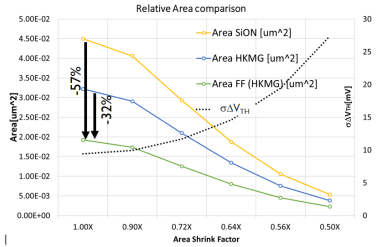
Reference value for DDR3, DRAM 20 nm node; Adapted from S. Y. Cha, IEDM 2011 short course;

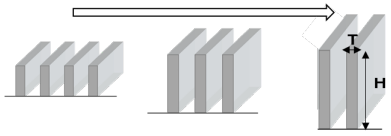
Area breakdown: Memory Array ~50%,
Periphery Transistor ~50% (~1/3 Sense Amp; ~2/3 Regular Logic + Decoder)

FINFET FOR DRAM PERI VALUE PROPOSITION

See also PTW 201810 F800

~50% area saving in the analog part



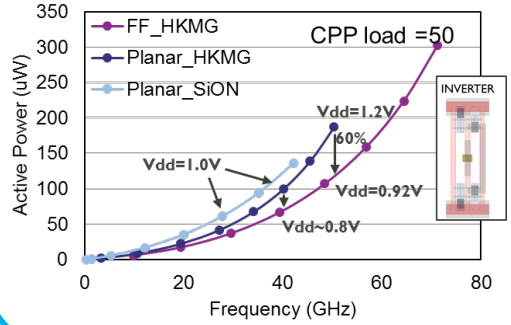


W(FinFET) = (2H+T) * Fin number

$$\partial \Delta Vt = \frac{Avt}{\sqrt{W * L}}$$

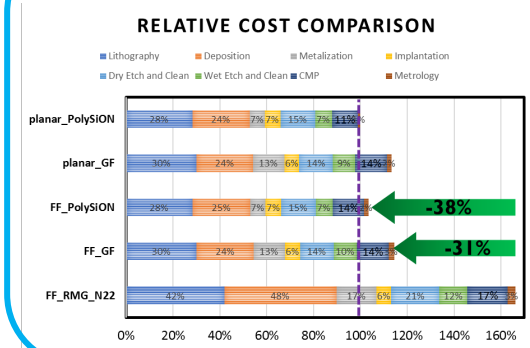
Sense/Amp benefit FinFET HMGK can enable ~50% area gain due to improved mismatch and taller fin

AC Power/Performance improvement (RO level) wrt planar



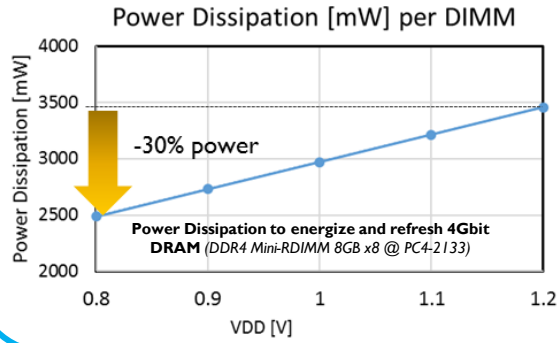
FinFET HMGK device outperform planar HKMG (60% less power at similar performance of HKMG planar with further V_{DD} reduction down to 0.8V)

Cost effective flow wrt High Performance Logic



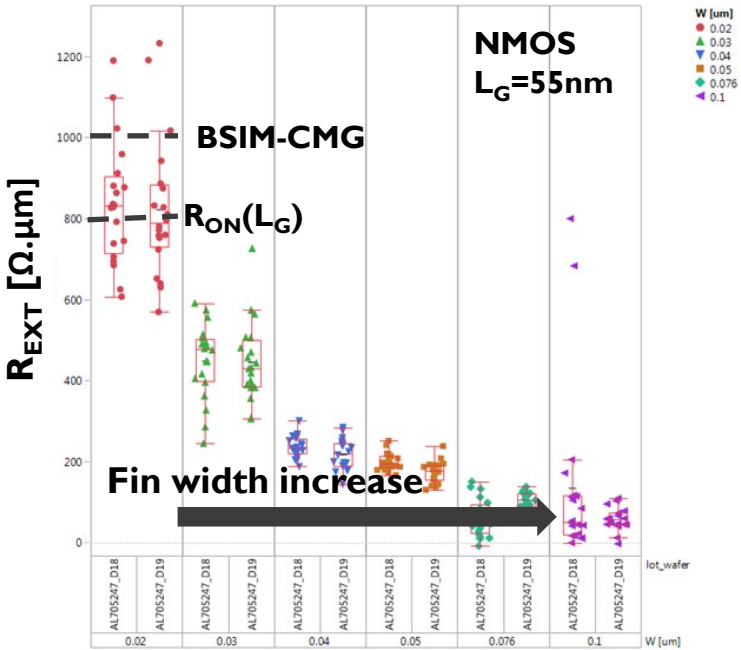
Proposed FinFET flow remains more cost effective than logic flow at corresponding dimensions

Power saving at system level wrt planar

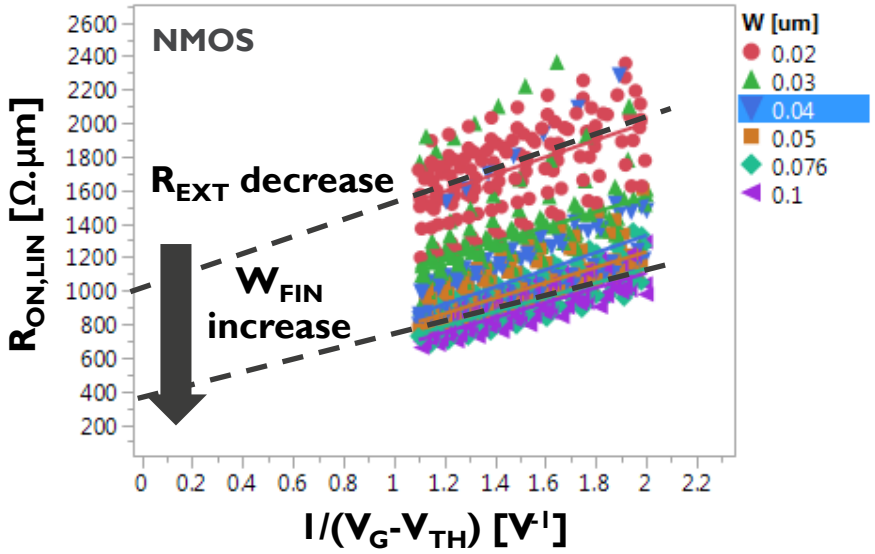


FinFET HMGK can enable 30% power saving at DIMM level wrt planar SiON devices by reducing internal V_{DD} down to 0.8V.

FINFET: EXPERIMENTAL R_{EXT} VS. FIN WIDTH



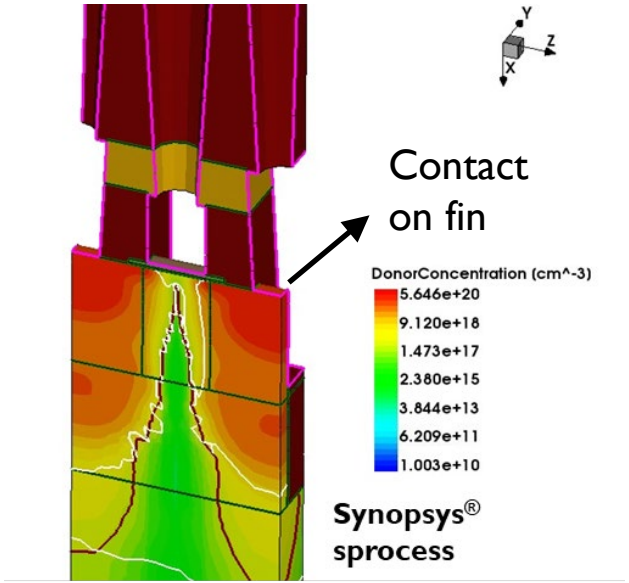
Lot: AL705247

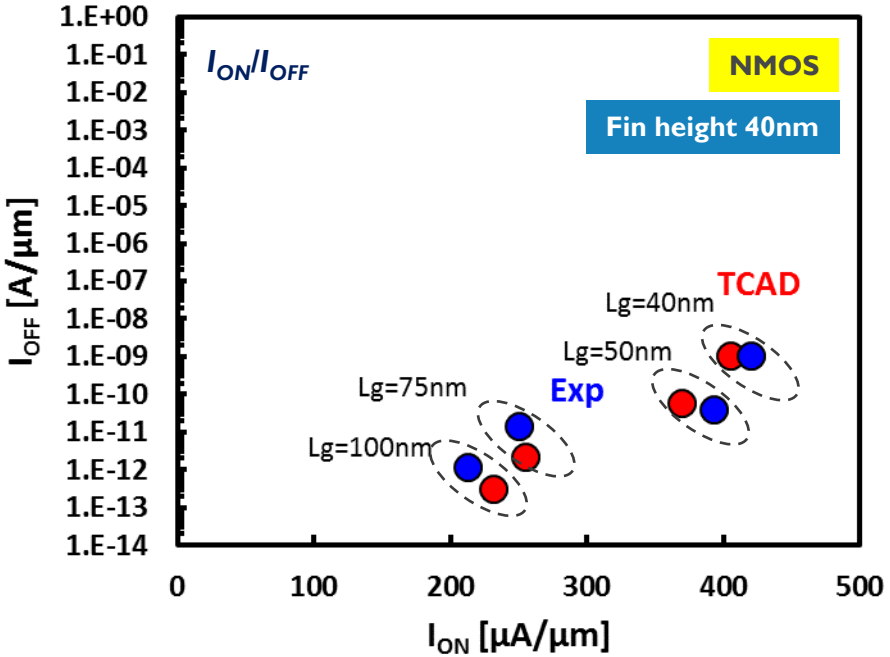


- Methods used : $R_{ON}(1/V_G-V_{TH})$*, $R_{ON}(L_G)$, and BSIM-CMG compact model fit.
- **Clear increase of external resistance R_{EXT} with decreased fin width.**

*** A. Paul et al., IEDM 2013**

UNDOPED Si EPI S/D + ION IMPLANTATION



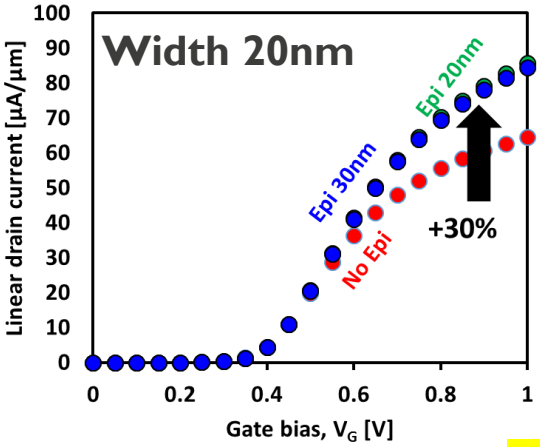


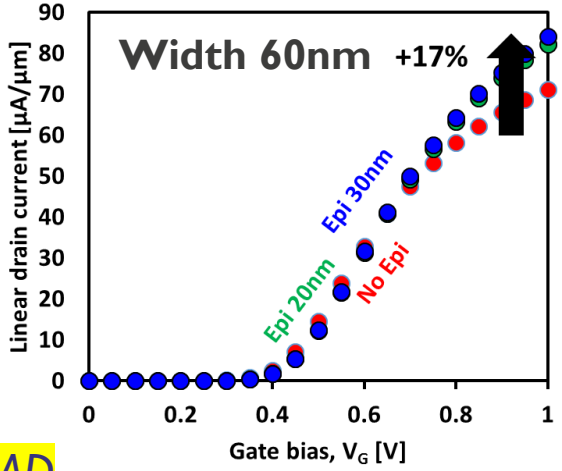
- FinFET current option: contact directly on fin.
- Undoped Epi S/D + Ion implantation could help alleviate this issue.
- Option assessed by TCAD

UNDOPED Si EPI S/D + ION IMPLANTATION:TCAD

FIN HEIGHT 40NM

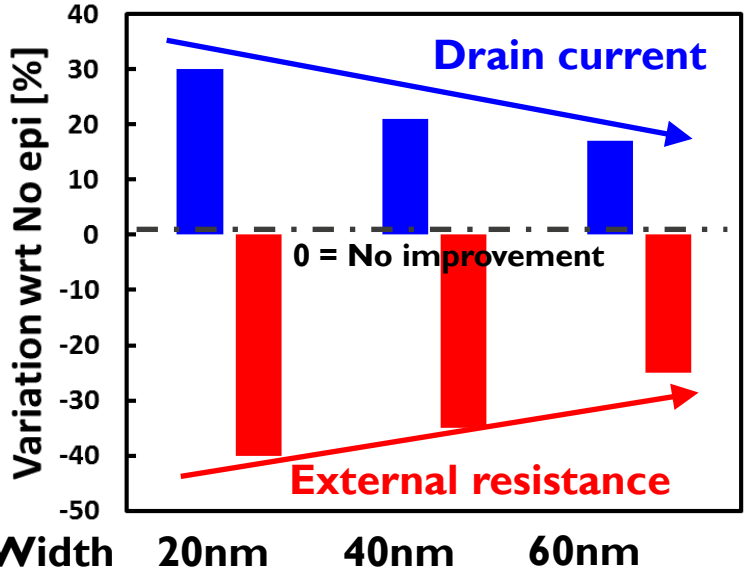
See also PTW 201810 F801





TCAD

Fin height 40nm



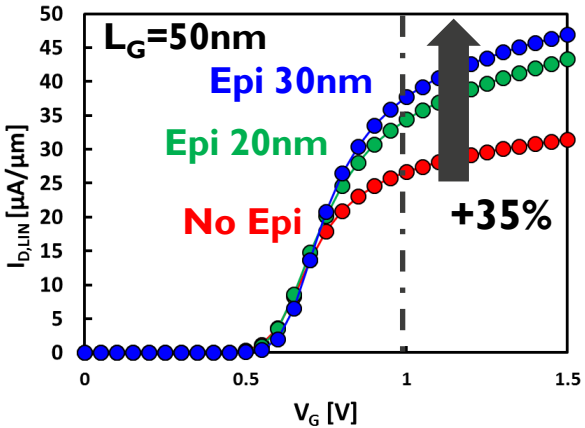
- Effect of undoped Epi S/D + Ion Implantation: drive current improvement wo/ short channel margin degradation, consequent to external resistance decrease.

UNDOPED Si EPI S/D + ION IMPLANTATION

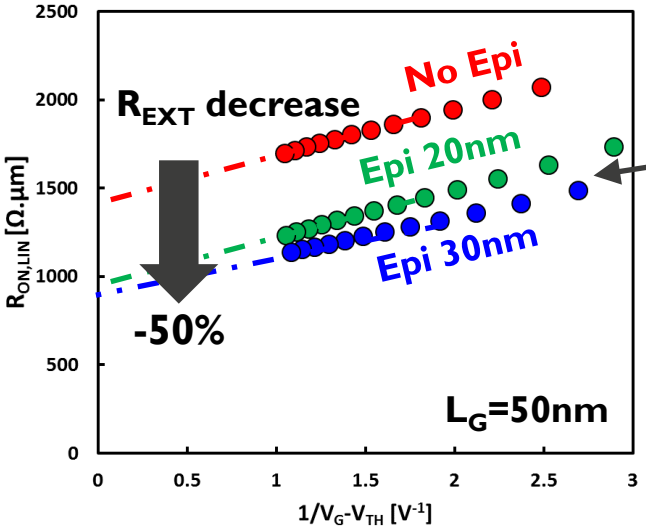
FIN HEIGHT 40NM

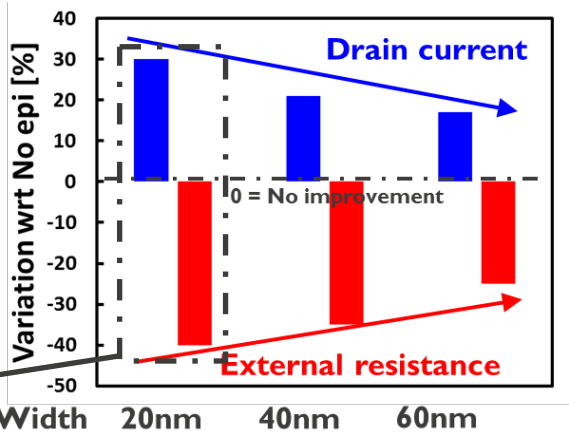
See also PTW 201810 F801

Electrical data



Lot: AL804209





TCAD predictions

Si validation

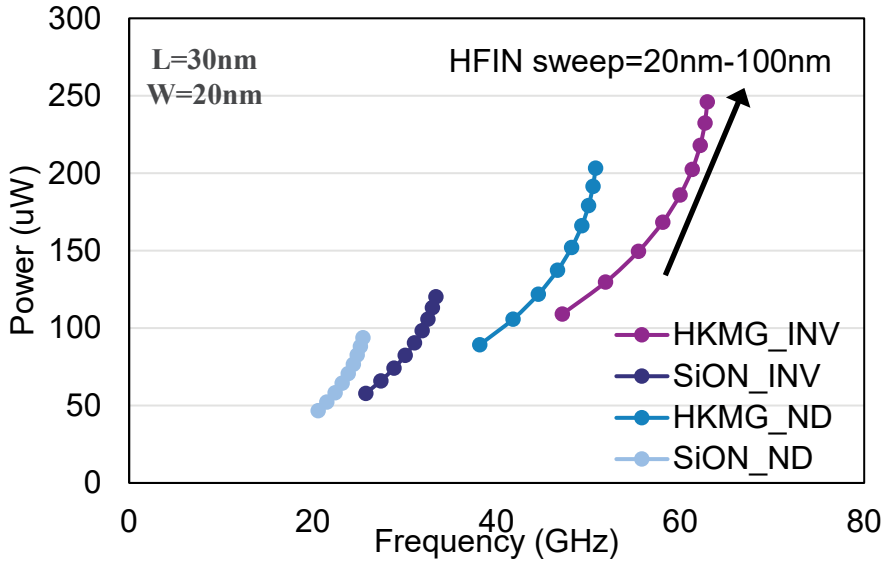
Fin height 40nm

- Electrical confirmation of improved drive current w/ Epi S/D + I/I
- Numbers comparable to TCAD predictions.
- Next: validation with <u>increased fin height of 80nm (target fin heigth).</u>

FINFET: H_{FIN} IMPACT

See also PTW 201810 F800

H_{FIN} > 80NM LEADS TO SATURATION IN PERFORMANCE

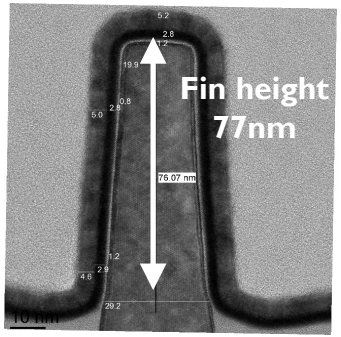


Compact models projections

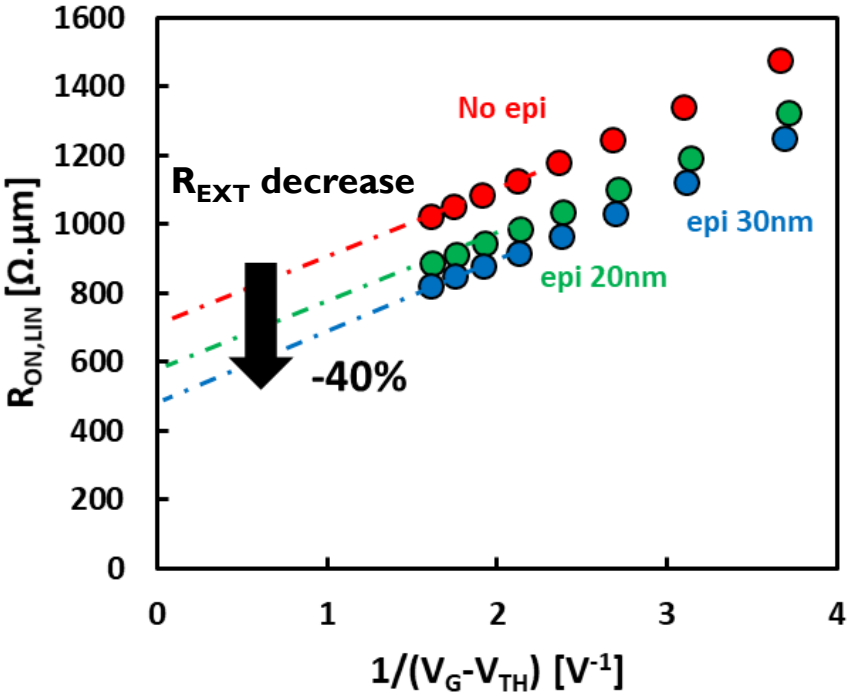
- Taller fins (H_{FIN}>80nm) leads to saturation in performance benefit.
- Leads to increase in power only.
- Similar trend obtained across INV and NAND based RO.

Target Fin height set at 80nm

TEM Channel cross-section



FINFET WITH FIN HEIGTH 80NM + S/D EPITAXY: TCAD ASSESSMENT

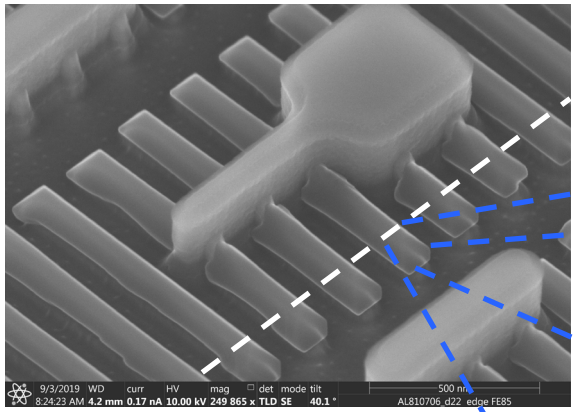


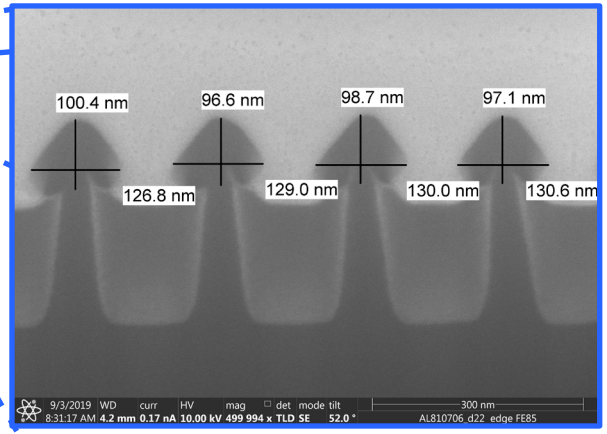
- External resistance improvement with Epitaxied S/D maintained with 80nm high Fins.

TCAD

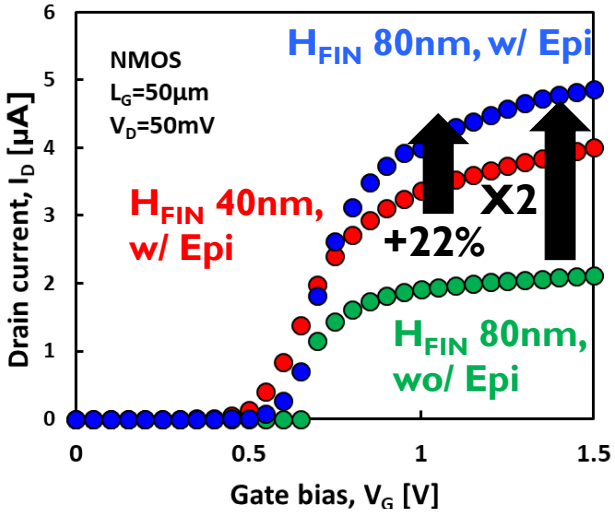
Fin height 80nm

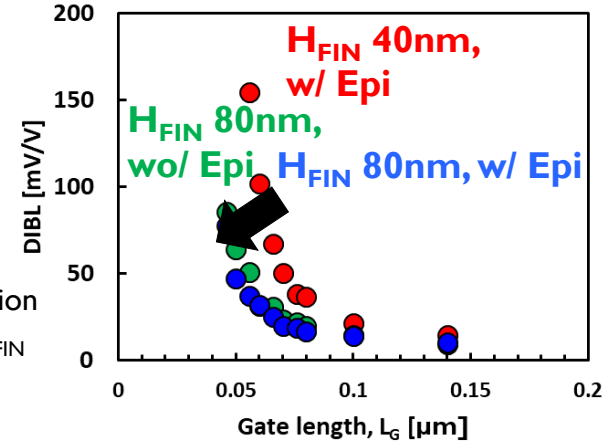
EXPERIMENTAL DEMONSTRATION (H_{FIN} 80NM)





Lots: AL804209, AL810706





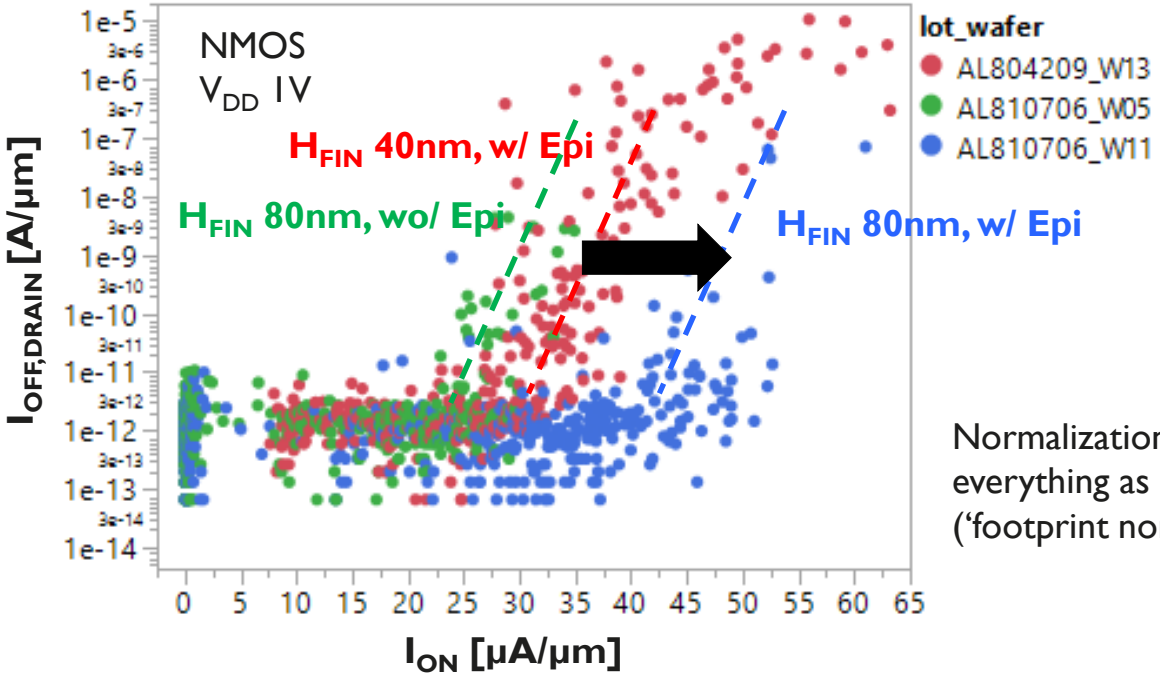
- Fin height 80nm: demonstrated current improvement w/ Epi, for no Short Channel Margin degradation.

Si validation

Fin height 80nm

*note: different set of junction between H_{FIN} 40nm and H_{FIN} 80nm

EXPERIMENTAL DEMONSTRATION (H_{FIN} 80NM)



Si validation

Fin height 40/80nm

Normalization:
everything as if H_{FIN}=40nm
('footprint normalization')

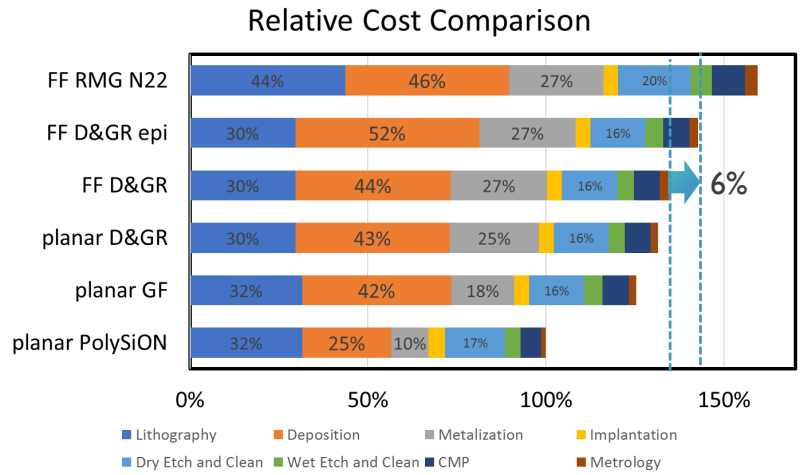
- Improvements confirmed in I_{ON}/I_{OFF} plots.

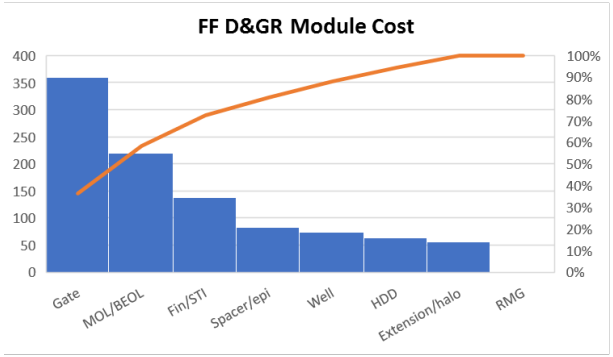
RELATIVE MODULES COST COMPARISON WITH S/D EPI & D&GR

EPI MODULES ACCOUNT FOR ~6% OF THE FINFET PERI FLOW COST

	planar PolySiON	planar GF	planar D&GR	FF D&GR	FF D&GR epi	FF RMG N22
Lithography	231.91	231.91	217.72	217.72	217.72	321.06
Deposition	184.44	308.07	319.18	321.22	380.01	339.04
Metalization	76.45	130.15	183.86	199.09	199.09	195.28
Implantation	34.4	30.88	30.88	30.88	30.88	29.13
Dry Etch and Clean	124.79	114.25	114.25	114.25	114.25	150.5
Wet Etch and Clean	31.07	37.7	32.63	34.29	36.36	43.91
CMP	43.44	54.05	54.05	54.05	54.05	68.71
Metrology	9.37	15	15	18.12	18.12	25.54
Total	735.87	922.01	967.57	989.62	1050.48	1173.17

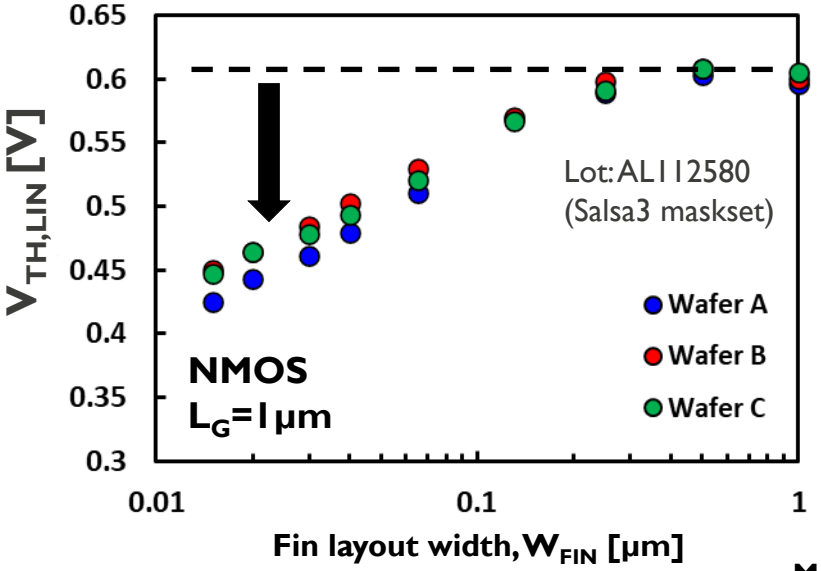
See PTW 201810 F801

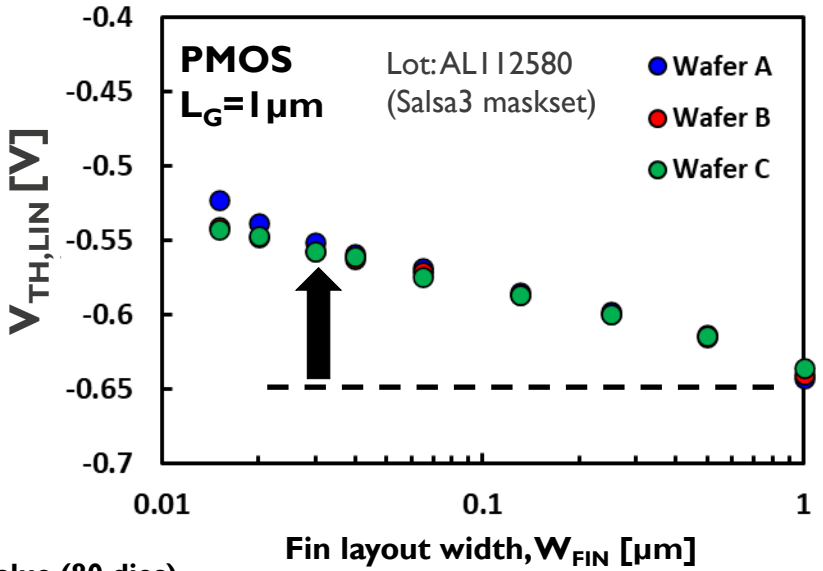




Calculation assumptions: "R&D flow", thin oxide only, HKMG with 1 Gate Stack for NMOS and 1 for PMOS, single I/I V_{TH}, periphery only; GF NMOS La; D&GR TiN/Mg/TiN

HKMG FINFET GATE STACK: THRESHOLD VOLTAGE

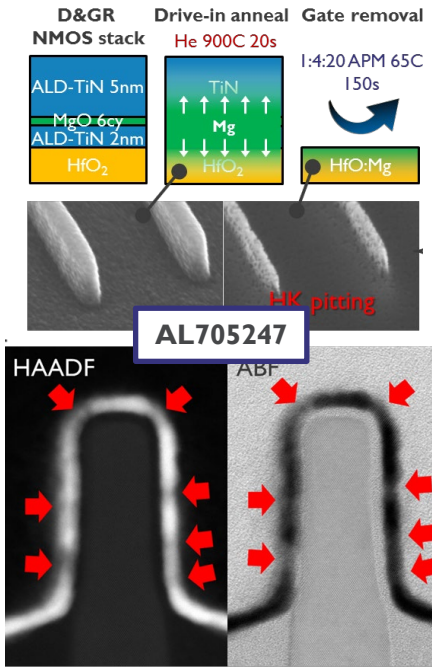




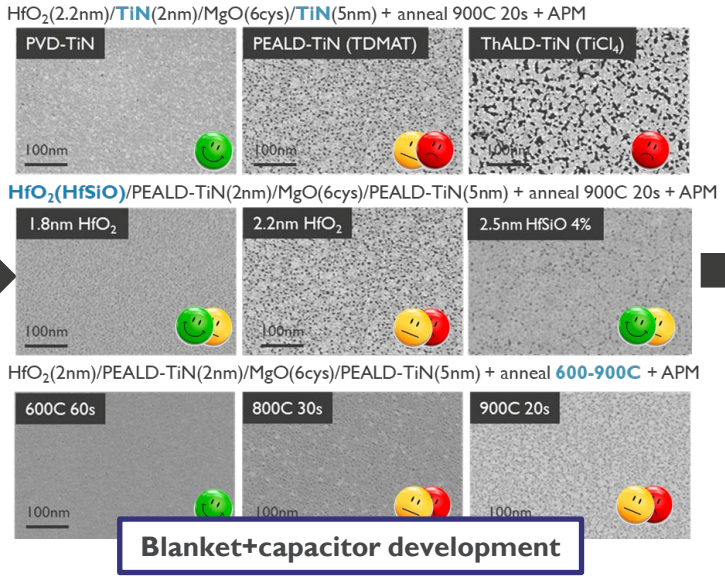
Median value (80 dies)
Gate stack: Chemical oxide (imec clean)/1.8nm ALD HfO_2/2nm ALD TiN. No eWF shifters

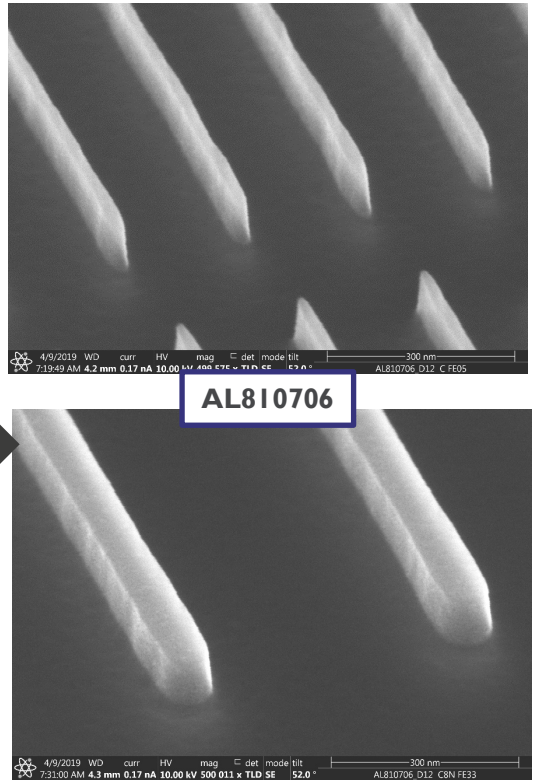
FinFETs: lower V_{TH} compared to Planar (better electrostatic control).
eWF tuning with capping layers still needed for low and multi V_{TH} enablement

HKMG FINFET GATE STACK



See also PTW 201910 F303



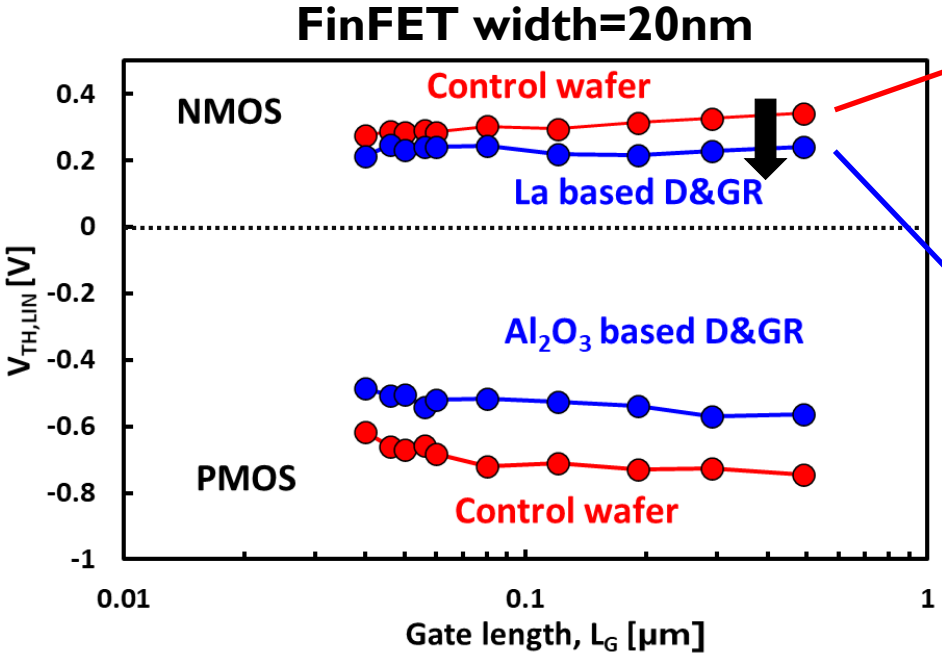


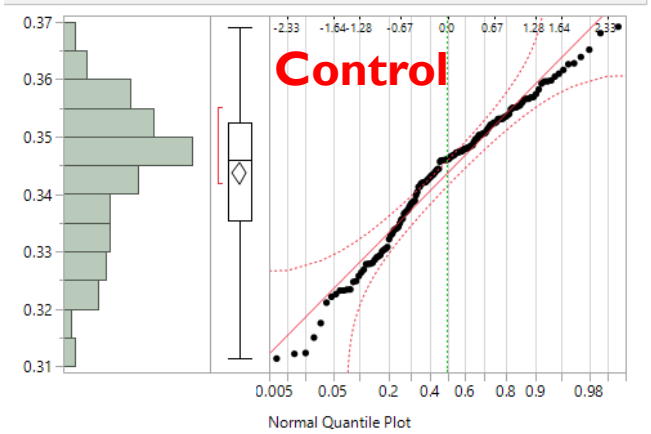
- D&GR= Diffusion and Gate Replacement (here in a Gate First Integration scheme)
- D&GR process implemented in FinFETs with PEALD TiN

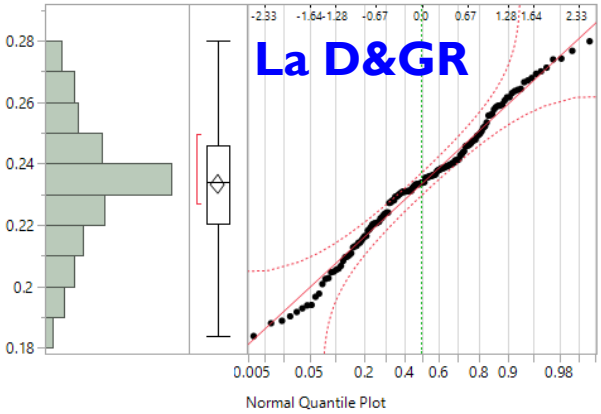
La BASED D&GR FINFET

FULL WAFER MAPPING

Lot: AL810706



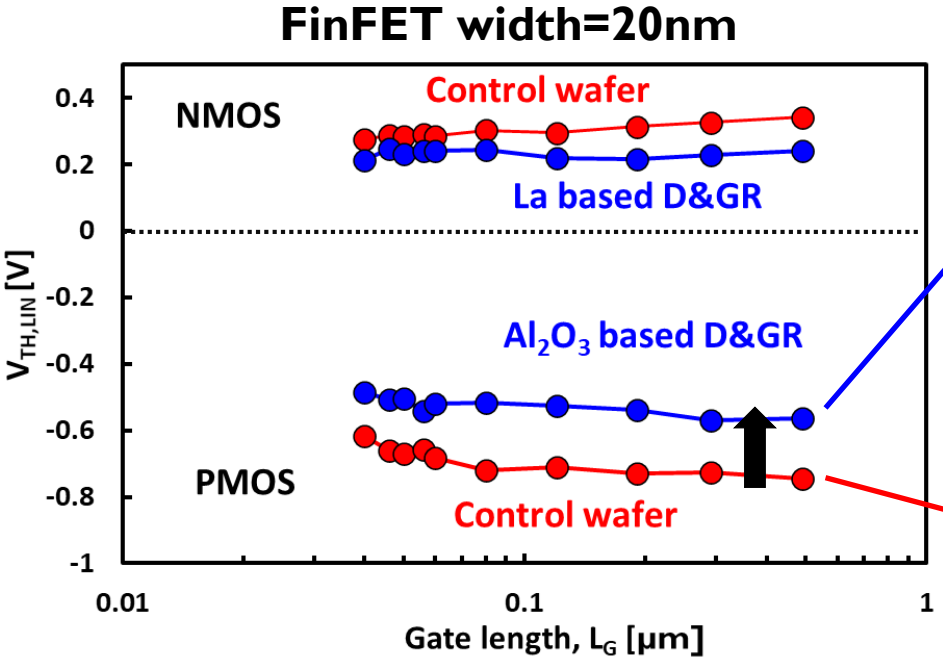


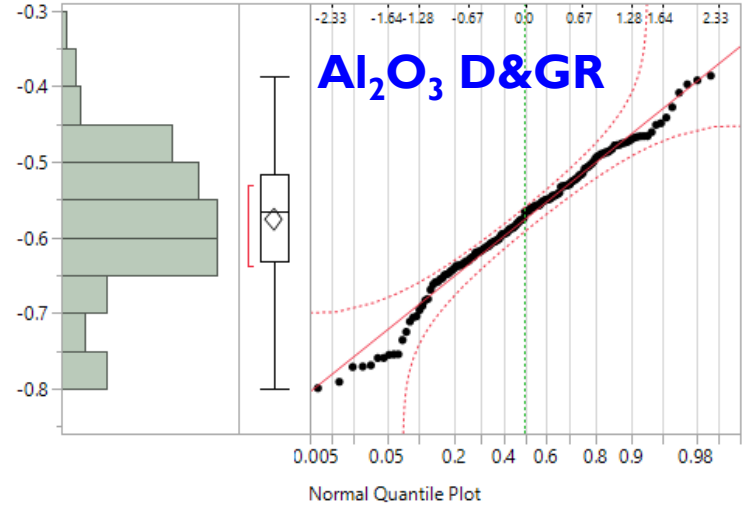


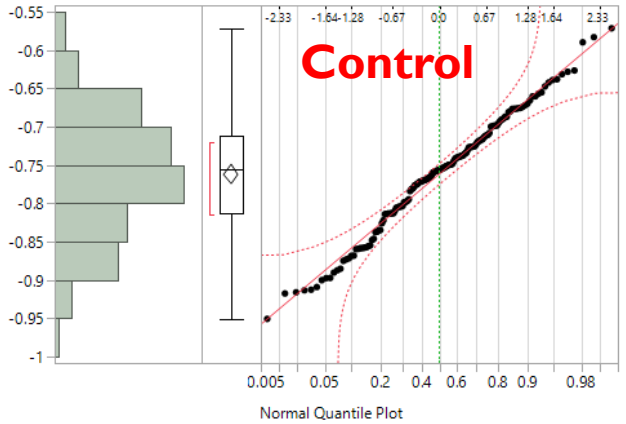
La D&GR: 110 mV V_{TH} shift in long channels

Al_2O_3 BASED D&GR
FULL WAFER MAPPING

Lot: AL810706



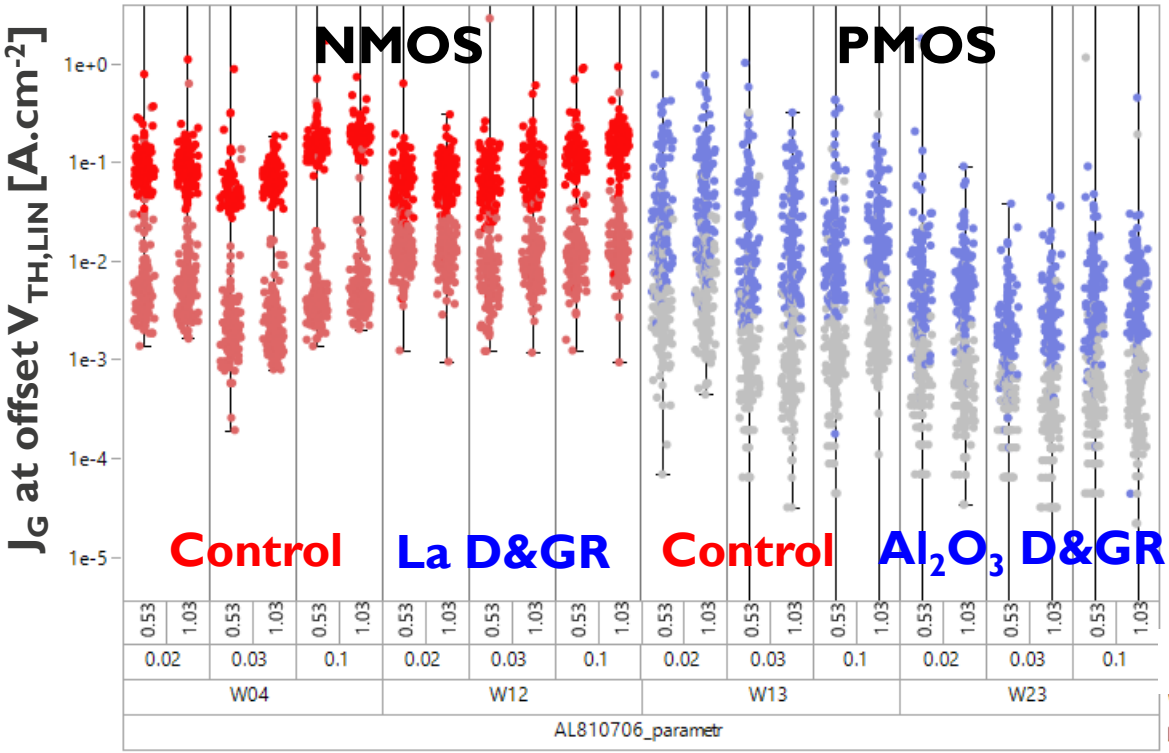




Al_2O_3 D&GR: 185 mV V_{TH} shift in long channels

D&GR FINFET: GATE LEAKAGE

FULL WAFER MAPPING



Gate overdrive [V]

- -1
- -0.6
- 0.6
- 1

Lot: AL810706

Consistent distributions
Gate leakage apparently not degraded with D&GR flow

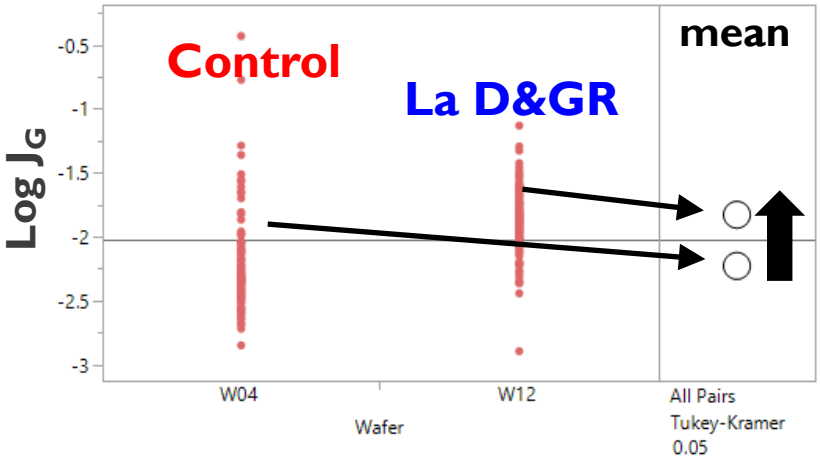
L_G [µm]

Fin Width [µm]

D&GR FINFET: GATE LEAKAGE

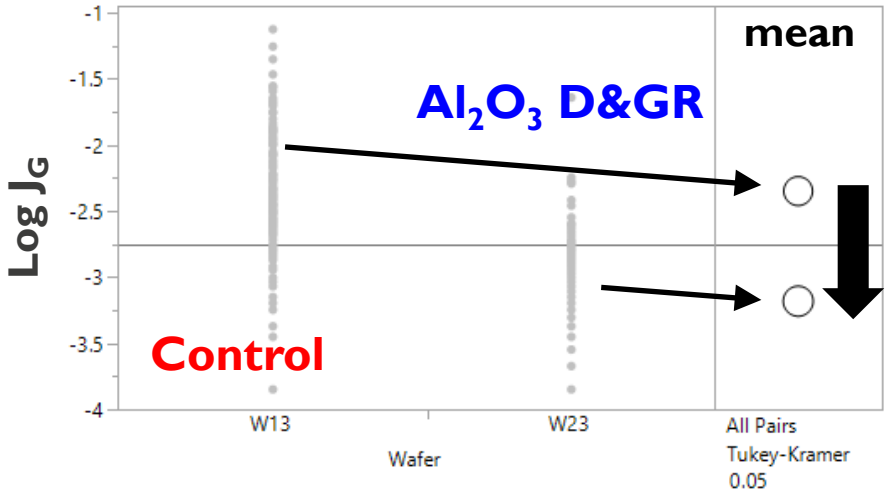
FULL WAFER MAPPING

NMOS, W_{FIN}=20nm, L_G=500nm, gate overdrive 0.6V



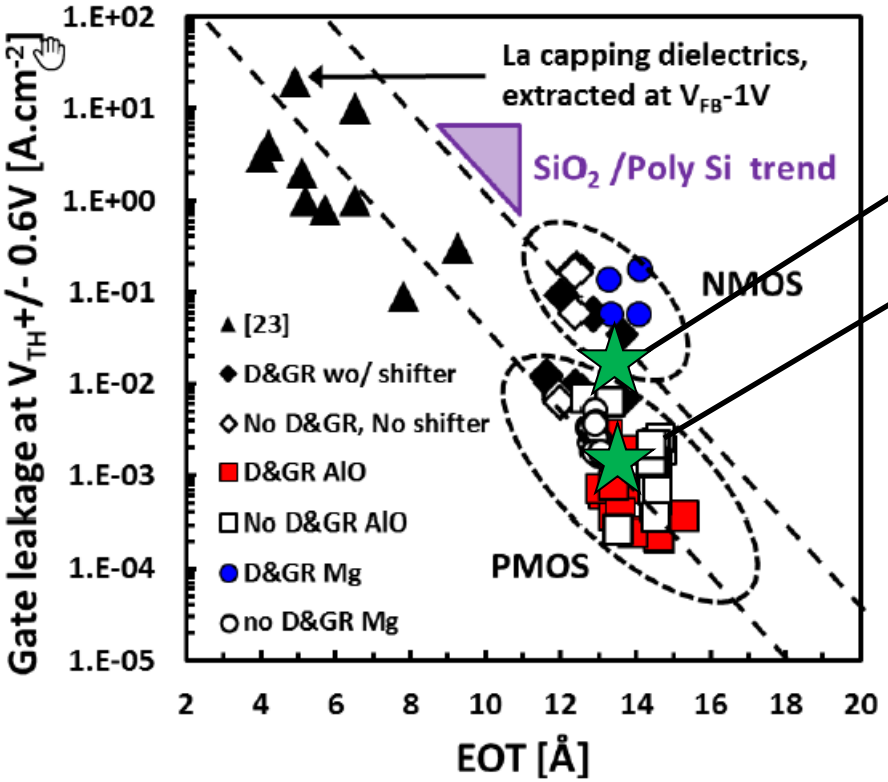
Lot: AL810706

PMOS, W_{FIN}=20nm, L_G=500nm, gate overdrive 0.6V



Means anova: means are significantly different, w/ a small J_G increase for NMOS w/ eWF shifters, while for PMOS w/ eWF shifters J_G is slightly improved.

D&GR FINFET: GATE LEAKAGE



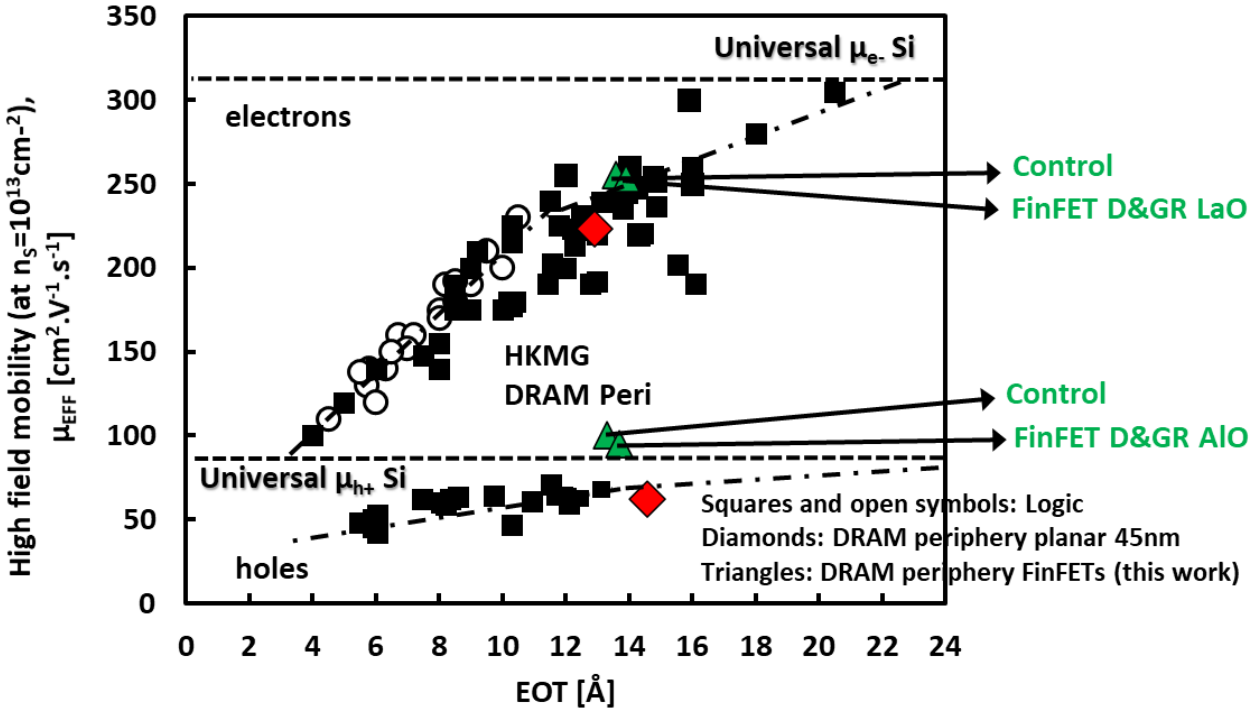
FinFET D&GR LaO

FinFET D&GR Al_2O_3

FinFET D&GR: Consistent gate leakage wrt planar baselines

Note: all points are for planar baselines, expect specified otherwise

D&GR FINFET: LONG CHANNEL MOBILITY



- Little mobility variations between control and D&GR FinFET.
- Note: trade-off to find between obtained eWF shift and mobility degradation, through drive-in anneal thermal budget.

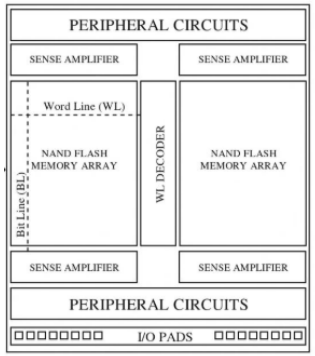
Reliability performance: presentation F205

OUTLINE

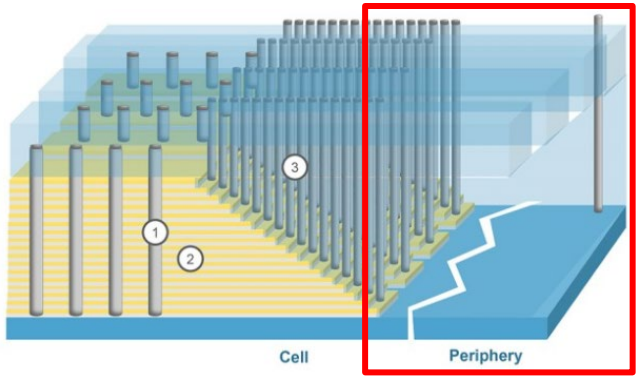
- Introduction
- DRAM peripheral devices
- NAND peripheral devices
- Conclusions

EXAMPLE OF RELEVANT DIMENSIONS IN NAND PERIPHERAL DEVICES

- Logic LV (e.g.: Page Buffer)
  - L_G ~200-300 nm;
  - Gate stack oxide thickness ~ 5 nm;
  - CPP<500 nm;

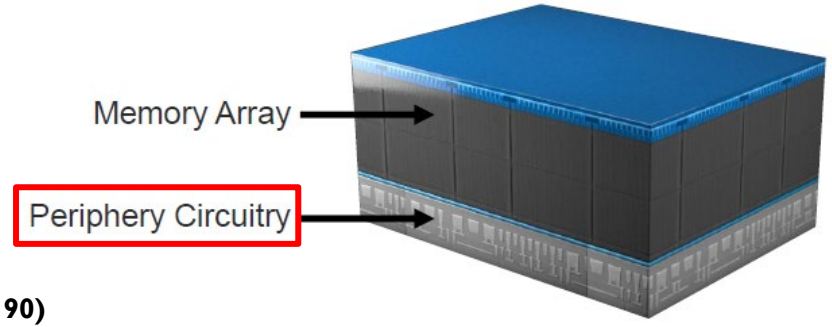


S. Lee et al., ISSCC'18



- Logic HV (e.g.: Word Line Decoder/Switch)
  - L_G ~1000 nm;
  - Oxide thickness >~ 40-50nm

Courtesy A. Spessot

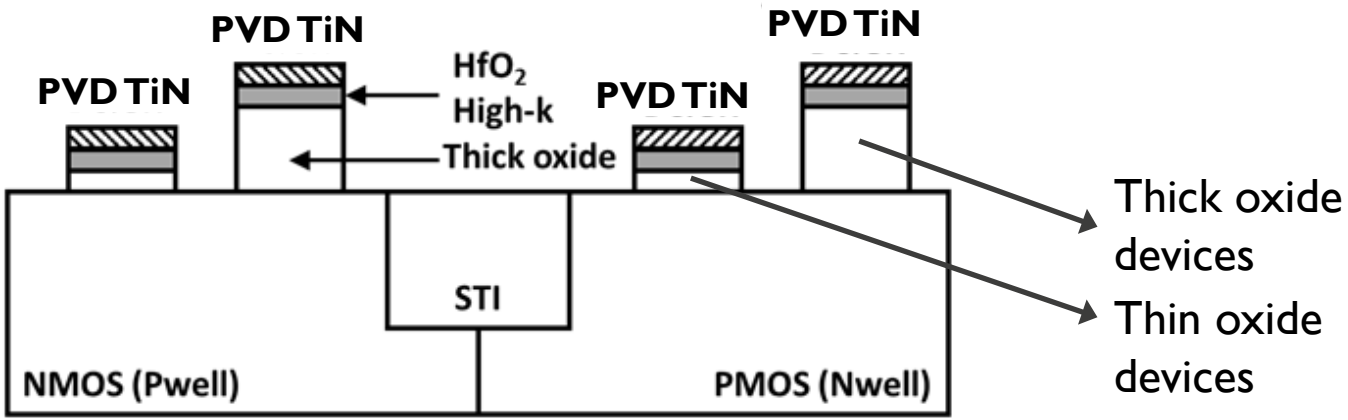


3D NAND memory conceptual view

*** Data extracted from state-of-the-art 3D NAND technology (# layers > 90) reverse engineering report**

https://www.extremetech.com/computing/212108-samsung-announces-new-256-bit-3d-nand-stacked-48-layers-high

INTEGRATION OF HKMG THICK OXIDE DEVICES

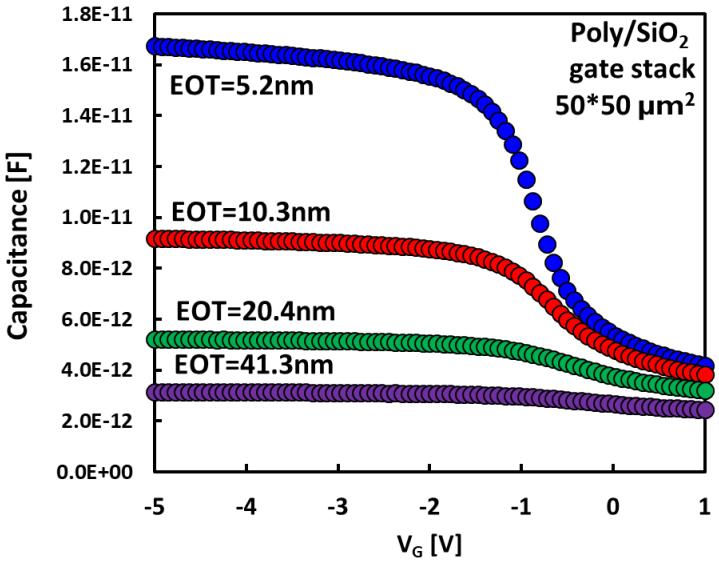


Main objectives:

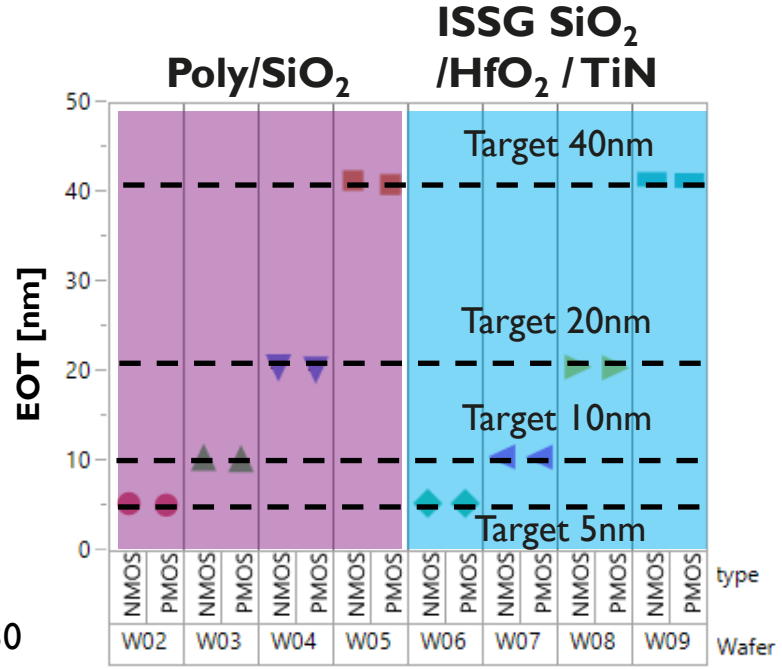
- Assess the effect of using a thick oxide device (5 to 40nm ISSG SiO_2) with a 2nm HfO_2 high-k/5nm PVD TiN Metal gate on top, vs. a purely PolySilicon/SiO_2 gate stack.
- Assess the effect of 'NAND anneal' (1050 °C, 45s) on gate stack and junctions.
- Assess the resistance of current junctions to higher supply voltages.

INTEGRATION OF HKMG THICK OXIDE DEVICES

GATE STACK THICKNESS EOT



Lot: AL904930



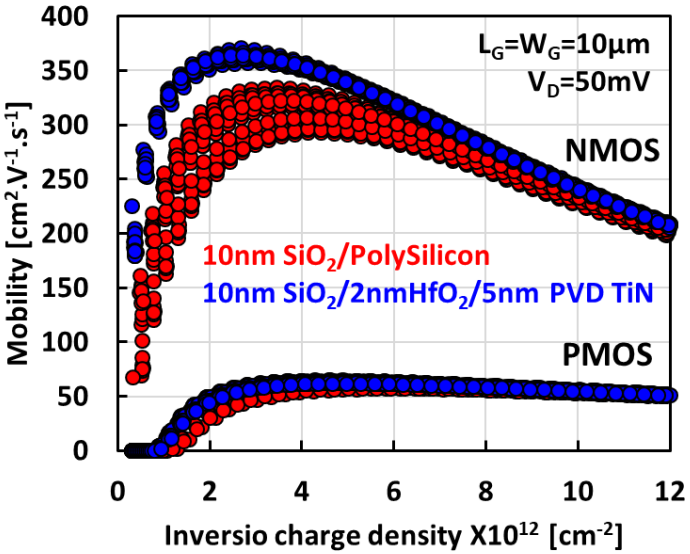
- Good EOT consistency between Poly/SiO_2 and HKMG gate stacks.
- EOT on target.

*Note:'Target 40nm' splits are using RTO SiO_2 iso ISSG.

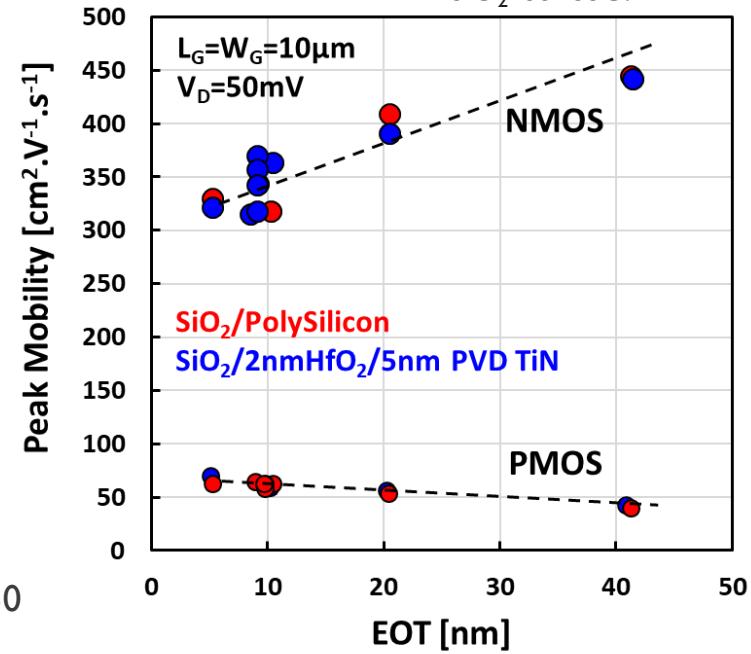
INTEGRATION OF HKMG THICK OXIDE DEVICES

SPLIT CV LONG CHANNEL MOBILITY

*Note:'Target 40nm' HKMG splits are using RTO SiO_2 iso ISSG.



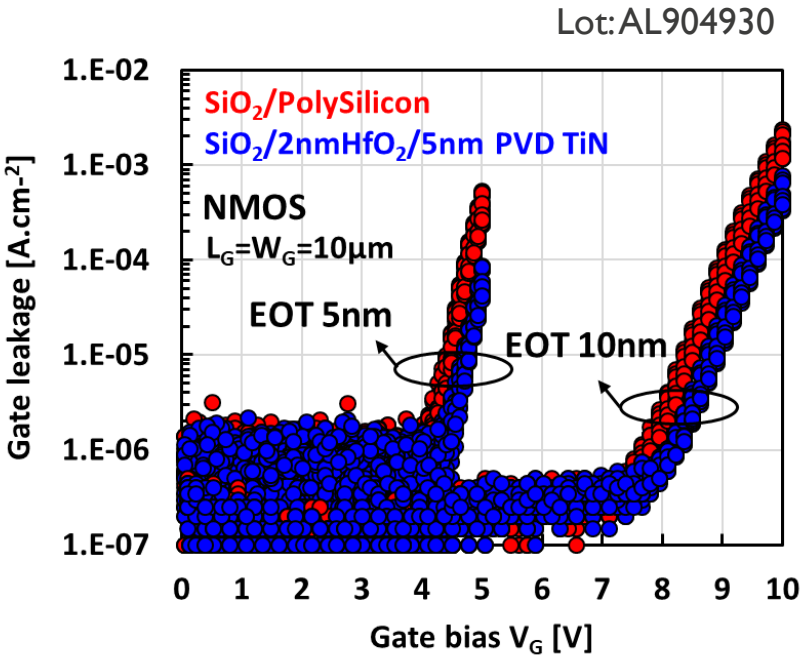
Lot:AL904930

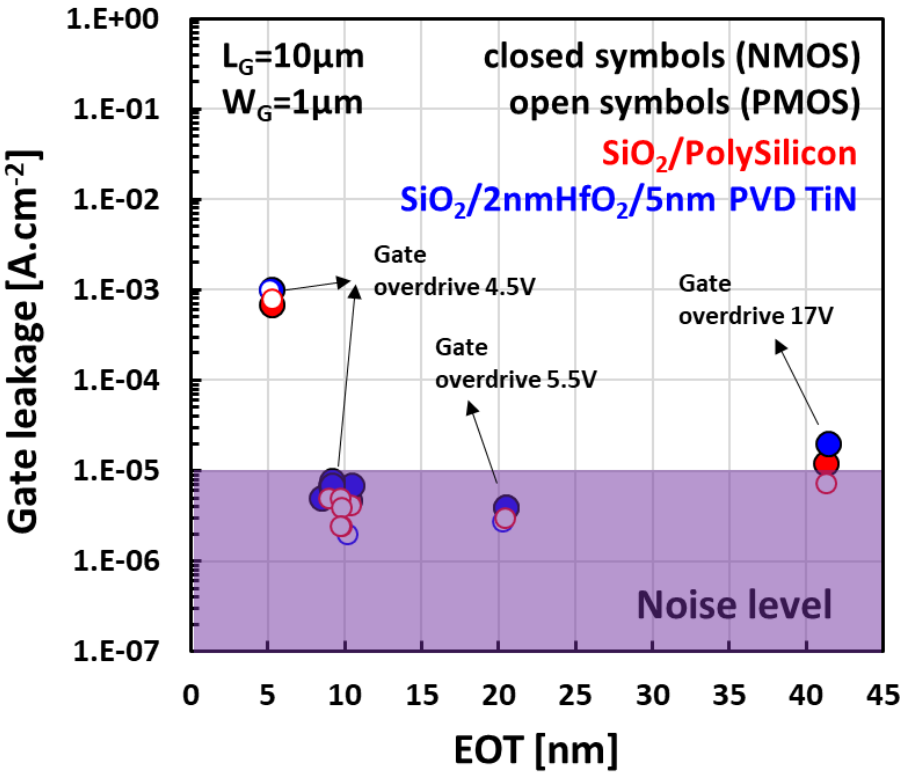


- HfO_2/TiN layers on top of thick SiO_2 have no impact on long channel mobility, for all investigated thicknesses.

INTEGRATION OF HKMG THICK OXIDE DEVICES

GATE LEAKAGE

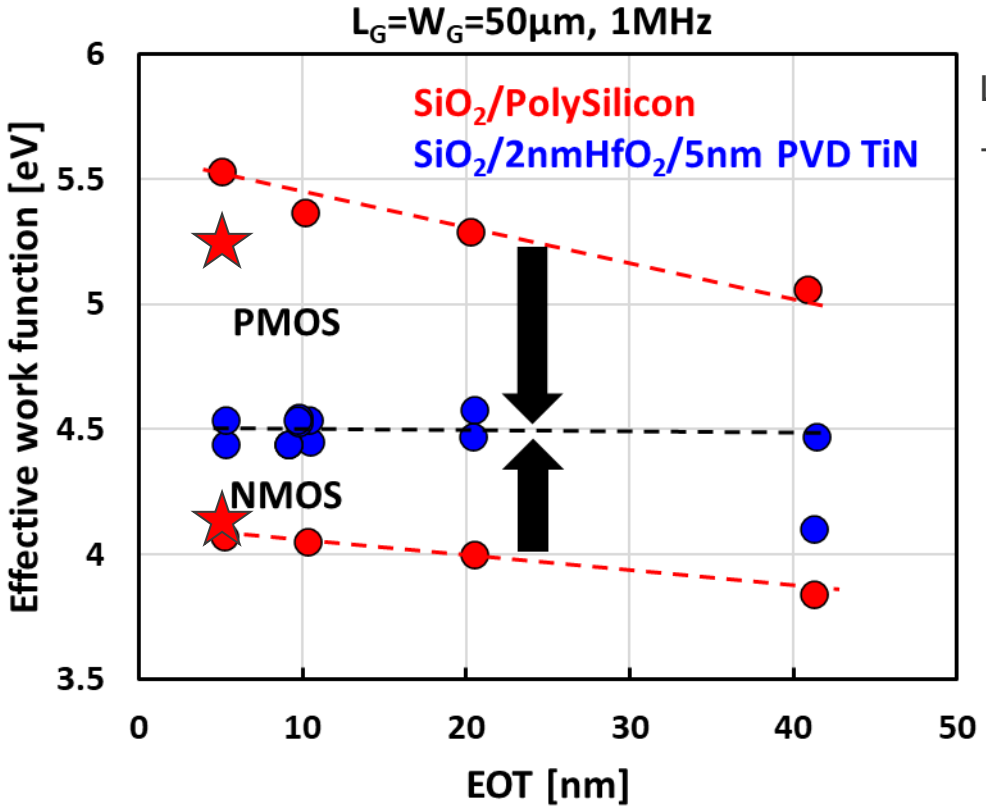




- HfO_2/TiN layers on top of thick SiO_2 have no impact on long channel gate leakage.

INTEGRATION OF HKMG THICK OXIDE DEVICES

EFFECTIVE WORK FUNCTION



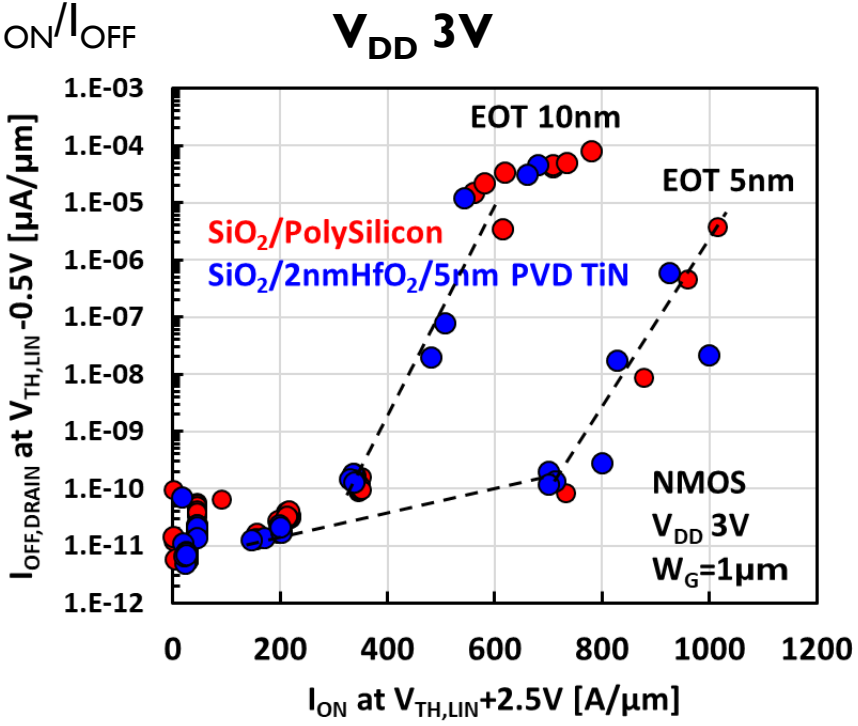
Lot AL904930 (NAND periphery)

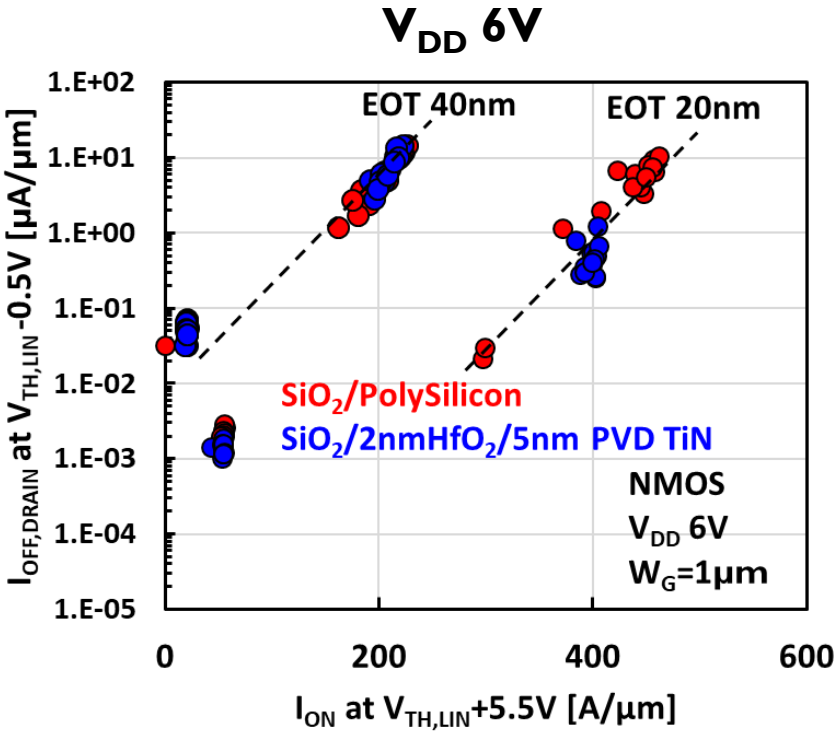
+ Lot AL504455 (DRAM periphery lot, ★)

- HKMG gate stacks: effective work functions move toward mid-gap.

INTEGRATION OF HKMG THICK OXIDE DEVICES

I_{ON}/I_{OFF}





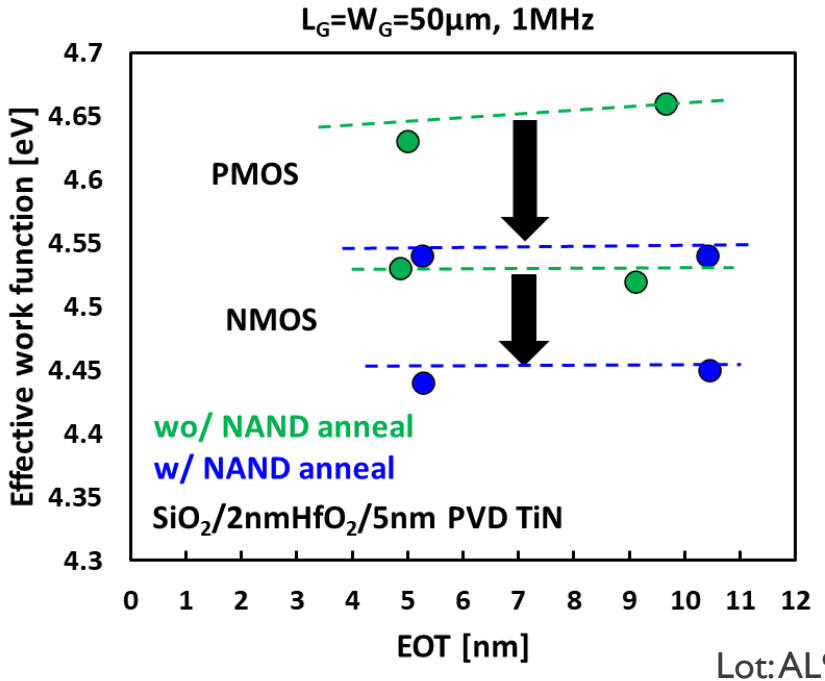
- HfO_2/TiN layers: comparable I_{ON}/I_{OFF} performance

Lot: AL904930

Reliability performance: presentation F205

ASSESSMENT OF NAND ANNEAL IMPACT

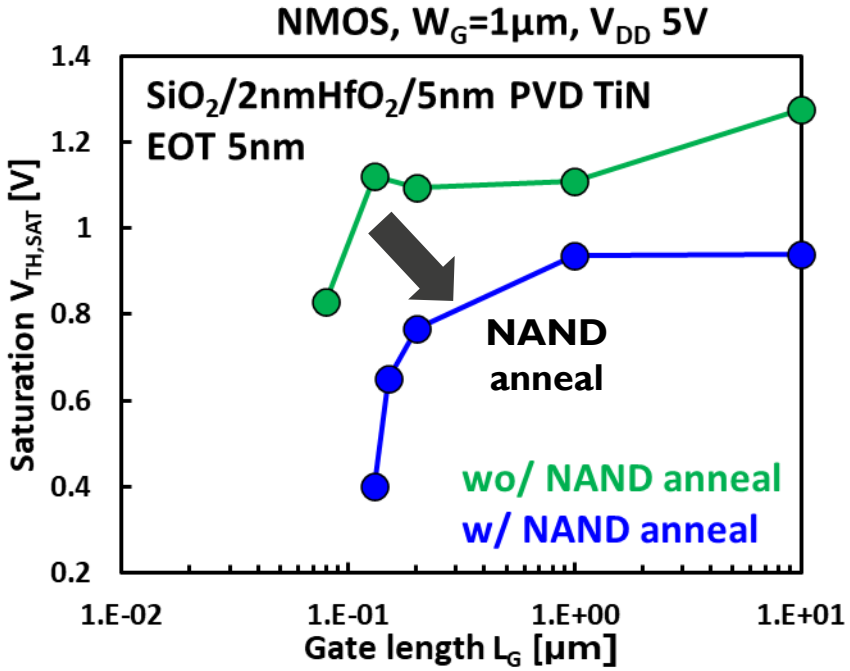
'NAND anneal' = 1050 °C, 45s



Lot: AL904930

- NAND anneal: strong roll-off increase.

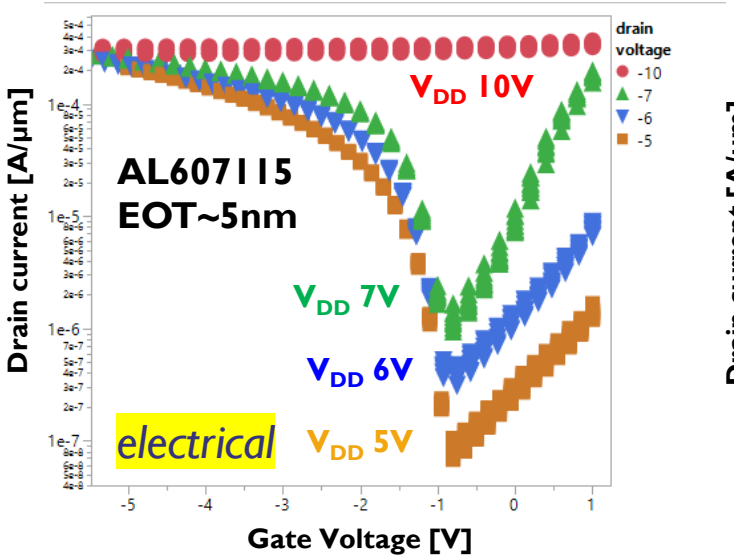
- NAND anneal effect on HKMG gate stacks: effective work function decrease.
- Possible model: passivation of oxide charges.



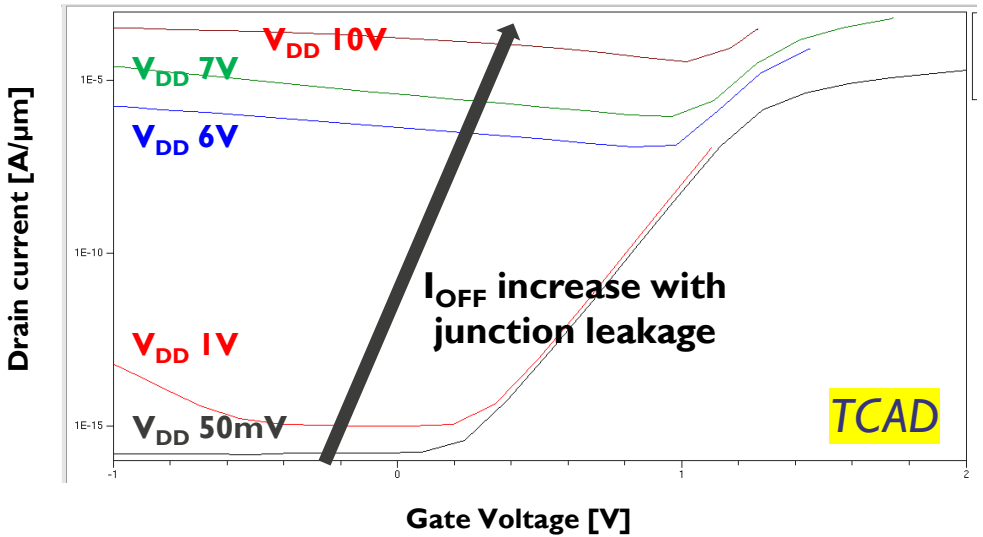
JUNCTIONS - INCREASED SUPPLY VOLTAGE

See also PTW 201910 F304

Junction hard breakdown



Junction leakage

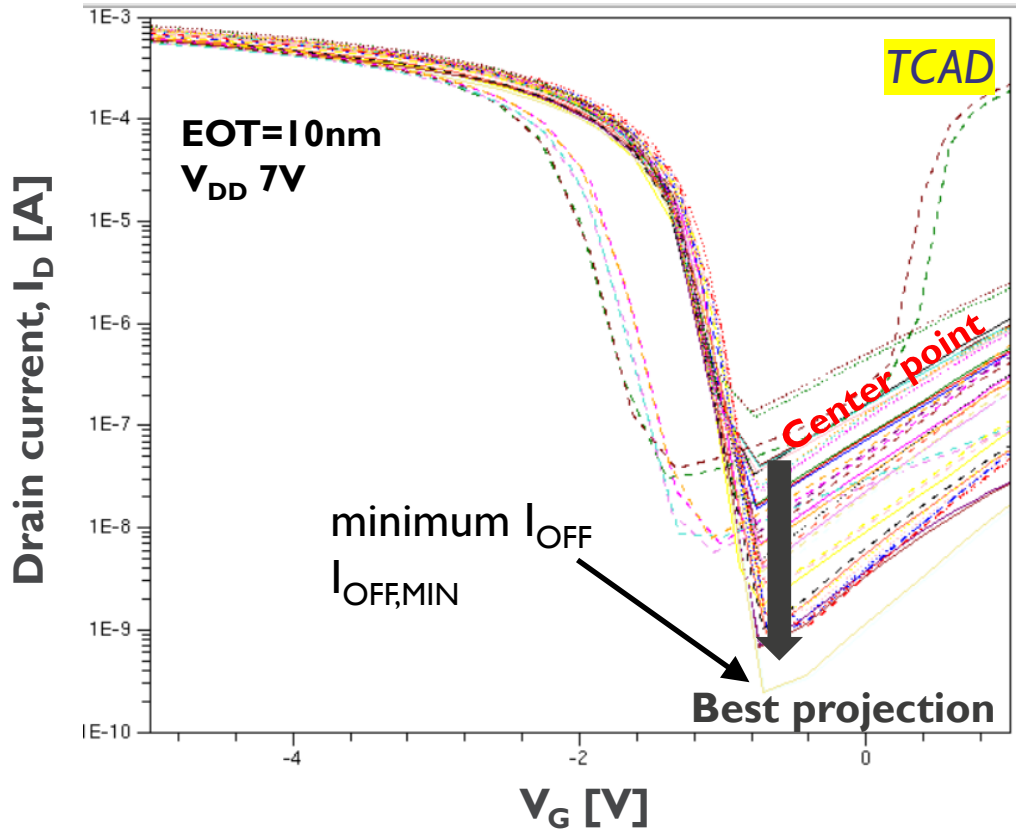


- Readout from previous lots: BKM junctions break above 7V, for both NMOS and PMOS, and junction leakage alone might be is a serious issue.
- Electric field in the junction should be decreased for V_{DD}>7V.

JUNCTIONS - INCREASED SUPPLY VOLTAGE

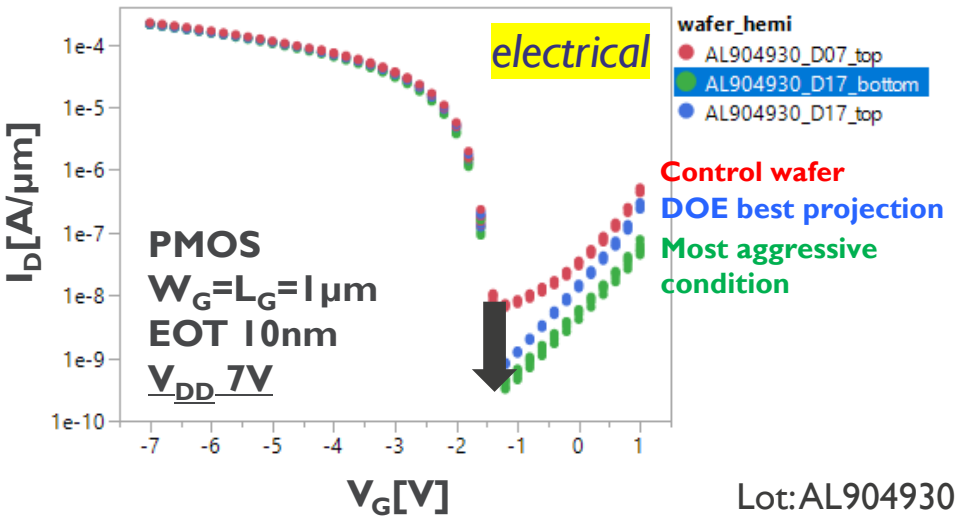
See also PTW 201910 F304

- TCAD based DOE (Parameters: Anti Punch Through dose, LDD dose, HDD dose and energy).
- With doses reduction and implant energy adjustment: 2 decades minimum I_{OFF} reduction reached.
- Proposal for new junctions set.

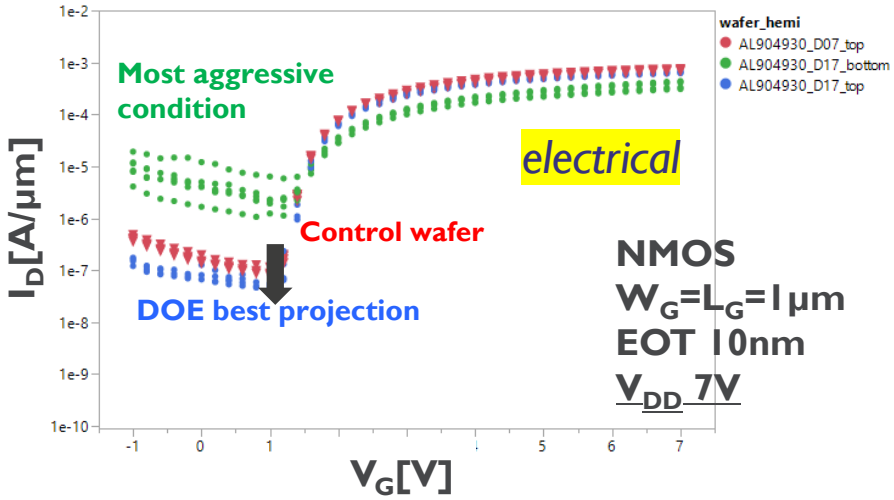


JUNCTIONS - INCREASED SUPPLY VOLTAGE

EXPERIMENTAL READ-OUT



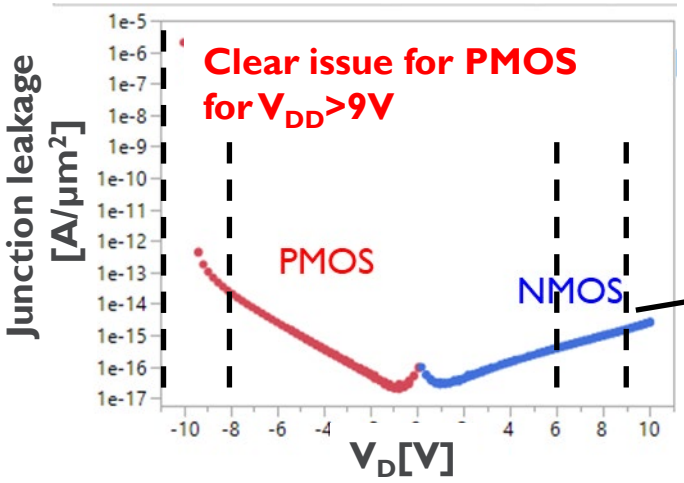
Lot: AL904930

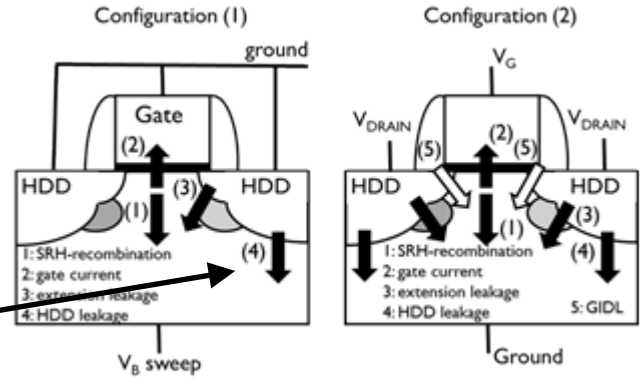


- PMOS: the 1 to 2 decades predicted by TCAD are obtained w/ the modified junction conditions.
- NMOS: marginal improvements.

JUNCTIONS ANALYSIS

Wafer: AL904930 'DOE best guess'



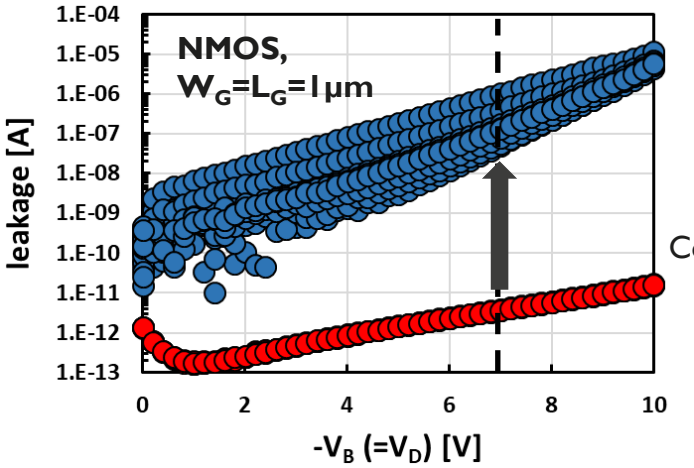


- Components responsible for current in the accumulation regime:
  - Junction leakage (HDD to well leakage (4), HDD/LDD to Halo to well leakage (3)).
  - GIDL (5)

- Probing (4) – **HDD/Well junction leakage.**
- Measurements done on area diodes.
- PMOS junction: high current at V_{DD} 10V, due to avalanche onset.

JUNCTIONS ANALYSIS ON 'DOE BEST PROJECTION'

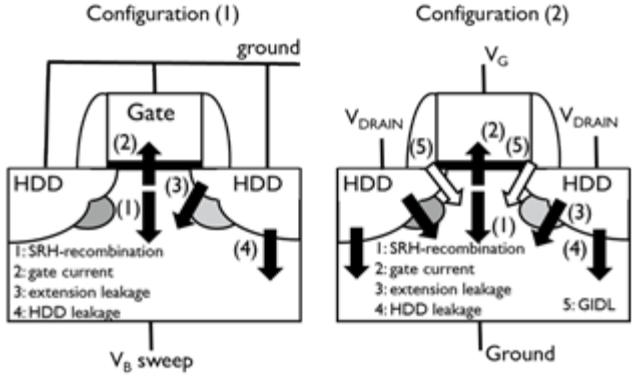
Wafer: AL904930 'DOE best guess'

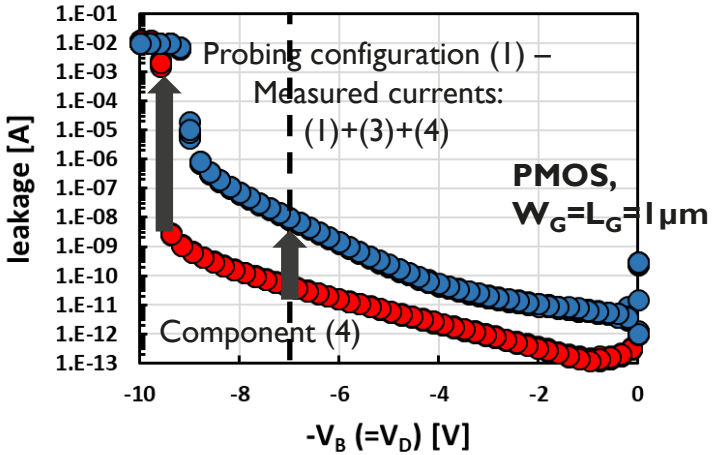


Probing configuration (1) – Measured currents: (1)+(3)+(4)

Component (4)

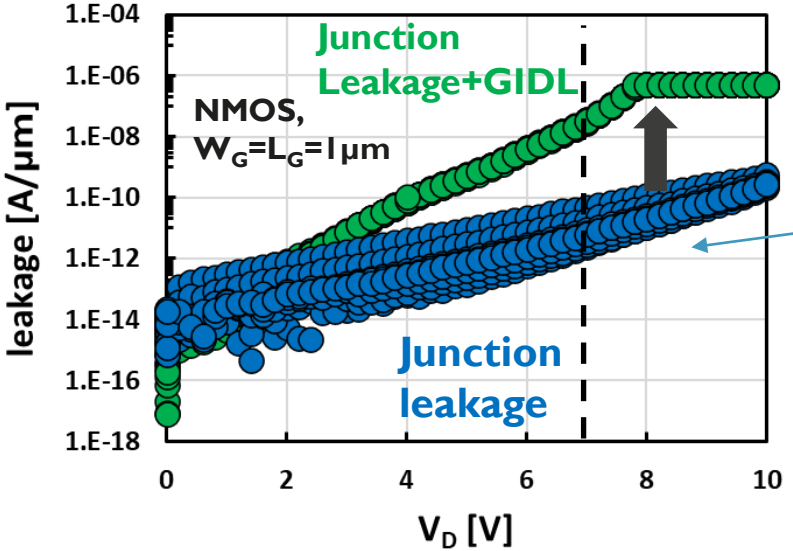
*Note: some currents normalize with surface, others with device width. Current therefore expressed in A for comparison.





- At V_{DD} 7V, NMOS/PMOS HDD to well leakage component (4) << extension leakage.
- Above ~V_{DD} 9V, PMOS HDD to well leakage component (4) becomes the dominant source of junction leakage.

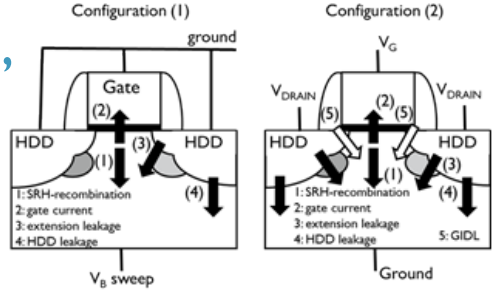
JUNCTIONS ANALYSIS ON 'DOE BEST PROJECTION'

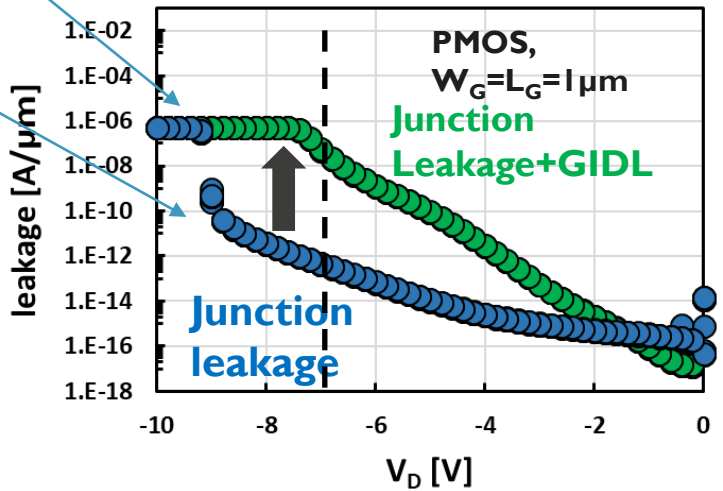


Probing configuration (2) – Measured currents: (1)+(3)+(4)+(5)

Probing configuration (1) – Measured currents: (1)+(3)+(4)

*Note: all currents normalize with transistor width





Wafer: AL904930 'DOE best guess'

- At V_{DD} 7V and above, NMOS/PMOS GIDL is several orders of magnitude higher than junction leakage.
- Overall conclusion: if V_{DD}>7V, GIDL current (NMOS/PMOS) and HDD to well leakage (PMOS) are the key parameters to optimize.

OUTLINE

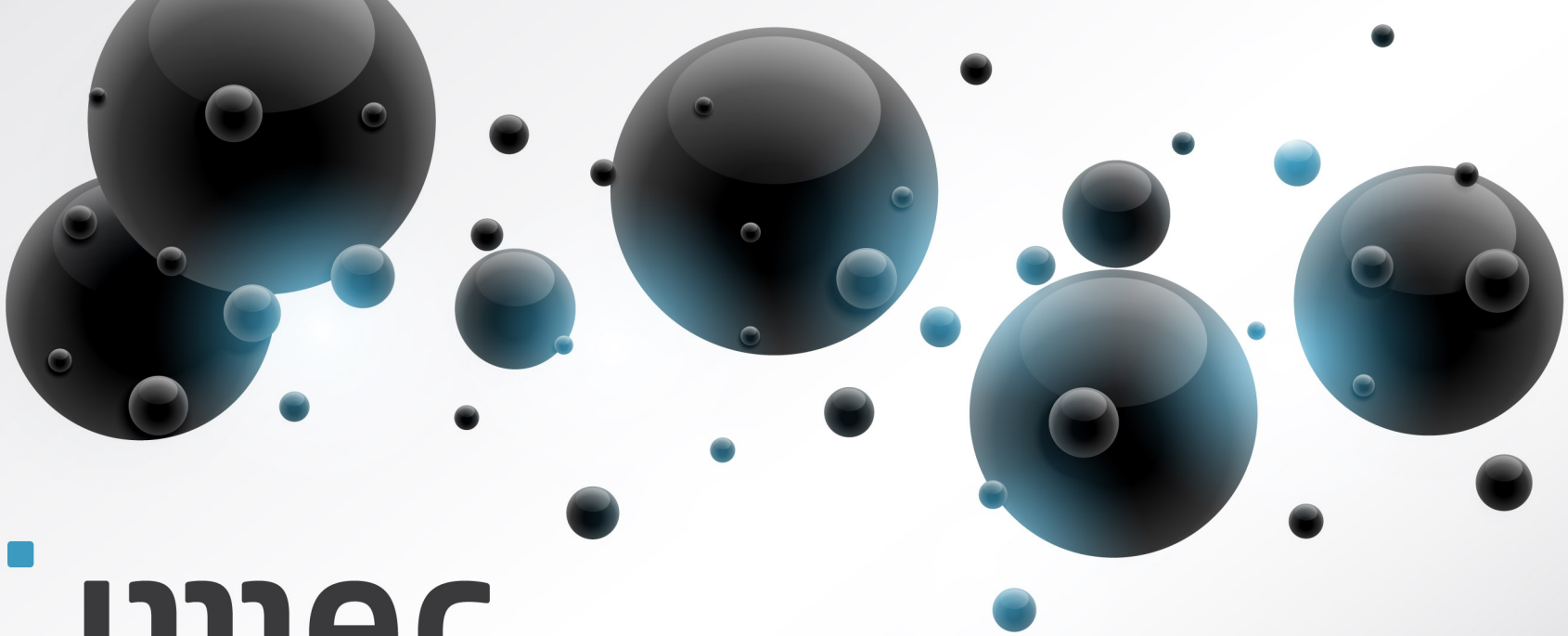
- Introduction
- DRAM peripheral devices
- NAND peripheral devices
- Conclusions

CONCLUSIONS (1/2)

- **DRAM peripheral devices learning:**
  - FinFET with Fin height 80nm and undoped epi S/D + Ion Implantation:
    - Demonstrated current improvement wrt no Epi fins, for no short channel margin degradation.
    - Demonstrated current improvement wrt Fin height 40nm with Epi.
    - Improvements confirmed in I_{ON}/I_{OFF} (normalized per footprint).
  - Demonstration of D&GR FinFET w/ fin height 80nm & PEALD TiN:
    - 110mV V_{TH} shift w/ LaO D&GR, 185mV V_{TH} shift w/ Al_2O_3 D&GR, for no gate leakage/mobility penalty.
    - No Gate leakage penalty wrt to D&GR planar baseline.

CONCLUSIONS (2/2)

- **NAND peripheral devices learning:**
  - Poly/SiO_2 & HKMG (SiO_2 ISSG/HfO_2/PVD TiN) thick oxides integration:
    - Gate leakage/Long channel mobility/I_{ON}(I_{OFF}): no impact of HKMG gate stacks on top of SiO_2.
    - NAND anneal impact: no EOT variation, eWF reduction, and roll-off clearly increased with NAND anneal.
    - Junctions learning:
      - Current BKM junctions work with EOT=5/10nm up to V_{DD}=7V.
      - Cutting extension doses (LDD, HDD, APT, ...) yield some $I_{OFF,MIN}$ reduction, as predicted by TCAD, but not enough to enable high V_{DD}.
      - Decreasing GIDL current is key for the transistor to sustain higher supply voltages.
      - HDD to Well leakage is also very high in PMOS for V_{DD}>9V.



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