imec

partner
technical
week

F200 MEMORY PERI

ALESSIO SPESSOT

GLOBALFOUNDRIES intel KIOXIA Western Digital. SAMSUNG HLMC SK hynix tsmc Micron SONY socionext QUALCOMM HUAWEI SMIC

LOGIC DEVICES

F200

NOW IN COURSE:

MEMORY PERI ROADMAP FOR DRAM AND NAND

ALESSIO SPESSOT

THIS PRESENTATION IS OPEN TO:

CORE PARTNERS, APPLE, SOCIONEXT

AMAT, ASM, BASF, SCREEN, KLA-TENCOR, KULEUVEN, LAM, SYNOPSYS, RIBER, COVENTOR, NOVA, THERMOFISHER, PARK SYSTEMS, SOITEC, KURITA, KOKUSAI, SILTRONIC, AIR LIQUIDE, EBARA, GLOBALTCADSOL, VERSUMMATERIALS, HPSP, ASML, MERCK, HITACHI, TEL, SHINETSU

imec partner technical week

TECHNOLOGY DRIVERS FOR MEMORY PERI PLATFORM

- DRAM

  Strategic Goal: power reduction (mobile application), high performance (graphic market/AI)

  - Development of **HKMG FF** platform (thin oxide, thick oxide) / **reliability** concern for **planar** and **FF**

- SCM:

  Strategic Goal: power and performance as close as possible as DRAM (power reduction, high performance), enablement of **selector** bias

- NAND:

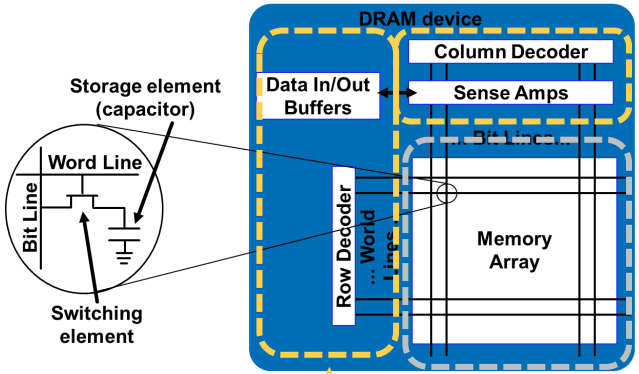
  Strategic Goal:

  - 1) power/performance benefit improvement on **I/O**;
  - 2) **area** reduction

DRAM

TRANSISTORS USED IN DRAM MEMORY CHIP

- In DRAM technologies, transistors are used as access devices and in the peripheral circuitry.
- Peripheral transistors serve several purposes: address decoders, sense amplifiers, output buffers, control circuitry



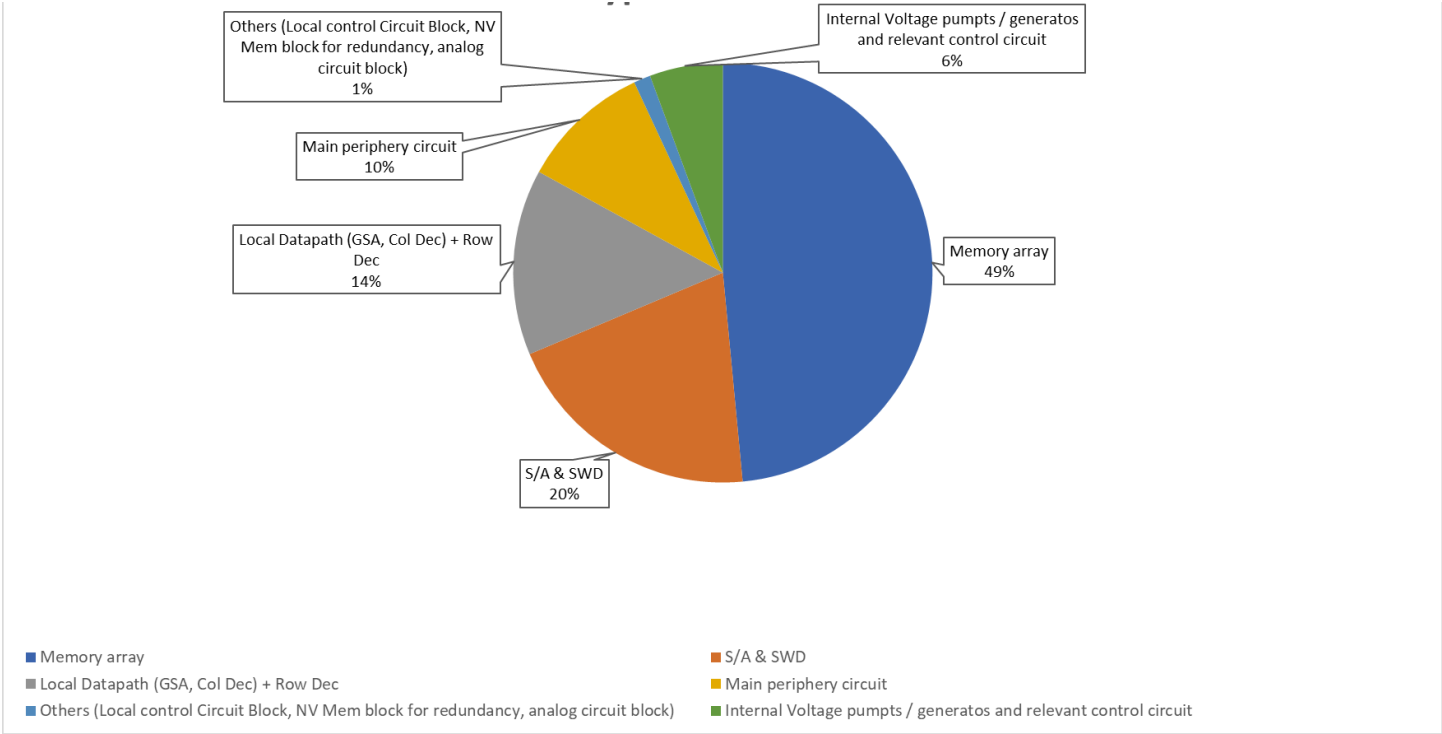
	Cell Transistor	Periphery Transistor		
Type of transistor	**Access Device**	**Regular Logic Transistor**	**Sense/Amplifier**	**Row Decoder (SWD)**
Applied Voltage	VPP (~3.0V)	VDD (1.5V)	Vcore (1.0V~1.3V)	VPP (~3.0V)
Gate Oxide thickness	THICK (>=6nm)	thin (<2.5nm)	thin (<2.5nm)	THICK (>=5nm)
Gate Length	Determined by WL pitch & vertical depth	Larger than Cell minimum dimensions; determined by Ion/Ioff specs and SCE (<50nm)	Maximize Lg within BL pitch (e.g.: ~100nm)	Maximize Lg within WL pitch (e.g.: ~120nm)
Key features/Attention point	Junction Leakage Short Channel Margin	Speed Short Channel control	Local Variation; low Vth	Reliability

Reference value for DDR3, DRAM 20 nm node; Adapted from S. Y. Cha, IEDM 2011 short course;

- Additional customized requirements are needed, diversifying them from standard logic flow:
  - **Low power/low leakages** (low I_{OFF} and J_G mandatory)
  - Compatibility of fabrication process (gate stacks, silicide, junction scheme) with the **prolonged thermal treatment** needed in a DRAM process (typically several hours above 600°C).
  - **Low(err) cost** (than advanced high-performance devices)

AREA BREAKDOWN EXAMPLE (GDDR6)

NON MEMORY AREA > MEMORY AREA



AUTOMOTIVE DRIVES HIGH PERFORMANCE DRAM MARKET

ADVANCED DRIVER-ASSISTANCE SYSTEMS (ADAS), IN-VEHICLE INFOTAINMENT (IVI)

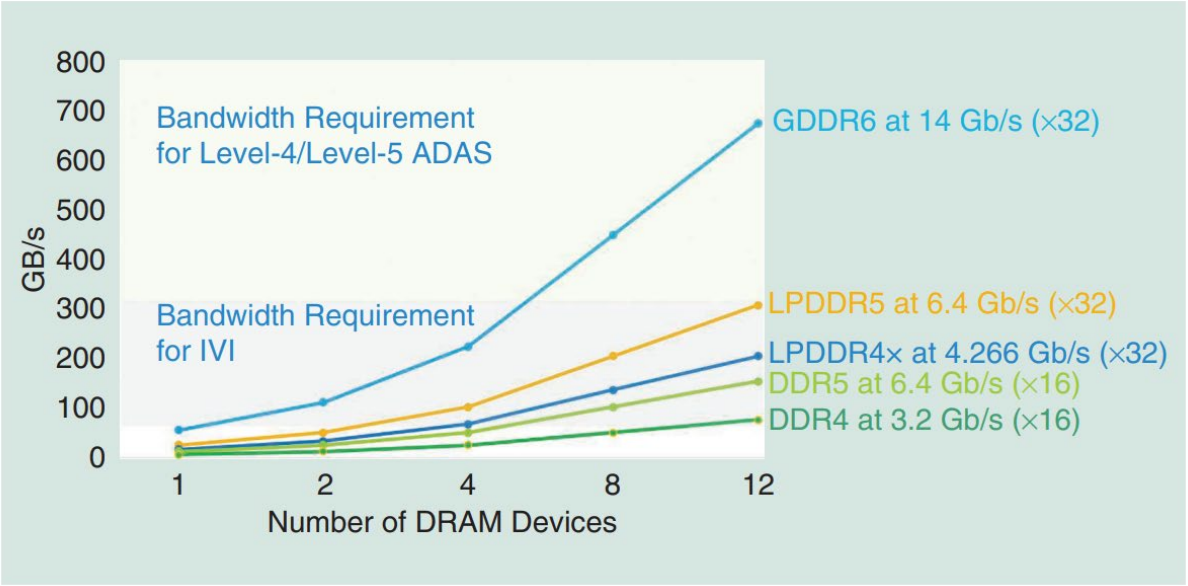


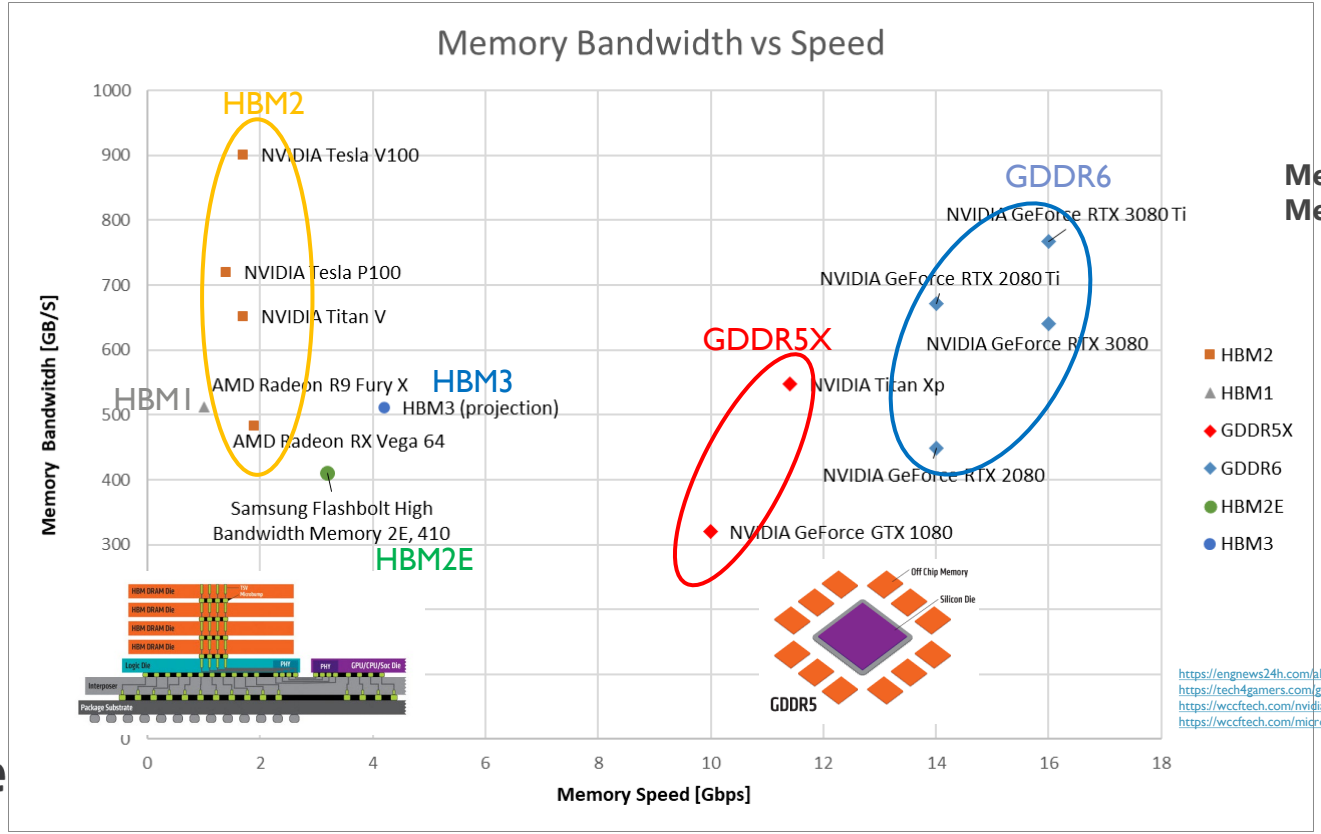
FIGURE 18: The system bandwidth requirements of autonomous and semiautonomous ADASs and IVI.

memory bandwidth requirements:

- in-vehicle infotainment (IVI) can demand 50- to 300-GB/s
- advanced driver-assistance systems (ADASs): 300-GB/s to 1-TB/s

MEMORY BANDWIDTH VS SPEED

HIGH-END GAMING, VIRTUAL REALITY, CRYPTOCURRENCY MINING AND ARTIFICIAL INTELLIGENCE (AI) REQUIRES HIGH PERFORMANCE MEMORY



Memory Bandwidth = (Effective Memory Clock x Bus Width) / 8

https://engnews24h.com/all-details-on-nvidia-ampere-and-rtx-3000-series/
https://tech4gamers.com/geforce-rtx-3080-ti-would-be-40-faster-than-geforce-rtx-2080-ti/
https://wccftech.com/nvidia-quadro-rtx-turing-gpu-samsung-gddr6-memory/
https://wccftech.com/micron-gddr6-memory-20-gbps-speeds/

PERFORMANCE AND POWER

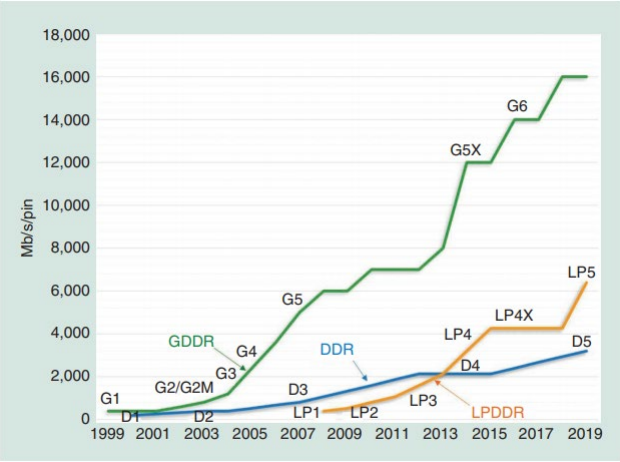


FIGURE 2: The DRAM per-pin bandwidth history for the DDR family.

High performance path: GDDR5 reaches 8Gbps, increasing energy/bit vs LPDDR4

Nagashima, JEDEC Aug 2018

- GDDR5 can reach 8000MBPS, about x2 faster than the LPDDR4
- Energy/bit is higher in GDDR5 than in LPDDR4

https://www.jedec.org/sites/default/files/Osamu_Nagashima_Mobile_August_2016.pdf

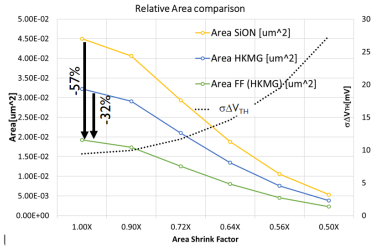
MULTIPLE HKMG PLANAR SOLUTION DEVELOPED IN IMEC

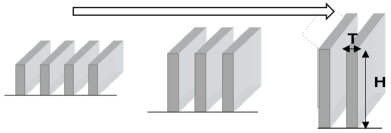
	NMOS									PMOS					
	MIPS						D&GR		RMG	MIPS			D&GR	SiGe	RMG
	TiN	TiN + As I/I	La above	La below	TiN\Mg\ TiN	TiN\Mg\ TiN + As I/I	La	TiN\Mg\ TiN	TiN\TiAl \Ta\TiN	TiN	Al2O3 below	Al2O3abo ve	Al2O3 D&GR	SiGe + Si Cap	TiN\TiN
Low VTH thermally stable?	NO	Partial	Yes	Yes	Yes	Yes	Yes	Yes	Yes	NO	Yes	Yes	Yes	Yes	Yes
imec Demo Level															
imec capacitor	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
unichannel device	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	NO	Yes	Yes	Yes	Yes	Yes	NO
CMOS device	Yes	Yes	Yes	NO	Yes	Yes	NO	NO	NO	Yes	Yes	Yes	Yes	NO	NO
CMOS device with RO (un optimized)	Yes	Yes	NO	NO	Yes	Yes	NO	NO	NO	Yes	Yes	Yes	Yes	NO	NO
CMOS device with RO (optimized)	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO

Illustration purpose only

FINFET FOR DRAM/SCM PERI VALUE PROPOSITION

~50% area saving in the analog part



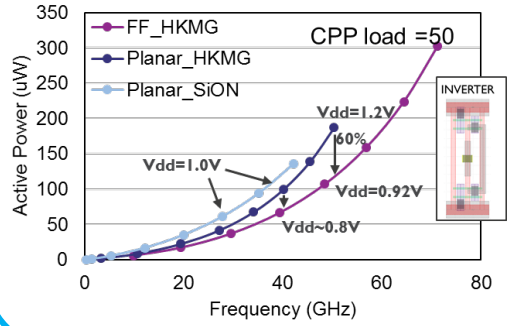


W(FinFET) = (2H+T) * Fin number

$$\partial \Delta Vt = \frac{Avt}{\sqrt{W * L}}$$

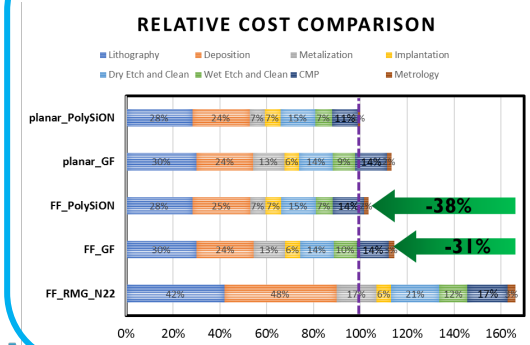
Sense/Amp benefit FinFET HKMG can enable ~50% area gain due to improved mismatch and taller fin

AC Power/Performance improvement (RO level) wrt planar



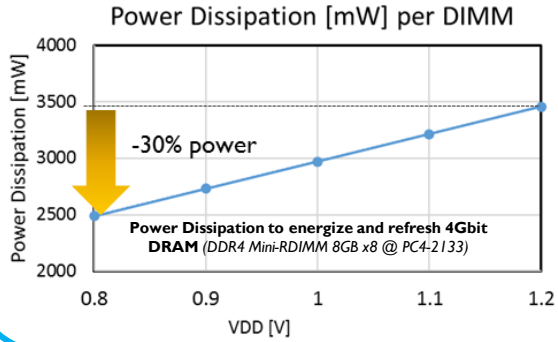
FinFET HKMG device outperform planar HKMG (60% less power at similar performance of HKMG planar with further VDD reduction down to 0.8V)

Cost effective flow wrt High Performance Logic



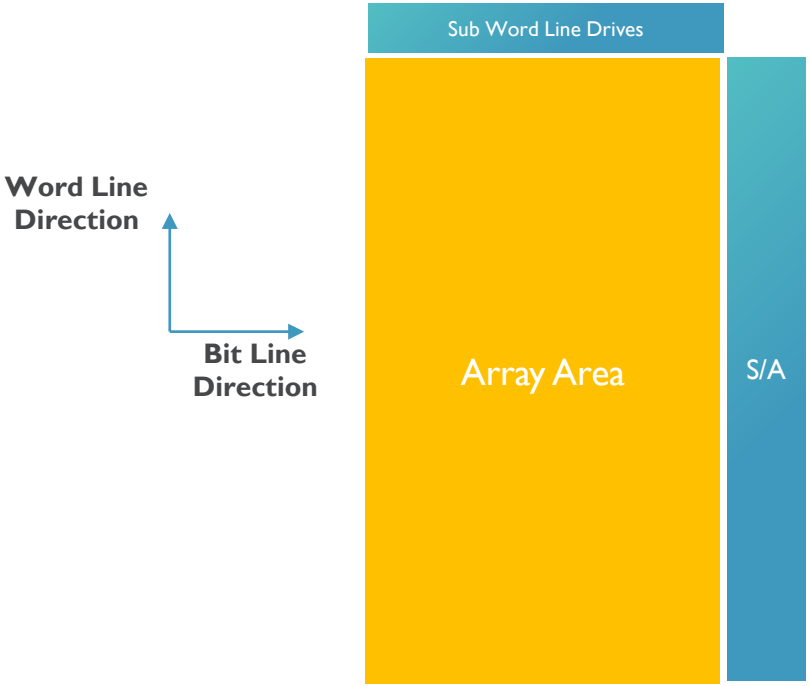
Proposed FinFET flow remains more cost effective than logic flow at corresponding dimensions

Power saving at system level wrt planar



FinFET HKMG can enable 30% power saving at DIMM level wrt planar SiON devices by reducing internal VDD down to 0.8V)

FINFET: AREA SAVING SENSITIVITY STUDY (S/A PART)



Sub Word Line Drives (thick oxide): 3 MOSFETs (2N, 1P)

S/A (thin oxide): ~9 MOSFETs
7N (2 S/A + 3 Equalizer + 2 CSL) + 2P (2 S/A)

SCM

PERIPHERY DEVICES REQUIRED BY STORAGE CLASS MEMORY

HIGHER BIAS COMPATIBLE DEVICES REQUIRED

- XP transistor needs to deliver power/performance similar to DRAM, including also an option for 7.5-8V bias required to row decoder ➔ different requirement for thicker gate stack needed wrt DRAM

	Cell Transistor	Periphery Transistor		
Type of transistor	**Access Device**	**Regular Logic Transistor**	**Sense/Amplifier**	**Row Decoder (SWD)**
Applied Voltage	VPP (~3.0V)	VDD (1.5V)	Vcore (1.0V~1.3V)	VD~7.5/8
Gate Oxide thickness	THICK (>=6nm)	thin (<2.5nm)	thin (<2.5nm)	>= 15nm
Gate Length	Determined by WL pitch & vertical depth	Larger than Cell minimum dimensions; determined by Ion/Ioff specs and SCE (<50nm)	Maximize Lg within BL pitch (e.g.: ~100nm)	Maximize Lg within WL pitch (e.g.: ~120nm)
Key features/Attention point	Junction Leakage Short Channel Margin	Speed Short Channel control	Local Variation; low Vth	Reliability

DRAM:

- Thinner gate stack option: "Tall" Finfet HKMG Gate First , with EOT target ~ 1.4 nm and good mismatch
- Thicker Gate stack option: increased EOT ~ 5nm and longer channel needed (Lg>~100nm) for SWD ➔ HKMG FF with thicker EOT and optimized junctions is considered

SCM:

- Thinner gate stack option: "Tall" Finfet HKMG Gate First , with EOT target ~ 1.4 nm and good mismatch (as DRAM)
- Thicker Gate stack option: increased EOT ~ 5nm and longer channel needed (Lg>~100nm) for SWD ➔ HKMG FF with thicker EOT and optimized junctions is considered

COMPHY SETUP

- N_D=1e15/cm^3
- WF=4.34eV (n-type)
  - note: doping minimized to suppress V_{th0} depends on t_{ox} due to the depletion charge
  - For this setup: V_{th0} ~ – 0.649 V – 0.004 * t_{ox}[nm]
- 2nm HfO_2 (k=24) on top of SiO_2 of varying thickness

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_{ox}}$$

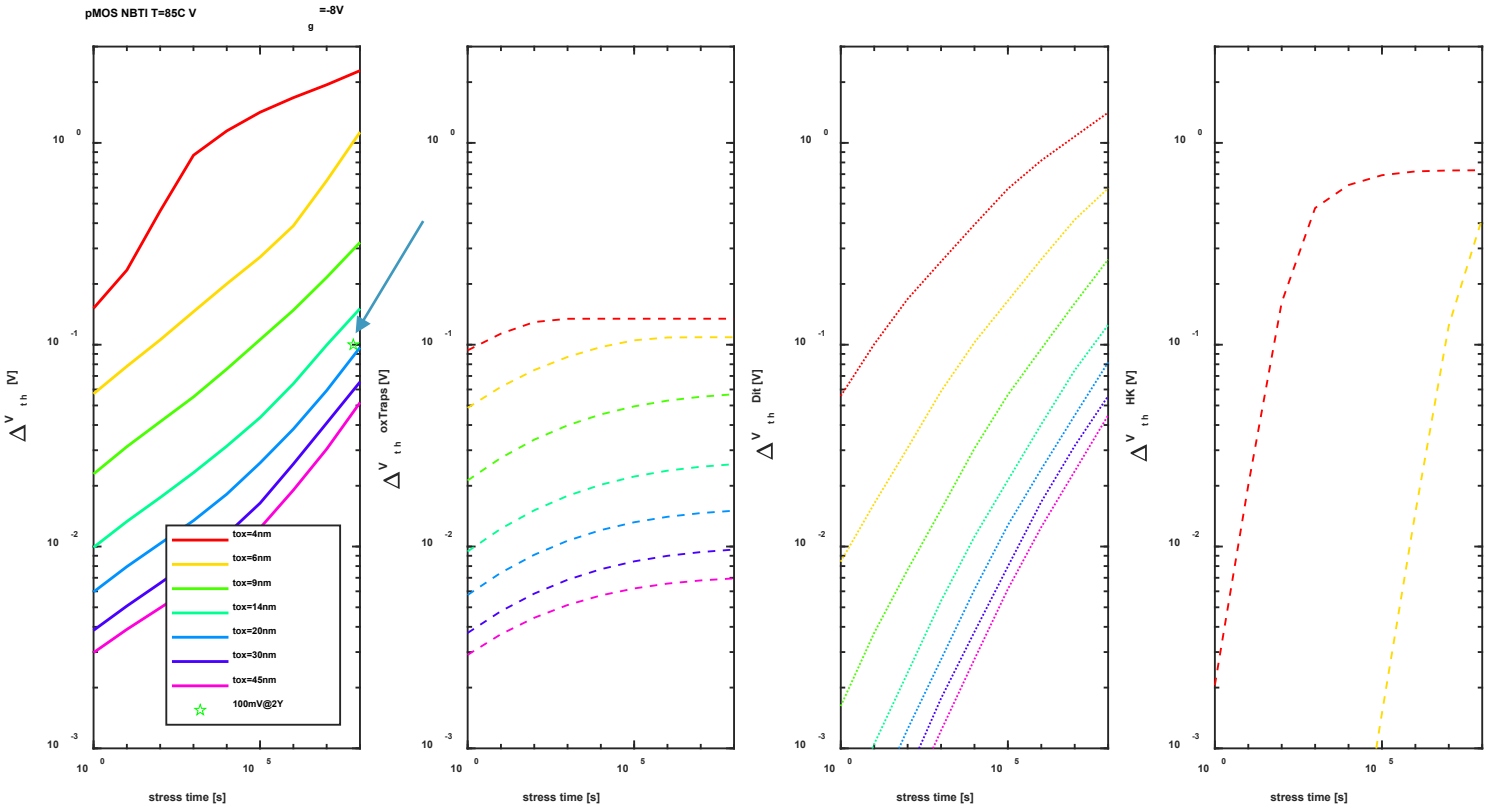
Defect models (as calibrated on Memory Peri HKMG stack (EOT~5nm, HKMG) [G. Rzepa, MR18])

- Hole trap defect band only ***across first 0.6nm of SiO_2 (defective transition layer)***
- Hole trap in HfO_2
- Double-Well model for interface state generation
  - Disclaimer: model calibrated on stack with t_{ox}=5nm → D_{it} becomes the dominating for even thicker tox ➔ accuracy might be limited

pMOS NBTI, T=85C, V_{DD}=8V

t_{ox} slightly thicker than 14nm can meet NBTI reliability target

Lifetime criteria defined as Vth shift of 100mV in 2y @85C



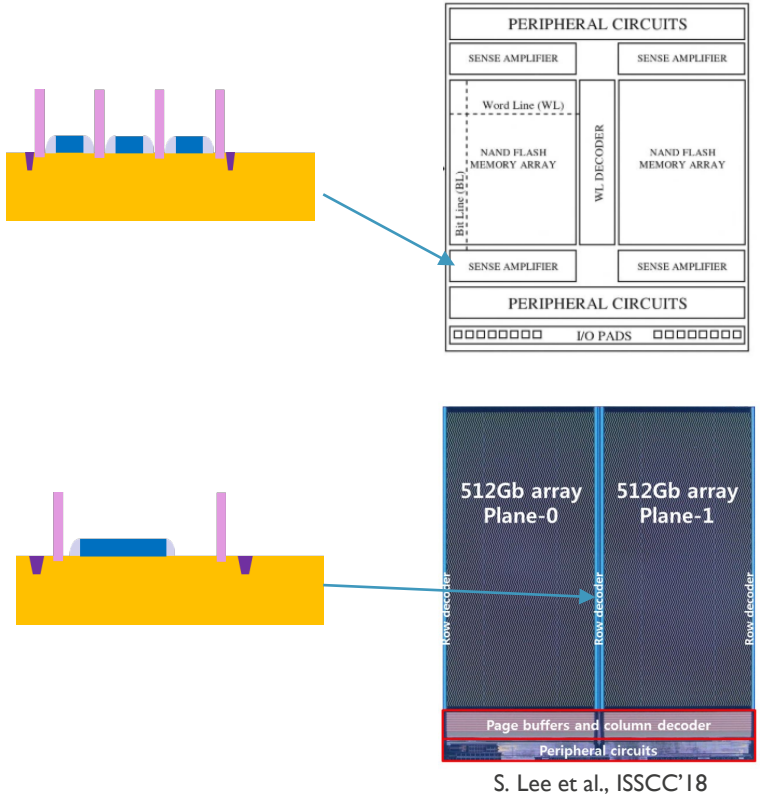
hole trap in HfO_2 has minor/negligible contribute for a thick t_{ox}

NAND

NAND PERIPHERAL DEVICES & ASSUMPTIONS USED

EXAMPLE OF TRANSISTOR USED

- Logic MV (e.g.: Page Buffer)
  - Lgate <200 nm;
  - Gate stack oxide thickness ~ 5 nm;
  - CPP<500 nm;
- Logic HV (e.g.: Word Line Decoder)
  - Lgate ~1000 nm;
  - Oxide thickness >~ 40-50nn

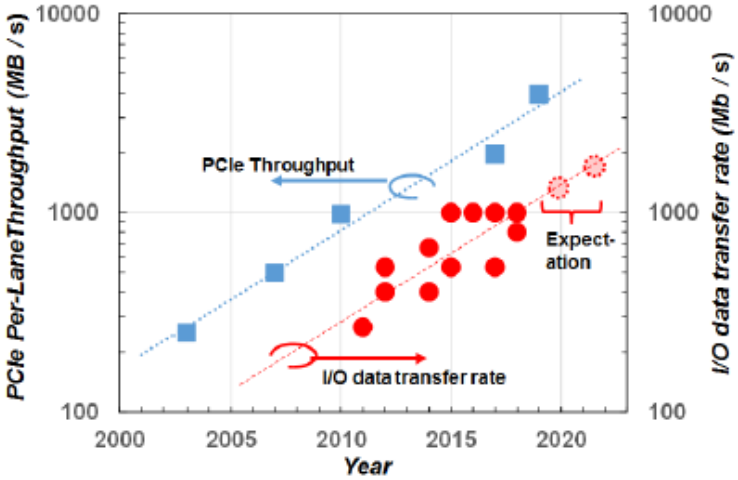


S. Lee et al., ISSCC'18

Data extracted from state-of-the-art 3D NAND technology (# layers > 90) reverse engineering report

SPEED OF NAND I/O EXPECTED TO INCREASE IN THE NEXT GENERATION PRODUCTS

Motivation



Satoshi Inaba "3D Flash Memory for Data-intensive Applications" pp. 1-4, IMW 2018

Major challenges:

- Power consumption
- Power delivery to the drivers
- Noise margin
- Frequency of operation

Objective:

- Define the I/O topology and optimal device specs (*Gate length, Channel width, Gate oxide thickness, Supply voltage*) to meet the high speed requirement (~2GBPS data rate)
- Define the guidelines for IC interface (*pad, bondwire, pin, Transmission line RLC*)

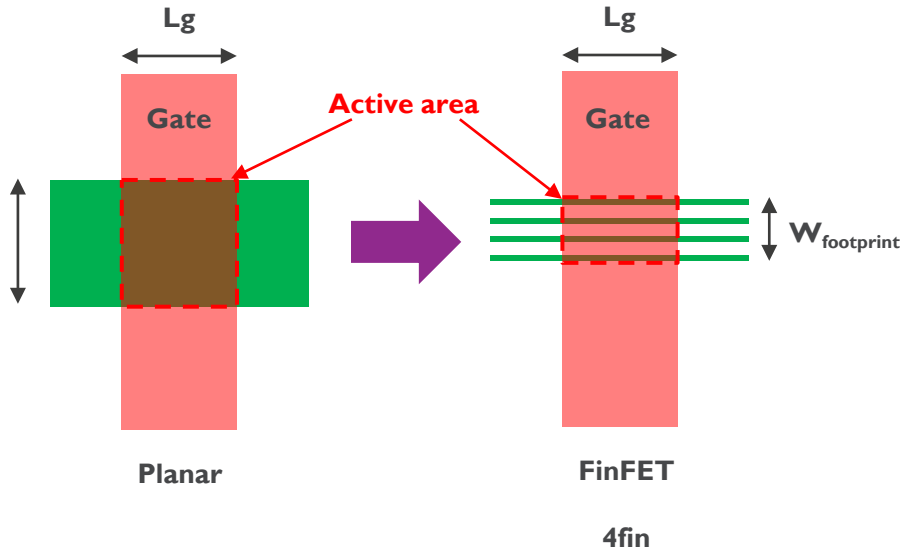
Methodology:

- DoE of device based on compact model
- Determination done analyzing the *eye-diagram opening*
- Benchmark of *different sensing schemes*

KEY QUESTION

Is there a way to reduce the area impact of HV devices (EOT=40nm) in a NAND memory chip, without compromising performance (including the MV PPA)?

- Poly-SiO_2 tall FinFET cointegrating Low and High Voltage is under exploration
  - **Pros**: significant area reduction (~50% on HV
  - **Cons**: potential detrimental impact by larger parasitic capacitance of FinFET (which can be compensated by better electrostatic channel control)

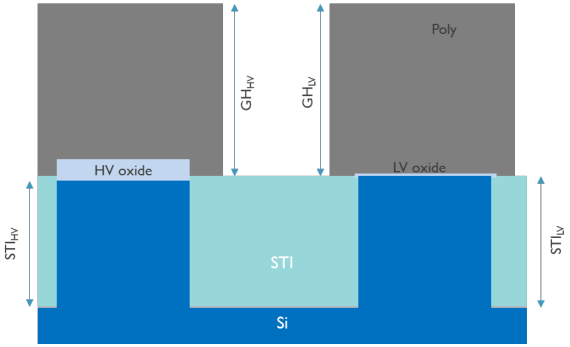


NAND: OPTION 1 (FF)

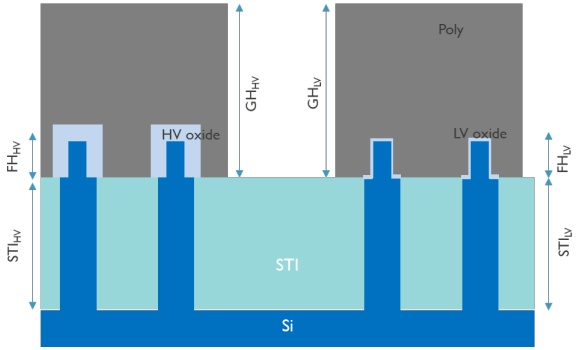
NAND: OPTION 2 (PLANAR HKMG)

CONSIDERED INTEGRATION OPTIONS

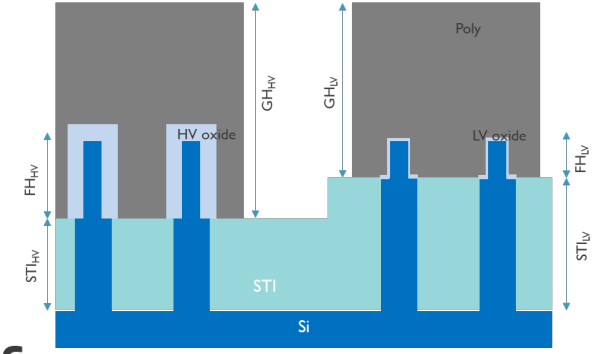
PLANAR HV + PLANAR LV



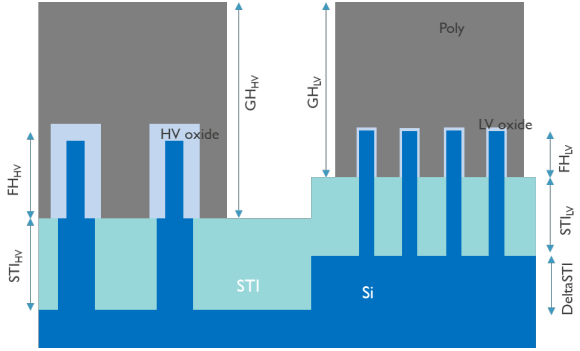
FF SP HV + FF SP LV (SAME FH)



FF SP HV + FF SP LV (DIFFERENT FH)



FF SP HV + FF SAPD LV



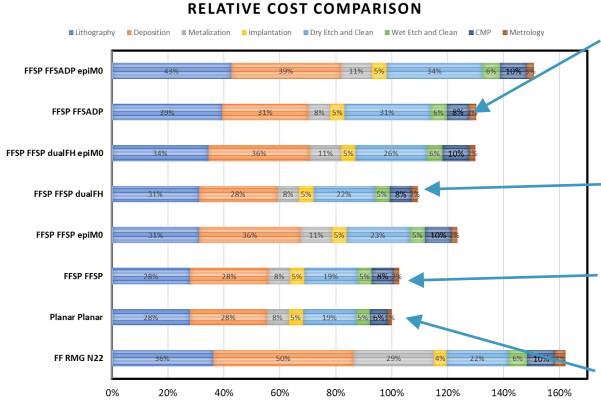
COO OF NAND PERI FF INTEGRATION

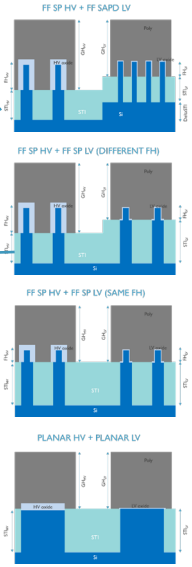
Module Cost

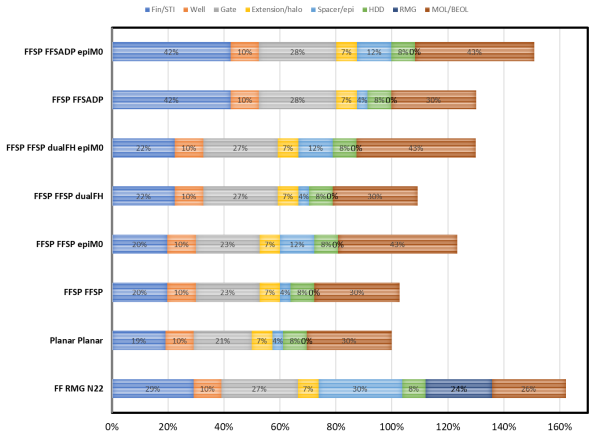
	FF RMG N22	Planar Planar	FFSP FFSP	FFSP FFSP epiM0	FFSP FFSP dualFH	FFSP FFSP dualFH epiM0	FFSP FFSADP	FFSP FFSADP epiM0
Fin/STI	196.54	128.73	133.25	133.25	151.64	151.64	286.15	286.15
Well	67.04	68.8	68.8	68.8	68.8	68.8	68.8	68.8
Gate	185.37	140.33	154.06	154.06	180.01	180.01	186.93	186.93
Extension/halo	49.66	49.66	49.66	49.66	49.66	49.66	49.66	49.66
Spacer/epi	201.98	25.54	25.54	83.12	25.54	83.12	25.54	83.12
HDD	57.24	57.24	57.24	57.24	57.24	57.24	57.24	57.24
RMG	159.82	0	0	0	0	0	0	0
MOL/BEOL	178.69	205.65	205.65	288.01	205.65	288.01	205.65	288.01
Total	1096.34	675.95	694.2	834.14	738.54	878.48	879.97	1019.91

Module Relative

	FF RMG N22	Planar Planar	FFSP FFSP	FFSP FFSP epiM0	FFSP FFSP dualFH	FFSP FFSP dualFH epiM0	FFSP FFSADP	FFSP FFSADP epiM0
Fin/STI	29%	19%	20%	20%	22%	22%	42%	42%
Well	10%	10%	10%	10%	10%	10%	10%	10%
Gate	27%	21%	23%	23%	27%	27%	28%	28%
Extension/halo	7%	7%	7%	7%	7%	7%	7%	7%
Spacer/epi	30%	4%	4%	12%	4%	12%	4%	12%
HDD	8%	8%	8%	8%	8%	8%	8%	8%
RMG	24%	0%	0%	0%	0%	0%	0%	0%
MOL/BEOL	26%	30%	30%	43%	30%	43%	30%	43%
Total	162%	100%	103%	123%	109%	130%	130%	151%







COO OF NAND (INCLUDING AREA SCALING)

	Cost	Area Saving (thick)	Area Saving (thin oxide)	Power-Performance (thin)
Planar Planar	1	3	3	2
FFSP FFSP	1	2	2	3
FFSP FFSP dualFH	2	1	2	1.5
FFSP FFSADP	3	1	1	1

1	best
3	worst

PERI TRANSISTOR: IMEC DEVELOPMENT SYNOPTIC VIEW

Memory type	Oxide type	FF HKMG Gate First	FF HKMG Gate First (thick IL)	FF HKMG Gate First (thick IL)	Planar HKMG Gate First	Planar HKMG Gate First (thicker IL)	FF SiO2 (MV)	FF SiO2 (HV)
DRAM	LV	Y						
	HV		Y					
SCM	LV	Y						
	HV			Y				
NAND	LV				Opt 1		Opt 2	
	HV					Opt 1		Opt 2
	HKMG	Y	Y	Y	Y	Y	SiO2	SiO2
	FF / planar	FF	FF	FF	Pl	Pl	FF	FF
	VDD target (V)	1.0	3.0	8.0	3.3	30	3.3	30
	EOT target (nm)	1.4	5	16	5	50	5	50

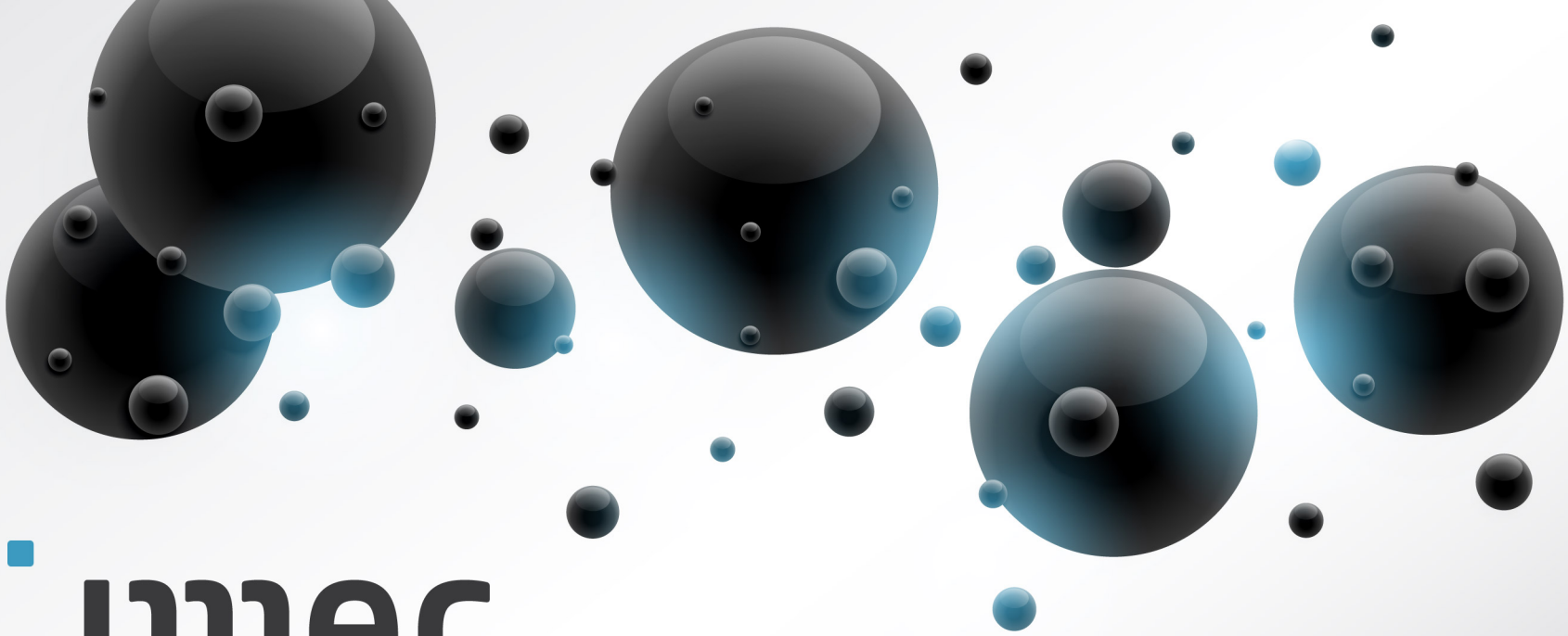
- SCM requires higher VDD option than DRAM, but the technology platform can be the same
- NAND is currently explored as planar HKMG or FF SiO2

CONCLUSIONS

- DRAM
  - Multiple HKMG planar platform solutions have been developed for thin oxide
  - Current imec HW focus is on FF development for next gen memory and integration of thick oxide (EOT ~4-6 nm), addressing also the reliability concern for planar and FF
- SCM
  - HKMG is a need to keep up speed close/similar to DRAM:
    - What are the integration challenges due to higher bias needed for the memory cells?
    - Are specific reliability concern due to integration of HKMG on thicker oxide (~15nm)?
- NAND
  - Higher I/O speed → triple oxide thickness: which platform is the best options?
    - HKMG planar (do we deliver the expected specs? Reliability concern in thicker oxide?)
  - Area saving → FF HV platform assessment

ACKNOWLEDGMENT

- Eugenio Dentoni Litta
- Jacopo Franco
- Hyungrock Oh
- ...
- Naoto Horiguchi



imec

partner
technical
week

GLOBALFOUNDRIES intel KIOXIA Western Digital. SAMSUNG HLMC SK hynix tsmc Micron SONY socionext QUALCOMM HUAWEI SMIC