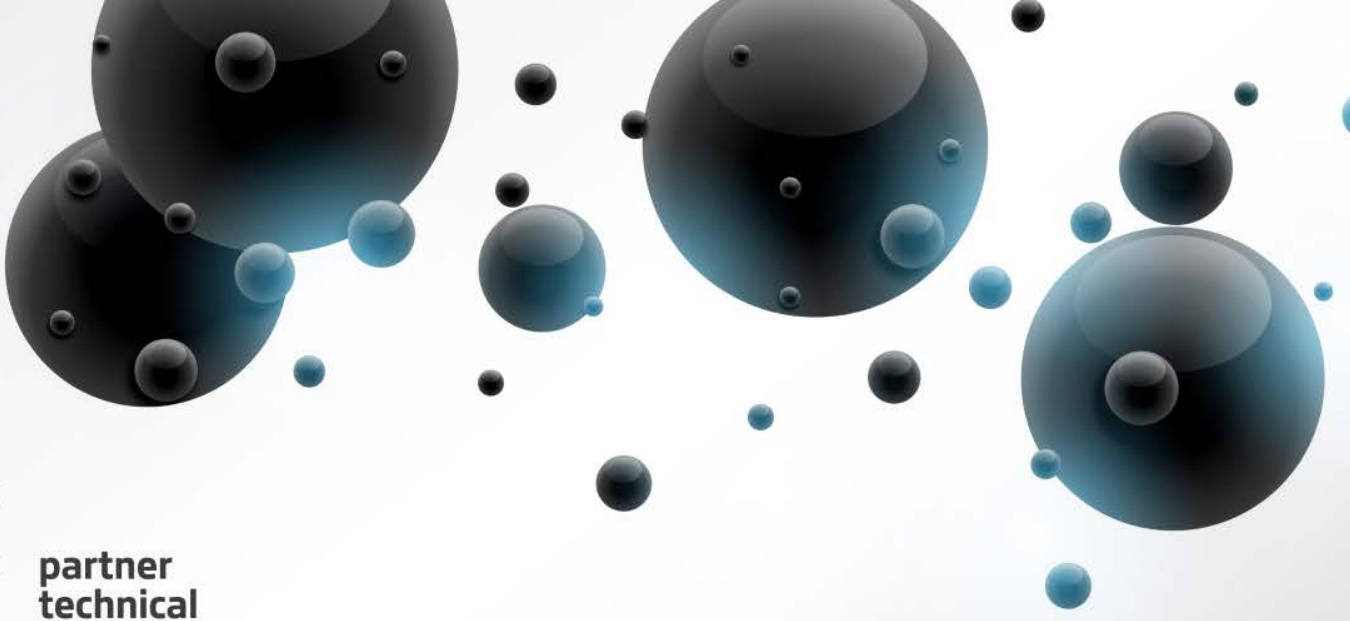
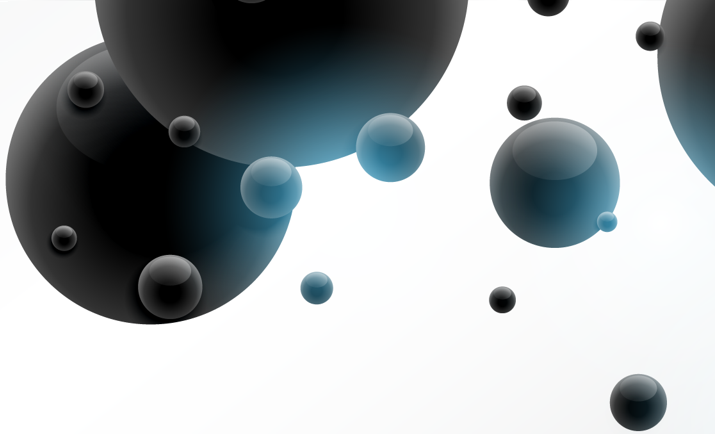


imec partner technical week

FINFET INTEGRATION IN MEMORY PERIPHERY TRANSISTORS

EUGENIO DENTONI LITTA, ON BEHALF OF THE MEMORY PERIPHERY TEAM

GLOBALFOUNDRIES intel SAMSUNG SK hynix tsmc TOSHIBA Micron SONY HUAWEI QUALCOMM SanDisk socionext



LOGIC DEVICES

F1110

NOW IN COURSE:

FINFET INTEGRATION IN MEMORY PERIPHERY TRANSISTORS

EUGENIO DENTONI LITTA

THIS PRESENTATION IS OPEN TO:

CORE PARTNERS,
HUAWEI, APPLE, SOCIONEXT

AMAT, ASM, BASF, SCREEN, KLA-TENCOR, KULEUVEN, LAM, SYNOPSYS, ULTRATECH, COVENTOR, NOVA, PARKSYSTEMS, SOITEC, KURITA, SILTRONIC, VOLTAIX, AIRLIQUIDE, CENTRALGLASS, EBARA, GLOBALTCADSOL, VERSUMMATERIALS, POONGSAN, ASML, HITACHI, TEL

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OUTLINE

- Introduction
- FinFET integration in memory periphery
  - Process/device pathfinder lot: module development status
  - Key challenges & outlook
- Electrical evaluation of FinFET pathfinder
  - Device performance: HKMG vs SiON/poly
  - Threshold voltage tuning
  - Thermal stability
- Conclusions and outlook

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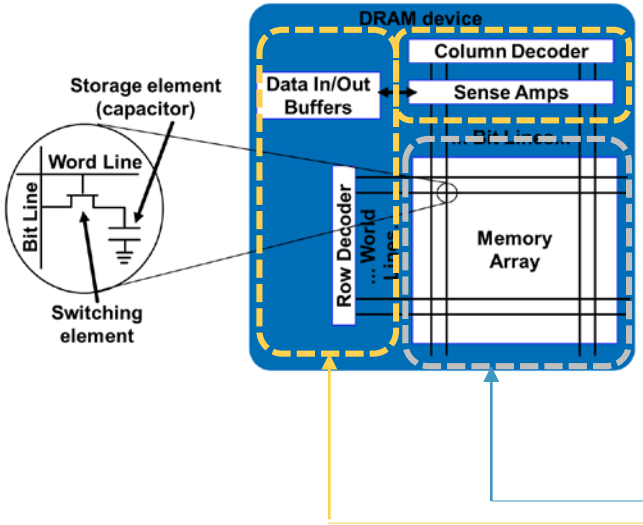
TRANSISTORS USED IN DRAM MEMORY CHIP

- Peripheral transistors serve several purposes: address decoders, sense amplifiers, output buffers, control circuitry
- This presentation: FinFET integration in low voltage transistors
- Key integration challenges: gate-first FF flow, high thermal budget



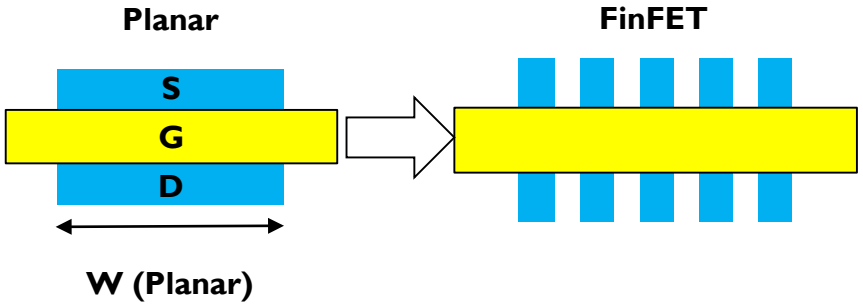
	Cell Transistor	Periphery Transistor		
Type of transistor	**Access Device**	**Regular Logic Transistor**	**Sense/Amplifier**	**Row Decoder**
Applied Voltage	VPP (~3.0V)	VDD (1.5V)	Vcore (1.0V~1.3V)	VPP (~3.0V)
Gate Oxide thickness	THICK (>=6nm)	thin (<2.5nm)	thin (<2.5nm)	THICK (>=5nm)
Gate Length	Minimum Feature size	Larger than Cell (~50nm)	Longer Lg within pitched layout (e.g.: ~100nm)	Longer Lg within pitched layout (e.g.: ~120nm)
Key features/Attentio	Junction Leakage Short Channel	Speed Short Channel	Local Variation (mismatch)	Reliability

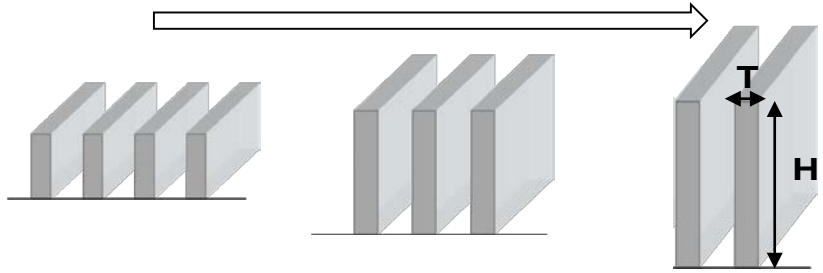
Reference value for DDR3, DRAM 20 nm node; Adapted from S. Y. Cha, IEDM 2011 short course;

Area breakdown: Memory Array ~60%,
Periphery Transistor ~40% (~1/3 Sense Amp; ~2/3 Regular Logic + Decoder)

FF MEMORY PERIPHERY EXPECTED VARIABILITY & PERFORMANCE IMPROVEMENT

WIDE EFFECTIVE TRANSISTOR WIDTH IN FINFET W/ HIGH FINS





W(FinFET) = (2H+T) * Fin number

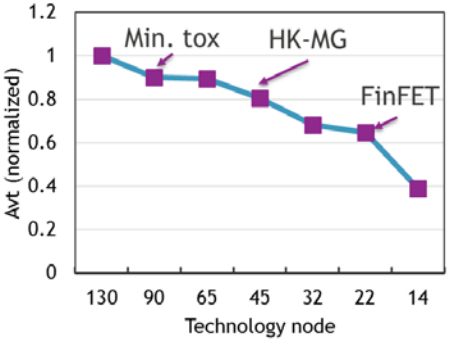
Wide effective transistor width in FinFET achievable with higher fin

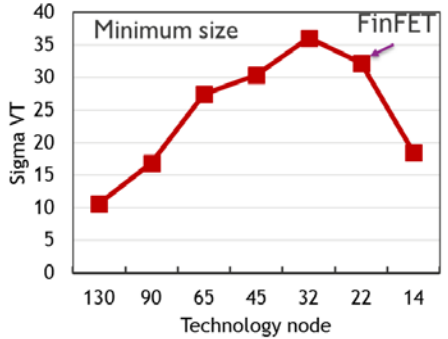
- **Larger drive current/foot print**
- **Small variability**

$$\partial \Delta Vt = \frac{Avt}{\sqrt{W * L}}$$

better mismatch with taller FF

FinFET has intrinsically better variability thanks to low channel dopant concentration.





KEY PROCESS ASSUMPTIONS

- Fin geometry:
  - 40nm initial fin height target, to be extended to taller fins
  - Single patterning (cost effectiveness, variable fin width)
  - -> Gemini maskset: variable fin W (15-100nm)
- Gate stack:
  - Gate-first SiON/poly (lower process cost)
  - Gate-first HKMG (performance, scalability, process window)
  - Gate-last not considered at this point (higher cost, thermal budget considerations)
- Junctions/contact:
  - Epi not implemented yet (lower process cost), evaluation planned
  - Junction design by ext/halo and HDD implantations
  - Extended silicide contact (Salicide) without M0/LI module (lower process cost)

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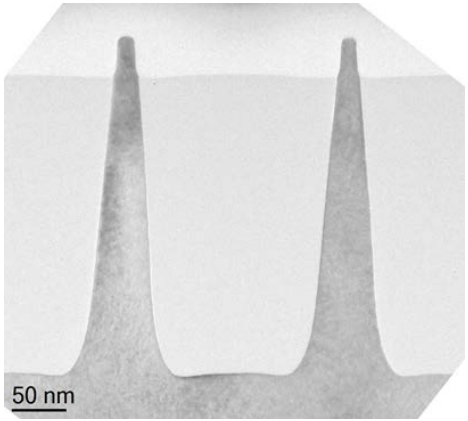
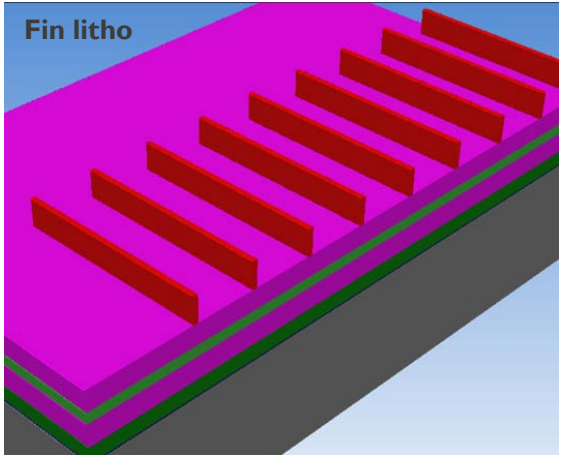
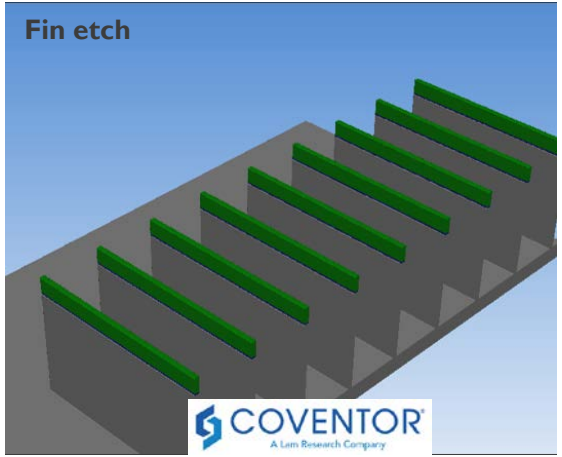
FIN/STI MODULE

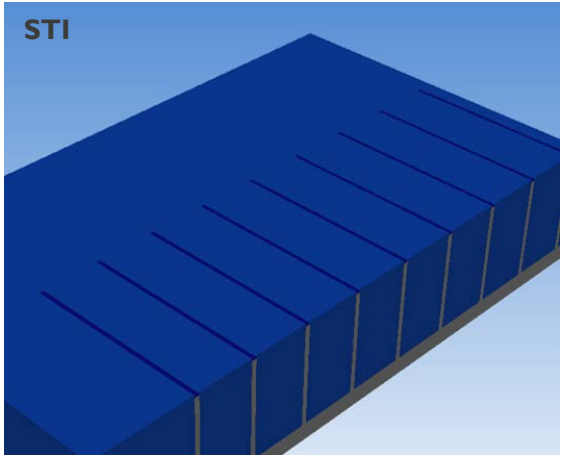
Development needed: None

- Key layout/process values:
  - Fin width: 15-100 nm
  - Fin pitch: 200-600 nm
- Key device splits:
  - None
- Major challenges:
  - None







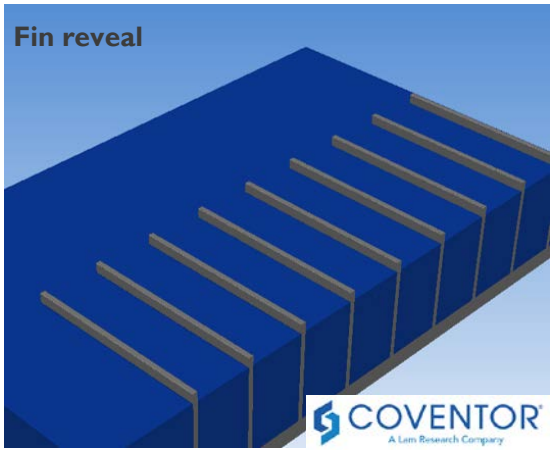


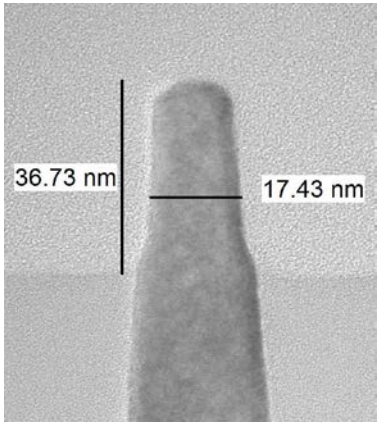
CHANNEL DOPING/FIN REVEAL

Development needed: Tall fin reveal

- Key layout/process values:
  - Fin height: 40 nm (evaluation to be extended to 80nm)
- Key device splits:
  - Channel implant conditions (based on Everest and Salsa3 baselines)
  - V_T adjust implants

- Major challenges:
  - None expected



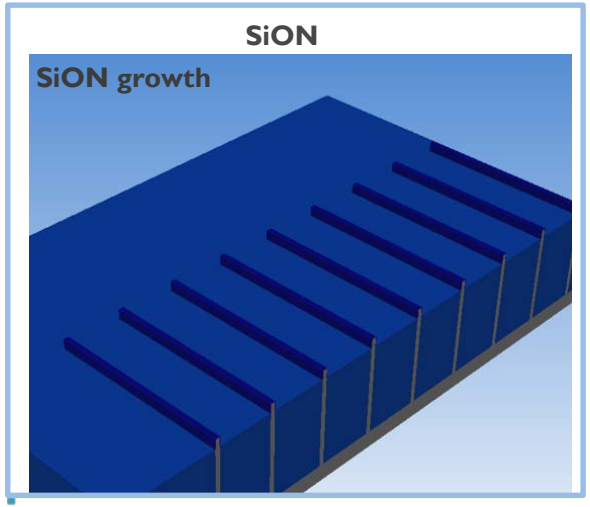


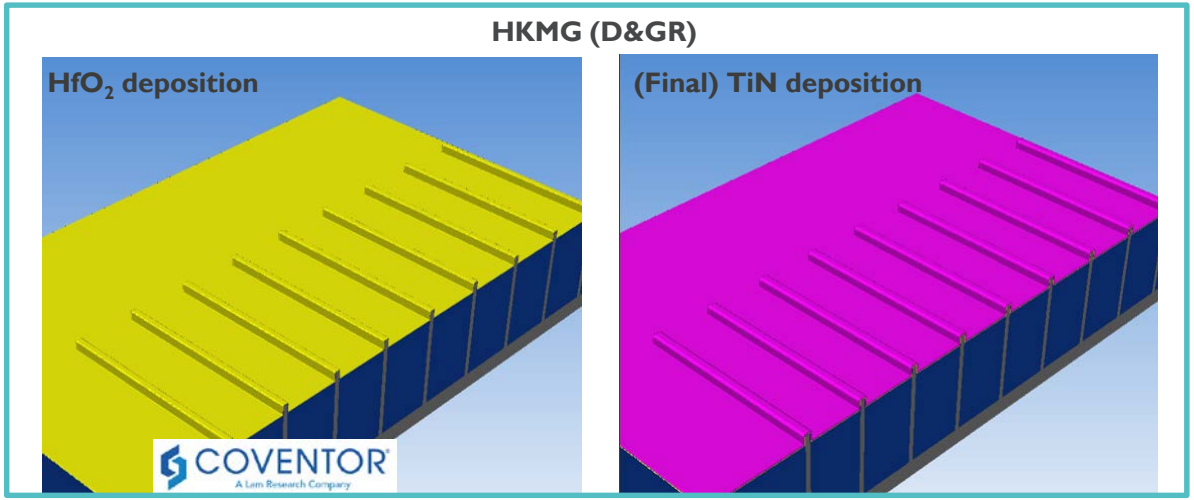
GATE STACK DEPOSITION

Development needed: **D&GR optimization**

- Key layout/process values:
  - Two gate-first options (SiON/poly and D&GR HKMG)
- Key device splits:
  - V_T tuning in SiON/poly (channel and poly implants)
  - V_T tuning in HKMG (channel implants, dielectric caps)

- Major challenges:
  - None expected



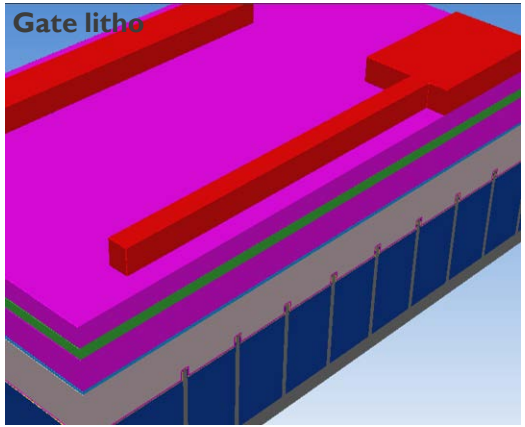


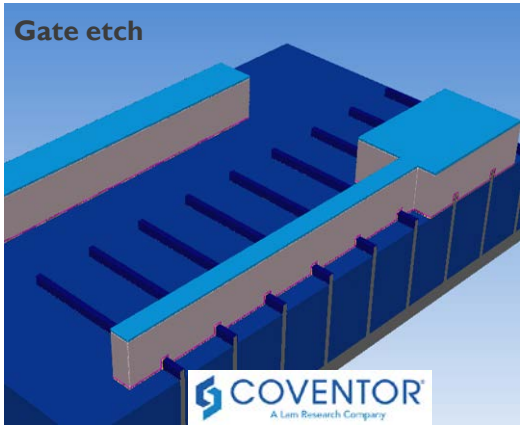
GATE PATTERNING

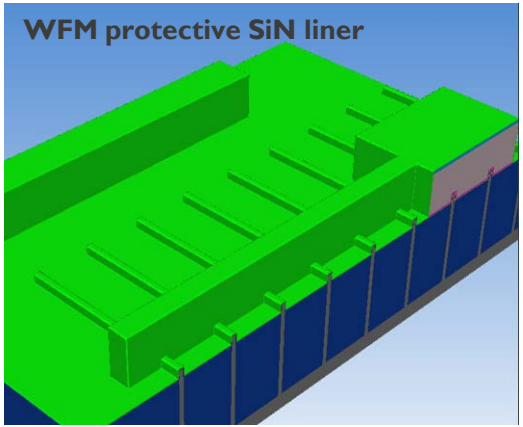
Development needed: Gate etch

- Key layout/process values:
  - Gate length (min): 35 nm (30nm trim)
  - Fin pitch (min): 500 nm
  - WFM protective liner: 3nm
- Key device splits:
  - None

- Major challenges:
  - Gate profile / fin attack tradeoff in SiON/poly

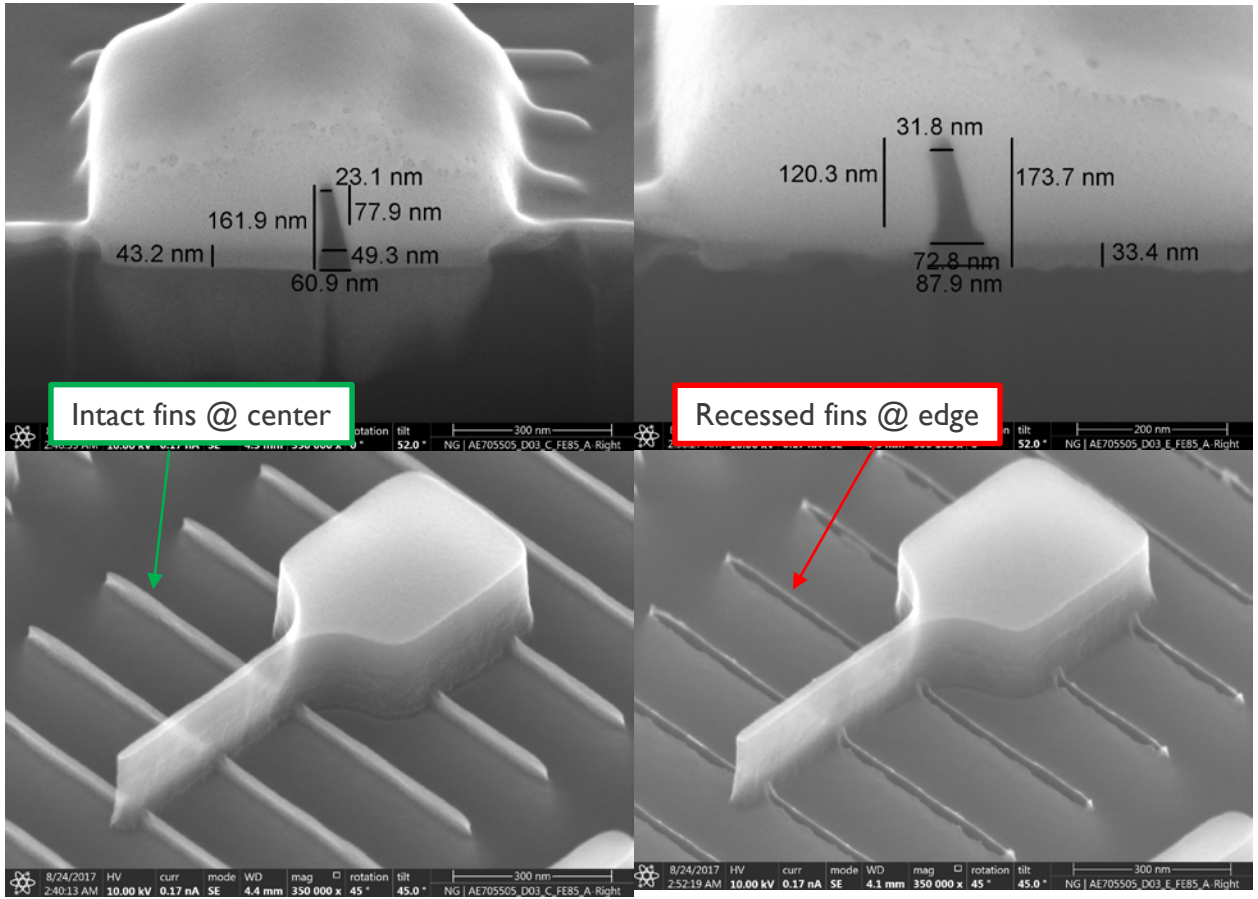






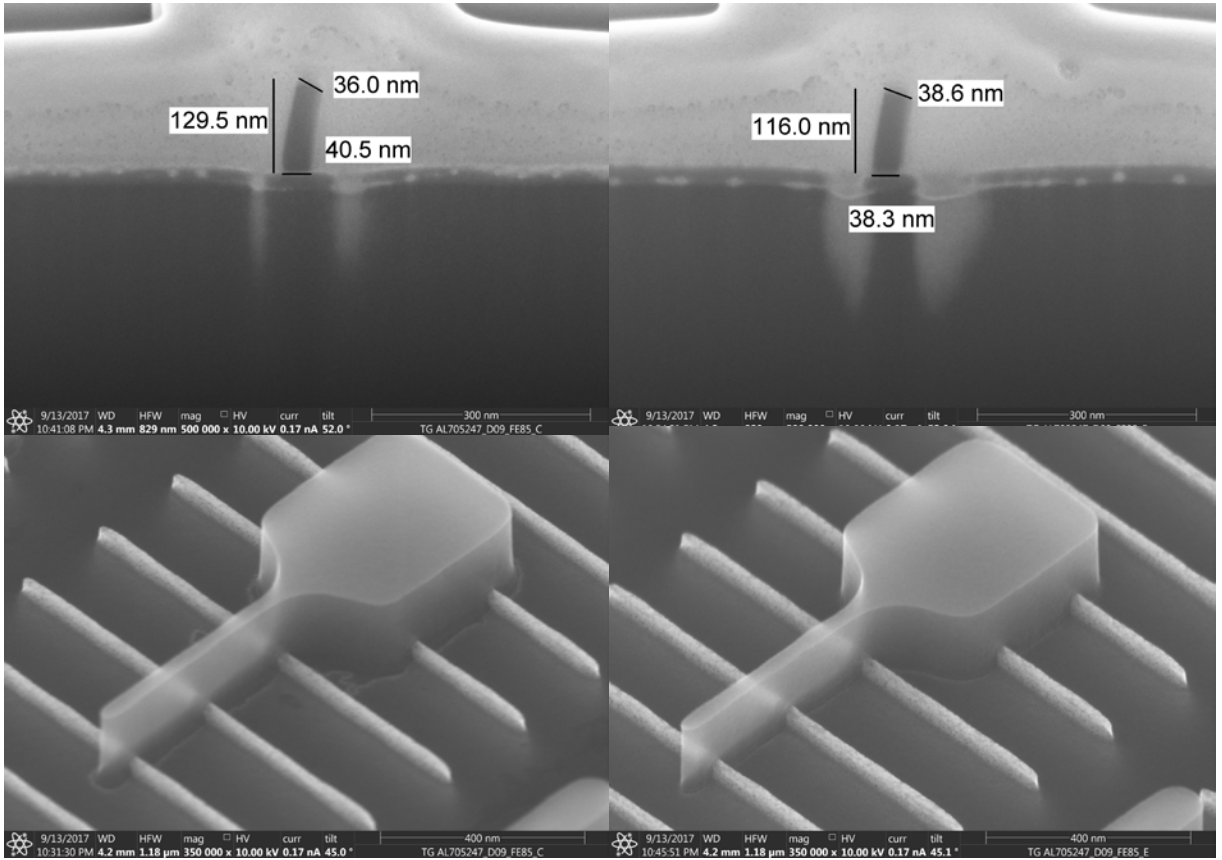
GATE PATTERNING: SION/POLY

- Fin attack at wafer edge
  - Linked to polySi uniformity and SiON thickness
  - Outlook: improved poly dep uniformity and CMP planarization
- Strongly tapered profile
  - Due to lateral etch of doped poly
  - Unclear if process window exists
  - Outlook: process window exploration



GATE PATTERNING: HKMG

- Gate profile OK
- No fin attack
- Residues observed at north of wafer
  - Linked to poly uniformity
  - Outlook: improved poly dep uniformity and CMP planarization

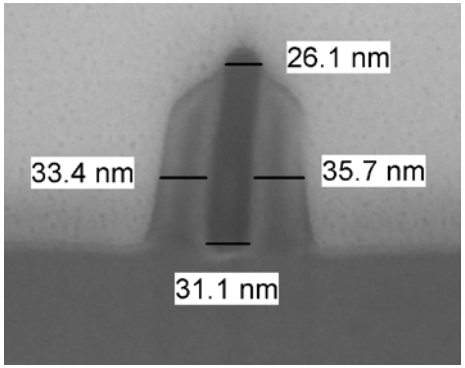


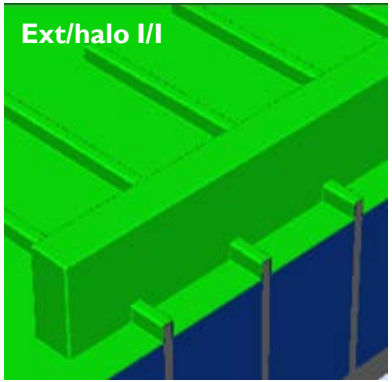
JUNCTION FORMATION

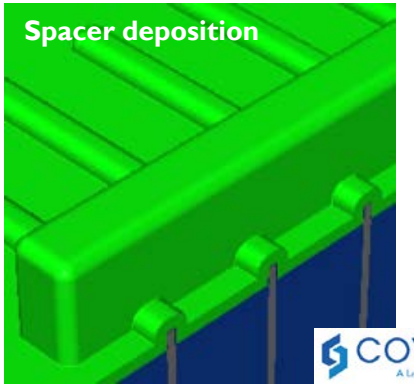
Development needed: Spacer etch selectivity

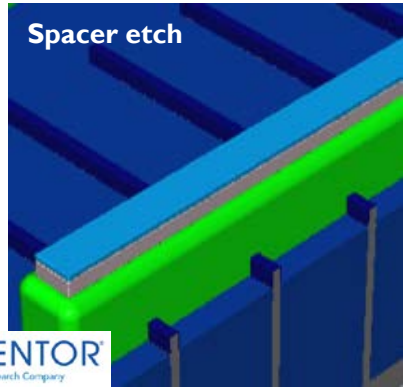
- Key layout/process values:
  - Spacer width: 30nm (to be scaled)
- Key device splits:
  - Ext/halo implants (based on Everest and Salsa3 baselines)
  - HDD implants (based on Everest and Salsa3 baselines)
  - DRAM anneal

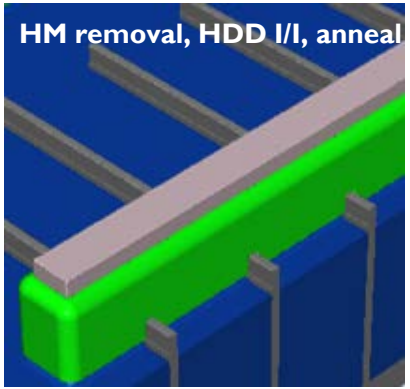
- Major challenges:
  - None expected











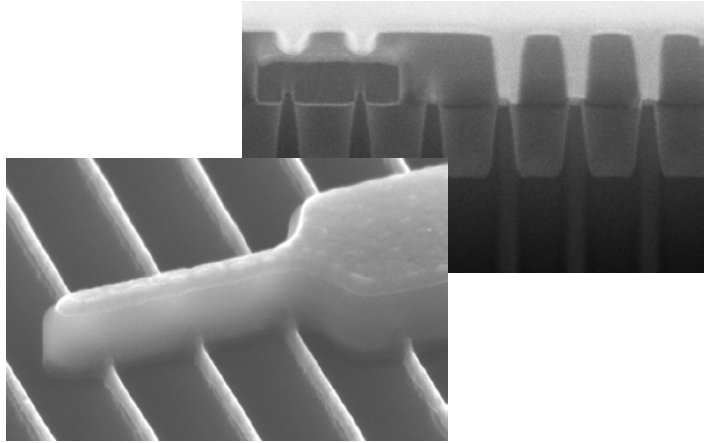
COVENTOR
A Lam Research Company

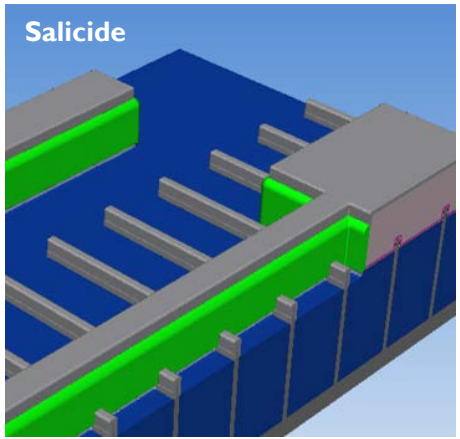
MOL

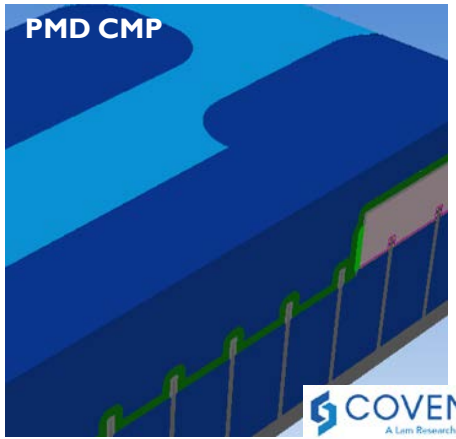
Development needed: Contact etch tuning

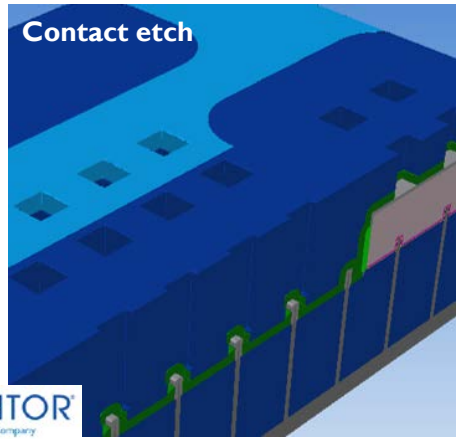
- Key layout/process values:
  - Self-aligned silicide
  - PMD/contact scheme ported from planar baseline
- Key device splits:
  - None

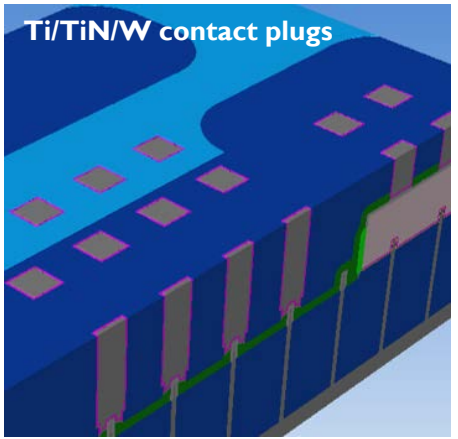
- Major challenges:
  - None











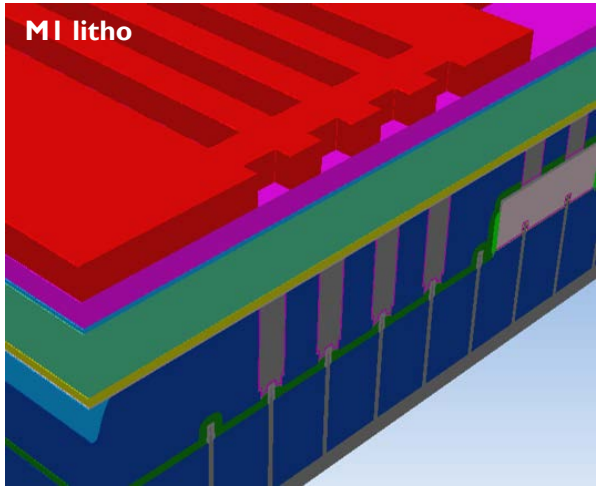
COVENTOR
A Lam Research Company

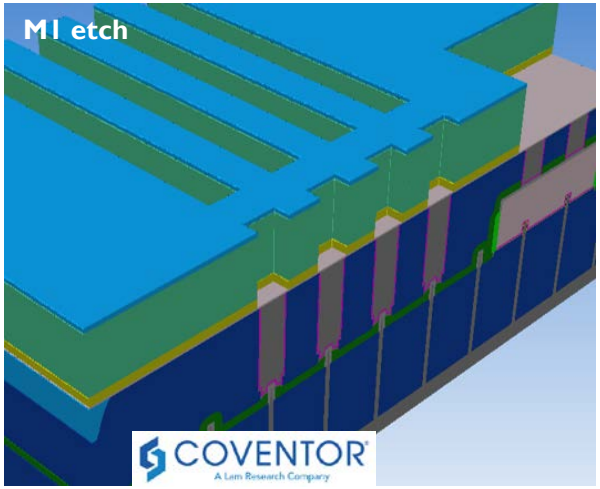
BEOL

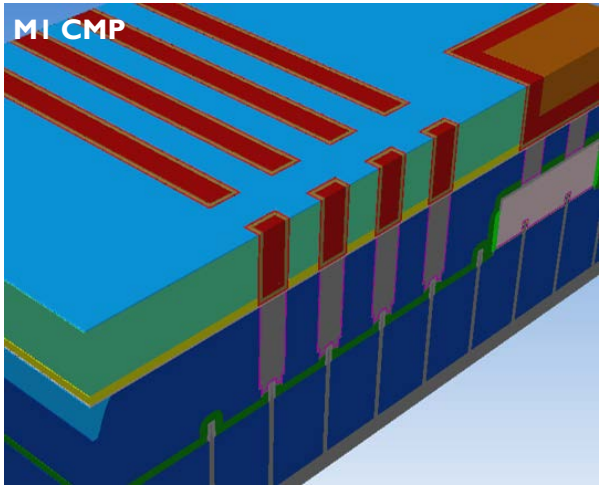
Development needed: None

- Key layout/process values:
  - Cu damascene as in planar baseline
- Key device splits:
  - None

- Major challenges:
  - None







KEY CHALLENGES & PLAN

Module	Status	Development plan
Fin/STI	OK	-
Channel doping/fin reveal	OK for 40nm fins	Fin reveal and implant conditions to be developed for tall fins
Gate stack deposition	Working	SiON thickness tuning, D&GR process optimization for fins
Gate patterning (SiON/poly)	Tapered profile, fin attack	PolySi uniformity improvement, etch window exploration
Gate patterning (HKMG)	OK for 40nm fins	PolySi uniformity improvement, process optimization for tall fins
Junction formation	Working	Spacer and I/I tuning for 40nm and tall fins
MOL	OK	Contact etch tuning
BEOL	OK	-

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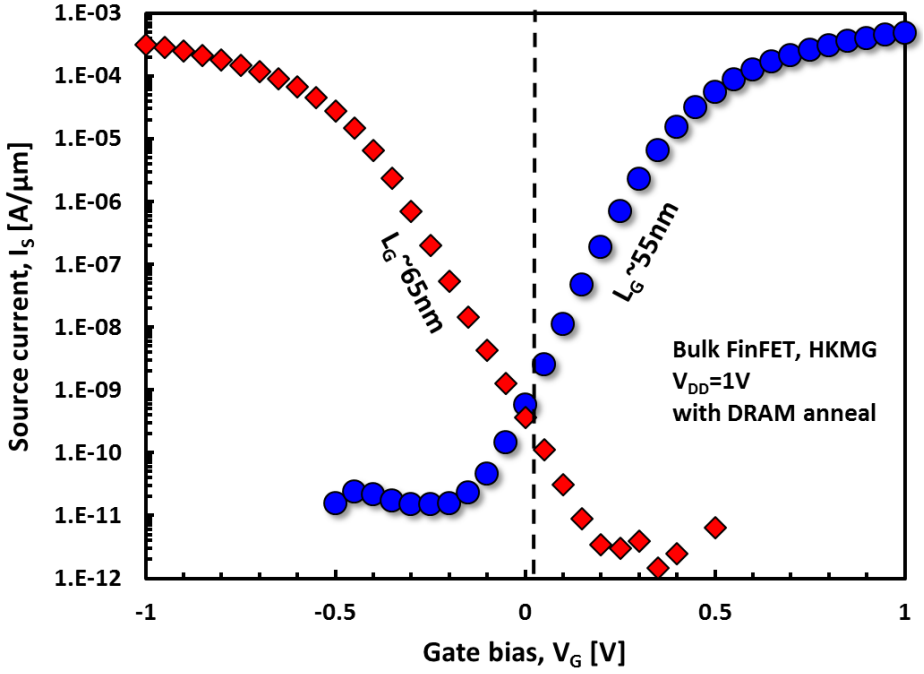
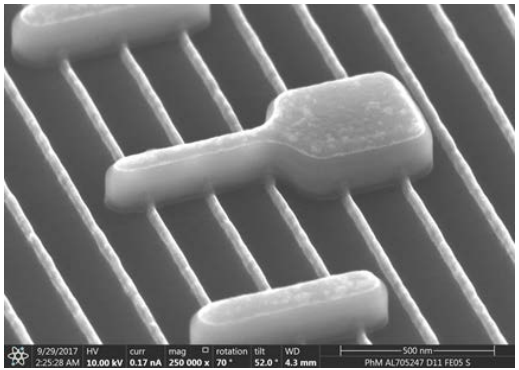
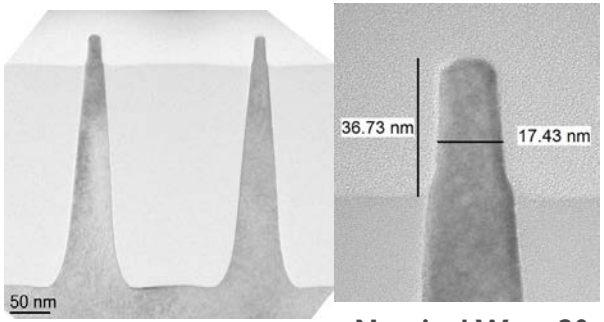
GATE-FIRST HKMG FINFET DEMONSTRATED



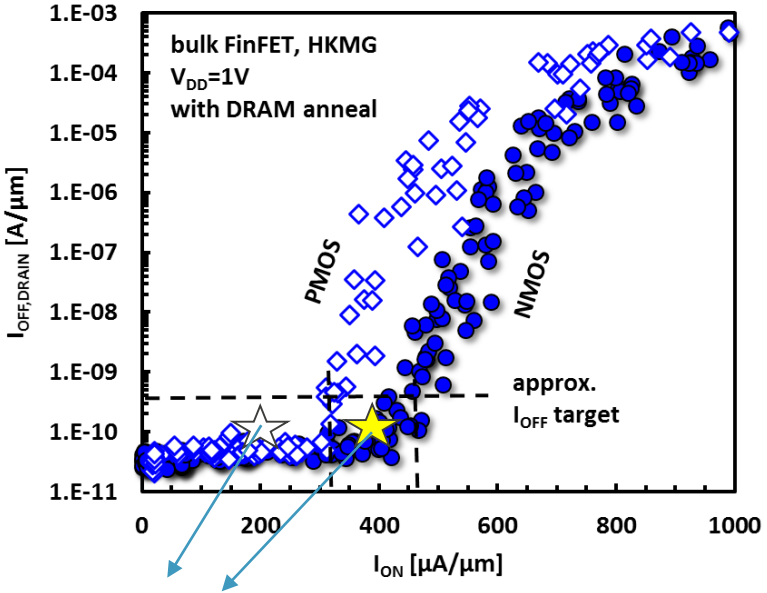




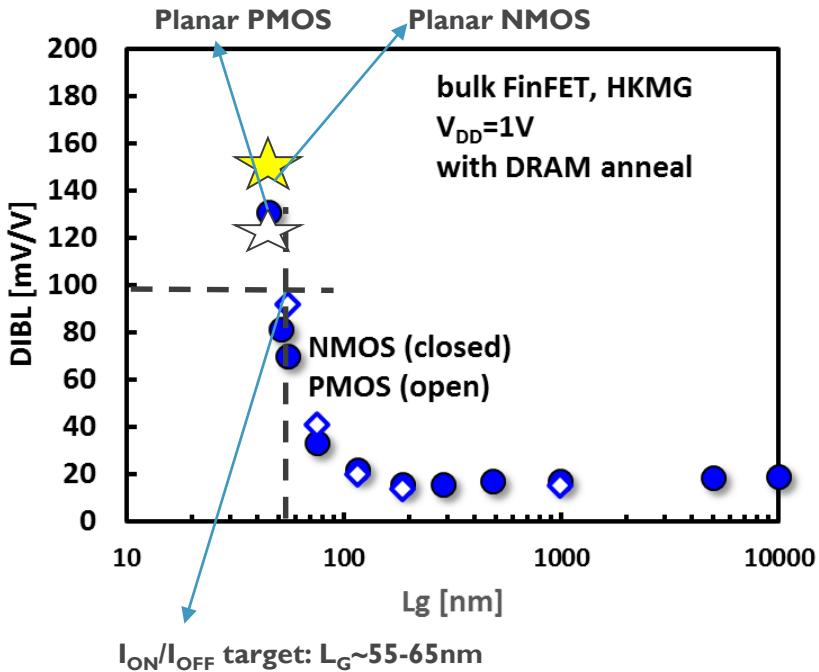
Nominal W_{FIN}=20nm

- FinFET process/device pathfinder: gate first integration, with good electrostatics down to target L_G

DEVICE PERFORMANCE: HIGH-K/METAL GATE



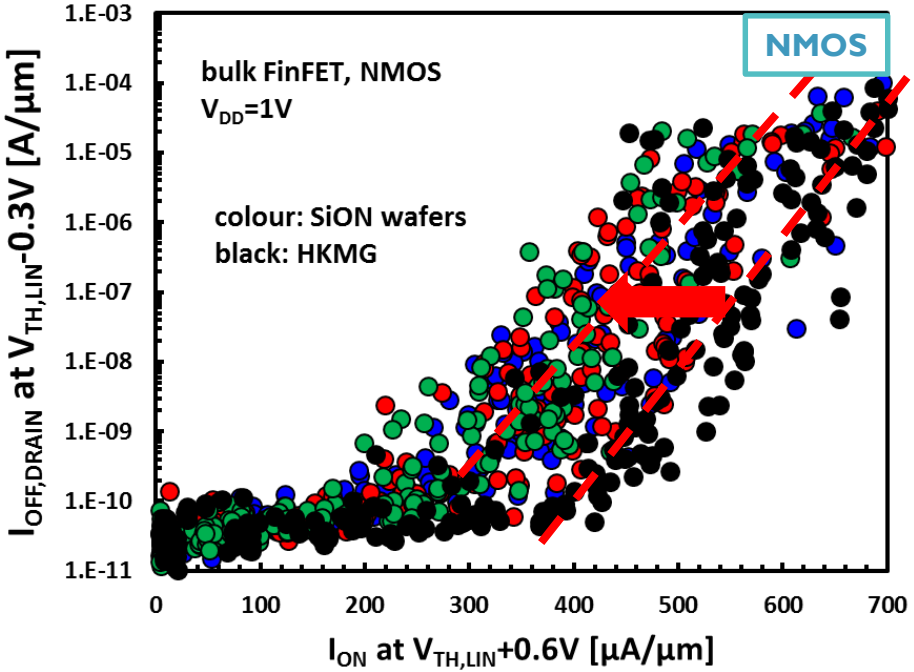
Imec HKMG PMOS/NMOS I_{ON}/I_{OFF} planar performance (see R Ritzenthaler et al, TED 2014 for further details)

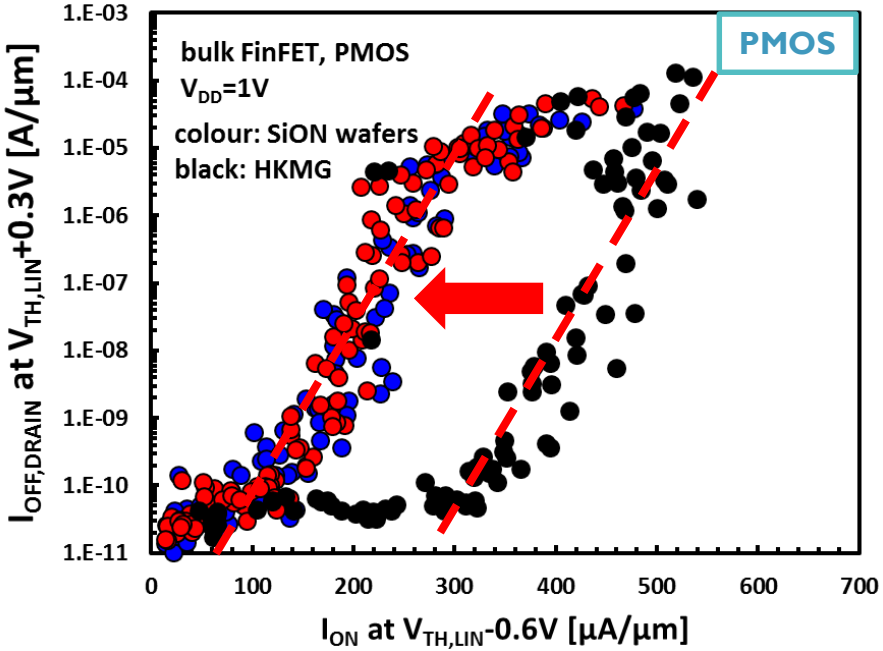


I_{ON}/I_{OFF} target: L_G~55-65nm

- FinFET HKMG wafers: pathfinder lot at performance level (I_{ON}/I_{OFF}, short channel margin) of planar baseline

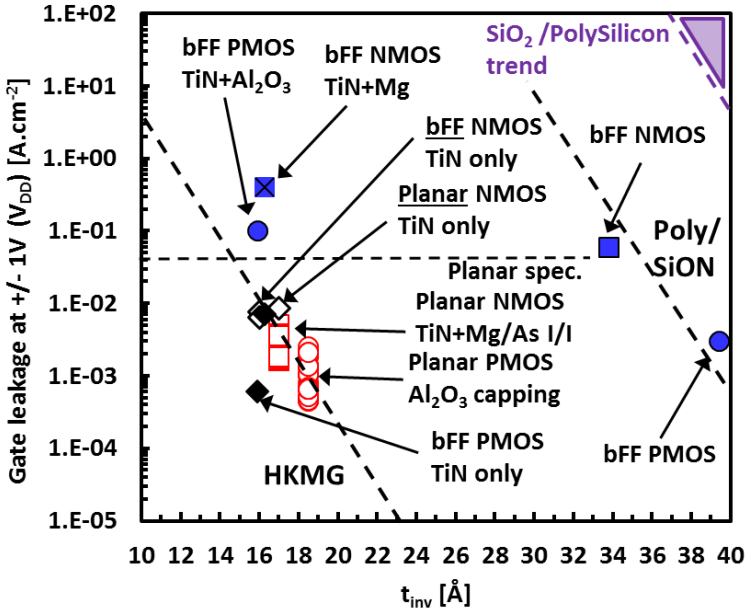
DEVICE PERFORMANCE: POLY/SION



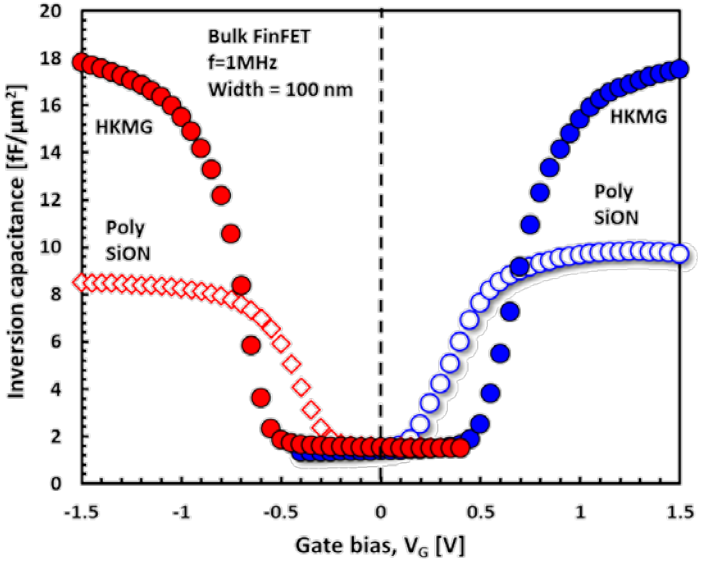


- Functional Poly/SiON FinFETs, but worse performance than HKMG
- SiON T_{inv} thicker than in HKMG wafers (see next slide)

GATE STACK COMPARISON

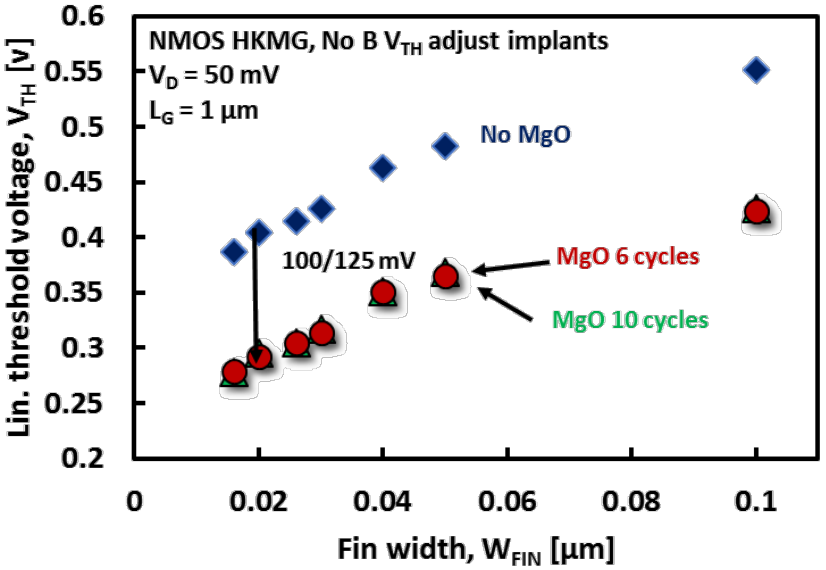


t_{INV} [nm]	NMOS	PMOS
HKMG	1.6	1.6
Poly/SiON	3.4	3.9



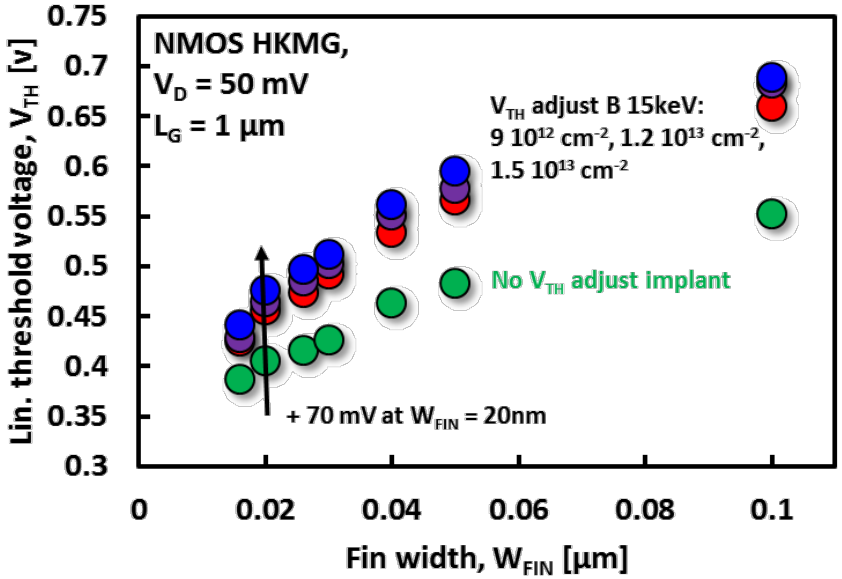
- HKMG:
  - Consistent values for TiN only HKMG wrt planar baseline
  - Gate leakage degradation with integration of eWF shifters in FinFETs (under investigation)
- Poly/SiON:
  - Higher Tinv than expected (under investigation)
  - Acceptable gate leakage, but higher than expected

V_{TH} TUNING: HIGH-K/METAL GATE NMOS

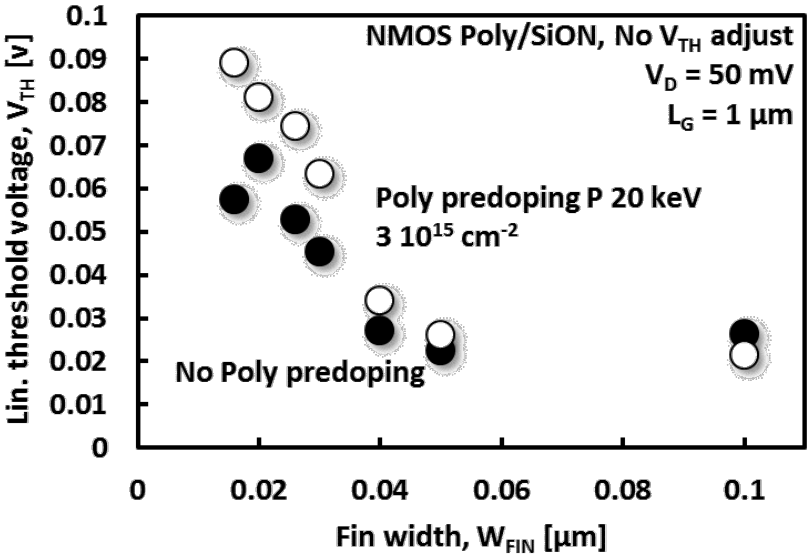


- D&GR MgO cap:
  - Shift preserved down to narrow FinFETs
  - >100mV shift obtained at 15-20nm FinW
  - No effect of MgO thickness

- Channel implant
  - Reduced efficiency of V_{TH} adjust implants with fin width reduction
  - Maximum +70 mV shift obtained for narrow FinFETs with V_{TH} adjust implants

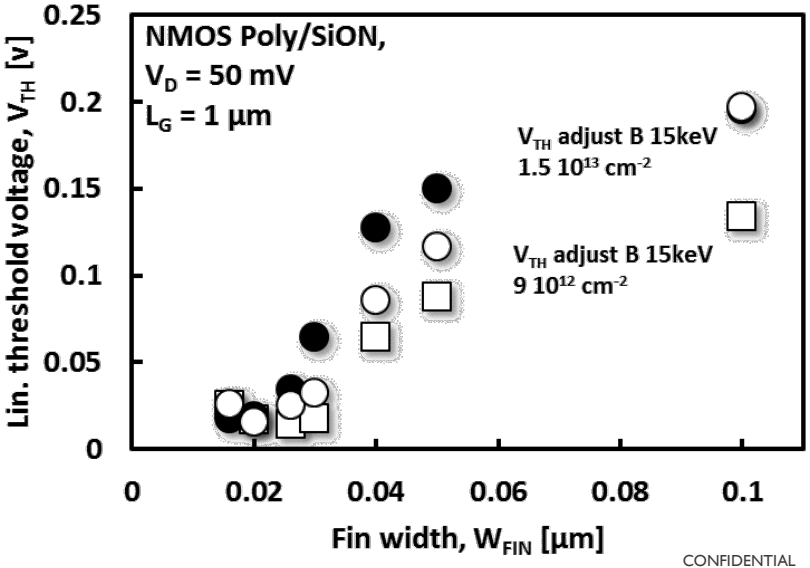


V_{TH} TUNING: POLY/SION NMOS

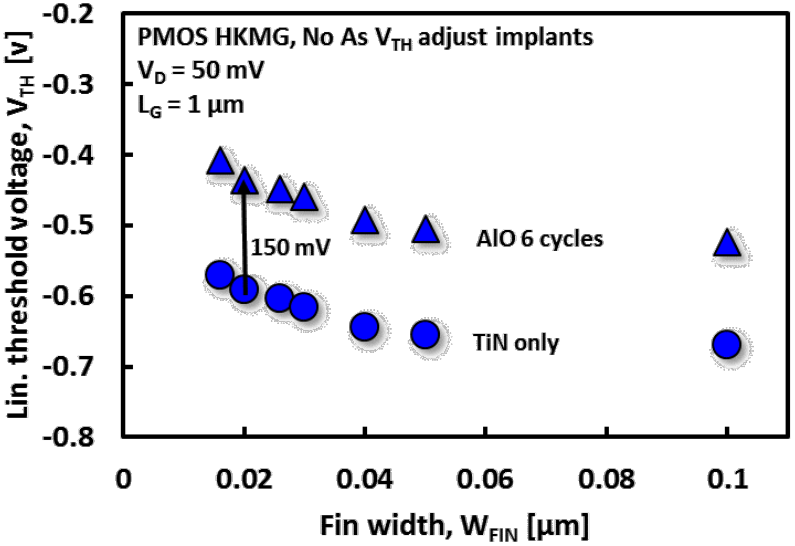


- Poly doping:
  - Limited V_{TH} shift obtained with gate predoping implant

- Channel implant:
  - Reduced efficiency of V_{TH} adjust implants with fin width reduction
  - Limited V_{TH} shift obtained for narrow FinFETs with V_{TH} adjust implants

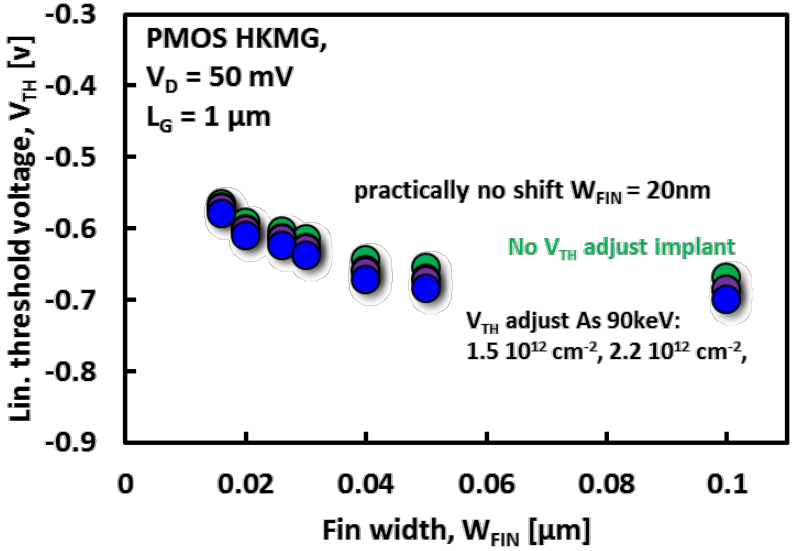


V_{TH} TUNING: HIGH-K/METAL GATE PMOS

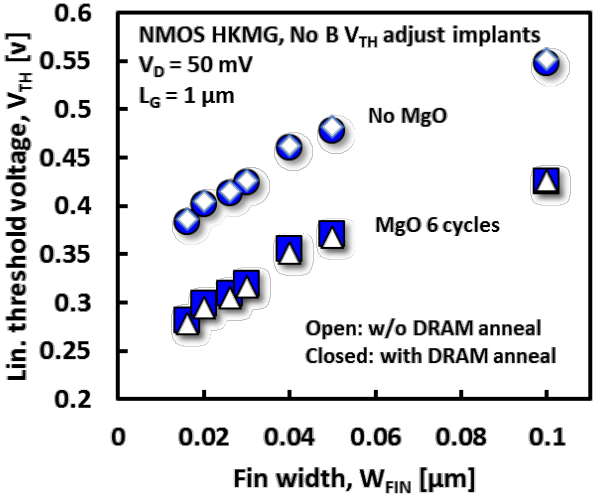


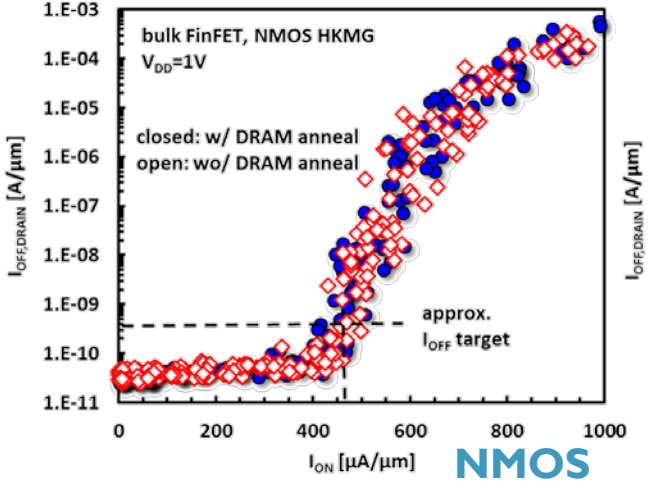
- D&GR AlO cap:
  - Shift preserved down to narrow FinFETs
  - 150mV shift obtained at 15-20nm FinW

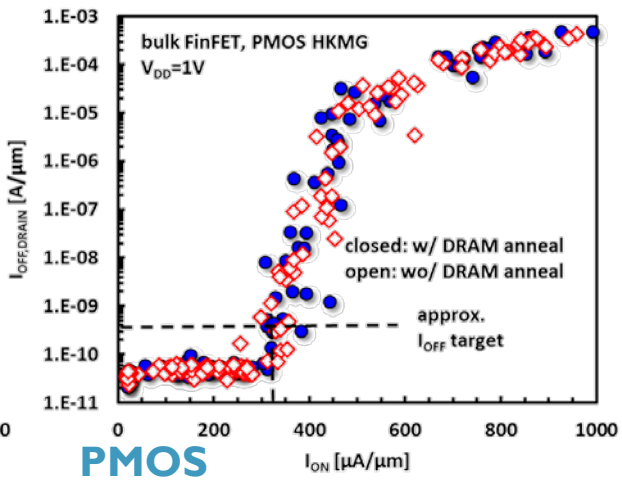
- Channel implant
  - Very limited shift with the chosen implant conditions



THERMAL STABILITY: EFFECT OF DRAM ANNEAL

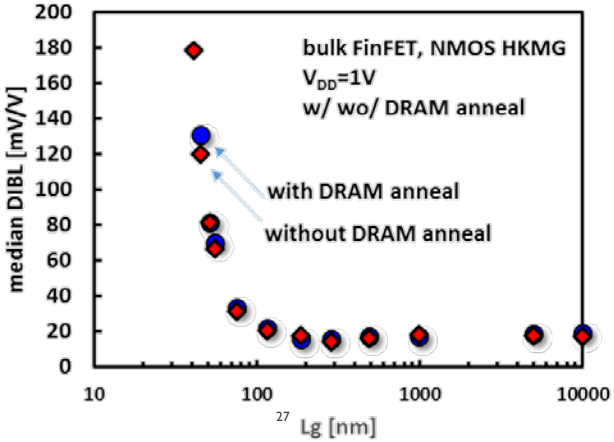


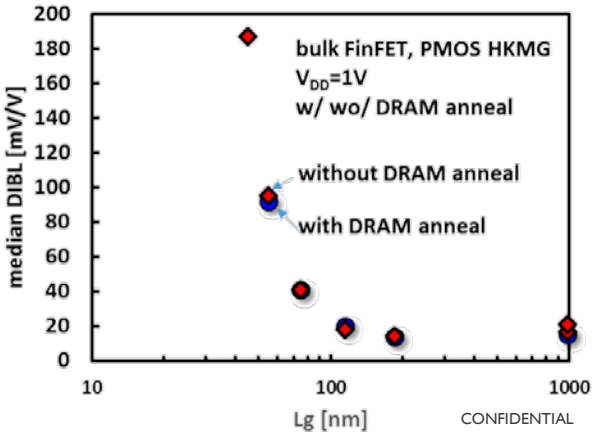




NMOS PMOS

- No effect of DRAM anneal (650°C, 4 hours) on gate stack (expected from planar D&GR baseline)
- No effect of DRAM anneal on I_{ON}/I_{OFF} and short channel margin (potential model: junction diffusion corrected by electrostatic control)





OUTLINE

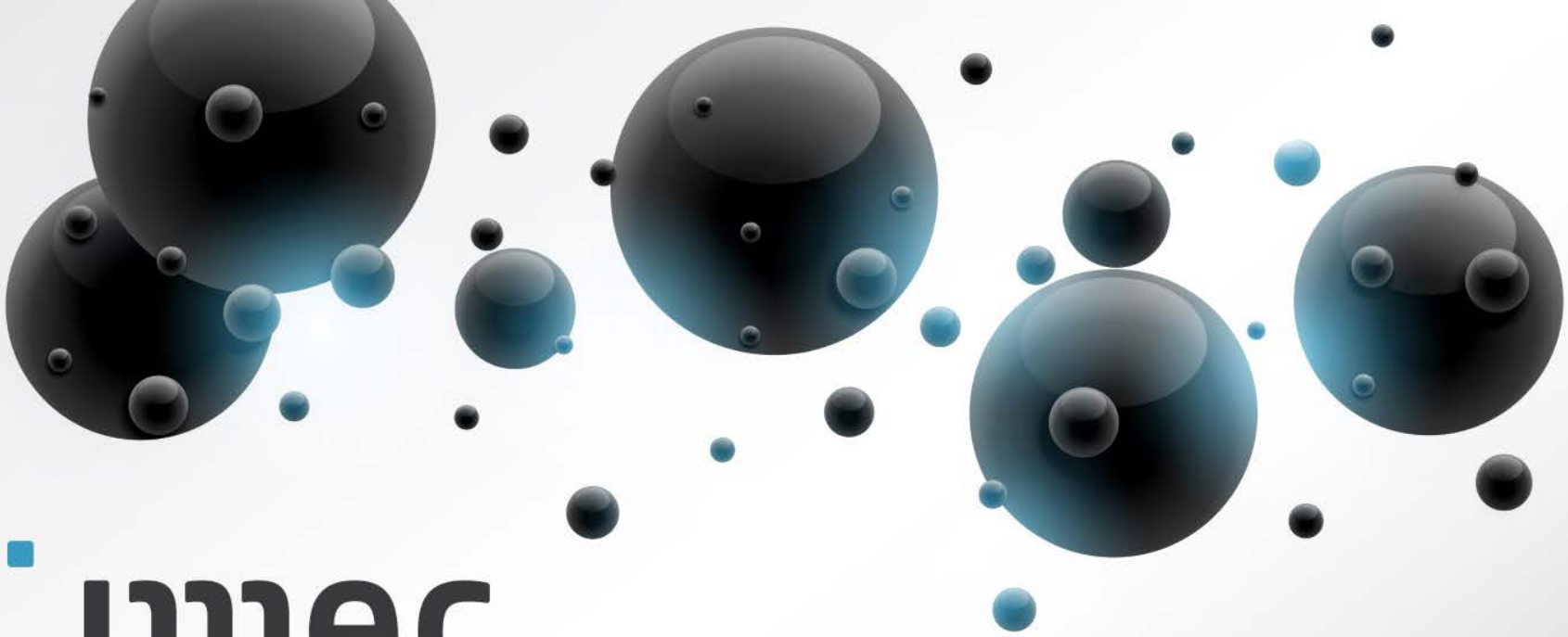
- Introduction
- FinFET integration in memory periphery
  - Process/device pathfinder lot: module development status
  - Key challenges & outlook
- Electrical evaluation of FinFET pathfinder
  - Device performance: HKMG vs SiON/poly
  - Threshold voltage tuning
  - Thermal stability
- Conclusions and outlook

CONCLUSIONS

- Process/Device pathfinder for FinFET integration in memory periphery successfully fabricated and evaluated
  - 40nm fin height, unichannel NFET & PFET
  - Gate-first SiON/poly and HKMG
- Initial module development completed, key challenges identified
  - Key modules set up for HKMG gate first integration on 40nm fins
  - Challenging gate patterning for SiON/poly
- Electrical performance close to pathfinding targets
  - Acceptable I_{ON}/I_{OFF} and DIBL at Lg~55-66nm, competitive performance wrt planar baseline
  - Successfully demonstrated D&GR HKMG scheme on FinFET with MgO and AlO eWF caps
  - Initial exploration of V_{TH} tuning options for HKMG and poly/SiON
  - Excellent thermal stability of gate stacks and junctions

OUTLOOK

- Process optimization for 40nm fins
  - Improvement of polySi uniformity and planarity to enable gate etch learning
  - Process window exploration for SiON/poly gate etch
  - Identification and reduction of process variability sources
- Tall fin demonstration
  - Extension/development of process modules for 80nm fin height
- Device optimization
  - Assessment of maximum V_{TH} tunability in D&GR HKMG scheme
  - Further exploration of V_{TH} tuning via implantation



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