Monolithic 3D Integration: A Path From Concept To Reality

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Abstract

Monolithic three-dimensional (3D) integration enables revolutionary digital system architectures of computation immersed in memory. Vertically-stacked layers of logic circuits and memories, with nano-scale inter-layer vias (with the same pitch and dimensions as tight-pitched metal layer vias), provide massive connectivity between the layers. The nano-scale inter-layer vias are orders of magnitude denser than conventional through silicon vias (TSVs). Such digital system architectures can achieve significant performance and energy efficiency benefits compared to today's designs. The massive vertical connectivity makes such architectures particularly attractive for abundant-data applications that impose stringent requirements with respect to low-latency data processing, high-bandwidth data transfer, and energy-efficient storage of massive amounts of data. We present an overview of our progress toward realizing monolithic 3D ICs, enabled by recent advances in emerging nanotechnologies such as carbon nanotube field-effect transistors and emerging memory technologies such as Resistive RAMs and Spin-Transfer Torque RAMs.

I. Introduction

The traditional path for improving the energy efficiency of digital systems through silicon CMOS (Dennard [Frank01]) scaling is becoming increasingly difficult [Kuhn12]. Hence, alternative technologies beyond silicon CMOS are being explored. For example, ultra-thin (~1 nm) 1D semiconductors such as carbon nanotubes (CNTs) represent a significant departure from today's silicon CMOS technology, promising improved device scalability and performance [Wong11]. Carbon nanotube field-effect transistors (CNFETs) are projected to improve the energy-delay product (EDP, a measure of energy efficiency) of very-large-scale integrated (VLSI) digital systems by an order of magnitude vs. silicon CMOS [Chang12]. CNFETs are also unique among emerging nanotechnologies since digital circuits and systems fabricated using CNFETs have been demonstrated [Shulaker13a-b, Shulaker14a]. Additionally, high-performance and highly-scaled CNFETs have also been demonstrated [Shulaker14b-c, Franklin12a]. Therefore, CNFETs are promising candidates for building the next-generation of high-performance and energy-efficient digital systems.

Even with improved next-generation logic devices, system-level performance will remain severely constrained by the growing memory-logic communication bottleneck [Stanley-Marble11, Dally11]. To overcome this bottleneck, revolutionary digital system architectures with highly fine-grained integration of logic circuits and massive amounts of memory is required.

3D integration, whereby circuits are stacked vertically over one another, can achieve such increased level of integration [Banerjee01]. Today, 3D integration typically relies on vertical stacking of various circuit layers using vertical through silicon vias (TSVs)[1]. TSVs occupy a relatively large footprint: for example, typical TSVs are 5 μm in diameter with a 20 μm inter-TSV pitch [Xu13]. The large dimensions of the TSVs limit the density of vertical connections.

To achieve fine-grained integration, denser connections between layers is necessary. **Monolithic** 3D integration, whereby each vertically-stacked layer of the 3D IC is fabricated directly over the previously fabricated layers, enables such future systems by allowing nano-scale inter-layer vias (ILVs) to be used to connect vertical circuit layers (i.e., no TSVs are required). These nano-scale ILVs have the same pitch and dimensions as tight-pitched metal layer vias, and are therefore orders of magnitude smaller than TSVs [Panth13, Batude11]. Given the ratio between TSV and ILV pitch, monolithic 3D integration enables massive vertical integration, achieving orders of magnitude (~1,000X) denser vertical connections compared to TSV-based 3D ICs.

Fine-grained monolithic 3D integration of logic gates has been discussed in [Bobba11, Lee13]. However, such monolithic 3D integration (restricted to logic gates only) has limited benefits. In contrast, the massive connectivity enabled by monolithic 3D integration of logic **and** memory (and memory interface circuits) can directly translate into unprecedented memory bandwidth [Ebrahimi14], which in turn translates into significant improvements in performance and energy efficiency.

While monolithic 3D integration is an attractive technological option, processing obstacles have posed major roadblocks: circuits on the upper-layers must be fabricated at a

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low temperature (<400 °C) [Wong07][1]. This is also referred to as the process thermal budget constraint.

CNFETs, which are promising candidates for next-generation high-performance and highly energy-efficient digital systems, are naturally suited for monolithic 3D integration. In this paper, we focus on monolithic 3D ICs enabled by emerging nanotechnologies for both computing and storage: particularly, CNFETs for logic circuits, and emerging non-volatile memory (NVM) technologies such as Spin-Transfer Torque RAM (STTRAM) [Kawahara12] and Resistive RAM (RRAM) [Wong12]. CNFET circuits and the NVM technologies can be fabricated with a maximum processing temperature of <250 °C, making them suitable for monolithic 3D fabrication.

Figure 1 shows a target monolithic 3D IC enabled by such emerging technologies. The computing elements and memory access circuitry are built using emerging 1D CNFETs[2]. STTRAM is used for caches (L2 and higher) and main memory to utilize its access time, energy, retention, and endurance characteristics [Smith10]. RRAM (specifically 3D RRAM [Chen12]) is used for massive on-chip storage to minimize off-chip communication. Various layers of the 3D IC are connected with nano-scale ILVs, permitting massive connectivity between the vertical layers. In monolithic 3D ICs with high-performance computing elements on upper layers, appropriate inter-layer cooling techniques must also be integrated.

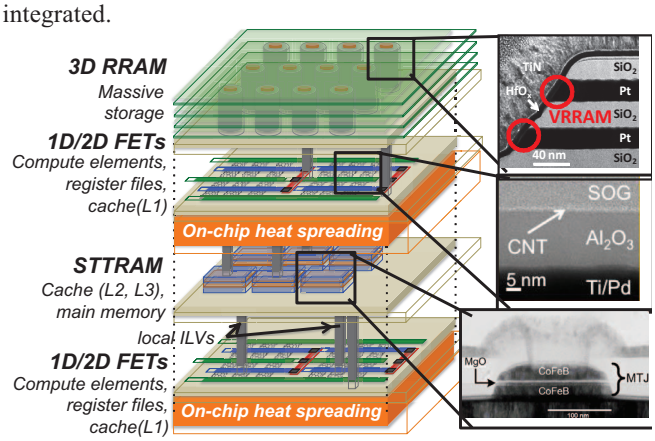

Figure 1. Monolithically integrated computing platform with CNFET-based logic circuits (for computing elements and memory access), STTRAM-based caches and main memory, and RRAM-based massive storage. The right-half portion of the figure includes the transmission electron microscopy (TEM) images of the different technologies. TEMs (top-to-bottom) from [Wong12], [Wei13], and [Smullen11].

The outline of this paper is as follows: Section II begins with a description of the current status of CNFET technology and how CNFETs can enable monolithic 3D ICs, highlighting experimental demonstrations. In Section III, we present an overview of recently achieved demonstrations of monolithic 3D integration of memory and logic, with arbitrary layering and connectivity between logic and memory layers. We discuss the architecture-level implications of monolithic 3D integration in Section IV. We conclude in Section V.

II. CNFETs For Monolithic 3D ICs

A. From Device to Systems

While CNFETs represent a promising emerging nanotechnology, substantial imperfections inherent to CNTs prevented the demonstration of digital VLSI systems using CNFETs [Zhang12]:

1) Mis-positioned CNTs: While CNT growth can achieve >99.5% CNT alignment [Patil09a], the remaining mis-positioned CNTs can cause stray conducting paths inside CNFET circuits, resulting in incorrect logic functionality [Zhang12].

2) Metallic CNTs: Due to chirality, some proportion of all grown CNTs are metallic (i.e., those CNTs have little or no bandgap), resulting in low I_{ON}/I_{OFF}, increased leakage power, and incorrect logic functionality [Zhang12].

The imperfection-immune paradigm (IIP) overcomes these inherent imperfections in a VLSI-compatible manner [Zhang12]. Mis-positioned CNT-immune layout design enables CNFET circuits that are immune to mis-positioned CNTs [Patil08]. VMR (VLSI-compatible Metallic CNT Removal) combines CNT processing with CNFET circuit design to remove metallic CNTs [Patil09b, Wei10] using chip-scale electrical breakdown. As shown in [Shulaker14a], VMR can selectively remove >99.99% of all metallic CNTs versus inadvertently removing <4% semiconducting CNTs. In addition to the above sources of imperfections, one must also pay attention to CNT-specific variations in CNFET circuits. Techniques for overcoming such CNT-specific variations are discussed in [Zhang12, Hills13, Hills15]. The entire IIP is VLSI-compatible, inexpensive, and can be applied to arbitrary logic functions; it enabled the first CNFET-based digital system demonstrations, including a CNFET-based microprocessor [Shulaker13a-b, Shulaker14a].

In addition to realizing CNFET-based digital systems, recent work has also demonstrated scalability of CNFETs to advanced technology nodes as well as high-performance CNFETs. CNFETs with sub-10 nm channel lengths have been demonstrated in [Franklin12a]; 32 nm channel length-CNFET circuits have been demonstrated in [Shulaker14b]; and, high-current drive CNFETs with high I_{ON}/I_{OFF} have been demonstrated in [Shulaker14c]. Controlled CNT doping, metal-CNT contact resistance, and hysteresis need to be further improved to realize a high-performance and energy-efficient CNFET digital VLSI technology, and recent work has shown progress in these areas [Chai12, Ding11, Franklin12b, Franklin14, Suriyasena14].

B. CNFETs: from 2D to 3D

The key to enabling monolithic 3D CNFET ICs is a low-temperature and wafer-scale CNT transfer technique that decouples high-temperature CNT growth from low-

[1] Monolithic 3D integration of silicon CMOS transistors is generally considered to be difficult. Silicon-based monolithic 3D integration has been investigated using low-temperature solid phase epitaxy and layer transfer [Tsai66, Hamaguchi85, Batude11, Mono3D].

[2] In addition to 1D materials, 2D semiconductors such as MoS_2 are promising next-generation technologies [Wang12].

temperature monolithic 3D integration [Patil09a]. The low-temperature (<130 °C) CNT transfer technique is shown in Figure 2, rendering the entire CNFET fabrication process on the final monolithic 3D IC < 250 °C [Wei09, Wei13].

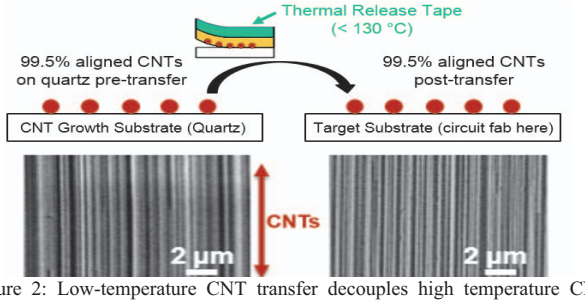

Figure 2: Low-temperature CNT transfer decouples high temperature CNT growth at 850 °C from the target substrate, which remains <130 °C during the CNT transfer process.

It is important to note that the CNT transfer process has additional benefits, as it can be performed multiple times onto the same target wafer, effectively combining multiple CNT growths together [Shulaker11]. By optimizing the CNT transfer process using a combination of new processing and design solutions, [Shulaker14c] demonstrated CNT densities of >100 CNTs/μm. This resulted in the highest current-drive CNFETs with simultaneously and consistently high I_{ON}/I_{OFF} [Shulaker14c].

After performing CNT transfer, the CNFETs on a given layer of a monolithic 3D IC are fabricated. IIP is employed for each layer of CNFET circuitry, rendering all layers immune to the inherent CNT imperfections. [Wei13] demonstrated that IIP can scale to monolithic 3D ICs with an arbitrary number of CNFET circuit layers. Specifically, as shown in Figure 3, VMR for 2D circuits relies on a highly-doped silicon substrate to act as a global back-gate. This is not scalable to 3D circuits, since the wafer substrate (a global back-gate) has diminishing control over semiconducting CNTs on the upper layers of monolithic 3D ICs.

To overcome this scalability challenge, monolithic 3D ICs leverage a new 3D-VMR technique, using local back-gates of CNFETs on each layer to maintain strong gate control, resulting in effective metallic CNT removal on each layer of the monolithic 3D IC [Wei13]. Using 3D-VMR, CNFETs exhibiting high I_{ON}/I_{OFF} (10^3 to 10^5) have been consistently demonstrated across multiple (three) layers of CNFET circuits [Wei13].

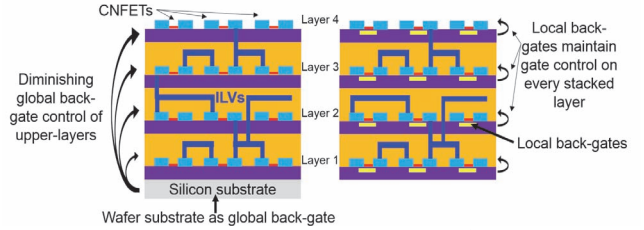

Figure 3: Schematic of 3D-VMR. 2D-VMR relies on a heavily doped silicon substrate acting as a global back-gate for CNFETs on every layer, turning-off semiconducting CNTs during electrical breakdown. With increasing number of circuit layers in a monolithic 3D IC, the global back-gate gets further away and therefore has less control over upper-layer CNFETs. 3D-VMR leverages CNFET local back-gates on each layer of a monolithic 3D IC during electrical breakdown of metallic CNTs on each layer.

The fabrication flow for CNFET-based monolithic 3D ICs is shown in Figure 4. Each circuit layer in the monolithic 3D IC follows the same repeated steps: low-temperature CNT transfer followed by CNFET circuit fabrication using IIP (3D-VMR and mis-positioned CNT-immune design). A thin inter-layer of dielectric (ILD) is deposited (<250 °C), and (conventional) nano-scale ILVs are fabricated to connect various vertical circuit layers. The process is repeated for as many vertical circuit layers as required.

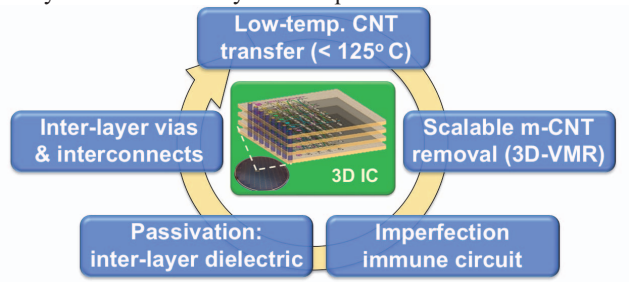

Figure 4: CNFET-based monolithic 3D IC fabrication flow. Processing details, including details of 3D-VMR, are in [Wei13].

C. *Experimental Demonstrations of CNFET-based Monolithic 3D ICs*

Several experimental demonstrations have illustrated the feasibility of achieving monolithic 3D ICs using CNFETs. Initial demonstrations showed 3 vertically stacked layers of CNFETs, while also integrating CNFETs with CNT local interconnects [Wei09, Wei13]. Transmission electron microscopy (TEM) images in Figure 5 show 3 vertically stacked layers of CNFET circuits directly overlapping one-another [Wei13].

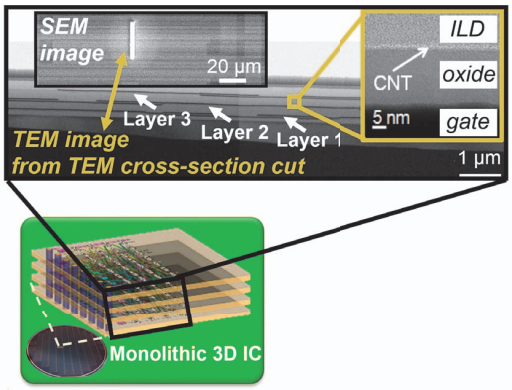

Figure 5: Scanning electron microscopy (SEM) and TEM images of a CNFET monolithic 3D IC, consisting of three layers of overlapping CNFETs. As shown in the inset, a metal local back-gate is used with high-k gate dielectric to form the CNFETs. An ILD is deposited over each layer of CNFETs and planarized. The next layer of CNTs is transferred over the ILD, continuing for as many circuit layers as required.

We demonstrated the flexibility of our integration approach through CNFET digital logic circuits across 3 vertical layers of monolithic 3D ICs, with fully-complementary intra-layer logic gates (logic gates in digital circuit on multiple vertical layers and interconnected using nano-scale ILVs) and inter-layer logic gates (logic gates consisting of CNFETs split between multiple vertical layers and interconnected using nano-scale

ILVs). Figure 6 shows fully complementary inter-layer CNFET logic circuits, fabricated in a VLSI-compatible manner. The complementary logic circuits could operate correctly at supply voltages all the way down to 0.2V and are cascadable, while spanning multiple layers of a CNFET monolithic 3D IC [Wei13]. Figure 6(c) shows one-such cascaded (multi-stage) CNFET logic circuit fabricated across 2 vertical layers.

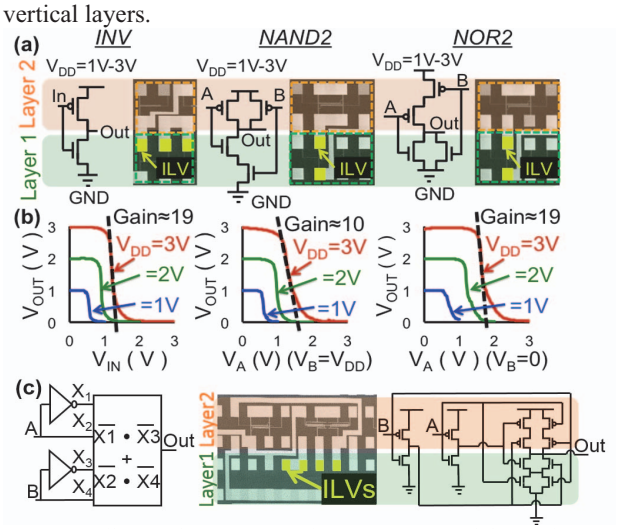

Figure 6: Fully complementary inter-layer CNFET monolithic 3D logic gates, enabled by 3D-VMR [Wei13]. (a) Schematics and SEM images of inter-layer INV, NAND2, and NOR2 logic gates. Conventional nano-scale ILVs instead of TSVs are used to connect the pull-up and pull-down networks on two separate layers. (b) Measured voltage transfer curves show correct operation and gain ≥ 10 for each type of logic gate, for V_{DD} = 3V all the way to V_{DD} = 1V. (c) Cascaded (multi-stage) fully-complementary CNFET logic circuit, consisting of inter-layer and fully-complementary monolithic 3D inverters followed by an inter-layer and fully-complementary monolithic 3D complex gate.

Additionally, monolithic 3D integration of CNFETs has been demonstrated on silicon FETs, showing that our monolithic 3D process flow is silicon CMOS compatible [Shulaker14d]. As shown in Figure 7, fine-grained monolithic 3D integration is achieved at the logic gate level, whereby individual fully-complementary logic gates are composed of both CNFETs and silicon FETs stacked directly vertically over each other and interconnected using nano-scale ILVs; integration is also achieved at the circuit-level, with CNFET logic gates on the upper circuit layers cascaded to silicon CMOS logic gates underneath, creating hybrid monolithic 3D CNFET-silicon CMOS logic circuits.

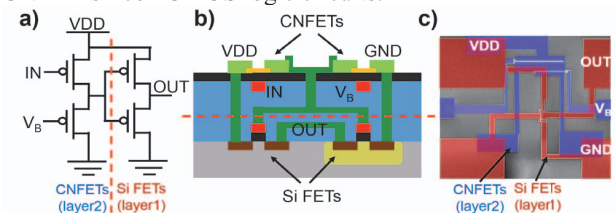

Figure 7: Monolithic 3D integration of CNFETs over silicon FETs. (a) Circuit schematic of cascaded inverters. 1st inverter implemented with CNFETs on the 2nd layer of circuits. 2nd inverter implemented with silicon-CMOS on the 1st layer of circuits. (b) Cross-section of CNFETs fabricated directly over silicon-CMOS, connected using conventional ILVs. (c) SEM image of the fabricated circuit illustrated in (a-b).

III. Monolithic 3D Integration of Logic and Memory: Experimental Demonstration

We recently demonstrated monolithically-integrated 3D ICs with both logic and memory layers [Shulaker14e]. Building on our monolithic 3D integration of CNFET logic (Sec. II), we used the low-temperature CNFET fabrication flow for the upper layers of logic in the monolithic 3D IC. We used RRAM for the memory layers using a low-temperature fabrication process (<200 °C). RRAM is a promising emerging technology for realizing a high-capacity storage and back-end-of-line (BEOL)-compatible NVM [Wong12].

The RRAM and CNFET logic layers were fabricated on a silicon CMOS substrate, demonstrating that the entire process is not only VLSI-compatible, but also silicon CMOS compatible. As shown in the TEM images in Figure 8, the monolithic 3D IC has 4 vertically-stacked layers: a logic layer (silicon FETs), a memory layer (RRAM), another memory layer (RRAM), and another logic layer (CNFETs). The layers overlap each other, and are connected using conventional nano-scale ILVs (i.e., we do not use any TSVs).

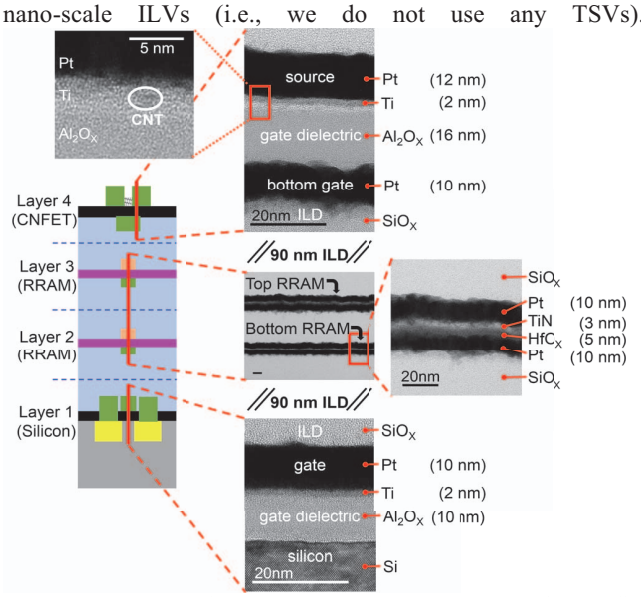

Figure 8: Transmission electron microscopy (TEM) images of each vertically-stacked layer in the 3D IC. Silicon-FETs are on the bottom layer, followed by two layers of RRAM, followed by the top layer of CNFETs.

We demonstrated arbitrary connectivity between layers, and that the performance of both logic and memory elements in the monolithic 3D IC were invariant to their vertical stacking order (i.e., the performance of the silicon FETs, RRAM, and CNFET logic show negligible change before and after the vertical layers were fabricated) [details in Shulaker14e].

To demonstrate correct functionality of the resulting monolithic 3D IC integrating both logic and memory, we fabricated a 4-layer routing element of an FPGA, schematically shown in Figure 9. As shown in Figure 10, the configuration memory is implemented using 2 RRAM cells, the select transistor to program the RRAM cells in (either a high or low resistance state) is implemented using a CNFET, while the routing transistor in implemented using a silicon FET. The RRAM cells, CNFETs, and silicon FETs are

stacked vertically in a 4-layer monolithic 3D IC. Figure 10(b) demonstrates correct circuit operation of the routing element by switching the routing transistor between on and off states.

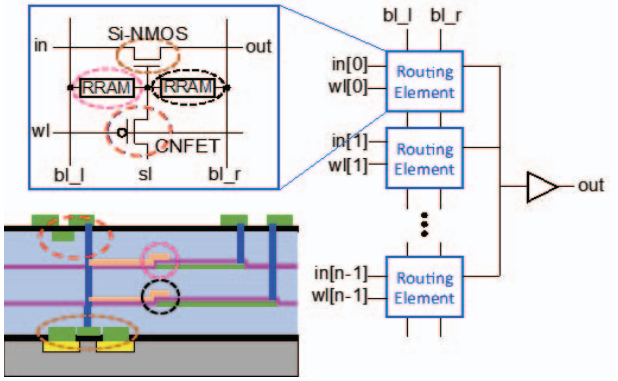

Figure 9: Schematic of the 4-layer routing element containing 2 RRAM cells to form configuration memory, a CNFET select transistor to program the RRAM in either a high or low resistance state, and a silicon FET-based routing transistor. Each element is on its own layer. Elements are interconnected using nano-scale ILVs.

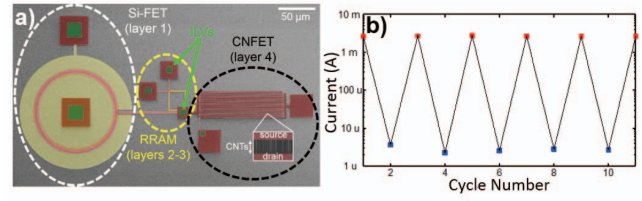

Figure 10: Monolithic 3D routing element for an FPGA. (a) SEM (false colored) of the routing element consisting of a CNFET select transistor for the 2 RRAM cells and the silicon routing transistor. All these elements are on different layers of a monolithic 3D IC, and are interconnected using nano-scale ILVs. (b) Results for the FPGA routing element, showing difference of ~1,000X between I_{ON} and I_{OFF}.

IV. Architectural Impact of Monolithic 3D ICs

We expect that the significant technology-level advances in monolithic 3D integration (as demonstrated in Sec. II and Sec. III) will have direct impact on architectures of 3D ICs. The resulting question is: *Which applications would benefit the most from monolithic 3D ICs and by how much?* Abundant-data applications (e.g., big-data analytics on structured or unstructured data with massive volume and rate [Russom11]) impose stringent system-level requirements such as low-latency processing, high-bandwidth transfer, and energy-efficient storage of massive amounts of data [Satish14].

Monolithic 3D ICs with fine-grained integration of logic and memory can enable significant EDP benefits compared to the state-of-the-art computing system architectures (and TSV-based 3D architectures as well), due to the EDP benefits of CNFETs, the improved energy-efficiency of emerging non-volatile memories, and the massive vertical connectivity.

Significant improvements in memory bandwidth, enabled by monolithic 3D integration, can help overcome memory wall bottlenecks of computing systems. This raises the following question: *How should various architectural blocks be re-designed in monolithic 3D context?* Conventional computer architectures often assume that memory access latencies are orders of magnitudes longer than the time spent on actual computations. Accordingly, various architectural techniques are used to hide memory latencies. With low-latency and high-bandwidth memory accesses in monolithic 3D ICs, it may be possible to simplify the design of various micro-architectural blocks (and, hence, further improve energy efficiency). Memory interfaces are also expected to undergo redesign because they can now take advantage of improved memory bandwidth and latency, as well as the non-volatile nature of emerging NVM technologies.

Monolithic 3D integration requires deep understanding of variability, yield, and reliability. To that end, we have created a preliminary framework for CNFET circuit design [Hills13, Hills15] based on hardware-calibrated device models [Luo13] which is 100-fold faster than existing approaches. This enables us to rapidly explore the large space of interplay between CNT variations, energy, delay, noise margin, and circuit-level functional and performance yield. Monolithic 3D integration of logic and memory requires detailed study of ways to manage yield, variability, and reliability at the device, circuit, and architecture levels. We have also developed SPICE device models for emerging memories such as RRAM to enable such detailed studies [Jiang14].

With monolithic 3D, thermal cooling of ICs is expected to require significant redesign. Although the use of energy-efficient CNFETs can result in lower heat generation, the large number of layers in monolithic 3D ICs can result in a substantial increase in on-chip heat flux. These thermal challenges are exacerbated by the use of thin-film inter-layer dielectrics that reduce the thermal conductivity of the dielectric material [Pop10].

V. Conclusion

Emerging logic (e.g., CNFETs) and NVM technologies promise both continued scalability and increased energy efficiency of electronic systems beyond silicon CMOS. Moreover, these nanotechnologies provide a unique opportunity for monolithic 3D integration, enabled by low-temperature processing. Monolithically-integrated 3D ICs, consisting of CNFETs and silicon FETs for logic layers and emerging NVM such as RRAM for the memory layers, have been demonstrated. All fabrication processes are VLSI-compatible and silicon CMOS compatible. Thus, monolithic 3D integration is morphing from an idea to reality. The paradigm shift in computing due to monolithic 3D integration of logic and memory with high density inter-level vias can enable new generations of computing systems with unprecedented levels of energy efficiency and performance especially for abundant-data applications.

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