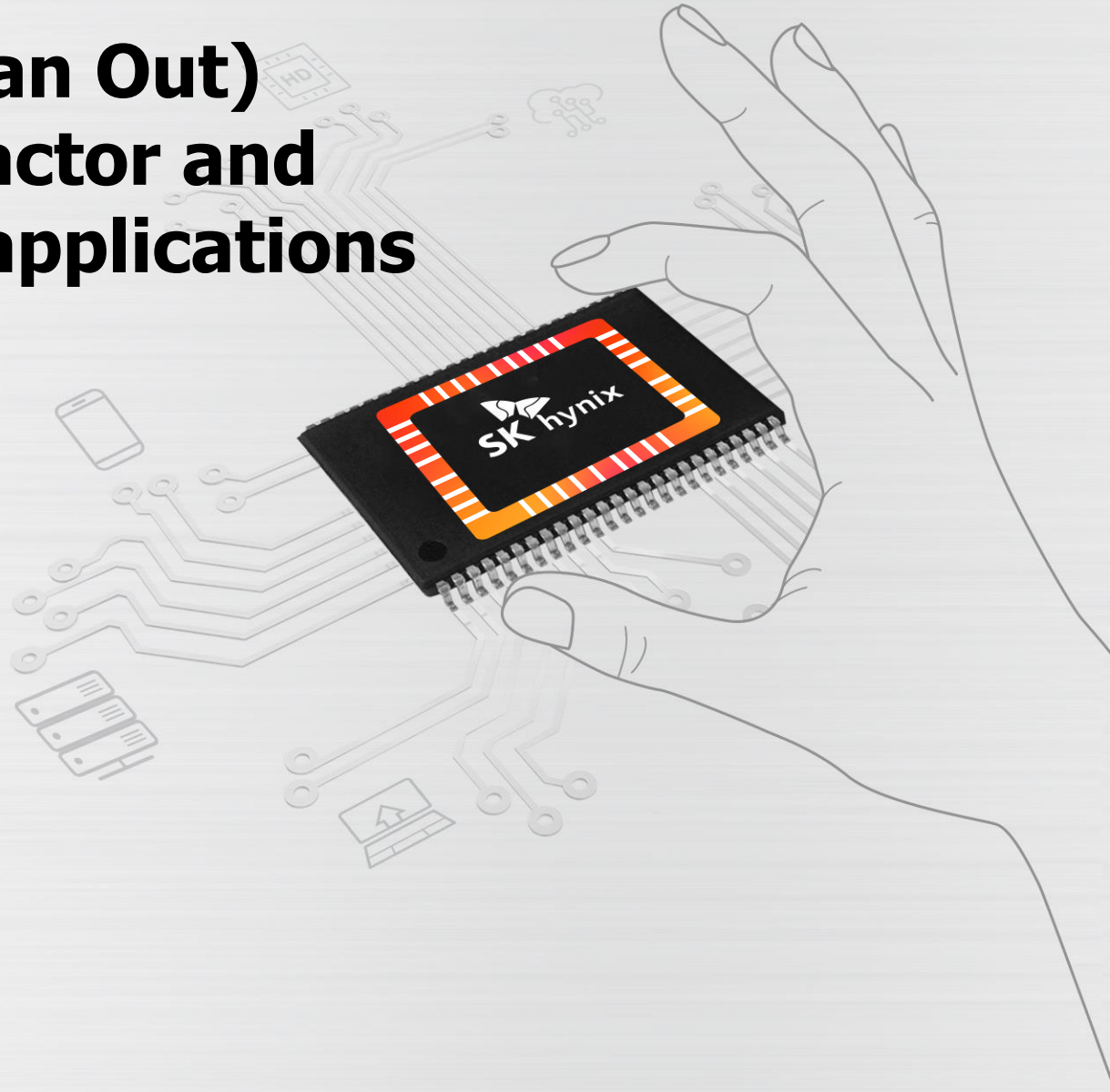
Confidential

A noble VFO(Vertical wire Fan Out) technology for small form factor and high performance memory applications



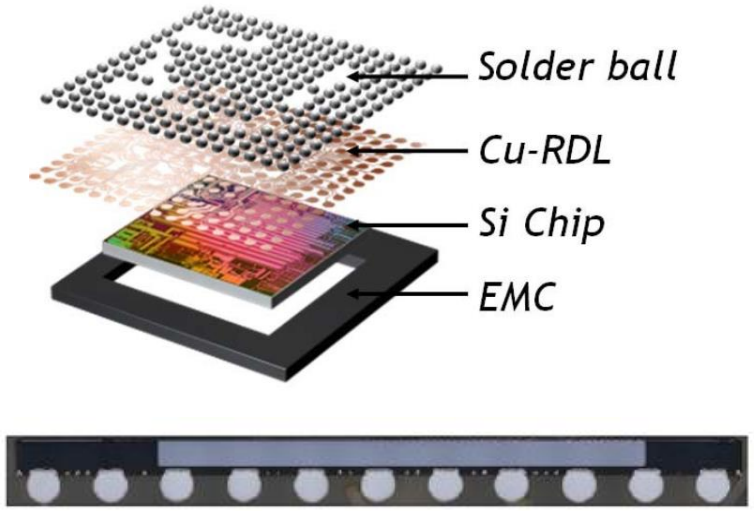
OCT. 2023

Advanced PKG TD, SK hynix Inc.

SK hynix

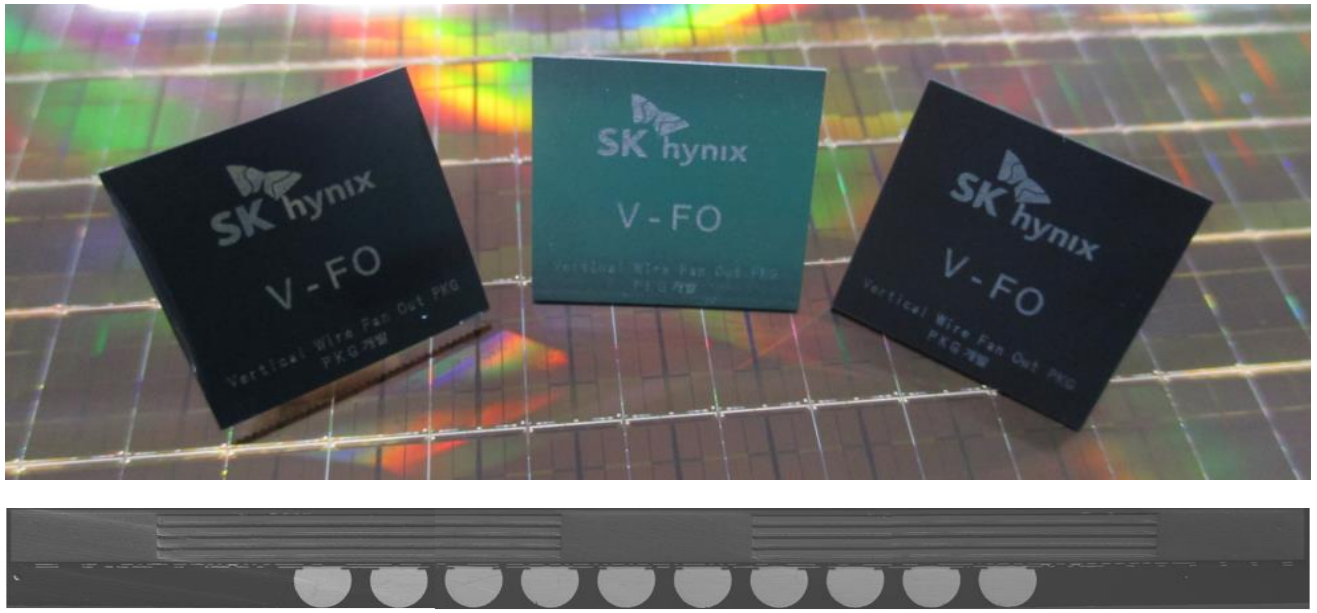
SK hynix's FOWLP technology

Fan Out Package



- Single or dual Die
  (Non-stacked dies)
- Peripherals application
  (RF, PMIC and AP)

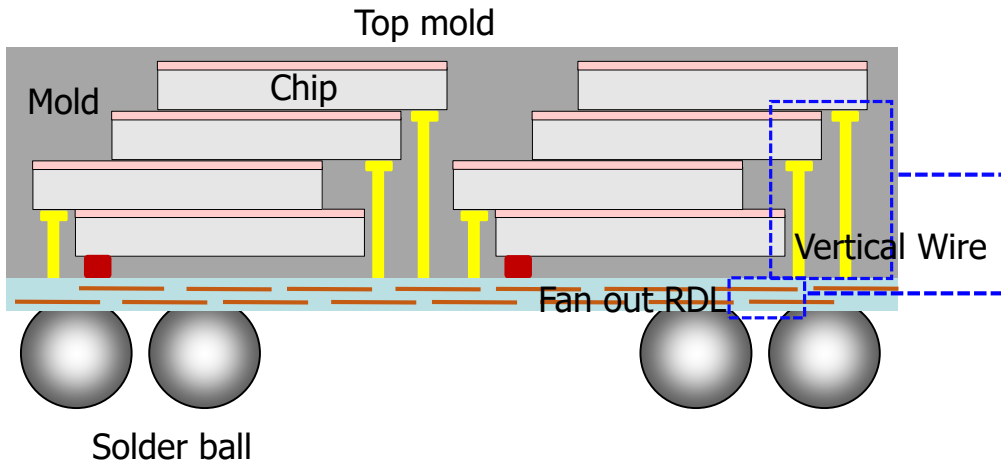
VFO™ (Vertical Fan Out package)



- **Short vertical wire**
- **Multi stacked memory dies**
- **Multi layer fan out RDLs**

VFO's technologies

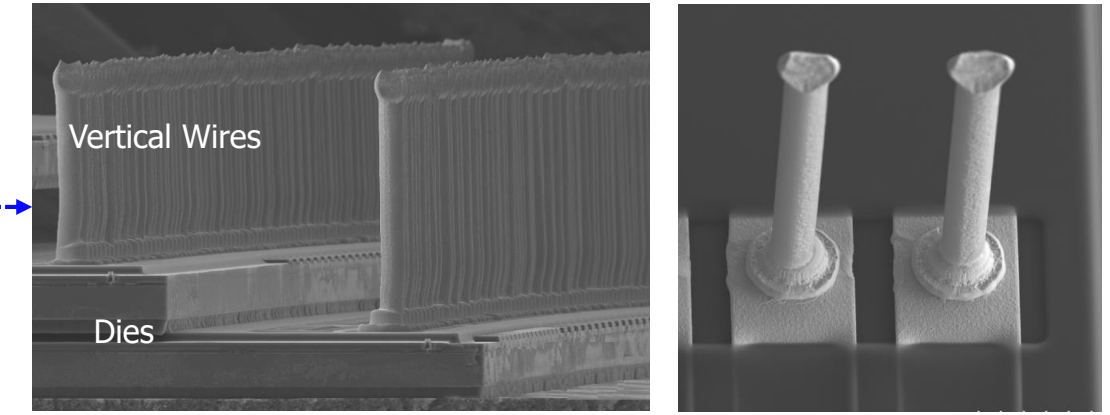
VFO has "Vertical-Wires" and " Fan Out RDLs" for high density DRAM



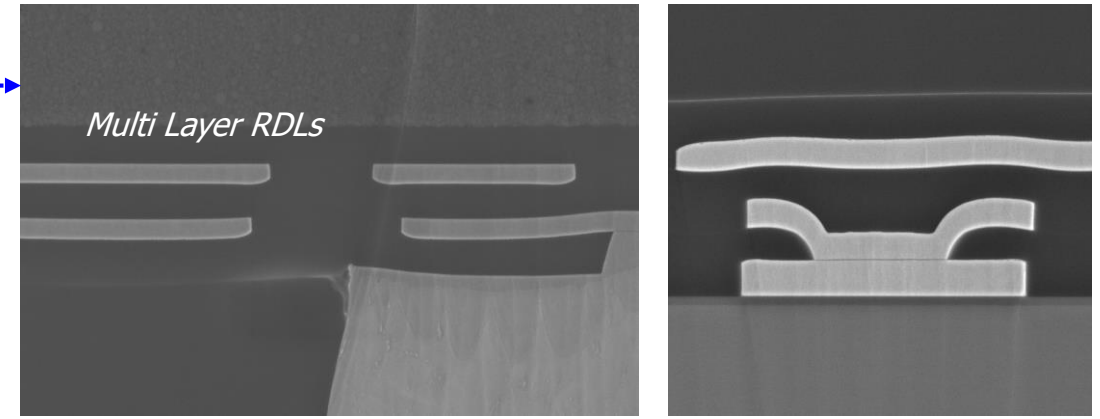
< VFO packaging process >

- **Wafer level vertical wire bonding**
- **Wafer level Molding**
- **Wafer level RDLs**

<Vertical Wire on stacked dies>

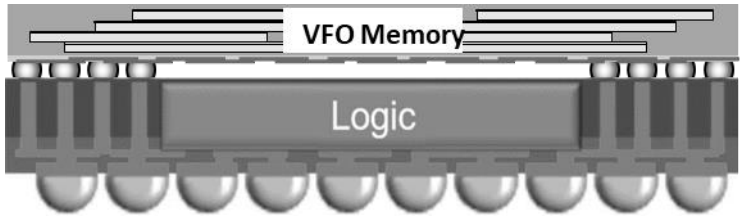


<Fan Out RDL on molded wafer >

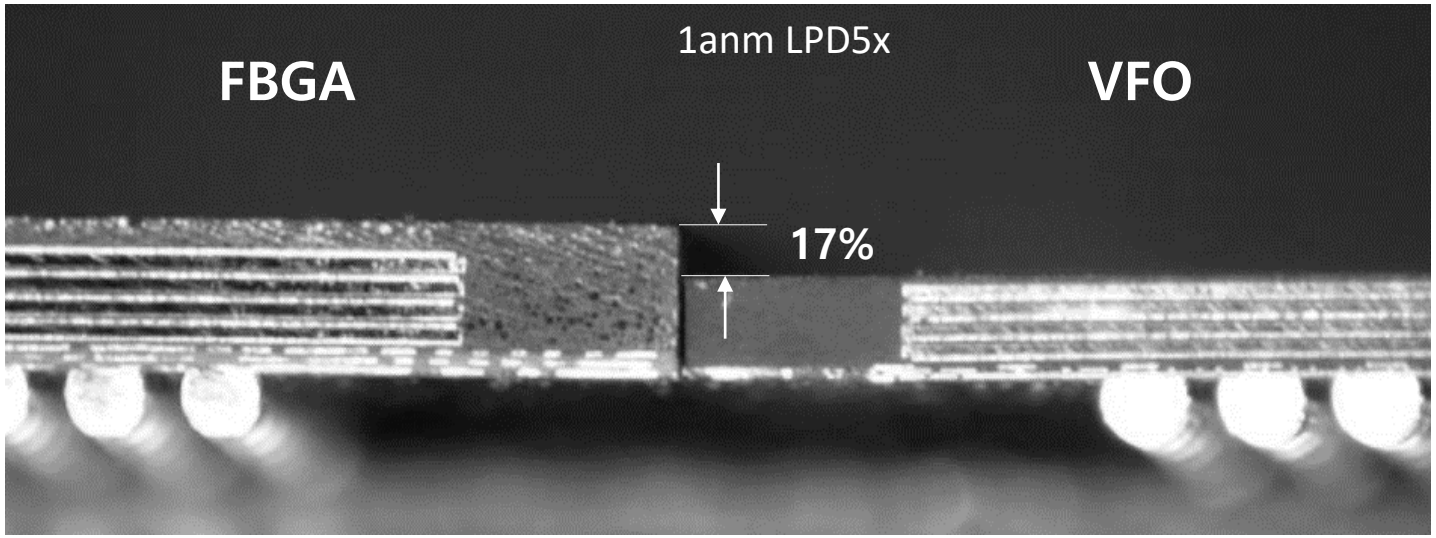


Comparison of package height

VFO is approx. 17% thinner than FBGA height, despite same chip height



<Mobile PoP with VFO PKG>



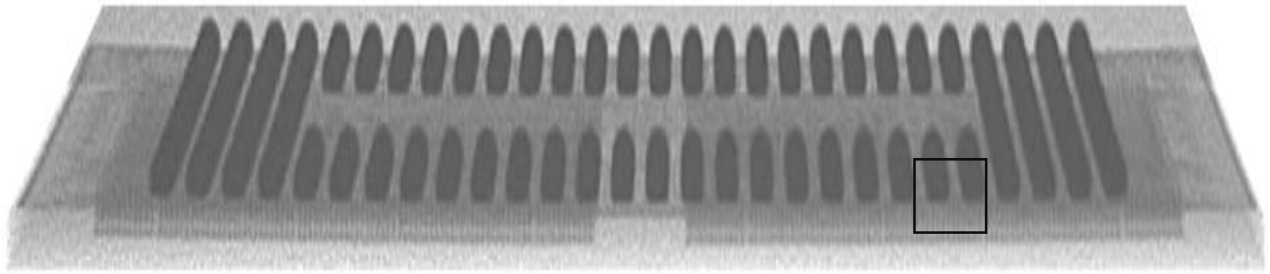
<Overall package thickness>

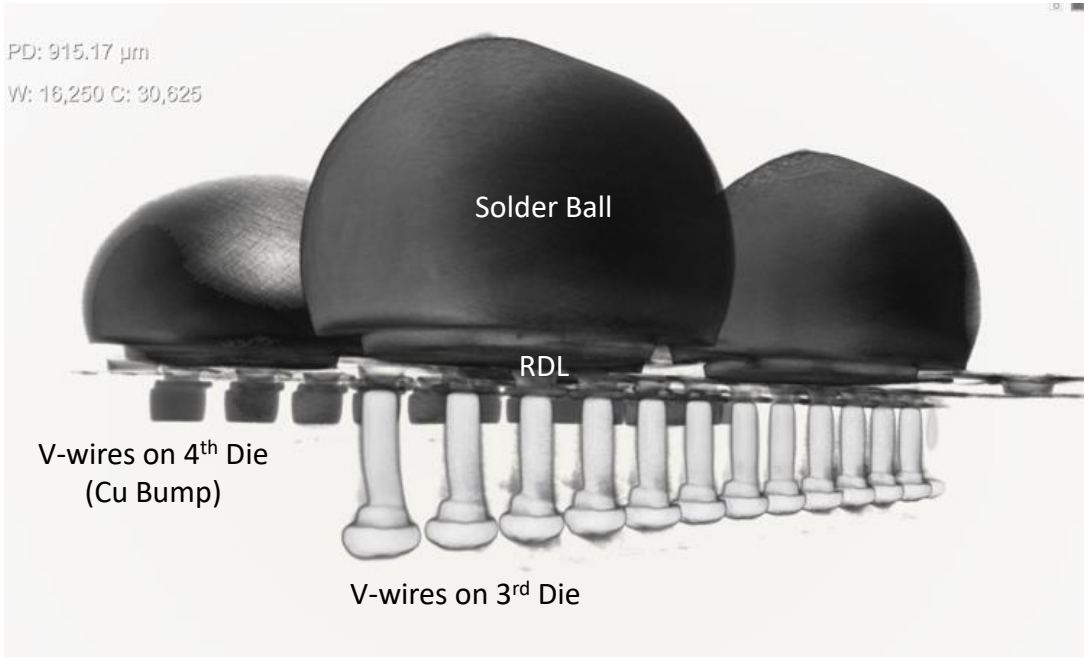
	FBGA	VFO
Structure	2L_4 Hi	2L_4 Hi
Substrate/RDL	90um	40um
Package body	330um	260um
Mold Top	110um	20um
Solder ball	200um	200um
Overall PKG height (w warpage)	**710um**	**590um**

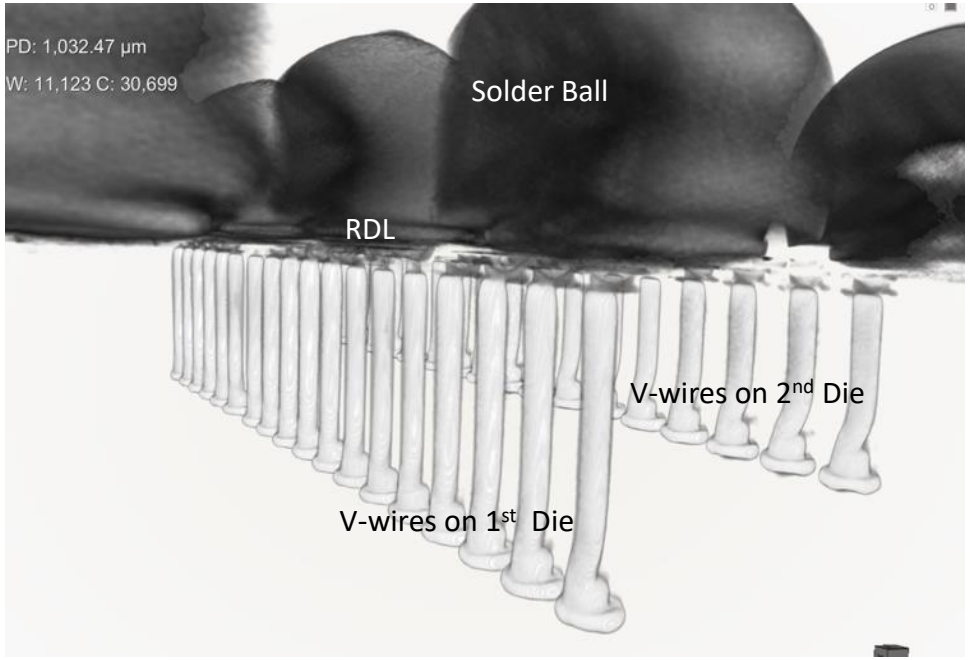
VFO's mechanical analysis

No vertical wire distortions was found in joints with multi layer RDLs

<Vertical wires in a PKG by 3D scan>





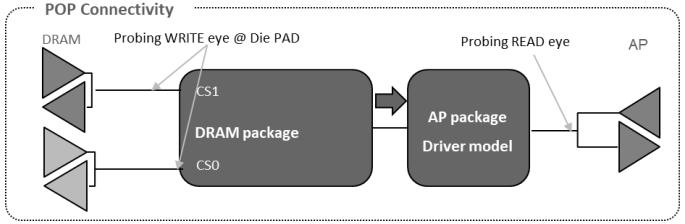


Electrical Characteristic

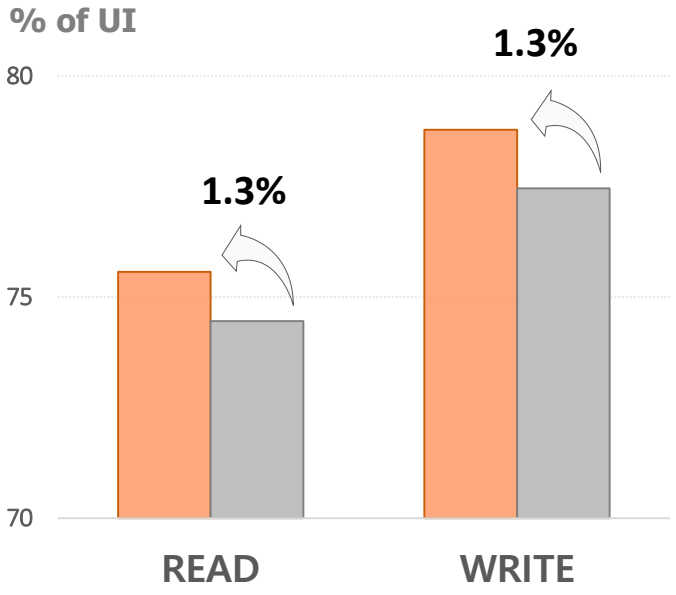
VFO shows high SI performance & Enhanced PDN impedance

<Simulation Condition>

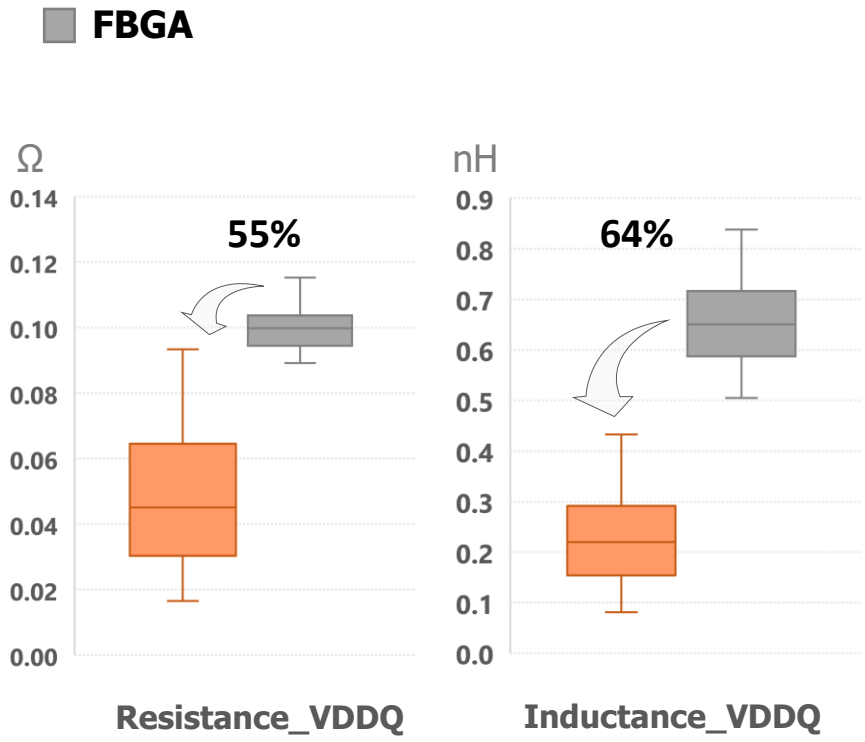
- Data path: READ / WRITE
- Driver model(Tx/ Rx)
  DRAM- 1anm LP5x(8533Mpbs),
- AP- A company
  Corner: T
- Channel Topology (Below)



<System Integrity>



<Power Integrity>



Thermal Characteristic

VFO provides more valuable thermal performance

<JEDEC Standard>

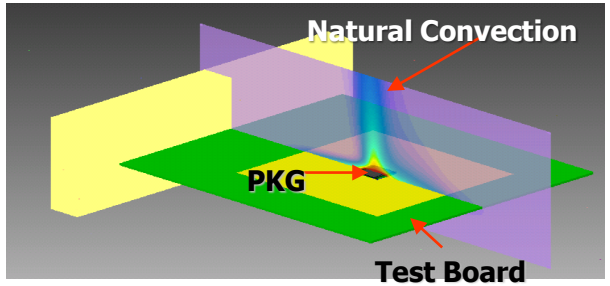
- No. of Elements at 1 Model: About 300K
- Test Board : 2s2p(2signals 2planes : high conductivity)
- Ambient Temperature : 25°C
- Power Dissipation : 1W

Boundary condition	JEDEC	
TEST Board	*JESD 51-9*	*2s2p (2signals 2planes)*
ΘJB	*JESD 51-8*	$(T_j - T_b)/Power[℃/W]$
ΘJC	*JESD 51-14*	$(T_j - T_c)/Power[℃/W]$

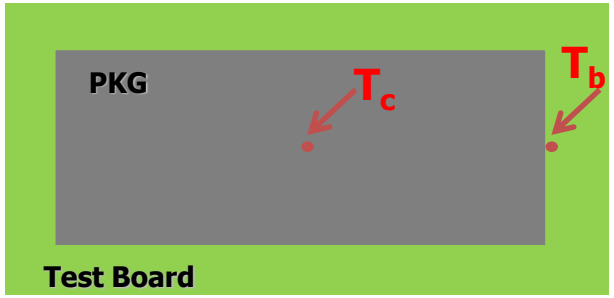
<Simulation Results>

	FBGA	VFO
ΘJa	24.3 ℃/W	23.0 ℃/W
ΘJb	7.6 ℃/W	7.5 ℃/W
ΘJc	1.5 ℃/W	1.2 ℃/W

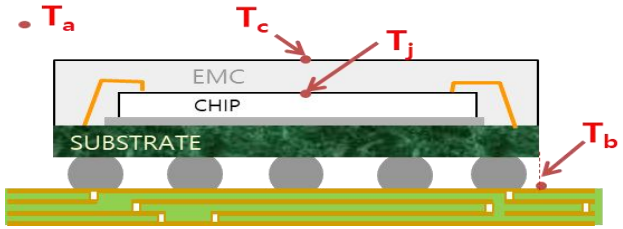
<Measurement point>



Top view



X-section view



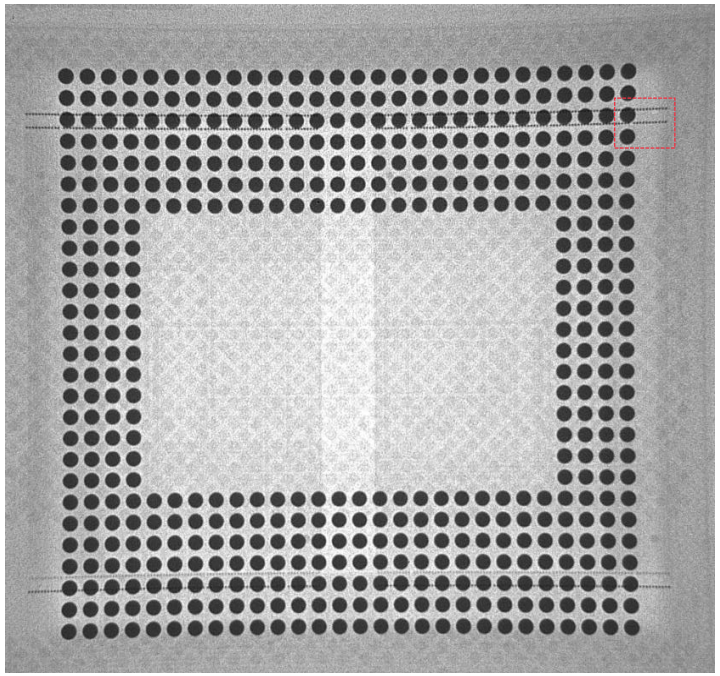
Package reliability

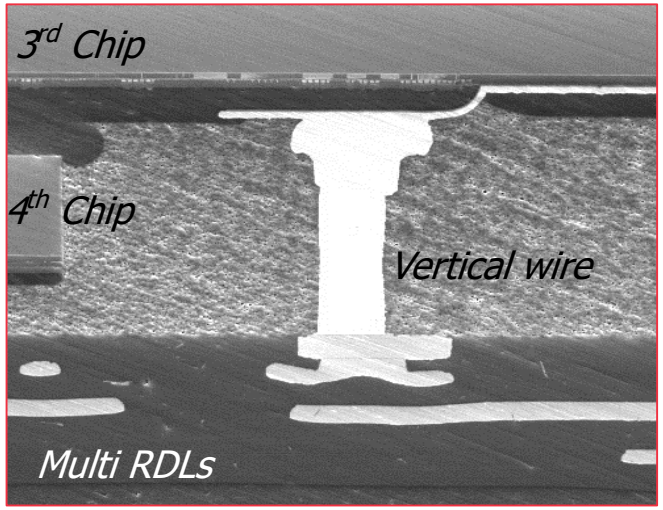
The results of reliability were passed without any failure

<Reliability test results of VFO>

TEST	Condition	VFO
TCB	-55~125°C/1000C	Pass
uHAST	110°C/85%, 168hrs	Pass
HAST	130°C/85%, 96hrs, Applied voltage	Pass
HTS	150°C/1008hrs	Pass

<X ray & Vertical Wire>





VFO technical benefits summary

VFO gives a lot of technical benefits for mobile applications

4hi-stacked dies are available in 3Q ’24

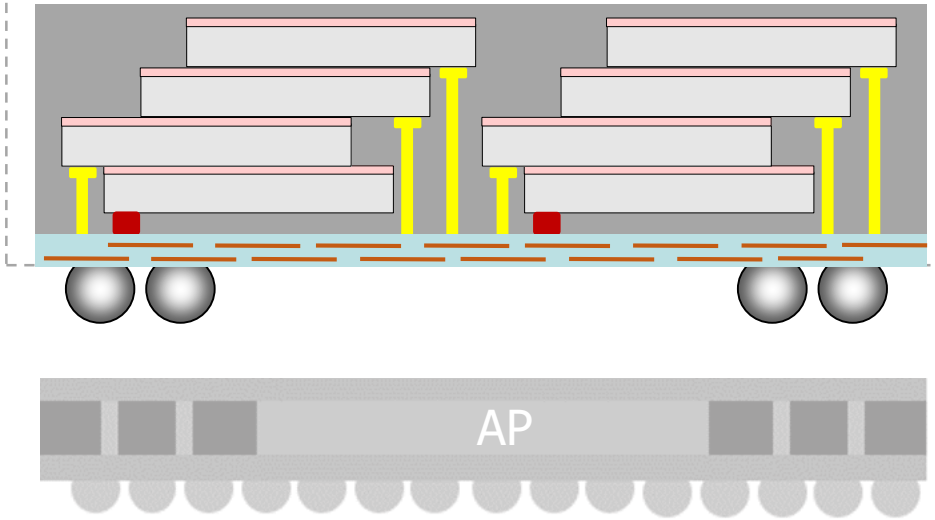
① Ultra Thin PKG Height
Thin mold top and RDL height

② PKG Design Flexibility
Smaller X-Y PKG Size

③ Enhanced Electrical Perf.
High SI and PDN properties

④ Removed Sub. dependence
Fully in-house process in SKH

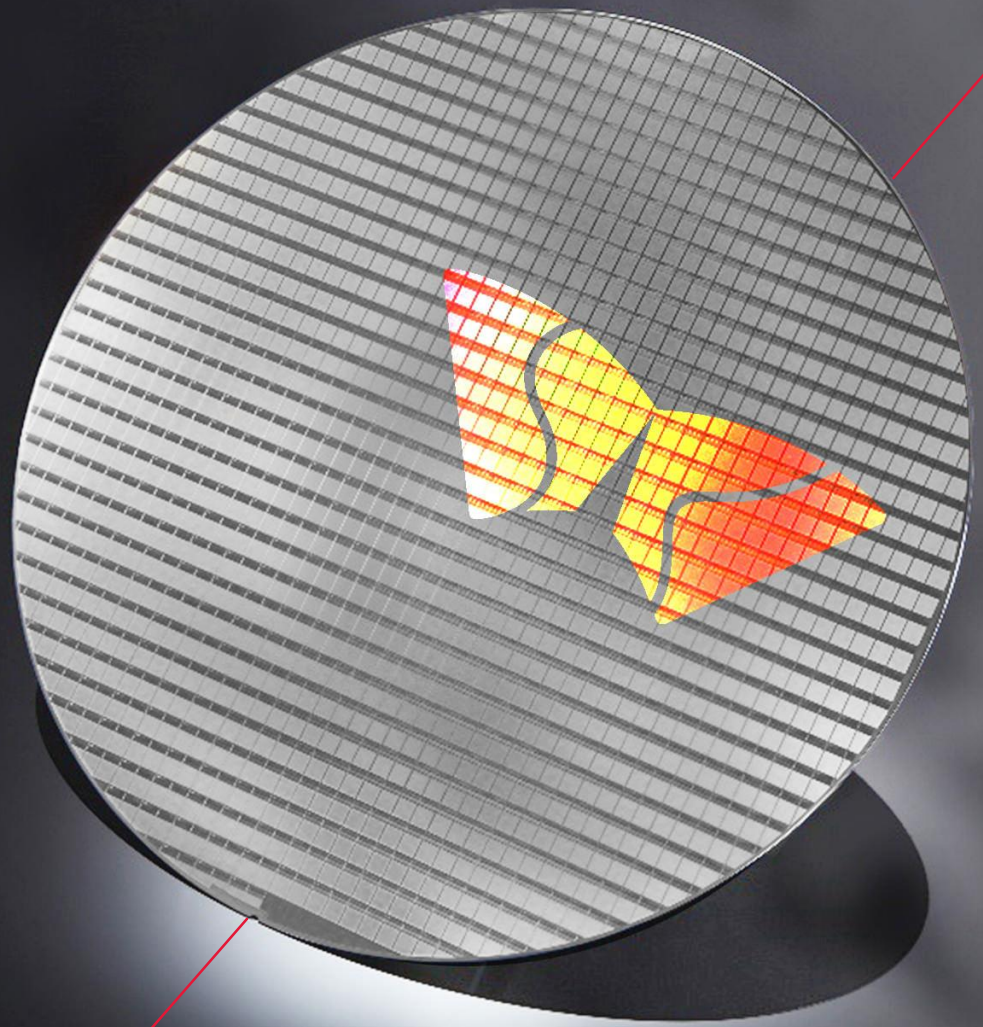
⑤ Effective heat dissipation
Thin mold top and RDL height



[Vertical wire Fan-Out Package in PoP System]

Summary

- **Mobile application needs high performance, small form factor and high thermal characteristic**
- **A noble VFO for memory packages has been developed by SK hynix**
- **VFO excelled at mechanical, electrical and thermal performances will be one of the best solutions in thin mobile packages**
  - It's package z-height was reduced by 17%
  - Electrical performance was better by 1.3% and 1.3%
  - Thermal properties was improved by about 1.4%
- **It will lead small form factor and high performance memory applications in packaging industries.**



THANK YOU

SK hynix