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Advanced Packaging Update: Market and Technology Trends, Vol. 3, October 2021

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Advanced Packaging Update: Market and Technology Trends

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Advanced Packaging Update

This issue of the Advanced Packaging Update features a financial analysis of OSATs, including performance metrics. Continuing semiconductor shortages and supply chain disruptions are discussed, including an update on automotive electronics. The special section on packaging trends for advanced semiconductor nodes includes a package forecast for silicon interposers and high-density fan-out. Packaging challenges for chiplets and especially 3D are discussed. Trends in high bandwidth memory (HBM) are discussed and a market forecast is provided.

1 Industry and Economic Trends

This section examines general macroeconomic trends in the world economy and microeconomic trends in the semiconductor packaging and assembly industry.

1.1 Economic Trends

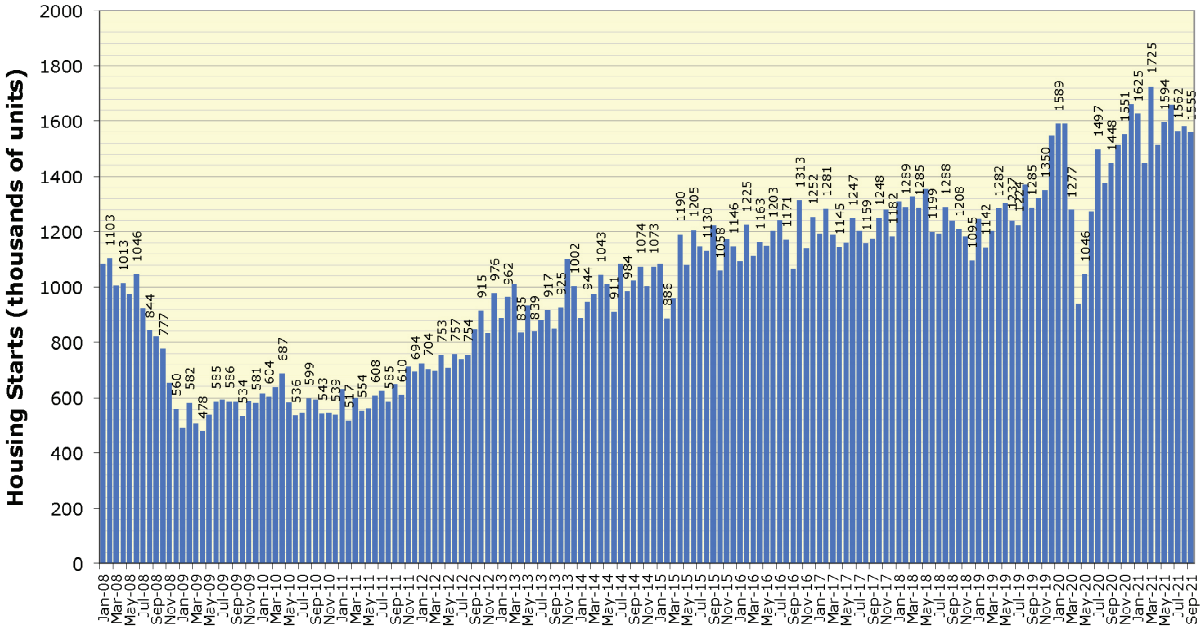
The World Bank expects the global economy to expand 5.6 percent in 2021, which is the strongest post-recession pace in 80 years. However, the recovery is uneven and largely reflects sharp rebounds in some major economies.

The World Trade Organization (WTO) has revised its growth forecasts for global goods trade higher for this year and 2022, but warns of a two-track recovery leaving poor countries behind and downside risks from the COVID-19 pandemic and supply chain problems. After a decline of 5.3 percent in 2020, the WTO forecasts trade will grow 10.8 percent this year. Growth in 2022 is projected to be 4.7 percent. Low-income countries where vaccines have not been administered are lagging [1].

Federal Reserve Chairman Jerome Powell said that a recent spell of higher inflation might last longer than central bank officials had anticipated, but the price surge will eventually fade [2].

U.S. Commerce Department data show housing start trends, an important economic indicator for the economy (See Figure 1.1). In September, U.S. housing starts decreased 1.6 percent to a seasonally adjusted rate of 1.555 million units. This is the lowest level since April. Data for August was revised down to 1.580 million units from the previously reported 1.615 million units.

Figure 1.1. Monthly U.S. housing starts.



Source: U.S. Department of Commerce.

The U.S. Bureau of Labor Statistics reported a 4.8 percent unemployment rate in September, the lowest since February 2020. This is a 0.4 percentage point decline from the August rate. However, the economy added only 194,000 non-farm jobs in September, much lower than the expected 500,000 jobs.

1.2 China's Power Shortage

Power shortages in China are curtailing factory output in manufacturing segments across the board. The power shortages are caused by a shortage of coal. Flooding in China's coal producing region reduced the output of mines. To help alleviate the shortage, China just reversed its almost year-long ban on the purchase of Australian coal. The coal shortage is expected to last through Q4 and possibly into February or March when the heating season ends [3]. China is also pushing ahead with goals to cut carbon emissions. Clearing the air for the 2022 Winter Olympics in Beijing is driving the desire to reduce coal emissions, but clearly the shortage is the main reason for the reduced factory output in regions including Jiangsu Province (includes Suzhou and Kunshan), Hubei, and Guangdong. Factory operators do not know how long the power restrictions will last, but they are being informed of power cuts eight to ten hours in advance. Long term forecasts are not provided by the local governments.

The power shortage is impacting production of metals including aluminum and steel; soybean processing; fertilizer; polysilicon used in solar panels; and other products [4]. China's semiconductor foundries are excluded from power cuts.

In the electronics industry, power shortages are impacting the production of PCBs, copper clad laminate (CCL), semiconductor package assembly, and materials ranging from solder balls to underfills. Production at China manufacturing sites of Taiwan headquartered PCB makers including Dynamic Electronics, Flexium Interconnect, Gold Circuit Electronics, Nan Ya PCB, and Unimicron Technology has been impacted. Ten Taiwan-based semiconductor-related companies filed announcements on the Taiwan Stock Exchange that they temporarily closed China facilities in September [5]. Production in China accounts for 37.3 percent of Taiwanese multilayer PCB production, with high-density interconnect (HDI) boards accounting for 19.1 percent. Flex circuit production in China by Taiwanese companies accounts for 26.7 percent of their production [6]. PCB consultant Hayao Nakahara estimates that China accounted for as much as 60 percent of the world's PCB production in 2020, the dollar value includes assembly services.

EMS companies are also impacted by the power shortages. These include Pegatron, which assembles some of Apple's products. IC test operations such as KYEC are also impacted. [7]. LCD module makers in southern and eastern China have been impacted by the power shortage.

Power restrictions in Suzhou impacted Apple, Tesla, Microsoft, HP, and Dell. The restrictions interrupted assembly and test operations for Qualcomm, NVIDIA, and Intel [8]. The restrictions have also impacted the production of test sockets, passive devices, and other components.

Many leadframe manufacturers also have production facilities in China. Thirty-three of the 59 suppliers listed in SEMI/TechSearch International, Inc. Global Semiconductor Packaging Materials Outlook report have production in China. While not all are impacted by the power shortage, leadframe production is already tight. Supply has been restricted by copper shortages as well as insufficient capacity to meet demand. Leadframes are expected to be in short supply through mid-2023.

Production sites in China account for some of the world's semiconductor packaging material production, such as underfill, die attach, and solder balls.

China sites also account for an increasing share of the world's semiconductor assembly services. Flip chip bumping and wafer level package (WLP) capacity is also located in China (see Table 1.1). This capacity includes domestic Chinese companies as well as overseas companies with operations in China.

Table 1.1. Bumping and WLP Capacity in China

Product/Service	China Share of World Capacity
Gold Bumping	36%
Flip Chip Wafer Bumping	16%
WLP	12%

Source: TechSearch International, Inc.

1.3 Shipping Disruptions

Supply chain disruptions continue to cause problems for all industries. The transportation of goods from Asia to the U.S. remains backed up. Ships remain outside West Coast ports waiting to unload. Goldman Sachs indicates that as of the end of October, 77 ships carrying $24 billion worth of goods are waiting outside docks in Los Angeles and Long Beach, California [9].

There are many reasons for this logistical nightmare. Freight-handling equipment is not where it is needed, and there are not enough warehouse workers or truckers. The pandemic increased demand for goods and exposed weaknesses in the U.S. transport system such as investment shortfalls at key ports, controversial railroad industry labor cuts, and chronic collaboration failures among key players. For goods to move seamlessly from overseas factories to the U.S., oceangoing vessels, shipping containers, cargo terminals, truckers, chassis providers, and railroads must all be coordinated for planning purposes. The executive director of the Port of Los Angeles stated that concerns over data privacy, business secrets, and security have resulted in a fragmented approach. Individual ports operate as separate fiefdoms rather than as part of a national system. This is in contrast to ports in other countries. In Rotterdam, Europe's largest port, everyone involved in a cargo vessel's arrival sees the same information on a common data-sharing platform called PortXchange. The software makes port calls smarter and more efficient than the use of separate systems or the telephone. New Orleans is the only U.S. port that is testing a tool called Port Optimizer, which forecasts three weeks of incoming cargo. Information sharing and transparency are necessary, especially with the historic amount of goods being imported by the U.S. The L.A.-Long Beach complex, which handles 36 percent of U.S. imports, has lagged East and Gulf Coast facilities over the past decades, $11 billion to $1 billion [10].

These issues are not expected to be resolved until the end of 2022 at the earliest. But the cost of shipping between China and the U.S. plunged in the first week of October because the power shortage in China has reduced the volume of products shipped. An executive with a Shanghai freight company indicates that the cost of shipping a 40-foot container from China to the U.S. West Coast dropped nearly half, decreasing from $15,000 to just over $8,000. The spot rate for shipping to the East Coast has fallen by more than one-quarter from over $20,000 to less than $15,000 [11].

1.4 Semiconductor Shortages

World Semiconductor Trade Statistics (WSTS) predicts that the worldwide semiconductor market will grow to $551 billion in 2021, representing 25.1 percent growth for the year.

The current semiconductor shortages continue, especially for the auto industry. More than half of the companies surveyed by IPC say they expect the shortage to last until at least the second half of 2022. The chip shortage is being exacerbated by

rising cost and a shortage of workers. According to the IPC survey, 80 percent of chip makers say that it has become difficult to find workers specifically trained to handle the highly toxic compounds used in semiconductor manufacturing. The problem is worse in North America and Asia, where there are more companies reporting rising labor costs than in Europe. Rising material costs were also reported as a problem by 90 percent of the companies [12].

Semiconductor shortages, trade restrictions, and a new co-build, co-share arrangement between Chinese telecom companies are impacting the number of base stations that will be deployed this year in China. China accounts for more than 60 percent of the global 5G market. Output of base station parts decreased 53 percent from January to August, compared to the previous year, according to China's National Bureau of Statistics [13]. Spending on 5G networks and other infrastructure by Chinese telecommunication companies decreased 25 percent in the first half of the year, which would normally be the peak time for building out infrastructure [14]. Less than 600,000 base stations will be installed by the end of this year.

Component shortages are impacting shipments of wire bonders. Lead times are up to 42 weeks for some suppliers. When one component shortage is resolved, another one appears. Some suppliers have been able to decrease the lead times to four to five months.

Semiconductor production capacity continues to be added for both 200mm and 300mm wafer production. There are concerns that the industry could reach a situation of overcapacity, as it has experienced in the past.

IDC projects the semiconductor market will grow by 17.3 percent in 2021 and reach potential overcapacity by 2023. Capacity utilization in the industry is reported to be almost 100 percent. Growth is driven by applications including mobile phones, notebooks, servers, automotive, smart home, gaming, wearables, and Wi-Fi access points. Memory prices are projected to increase. IDC believes that 2022 will be more balanced.

1.4.1 Automotive Sector

The automotive industry is expected to lose out on $210 billion in revenue in 2021, according to AlixPartners. A shortfall of 7.7 million vehicles worldwide is forecasted. Only 74 million vehicles were produced in 2020. Components in short supply include microcontrollers and sensors.

Ford, General Motors, Nissan, Daimler, BMW, Renault, and Toyota have all announced production cuts due to shortages of semiconductors. Much of the shortage is for 200mm wafers. SEMI reports that 200mm fab capacity will increase by 950,00 wafers (17 percent) from 2020 through 2024 to reach a record high of 6.6 million wafers per month [15].

Renesas Electronics, NXP Semiconductor, and Infineon are trying to increase output. The Renesas 200mm fab in Kyushu and the 300mm Naka fab are operating at full capacity. For every 40nm node microcontroller at the Naka fab, six are ordered from TSMC. The ratio has not changed with the shortage. Foundries are trying to help increase production on these older nodes for customers [16]. All sectors of the automotive supply chain have been impacted. Operations of Continental AG, and Magna have been impacted by the chip shortage. ABB expects shortages to impact industrial robot production. There is no consensus on when the shortage will end.

2 OSAT Financial Analysis

This section provides a financial analysis of the outsourced semiconductor assembly and test (OSAT) service provider market. The cumulative revenues of the top 20 OSATs (based on year end 2020 ranking) reached $9.19 billion in Q2 2021 using quarterly average fluctuating currency to convert to U.S. dollars. This represents a 27.5 percent increase over Q2 2020.

The role of an OSAT remains critical to the electronics industry supply chain. These companies are involved in substrate design, material selection, package selection and design, assembly, and test. Some companies have also incorporated traditional electronic manufacturing services (EMS) and even substrate manufacturing.

To identify the market size within this sector, it is critical to establish a clear definition of the services included. TechSearch International defines an OSAT as a company that provides chip package assembly with wire bonding, flip chip, or direct bonding, wafer thinning, bumping, and wafer and package test. Companies that offer chip-on-flex assembly for individually packaged devices such as driver ICs are counted as OSATs. Revenues from EMS, including board-level assembly or substrate manufacturing, are not included. Also not included are the assembly and test performed by foundries or IDMs when providing a full-service solution. Only companies that perform outsourced packaging and test of ICs they do not produce meet the definition of an OSAT. These excluded areas, however, are considered as part of the total available semiconductor packaging and assembly market when assessing opportunities for growth.

2.1 Industry Overview

Second-quarter results for electronic goods appear to provide mixed messages. IDC trackers indicate that shipments in Q2 2021 for PCs, servers, smartphones, and wearables continued to outpace shipments during the same period in 2020.

IDC reported that unit volume shipments of PCs grew 13.2 percent year-over-year but were flat quarter-to-quarter. Supply chain constraints and logistical challenges continue to plague the segment. However, demand remains strong and 14.2 percent unit growth is projected for 2021.

The server market is also feeling issues in the supply chain. During Q2, volume shipments grew more than 10 percent over Q1, but were less than one percent more than Q2 2020.

The smartphone sector continues the move to 5G. IDC reported a 13.2 percent increase in volume shipments in Q2 2021 over Q2 2020. Despite the challenges faced in 2020, major brands continued with production plans, pushing out delivery schedules rather than cutting orders. Therefore the supply chain became better

positioned to answer industry needs in 2021. IDC projects about a 7 percent growth in unit volume over 2020.

As consumers began increase outdoor activities, a renewed focus on health tracking occured. The wearables market surged in Q2 with a 32 percent increase in shipments year-over-year and over 9 percent quarter-to-quarter. Demand for hearables (such as earbuds) and watches led the growth spurt.

The semiconductor industry experienced 29.2 percent growth in revenues year-over-year in Q2 2021 according to data published by World Semiconductor Trade Statistics (WSTS). Worldwide sales grew 8.5 percent quarter-to-quarter with capacity fully booked at the key fabs. Investment in additional capabilities and capacity is planned in the United States, Europe, China, and Taiwan, among others.

2.2 OSAT Market Performance

Strong demand for OSAT services propelled the market value in this sector to a new high. During Q2 2021, the cumulative revenue for the top 20 companies increased 8.7 percent quarter-to-quarter and 27.5 percent year-over-year (see Table 2.1).

Table 2.1. Top 20 OSATs 2021 Quarterly Revenue ($ in millions)

Rank	Company	Headquarters	Q1 2021	Q2 2021	Q-to-Q
1	ASE Technology Holdings	Taiwan	$2,499.4	$2,710.2	8.4%
2	Amkor Technology	U.S.	$1.326.2	$1,407.0	6.1%
3	JCET Group	China	$1,035.9	$1,100.2	6.2%
4	Powertech Technology	Taiwan	$656.5	$737.0	12.3%
5	Tongfu Microelectronics	China	$504.3	$591.6	17.3%
6	Tianshui Huatian Technology	China	$400.8	$464.9	16.0%
7	KYEC	Taiwan	$271.8	271.5	-0.1%
8	UTAC	Singapore	$273.7	$323.9	18.3%
9	ChipMOS	Taiwan	$230.3	$249.6	8.4%
10	Chipbond	Taiwan	$228.7	$249.2	9.0%
11	SFA Semicon	Korea	$125.5	$136.1	8.4%
12	Sigurd (includes Winstek)	Taiwan	$124.8	$150.3	20.4%
13	Carsem	Malaysia	$129.6	$130.2	0.5%
14	AOI	Japan	$99.2	$98.0	-1.2%
15	LB Semicon	Korea	$102.3	$108.4	6.0%
16	FATC	Taiwan	$90.3	$88.2	-2.3%
17	Ardentec	Taiwan	$93.4	$102.7	10.0%
18	Unisem	Malaysia	$92.0	$97.5	6.0%
19	Tong Hsing + Kingpak	Taiwan	$85.6	$90.8	6.1%
20	Nepes	Korea	$85.4	$84.0	-1.6%
Total Revenue			$8,455.7	$9,191.3	8.7%

Source: TechSearch International, Inc.

Every company reported year-over-year growth in Q2. During the first half of 2021, the top 20 companies registered a very wide range of sales growth from a low of 1.6 percent to a high of 65.1 percent.

Table 2.2 reflects revenue growth for the top 20 companies for the first half of 2021 as compared to the first half of 2020.

Table 2.2. Top 20 OSATs First Half 2021 ($ in millions)

Rank	Company	Headquarters	1H 2020	1H 2021	Percent Growth
1	ASE Technology Holdings	Taiwan	$4,319.8	$5,209.6	20.6%
2	Amkor Technology	U.S.	$2,325.5	$2,733.2	17.5%
3	JCET Group	China	$1,702.2	$2,136.0	25.5%
4	Powertech Technology	Taiwan	$1,275.0	$1,393.5	9.3%
5	Tongfu Microelectronics	China	$663.7	$1,095.9	65.1%
6	Tianshui Huatian Technology	China	$527.8	$865.8	64.0%
7	KYEC	Taiwan	$489.1	$543.4	11.1%
8	UTAC	Singapore	$341.1	$597.6	75.2%
9	ChipMOS	Taiwan	$367.4	$479.9	30.6%
10	Chipbond	Taiwan	$344.9	$477.8	38.5%
11	SFA Semicon	Korea	$246.6	$261.6	6.1%
12	Sigurd (includes Winstek)	Taiwan	$187.4	$275.1	46.8%
13	Carsem	Malaysia	$183.9	$259.8	41.3%
14	AOI	Japan	$194.0	$197.2	1.6%
15	LB Semicon	Korea	$170.0	$210.7	23.9%
16	FATC	Taiwan	$165.5	$178.4	7.8%
17	Ardentec	Taiwan	$145.3	$196.1	35.0%
18	Unisem	Malaysia	$137.2	$189.5	38.1%
19	Tong Hsing + Kingpak	Taiwan	$133.4	$176.4	32.2%
20	Nepes	Korea	$144.4	$169.5	17.4%
Total Revenue			$14,064.2	$17,647.0	25.5%

Source: TechSearch International, Inc.

COVID-19 cases in Taiwan increased in Q2. While the country weathered the virus storm well during the first year of the pandemic, foreign workers employed by a few of the larger firms appear to have been the source of some cluster outbreaks at some of those companies. At this writing, the situation is reported to be under control; but it is another reminder of how quickly things can change when dealing with this virus.

Demand has continued to be strong for advanced packaging solutions, such as those needed for high-performance computing (HPC), but build-up film substrate supply is a limiting factor. The sector under the greatest strain continues to be wire-bond. Demand for test services has also started to rise. Orders for wafer probing have been extended to secondary suppliers, as the primary partners have been unable to

meet the demand. Most companies are reporting extremely high factory utilization. These issues, along with increases in cost for materials and components, have resulted in price increases as the OSATs pass along cost and enjoy premiums for capacity reservation.

The extremely high loading at the first-tier OSATs is presenting opportunities for second-tier companies. During the first half of 2021, the top 10 OSATs registered a cumulative growth of 25.7 percent over the prior year. Not far behind, the second-tier companies saw their revenues increase in the first half by 23.8 percent over the prior year. While not every company experienced double-digit growth, all had positive gains. Demand, whether to restock inventory or for new product, is clearly real and positive for the entire OSAT market. Sales growth will remain strong across the top 20 as even the second-tier companies are reported to be cancelling volume discounts for the remainder of the year.

2.3 Company Highlights

This section presents the highlights of the top 10 OSATs. The three domestic China companies, JCET Group, Tongfu Microelectronics (TFME), and Tianshui Huatian Technology (Huatian) all recorded strong growth quarter-to-quarter and astounding growth year-over-year.

2.3.1 ASE Holdings

ASE Technology Holding Co. (ASEH) reported that sales of its semiconductor assembly and test business in Q2 beat expectations, growing 8.4 percent quarter-to-quarter and 22.1 percent year-over-year. Sales have increased for six consecutive quarters. Quarter-to-quarter, the company's published sales were up uniformly in the communications, computing, and automotive/consumer sectors.

However, comparing data from the first half of 2021 to the first half of 2020 provides a slightly different view. During the first half of 2021, assembly and test revenue increased 20.6 percent. Growth from the automotive/consumer sector as tracked by ASEH grew 37.8 percent, reaching almost $1.9 billion. The total sales from the communications sector reached $2.6 billion, an 11.7 percent increase for first half of 2021 over the first half of 2020. The computing sector was the smallest contributor at $0.73 billion in the first half of 2021, with growth of 16.5 percent over the first half of 2020.

ASEH provided further insight regarding the impact that the U.S. Bureau of Industry and Security's Export Administration Regulation (EAR) had on its business. If EAR-affected revenue is excluded, the year-over-year growth for first half of 2021 was 48 percent. The true impact of the regulation was most dramatic in the test sector. Recovering ahead of schedule, the company stated that this sector's revenue growth was 54 percent year-over-year if the EAR business is excluded.

Roughly 85 percent of the company's revenue is generated in assembly operations. Advanced products such as system-in-package (SiP), flip chip, bumping, and wafer-level packages represent about a third of the total. While 5G, AI, and new solutions for the automotive sector require advanced packaging solutions, the demand for wire bond packages continues to be the major revenue driver. Wire bond grew to 42 percent of sales in Q2 with both volume and prices increasing. Wire bonding is currently running at maximum utilization. The company plans to add 3,500 to 4,000 wire-bonders in 2021. In Q2, the company added 1,482 machines, bringing its total to 2,595 in the first half of 2021.

In addition to the wire bond sector, all other assembly and test operations are currently running at high utilization rates. ASEH reported that long-term contracts are viewed as a requirement by both customers and the company. A number of customers are extending long-term service agreements into 2023. In addition, the tight supply of wafers, components, materials, and substrates, along with fully loaded manufacturing lines will continue to drive price increases. One advantage the company has is its ability to manufacture substrates internally, providing between 42 and 45 percent of demand internally.

ASEH believes that the industry will not reach a balanced state of supply and demand until 2023. It believes the global pandemic has increased demand on existing systems and current technology. The rapidly growing areas such as 5G, IoT, next generation automobiles, will use advanced packaging including heterogeneous integration and chiplets, that require advanced manufacturing techniques, innovation, and new infrastructure. For this reason, ASEH believes capacity increases at the semiconductor fabs and the OSATs are necessary to expand the overall infrastructure to handle both short and longer-term needs. It does not believe that will drive an oversupply although some sector balancing may be required. While there may be some localized and time-dependent double-booking and inventory build, it is not viewed as an impact to ASEH's business. A continued focus on efficiency and technology, and demonstrated leadership, place the company in a strong position to manage the next phases in the industry. The company is projecting revenue and gross margin expansion during the next two quarters, which will result in sales growth of 20 percent in 2021.

2.3.2 Amkor Technology

Amkor saw the momentum from Q1 carry into Q2, recording better-than-expected results of $1.4 billion in sales, the highest quarter in its history. This represents a six percent increase quarter-to-quarter and 20 percent year-over-year. The first half of 2021 results were 17.5 percent higher than first half 2020 levels.

The company reported sequential quarterly growth across all market segments. Shipments of 5G-enabled smartphones, many of which utilized the company's RF solutions, drove a six percent sequential quarterly revenue increase. Solutions for the consumer space, including those for gaming, displays, video devices, and IoT wearables, that utilize Amkor's SiP solution, drove sales up nine percent quarter-to-quarter. Despite continuing supply chain constraints for wafers and substrates,

sales to the automotive and industrial sector increased four percent sequentially, with the company's fan-out wafer level package in demand for radar sensors. Shipments for high power and for electronic vehicles also grew. The company's investment in both capacity and technology for AI and HPC are paying off as sales increased six percent sequentially in the computing sector.

Advanced product offerings such as SiP, flip chip, WLP, and bumping continue to generate 70 percent of the company's revenue, increasing 17 percent in the first half over the same period the prior year. SiP solutions increased by double digits sequentially. Factory utilization continues to be very high. Assembly operations contributed 85 percent of revenue and 15 percent came from test. Test revenue increased 12 percent year-over-year in Q2 and 13.7 percent in the first half of 2021 over the first half of 2020, driven by increased offerings in 5G and system-level solutions.

Amkor has expanded cleanroom space and capacity for advanced packaging to accommodate demand. It announced that efforts are underway to identify potential locations for a U.S. factory, aligning the company with the country's investment in semiconductor fabrication. Total CAPEX target has increased to $775 million to support that effort.

Amkor believes the capacity investments already made and the contracts in hand positions it well for the remainder of 2021. It is expecting to see an increase between 17 and 24 percent in Q3 sales, largely driven by 5G in smart phones, IoT wearables, driver assistance systems, and power solutions for automotive and HPC. This growth will occur despite continued impacts from wafers and substrate shortages. It continues to project that its sales for 2021 will outpace the semiconductor market projections.

2.3.3 Powertech Technology

Powertech Technology (PTI) achieved a new quarterly revenue high in Q2 2021, reaching $737 million: a 12.3 percent increase quarter-to-quarter and 9.3 percent increase in the first half of 2021 year-over-year. The company reported strong demand for DRAM and Flash memory and good recovery for SSD. The strong performance was achieved despite cluster breakouts of COVID-19 within the company.

The company's focus on expanding its backend services for logic devices has resulted in strong gains. Greatek, a PTI subsidiary, saw revenues grow 34 percent year-over-year, resulting in tight capacity. PTI experienced over 100 percent revenue growth as new products ramped. PTI also exceeded its target of 50 percent WLP capacity for logic products. Although the company is experiencing rising costs and shortages of packaging materials, it has no plans to raise prices during the second half of the year.

Wire-bonding lines continue to run at full capacity. Bumping capacity has been expanded to 95,000 pieces per month. The company announced it has increased its

CAPEX target to $606 billion. It plans to increase bumping capacity to 105,000 pieces per month. A new factory is scheduled for completion in June 2022 at Greatek's manufacturing site in Toufen, Taiwan, which will add another 800 sets of wire-bonding equipment. Test capacity will also be expanded at the factory in Chunan, adding 230 testers.

2.3.4 JCET Group

Number-three-ranked JCET reported a revenue increase of 6.2 percent quarter-to-quarter and 24.4 percent year-over-year. The company cited its continuous investment in advanced technology as the foundation for its growth. JCET noted completion of its acquisition of Analog Devices Inc.'s Singapore facility. Second quarter sales included revenues generated from the new asset. To strengthen customer support and further its market penetration, the company established a Design Service Business Center and an Automotive Electronics Business Center.

2.3.5 Tongfu Microelectronics

Tongfu Microelectronics (TFME) saw quarter-to-quarter sales increase 17.3 percent. This represents a new high mark. TFME realized a 67.4 percent growth year-over-year in Q2. As a major supplier to AMD, a significant portion of TFME's revenue can be linked to the 99 percent increase in sales year-over-year recorded by its customer.

2.3.6 Huatian

Tianshui Huatian Technology (Huatian) reported a quarter-to-quarter sales increase of 16 percent. Huatian realized 62.3 percent growth year-over-year in Q2.

2.3.7 KYEC

Test specialist KYEC's revenues remained essentially flat in Q2 with modest growth of six percent year-over-year, resulting in 11.1 percent growth in the first half of 2021 over the prior year. Like PTI, KYEC was forced to run at reduced capacity in June due to COVID-19 infections. During that month, production was down by 30 to 35 percent.

The company generated just over 79 percent of its sales in test services during Q2. The strongest increase in total sales came from the communication sector, while other segments remained flat. KYEC expects to strengthen revenue from the automotive sector with orders into 2022.

2.3.8 ChipMOS and Chipbond

Display driver IC and memory backend specialist ChipMOS saw sales increase 8.4 percent fom Q1 to Q2 and 37.4 percent year-over-year. Overall factory utilization was 87 percent, with assembly operations running at 94 percent. The company reported increasing revenues in memory, specifically DRAM, mixed signal, and DDIC. The memory sector accounted for about 43 percent of the company's first half revenue, and display driver assembly was 29 percent.

Sales from assembly operations increased 6.8 percent quarter-to-quarter and represent about 78 percent of the total. Demand for test services ticked up one percentage point.

ChipMOS sees end markets continuing to recover which is generating higher demand. It is also monitoring fluctuations in wafer supply. Long-term contracts with key customers were reported. The company plans to increase its 2021 capital investment to 20 to 25 percent of revenue to add capacity strategically.

Chipbond saw a quarter-to-quarter increase in sales of nine percent in Q2 and a year-over-year increase of 48.5 percent. First half revenues were 38.5 percent higher than the prior year. The company has increased its market presence as a supplier for 5G power and benefitted from increasing demand for high-end test support for 5G TDDI ICs and OLED DDI. Revenue for non-display driver assembly/test services is projected to increase as much as 30 percent during the year.

In September, the company announced the establishment of a long-term strategic partnership with United Microelectronics (UMC). The two companies will cooperate closely in the field of driver ICs, integrate front-end and back-end process technologies, and develop driver IC solutions of higher frequency and lower power consumption. UMC's offerings for high-efficiency power and 5G RF components mesh well with Chipbond's capabilities in packaging and test for both products.

Both ChipMOS and Chipbond are benefiting from robust demand for DDIC chips found in handsets, TVs, and automotive applications. Where fabricated wafers were typically delivered in one to two days, the companies now receive chips for assembly only weekly. Price increases are again expected during the second half of 2021 for DDIC and NOR flash devices.

2.3.9 UTAC

Although UTAC is no longer a publicly traded company, TechSearch International has continued to track and include it in the top 10 ranking to ensure visibility to a significant portion of revenue. The company saw Q2 sales increase 18.3 percent quarter-to-quarter and 84.8 percent year-on-year. The year-over-year performance can be attributed in part to the company's purchase of PTI's wafer bumping assets in Singapore, which closed in January 2021.

2.4 OSAT Performance Metrics

TechSearch International continues to track several key metrics such as gross margin, R&D spending, and CAPEX for the top 10 OSATs.

2.4.1 Gross Margin

Nine of the top 10 OSATs reported higher gross margins in the first half of 2021. Table 2.3 compares gross margin for the top 10 companies from the first half of 2020 to the first half of 2021. KYEC was the only company that did not show gross margin improvement, due largely to running at reduced capacity in Q2 because of COVID-19 outbreaks.

Table 2.3. Gross Margin for Top 10 OSAT Companies

Company	1H 2020	1H 2021
ASEH (ASE+SPIL)	20.9%	25.0%
Amkor	16.4%	19.7%
JCET Group	14.5%	17.1%
PTI	19.6%	22.3%
TFME	15.2%	18.5%
Huatian	21.6%	24.5%
KYEC	29.9%	27.9%
UTAC	17.0%	18.0%
ChipMOS	21.7%	26.2%
Chipbond	26.4%	31.1%

Source: TechSearch International, Inc.

Within the dynamics of the supply chain, OSATs have seen orders surge, lead times extend, capacity pushed to the limit, and materials costs increase. While the cost increases negatively impact gross margin, the high utilization rates and price increases drove profit up almost universally.

Despite the groundswell of orders utilizing wire bond, concurrent demand for more advanced packaging solutions also contributes to margin improvement.

2.4.2 R&D Spending

Early in 2020, OSAT companies were cautiously investing in technology that would continue to deliver leading-edge technology and improve efficiency. Late in that

year, the tide began to turn. Spending for research and development by the top 10 is summarized in Table 2.4.

Table 2.4. OSAT R&D Spending ($ in millions)

Company	1H2020	1H2021
ASEH	$247.7	$268.6
Amkor	$63.8	$87.8
JCET Group	$69.8	$84.8
PTI	$38.1	$42.5
TFME	$48.2	$80.1
Huatian	$28.4	$46.3
KYEC	$18.2	$20.4
UTAC	$18.4	$21.5
ChipMOS	$17.0	$19.8
Chipbond	$8.2	$10.9
Total	$557.8	$682.7

Source: TechSearch International, Inc.

A total of $682.7 million was directed toward R&D activities in the first half of 2021. This investment represents a 22 percent increase over the first half of 2020. Of the top 10, half have chosen to increase their spending as a percentage of revenue and the other half have tempered that metric. The latter is likely due to the uncharacteristic revenue growth driven largely by the supply constraint and favorable pricing environment.

2.4.3 CAPEX

The current environment has driven capital investments to an unprecedented level across the top 10 companies.

Table 2.5 shows CAPEX spending for the top 10 OSATs in the first half of 2021.

Table 2.5. CAPEX for Top 10 OSATs ($ in millions)

Company	1H2020	1H2021
ASEH	$813.0	$1,021.0
Amkor	$134.3	$273.6
JCET Group	$190.0	$254.8
PTI	$363.6	$226.5
TFME	$249.9	$416.6
Huatian	$182.3	$368.1
KYEC	$178.7	$309.7
UTAC	$48.0	$125.6
ChipMOS	$73.3	$109.8
Chipbond	$40.9	$100.1
Total	$2,274.0	$3,205.8

Source: TechSearch International, Inc.

Slightly more than $3.2 billion was invested in the first half of 2021, a 41 percent increase over the prior year. Orders for wire bonding equipment have skyrocketed, with most of the OSATs showing significant capacity ramps. Expansion of test capacity is also underway. Finally, the migration to advanced solutions is triggering some investments in wafer bumping. The challenge for the OSATs will be to right-size their operations so as to not end up with significant idle capacity when the industry returns to a more balanced state.

2.4.4 Test Services

Demand for test services continues to increase, and an increasing portion of OSAT revenues is derived from test services. This revenue is derived from both wafer test and final package test. TechSearch International provides a revenue breakout wafer and final package test for the top five OSATs (see Table 2.6). Wafer probe represents approximately 23 percent of the market. Growth in test revenue is expected to continue as complexity increases and OSATs expand test capacity. Test capacity will remain tight.

Table 2.6. 2020 Test Revenue Split Top 5 OSATs ($ in millions)

Test Revenue	Wafer Probe	Final Package
$3,833	$843	$2,990

Source: TechSearch International, Inc.

2.5 Outlook

In August, WSTS revised its projection upward, saying that the worldwide semiconductor market was on track to grow 25.1 percent year-over-year in 2021. IC Insights projected a growth of 24 percent for the year.

Most OSATs continue to project a year of unprecedented growth. The top players have clear order visibility for the balance of 2021 and contracts that extend into 2022. Factories are fully utilized, prices are up, lead times are up, and capital investment is growing.

Demand continues to grow for memory and logic devices, DDICs, sensors, power amplifiers, 5G solutions, and RF across multiple market segments. IC fabs are investing in new capacity, but more important for the near term, they are working to alleviate shortages in the automotive sector.

With only a few months left in the year and barring a major turn of events on the political or health stage, TechSearch International, Inc. sees further growth clearly ahead for the OSATs. With price increases still on the table, growth of 24 to 30 percent is feasible for the market. It will be important to follow the power shortage in China, which could reduce output and revenue for OSATs with some of the highest growth rates.

While the industry has seen phenomenal growth, it is highly improbable that such growth will continue in subsequent years. At some point supply and demand will stabilize. At what volume levels will this occur? If there is double booking, how many units will be needed to match end-market demand? Prices (and price premiums) reflect capacity reservation, extremely high loading, and short lead times, raising the question: what adjustments will occur?

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3 Next Generation Packaging

TSMC produces 92 percent of the global advanced silicon, and Samsung accounts for the remaining 8 percent [17]. TSMC's 3nm silicon node is moving into production next year. Samsung's gate-all-around (GAA) technology will see the first designs in the first half of 2022, and second-generation 3nm technology is scheduled for 2023. At the Samsung Foundry Forum on October 6, Samsung announced plans to develop a 2nm GAA transistor to be completed by 2025. Samsung continues its strong partnership with IBM for advanced silicon development. Samsung, TSMC, and IBM continue to develop advanced packaging solutions to meet the needs of advanced silicon nodes. Intel's new management is focused on improving its advanced silicon production capability. Intel's version of 3nm is scheduled for 2024 at its new Arizona wafer fabs. Intel continues to develop its advanced packaging capability.

As silicon nodes have advanced, package types have migrated from leadframe to area array to WLP, silicon interposer, and 3D. Samsung showed this progression along with the key package requirements at the Samsung Foundry Forum (see Table 3.1). Samsung indicated that 50 years after the creation of the integrated circuit, new requirements such as timing, power, and mechanical integrity are increasingly important due to the added complexity of advanced silicon technologies.

Table 3.1. Silicon Nodes Package Trends

Si Node	10-1 μm	Submicron	Deep Submicron	Nano	FinFET (14-4nm)	GAA (< 3nm)
Timeframe	1970s-80s	1990s	2000	2010	2020 - 2025	
Package	DIP / QFP	PGA / BGA	CSP / SIP	POP	WLP / 2.5D /3D	
						EMI
						Mechanical
					Thermal	Thermal
					Reliability	Reliability
			Power		Power	Power
		Timing	Timing		Timing	Timing
	Function	Function	Function		Function	Function

Source: Samsung.

As the industry moves to next-generation packages for 3nm silicon nodes and beyond, new design, test, and packaging requirements are emerging. The main challenge at the 3nm node is manufacturing cost, including mask and fabrication. With the higher cost and yield challenges at these advanced nodes, more chiplet designs are anticipated. A variety of different packages will be used including

silicon interposers, laminate substrates with embedded bridges, high-density fan-out (HD FO), and redistribution layer (RDL) substrates.

3.1 High-Performance Solutions

With the introduction of the 3nm silicon node, the cost to design and fabricate a monolithic design increases. Companies are expected to move to chiplet designs to lower cost with improved yield for smaller size die. AMD reported this as one of the main drivers for its chiplet design. Another driver for the adoption of a chiplet design for high-performance applications is to improve memory latency [18]. According to AMD, higher core counts and performance are possible with chiplet design than with a monolithic design. Lower costs at all core count/performance points for a variety of product lines are possible. Cost scales down with performance by depopulating chiplets. For example, using 14nm technology for the I/O die, instead of fabricating it on a more advanced silicon node, reduces fixed cost. A 32-core die would require an area of 777 mm^2. Splitting out I/O, which is 44 percent of the area, and the CPU core, which is 56 percent of the area, allows these two functions to be fabricated as smaller die. The compute functions scale more than I/O, therefore it would be fabricated in the most advanced node and the I/O function could be fabricated in a trailing node. AMD also indicates that with a chiplet design half the power consumption for the same power performance is possible in some cases. The greatest benefit of chiplets will be for silicon nodes at 7nm and below [19].

3.1.1 Challenges for Chiplets

There are a number of challenges to the use of chiplets. AMD indicates that a chiplet design requires more engineering work upfront to partition the SoC in the correct number and chiplets function blocks [20]. Not all combinations will work for a specific application. Inter-chiplet communication is required. Compared to on-chip metal, these interconnects may have longer routes with higher impedance, lower bandwidth and higher power consumption and/or higher latency. Interconnect overhead may include circuits for crossing voltage and timing domains, protocol conversions, and/or SerDes. The combination of all these circuits can contribute to additional power and silicon area overheads that would not be found in a monolithic design. Additional chip functions include test and debug interfaces, clock generation and distribution, power management, on-chip temperature sensors, and I/O. Even though the total amount of silicon area increases for chiplet designs, it may still cost less than a monolithic design at the most advanced nodes.

3.1.1.1 Test Challenges

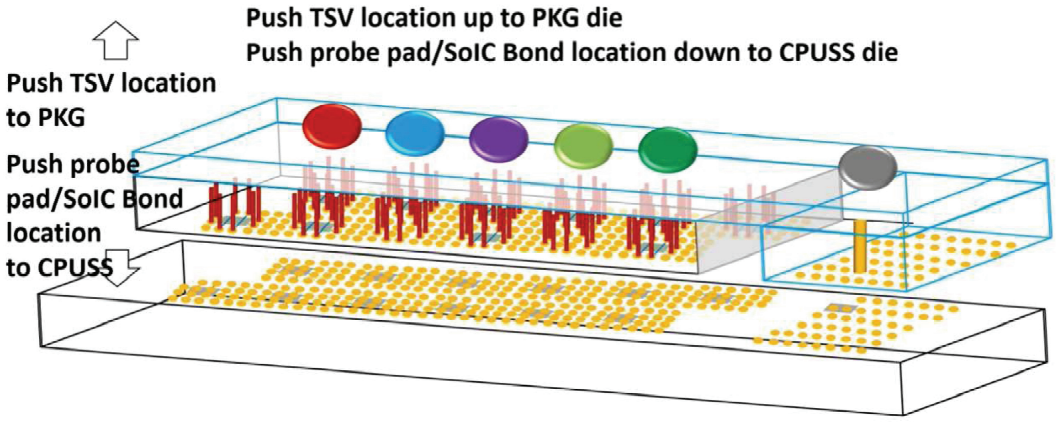
AMD indicates that rework is not possible on integrated chiplet packages. A defect in the package means that the entire package and all the chiplets must be discarded. Wafer sort test is imperative in the delivery of known good die (KGD) and requirements include:

- State-of-the-art fault models for automatic test pattern generation
- Mission-mode testing at wafer sort
- Careful selection of test points, board bands, die matching
- Redundancy/repair strategy for features not tested at sort
- Test access features for in-package testing to ensure quality

Full probe at wafer sort is needed, but even microbump probing is a challenge for high volume manufacturing. Probing dense Cu pillars is not feasible today and companies are opting for sacrificial probe pads. Mechanical engineering challenges include temporary, reliable contacts at very fine pitch. Electrical engineering challenges include better interfaces for tester access (including power delivery), self-testing functional interfaces that do not need probing, and redundancy/repair options [21].

Test becomes increasingly important for 3D chiplets with hybrid bonding. It may no longer be possible to probe the pads prior to bonding. Because direct probing on some areas of the chiplet may not be possible, test probe areas are suggested. TSMC shows some of the test probe design for its SoIC (see Figure 3.1). In determining the probe pad locations, TSMC suggests it is necessary to determine the I/O location, map the location to the probe pad, place a dummy SoIC bond, swap the dummy SoIC bond to the active SoIC bond, and assign a net based on the nearest probe pad. Then a TSV can be placed on the active SoIC bond. The TSV location goes up to the package die and it is necessary to push the probe pad/SoIC bond location down to the CPU die [22].

Figure 3.1. Determine probe pad locations for SoIC.



Source: TSMC.

3.1.1.2 Assembly Challenges for Hybrid Bonding

Assembly challenges for die-to-wafer (D2W) bonding have been described. Equipment selection is an important consideration for the process. Cu terminal

metallurgy on the front and backside of the chips is typically used. Specific front side topology is required to ensure good Cu-to-Cu contact. A good chemical mechanical polishing (CMP) process is important.

Samsung indicates that the challenges with die-to-wafer hybrid bonding include:

- Cu pad surface control
- Particle-free process to avoid contamination that causes voids
- Bonding temperature
- Metrology/inspection
- Integrated bonding/assembly system

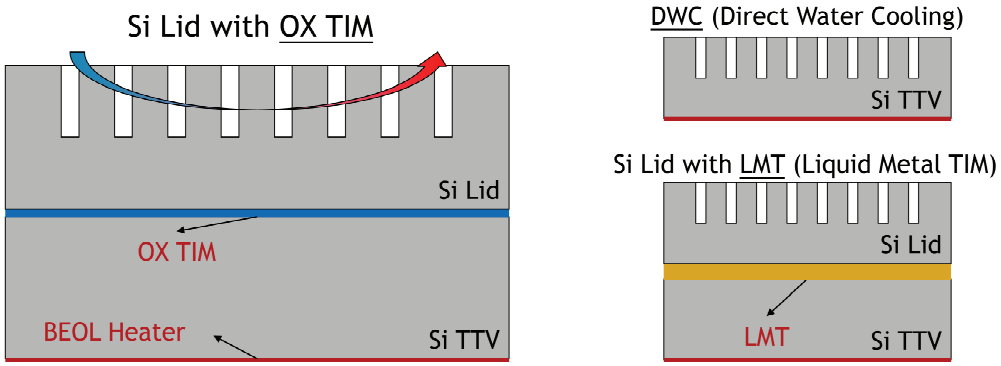
3.1.1.3 Thermal Challenges

AMD indicates that thermal requirements are also greater with chiplets, especially for 3D. Stacking increases power density. There is a need to create interleave cool and hot components when going vertical. BEOL dielectrics act as thermal insulators, reducing cooling efficiency with stack height. Power management must become more sophisticated and new approaches for heat extraction are needed.

Several companies are using Indium as the thermal interface material (TIM), especially for large die. Metal TIM is not the only option.

TSMC announced the development of an integrated Si Micro-Cooler (ISMC). A Cu lid is replaced with a silicon lid with preformed microstructures to allow liquid coolant to get closer to the heat source. The metal TIM is replaced with a thin SiOx bonding interface (OX TIM) formed by fusion bonding between the silicon lid and silicon chip (see Figure 3.2). It has a low interface thermal resistance, even though the dielectric constant of the SiOx is at a low single digit W/m•K. Direct wafer cooling removes heat from the back of the SoIC [23].

Figure 3.2. Silicon lid with SiOx bonding interface.



Source: TSMC.

3.1.2 Silicon Interposers

TSMC has been in production with silicon interposers for 10 years and the next node products are expected to continue to use this technology. Xilinx uses a 2X reticle silicon interposer for its FPGA slices. With as many as 20,000 connections between each slide, the high-density of a silicon interposer is required. The largest silicon interposer in production is 1,700 mm^2 (~2X reticle size) for a 7nm silicon node die with six HBMs. TSMC has demonstrated a 4X reticle size supporting chiplets and 12 HBMs.

Marvell plans to introduce its new data infrastructure product using TSMC's 3nm silicon node process that will be packaged using advanced die-to-die interface IP and TSMC's CoWoS package. Marvell's new 3nm multichip platform includes advanced die-to-die interfaces. The first is a flexible extra short reach (XSR) interface for connecting multiple die on a package substrate for applications such as co-packaged optics (CPO) for cloud data centers. Marvell is also developing an ultra-low power and low-latency parallel die-to-die interface with the highest industry bandwidth. The new parallel interface is compatible with emerging Open Compute Project (OCP) standards and enables high-performance chiplet solutions by connecting multiple silicon devices on an interposer. Both interfaces are also available on 5nm to enable multi-node solutions.

Samsung is in production with silicon interposers for AI (training/inference) and network switch applications, and sees the technology extending to advanced silicon nodes with its I-Cube family (see Table 3.2). The trend is toward larger interposers to support more HBMs, and larger package sizes.

Table 3.2. Silicon Interposer in Mass Production for AI

	1 HBM	2 HBMs	2 HBMs	4 HBMs	8 HBMs
Package size (mm^2)	1,806	2,500	3,300	4,600	7,225
Interposer size (mm^2)	535	850	1200	1500	>2,800
ASIC size (mm^2)	270	500	800	600 (300 mm^2 x 2)	1,600 (800 mm^2 x 2)
Fab node	14nm	14nm	7nm	4nm	NA
Application	Network	HPC AI	GPU	HPC AI	-

Source: Samsung.

3.1.3 High-Density Fan-Out

Several companies are investigating HD FO on substrate for next generation chiplet solutions. The main driver is lower cost.

Insertion loss is mentioned as a consideration for the adoption of HD FO because the oxy nitride may not provide as good a performance at high-speed as RDL using a polyimide in the FO solution. However, Xilinx indicates that even if TSV insertion loss contributes 0.3 to 0.5dB loss, since the entire link from transmit to receive has 30dB budget, it is not an issue. While organic materials are better for loss, there are other disadvantages from signal integrity considerations. Some argue that silicon interposer could push higher data rates such as 8-10 Gbps.

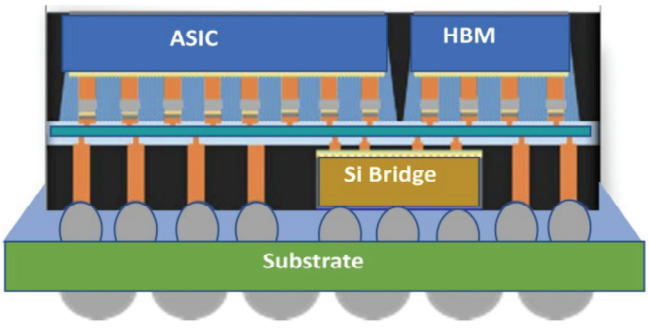
HD FO solutions are increasingly moving into production for networking ASIC, GPUs, and server CPU applications. HD FO solutions are also being considered for client CPUs in the future.

Amkor expects its HD FO, Substrate-SWIFT®, to be in production by Q2 2022 for the first application. Additional applications are expected to follow in 2023. This is a chip last solution. A typical product will have a 38mm x 46mm FO area, and a 52mm x 54mm FO area will be the largest in development. Up to four RDLs are qualified and six layers will be qualified by the end of the year. Amkor offers a silicon bridge solution.

ASE offers chip-first and chip-last solutions for its FOCoS. The largest in production is a 67mm x 67mm package with a 32mm x 26mm FO area. It is a chip-last solution. This is for a network application with an ASIC fabricated on 14nm silicon node.

A silicon bridge FO version is expected to move into production in the next year or so. The sFOCoS test vehicle is a 40mm x 30mm package with a 27mm x 14mm fan-out area. A 6mm x 6mm silicon bridge is used to connect the ASIC and the HBM (see Figure 3.3). The bridge is chip first and the ASIC and HBM are chip last. The use of the bridge can reduce the number of layers in the RDL [24].

Figure 3.3. ASE sFOCoS test vehicle.



Source: ASE.

Deca has introduced a version of its M-Series™ fan-out technology targeted to chiplets. Work is underway on a fan-out chips-first embedded die structure that includes active die as well as a bridge die version to improve overall system performance. A recent customer design includes both (see Figure 3.4). Adaptive patterning is used.

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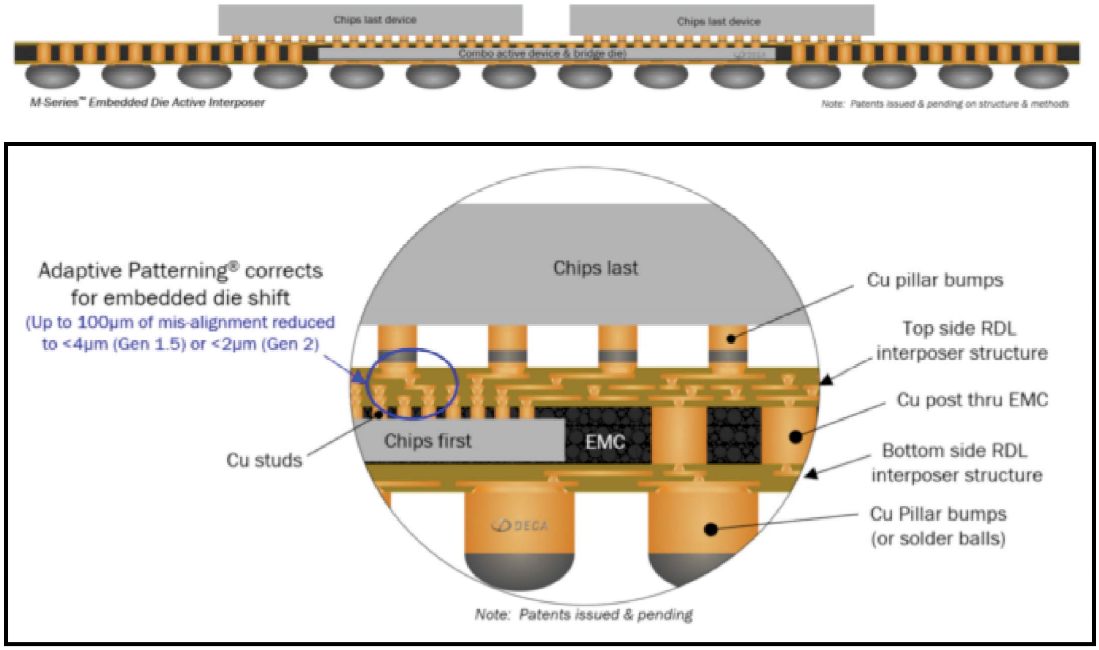
Figure 3.4. M-Series™ bridge interposer with embedded die.



Source: Deca.

Adaptive patterning is used to create perfect substrate I/O pads for multiple chip-last devices, including CPU, GPU, HBM, or other functionality independent of natural die shift of multiple bridge chips. Adaptive patterning corrects for shift of single or multiple bridge die. For example, mis-alignment up to 100 μm can be reduced to <4 μm in Gen 1.5 or <2 μm in Gen 2. Deca has a relationship with a wafer foundry where the silicon bridge chips can be fabricated.

Samsung has developed its R-CUBE as an alternative to a silicon interposer for chiplet applications. Up to four RDL layers have been demonstrated.

SPIL has developed a FO embedded bridge solution, FO EB that is moving into production. Features of 2μm line and space are offered and 1μm line and space is possible. The embedded bridge is chips first and using it for the highest density connections reduces the requirement for a dense 2μm L/S RDL pattern. Relaxing the RDL line and space design can improve yield. The logic and HBM are assembled using a chip last approach. Target applications include GPUs and CPUs.

SPIL demonstrated good advantages of a GPU plus HBM using the embedded bridge in the RDL. Results show better signal integrity than with a silicon interposer or EMIB. This results from the SI/PI transmission patch (see Table 3.3).

Table 3.3. SI/PI Path Transmission

HBM-GPU Module	Silicon Interposer Platform	EMIB Platform	FO-EB Platform
SI Path	HBM→Cu Via thru Si interposer→Cu length thru Si Interposer→Cu Via thru Si interposer→ GPU	HBM→Cu Via thru FCBGA→Cu length thru Si interposer→Cu Via thru FCBGA→GPU	HBM→Cu Via thru RDL interposer→Cu length thru Si interposer→Cu Via thru RDL interposer→GPU
PI Path	BGA→TSV→GPU/HBM→TSV→BGA	BGA→GPU/HBM→BGA	BGA→Thru EMC/RDL Via→GPU/HBM→Thru EMC/TDL Via→BGA

Source: SPIL.

JCET's FO is called XDFOI™. It is available in a chip-first or chip-last option. Target applications include consumer, automotive, computing, and communications. A chip-on-chip face-to-face version is also offered. It is targeted at AI, HPC, IoT, and medical applications. The 2D RDL version is in pilot production. A 2.5D version of XDFOI™ will be ready for production-level verification by Q3 2022. Full 3D versions will be ready by Q1 2023.

Tongfu Microelectronics is also developing a HD FO solution. The fan-out package on substrate (FOPoS) is a chip-first solution. It features 2μm lines and spaces and up to three RDLs.

TSMC is targeting AI, network system, and edge computing with its chip-first InFO_oS. TSMC has demonstrated a fan-out area of 51mm x 42mm on a 110mm x 110mm substrate. The test vehicles integrated two logic die and eight I/O die. There are five RDLs, with 2μm line and space and one with 5μm line and space. The die-to-die I/O pitch is 36 μm.

InFO_L has been introduced. The local silicon interconnect (L) or bridge allows connections between multiple die. It is a chip first approach. InFO_L would not be suitable for the addition of HBM.

TSMC has also developed a CoWoS®-R process that is a chip-last solution. Chiplets, HBM, and passives can be integrated on multiple RDLs connected to the substrate. A test vehicle with four RDLs with 2μm line and space has been demonstrated. The use of the RDL provides a stress buffer layer to protect the bumps on the chip. The RDL area is 53 mm x 34 mm, which is two times the reticle size. No stitching is required for the interposer with the RDL design and formation process [25].

TSMC has also introduced CoWoS_L as a chip-last solution. The silicon interposer is replaced with an organic substrate (RDL) with an embedded bridge to increase signal density. A 1.5X reticle with one logic die plus 4 HBM2e has been demonstrated. A 3X reticle with three logic die and 8 HBMs is planned.

3.1.4 High-Density FO and Si Interposer Forecast

A market forecast for high-density silicon interposers with TSVs and alternatives such as fan-out on substrate, calculated in 300mm wafers, is provided in Table 3.4. Because Intel uses EMIB instead of a silicon interposer, it is not counted in the analysis. The analysis includes FPGAs, CPUs, GPUs, and ASICs. The analysis allows for growth in interposer area over time. High-density is defined as ≤2μm line and space. High-density FO-WLP such as InFO used for application processors is not included in the forecast.

Table 3.4. Market Projections for Si Interposer and HD FO

	2020	2021	2022	2023	2024	2025	2026
Interposers/HD FO (millions of units)	9	11	15	21	35	43	50
Thousands of 300mm wafers	173	228	382	539	832	1,061	1,312

Source: TechSearch International, Inc.

3.1.5 Silicon Interposer Suppliers

Silicon interposers are used for high-performance applications such as AI accelerators and network switches. Silicon interposers with through silicon vias (TSVs) provide the highest routing density possible for a substrate and serve segments and applications that require >200 lines/mm for die-to-die connection. Silicon interposers have been in production for many years with ≤1μm line and space. Silicon interposers with TSVs are used to route high-density signals between logic devices or between logic and high bandwidth memory (HBM) stacks.

The major suppliers of silicon interposers are located in Asia (see Table 3.5). TSMC and UMC are located in Taiwan, and Samsung is located in South Korea. TSMC and Samsung only provide substrates for foundry customers. Fraunhofer in Germany offers pilot production of silicon interposers and is mainly focused on working with companies to develop a fabrication process. A few companies in Japan, including GINTIC, offer silicon interposers. GLOBALFOUNDRIES is located in Malta, New York and offers silicon interposers. Micross in Research Triangle, North Carolina, offers silicon interposers with TSV in small volumes. Skorpios Technologies (formerly Novati) is expanding its capacity in Austin, Texas. Skywater has purchased BRIDG in Kissimmee, Florida, and is expected to offer silicon interposers.

Table 3.5. Suppliers of Si Interposers

Company	Wafer Size	Status
Fraunhofer (Germany)	300 mm	Pilot line
GINTEC (Japan)	200 mm, 300 mm	Small volume
GLOBALFOUNDRIES (U.S.)	300 mm	Production
Micross (U.S.)	200 mm	Small volume
Samsung (S. Korea)	300 mm	Production for foundry customers
Skorpios Technologies (U.S.)	200 mm	Production
SkyWater (U.S.)	200mm	Future production
TSMC (Taiwan)	300 mm	Production for foundry customers
UMC (Taiwan)	300 mm	Production

Source: TechSearch International, Inc.

Though it provides a high-density interconnect, the silicon interposer requires the use of a laminate substrate to form the package.

3.1.6 High-Density Laminate

IBM and Intel are promoting laminate solutions for high-performance applications including AI and servers.

Intel uses its EMIB solution in which it fabricates the bridge chip, and the substrate supplier embeds it into the laminate build-up substrate. This allows the high density to be used only where needed. Intel's Sapphire Rapids is a full-reticle CPU that will be portioned into four chiplets. All four chiplets will access shared cache and are connected using the modular die fabric (MDF). Any core can talk to other cores on the four die and access the shared cache across all four quadrants, as well as access I/O across the four quadrants.

Intel's Ponte Vecchio is designed using the Co-EMIB process (see Table 3.6). Two GPUs (tiles using Foveros) will be connected to 8 HBMs. Up to 11 bridges will be used.

Table 3.6. Intel's Ponte Vecchio Features

Item	Feature
D2D Pitch	36 μm
Active Top Die Count Per Stack	16
Max Active Top Die Size	41 mm^2
Base Die Size	650 mm^2
EMIB Pitch	55 μm
Core Pitch (minimum)	100 μm
Memory (HBM)	8
Package Size	77.5 mm x 62.5 mm
EMIB Count	8

Source: Intel.

IBM has introduced a bridge solution in which the die are connected using a silicon bridge prior to assembly on a build-up laminate substrate. In today's version there is a trench in the substrate, but IBM is working on a new version with a thinner bridge that will not require the trench. This will require the bridge chip thickness to be reduced. IBM is also working on C4 standoff height optimization.

IBM is also focused on developing wafer-level FO organic solutions to achieve the high-density interconnect that is difficult to meet with laminate solutions. Large laminate solutions have reliability challenges and warpage issues. Power delivery and signal integrity are important considerations.

TSMC's System on Integrated Substrate (SoIS) leverages the use of the InFO RDL process to create a high-density RDL on top of a build-up substrate. High-density routing of <10 μm pitch is possible and the via size is 25 μm. An advantage is more SerDes parings and mitigated signal crosstalk. The small mesh (10*10 μm) on the power and ground planes should provide significantly better return loss (<-45dB). A 91mm x 91mm organic substrate test vehicle has a yield higher than 95 percent. TSMC also reports 100 percent yield on a 110mm x 110mm SoIS [26]. The package is targeted to replace large format, high layer count build-up substrates.

3.1.7 3D Solutions with Hybrid Bonding

3D solutions with hybrid bonding are moving into production at TSMC with AMD as the first customer, and are in development at IBM, Intel, and Samsung.

AMD will ship its V-Cache solution based on TSMC's 3D with hybrid bonding for a gaming application early next year. A 6mm x 6mm SRAM is direct bonded on top of the logic device using a chip-on-wafer process.

IBM has announced it is developing a 3D integration solution with hybrid bonding for AI applications. The 3D solution will provide the highest density and is targeted for 5nm nodes and beyond. IBM refers to the logic devices as "nanosheets" and indicates design considerations and thermal management are important.

3.2 Mobile Solutions

Apple's A14 for the iPhone 12 was fabricated on TSMC's first-generation 5nm semiconductor node and the A15 processors for the iPhone 13 are fabricated on TSMC's second-generation 5nm process node. Both devices are packaged in TSMC's InFO PoP.

Table 3.7 provides details of the processor packages using TSMC's InFO found in Apple's iPhones. The Cu pillar size and pitch are the same for the A15 application processor as the A14. The total Cu pillar count on the A15 increased to 8,656 with a 21.5 percent larger die size.

Table 3.7. Apple's Processors in TSMC's InFO

Item	A14	A15
Semiconductor Node	1st generation 5nm	2nd generation 5nm
Processor size (mm x mm)	10.32 x 8.56	12.63 x 8.50
Number of Cu pillars	7,053	8,656
Pitch (μm)	80, 110	80, 110
InFO RDLs	3	3
RDL min. L/S	8/8	8/8
InFO package size (mm)	14.67 x 12.87 x 0.38	17 x 12.8 x 0.38
Total PoP height	0.86	0.86
Ball count	1,140	1,521
Ball diameter (μm)	190	190
Ball pitch (mm)	0.32	0.31

Source: TechSearch International, Inc.

TSMC will offer the InFO Bottom only (InFO_B) package for future application processors to provide enhanced performance with lower parasitics. TSMC will use its deep trench capacitor technology. InFO_B remains a chip-first package in which the die with a Cu post is mounted face-up on a carrier and molded. The mold compound is ground down and the Cu post is exposed. The RDL is formed and patterned.

Table 3.8 provides advantages of the processor packages using TSMC's InFO_B for a 14mm x 14mm package. With InFO_B it will be possible to have a memory package from any supplier mounted on the application processor package at board-level assembly. The contract assembly service provider will attach the LPDDR DRAM on top of the InFO containing the application processor to create the PoP.

Table 3.8. TSMC's InFO_B Advantages

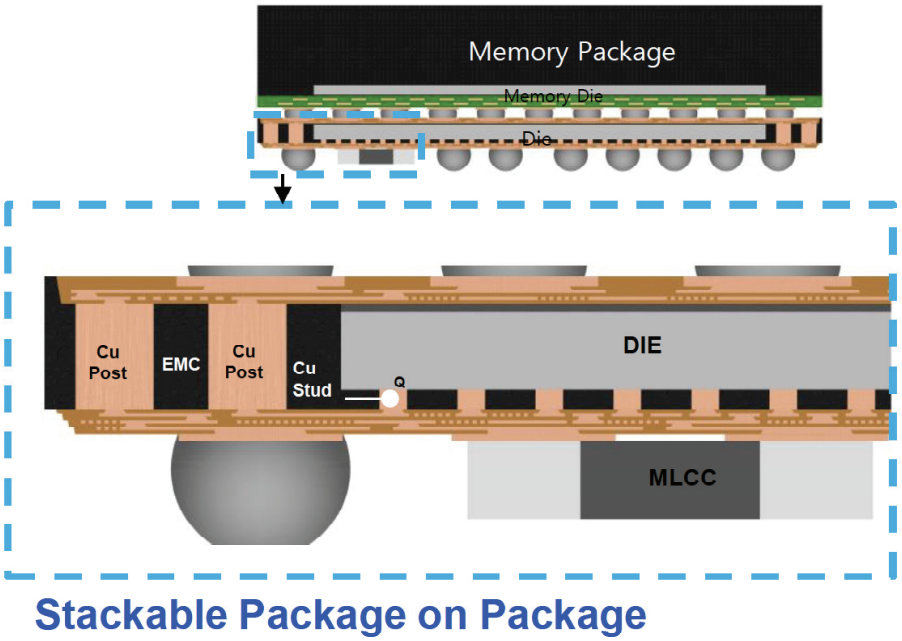
Attribute	InFO_B	FC-CSP
CPU voltage drop decrease	1.06X	1X
Max chip size (mm^2)	135	115
CPI sensitivity	Low	High
TIV/TMC pitch (μm)	180	~270

Source: TechSearch International, Inc., adapted from TSMC.

MediaTek is expected to be a customer for InFO_B, with its application processors fabricated on the 5nm semiconductor node in Q1 2022.

Deca has proposed its M-Series™ FO-WLP process for mobile applications. Nepes, a licensee of the M-Series™ process, has introduced a stackable package structure called mPoP that allows the memory package to be stacked on top of the application processor packaged in M-Series™[27]. Figure 3.5 shows the structure.

Figure 3.5. mPoP based on M-Series™ process.



Source: Nepes corporation.

Samsung will introduce its chip last FO-WLP processed on a 300mm wafer carrier in one to two years. In the process, the application processor die is flip chip bumped and assembled on the RDL. The part is molded. Samsung and others indicate the die at advanced 3nm silicon nodes will typically be the same thickness, but the cost due to yield at the advanced nodes is an issue. For this reason, a chip last approach is suggested. There should be no difference in handling.

There are several drivers for the adoption of FO-WLP for mobile processors. In the advanced technology nodes, as the number of transistors increases, so does the bump density. A high-density substrate is required to route the signals. Companies are selecting a fan-out solution instead of a laminate substrate to achieve these high-densities. The laminate substrate shortage is also a driver. In addition, FO-WLP offers a low-profile package. Electrical performance advantages include low-profile Cu.

Future application processors are also expected to adopt a 3D solution with hybrid bonding for advanced semiconductor nodes. TSMC has announced its InFO SoIC will be ready in the middle of next year.

4 Growing Demand for HBM

High bandwidth memory (HBM) is used in applications where reduced latency is required between memory and logic. The major applications are AI training, networking, gaming and graphics, autonomous driving, and sensor processing. Suppliers of HBM include Micron, SK Hynix, and Samsung. Renesas also offers a low-latency HBM that is assembled by an OSAT.

HBM2e is in volume production for most applications. The price of HBM2e remains high, but the price of HBM3 is expected to be even higher. HBM3 is expected in 2023 for products including high-performance data centers, AI machine learning platforms, and supercomputers. It will provide a 2X increase in bandwidth and capacity per stack. HBM3 is expected to process up to 819 GB per second, a 78 percent increase over HBM2e [28]. Rambus indicates that HBM3 subsystem bandwidth will increase to 8.4 Gbps, compared with 3.6 Gbps for HBM2e. Capabilities will enable the next level of energy efficiency in terms of joules per transferred bit, as well as more designs with an HBM3-only memory solution with no additional off-package memory, according to Arm [29].

Rambus, with its acquisition of Northwest Logic, released an HBM3-ready interface consisting of a fully integrated physical layer (PHY) and digital memory controller. Integrating the PHY and controller makes HBM3 memory subsystems easier to use and reduces the complexity of ASIC designs [30].

The HBM3 introduced by SK Hynix will be square and is expected to be 11 mm x 11 mm, compared to the 10mm x 11mm HBM2. There will be more fine pitch bumps and the bump pitch is expected to be 96 μm x 119 μm. Two capacity types will be available: 16 GB and 24 GB. Thinning each of the 12 DRAMs to 30 μm is required for the 24 GB product.

4.1 HBM Forecast

High-performance computing and networking are the main product drivers for HBM. Table 4.1 provides a projection for HBM demand based on its use in AI accelerators, networking, and other applications including graphics. The estimate assumes that the majority of HBM stacks are 8-high stacks and that 12-high stacks will be used in the future.

Table 4.1. HBM Market Projections

	2020	2021	2022	2023	2024	2025	2026
Number of HBM stacks (millions)	26	38	57	83	104	127	163
Thousands of 300mm wafers	965	1,391	2,087	3,038	3,807	4,658	6,530

Source: TechSearch International, Inc.

5 Substrate Shortages

Unexpected demand, global supply chain uncertainty, accidents, and weather-related events have resulted in semiconductor shortages. All types of substrates are in short supply; including substrates for chip scale packages (CSPs) and flip chip ball grid arrays (FC-BGAs). Despite some capacity expansion over the next few years, and new plants planned to come online in 2024-25, the situation is not expected to improve for at least two to three years. Some companies are considering substitutes that do not use substrates, including fan-out wafer level packages (FO-WLPs). Layer count reduction in substrate designs with the adoption of RDL is also under consideration.

5.1 CSP Substrates

CSP substrate, including flip chip and wire bond, are also in short supply. Several companies in Taiwan, including Kinsus, Nan Ya PCB, and Unimicron will expand capacity. Simmtek will also expand capacity. Some companies are considering the use of FO-WLP because a laminate substrate is not required for the small body sizes.

5.2 Supply and Demand for FC-BGA

Unlike many segments of the industry, the shortage of FC-BGAs is not driven by the pandemic. FC-BGA substrates fabricated with build-up materials are required to support the fine pitch bumped die used for applications including CPUs for servers, laptops, desktops, AI accelerators, ASICs found in telecommunications, and media chips such as HDTV, DSPs, and FPGAs.

While there is increased demand for servers, laptops, and desktops, demand for additional substrate manufacturing capacity is primarily driven by the larger body sizes and increased layer counts in some segments.

Increased body sizes and layer counts for server CPUs are a major contributor to higher demand for substrate capacity. High-end server CPUs are expected to use body sizes up to 100mm x 100mm with 10 build-up layers on each side of the core. At the upper end of the spectrum, high-end network switch packages range from 70 mm to 90 mm on a side. Even larger body sizes are being considered. OSATs report that they expect to see requirements for 100mm x 100mm substrates by 2023. The minimum layer count is six or seven build-up layers per side, with a few eight-layer and designs with nine-build-up layers on the horizon. While the unit volumes are low, the panel requirements are large because the substrates are large and complex, impacting layout on the panel as well as panel yield. Even larger body sizes are expected for co-packaged optics.

The shortage has led to an increase in substrate prices of as much as 15 percent or more this year and a change in the business model. In many cases, substrate customers will subsidize the capacity expansion. One reason for a new business model is the cost of building a new state-of-the-art facility, which Intel estimates is up to $1 billion. For companies that have not adopted this the new business model, it may be difficult to obtain substrates.

To meet the growing demand, several companies have announced plans to add FC-BGA capacity. Companies including AT&S, Ibiden, Kinsus, Kyocera, Nan Ya PCB, Toppan, Samsung Microelectronics Company, Ltd. (SEMCO), Shinko Electric, Toppan, and Unimicron have all announced capacity expansions for this year through 2025. Ibiden's capacity from the rebuilt Gama plant will not be available until 2026. Domestic Chinese suppliers such as Shennan Circuit (SCC) and PCB maker ZDT (Avery) are also planning to enter the FC-BGA substrate market. Nonetheless, the growth in larger body size and higher layer counts threatens to continue to outpace capacity expansions.

TechSearch International's forecast for FC-BGA substrate demand and the planned capacity is provided in Table 5.1. The demand assumes that the body size growth is for server CPUs, network switch, and AI accelerators, with only small growth for graphics and ASICs.

Table 5.1. FC-BGA Substrate Supply and Demand

	2020	2021	2022	2023	2024	2025
Capacity (thousands of square meters)	8,150	10,405	11,646	12,575	14,748	15,080
Demand (thousands of square meters)	8,381	10,468	12,237	14,793	16,213	17,163

Source: TechSearch International, Inc.

Even without any increase in body size for graphics and ASICs, and assuming development of alternative substrate technologies for network switch packages that allow higher substrate yields, demand will still exceed capacity (see Table 5.2).

Table 5.2. Impact of Higher Yielding Alternatives for Networking

	2020	2021	2022	2023	2024	2025
Capacity (thousands of square meters)	8,150	10,405	11,646	12,575	14,748	15,080
Demand (thousands of square meters)	8,381	10,468	12,237	14,136	15,444	16,269

Source: TechSearch International, Inc.

Panel capacity is shown in square meters, taking into account the typical layer count running on the line. To calculate demand, the area of the package is adjusted by panel utilization and yield to arrive at square meters of panels fabricated, which is multiplied by the number of build-up layers.

One of the major challenges in capacity expansion is the long lead time for some key production equipment, which has stretched to almost two years. This means that new capacity with construction starting today will not be ready for two years, and then the substrate will still need to be qualified.

There are concerns about availability of materials for substrate production including those to produce the core and the build-up material. There are two main suppliers of build-up material: Ajinomoto and Sekisui Chemical. Ajinomoto has a major share of the market and promises to keep up its capacity expansion to meet demand. Core material suppliers are also expected to try to maintain sufficient capacity to meet demand.

6 Leadframe Packages

Leadframe packages such as QFNs remain the workhorse of the industry. While flip chip is increasingly used for some packages, the majority continue to use wire bond. TechSearch International's partner in Japan recently conducted an analysis of some of the materials used for QFN and DFN packages (see Table 6.1). Gold bonding wire continues to be used, but a number of companies have switched to Cu. TechSearch International estimates that Cu accounts for a growing share QFN packages. Solder paste is still used by some companies, but Ag paste is seeing expanded adoption. Some companies are evaluating Cu-sintered materials for power applications.

Table 6.1. QFN/DFN Materials Analysis Summary

Company	Plating		Base Material	Bond Wire	Remarks
	Die-pad	Lead			
Infineon IR3555MTRPBF	Ni-Pd-Au	Ni-Pd-Au	C194 8 mil (0.203 mmt)	Au	Ag paste
STMicroelectronics STPS30170DJF-TR	Au	Sn	C194 10 mil (0.254 mmt)	-	Solder paste
Monolothic Power Systems MPM3822CGRH-P	Sn	Sn	C194 8 mil (0.203 mmt)	-	Ni plated inductor chip is embedded
RECOM RPX-2.5-CT	Sn	Sn	C194 8 mil (0.203 mmt)	-	Ni plated inductor chip is embedded
Vishay Siliconix SIRA60DP-T1-G3	None	Sn	C194 10 mil (0.254 mmt)	Au	Solder paste
STMicroelectronics STL260N4F7	Ag	Sn	C194 10 mil (0.254 mmt)	Au	Solder paste
Rohm UT6JC5TCR	NA	Sn	C194 5 mil (0.127 mmt)	Cu	Ni plated inductor chip is embedded
Vishay Siliconix SIDR680ADP-T1-RE3	Ag	Sn	C194 8 mil (0.203 mmt)	Au	
Vishay Siliconix SIZ998BDT-Ti-GE3	Sn	Sn	C194 8 mil (0.203 mmt)	Au	Ag paste
Toshiba XPN12006NC.L1XHQ	None	Sn	Dilute copper alloy 6 mil (0.152 mmt)	-	Solder paste
Onsemi NTTFS2D1N04HLTWG	None	Sn	C194 8 mil (0.203 mmt)	Cu	Solder paste
Texas Instruments CSD19537Q3	Ag	Sn	C194 8 mil (0.203 mmt)	Au	-
Infineon IRLH2242TRPBF	Ni-Pd-Au	Ni-Pd-Au	C194 8 mil (0.203 mmt)	Cu	Ag paste
pSemi(Murata) PE64102B-Z	Ni-Pd-Au	Ni-Pd-Au	C194 6 mil (0.152 mmt)	Au	Ag paste
Onsemi FDMA008P20LZ	None	Sn	C194 8 mil (0.203 mmt)	Cu	Solder paste
Monolithic Power Systems MP5073GG-P	None	Sn	C194 8 mil (0.203 mmt)	Cu	
Infineon IR388MTRPBF	Ni-Pd-Au	Ni-Pd-Au	C194 8 mil (0.203 mmt)	Cu	Ag paste

Company	Plating		Base Material	Bond Wire	Remarks
	Die-pad	Lead			
Texas Instruments MSP430G2001IRSA16T	Ni-Pd-Au	Ni-Pd-Au	EFTEC-64T 8 mil (0.203 mmt)	Au	Ag paste
Texas Instruments TPS70633DRVT	Ni-Pd-Au	Ni-Pd-Au	EFTEC-64T 8 mil (0.203 mmt)	Cu	Ag paste
STMicroelectronics STM32L151CCU6	Au	Sn	C7025 6 mil (0.152 mmt)	Ag	Ag paste
Texas Instruments CC3100R11MRGCR	Ni-Pd-Au	Ni-Pd-Au	C194 8 mil (0.203 mmt)	Au	Ag paste
Renesas R5F523W8ADNG#30	None	Sn	C194 8 mil (0.203 mmt)	Cu	
Texas Instruments DAC348IRKDT	Ni-Pd-Au	Ni-Pd-Au	C7025 5 mil (0.127 mmt)	Cu	Ag paste
Texas Instruments TUSB7320RKMT	Ni-Pd-Au	Ni-Pd-Au	EFTEC-64T 8 mil (0.203 mmt)	Cu	Ag paste
Rohm BD9S400MUF-CE2	Ag	Sn	EFTEC-64T 8 mil (0.203 mmt)	Cu	Ag paste
Texas Instruments LM536253QRNLTQ1	Sn	Sn	C194 8 mil (0.203 mmt)	-	Unknown

Source: TPSS.

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