Advanced Packaging Update

- TRACK INNOVATION
- IDENTIFY TRENDS
- ANALYZE GROWTH
- INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY

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Semiconductor Industry Trends

China's Power Shortage

- **China's power shortages curtailing factory output in manufacturing in many sectors**
  - Impact on major areas electronics areas such as Jiangsu Province (includes Suzhou and Kunshan), Hubei, and Guangdong
  - Shortage of coal is causing the problem
  - May last until end of winter
- **Impact for electronics industry**
  - PCB production
  - Copper clad laminate (CCL) production used for PCBs and some substrates
  - Semiconductor package assembly operations
  - Packaging materials such as underfill, die attach, mold compound, and solder balls
  - Test socket production
  - Passive devices

Semiconductor Shortages

- **Semiconductor shortages continue, especially in auto industry**
  - IPC survey shows >50% of companies expect shortage to last until at least Q2 2022
- **Auto industry expected to have revenue loss of $210 billion in 2021**
  - Ford, GM, Nissan, Daimler, BMW, Renault, and Toyota
  - Component shortages include microcontrollers and sensors
  - Renesas Electronics, NXP Semiconductor, and Infineon working on increasing output
  - Renesas 200mm Kyushu fab and 300mm Naka fab at full capacity, Renesas orders six microcontrollers (40nm node) from TSMC for every one it makes
  - TSMC will build fab in Japan to support image sensor and microcontroller production
  - Shortage of 200mm wafer fab capacity
  - SEMI reports that 200mm fab capacity will increase by 950,000 wafers (17%) from 2020 to 2024 to reach a record high of 6.6 million wafers put month
- **Number of base stations installed in China will be lower than planned due to component shortage**
- **Equipment such as wire bonders have lead times of 42 weeks for some suppliers, in a few cases some suppliers have been able to decrease lead times to 4 to 5 months**

Shortages Lead to Higher Prices (2020 vs. 2021)

- Display drivers 50%
- Microcontrollers 30-40%
- Power management chips 30-40%
- Leadframes 25-30%
- Build-up substrates for FC-BGA >15-20%
- Ajinomoto build-up film 20-30%
- OSAT assembly services 15-20%
- Foundry services 8-10%
- Wafer materials 5%

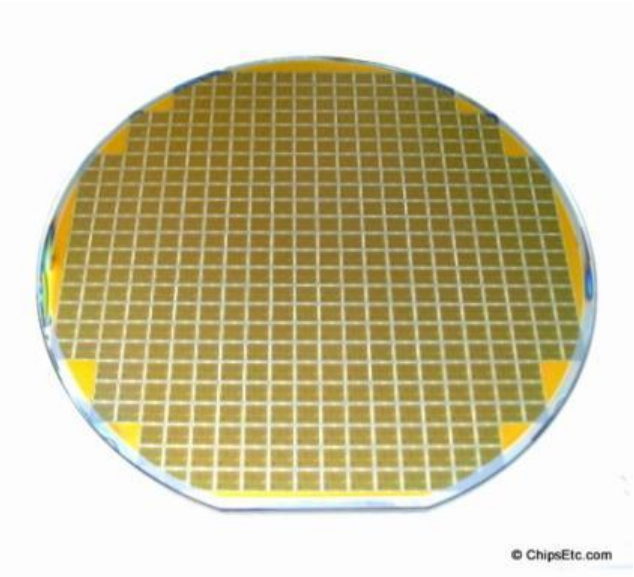
Source: Counterpoint Research and TechSearch International, Inc..

Government Semiconductor Spending: The New Arms Race

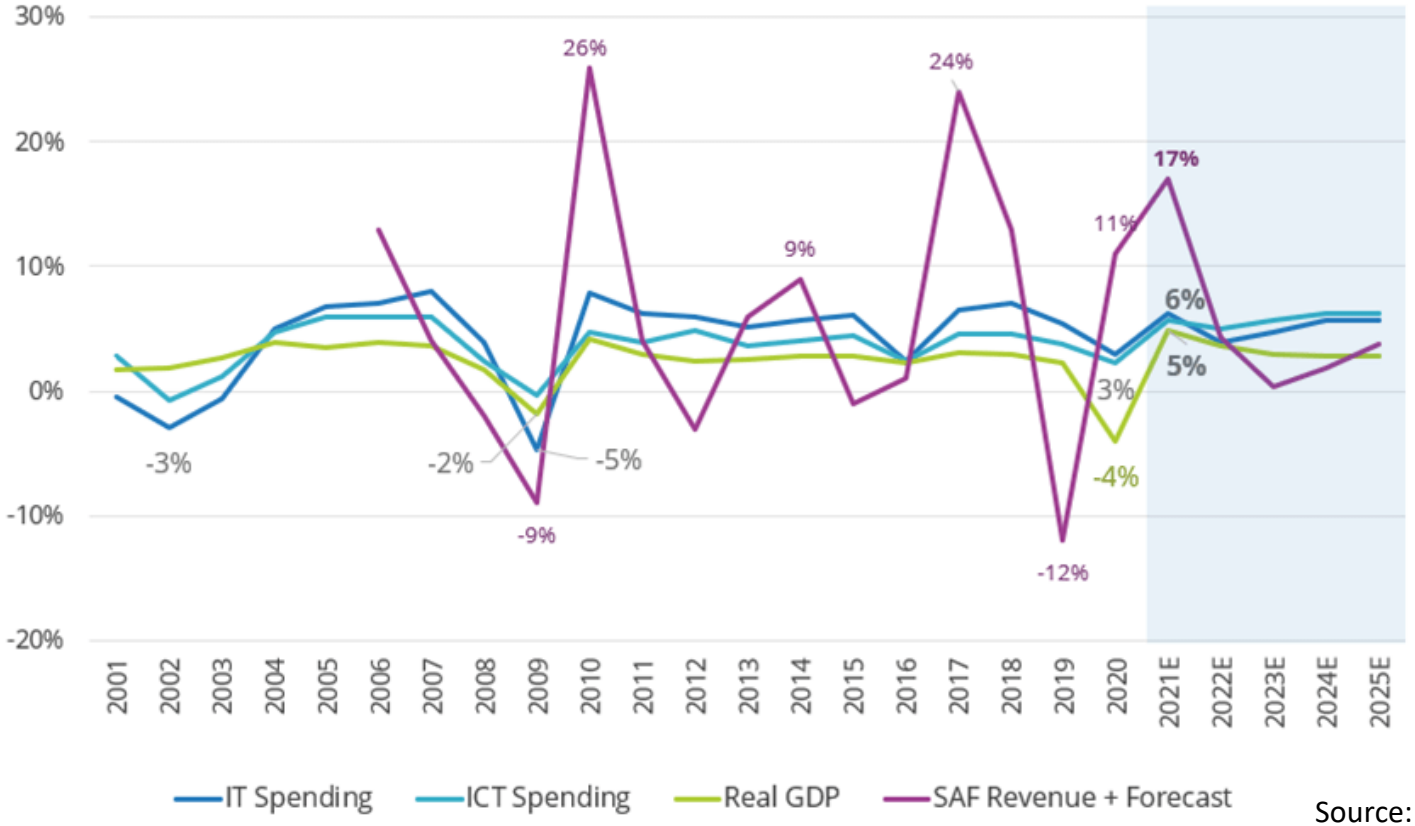
- **U.S. proposes to spend $52 billion in semiconductor production in U.S.**
  - Only 12% of global semiconductor manufacturing capacity in U.S.
- **EU is considering building an advanced semiconductor fab in Europe**
  - EU "European Chips Act" calls for manufacturing up to 20% of all leading-edge semiconductors in the world by 2030 (discussions with TSMC about fab location)
  - France aims to boost semiconductor production by 2030 with €6 billion
  - About 10% of world's semiconductor manufacturing facilities are in Europe
  - EU Commission's European Innovation Council selected 65 start-ups and small companies to receive €363 million in funding (grant financing and equipment investment) for healthcare, digital technologies, energy, biotechnology, space, and other
- **China is investing >$150 billion in semiconductors from 2014-2030**
  - Accounts for only 7.6% of total global semiconductor sales with foundries focused on more mature nodes
- **India is pushing to establish semiconductor production as part of "Made in India"**
  - Offering $1 billion to each semiconductor company that establishes operations in India

Semiconductor Foundry Expansions

- **Intel plans 2 new fabs in Arizona**
  - Plans to spend $20 billion by 2024
  - One fab is for Intel Foundry Services, includes partnership with IBM
- **TSMC spending $100 million for overseas expansion through 2023**
  - Arizona fab for 5nm technology with a capacity of 20,000 wafers per month by 2024
  - Announced plan to build a fab in Japan, primarily to serve Sony and other Japanese clients (22nm and 28nm node for image sensors and microcontrollers)
  - Considering a plant in Germany
- **Samsung will expand U.S. semiconductor production**
  - Plans to build a new $17 billion facility (51.7 million sq. ft., 4X size of Austin, Texas plant)



Potential Semiconductor Over Capacity Projected



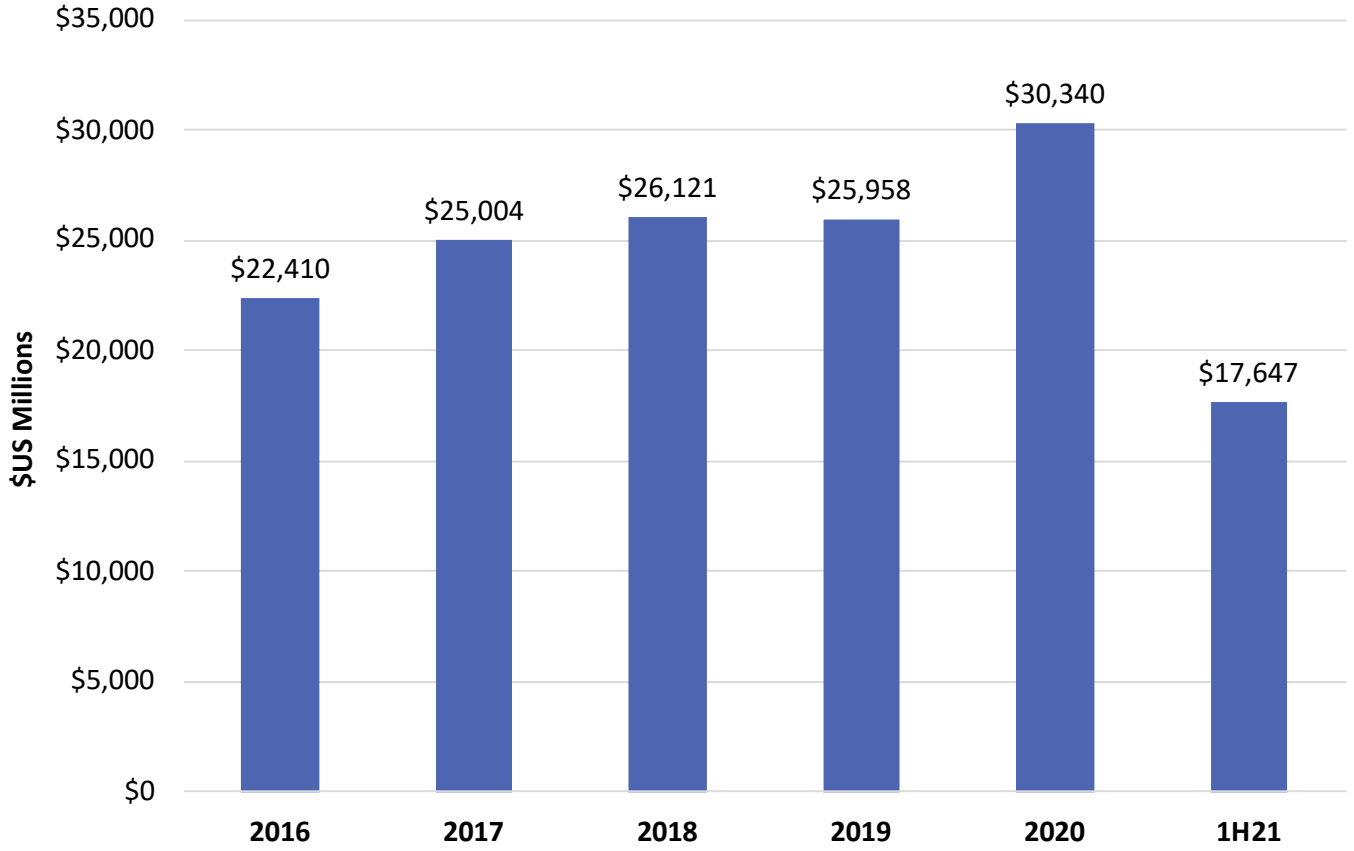
Source: IDC.

- **Current market projections from IDC**
  - Strong global recovery
  - Higher prices for DRAM and NAND Flash
  - Smartphone growth continues (Apple growth rate double Android)
  - Growth for high-performance computing and PCs
  - Edge device demand
- **IDC predicts potential over capacity in semiconductor industry by 2023 with current fab expansion plans**

OSAT Financials

Top 20 OSAT Revenue

Based on quarter average fluctuating exchange rates

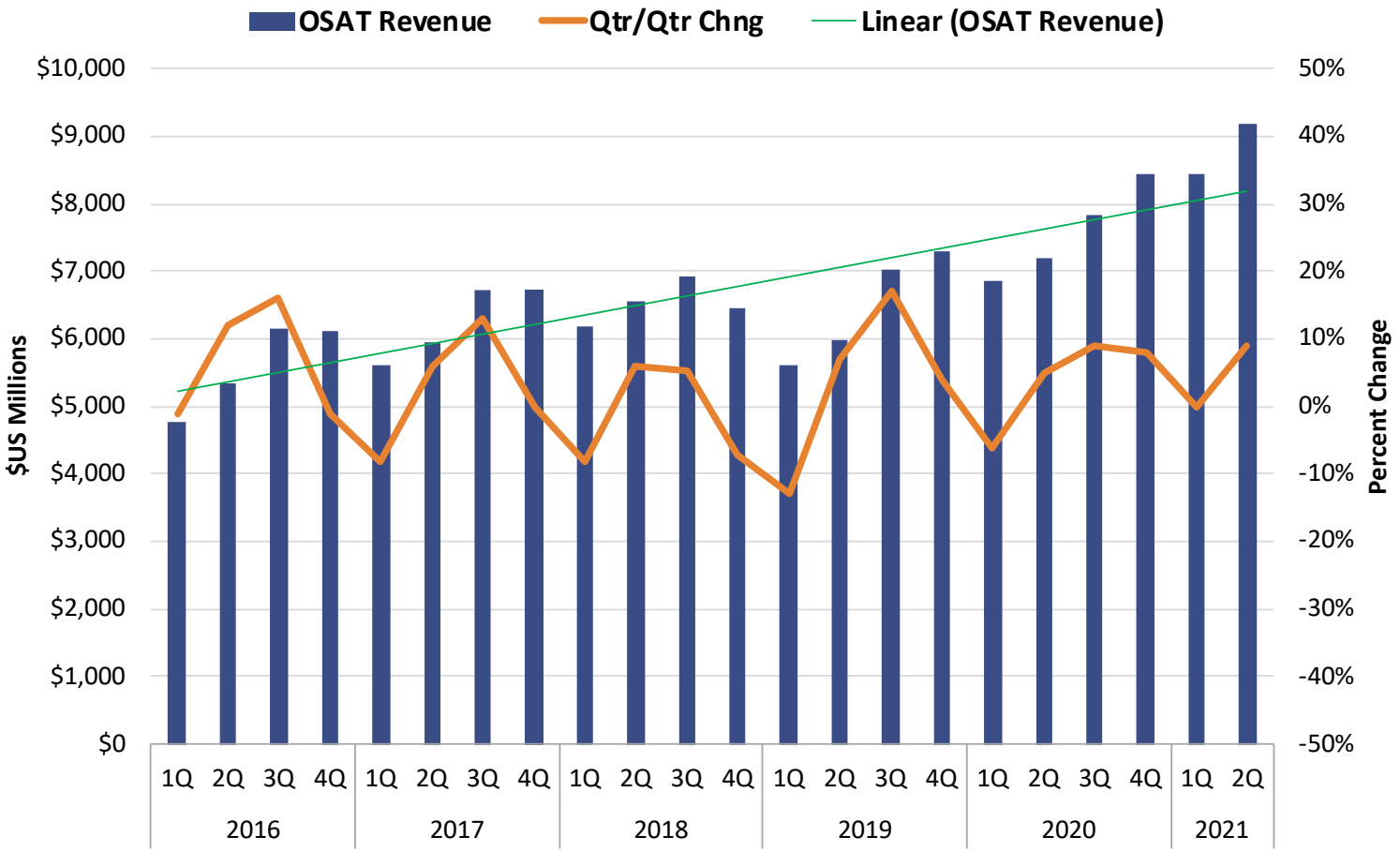


Source: TechSearch International, Inc.

- **Revenues generated by the top 20 OSATs reached a new record high during the first half of 2021**
  - Increased by 25.5% over the same period in 2020

Quarterly Revenue of the Top 20 Publicly Traded OSATs

Based on quarter average fluctuating exchange rates

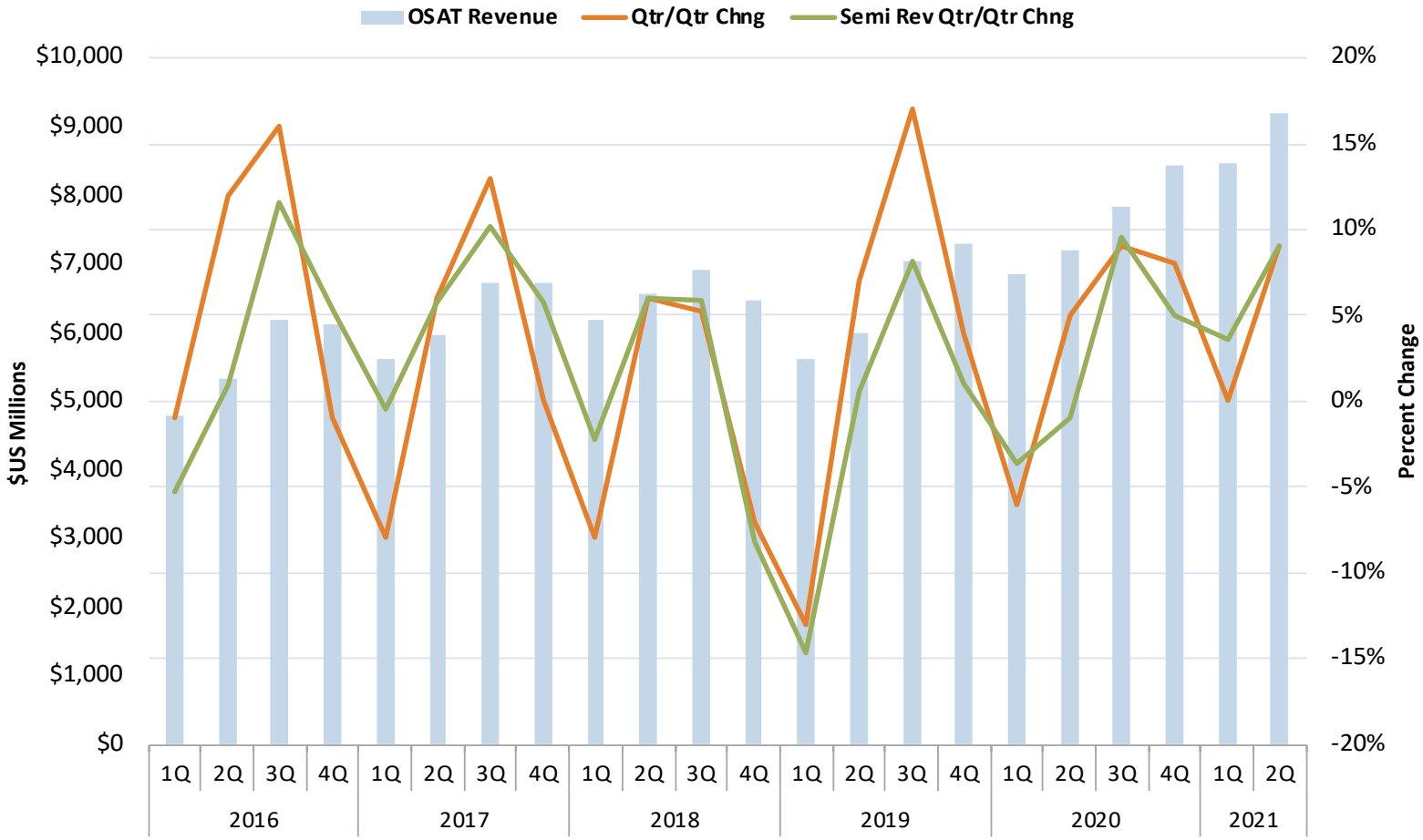


Source: TechSearch International, Inc.

- **2Q21 sales again set a new record**
- **OSAT industry registered growth for consecutive quarters**

Quarterly Revenue Trends for Top 20 OSAT Market and Semiconductor Industry

Based on quarter average fluctuating exchange rates



Source: TechSearch International, Inc.

- **Quarter-to-quarter growth in semiconductor revenue as reported by WSTS surged to 8.5% reaching an all time high as fab capacity utilization continued to be strained**
- **OSAT market growth recorded as 8.7% quarter-to-quarter with revenue at record high level**

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Revenue of Top 20 Publicly Traded OSATs

Based on quarter average fluctuating exchange rates

- **While slowing from first quarter, the top 20 OSATs registered 8.7% growth in Q2**
- **Record high Q2 results for 17 companies**
- **Return of demand for 5G, automotive**
- **Price increases continue driven by long lead times and very high loading along with increases in product complexity and higher test demand**
- **Overall capacity utilization continues to exceed 85% for many companies**

$US Millions (Totals may not add due to rounding)

Rank	Company	Headquarters	1Q 2021	2Q 2021	Q-t-Q
1	ASE Technology Holdings (1)	Taiwan	$2,499.4	$2,710.2	8.4%
2	Amkor Technology	U.S.	$1,326.2	$1,407.0	6.1%
3	JCET Group	China	$1,035.9	$1,100.2	6.2%
4	Powertech Technology (2)	Taiwan	$656.5	$737.0	12.3%
5	Tongfu Microelectronics	China	$504.3	$591.6	17.3%
6	Tianshui Huatian Technology	China	$400.8	$464.9	16.0%
7	KYEC	Taiwan	$271.8	$271.5	-0.1%
8	UTAC (3)	Singapore	$273.7	$323.9	18.3%
9	ChipMOS	Taiwan	$230.3	$249.6	8.4%
10	Chipbond	Taiwan	$228.7	$249.2	9.0%
11	SFA Semicon	Korea	$125.5	$136.1	8.4%
12	Sigurd (includes Winstek)	Taiwan	$124.8	$150.3	20.4%
13	Carsem	Malaysia	$129.6	$130.2	0.5%
14	AOI	Japan	$99.2	$98.0	-1.2%
15	LB Semicon	Korea	$102.3	$108.4	6.0%
16	FATC	Taiwan	$90.3	$88.2	-2.3%
17	Ardentec	Taiwan	$93.4	$102.7	10.0%
18	Unisem	Malaysia	$92.0	$97.5	6.0%
19	Tong Hsing + Kingpak (4)	Taiwan	$85.6	$90.8	6.1%
20	Nepes	Korea	$85.4	$84.0	-1.6%
Total Revenue			**$8,455.7**	**$9,191.3**	**8.7%**

1) Only external sales for packaging & test
2) Includes Greatek
3) No longer publicly traded
4) Does not include ceramic substrates

Source: TechSearch International, Inc.

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Revenue of Top 20 Publicly Traded OSATs

Based on quarter average fluctuating exchange rates

- **1H21 exceeded expectations of even the most optimistic projections of OSATs**
- **All the top 20 OSATs outperformed their 1H20 results**
- **Unprecedented double-digit growth**
  - >30% for 11 of the top 20 OSATs

$US Millions (Totals may not add due to rounding)

Rank	Company	Headquarters	1H 2020	1H 2021	H-t-H
1	ASE Technology Holdings (1)	Taiwan	$4,319.8	$5,209.6	20.6%
2	Amkor Technology	U.S.	$2,325.5	$2,733.2	17.5%
3	JCET Group	China	$1,702.2	$2,136.0	25.5%
4	Powertech Technology (2)	Taiwan	$1,275.0	$1,393.5	9.3%
5	Tongfu Microelectronics	China	$663.7	$1,095.9	65.1%
6	Tianshui Huatian Technology	China	$527.8	$865.8	64.0%
7	KYEC	Taiwan	$489.1	$543.4	11.1%
8	UTAC (3)	Singapore	$341.1	$597.6	75.2%
9	ChipMOS	Taiwan	$367.4	$479.9	30.6%
10	Chipbond	Taiwan	$344.9	$477.8	38.5%
11	SFA Semicon	Korea	$246.6	$261.6	6.1%
12	Sigurd (includes Winstek)	Taiwan	$187.4	$275.1	46.8%
13	Carsem	Malaysia	$183.9	$259.8	41.3%
14	AOI	Japan	$194.0	$197.2	1.6%
15	LB Semicon	Korea	$170.0	$210.7	23.9%
16	FATC	Taiwan	$165.5	$178.4	7.8%
17	Ardentec	Taiwan	$145.3	$196.1	35.0%
18	Unisem	Malaysia	$137.2	$189.5	38.1%
19	Tong Hsing + Kingpak (4)	Taiwan	$133.4	$176.4	32.2%
20	Nepes	Korea	$144.4	$169.5	17.4%
Total Revenue			**$14,064.2**	**$17,647.0**	**25.5%**

1) Only external sales for packaging & test
2) Includes Greatek
3) No longer publicly traded
4) Does not include ceramic substrates

Source: TechSearch International, Inc.

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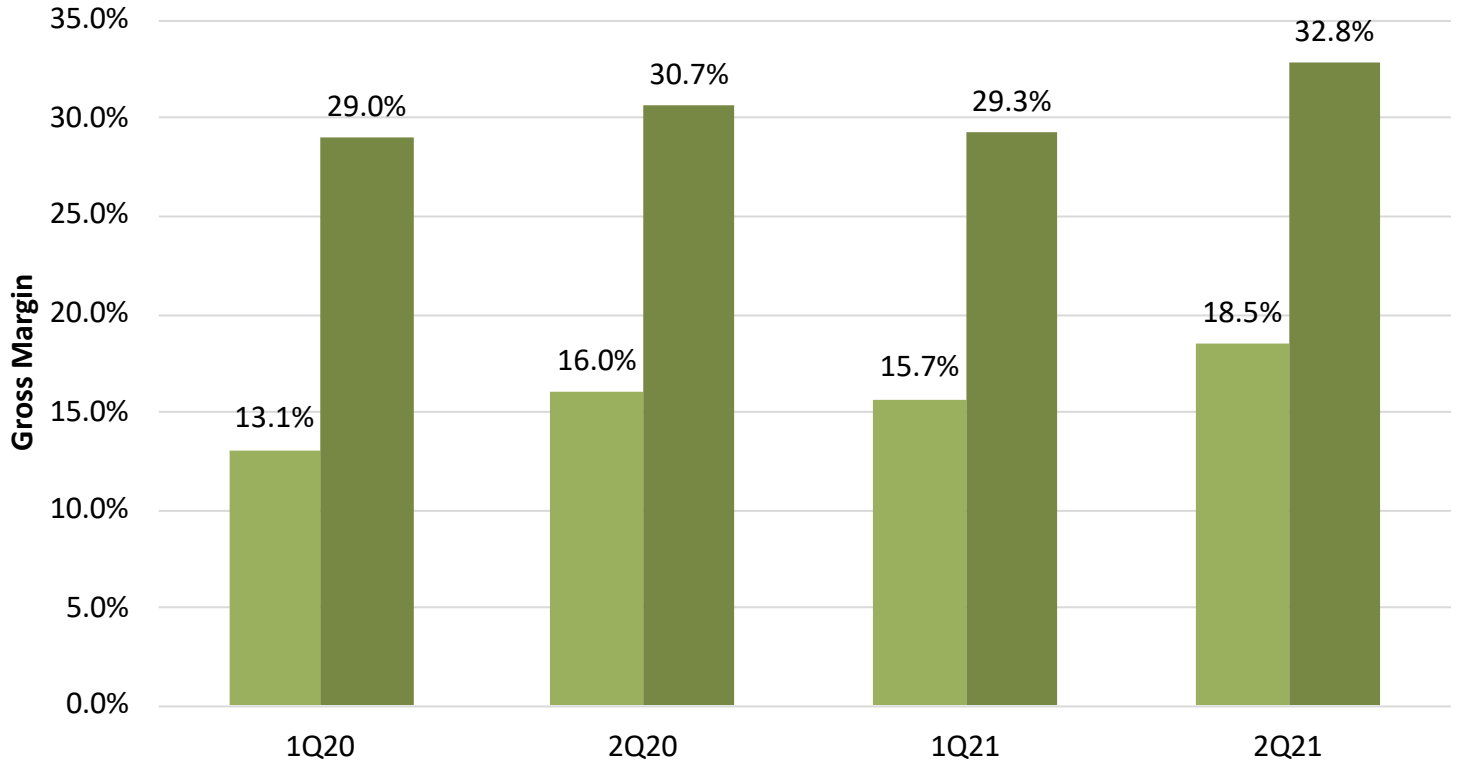
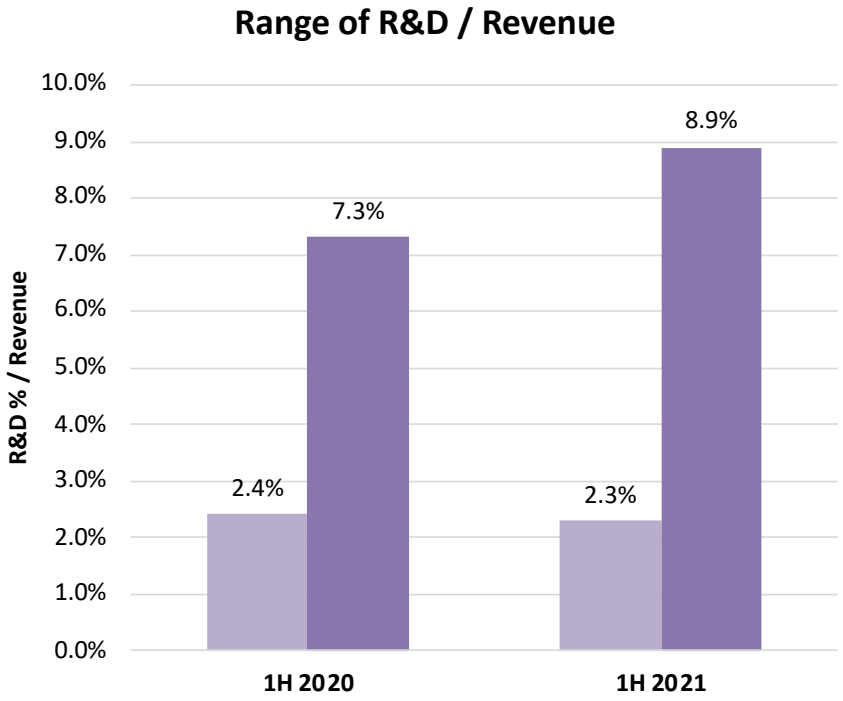
Gross Margin Performance for Top 10 Publicly Traded OSATs

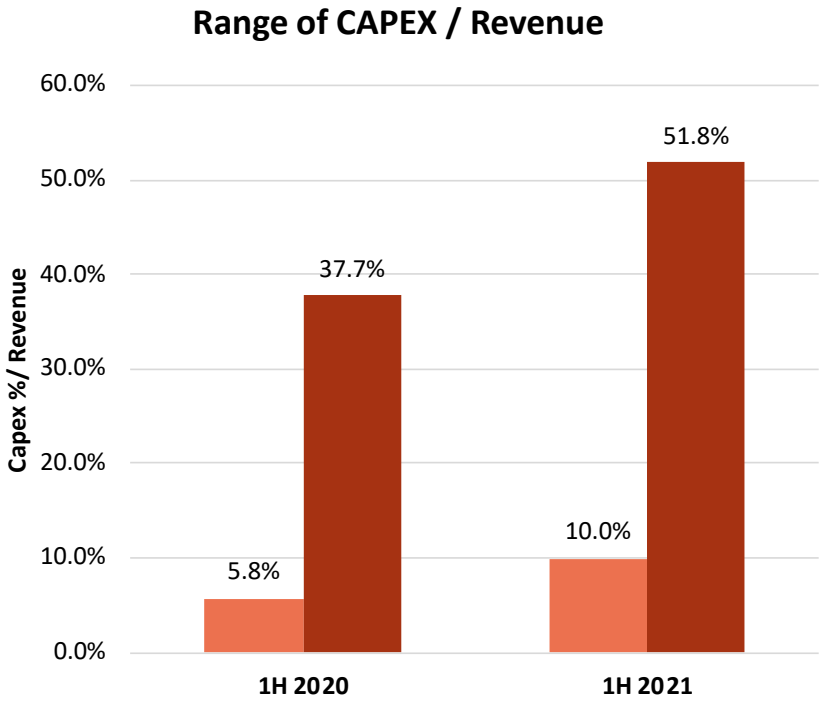


Source: TechSearch International, Inc.

- **Range of gross margin (low vs. high) shown**
- **Gross margins pushed upward as product value increases with complexity and price points rose as demand exceeded capacity**

Metrics for the Top 10 Publicly Traded OSATs





Source: TechSearch International, Inc.

- **With increased revenues, some companies showed a slight increase in R&D investment**
- **Capital investment was significantly increased as companies sought to expand capacity for wire bond, test, and bumping**

Advanced Packaging for Advanced Semiconductor Nodes

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Next Generation Packaging for Advanced Silicon Production

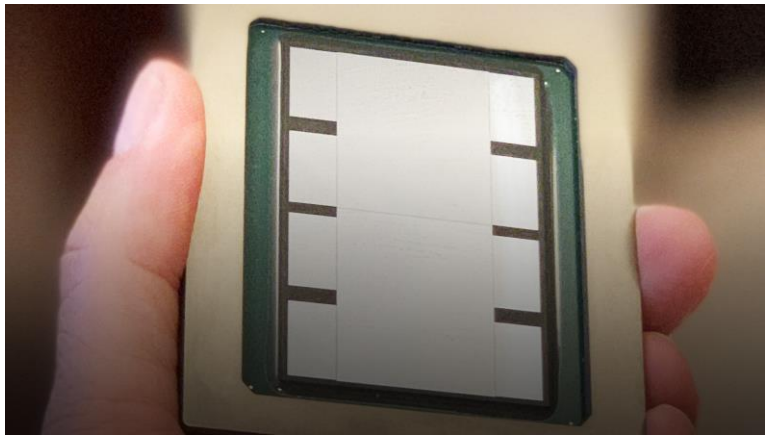
- **TSMC produces 92% of global advanced silicon (7nm and below); Samsung accounts for the remaining 8%**
  - TSMC's 3nm silicon node expected to move into production next year (some possible delay)
  - Samsung's gate-all-around (GAA) technology first designs expected in first half 2022, with 2nd generation scheduled for 2023, 2nm GAA transistor to be completed by 2025
  - Intel's version of 3nm scheduled for 2024 at new Arizona fabs
- **Companies developing advanced packaging technology for 3nm silicon nodes and beyond, expect increased use of chiplets, but concerns include:**
  - Package selection and design (silicon interposer, fan-out on substrate and other RDL structures, laminate substrates)
  - Assembly (3D vs. 2D, µbump vs. hybrid bonding)
  - Test (defect = discard entire package and all chiplets)
  - Thermal (thermal solutions, especially for 3D are critical)
  - EMI, mechanical, reliability, power delivery, timing, and function all important
- **Trade-offs**
  - Can save money on the advanced node fabrication with smaller, higher yielding die but package design and fabrication are more expensive

What Are Chiplets?

- **A chiplet is an integrated circuit block specifically designed to work with other chiplets to form a larger more complex system that often makes use of reusable IP blocks**
  - A chiplet can be created by partitioning a die into functions that are more cost effectively fabricated (smaller die, higher yield, and less advanced nodes)
  - A chiplet is a hard IP block
  - Functions with other chiplets, so design must be co-optimized and silicon cannot be designed in isolation
  - Made possible by communication using chiplet interface (proprietary today)
- **Differs from SiP or traditional MCM in that it is a new design, not just a combination of different "off-the-shelf" chips**
- **Chiplet is not the package, it's the design philosophy**
  - Change from "silicon centric thinking" to "system-level planning" and "co-design of IC and package"
  - The industry must think about chip design in a new way
  - Same impact as when the industry moved from a peripheral chip layout to area array!

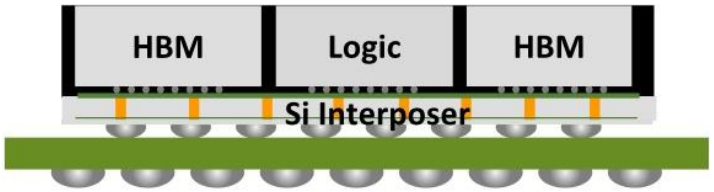
Moving to Larger Silicon Interposers

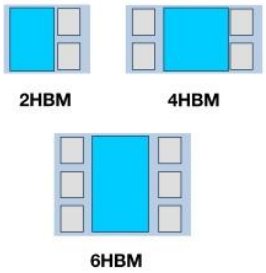
- **TSMC has been in production for 10 years, mature technology, highest density**
  - Xilinx uses 2X reticle for FPGA slices today
  - 4X reticle adoption by 2023 to support 12 HBMs
- **Samsung**
  - Demonstrated a 2,500mm^2 Si interposer for up to 2 logic die plus 8 HBMs
  - Qualification for 2,800mm^2 Si Interposer



Source: TSMC.

2,500mm^2 Si interposer, 8 HBMs, 2 Logic die 600mm^2, in 75mm x 75mm package
Silicon interposer mounted on laminated build-up substrate





Source: Samsung.

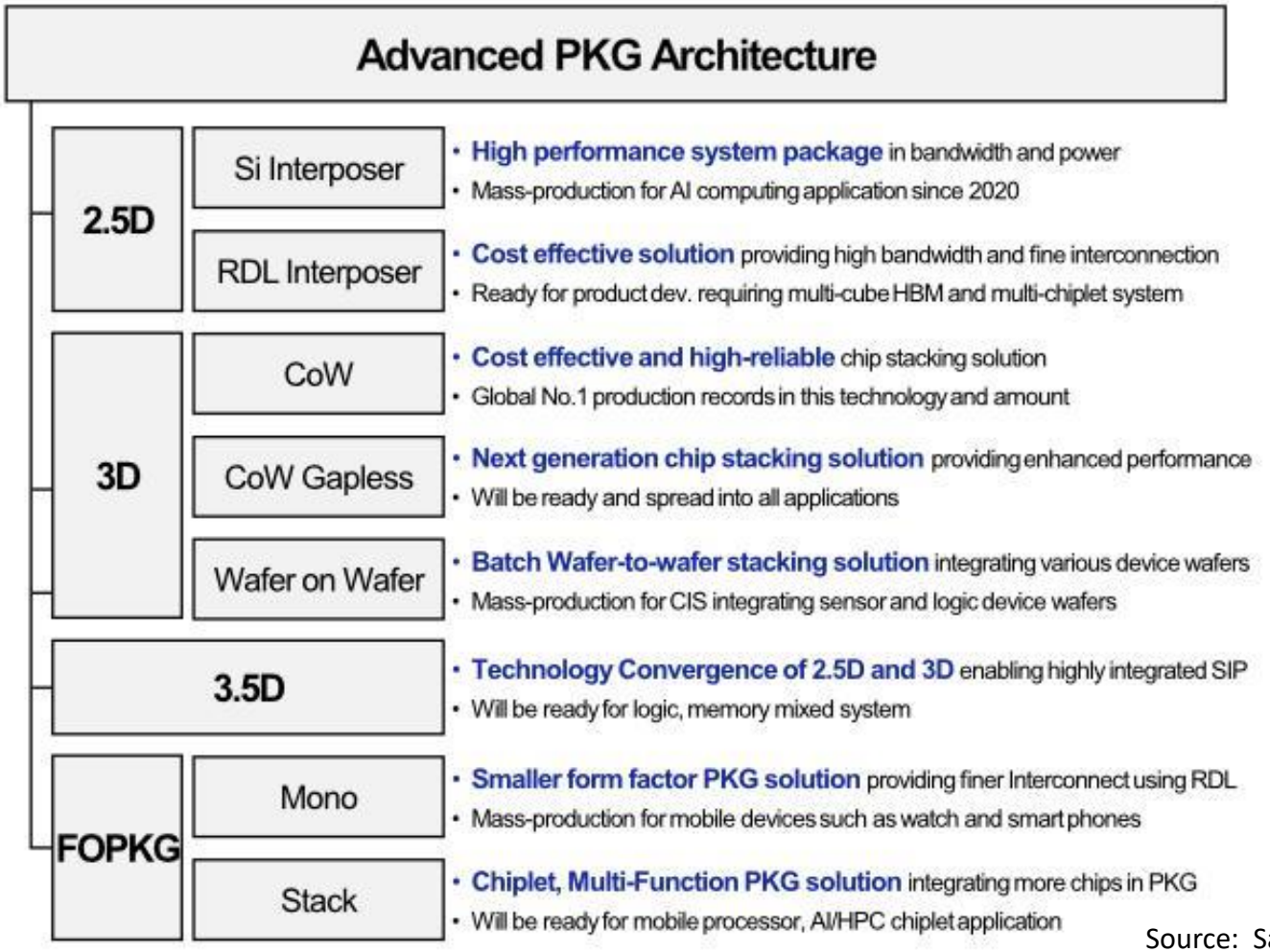
Silicon Interposer Products for Data Centers

- **Broadcom's Multi-Die ASIC for data center & cloud infrastructure**
- **5nm ASIC**
  - PCIe Gen5 protocol
  - 122Gbps SerDes
  - HBM2e operating at 3.6 Gbps
  - 3.6Tbps Die2Die PHY IP
- **Utilizes TSMC CoWoS**
- **Announced November 2020**

Source: Broadcom.

- **Marvell's new data infrastructure product using TSMC's 3nm silicon node, will be packaged in advanced D2D interface IP using TSMC CoWoS**
- **Marvell is also developing an ultra-low power, low latency parallel D2D interface compatible with Open Compute Project (OCP) chiplet standards**

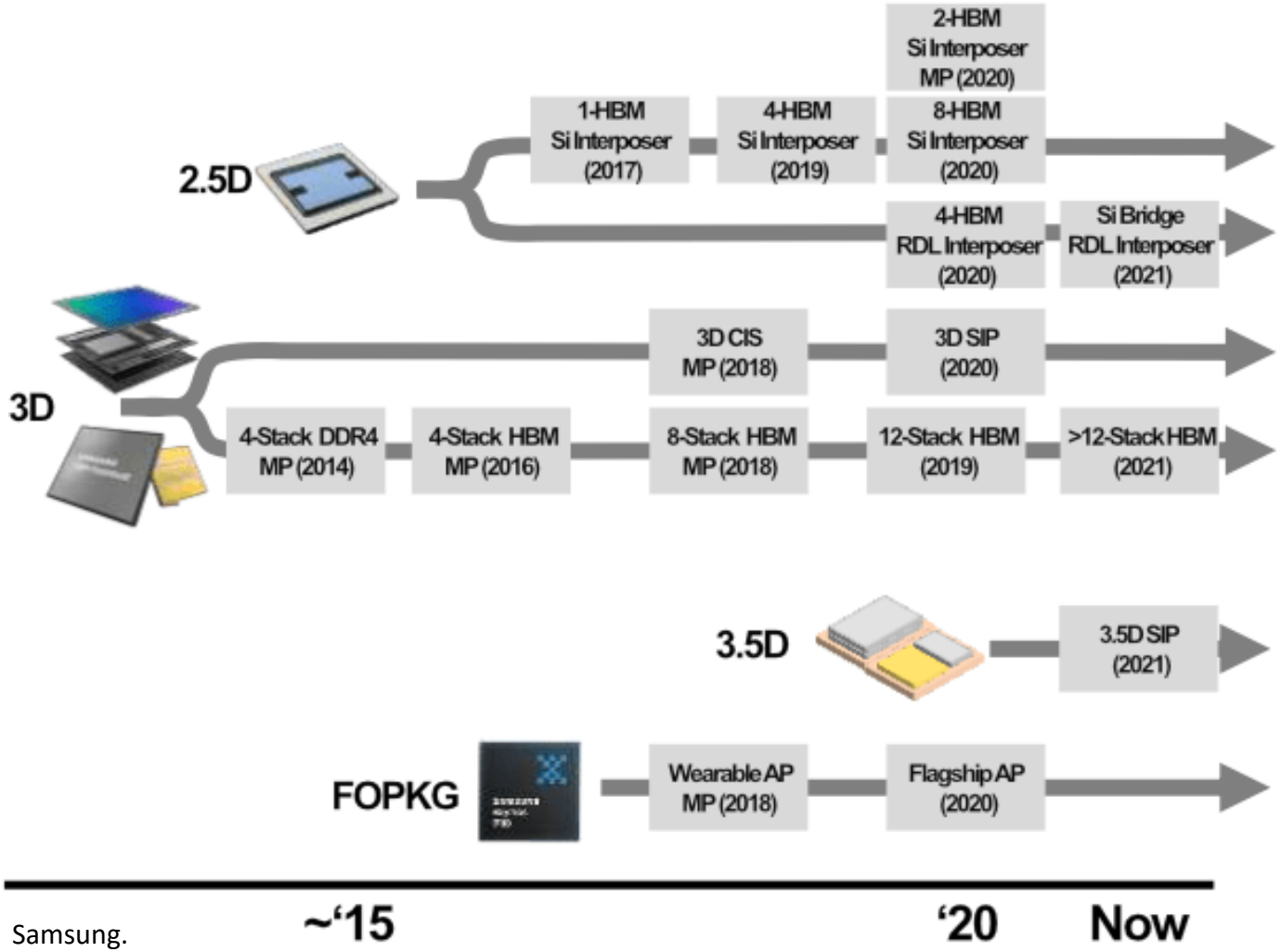
Samsung Advanced Packaging Options



Source: Samsung.

- **Options include vertical integration (3D), horizontal integration (Si Interposer & HD FO), form factor (fan-out)**

Samsung Advanced Packaging Options



Source: Samsung.

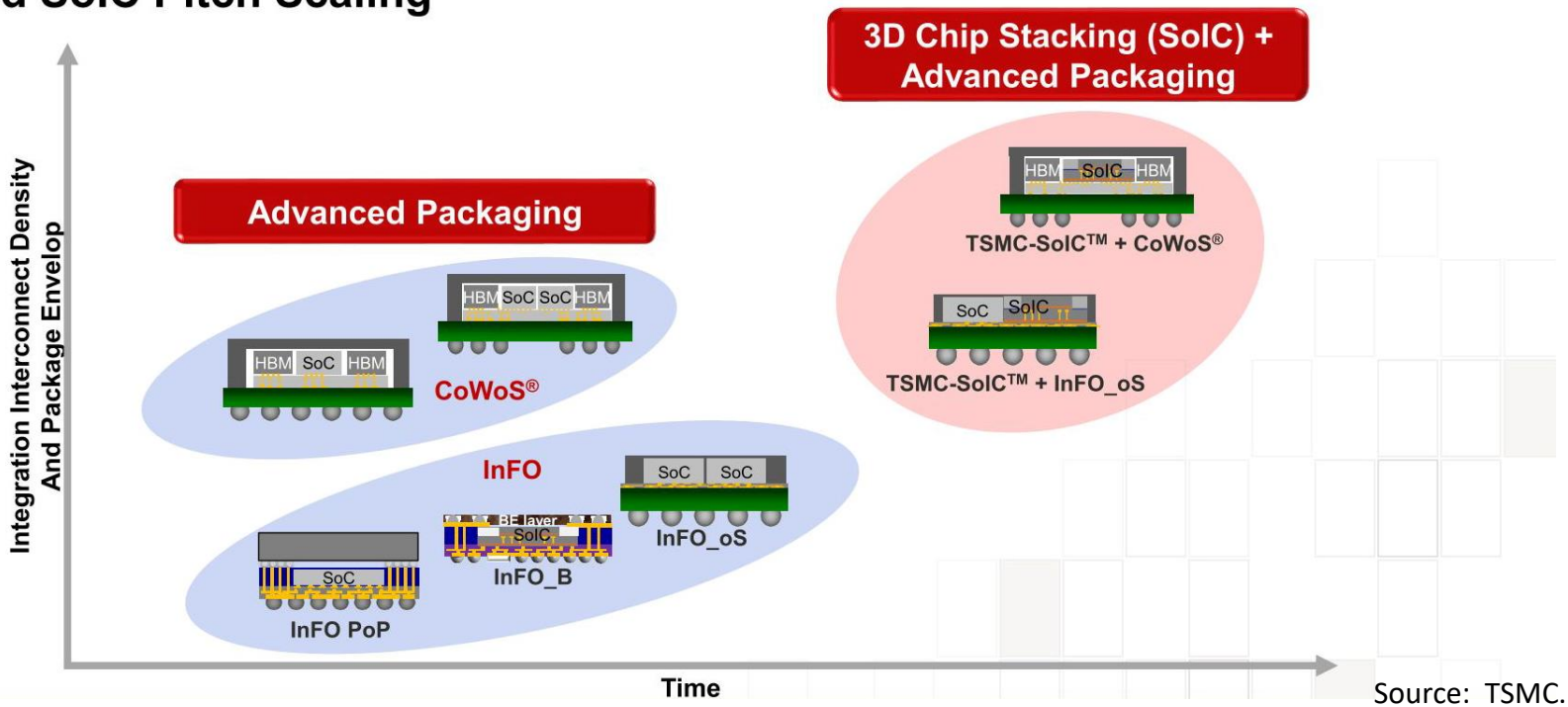
- **Increased use of HBM to meet BW needs in high-performance applications**

TSMC's 3DFabric Options

3DFabric™ Integration Technologies

tsmc Unleash Innovation

- 3DFabrics updates- additional structures, Packaging Envelop Increase and SoIC Pitch Scaling



Source: TSMC.

- CoWoS for chip last solutions, new RDL structures, and embedded bridge with TSVs
- InFO chip first versions, including options with embedded bridge

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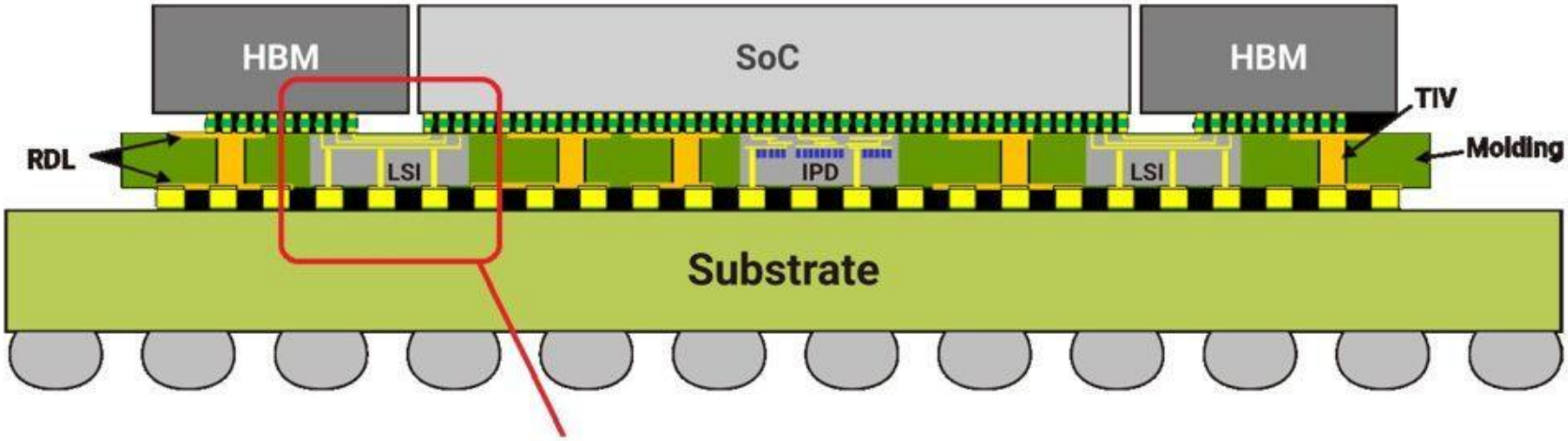
TSMC's CoWoS-L

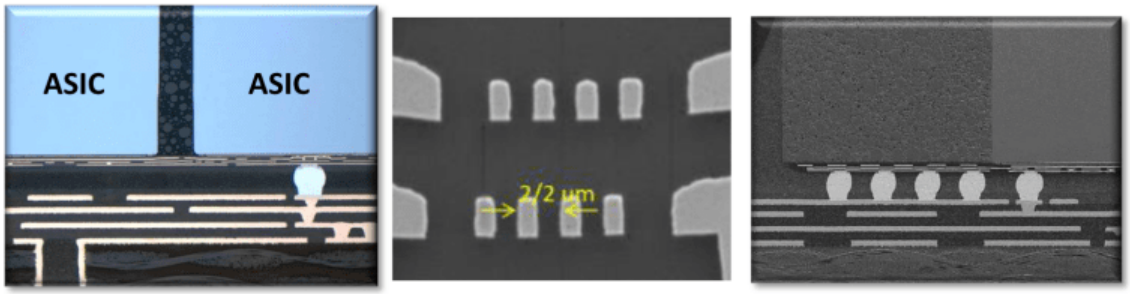


CoWoS-L, with embedded Local Silicon Interconnect bridge
"BEOL, chip-last assembly"

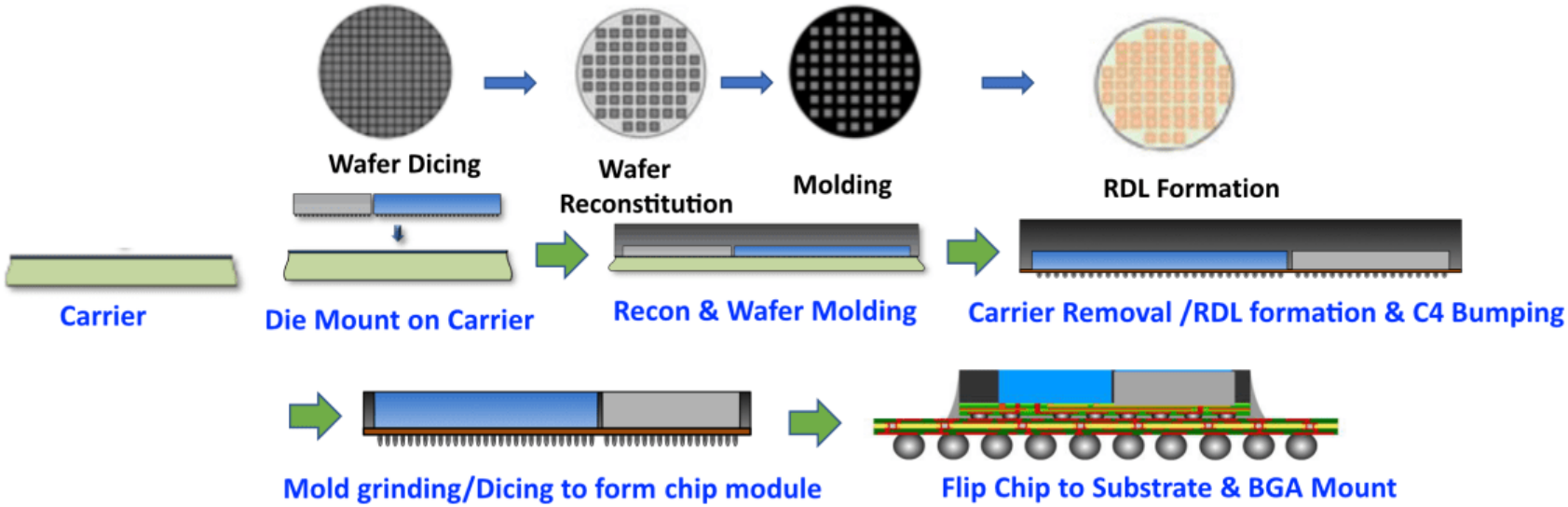
Source: TSMC.

- **CoWoS-L is a chip-last option (L = local silicon interconnect)**
- **Si interposer is replaced with an organic RDL**
  - Embedded bridge with TSVs used to increase signal density
- **Demonstrated a 1.5X reticle with logic + 4 HBM2e, 3X reticle size with 8 HBMs planned, 4X reticle size may be possible**
- **TSMC's deep trench capacitor (DTC) could be embedded in the RDL**

ASE's FOCoS-Chip First TV Structure and Process Flow



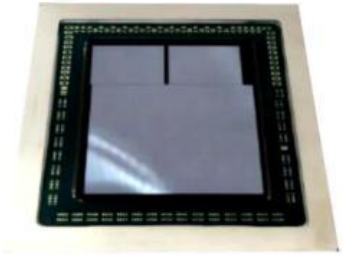
- 2 ASIC chiplets
- Module size: 30x28mm²
- 4 RDLs, L/S 2/2um
- Package size: 47.5x47.5mm²

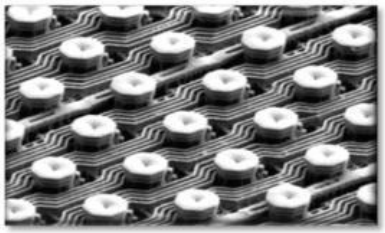


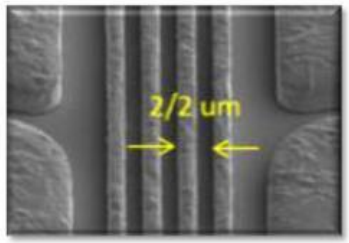
Source: ASE.

- **Improved electrical performance with the direct Cu to Cu interface (no bump)**
- **Die to FO interface pitch may be tighter because there is no bump**

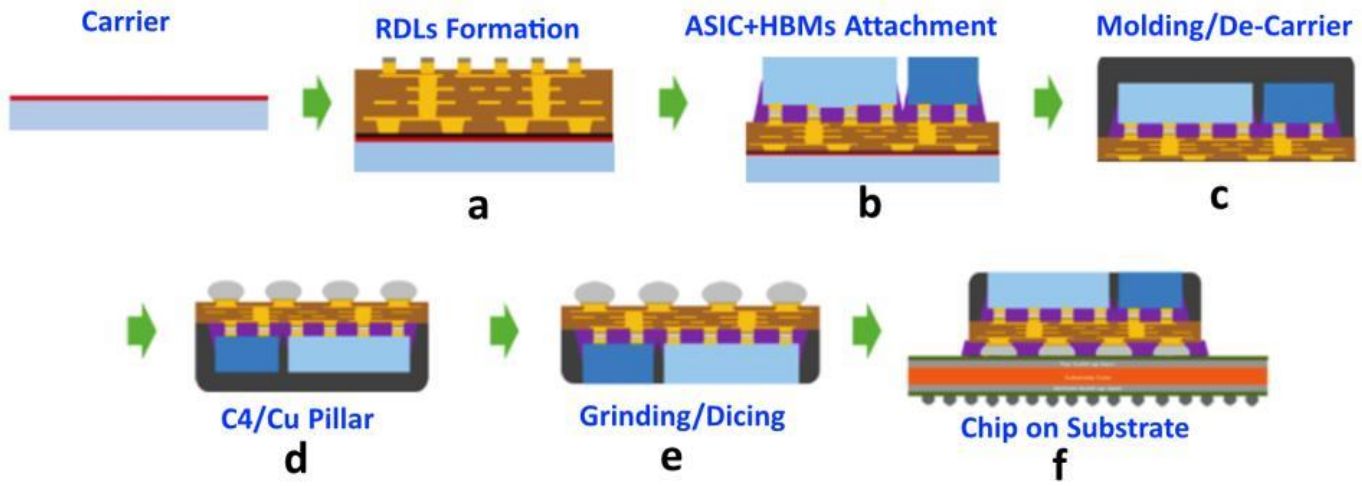
ASE's FOCoS-Chip Last TV Structure and Process Flow







- 1ASIC + 2HBM chiplets
- Module size: 30x28mm^2
- 4 RDLs, L/S 2/2um
- Package size: 47.5x47.5mm^2

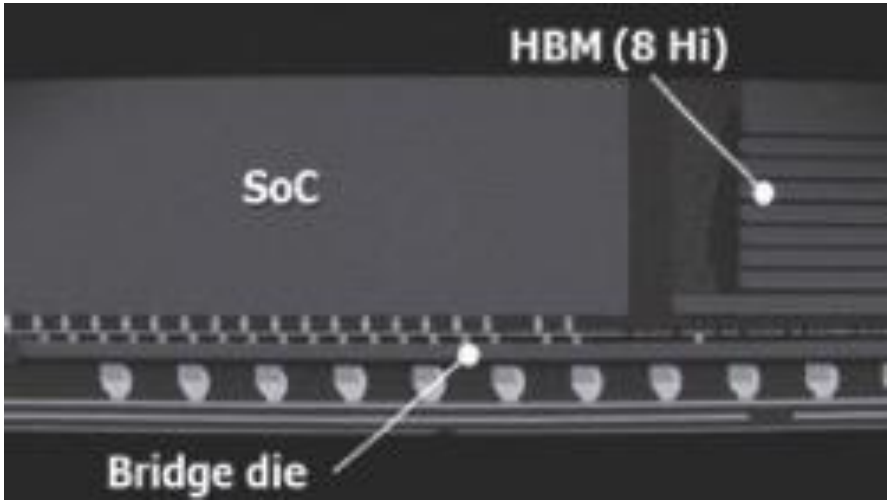


Source: ASE.

- **Less potential defects in RDL from particles because molding is after chip attach, making it more likely to have a known good substrate**
- **Good for complex packaging where die yield is a concern**
- **Good for assembly of different die heights including HBM**
- **Good for chips with lower thermal budget**
- **Some studies show less warpage than chip first process**

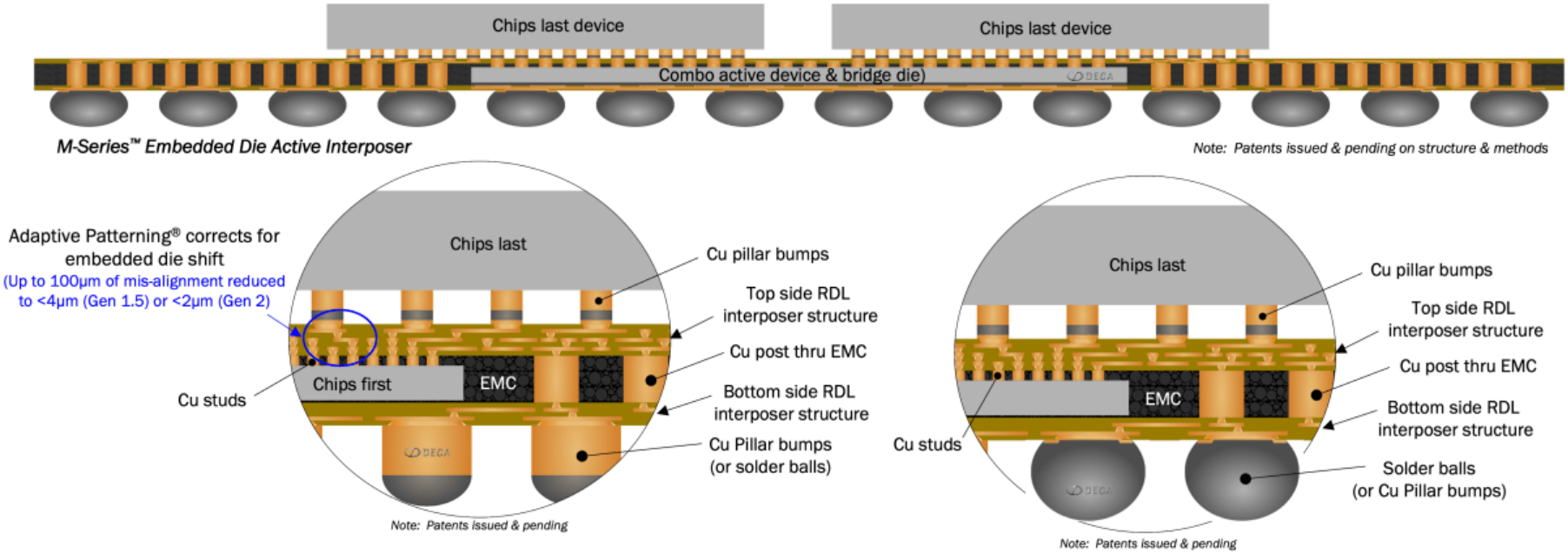
SPIL's Embedded Bridge FO with Embedded Bridge

- **Demonstrated for GPU + HBM with excellent signal integrity due to SI/PI path transmission**
- **Test vehicle with 4 silicon bridge die, 3 RDLs, Cu post connecting to form C4 bumps**
  - Bridge die with 0.8/0.8µm L/S and 40µm µbump pad pitch embedded into the organic interposer
  - RDLs with 10/10 µm L/S for power and ground and 2/2 µm L/S for signal layer
  - Bridge reduces requirement for dense RDL L/S, improves yield
- **TV size of 72mm x 72mm with a chip module size of 28mm x 45mm**
  - Chip module is attached with C4 solder bumps onto an 8/2/8 organic substrate



Source: SPIL.

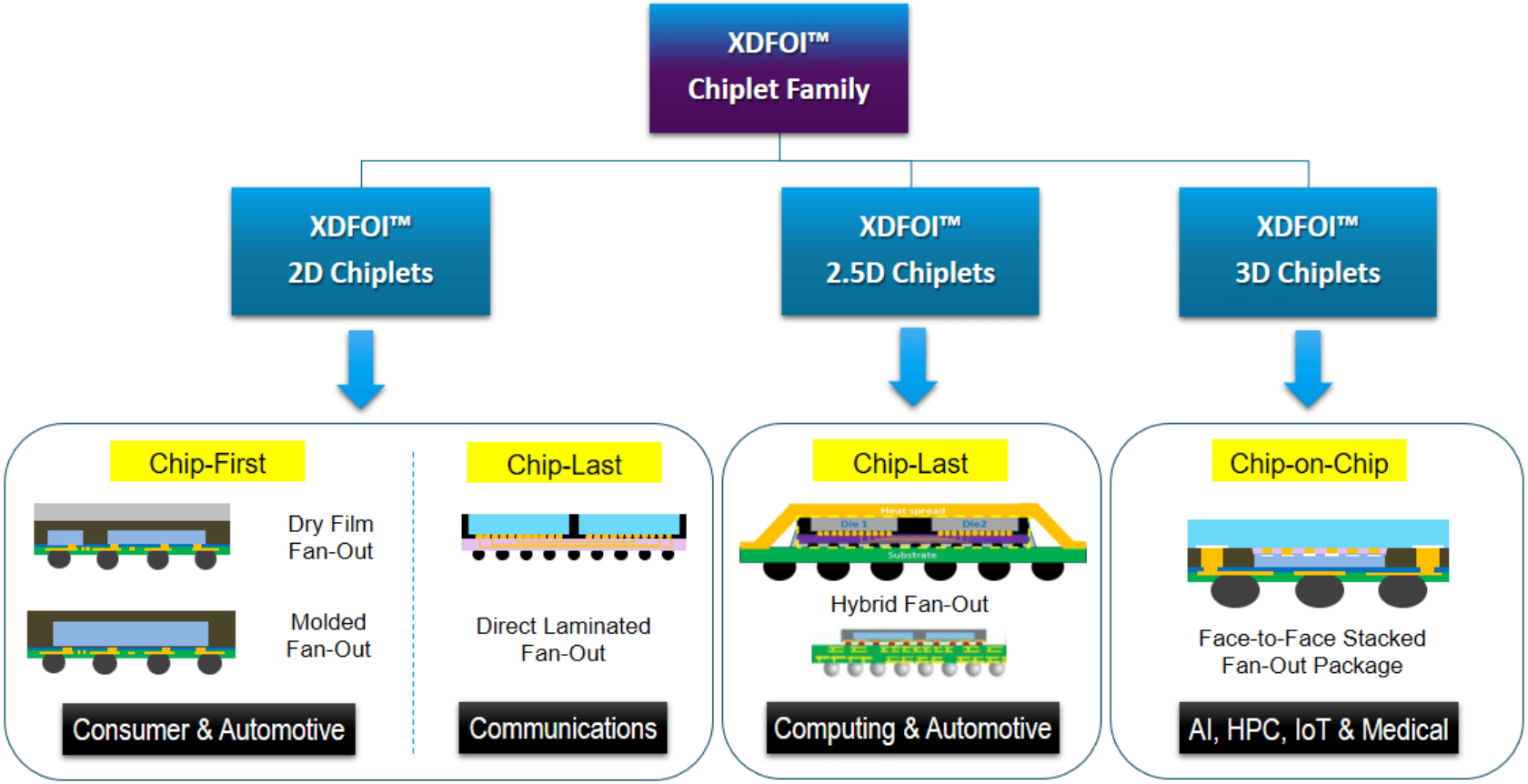
Deca M-Series Embedded Active & Bridge Interposer (Gen 1.5)



Source: Deca.

- **Deca has designed a Gen 1.5 M-Series FO with active and bridge die**
- **Adaptive patterning corrects for shift of a single or multiple bridge die**
  - Misalignment up to 100 µm can be reduce to <4 µm in Gen 1.5 or <2 µm in Gen. 2

JCET Group's XDFOI™



Source: JCET.

- **Available in chip-first or chip-last options, with chip-on-chip, face-to-face version offered**
  - 2D RDL in pilot production, 2.5D version will be ready for production line verification by Q3 2022, full 3D versions will be ready by Q1 2023
- **Targeted at AI, HPC, IoT, and medical applications**

Amkor's S-Connect Fan-out Interposer

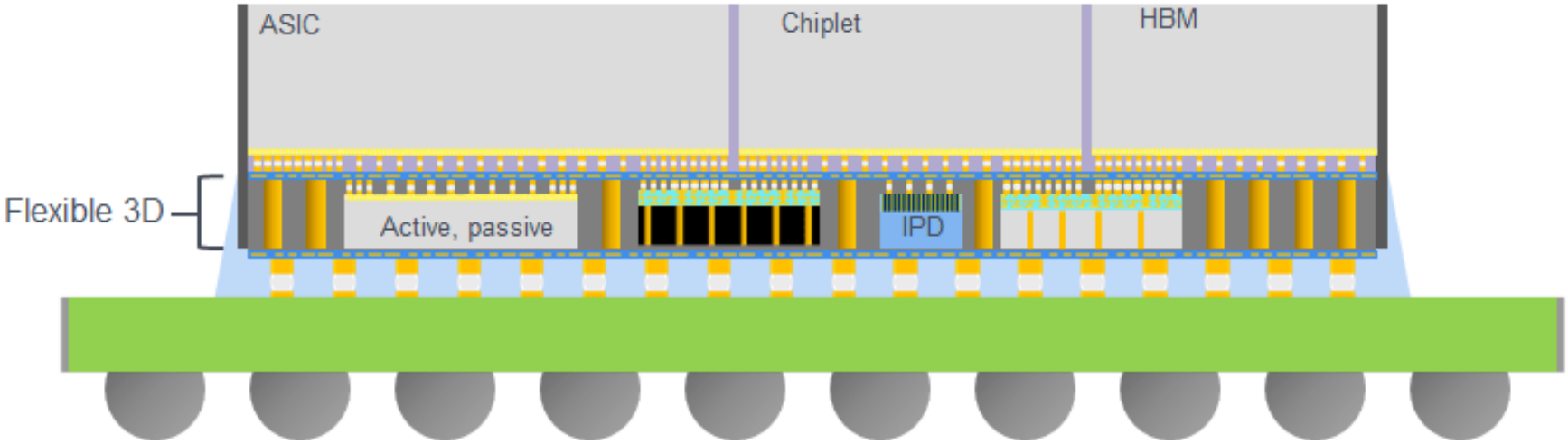
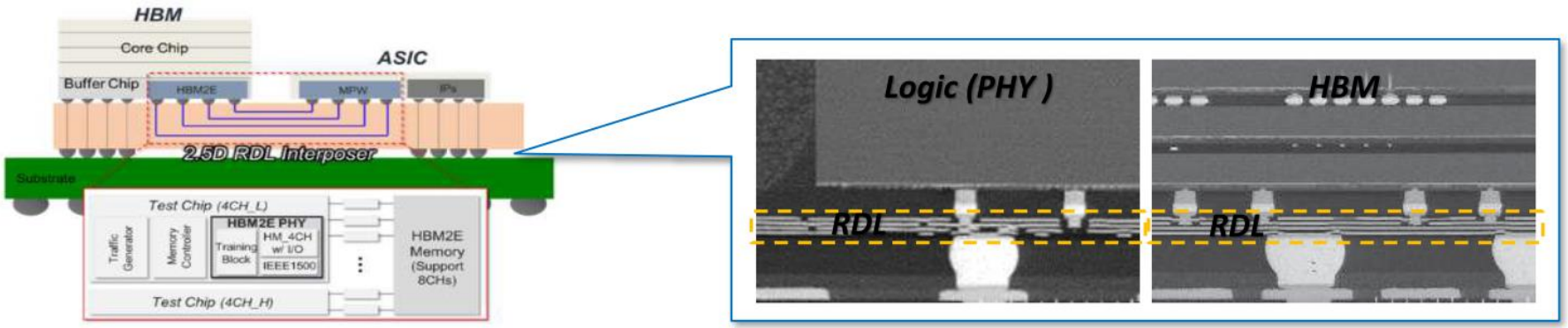


Image courtesy of Amkor Technology.

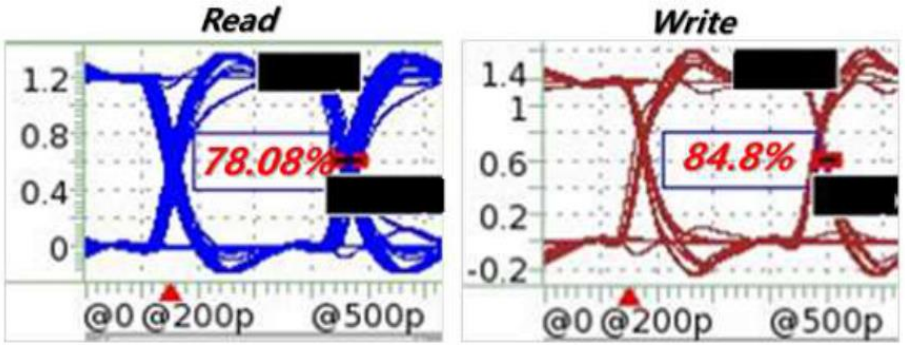
- **Amkor's first Substrate-SWIFT products are expected in Q2 2022, followed by additional products in 2023**
  - A typical product would have a 38mm x 46mm FO area, with a 52mm x 54mm the largest in development
  - Up to 4 layers of RDL are qualified and 6 layers will be qualified by the end of the year
- **Amkor offers a chip-last FO on substrate solution with an embedded bridge**
  - The use of a bridge can reduce the number of RDLs

Advantages of Samsung's R-Cube Alternative to Si Interposer



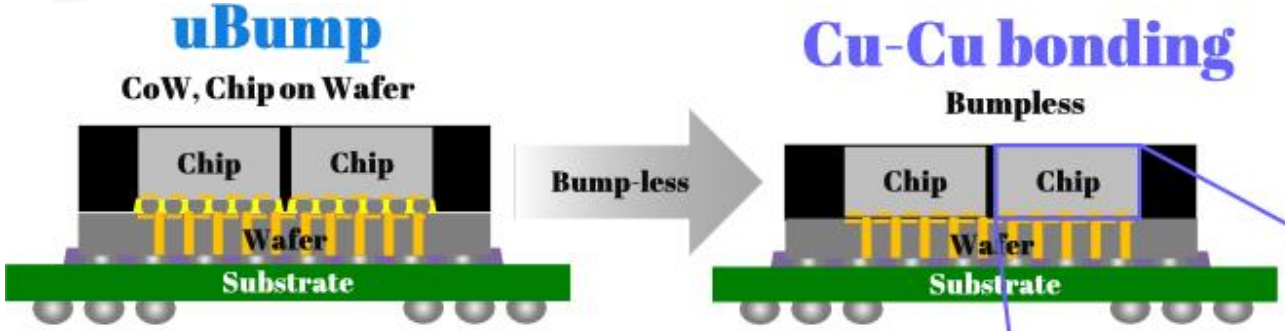
- **No Si-interposer (TSV-less)**
- **Short TAT of product development and mass production**
- **Simple assembly process flow**
- **Better electrical performance with thicker Cu RDL**
- **Standard flip chip assembly (less warpage control required)**

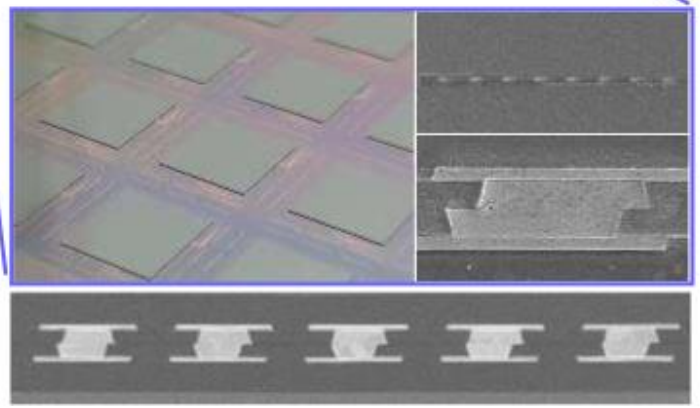
Eye diagrams of HBM2E PHY interface after optimization of RDL interposer



Source: Samsung.

Many Companies Developing Cu-Cu Hybrid Bonding



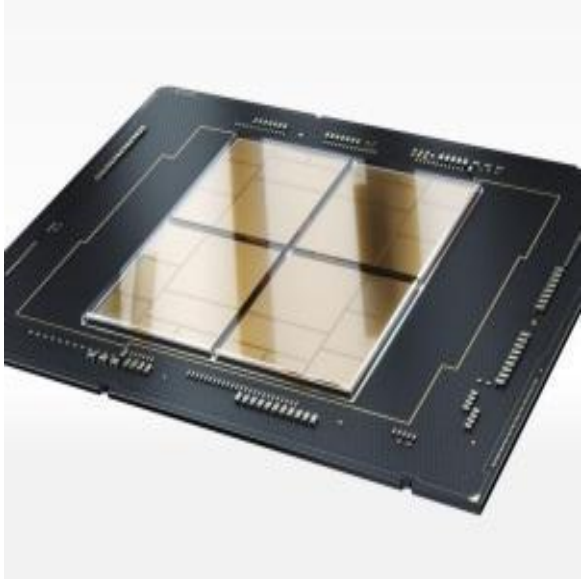


- **TSMC process moving into production with AMD's gaming product, shipping in 2022**
- **Intel, IBM, and Samsung developing a process**
- **OSATs including ASE and Amkor are investigating**
- **Challenges**
  - Cu pad surface control (use of CMP)
  - Cleanliness required (particles cause voids) = use of plasma clean and cleanroom assembly
  - Pad alignment accuracy required
  - Anneal process for bonding
  - Metrology/inspection

Source: Samsung.

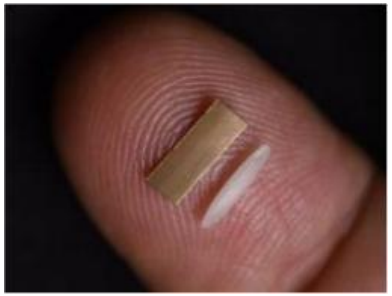
Intel's Data Center CPU with EMIB

- **Intel's Sapphire Rapids will be Intel's first CPU server for data centers using chiplets**
  - Full reticle CPU partitioned into chiplets
  - Uses Embedded Multi-die Interconnect Bridge (EMIB) technology
    - A small silicon bridge chip is embedded into the package (no TSVs) to provide in-package, high-density connection
  - All 4 chiplet die will access shared cache and are connected using the modular die fabric (MDF)
  - Any core can talk to other cores on the 4 die and access the shared cache across all 4 quadrants as well as I/O across 4 quadrants

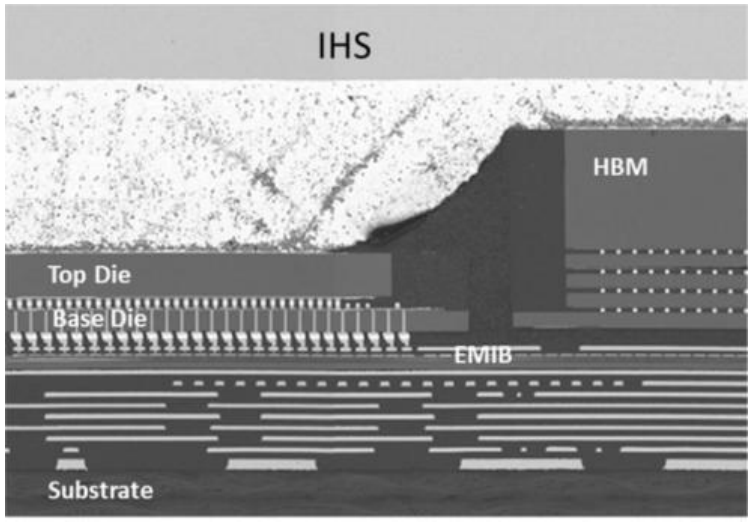


Source: Intel.

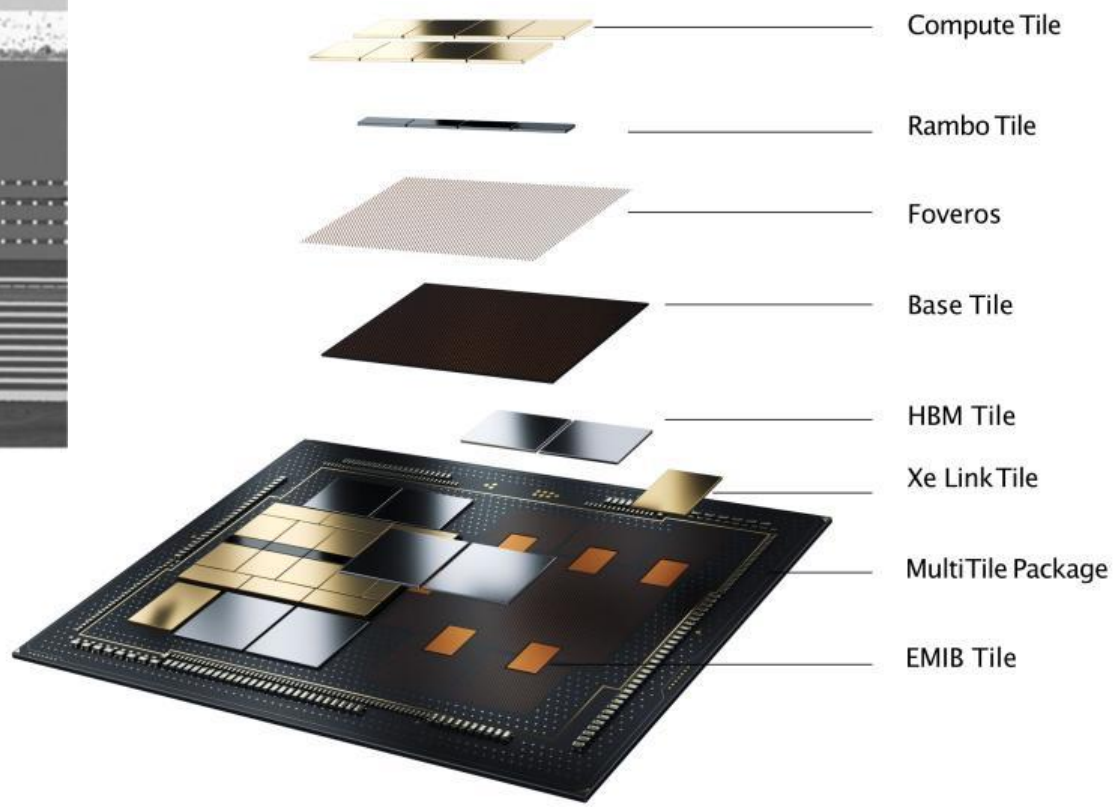
EMIB size compared to grain of Basmati rice



Intel's Co-EMIB for Ponte Vecchio



D2D pitch	36 µm
Active top die count per stack	16
Max active top die size	41 mm^2
Base die size	650 mm^2
EMIB pitch	55 µm
Core pitch (min)	100 µm
Memory (HBM)	8x
Package size	77.5 mm x 62.5 mm
EMIB count	11

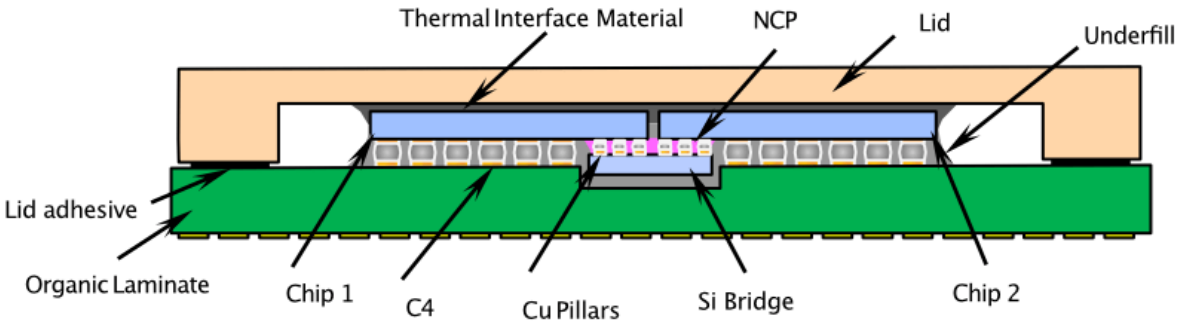


Source: Intel.

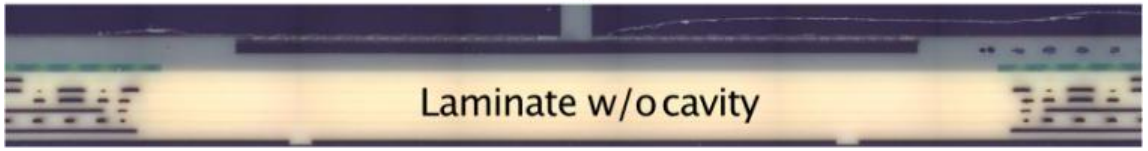
- **>100 billion transistors, 47 active tiles, 5 process nodes**
- **Up to 11 bridges may be used in production**

IBM's Si Bridge (DBHi)

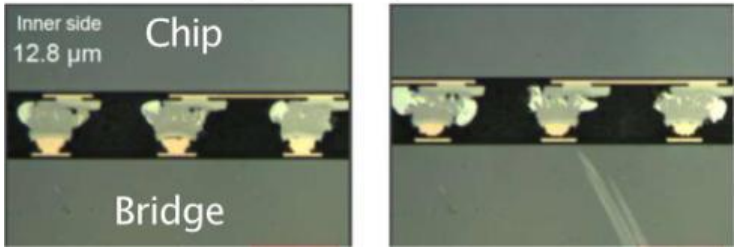
- **In IBM's current version of DBHi the chips are joined to the silicon bridge and placed in cavity of the laminate substrate**
  - Focus on eliminating the cavity in the substrate
    - Bridge chip thickness reduction
    - C4 standoff height optimization
- **Bridge ground rule scaling**
  - Interconnect wiring to sub micron
  - C4 scaling to 30 µm
  - Feasibility of hybrid bonding (sub 10µm pitch)



Laminate cavity elimination



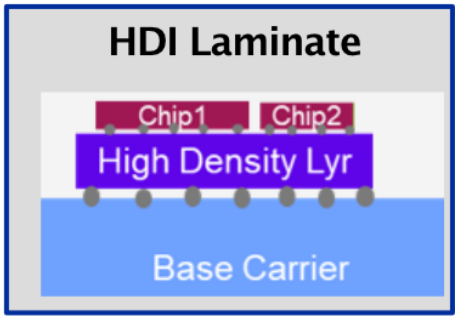
30 um pitch Cu pillar x-sections



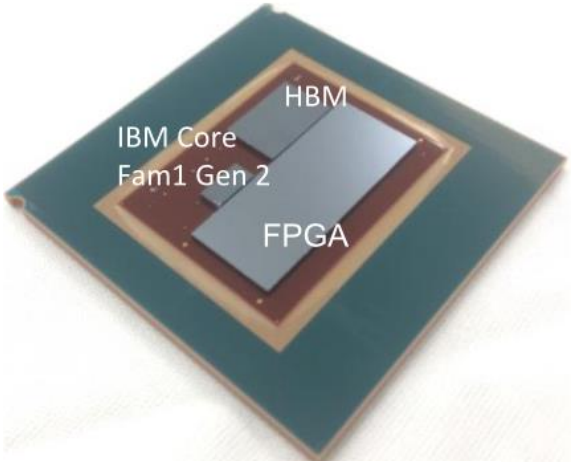
Source: IBM Research.

IBM's High Interconnect Density Scaling

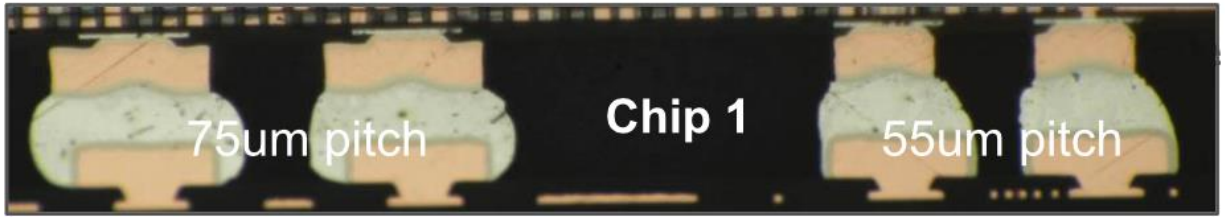
- **Drive to large body size to enable up to 9 chip module architecture**
- **Develop and assess alternative high-density wiring options**
- **Qualify reliability performance of 70mm x 70mm laminate**
- **Develop and assess organic interposer**
  - Focus on WLFO technologies
- **Qualify electrical performance**
  - Power delivery
  - Signal integrity



Functional Test Vehicle

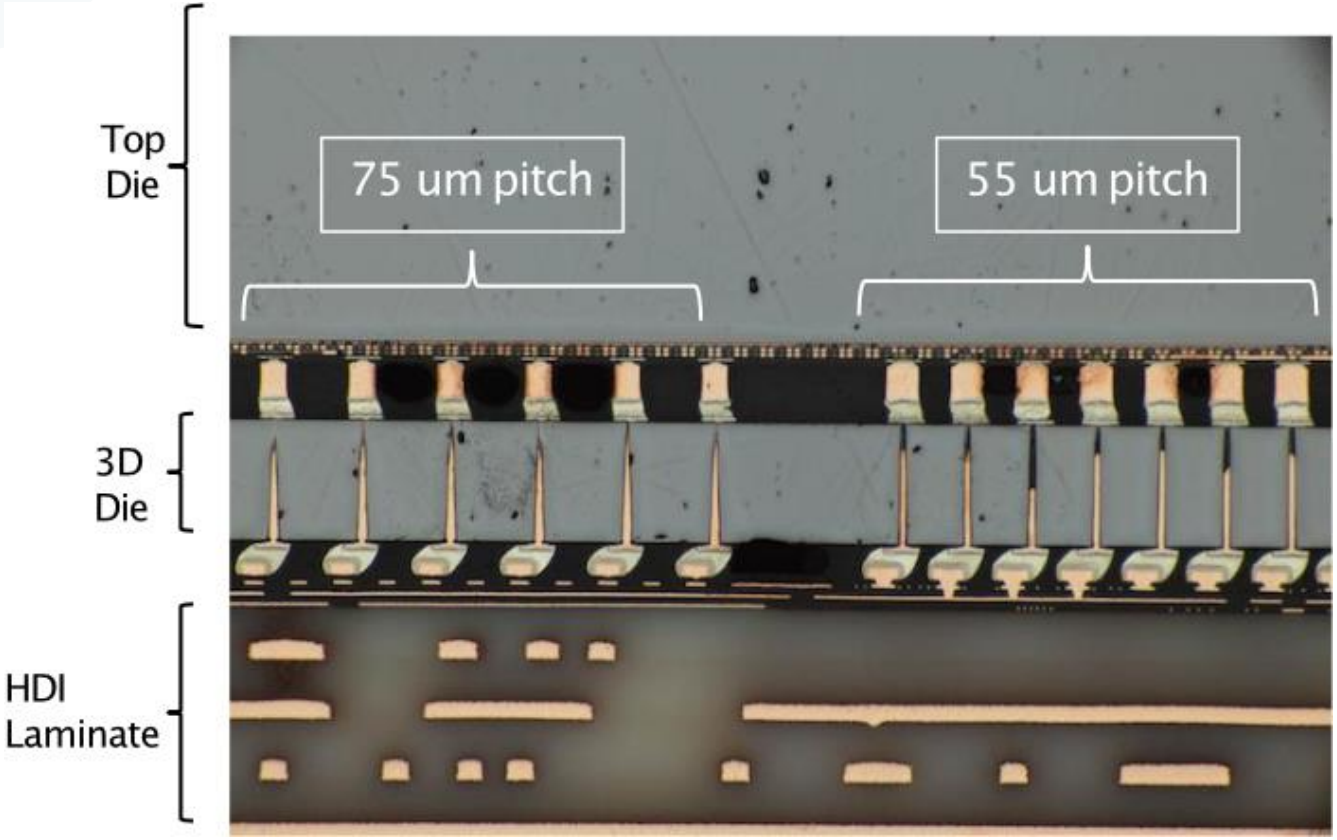


HDI Interconnect Structure



Source: IBM Research.

IBM Developing 3D Solution, Future Hybrid Bonding



Source: IBM Research.

- **3D integration with accelerator to memory configuration is under development using 3D chiplets with nanosheet logic die stacking**
  - Proximity effects with nanosheet devices
  - Reliability of 5nm and beyond BEOL stacks w/ late TSV integration
  - Working on hybrid bonding, thermal management of 3D chip stacks important
- **3D configuration placed on HDI laminate substrates**

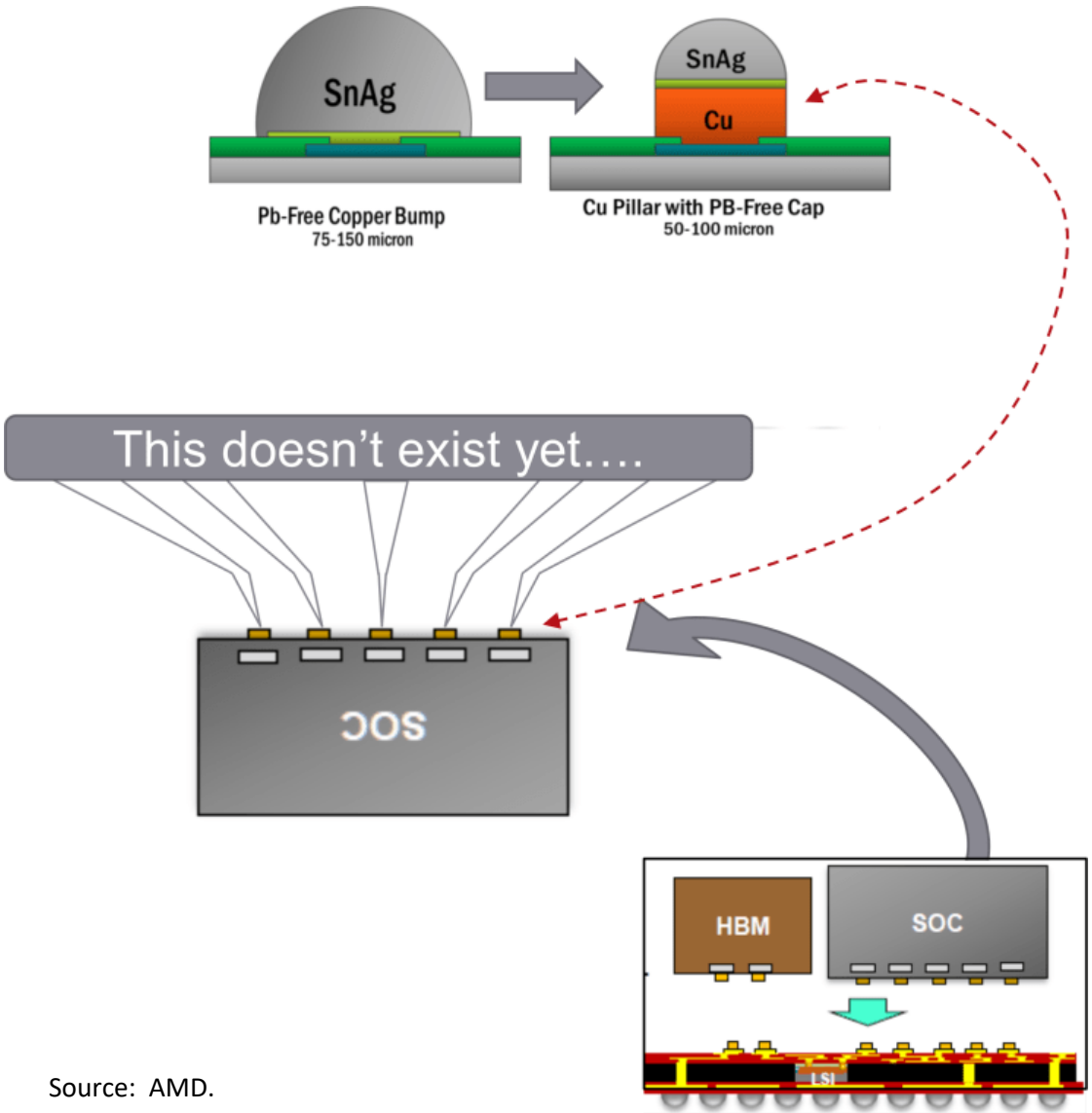
Chiplet KGD Testing

AMD Chiplet Testing Suggestions

- One faulty die could ruin entire stack (very expensive)
- Need to test functionality (at least partially) before stacking/bonding
- Challenges
  - Limited connectivity (few pads, maybe none?, only TSVs/µbumps?)
  - Limited ability to supply power
  - Incomplete functionality (issues such as PLL/clocking on a different chip)
- High cost of missing a defect
  - No rework possible on integrated chiplet packages (defect = discard package and all chiplets)
  - Wafer sort test must deliver KGD (need mission-mode testing at wafer sort, need careful selection of test points, guard bands, die matching)
    - Redundancy/repair strategy for features not tested at sort
    - Test access features for in-package testing to ensure quality

Source: AMD.

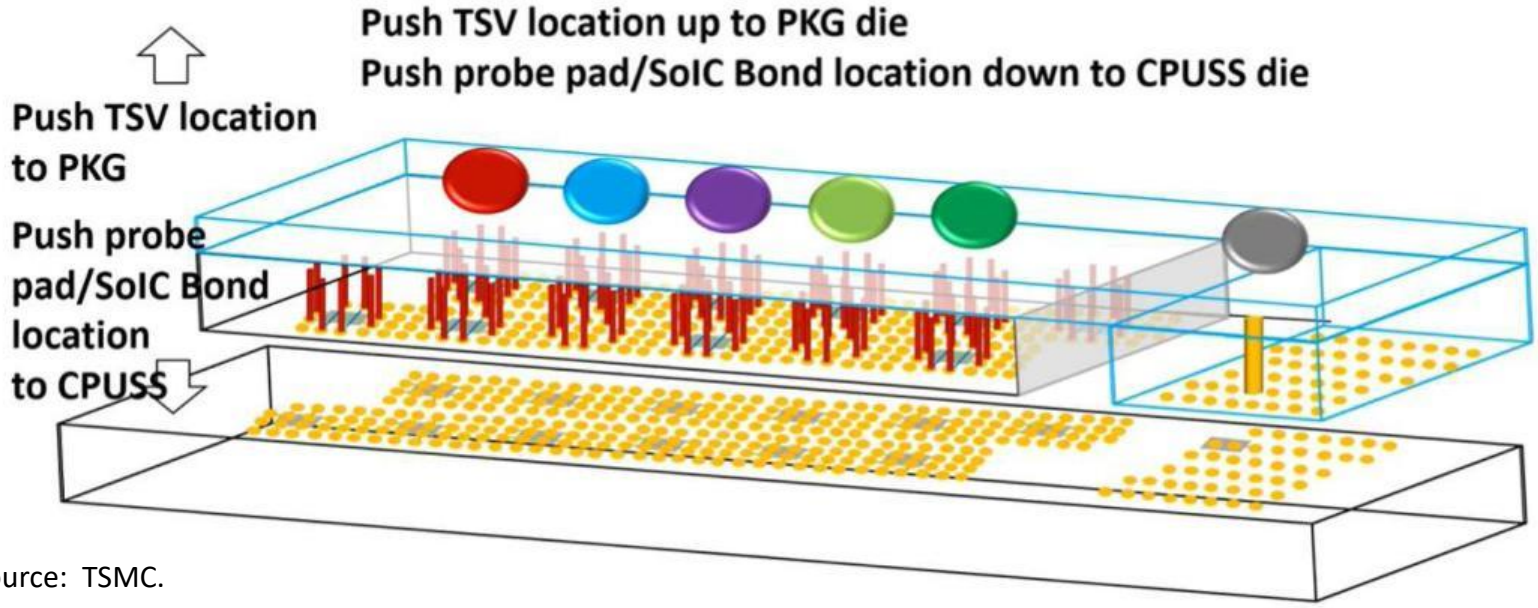
KGD: Full Probing at Wafer Sort



Source: AMD.

- **Even µbump probing is challenge for HVM**
- **Probing dense Cu pillars not feasible today**
- **Compromise: Essential sacrificial probe pads**
- **Mechanical engineering challenge**
  - Temporary, reliable contact at very fine pitch
- **Electrical engineering challenges**
  - Better interface(s) for tester access (including power delivery)
  - Self-testing functional interfaces that don't need probing
  - Redundancy/repair

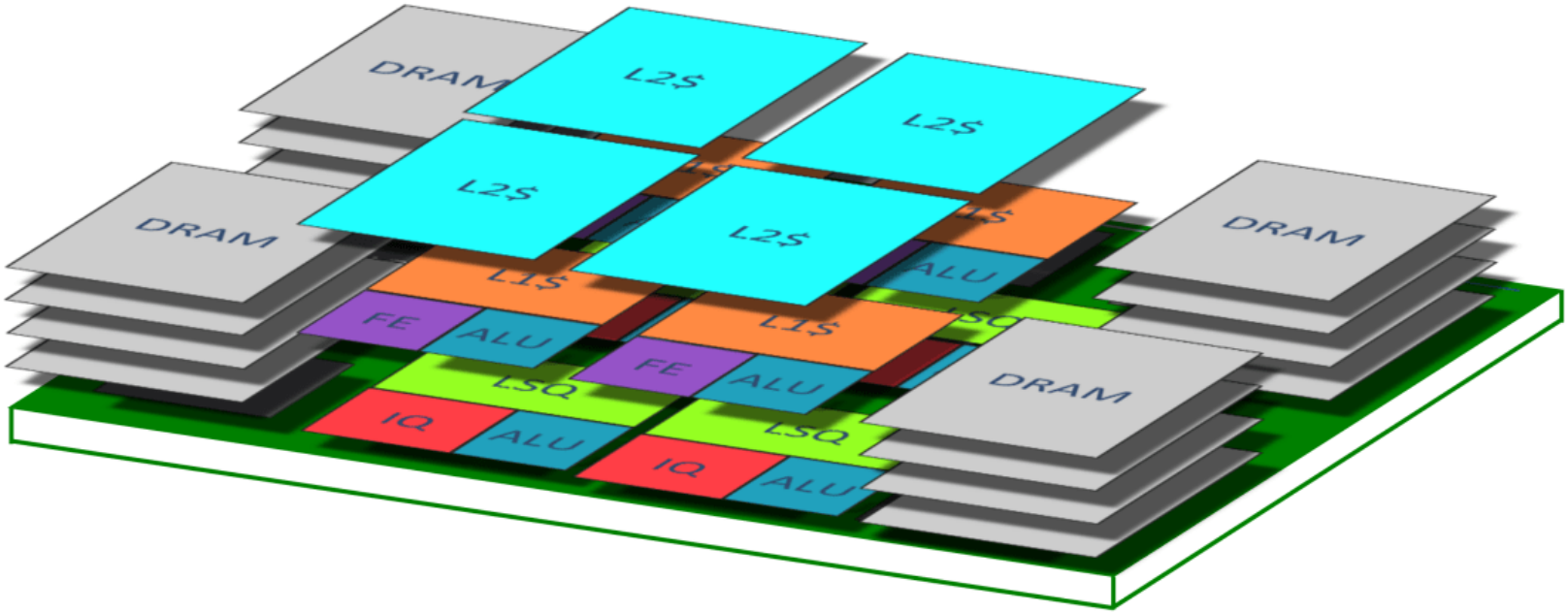
Determining Probe Pad Locations for SoIC



Source: TSMC.

- **Power domain for both dies can be shared, CPUSS die only power domains can't be shared with SRAMSS**
- **Need to map I/O location to probe pad, place dummy SoIC bond**
- **Swap dummy SoIC bond to active SoIC bond, assign net on it based on the nearest probe pad**
- **Grow TSV on active SoIC bond**
- **Push TSV location up to package die, push probe pad/SoIC bond location down to CPUSS die**
- **Push TSV location to package and push probe/pad SoIC bond to CPUSS**

Test Scalability

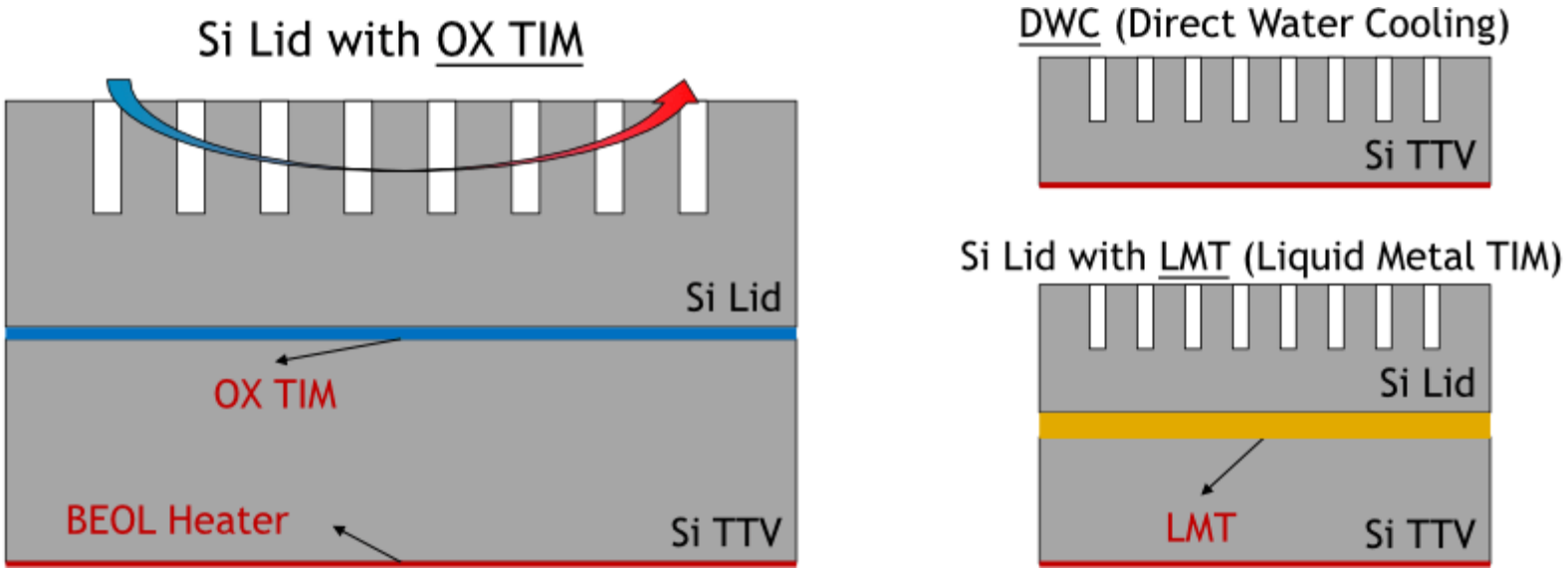


Source: AMD.

~~PC Board~~ -> Package

- **AMD says there is as much silicon in a multi-die package as there was on an entire PCB 10 years ago**
  - Many more transistors, much more functionality, higher quality requirements, in-field test expectations
  - Chiplet testing must scale accordingly (maybe post burn-in test)
  - Package test and system-level test blur (extend to field)

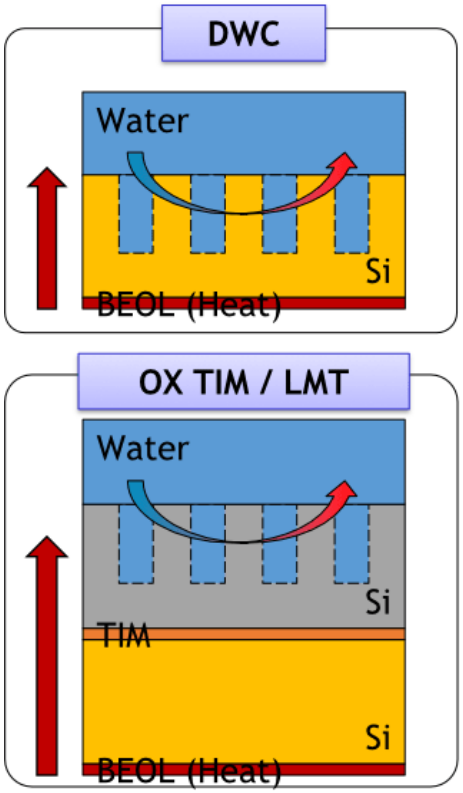
TSMC's Integrated Si Micro-Cooler (ISMC)

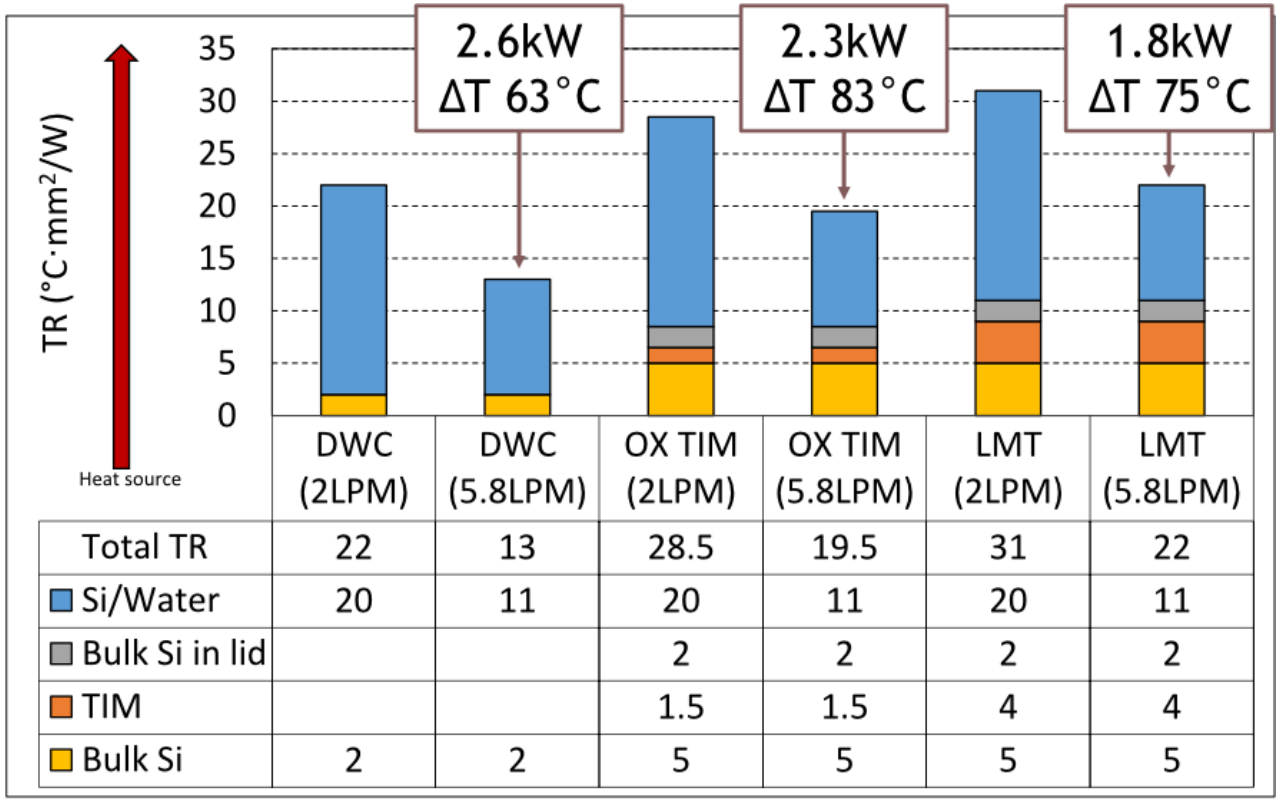


Source: TSMC.

- **Silicon lid with microstructures replaces a Cu lid**
- **Allows liquid coolant to get closer to the heat source**
- **Metal TIM replaced by thin SiOx bonding interface (OX TIM) formed by fusion bonding between the Si lid and the chip**

TSMC's Integrated Si Micro-Cooler (ISMC) Performance



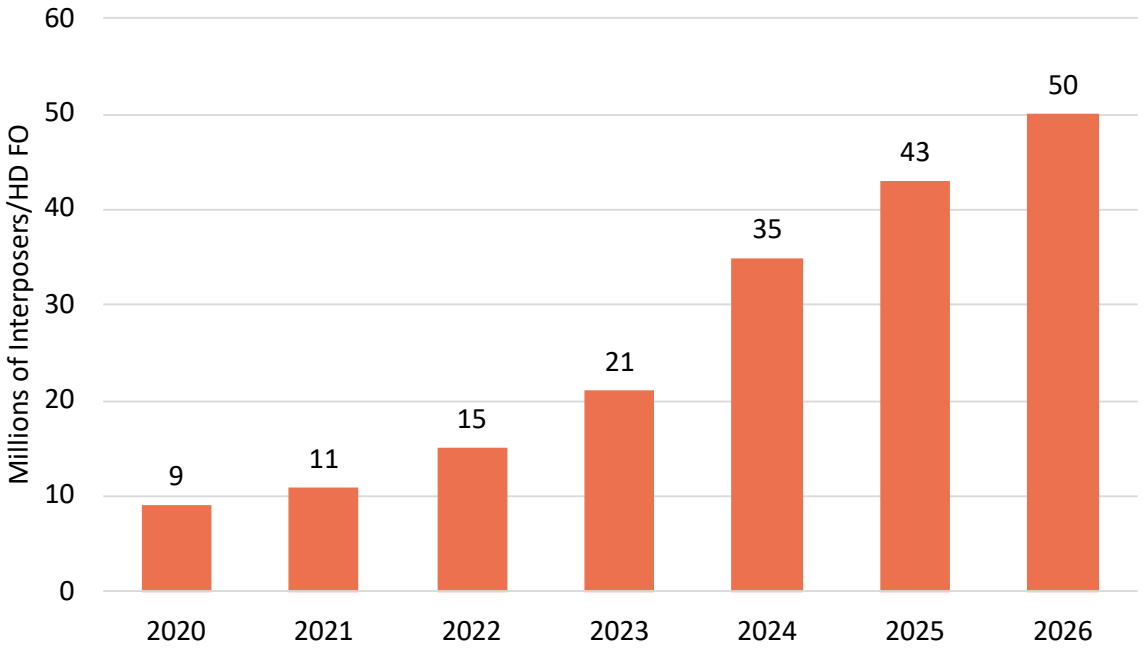


	DWC (2LPM)	DWC (5.8LPM)	OX TIM (2LPM)	OX TIM (5.8LPM)	LMT (2LPM)	LMT (5.8LPM)
Total TR	22	13	28.5	19.5	31	22
Si/Water	20	11	20	11	20	11
Bulk Si in lid			2	2	2	2
TIM			1.5	1.5	4	4
Bulk Si	2	2	5	5	5	5

Source: TSMC.

- **TSMC's performance results with ISMC**

Market Projections for Si Interposers and HD FO



	2020	2021	2022	2023	2024	2025	2026
Interposers/HD FO (millions of units)	9	11	15	21	35	43	50
Thousands of 300mm wafers	173	228	382	539	832	1,061	1,312

Source: TechSearch International, Inc.

- **Applications include FPGAs, CPUs, GPUs, and ASICs for AI accelerators, servers, graphics and other high-performance applications, excluding mobile**
  - Forecast counts FO on Substrate using a carrier wafer + silicon interposers
  - EMIB and other embedded laminate substrates are not included

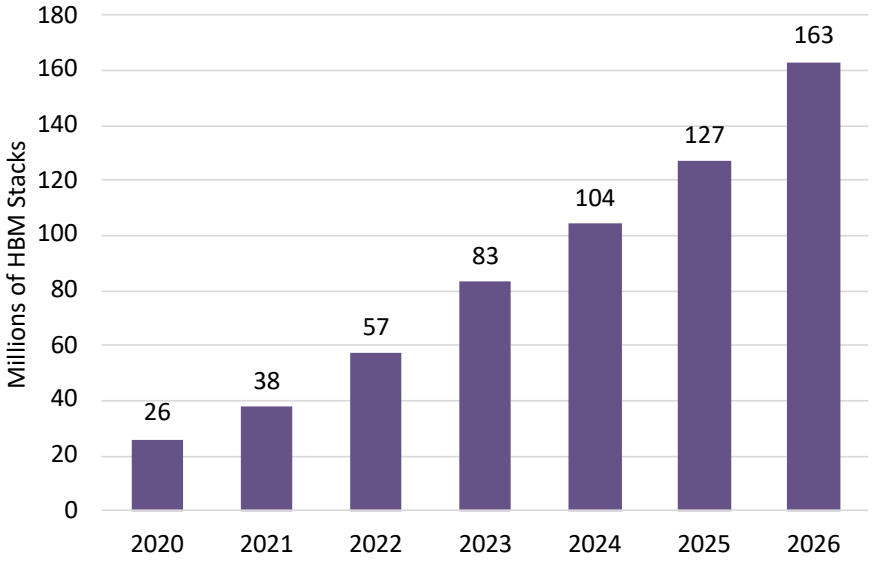
Suppliers of Si Interposers

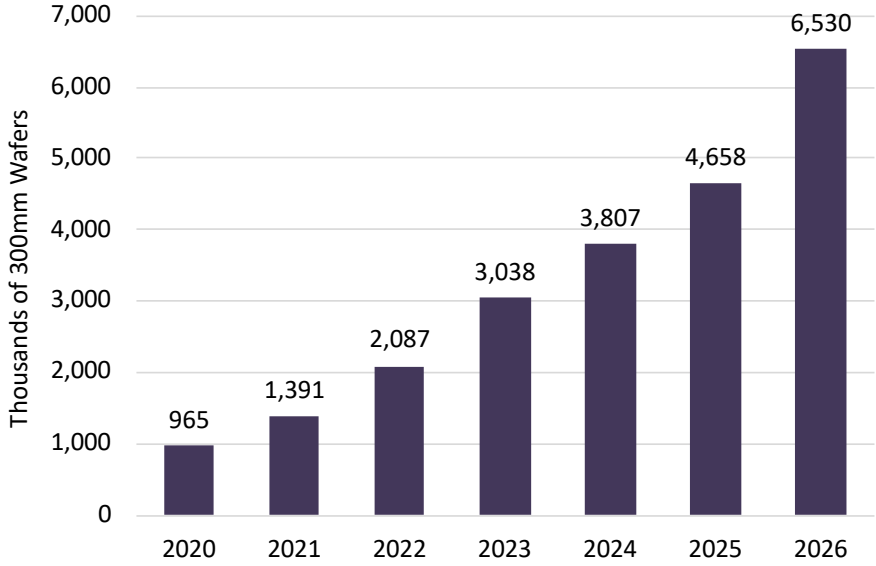
Company	Wafer Size	Status
Fraunhofer (Germany)	300 mm	Pilot line
GINTEC (Japan)	200 mm, 300 mm	Small volume
GLOBALFOUNDRIES (U.S.)	300 mm	Production
Micross (U.S.)	200 mm	Small volume
Samsung (S. Korea)	300 mm	Production for foundry customers
Skorpios Technologies (U.S.)	200 mm	Production
SkyWater (U.S.)	200 mm	Future production
TSMC (Taiwan)	300 mm	Production for foundry customers
UMC (Taiwan)	300 mm	Production

Source: TechSearch International, Inc.

- **Samsung and TSMC supply Si interposers to foundry customers only**
- **TSMC accounts for the majority of the market**

HBM Market Projections





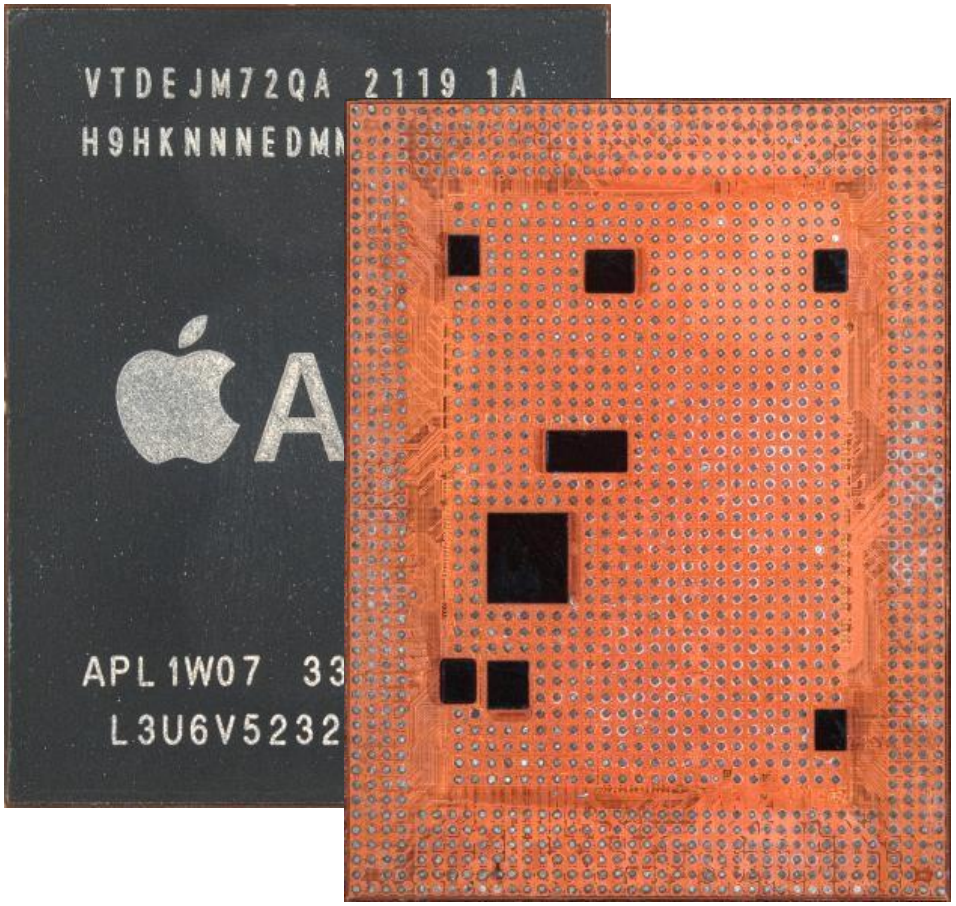
Source: TechSearch International, Inc.

- **HBM is offered by Samsung, SK Hynix, and Micron with internal production**
  - Renesas offers a low-latency HBM assembled by an OSAT
- **HBM2e is in volume production for AI machine learning**
- **SK Hynix is expected to introduce HBM3 in 2023, target applications include data centers, AI machine learning, and supercomputers**
  - Expected to be 11mm x 11mm with more fine pitch bumps than HBM2e
  - Products include 16 GB and 24 GB, with the 24 GB in a 12-die stack, each DRAM is thinned to 30 µm

Advanced Packages for Mobile Devices

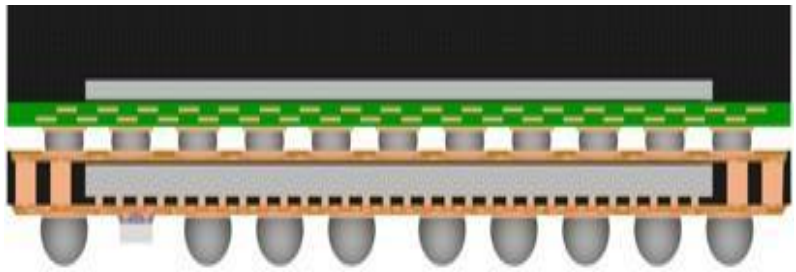
Characteristics of A15 Bionic PoP and Comparison with A14

- **Size: 17.0 mm x 12.8 mm**
  - 15.7% larger than A14
- **Height: 0.86 mm (PoP), 0.38 mm (A15 only)**
  - Same as for A14
- **Contacts: 1,521 solder balls at 0.31mm pitch**
  - 33% more balls than A14
  - Slightly tighter pitch than 0.32mm on A14
- **InFO RDLs: 3 layers with 8/8 min. L/S**
  - Same as for A14
- **TSMC process: N5P**
  - 2nd-generation 5nm
  - A14 used 1st-gen N5 process



M-Series 3D PoP

- Deca has developed M-Series PoP structure design rules
- Multi-layer front & back side RDL (up to 4 layers each)
- Through-mold 3D interconnect on 150µm pitch

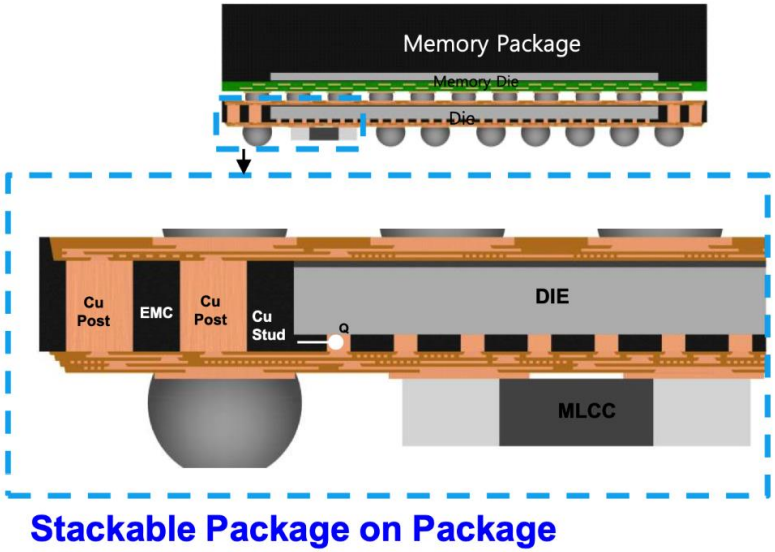


3D PoP - Mobile Applications Processor

- Adaptive patterning utilized for M-Series to enable 45µm bond pad pitch
- 5µm line and space RDL
- Process flow defined for overall structure including multiple passive integration options
- Full array memory BGA package mounted on top of M-Series

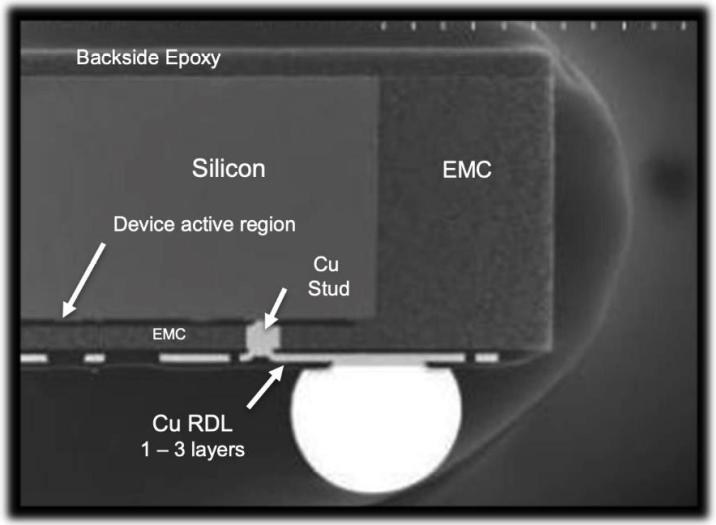
Nepes mPoP M-Series Stackable Package-on-Package

***m*PoP**(M-Series stackable Package on Package)



Stackable Package on Package

Standard M-Series (non-stackable package)

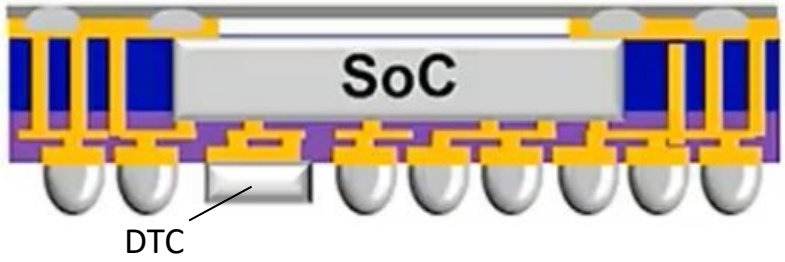


Source: Nepes.

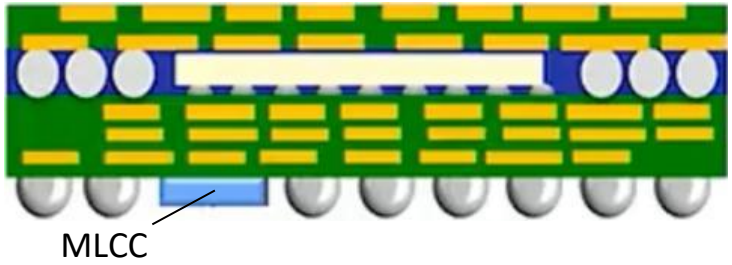
- **Nepes mPoP is based on Deca's M-Series technology**
- **mPoP is a stackable structure provides a competitive integration solution of application process (AP) and memory device**

TSMC InFO_B (Bottom Only) for Mobile AP

InFO_B



FC-CSP



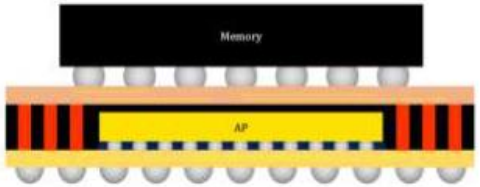
Attribute	InFO_B	FC-CSP
CPU voltage drop decrease	1.06X	1X
Max chip size (mm^2)	135	115
CPI sensitivity	Low	High
TIV/TMC pitch (µm)	180	~270

Source: TSMC.

- **InFO Bottom only (InFO_B) allows the use of any memory supplier's top package assembled at board-level assembly**
  - Possible to use TSMC's DTC with InFO_B

Samsung Developing FO-WLP (300mm) for Mobile AP

FO-WLP (Wafer Level PKG)



High performance (Thermal, Electrical) and Thin Profile Solution for Mobile Products

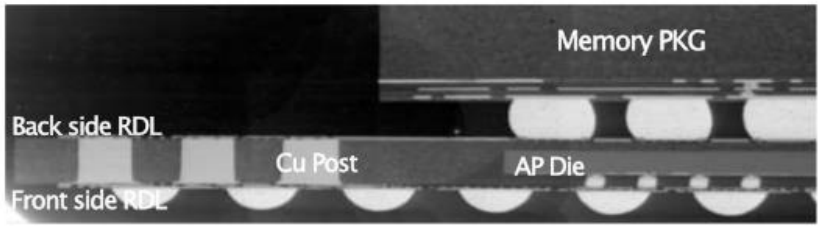
Items	Key Technology
Frontside RDL	3-Cu RDL layers with min. 2/2 LS fine pattern
Warpage Control	Well controlled warpage with optimized material set
Backside RDL	Low Temperature Multi-layer backside RDL

Qualified Functional Test Vehicles

. Fully Qualified with 10nm functional device of mobile AP
. PKG Size : 13.4 x 14.9mm
. PKG Height : 0.38mmt (Ball Height 0.08mm)
. RDL : Front-side RDL 3 Layer, Back-side RDL 2 Layer
. Cu Post : Pitch 0.35mm, Height 0.185mm
. Optimized PKG warpage : -18um@R.T, -27um@250°C

PKG Bottom View

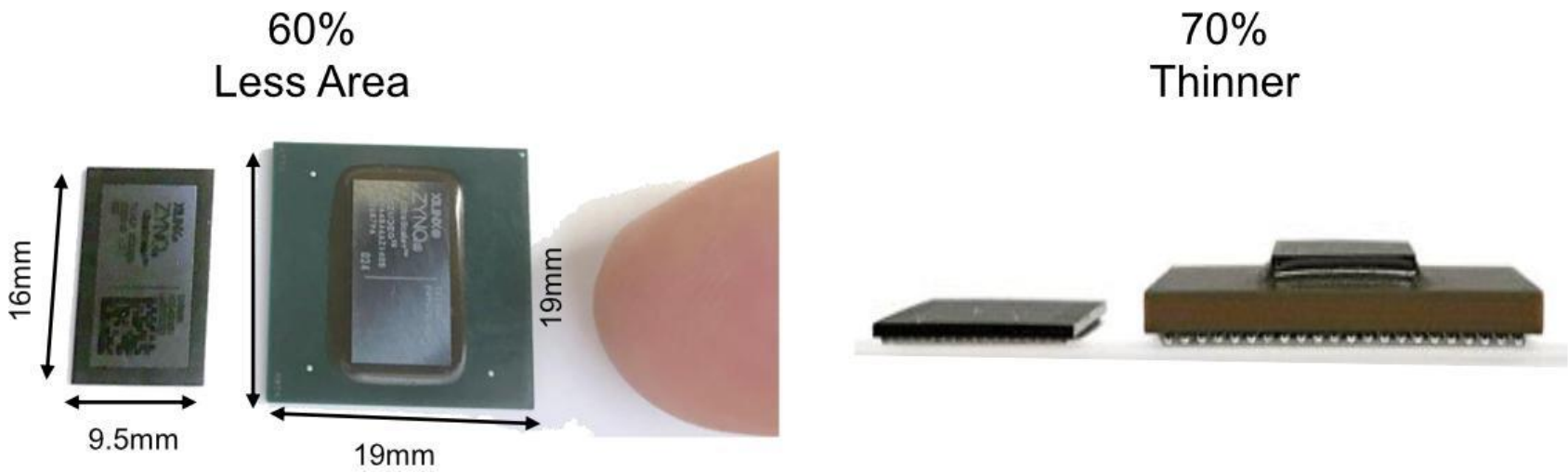
PKG Top View



Source: Samsung.

- **FO-WLP (chip last) will be introduced in next 1-2 years for 3nm node processors**
- **Application processor with Cu pillar in molded RDL**

Xilinx Zynq UltraScale+ MPSoC in InFO Package



Source: Xilinx.

- **With the substrate shortage, some companies are looking to use FO-WLP**
  - No substrate is required for a FO-WLP with a small body size
- **Xilinx is expected to increasingly use FO-WLP for its Zynq family of products**

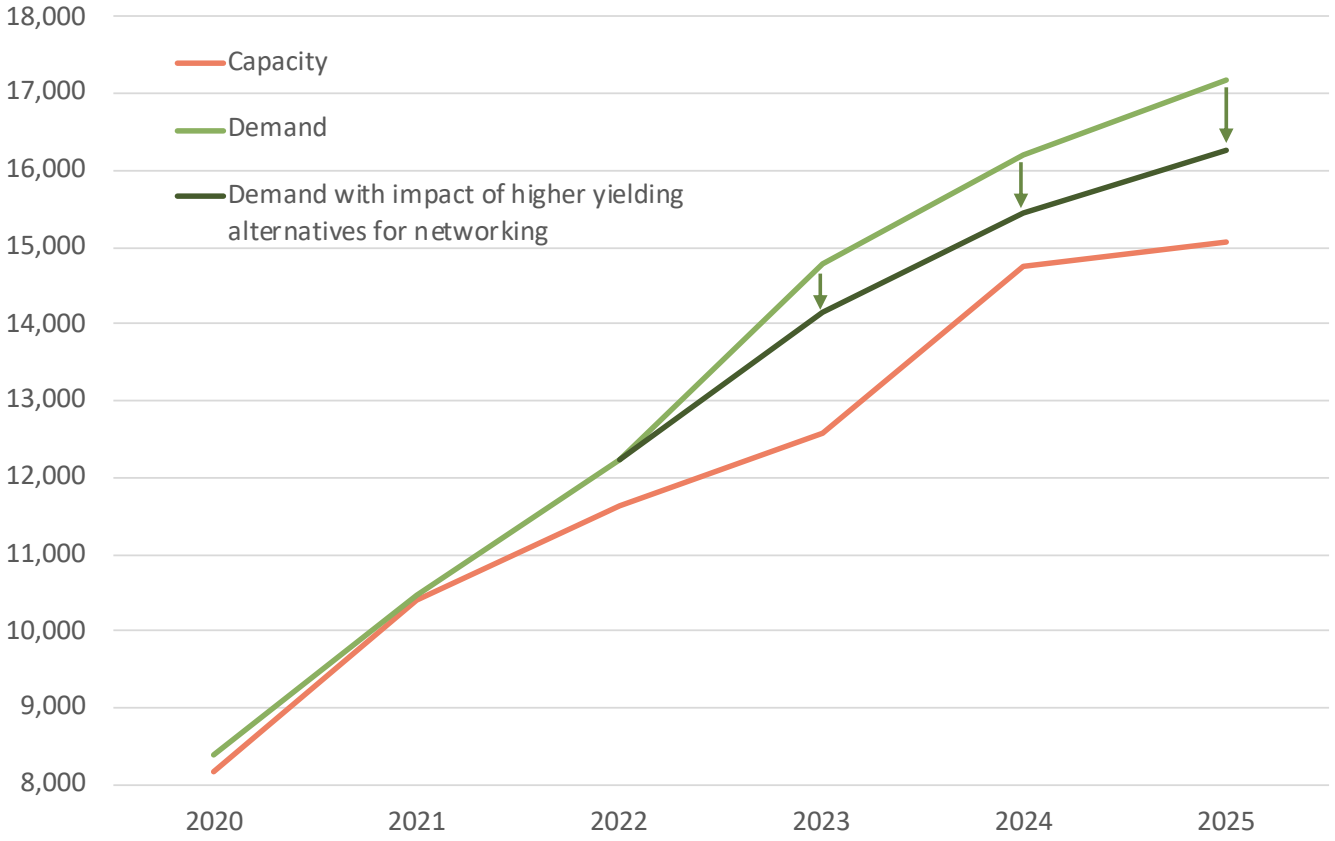
FC-BGA Substrate Supply and Demand

	2020	2021	2022	2023	2024	2025
Capacity (thousands of square meters)	8,150	10,405	11,646	12,575	14,748	15,080
Demand (thousands of square meters)	8,381	10,468	12,237	14,793	16,213	17,163

Source: TechSearch International, Inc.

- **Capacity will be expanded, but demand driven by larger body sizes and higher layer counts still outstrips the added capacity**
  - Major players investing in capacity expansions will have access, smaller players still suffer
- **Earlier this year build-up capacity expansion plans were announced by AT&S, Ibiden, Kinsus, Kyocera, Nan Ya PCB, SEMCO, Toppan, and Unimicron**
  - Ibiden will tear down the existing Gama plant and bring new capacity online in 2026
  - Domestic China suppliers such as Shennan Circuit (SCC) and PCB maker ZDT (Avery) also plan build-up substrate production
- **Recent FC-BGA build-up substrate capacity announcements from SEMCO and Shinko Electric promise to add additional capacity**
  - SEMCO will convert an RF module plant in Vietnam to FC-BGA, capacity will be online starting in mid-2023 with much of the capacity dedicated to a single customer
  - Shinko Electric has announced a $1.4 billion expansion plan that will add capacity as early as 2024, specifically targeted for a specific customer

FC-BGA Substrate Supply and Demand



Source: TechSearch International, Inc.

- **Assuming no increase in the body size for graphics or ASIC packages, and assuming alternative substrate technologies with higher yields can be developed, demand will still exceed capacity, but the gap closes**