A stackable cross point phase change memory

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Abstract

A novel scalable and stackable nonvolatile memory technology suitable for building fast and dense memory devices is discussed. The memory cell is built by layering a storage element and a selector. The storage element is a Phase Change Memory (PCM) cell [1] and the selector is an Ovonic Threshold Switch (OTS) [2]. The vertically integrated memory cell of one PCM and one OTS (PCMS) is embedded in a true cross point array. Arrays are stacked on top of CMOS circuits for decoding, sensing and logic functions. A RESET speed of 9 nsec and endurance of 10^6 cycles are achieved. One volt of dynamic range delineating SET vs. RESET is also demonstrated.

Introduction

PCM arrays with different selectors have been disclosed. In a 0T1R configuration [3], the small read and write windows pose a severe limitation to the size of the array. In a 1T1R configuration [4], the paired MOS selector limits the layout at $8\lambda^2$ or higher. Using a crystalline bipolar selector [5, 6], cell sizes could approach ~$5\lambda^2$; however, decoding and selecting CMOS circuits share the substrate with silicon selectors, resulting in reduced array efficiency. Recent advances in thin film diode technology improve layout efficiency and stack-ability [7] but the on-off ratio of the thin film selectors will limit the size of each array partition. In this work, a thin-film two-terminal Ovonic Threshold Switch is deployed as the selector of a memory cell. The symmetrical blocking or triggering voltage, a.k.a. the threshold voltage, of the amorphous alloy [8] provides the base for a robust inhibiting scheme to isolate individual PCM cells in the cross point array. OTS shares the matched physical and electrical properties for PCM scaling. Given the compatibility of thin-film PCMS with mainstream metallization schemes, multiple layers of cross point memory arrays are feasible. Also, this back-end technology is fully stackable over CMOS circuits to achieve excellent array-efficiency and reduced die size.

The Memory Cell

The physical construction of a memory cell is shown in Fig. 1. The vertical stack of a PCMS cell consists of a top electrode connecting to a column metal, an OTS and a PCM interlinked by a middle electrode, and a bottom electrode connecting to a row metal. The IV characteristics are shown in Fig. 2. SET and RESET states are delineated by the threshold voltages.

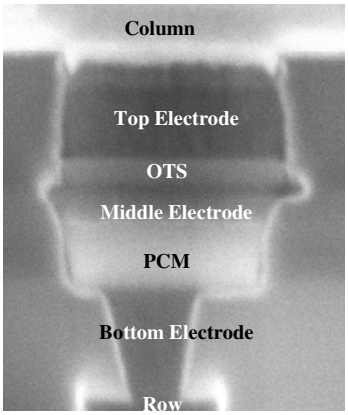

Fig. 1. SEM cross section of a PCMS cell.

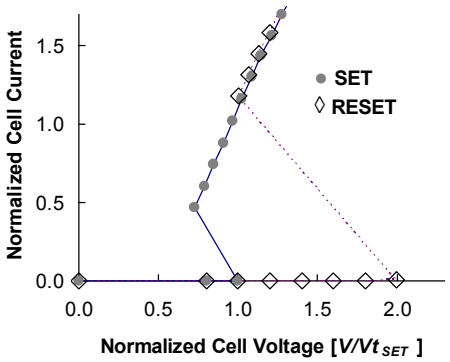

Fig. 2. The I-V Characteristics of a PCMS cell in SET and RESET. Voltage is normalized to the threshold voltage of the SET state, Vt_{set}. Cell current is normalized to melting current, I_{melt}, the least current required to amorphize the material. (see Fig. 4)