2021 International Symposium on VLSI Technology, System and Application
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The Pursuit of Atomistic Switching and Cross Point Memory

DerChang Kau
Intel Corporation

Outline

- Introduction
- Problem Statement and Solution Space
- Cross Point Memory Array and Choices of Selector
- 3D XPoint Memory Technology
- Conclusion

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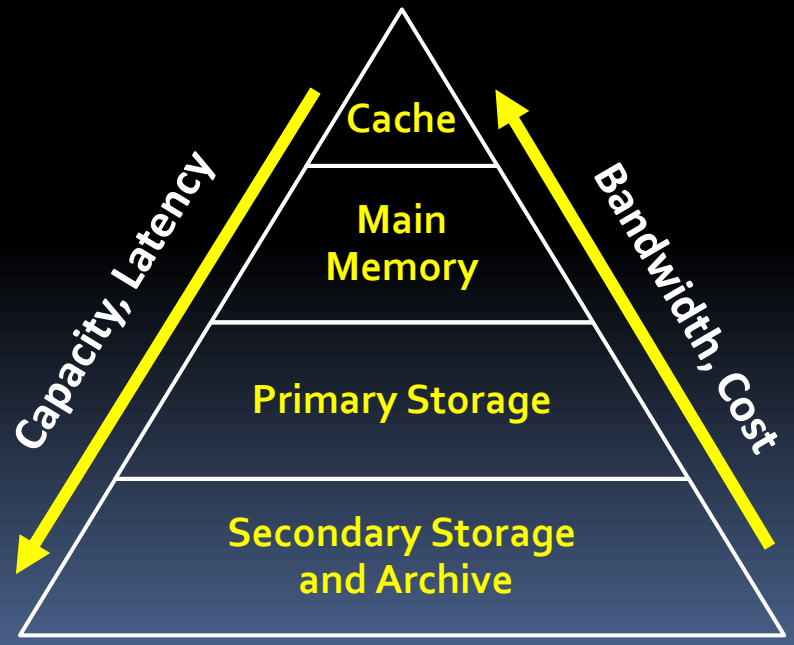
Computer Architecture 101: Hierarchy of Memory

each has greater capacity than the preceding but less quickly accessible

> ***"The Memory Organ –*** *Ideally one would desire an* ***indefinitely large memory capacity*** *such that any particular … **word** would be **immediately** … available. … It does not seem possible physically to achieve such a capacity. …We are therefore forced to recognize the possibility of constructing a **hierarchy of memories**, each of which has greater capacity than the preceding but which is less quickly accessible."*

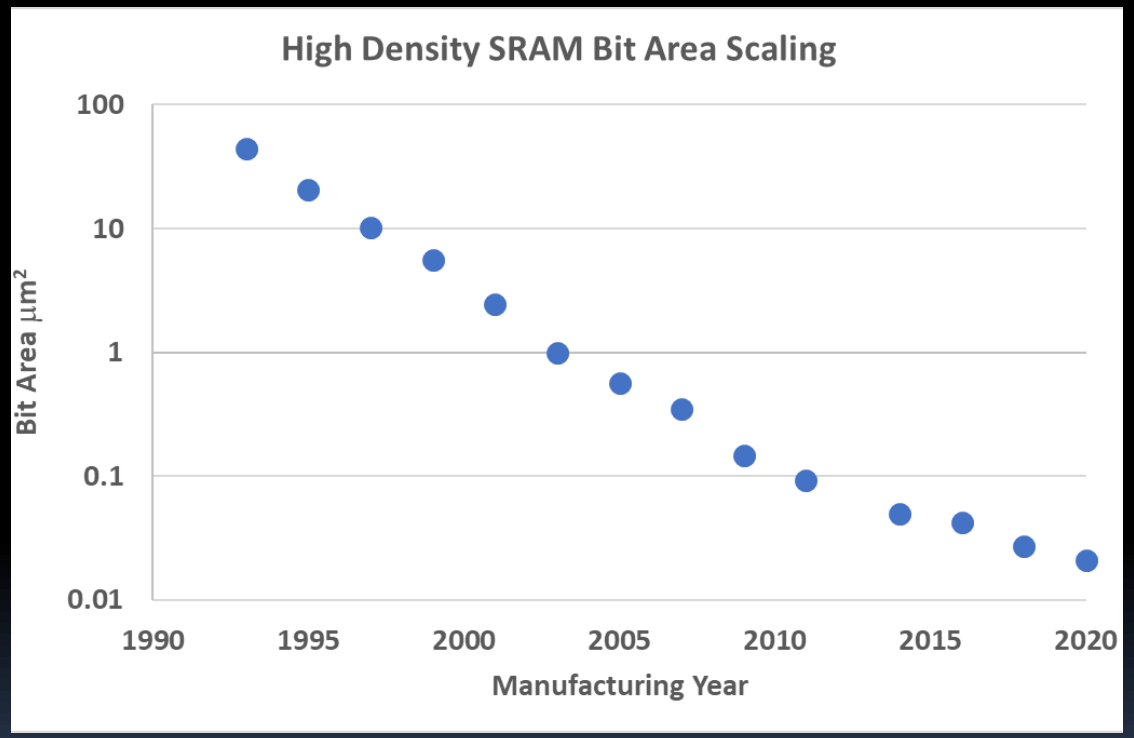
Preliminary Discussion of the Logical Design of an Electronic Computing Instrument

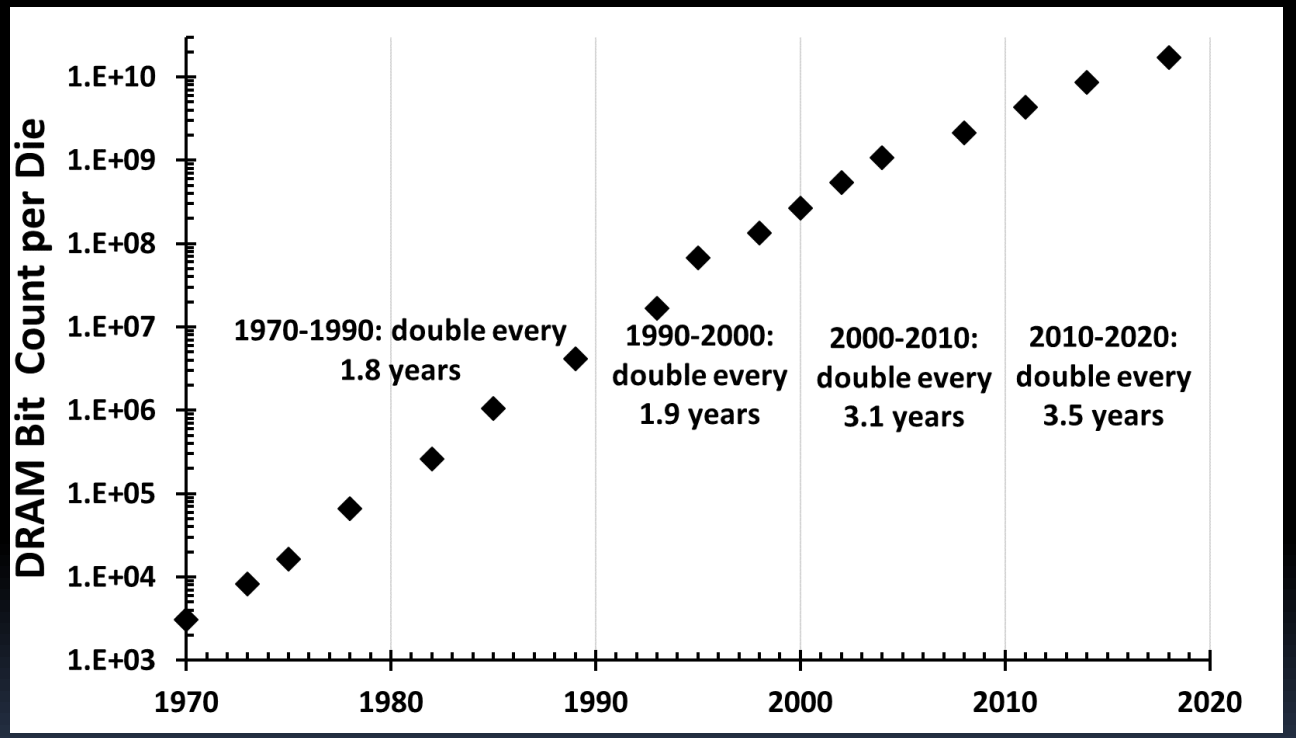
Arthur Burks, Herman Goldstine and John von Neumann, June/28/1946



Cache and Main Memory Scaling

SRAM and DRAM scaling have significantly slowed



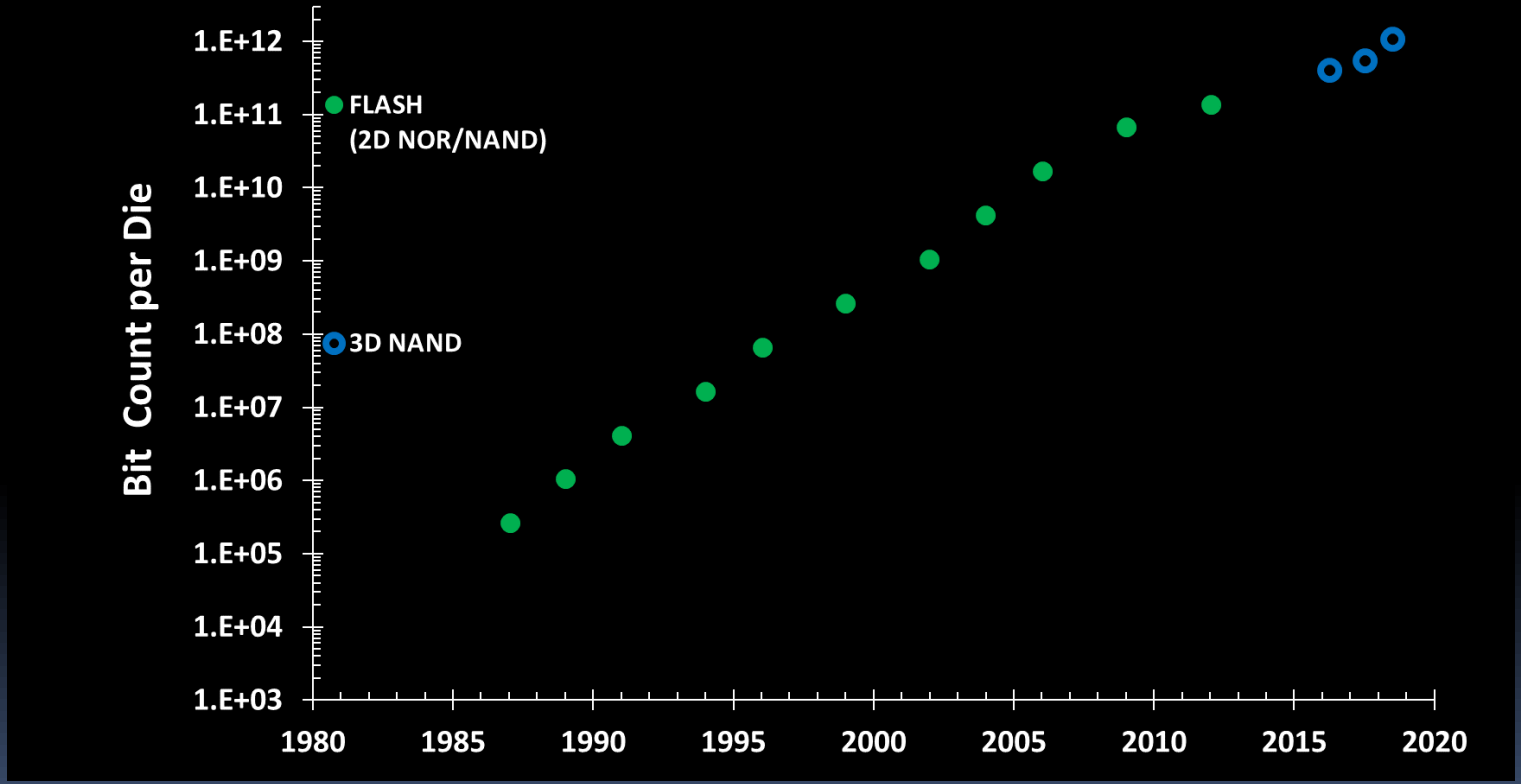


A. Fazio, "Advanced Technology and Systems of Cross Point Memory", IEDM 2020, S24.1

Storage Scaling –

Flash based Solid State Drive displaces Hard Disk Drive*

3D NAND warrants Cost scaling superiority for path ahead



*: Intel Ships Enterprise-Class Solid-State Drives
https://www.intel.com/pressroom/archive/releases/2008/20081015comp.htm

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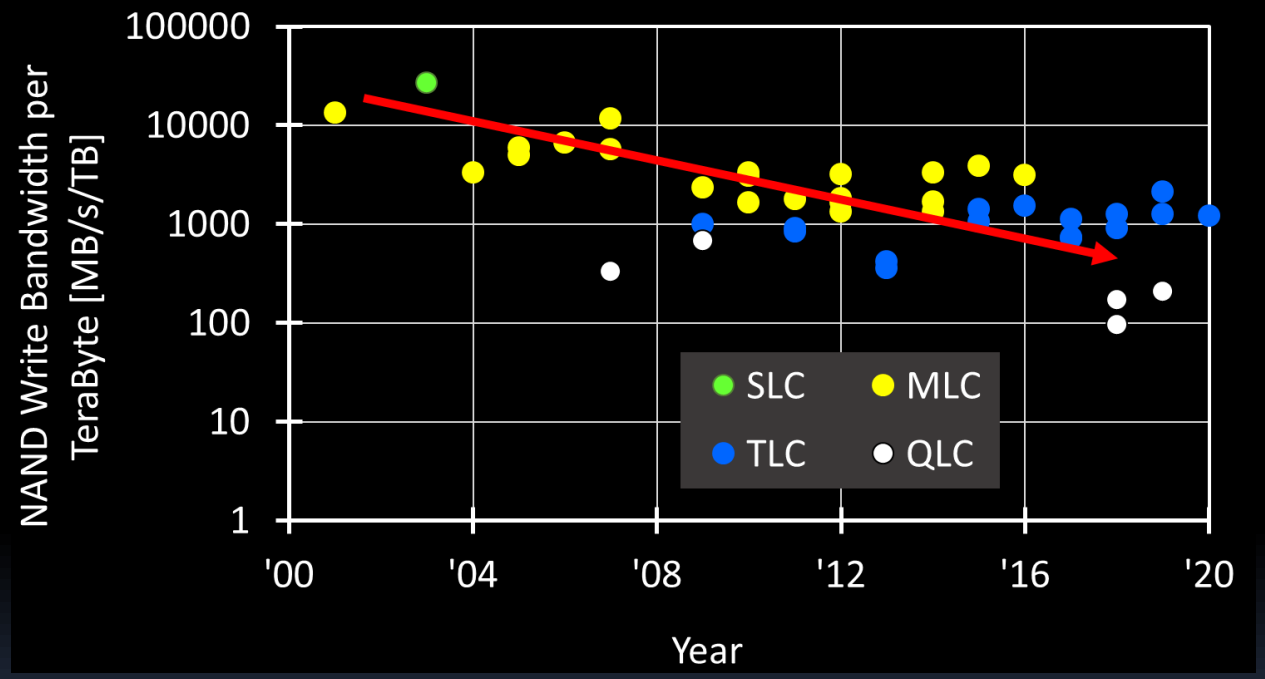
Storage hardly improves bandwidth without adding capacity



Source: various IEEE, ISSCC, IEDM, and IMW papers.

While capacity has grown for NAND, performance – write performance and in particular as more bits per cell are added – has not kept up with capacity growth.

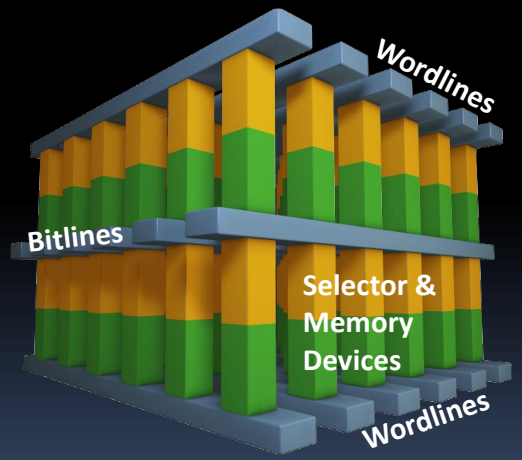
As BW goals often solved by brute force (parallel die), BW density scaling becomes critical due to cost barriers. It amplifies scaling challenges.

The anticipated solution to bridge the gap

von Neumann architecture gave away the answer long ago –

large memory capacity
word
immediately available

Cross Point Memory is a promising scalable solution



- Simple scalable structure + 3D technology
  ➔ Large Memory Capacity
- Individual Cell Access
  ➔ Word (small granularity accessible)
- Fast switching materials + low resistance metal interconnect
  ➔ Immediately Available

Challenge: Mating a selector device with non-linear I-V & a memory element with tight distribution

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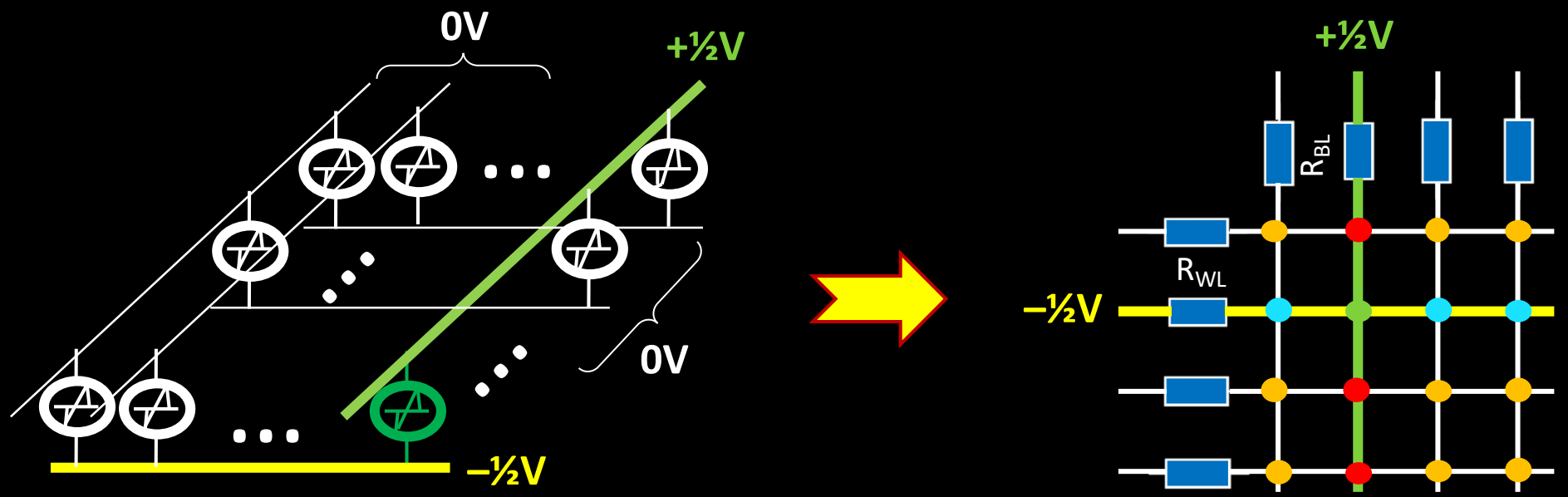
Cross Point Memory Array – ½ voltage biased scheme



The selected bit (•) is at the cross point of the selected bitline (BL) and wordline (WL)

Functionality –

- A fully networked x-y resistive array ➔ Sneak paths thru all de-selected cells (•) connect the selected BL/WL

Reliability –

- All bits on selected BL (•) and selected WL (•) are biased ➔ Read/Write disturbance and retention

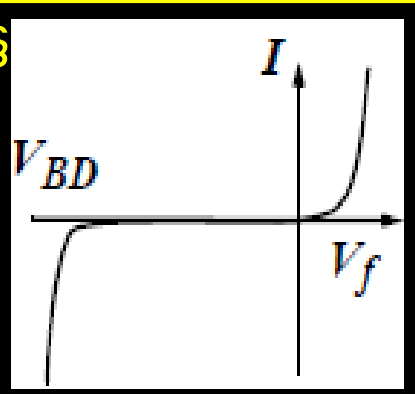
A selector isolates memory cells in an array, improves access accuracy and strengthens reliability.

Selector of a cross-point memory cell is a diode

Diode: two terminals and exhibiting a nonlinear I-V, *IEEE Standard Dictionary of Electrical and Electronics Terms, 1980*

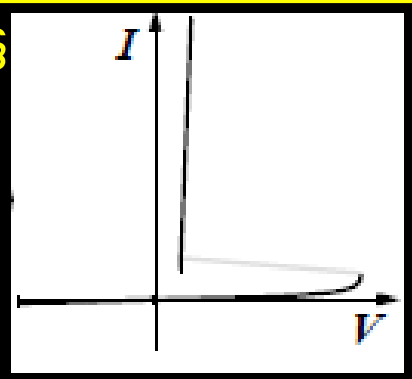
Unidirectional
Asymmetric
Unipolar

§



L-Shape

§



S-Shape

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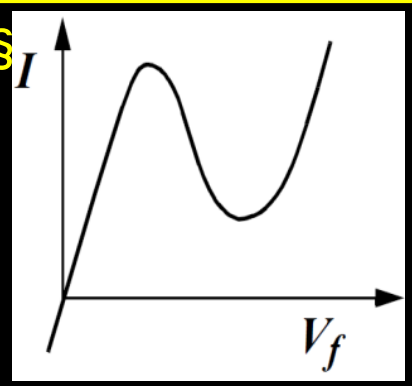
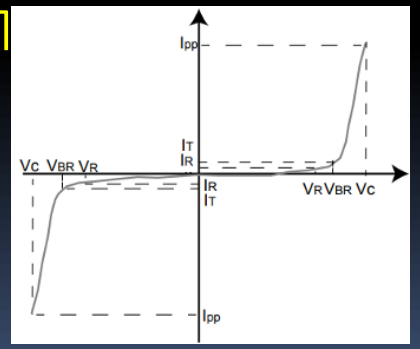


N-Shape

Bidirectional
Symmetric
Ambipolar

¶



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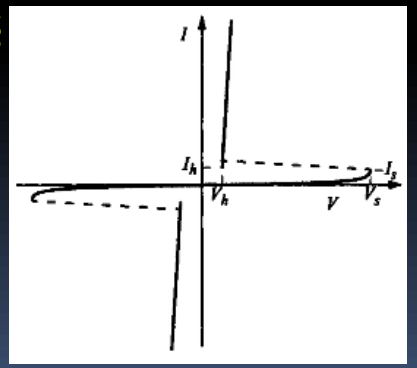

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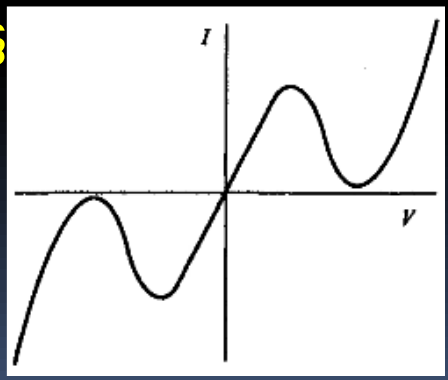
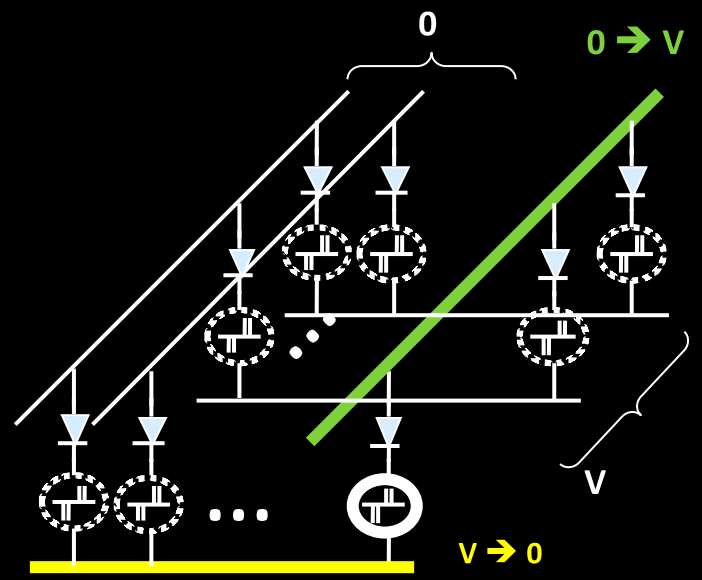


§ : Kowk K. Ng, Complete guide to semiconductor devices, 2nd ed., 2002
¶ :https://www.digikey.com/en/articles/design-in-tvs-diode-protection-enhance-can-bus-reliability

Random Access of a Memory in Cross Point Array

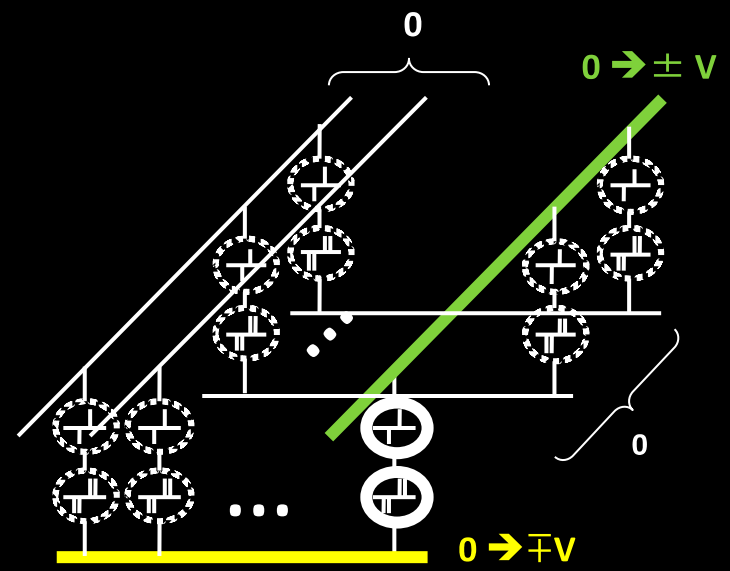
Unidirectional L-Shape Selector



A rectifying selector turns on one bit with forward bias and isolates others with reverse bias.

- Selected BL/WL are toggled between 0V and V
- All bits but selected WL/BL are reversed biased

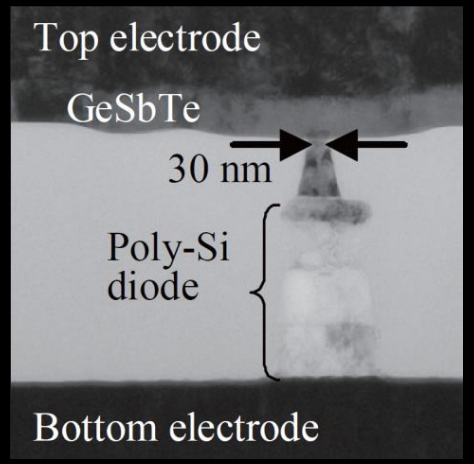
Bidirectional S-Shape Selector



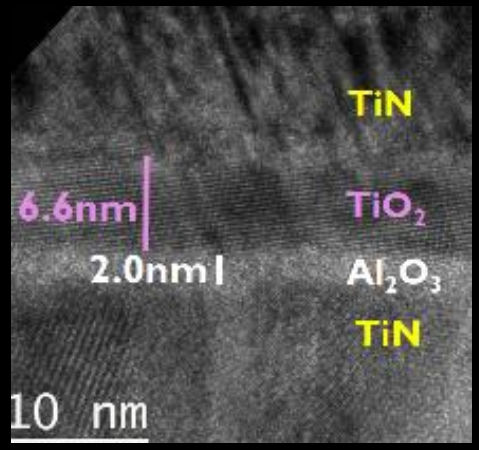
Subject to V_{drop} at each cross points, the selected bit is triggered, and the unselected bits are blocked.

- Selected BL/WL are toggled between 0V and ±V
- All bits but selected WL/BL are 0 biased

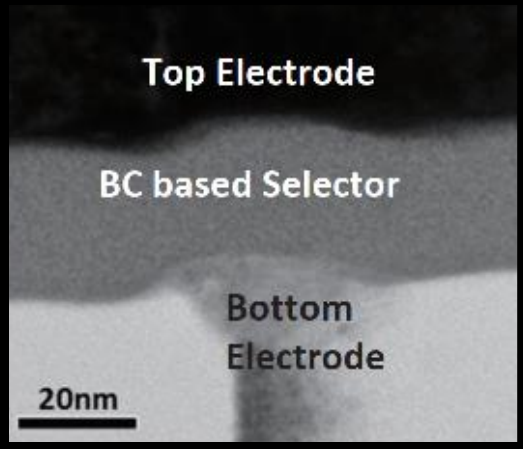
Thin Film Diode Candidates for Cross Point Memory



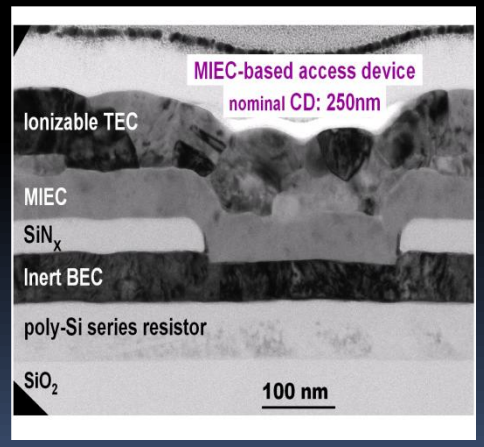
Y. Sasago, *et. al.*,
VLSI '09. T2B-1



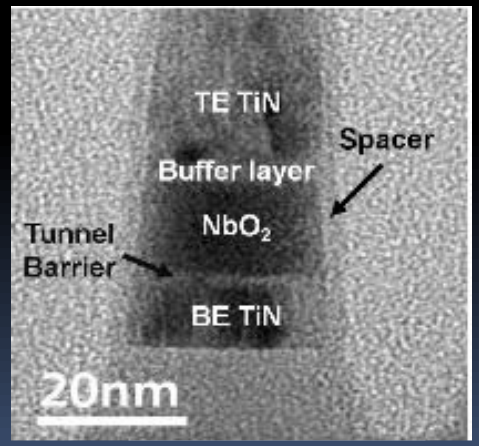
B. Govoreanu, *et.al.*,
IEDM'13. S10.2



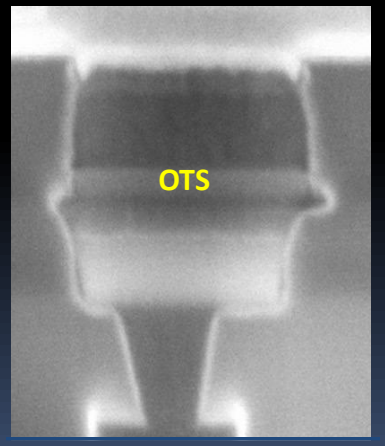
S. Yasuda, *et.al.*,
VLSI, 2017. T2-4



K. Gopalakrishnan, *et. al.*,
VLSI '10. TS19.41

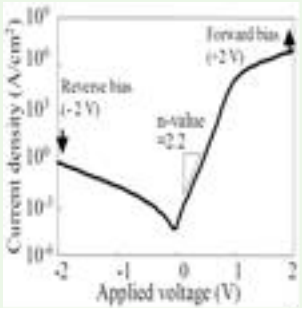
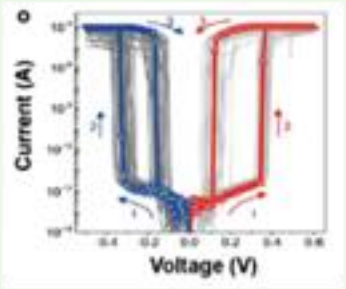
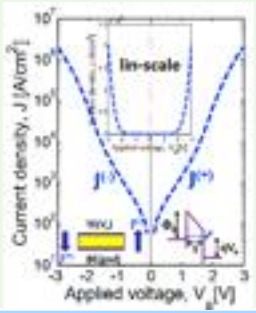
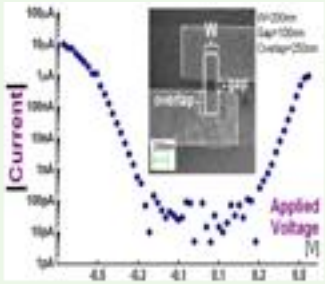
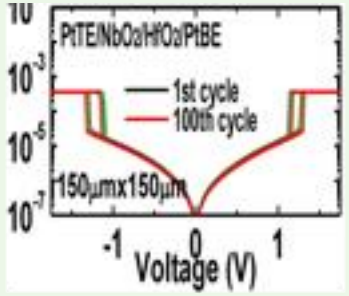
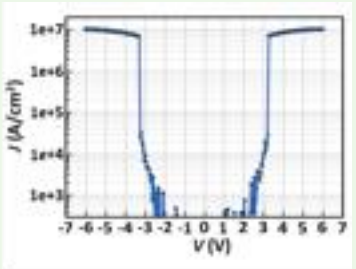


S.G. Kim, *et. al.*,
IEDM '15. S10.3



D. Kau, *et. al.*,
IEDM '09. S27.1

Threshold Switching Phenomenology & Mechanisms

Mechanism	Thermionic	Filamentation	Tunneling	MIEC	MIT	OTS
Construct.	P-N or M-S Jx	Ion (Ag^+) in Ox	MIM	Cu^+ in SE	NbO_2	Chalcogenide
Switching	Electronic	Atomistic	Electronic	Atomistic	Atomistic	Electronic
Polarity	Unidirectional	Bidirectional	Bidirectional	Bidirectional	Bidirectional	Bidirectional
τ_{switch}	sub nsec	ns ~ 100s ns	ps or faster	ns ~ 100s ns	ns to 10s ns	sub ns
J_{MAX}	< 10MA/cm²	1-10MA/cm²	< 1MA/cm²	~10MA/cm²	> 10MA/cm²	> 10MA/cm²
$J_{Inhibit}$	<1A/cm²	<1KA/cm²	<1KA/cm²	<1KA/cm²	<1KA/cm²	<1KA/cm²
$V_{Inhibit}$	< 3V	< 1V	<3V	< 1V	< 3V	< 3V
I-V						
Reference	Y. Sasago, *et. al., VLSI '09*	Z. Wang, *et.al., Adv Func Mtls (2018)*	B. Govoreanu, *et.al., IEDM'13*. P10.2	K. Gopalakrishnan, *et.al., VLSI Symposium* '10.	X. Liu *et.al., EDL* Oct.'14	S. Yasuda, *et.al., VLSI symposium*, '17,

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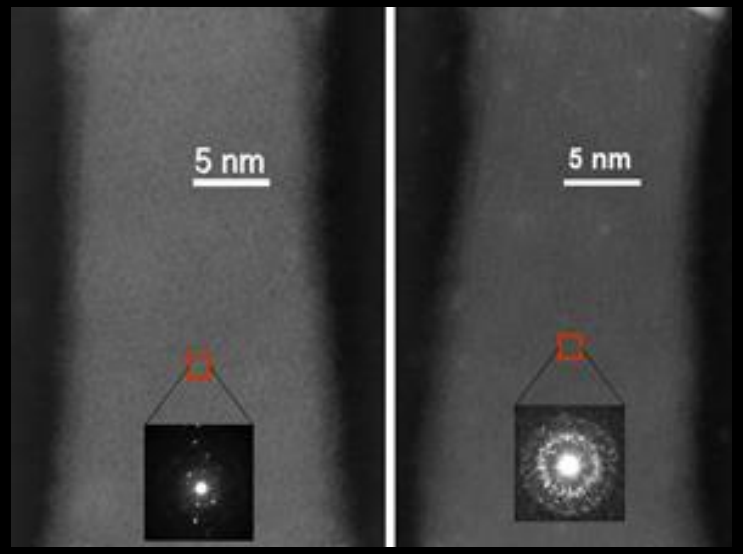
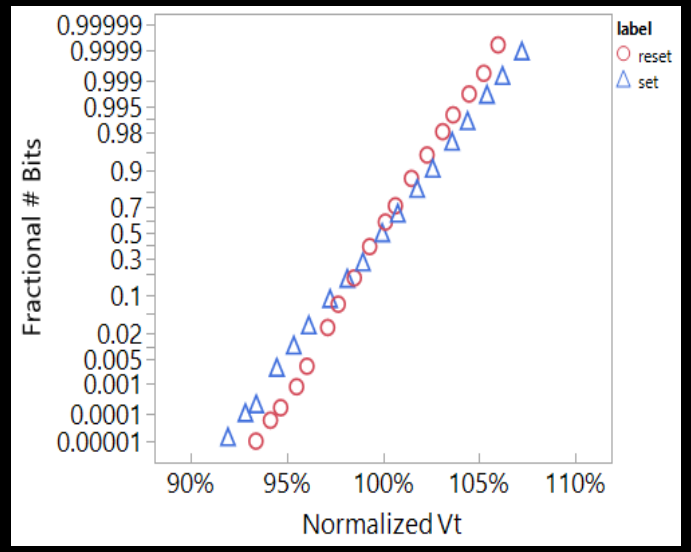
Memory Cell

- Sandwiched at the cross point of wordline and bitline metals
- Selector device is based on Ovonic threshold switches
- Storage element is based on chalcogenide alloy with power efficient memory switching without sub-lithography feature
- Carbon electrode has two jobs: electrical connector and chemical barrier

Memory Switching





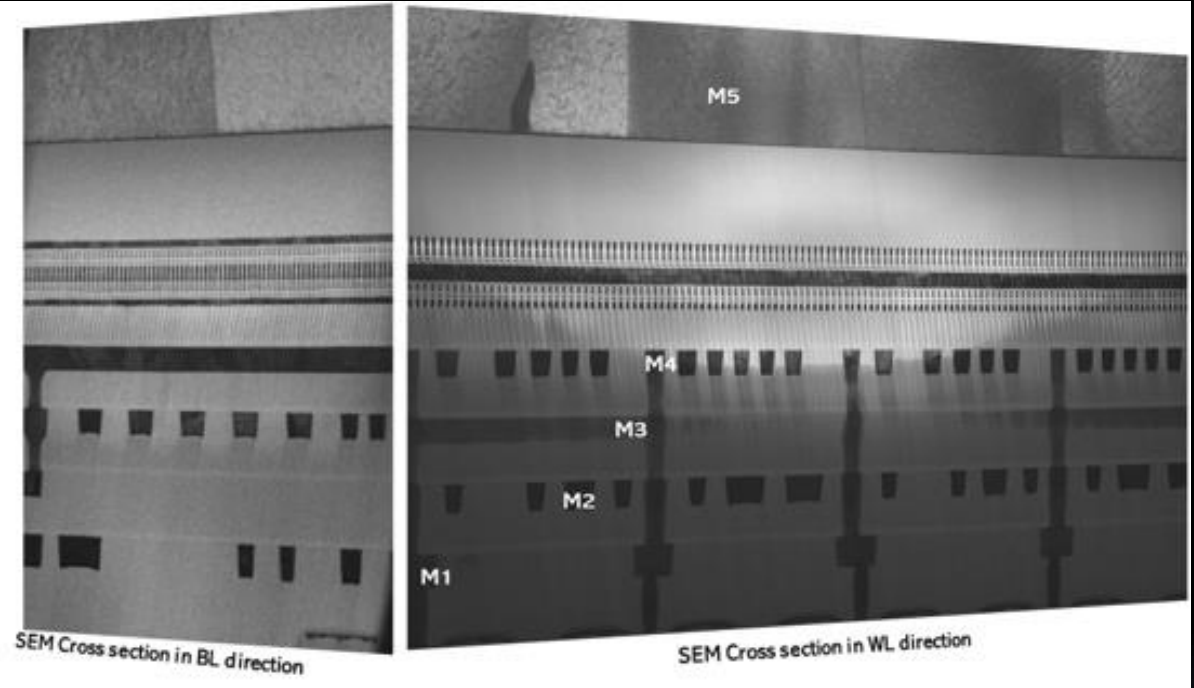
Distinct bulk switching in departure from prevalent chalcogenide memory

Tight statistical control: The entire volume of memory material undergoes bonding transformations between high (fully crystalline) and low (fully amorphous) conductivity with no partial switching.

Deterministic write algorithms: While it shares a chalcogenide-based genealogy with PCM, it does not rely on stochastic crystallization growth processes initiated at the amorphous-crystalline interface no program verification is required.

These fundamental architectural advantages enable low latency, high bandwidth, AND high endurance NVM subsystems.

High-Volume Manufacturing Proven



1st Generation 3D XPoint Media Attributes	
Attribute	Value
Cell Feature Size (half pitch)	20nm
# Decks	2
Die Capacity	128 Gbits
Bank Access Size	16 Bytes
# Independent Banks	16
Read Latency per Bank	100nSec
Write Latency per Bank	500nSec
Write Bandwidth (MB/s) per TB	>35,000MByte/sec/TB

First generation 128Gb 3D XPoint Memory featuring 5-level metal CMOS Under Array technology delivers high density, low latency nonvolatile memory.

Scaling Direction

- Physical Scaling (Density)
  - Increase deck count ➔ Vertical scaling
  - Pitch reduction ➔ Lateral scaling
- Energy scaling
  - Variation tightening for supply reduction
  - Circuit efficiency improvement to reduce AC and DC dissipation
- BW scaling
  - Protocol and circuit optimization to reduce access latency
  - Increase bank count for concurrency
  - Material tuning for performance improvement
- Flash inspired (NOR and NAND)
  - Multi-Level Cell
  - Architecture augmentation

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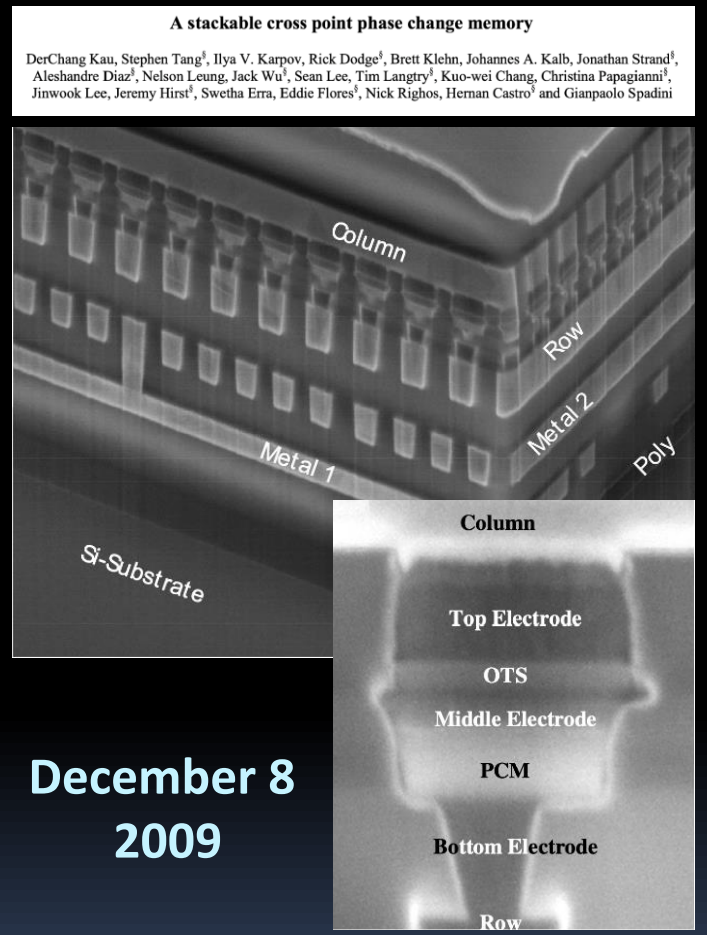
In Pursuit of a Dream …

September 28 1970

December 8 2009



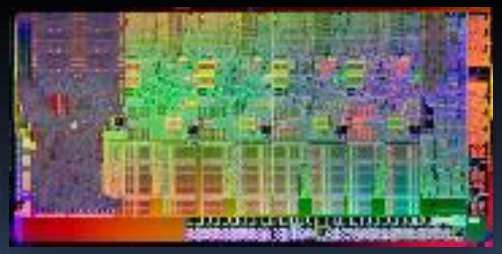
August 13 2020

A Half Century Endeavor

3D XPoint Technology Bridges Memory-Storage Gap

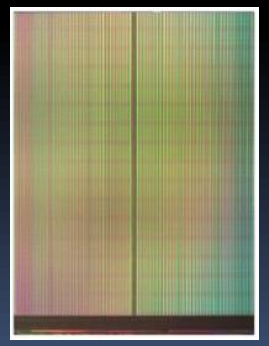
MEMORY + STORAGE

SRAM
Latency: 1X
Capacity: 1X

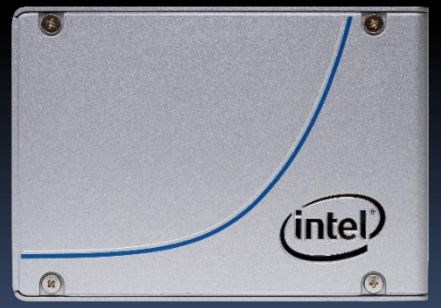


DRAM
Latency: ~10X
Capacity: ~100X

3D XPoint
Latency: ~100X
Capacity: ~1,000X

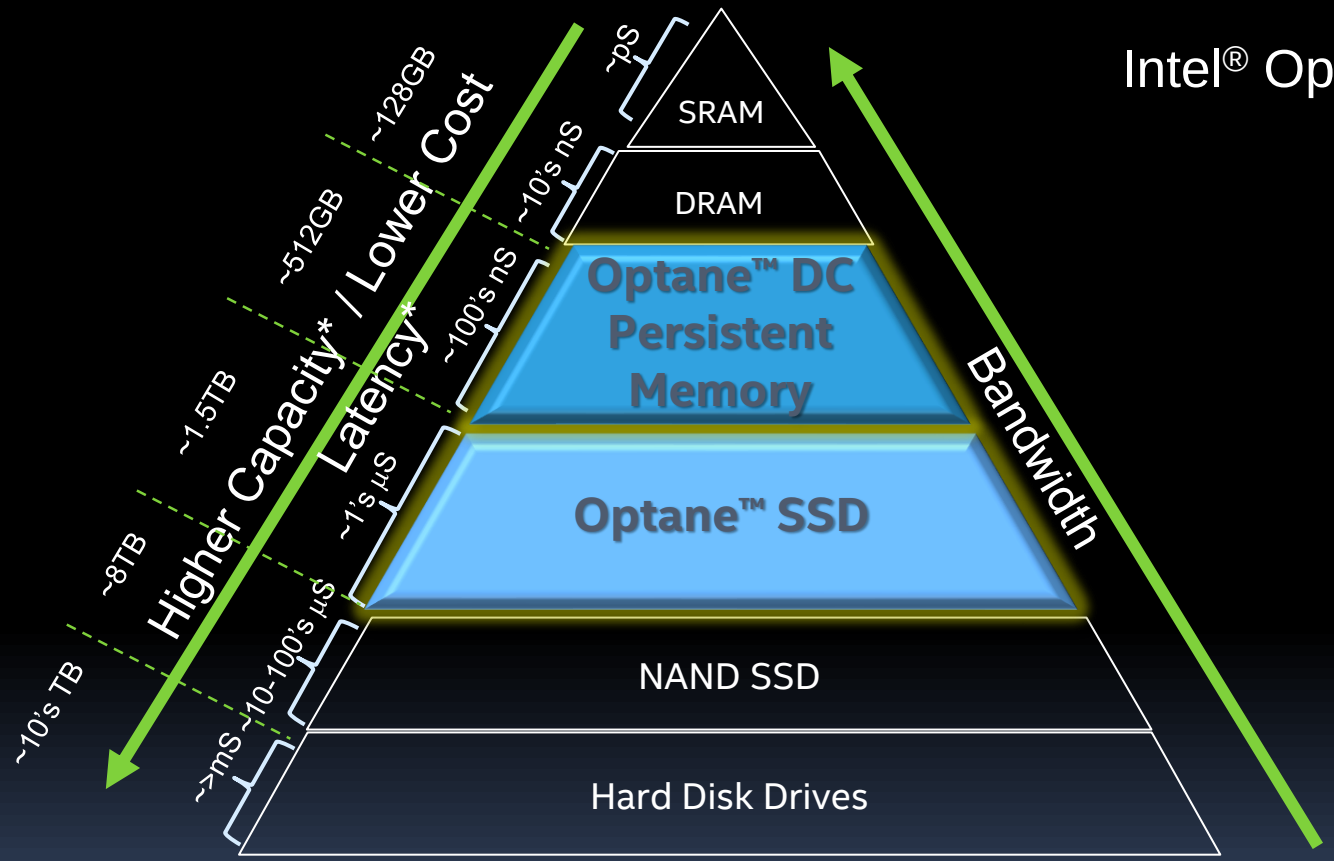


NAND SSD
Latency: ~100,000X
Capacity: ~4,000X-8,000X



HDD
Latency: ~10 Million X
Capacity: ~10,000X

Optane™ based on 3D XPoint



Intel® Optane™ Data Center Persistent Memory

Intel® Optane™ SSD's

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