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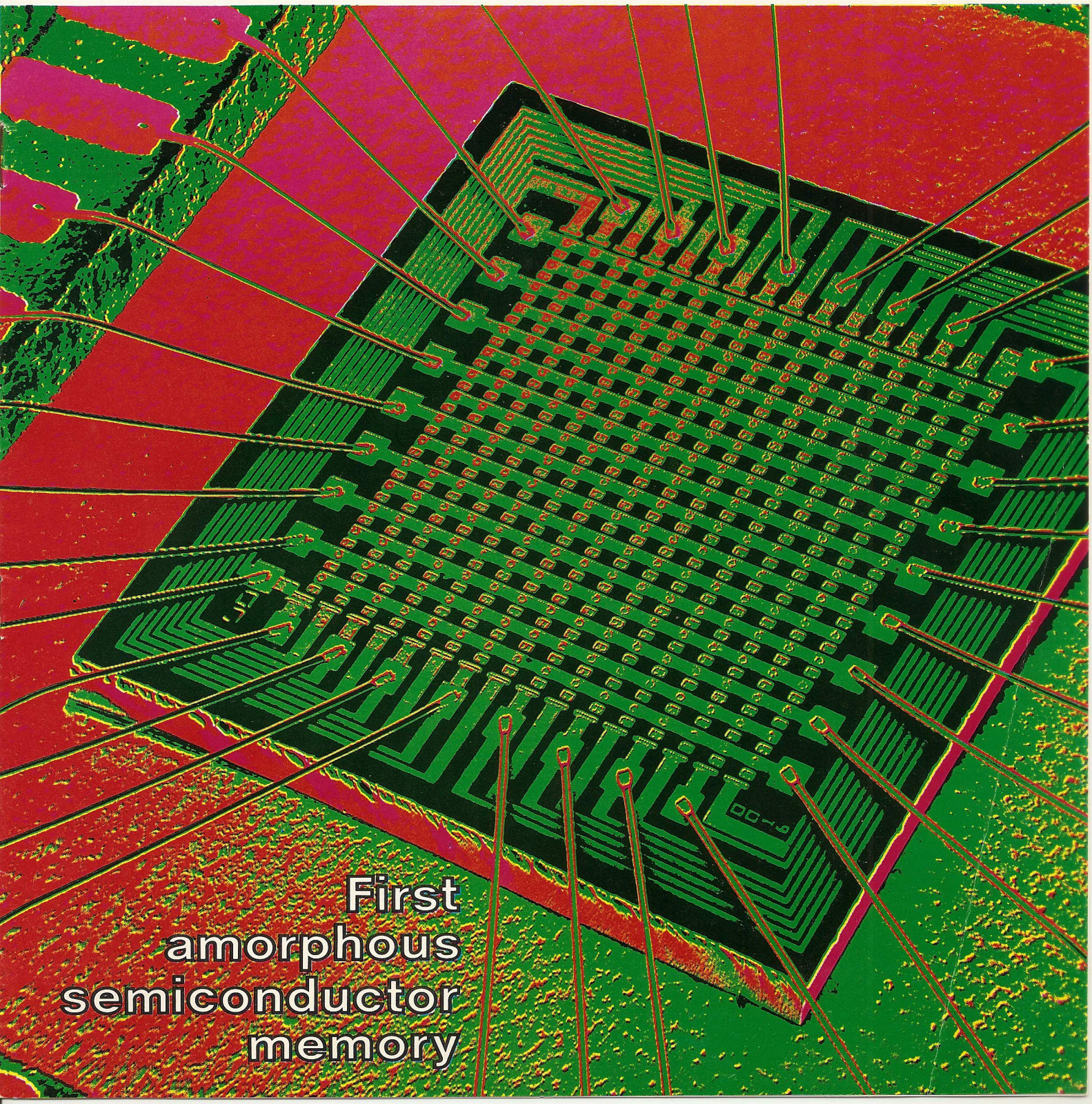

Amorphous semiconductors Part I

Nonvolatile and reprogramable, the read-mostly memory is here

Integrated arrays combine amorphous and crystalline technologies; new memories could help realize promise of microprograming

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☐ Both the read-only and random access varieties of semiconductor memories leave something to be desired in many applications. RAMs' volatility allows data stored to disappear if power fails. On the other hand, ROMs' inflexibility commits them to data that cannot be changed.

A new kind of integrated circuit, the "read-mostly memory," avoids these problems. An integrated array of amorphous and crystalline semiconductor devices available in sample quantities, the RMM can be programed, read, and reprogramed repeatedly. And once programed, the RMM retains data unless it's intentionally altered. The RMM, therefore, doesn't need the data storage on card, tape, or disk required to back up a RAM if power fails. And the same RMM can be used even if the program must be changed; there's no need for the time-consuming and expensive process of making new masks and fabricating a new IC, nor is it necessary to substitute an electrically programable but fixed type circuit.

Microprograming—a computer technique in which a programer can at will change an operational code or sequence—probably will emerge as the most important application for these devices. The great promise of the microprograming concept has yet to be fully realized—even though the idea originated almost 20 years ago—because of the difficulty and cost of changing the contents of microprogram stores with available memory devices.

Several fertile areas exist where the read-mostly memory's special property of electrically alterable, nonvolatile data storage could be usefully applied:

- Airborne computers, which often require a different set of data for a particular mission or operational situation.
- Industrial control systems, in which "canned cycles" —stored instructions—must occasionally be altered for new tooling, instrumentation, or test procedures.
- General purpose computers in which, even though storage of fixed data is required, it is still desirable to make changes in the data during the design phase.

Physically, the new 256-bit RMM's organization is a 16-by-16 matrix of amorphous semiconductor cells, which must be isolated from each other by integrated silicon p-n junction diodes, as shown on opposite page, to prevent spurious paths in the array. The 122-by-131-mil chip size gives a packing density comparable to that of bipolar or MOS techniques, and should improve with fabricating experience. The chip is enclosed in a 40-lead ceramic dual in-line package.

Each cell in the memory consists of an Ovonic amorphous semiconductor device and an isolating diode in series on a silicon substrate, as shown opposite. The Ovonic structure itself consists of a film of amorphous semiconductor material between two molybdenum electrodes. Many such cells—series combinations of Ovonic devices and silicon diodes—are arrayed over the silicon chip, with each cell addressable by an x-y grid, as shown on opposite page, below. The cell behaves like a nonvolatile bistable resistor with an on-to-off resistance ratio of about 10^3.

Without the series diodes, a few adjacent Ovonic devices in the on (low resistance) state might make the Ovonic device being interrogated appear to be on when it's really off. The resistance of the adjacent on cells would shunt the off resistance. With the diodes, however, the back resistance of the diodes added to the on resistance of the adjacent cells prevents this ambiguity.

Despite some superficial resemblances, the amorphous semiconductor memory is quite a different animal from the electrically alterable, fusable type of memory recently introduced by such companies as Radiation Inc., Motorola Semiconductor, and the Solid State Scientific Corp. Although both types can be programed in the same way, the fusable type's program can't be changed, whereas the amorphous semiconductor RMM can be reprogramed repeatedly.

Changing the memory cell from a high-resistance (disordered) to a low-resistance (ordered) state and vice versa—that is, programing—is done by applying a pulse of a certain voltage, current, and duration. The cell can then be interrogated, or read, without changing its state by applying a constant current and measuring the voltage to determine whether the Ovonic device is in its high or low resistance state.

What defines a set or a reset pulse is not so much its energy as its energy-time profile. Thus, the SET, RESET, and READ operations for the 256-bit memory array require significantly different drive conditions, with voltages varying from a few volts to 25 V, currents from a few milliamperes to over 100 mA, and pulse widths from nanoseconds to milliseconds.

Typical configurations for SET, RESET, and READ driving are shown on the next page. Preparatory to a SET operation, the critical voltage of the Ovonic memory must first be exceeded and a current of several milliamperes must flow for several milliseconds to ensure stable conversion to the low resistance state. This action is accomplished by bringing a selected y line (connected to the cathode of the memory cell to be set) to ground through a saturated transistor. Simultaneously holding all other y lines at 25 V (the inhibit voltage) reverse biases the other diodes and thus isolates the memory cells. At the same time, a selected x line (connected to the anode of the memory cell to be programed) is driven by a 5 mA constant current source at 25 V to insure that the amorphous semiconductor is in the ordered state. The drive voltage, however, must not be allowed to increase above 25 V, since a breakdown of the isolation diodes might result.

In the RESET operation, the procedure is similar except that the current source is increased to 200 mA and the pulse width is reduced to 5 μs. As with the SET operation, the voltage is limited to 25 V.

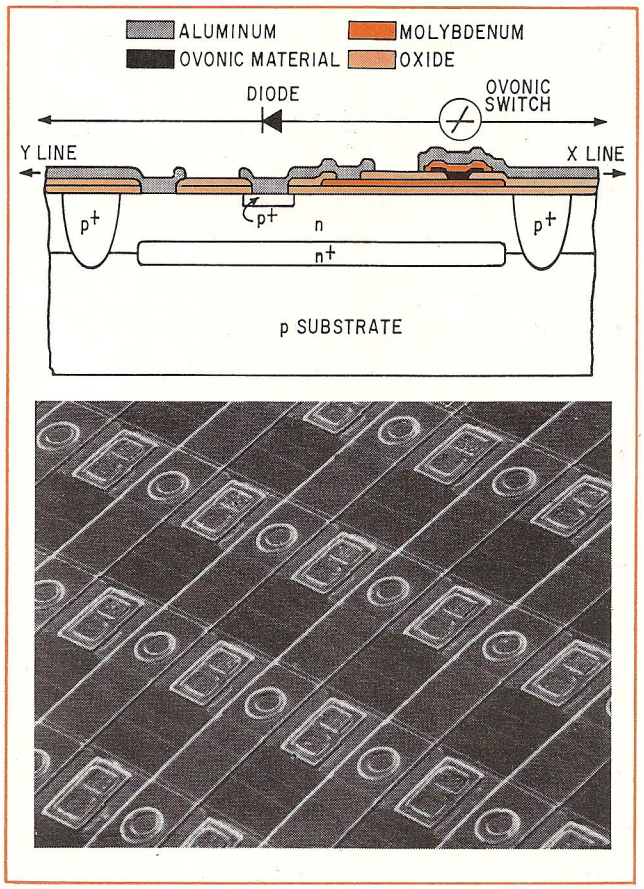
To read a cell it's merely necessary to apply a fixed current to the cell and measure the voltage drop. A low voltage indicates an on (or SET) cell, and a high voltage indicates an off (RESET) cell.

The circuitry for the READ operation must identify the SET and RESET states of a cell quickly. A typical READ condition is a 2.5 mA constant current applied to the selected x line and a grounded y line. The READ output voltage will then be less than 3 V for a SET memory cell, 5 V for a RESET cell.

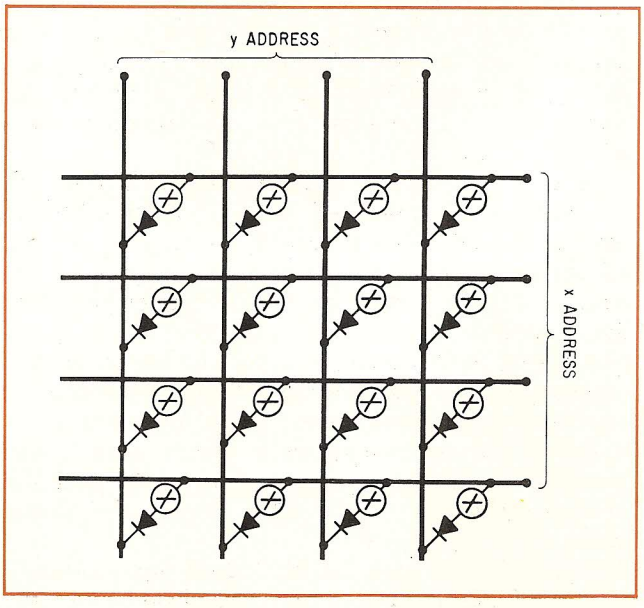
The memory cell array's line capacitance and the storage time of the isolation diode determine reading speed. For fast reading, the large capacitance of the y line should be driven by a low-impedance source. The small capacitance of the x line should be driven by a constant current source to forestall excess current through the amorphous memory switch. Such conditions could produce an array access time of about 65 ns. However, the access time for the system would be somewhat longer because of the propagation time of the decoder and driver circuitry.

Of course, the drive circuitry will vary with the particular system. Some applications may not require SET or RESET circuits in the system itself; programing would then be done by external equipment. Also, dropping the 25 V requirement for setting makes the READ circuit relatively easy to implement.

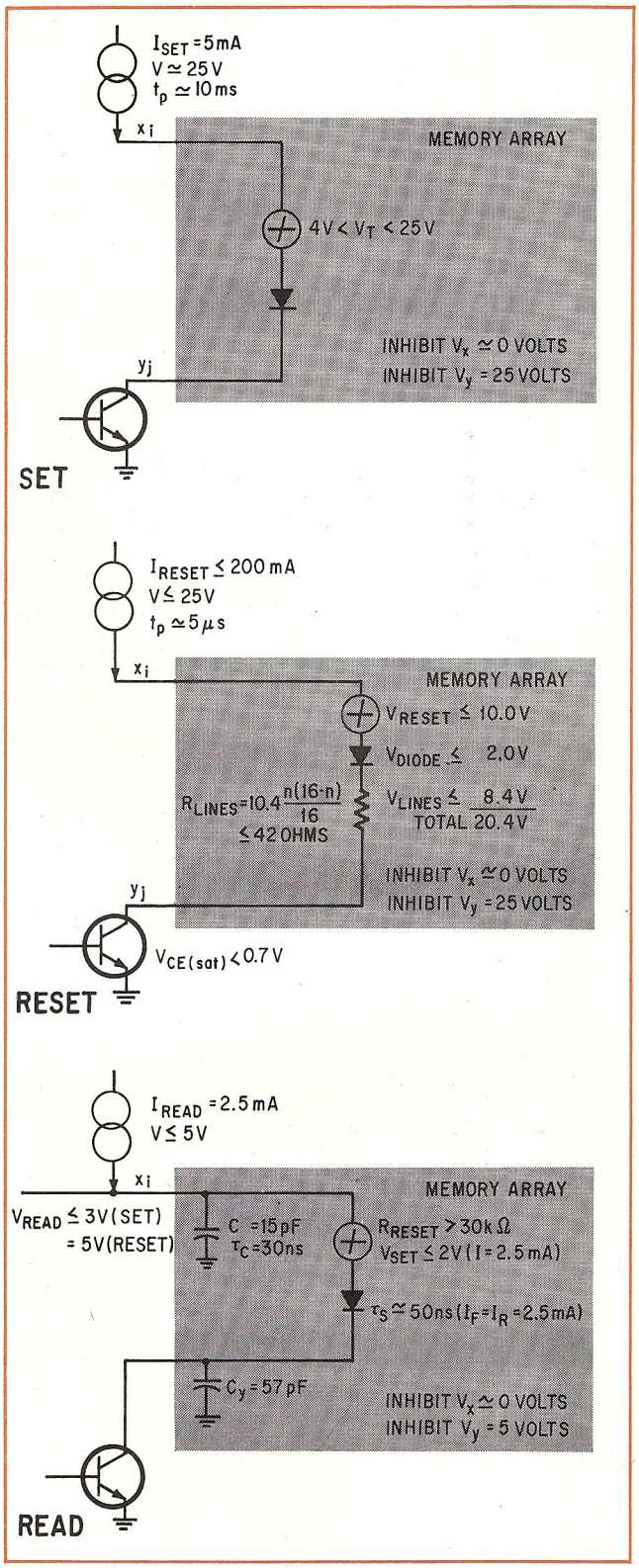
The simplicity and cost of the READ circuit depends



Winning combination. Each read-mostly memory cell contains a thin-film of amorphous semiconductor material deposited on a single-crystal silicon substrate in series with a silicon diode. The metal stripes—the x-address lines—connect the doughnut-shaped Ovonic switches. Running perpendicular to the stripes the y-address lines buried in the silicon connect the figure-eight-shaped silicon diodes. The diagram at top details the cross section of a complete memory cell.



Array. The isolating diodes and Ovonic switches are connected in series across an x- and y-address line. The RMM consists of 256 such combinations.



How to read. The operations of SET, RESET, and READ require significantly different values of voltage, current, and pulse duration. Typical conditions are shown in this diagram. The inhibit voltages are for the x and y lines, respectively; n is the number of diodes; V_T is the critical voltage of the amorphous semiconductor; t_p is the pulse duration, and τ_C and τ_S are the time constants affecting READ speed.

on speed requirements: at lower speeds, simple pull-up resistors will suffice, but higher speeds necessitate active pull-up drivers.

One of the knottiest aspects in the RMM development was how to integrate the amorphous-semiconductor memory cells and the silicon substrate containing the isolation diodes. The processing conditions and sequence had to be adjusted to insure compatibility with both types of device.

The problem centered on the aluminum that connects the isolation diodes to the Ovonic devices. This aluminum must be alloyed to the silicon substrate to assure a good contact. However, alloying requires a temperature of about 550°C, which would be too high, since it would also destroy the amorphous semiconductor materials.

This impasse was resolved by depositing and etching the molybdenum film that serves as the lower electrode for the amorphous semiconductor and then alloying or sintering the aluminum to both the silicon diode and the molybdenum. A clear molybdenum surface contact is thus left for the amorphous semiconductor. The aluminum applied over the amorphous semiconductor cell in a subsequent step need not be alloyed, since it doesn't contact the silicon.

As in other p-n junction isolated silicon ICs, the breakdown voltage is an important consideration. The diodes consist of p-type regions of material in n-type channels, as shown on the preceding page. Each of the 16 n-type channels contains 16 diodes. The maximum voltage that appears across the n-type channels must not exceed the breakdown voltage between the n-type channel and p-type isolation channel.

The resistivity of the n-type channel is about 20 Ω per square for the process used (the same process used to make transistor-transistor logic ICs). For a square memory cell (Ovonic device and isolating diode combined), the line resistance for 16 diodes would be 320 Ω. A RESET current of 100 mA passing through the channel develops a voltage drop of 32 V. In the TTL process, however, breakdown voltages usually range from 25 to 30 V, and the channel isolation would fail.

Diffusing a shallow n^+ region along the channel reduces the channel's resistivity from 20 Ω per square to 3 Ω per square and, hence, the voltage drop across it. Moreover, no extra process step is required as the n^+ diffusion is needed anyway to establish an ohmic contact between the aluminum and the n-type channel.

In addition, the diode channels have both ends shorted by an aluminum conducting strip around the outside of the array, reducing the effective interconnection resistance to the cells. This places the channel in parallel with the addressing line, reducing their effective resistance. Thus, the channel resistance for a channel of n cells is nR/4 when both ends of the channel are shorted, whereas it would be nR without the short.

Repeatability of SET and RESET cycles was the prime concern at the outset of the RMM development. Large quantities of devices were therefore tested to

Benign disorder

The useful bistable characteristic of amorphous semiconductor material depends on a reversible phase transition between two states of greater and less disorder—high resistance and low resistance. To understand the effect, consider the diagram of a thin film of amorphous semiconductor in a memory system, shown below. (The physics of amorphous-semiconductor switching are explained in detail in the article immediately following.)

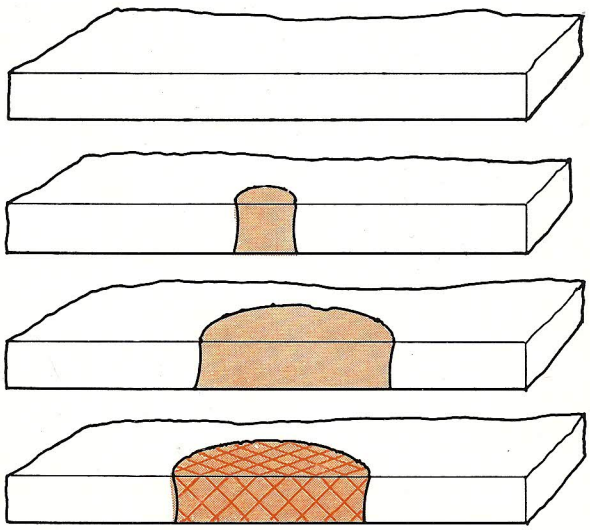
To switch a cell to the low resistance state, a voltage exceeding a certain threshold value V_t is applied across the amorphous film. This is an electronic process, not a thermal one, which switches the film and establishes an initial conducting condition that enables electrical energy to be deposited in a confined film channel. A 50-microjoule pulse applied in about 10 milliseconds heats the amorphous material sufficiently to change phase from a disordered or glassy state to a more ordered structure.

The crystallization, or ordering process, is related to the participation of carriers from the valence band—those that form the bonds in the material—in the conduction process. The removal of these carriers from the bonds allows atomic restructuring to take place more easily. Accompanying this change is a drop in resistance of some 3 or 4 orders of magnitude. The sequence of events is called SET process.

The duration of the SET pulse is important. For example, a pulse of only 0.1 ms won't create a permanent change in the amorphous film even though the pulse's amplitude is greater than the critical value V_t. The memory cell will switch to the low resistance state, but when the pulse terminates, the cell reverts to the high resistance state. But with a 10-ms pulse, the cell will remain in its low resistance (or on) state after the pulse is removed. The cell then can be continuously interrogated nondestructively. This is called the READ operation.

To return the cell to its high resistance (RESET) state, the material must be changed back to the disordered state. This is achieved by applying a high current for a short period (approximately 5 microseconds). With about 5 μJ of energy deposited in the cell, the heat generated returns it to the amorphous state, as shown below. The cell cools rapidly, and the disordered, high-resistance state is maintained at room temperature. A typical cell with critical voltage of 15 v is about 1.5 micrometers thick and 5 μm in diameter; such a cell cools to room temperature in about 1 μs.

SET—High to low resistance



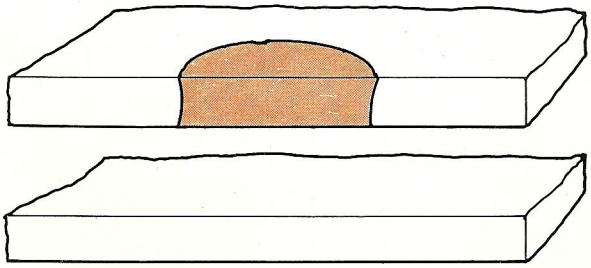
Initial state—high-resistance amorphous material

SET pulse is applied. Voltage across the device exceeds threshold and conduction starts in a small confined channel. Material is still amorphous.

Energy dissipation caused by current flow expands the channel's diameter until it reaches a size related to the SET energy-time profile; material is still amorphous.

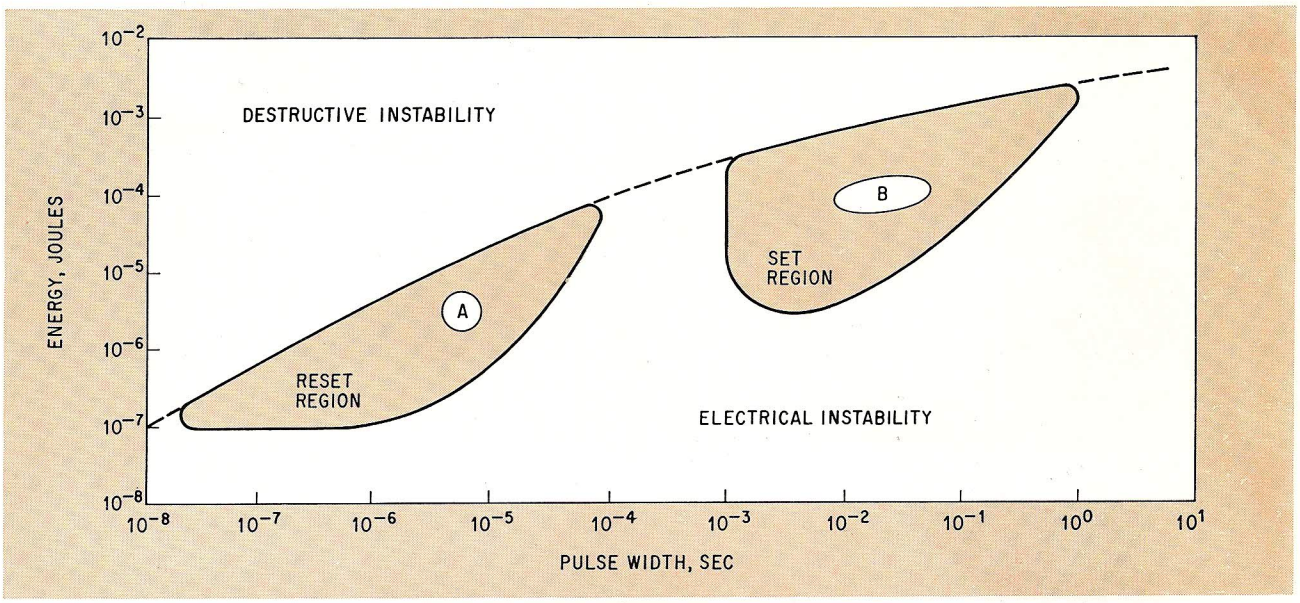
An ordered state with a greatly lower channel resistivity develops and is retained when the current is removed. The material is no longer amorphous.

RESET—Low to high resistance

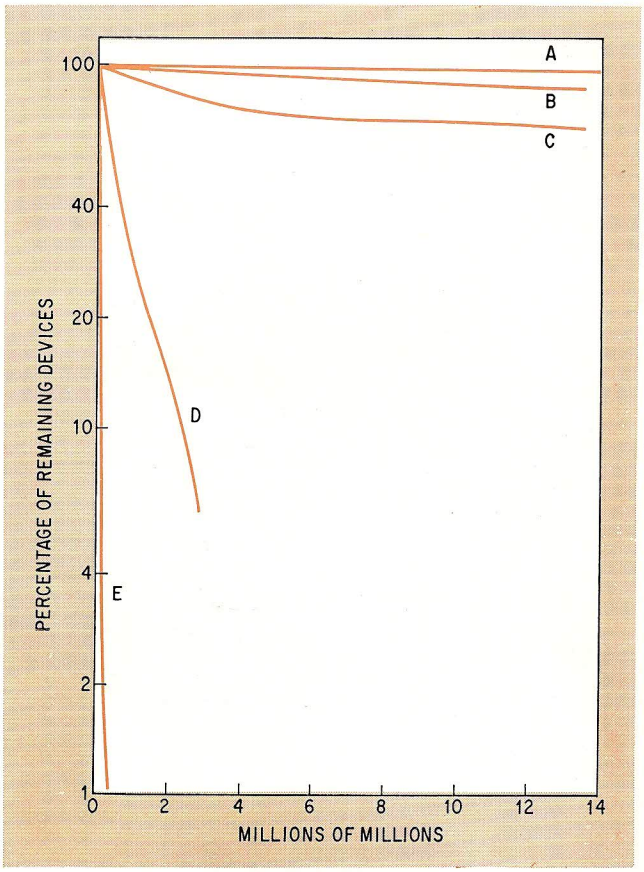


An applied RESET pulse returns the material to the high-resistance amorphous state.

The amorphous state remains when the power applied to the device is removed.



Time and energy. To ensure that the memory is stably SET or RESET without any damage, the energy-time product should fall within the shaded regions. Also an effective change of state requires sufficient RESET energy to reconvert the entire volume of material that has been SET. Thus, a cell that has been SET in region B must be RESET in region A



Life cycles. Relatively small changes in the composition of material will affect the operating lifetime of amorphous memory cells. Replacing two atomic % of one constituent in a three-element glass with another shifts the lifetime from the short-lived curve marked E to the long-lived curve marked A.

evaluate the effects of repeated cycling on various switching materials and geometries, and under differing processing and operating conditions. Thousands of test cycles were made.

It was found that the composition of an amorphous semiconductor can dramatically affect the lifetime of the device. The curves shown at left illustrate the effect: the nearly vertical short-lifetime curve (marked E) represents a three-element glass amorphous semiconductor.

The addition of only 2 atomic percent of an additional element shifts the cycle lifetime behavior to the nearly horizontal long-lifetime curve (marked A). The three upper curves represent material compositions that Energy Conversion Devices is studying and optimizing for use in the RMM.

The energy-time combination used for SET and RESET also profoundly affects life expectancy. Certain regions on an energy versus time plot result in effective setting and resetting, as shown above. An energy-time combination that falls below the regions defined by the roughly triangular regions will not produce a stable change in the state of the memory cell, not even after repeated cycling.

Another consideration is the energy-time balance; a cell set with a certain energy within the SET safe area must be reset at a compatible energy in the RESET safe area. Thus, if a cell is set within the ellipse marked B on the energy diagram, then the proper RESET condition should lie within the circle marked A.

The reason for this correspondence requirement is that the area of the converted region in the amorphous semiconductor film depends on the SET energy-time. Thus, as more material is converted to the ordered state, a larger energy is required to achieve a stable reconversion. □