The Pursuit of Atomistic Switching and Cross Point Memory

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Abstract: With the disclosure of the chalcogenide memory technology in the early 2000s[1], the pursuit of nonvolatile memory beyond electrostatic storage escalated across the industry. Various two-terminal switches exhibiting nonlinear I-V characteristics have been explored as a cost-effect solution. Within a decade, an experimental attempt to integrate chalcogenide switch and memory for a 64Mb array was successfully demonstrated[2]. It illustrated a vision of a new class of memory, bridging the gap between DRAM and SSD. Another decade later, 3D XPoint Memory is commercialized, disrupting the memory hierarchy.

I. Introduction

As illustrated in Figure 1, cost-effective computing architectures construct a layered pyramid of memories, each of which possesses higher performance at lower capacity than the layer beneath. NAND Flash based storage, SSD, has successfully displaced performance deficient hard disk drives as primary storage. However, the gap between main memory (DRAM) and SSD remains significant. 3D XPoint memory[3], with high capacity and performance at byte access, is designed to bridge the gap. This paper reviews cross point memory technologies and the enablers for high density, low latency memory.

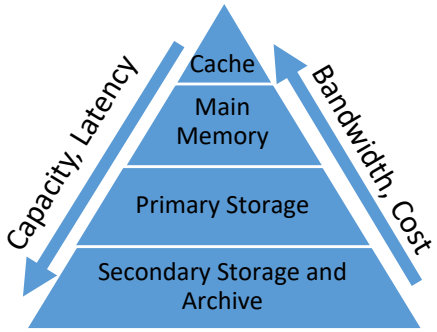

Figure 1. Layered pyramid of memory – Each layer possesses higher performance & lower capacity than the layer beneath.

II. Atomistic Memory Switching in Cross Point Array

A cross point memory array, as the name suggests, is an array of memory cells sandwiched between orthogonally oriented wordlines (WLs) and bitlines (BLs). As memory switches, the cell alternates between resistance states. Research of memory materials explores atomistic switching mechanisms including spin polarization, ferroelectricity, phase change, interfacial barrier modulation, and filamentation in solid electrolytes or composition segregation. Superior geometric scalability of atomistic memory switching has been demonstrated in research labs. For example, the GST scaling limit of the phase change mechanism is experimentally found between 3.6 to 8.8nm[4].

In a cross point memory array, shown in Figure 2, a cell consists of a storage element without a selector device. At standby, all BLs and WLs are 0V biased. When reading a bit, the selected BL goes to +V and the selected WL goes to –V in order to detect the selected bit resistance. However, in a fully networked x-y resistive array, sneak paths through all deselected cells interfere with the intended interrogation. The functionality of cross point array deteriorates as the array size increases. Another issue is the reliability of the array. Since all the deselected bits in the selected WL and BL are biased during memory operation, they are subject to read/write disturb and retention without proper insulation from the bias. Adding a selector in series to each storage element isolates the memory cells, reducing cross talk, improving access accuracy and strengthening reliability.

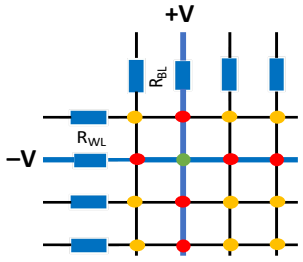

Figure 2: Memory access in a Cross Point Array

III. Choice of Two Terminal Selector

In a cross point array, a two-terminal selector must be low resistance when selected in order to access the memory and high resistance when inhibited in order to insulate the memory. Generically speaking, a two terminal selector is a diode exhibiting a nonlinear IV.

A unidirectional diode, such as a PN junction rectifier, can be used for polarity independent memory switching. A rectifying selector turns on one bit with forward bias and isolates others with reverse bias, as shown in Figure 3. During standby, all bits are reverse biased with BLs at 0V and WLs at +V. When one bit is selected, the selected BL switches to +V and selected WL switches to 0V.

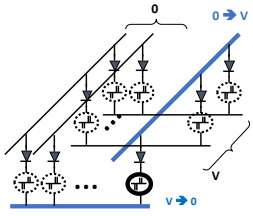

Figure 3. A rectifying selector turns on one bit with forward bias and isolates others with reverse bias.

A bidirectional diode, such as a S-shaped DIAC, can be used for both polarity-dependent and ambipolar memory switching. During standby, all bits are zero biased. When one bit is selected, the selected BL switches to +V and selected WL switches to –V. Given that only bits along the selected WL and

BL are biased, the bidirectional diode presents a clear advantage in leakage and disturbance.

In the past decade, there were several researches in pursuit of a two-terminal selector[2,5-11] (Table 1). Among those, the Ovonic Threshold Switch (OTS)[12], demonstrated its capability to construct a high density, low latency memory array. 3D XPoint, deployed with OTS, is the only cross point technology that has achieved high-volume production.

Mechanism	Thermionic[5]	Filamentation[6]	Tunneling[7]	MIEC[8]	MIT[9]	OTS[2,10,11]
Construct.	P-N or M-S Jx	Ion (Ag^+) in Ox	MIM	Cu^+ in SE	NbO_2	Chalcogenide
Switching	Electronic	Atomistic	Electronic	Atomistic	Atomistic	Electronic
Polarity	Unidirectional	Bidirectional	Bidirectional	Bidirectional	Bidirectional	Bidirectional
τ_{switch}	sub nsec	ns ~ 100s ns	ps or faster	ns ~ 100s ns	ns to 10s ns	sub ns
J_{MAX}	< 10MA/cm^2	1-10MA/cm^2	< 1MA/cm^2	~10MA/cm^2	> 10MA/cm^2	> 10MA/cm^2
$J_{Inhibit}$	<1A/cm^2	<1KA/cm^2	<1KA/cm^2	<1KA/cm^2	<1KA/cm^2	<1KA/cm^2
$V_{Inhibit}$	< 3V	< 1V	<3V	< 1V	< 3V	< 3V

Table 1. Pursuing 2-terminal selector for cross point memory

IV. 3D XPoint Technology

The core of 3D XPoint Memory is a two-terminal memory cell, pairing a storage element and an OTS. The storage element is designed such that the entire volume of memory material undergoes bonding transformations between high (fully crystalline) and low (fully amorphous) conductivity with no partial switching for tight statistical control of states (Figure 4).

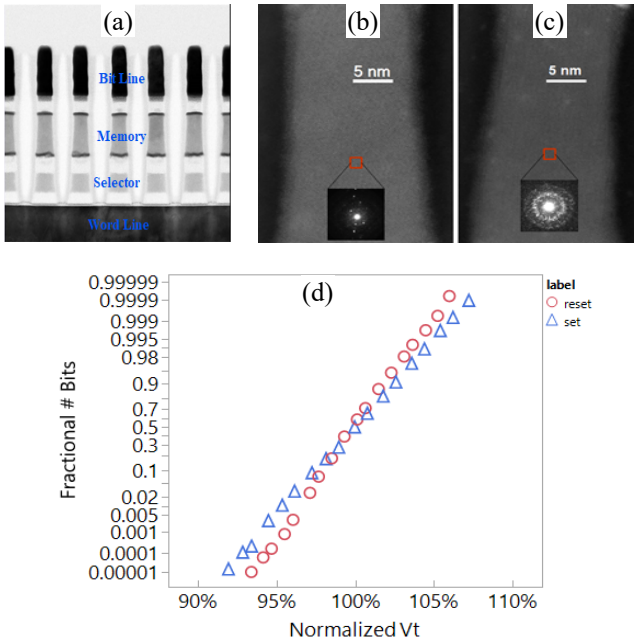

Figure 4: The core of 3D XPoint Memory cell consists of a storage element and an Ovonic Threshold Switch (a). Storage element is fully crystalline (b) or fully amorphous (c) for tight distribution of states (d).

Cost-effective cross-point memory technology is realized through low thermal budget processes integrated at the cross point between metals. This backend memory technology is compatible with mainstream semiconductor processes that feature CMOS under array allowing deck stacking for low-cost memory products. (Figure 5 and Table 2)

V. Summary

3D XPoint Memory introduces a novel memory cell, consisting of a switch and storage element, to bridge the gap between main memory and storage. The cross point architecture, integrating the Ovonic Threshold switch, a high speed non-volatile storage element, and low RC array parasitics, enables persistent, byte addressable, capacious memory.

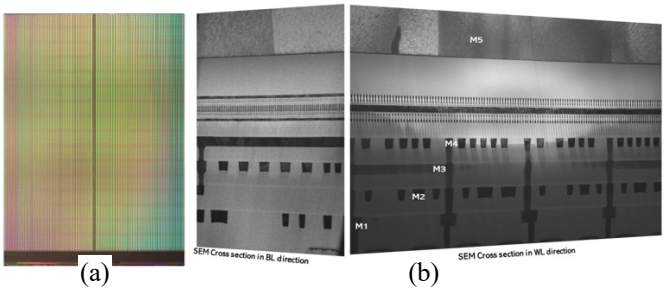

Figure 5: First generation 128Gb 3D XPoint Memory (a) featuring 5-level metal CMOS Under Array technology delivers high density, low latency nonvolatile memory.

1st Generation 3D XPoint Media Attributes	
Attribute	Value
Cell Feature Size (half pitch)	20nm
# Decks	2
Die Capacity	128 Gbits
Bank Access Size	16 Bytes
# Independent Banks	16
Read Latency per Bank	100nSec
Write Latency per Bank	500nSec
Write Bandwidth (MB/s) per TB	>35,000MByte/sec/TB

Table 2: Key attributes of 1st generation 3D XPoint media

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