工業技術研究院
Industrial Technology
Research Institute

2021 VLSI-TSA

INVITED SPEAKER'S REPLY SHEET

1. Personal Information

Profile

Photo 	**First Name** DerChang	**Middle Name**	**Last Name** Kau
	Title Mr.	**Position** Fellow	**Department** Intel Optane Group
	Affiliation Intel		
	Address **2200 Mission College Blvd, Santa Clara, CA 95052**		
	Nationality USA	**Tel.** **+1-408-7650-0266**	
Mobile **+1-408-398-6086**	**Email** derchang.kau@intel.com	**Special dietary requests** ☒ No ☐ Vegetarian ☐ Others:	

Brief Biography (for session chair to introduce the speaker)

Mr. DerChang Kau is an Intel Fellow and the director of NonVolatile Memory Technology Pathfinding at Intel. He leads the team exploring novel memory architecture and is responsible for the strategic direction of atomistic memory devices and switches. He is a veteran of the semiconductor industry; actively involved in R&D and scaling of logic, memory, mixed signal, and radio technologies.

◆ **Working Language:** The working language of the symposium is English. Interpretations will not be provided.

2. Speech Information

Topic of Speech：The Pursuit of Atomistic Switching and Cross Point Memory

Abstract (about 100 to 200 words):

With the disclosure of the chalcogenide memory technology in the early 2000s[1], the pursuit of nonvolatile memory beyond electrostatic storage escalated across the industry. Within a decade, an experimental attempt to integrate chalcogenide switch and memory for a 64Mb array was successfully demonstrated[2]. It illustrated a vision of a new class of memory, bridging the gap between DRAM and SSD. Another decade later, Optane™ Memory is commercialized, disrupting the prevailing memory hierarchy.

The core of Optane™ Memory is a two-terminal memory cell, pairing a storage element and a selector switch. The selector isolates memory cells in an array. It improves the signal to noise ratio and disturb immunity. Effective cross-point memory technology is realized through low thermal budget processes integrated at the cross point between metals. This backend memory technology is compatible with mainstream semiconductor processes that feature CMOS under array allowing deck stacking for low-cost memory products.

Prospective two-terminal switches exhibiting nonlinear I-V characteristics in a cross-point memory array will be discussed. The phenomenology, switching speed, underlying mechanisms, and compatibility to memory access will be benchmarked.

[1] Stefan Lai, *et.al.*, IEDM Tech. Dig., 2001, pp36.5.1-36.5.4
[2] DerChang Kau, *et.al.*, IEDM Tech. Dig., 2009, pp27.1.1-27.1.4

3. About the Symposium

- Submitting a 2-page extended abstract for the conference proceedings before February 1, 2021.

  ☒ Yes, I WILL submit the 2-page extended abstract and copyright right form (eCF) to the IEEE. (Please note that your paper will not be submitted to the IEEE Xplore database if you do not complete the eCF transfer.)

  ☐ No, I WILL NOT submit the 2-page extended abstract and will only show my short abstract (100~200 words) in the conference proceedings.

- I am willing to share my presentation slides (in PDF format) with the attendees after the symposium: (We will post the slides on the conference website for attendees to download it.)

  ☐ Yes, I am willing to share the **original** presentation file with the attendees.

  ☒ Yes, I am willing to share the **modified slides** with the attendees.

  ☐ No, I am not willing to share the slides.

- Will Attend Welcome Dinner on April 19, 2021.*

  ☒ Yes ☐No.

  Every invited speaker is invited to join the Welcome Dinner hosted by Prof. Steve Chung, the General Chair of 2021 VLSI-TSA Symposium. The dinner will start at 6:30 pm on April 19, 2021 at the Ambassador Hotel, the same venue as the symposium to be held. (*Subject to change in response to COVID-19 situation)

*A Special Note to Invited Speakers:

COVID-19 Watch: 2021 VLSI-TSA is planned for an in-person/on-site event. In the meantime, we will keep Hybrid meeting (same as 2020) if COVID-19 still keeps a threat to the convention, i.e., arranging overseas speakers to provide a pre-recorded video for presentation on condition that they render into travel restrictions.

☒ **I am willing to provide my video presentation to 2021 VLSI-TSA on the condition that there are travel restrictions in response to COVID-19 pandemic.**

4. Honorarium

We will offer invited speakers from USA West coast **USD 700** in cash onsite as the honorarium and registration fee waived to attend 2021 VLSI-TSA symposium. Due to COVID-19 situation, if you are not able to come to Taiwan in person, we will send the honorarium by remittance. Please sign your name below.

☒ I will need honorarium.

☐ I do not need honorarium.

Signature:  Date. 2020 (Y) 12 (M) 9 (D)

Please complete this form and send by email to Ms. Caroline Huang by **November 26, 2020**. Thank you!

Caroline Huang
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