DerChang kau
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EXPERIENCE

June 26, '95 – present, Intel Corporation, Santa Clara, CA, USA

January 2017 – present, Intel fellow, Director of 3D XPoint Memory Technology

Lead technology and design research team exploring novel memory architecture
Responsible for the strategic direction of atomistic memory devices and switches to build persistent memory architecture

April 2005 – December 2016, Senior Principal Engineer, Group Lead of 3DXP Technology

Led Intel memory technology from deep research stage of Phase Change Memory and Ovonic Threshold Switch to the inception of 1st generation 3D XPoint memory product.

April 2003 – March 2005, Principal Engineer, Group Lead of NOR Flash Technology

Led 65nm Self-Align Contact NOR Flash memory MLC device and architecture design. This memory cell and technology is commonly recognized as the de facto last generation NOR flash technology, which is still running in mainstream production.

April 2000 – March 2003, Senior Staff Engineer, SOC Technologist

Technologist and architect for 90nm Mixed Signal and Embedded Flash Technology. Managed DTCO with global collaboration from US, Europe and Israel design teams. Delivered world leading AFE and baseband processor for Blackberry; demonstrated the first Intel CMOS GSM radio. Co-led Technology Long-Range Strategic Planning of digital radio initiative.

June 1995 – March 2000, Staff Engineer

Delivered transistors in ¼µm NOR Flash Technology for automotive application. Awarded Intel IAA for Self-Aligned Floating Gate Technology of 130nm NOR Flash. Invented dual gate oxide process for logic transistors and high voltage transistors.

June 1, '87 – June 23, '95, Digital Equipment Corporation, Hudson, MA, USA

Individual contributor with 3 levels of career advances

Wide range of hands-on exposure from device design, layout, characterization, SRAM design, process development (clean, diffusion, implant, PVD, Silicide, Salicide, dry/wet etch), Frond-End Integration and Yield Improvement. Avid inventor and expert in high energy ion implantation beam line design, large angle ion implant device design and gate oxide hardening.

Education

Aug, '85 – May, '87: MSEE, Solid State Physics, Ohio State University, Columbus, OH, USA

Sep, '79 – May, '83: BSEE, Computer Engineering, Chung Yuan University, Chung-li, Taiwan

Reference upon requests