Emerging Memory Selector Devices

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***Abstract*—Selector devices are critical components in functional crossbar arrays of emerging nonvolatile memories. Both nonlinearity and asymmetry in device characteristics may enable device selection functions. A broad range of two-terminal devices are developed as selector; however, most of them still face great challenges to meet the performance requirements. Simulation of crossbar array characteristics based on selector device models and array design parameters help to assess selector device options and technology/design tradeoffs.**

Keywords-selector device; crossbar array; resistive switching memory; nonlinearity; asymmetry

I. INTRODUCTION

Nonvolatile memories (NVM) have become vital components in modern electronic systems for information processing and storage. While main-stream Flash memories are approaching their scaling limit, many novel memory concepts have emerged [1], as shown in Fig. 1. Promising examples include spin-transfer-torque RAM (STTRAM), phase-change memory (PCM), and resistive RAM (RRAM). Conventional memories (e.g., SRAM, DRAM, and Flash) are all based on transistors, which subject them to the benefits and limitations of CMOS scaling. In contrast, most emerging NVMs have two-terminal structures and may be integrated in high-density crossbar memory arrays. However, these two-terminal memory elements often have to be combined with so-called selector devices to be functional in memory arrays.

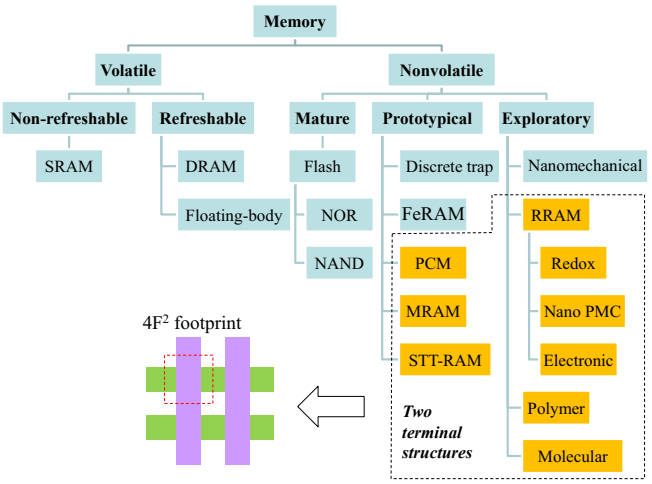

Figure 1. Memory taxonomy

This can be understood from the illustration of a crossbar memory array in Fig. 2. A device (in red) is selected by pulling up its wordline (WL) to V_{dd} and grounding its bitline (BL). Ideally, current should flow from V_{dd} to ground through the selected device, which is the selected path. In reality, the unselected devices form large number of sneak paths between V_{dd} and ground in parallel with the selected path. These parallel sneak paths reduce the effective voltage/current reaching the selected device, which may result in writing failures. The leakage current through these sneak paths may also dominate sensing voltage/current and make the selected device state (on/off) indistinguishable, causing reading failures.

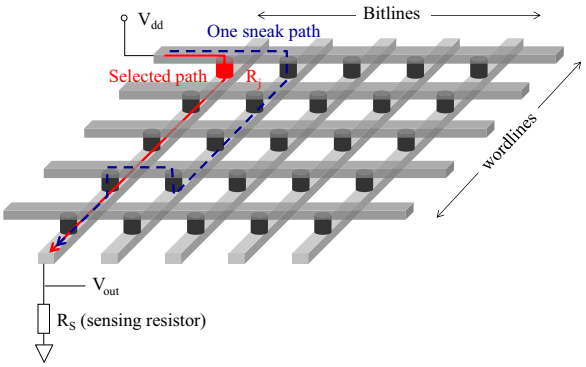

Figure 2. Illustration of a crossbar array

To avoid these failures, selector devices need to be inserted at every junction in a crossbar array to reduce the leakage through these sneak paths.

II. MEMORY SELECTOR DEVICES

A. Selector device characteristics

To understand what kind of device characteristics may enable device selection functions, it helps to highlight what make of sneak paths in a crossbar array, as shown in Fig. 3. Here device (i,j) between WLi and BLj is selected. Notice two features in all the sneak paths. First, leakage current through any sneak paths will pass three unselected devices in the direction of WL→BL, BL→WL, and WL→BL, i.e., sneak paths always comprise a "reverse-direction" segment. If devices with asymmetric characteristics (e.g., reverse resistance >> forward resistance) are inserted at every junction, leakage through sneak paths will be reduced by the reverse resistance

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while the resistance along the selected path will only increase by the small forward resistance. Second, voltage applied on a selected device is divided among multiple unselected devices along sneak paths, i.e., unselected devices typical have smaller voltage than the selected device. If nonlinear devices with higher resistance at lower voltage are inserted at every junction, sneak paths will also become effectively more resistive and leakage will be reduced.

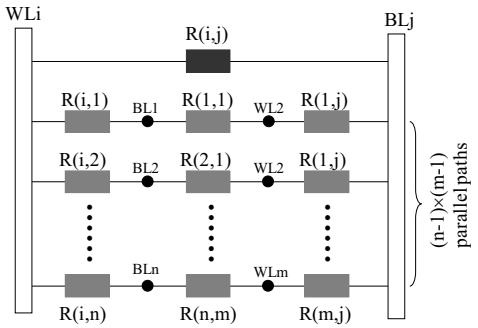

Figure 3. Illustration of sneak paths in a crossbar array

Therefore, both asymmetry and nonlinearity in device characteristics may reduce leakage through sneak paths and enable device selection functions.

B. Selector device options

Fig. 4 shows taxonomy of memory selector device options. Transistors are probably the best selector devices, with high maturity, large on/off ratio, and gate modulation capabilities. However, their large footprint limits the scalability of the memory cell and constrains their applications for high-performance space. Rectifying diodes provide asymmetry for device selection as discussed above. Si-diodes have been demonstrated as feasible selectors in crossbar arrays [2]; however, it requires high processing temperatures incompatible with many emerging NVMs. Oxide-based Schottky junction and hetero-junction diodes are more compatible with emerging memory processing, but they still fall far behind in terms of performance. Many devices could provide nonlinearity for device selection, either from transport mechanisms or creative structural engineering (e.g., complimentary structures).

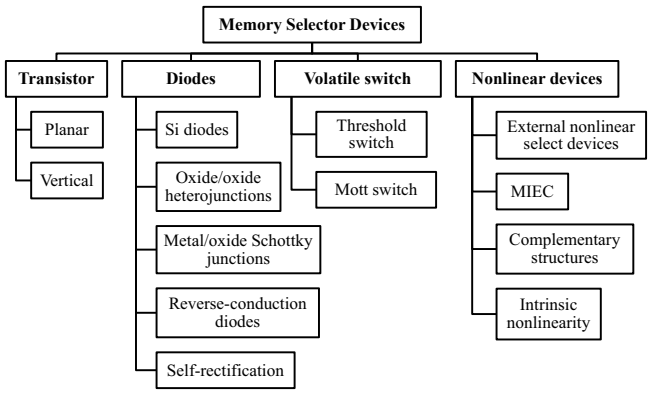

Figure 4. Memory selector device options

Volatile switching devices can also be used as memory selectors, by passing current through the selected path in their conductive state and blocking current through sneak paths in their high-resistance state. However, their switching properties have to be balanced with memory elements, which will be discussed later. Intrinsic asymmetry or nonlinearity in the property of memory elements may also enable "self-selecting" crossbar array designs without external selector devices.

III. Selector Device Performance Requirements

Functional selector devices have to meet certain performance requirements, which are determined by the applications and array design specifications.

A. Crossbar array figure-of-merit (FOM)

When reading a selected device in a crossbar array, its state needs to be clearly distinguishable from the sensing signal. When writing a selected device, sufficient voltage/current needs to be delivered to it without disturbing any unselected devices. It's also desirable that power/energy efficiency of both operations is maximized. The following key figure-of-merit (FOM) helps to measure crossbar array performance.

- *Sensing margin (SM)*: defined as the difference between the sensing signals (e.g., voltage) for the selected device in the on- and off-states.
- *Writing voltage margin (WVM)*: defined as the gap between the selected device voltage and the maximum disturbance voltage among unselected devices.
- *Operation efficiency*: defined as the ratio of the power consumed by the selected device over the total power provided by voltage sources.

B. Selector device parameters and requirements

To meet the array performance measured by FOMs defined above, there are a set of selector device parameters that need to satisfy certain requirements, as summarized in Table 1.

TABLE I. Selector Device Parameters

Parameters	**Requirements**
On/off ratio (or rectification ratio, nonlinearity ratio, *etc.*)	Sufficiently high for given memory element characteristics and target array size
On-current (or current density)	Sufficiently high for memory operation
Threshold voltage	Should be minimized
Scalability	Comparable with memory elements
Operation polarity	
Switching speed	
Endurance	
Manufacturability	Compatible with memory and CMOS

C. On/off ratio

The on/off ratio of selector devices determines the size of crossbar arrays that can be built. It is represented by the rectification ratio in rectifying diodes and the nonlinearity ratio of nonlinear selectors. For volatile switches, the on/off ratio is

defined as the ratio between the resistance in the blocking and that in conductive states. Notice that there are different definitions for selector device on/off ratio. In actual devices, this ratio is also not constant but voltage-dependent. Therefore, it is unrealistic to compare or assess selector devices based on a single value as their on/off ratio without considering the definition and applications. In memory arrays with parasitics (e.g., line resistance), the correlation between selector on/off ratio and maximum array size is not a simple analytical equation. Prediction of feasible array sizes solely based on selector on/off ratio is often over-optimistic. Many diode devices have demonstrated high rectification ratio (e.g., 10^8) at certain voltage range, as shown in Fig. 5 [2-9]. However, actual device working voltage may deviate from the voltages where the optimal on/off ratios were measured.

D. *Maximum on-current*

Maximum on-current of selector devices needs to be at least as high as the switching current of memory element. Many emerging NVMs, including STTRAM, PCM, and RRAM, require tens of μA for switching even at highly scaled device sizes. It is generally believed that current density over 1MA/cm^2 is needed for selector devices of emerging NVMs. As shown in Fig. 5, most demonstrated diode selectors are still unable to meet this target. The on-current is often limited by contact resistance rather than intrinsic conduction mechanisms of selector devices. Notice that the forward current density of some diodes in Fig. 5 only changes slightly between V = 1V and 0.5V. This is because their forward current is already limited by contact resistance at 0.5-1V. Contact resistance increases when device size scales down, which will only exacerbate the challenges of selectors when memory technology evolves. To meet the on-current requirement, it is necessary to utilize devices with high intrinsic conductivity and minimize contact resistance.

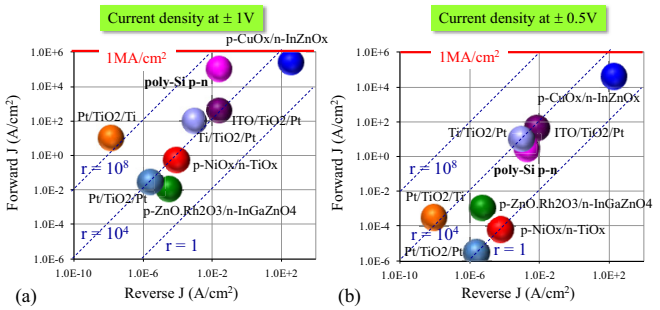

Figure 5. Forward vs. reverse current density of reported rectifying diode selectors at ±1V (a) and ±0.5V (b) [2-9].

E. *Scalability*

Selector devices have to be as scalable as memory elements to avoid compromising the scalability of emerging memories. Their key parameters (e.g., on/off ratio, on-current) should not deteriorate with scaling. Many selector devices demonstrated so far are fabricated at relatively large sizes, which provide little proof on their feasibility at the technology nodes where these emerging memories are likely to be adopted. Some study already indicates that enhanced tunneling in scaled diodes may eventually limit how small diodes can be made without sacrificing characteristics for selector applications [10].

F. *Operation compatibility*

The selector devices need to provide compatible operation polarity, speed, and endurance as the memory element. For volatile switch as selector devices, their switching voltage and on/off resistance levels also have to be balanced with the corresponding parameters of the memory element to make the 1S1R (1-selector-1-resistor) combination functional. Fig. 6 illustrates a load-line analysis for a 1S1R structure with the switching I-V loop of a volatile switch selector and the low-resistance-state (LRS) of a linear memory element. At the initial R_H state, the selector obtains voltage above V_{th} to switch to R_L state. In Fig. 6(a), after switching the selector maintains a voltage above V_{hold} and stay in the R_L state to allow the access to the memory element. However, if the V_{hold}-V_{th} window is too small as shown in Fig. 6(b), selectors will not remain in the R_L state after switching because their post-switching voltage falls below V_{hold}. Therefore the 1S1R combination in Fig. 6(b) will not work. Operation compatibility constrains selector device choices for different emerging memories.

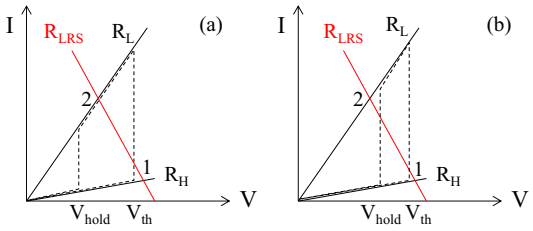

Figure 6. Illustration of functional (a) and non-functional (b) combinations of a volatile switch selector and a linear resistive switching memory element.

IV. A CASE STUDY: NONLINEAR DIODE SELECTOR

Bi-directional nonlinear diodes as selector devices work for both unipolar and bipolar memory elements. Nonlinearity may originate from transport mechanisms, e.g., tunneling across thin dielectrics. It is relatively easier to control than interface-induced rectifying behaviors that only work for unipolar memories. This section will use a demonstrated nonlinear selector device to quantify the impact of selector device properties on the crossbar array design and performance.

A. *Nonlinear bi-directional diode characteristics*

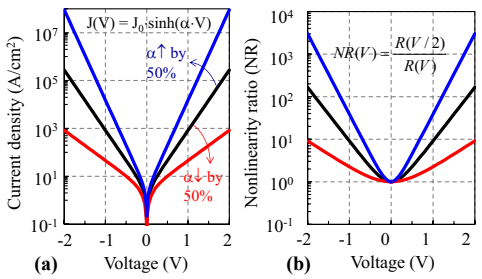

Figure 7. Simulated characteristics of a bi-directional nonlinear diode selector (TaN/SiN$_x$/TaN) reported in [11].

Fig. 7 simulates a bi-directional nonlinear diode selector reported in [11]. The I-V characteristics can be described by hyperbolic functions. By adjusting the pre-factor (J_0) and exponent coefficient (α), the black curve fits well with experimental I-V characteristics in [11]. Parameter (α) has strong impact on diode I-V and nonlinear ratio (defined at full bias and half bias). This selector device model will be used in the simulation of a 4kb (64×64) crossbar memory array based on a method developed in [12]. In all the simulations, the memory element is assumed to have an on/off ratio of 10 and on-state resistance of 10kΩ. Since the crossbar array performance depends on selected device location and resistance patterns in the array, worst-scenario analysis is adopted here for feasibility assessment, i.e., the selected device is located furthest from voltage sources and the resistance patterns that maximize sneak path leakage are assumed.

B. *Writing of a 1S1R crossbar array*

Line resistance causes voltage decay when current flows from V_{dd} to ground, which is simulated in Fig. 8 (dashed black curve) for a selected WL with 1024 junctions along the line. Due to this voltage decay, large arrays with high line resistance are more susceptible to switching failures and writing disturbance. Partial bias schemes (dashed red curve) reduce line voltage decay by supporting unselected lines to non-zero bias (e.g., $V_{dd}/2$). Nonlinear selectors in 1S1R arrays significantly reduce this voltage decay for both full-bias and partial-bias schemes. This improvement is attributed to the reduction of leakage through sneak paths by selectors.

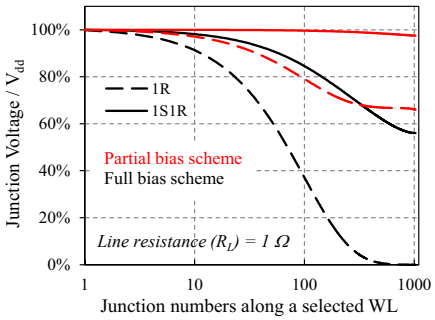

Figure 8. Line resistance induced voltage decay is reduced by selectors.

Writing voltage margin (WVM) of a 4kb crossbar array is calculated in Fig. 9 for different line resistance (a) and exponent coefficient α of selectors (b). WVM of an array without selectors diminishes to 0 at R_L of ~ 4Ω. With nonlinear selectors, the window between the selected junction voltage and the maximum unselected junction voltage remains almost constant up to R_L = 10Ω. The actual voltage of the memory element V_R (black curves) is much smaller than the junction voltage V_{1S1R} (red curves) due to the voltage dividing effect of selectors. Although the WVM of 1S1R arrays is smaller than that of 1R arrays at low R_L, it is almost unaffected by increasing R_L. As shown in Fig. 9b, using selectors with higher α parameters (i.e., stronger nonlinearity) helps to improve both selected device voltage and WVM by reducing the effective resistance of selectors and their voltage dividing effect in 1S1R structures.

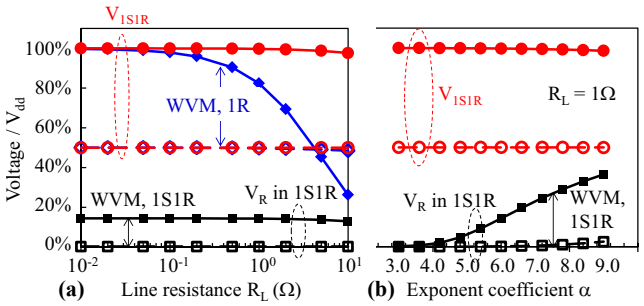

Figure 9. Writing voltage margin as a function of line resistance (a) and exponent coefficient of nonlinear selector (b). Solid symbols are values for the selected device and empty symbols are maximum values of unselected devices.

C. *Sensing of a 1S1R crossbar array*

Worst-scenario sensing margin (SM) of a 4kb crossbar memory array is calculated in Fig. 10 for 1S1R and 1R arrays. The output voltage (V_{out}) in the voltage-divider sensing scheme (Fig. 2) needs to be distinguishable for the selected memory element in the on- and off-states. With nonlinear selectors, the 1S1R array maintains positive SM although SM decreases with increasing R_L. However, without selectors, SM of 1R arrays is essentially 0 even at low R_L. This is because a 10× on/off ratio of memory elements is not sufficient to sustain positive SM without selectors, in the presence of large number of sneak paths in a 4kb array.

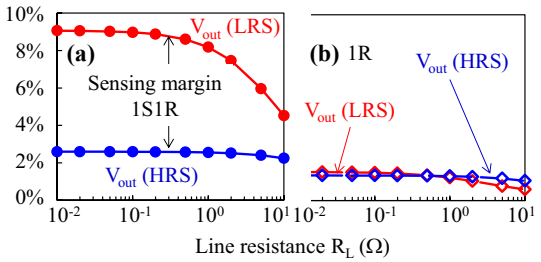

Figure 10. Worst-scenario sensing margin of 1S1R (a) and 1R (b) arrays.

The SM in the range of 2%-7% for a small 4kb array is much smaller than the prediction in some reports based on analytical solutions and constant nonlinearity ratios [13]. This large discrepancy highlights the effects of over-simplification in crossbar array analysis without considering line resistance and the voltage-dependent selector characteristics.

V. SUMMARY

Selector devices are indispensable in functional memory arrays of emerging NVMs. Although many two-terminal devices have been proposed as selector devices based on nonlinearity or asymmetry in their characteristics, it is still a great challenge to meet the performance requirements imposed by memory characteristics and array design targets. A case study of crossbar arrays with nonlinear selectors reveals the impact of selector device properties on the array operation and performance. The promise of scalable emerging NVM arrays hinges on the availability and quality of functional selector device solutions.

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