Vertical-Transport Nanosheet Technology for CMOS Scaling beyond Lateral-Transport Devices

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Abstract **-** We demonstrate, for the first time, Vertical-Transport Nanosheet (VTFET) CMOS logic transistors at sub-45nm gate pitch on bulk silicon wafers. We show that VTFETs present an opportunity to break the Contacted Gate Pitch (CGP) barrier faced by Lateral-Transport FETs. VTFETs offer scaling relief for electrostatics and parasitics by decoupling key device features from CGP-scaling roadblocks. First, nMOS/pMOS VTFET electrostatics are reported at sub-45nm gate pitch with SS = 69/68 mV/dec and sub-30mV DIBL. Well-behaved short channel characteristics with Si/SiGe source and drain are demonstrated in hardware. Symmetric device characteristics for SS and DIBL are achieved (with process optimization). Vertical nanosheets are utilized rather than vertical nanowires [1,2] for improved performance and area scaling. Functional ring oscillators demonstrate the excellent effective capacitance (Ceff) scaling advantages of VTFET nanosheets. Logic area scaling is furthered by use of Zero Diffusion Break (ZDB) isolation to eliminate dummy gates. Innovative I/O FET device design and hardware characteristics are shared.

Keywords: Vertical Transport Nanosheet FET, VTFET, Nanosheet, FinFET, Scaling, Zero Diffusion Break, ZDB.

Introduction

Vertical-Transport Nanosheets (VTFET), in which the transport path of the MOSFETs is orthogonal to the wafer plane, can enable scaling to advanced logic nodes by directly addressing the fundamental pitch scaling constraints that limit Lateral-Transport FETs (LTFET). In LTFETs, the gate length (Lgate), source/drain length (Ls/d), two spacers (2 x Tspacer), plus a tolerance, must fit within a single Contacted Gate Pitch (CGP). Each of these components is constrained against further scaling, presenting a vanishing design point in scaling of CGP. Inspired from trench-based DRAM [3,4] vertical access transistors, VTFET architecture allows for the independent optimization of Lgate and Tspacer by rotating these components out of the CGP plane to enable longer Lgate and larger Tspacer, thereby providing excellent electrostatics, increased contact area, and significantly reduced Ceff. One must address, however, the loss of Weff/Wfoot-print, or Fin-Effect. To address these issues, we examine circuit comparisons with matched-footprint layouts and include the VTFET advantage of Zero-Diffusion Breaks (ZDB).

Gate Pitch Scaling Challenges and Solutions

Lateral-Transport CMOS logic density advances, to the first order, can be represented by the product of Interconnect Pitch and Contacted-Gate-Pitch (CGP). In lateral-transport architectures, such as planar, FinFET, and Nanosheet FETs [5], there is a basic constraint that the sum of Lgate, 2xTspacer, and Ls/d as well as some variation (tolerance) in these components, add up to gate pitch, as illustrated in Fig. 1.

At present, state-of-the-art nodes are approaching scaling limits for Lgate, driven by electrostatics (short-channel effects), Tspacer, limited by drain-to-gate TDDB, and Ls/d, limited by specific contact resistivity, as shown in Fig. 2. It is helpful to illustrate this scaling challenge by examination of the operating-voltage range as a function of CGP, shown in Fig. 2. For any given CGP, Lgate, Tspacer, Ls/d can be traded-off against one another, however, when constrained by reasonable values for drive current vs. off-current, one invariably arrives at solutions that look roughly like that shown in Fig. 3. Vmax is rapidly diminished, and Vmin slowly increases, resulting in a vanishing window for Vdd as CGP is reduced towards ~40nm for Lateral FETs. Product performance demands may additionally push the CGP limit higher. The VTFET architecture enlarges the operating voltage range at ~50nm CGP and the advantage increases with smaller pitches.

In this paper, we suggest that one means of continuing CMOS density scaling is to orient the transport direction of the channel current out of the plane of the wafer, orthogonal to the CGP direction, and construct a Vertical-Transport FET. For a vertical transport configuration, the Lgate and Tspacer dimensions are decoupled from the gate pitch and the S/D contacts are removed from the CGP budget (Table 1). Thus, the sizes of Lgate, Tspacer, and Lcontact can be independently optimized for improved power and performance. Gate-stack thickness (Tgate) is a new pitch scaling component that must be considered for VTFETs.

VTFET Design Characteristics

Cross-sectional TEMs of VTFET nanosheet transistors from sub-45nm CGP hardware along with an example process flow are shown in Fig. 4. For design flexibility, the source can be located at either the top or bottom. The VTFET transistor includes low resistance Si/SiGe S/D and separate contacts are used for connection to the bottom S/D, top S/D, and gate. Innovative post gate stack integration is enabled for low temperature gate stack compatibility. VTFET devices also feature a simplified single metallization middle of line process integration flow.

Key VTFET device and circuit performance attributes are compared to FinFET at the same footprint and at an aggressive sub-45nm gate pitch. Adding lateral-transport Nanosheet to the comparison is best done once volume production has begun. VTFET nanosheet total device parasitic resistance and RO circuit capacitance is significantly improved over the FinFET reference via simulation (Fig. 5). VTFET provides a significant performance advantage over scaled FinFET, at an aggressively scaled CGP, due to VTFET maintaining good electrostatics and parasitics while FinFET performance is impacted by severe scaling constraints (Fig. 6). VTFET nanosheets also have improved performance over vertical nanowires due to the significantly higher total Weff of nanosheets.

Lateral-Transport FET circuit density is affected by Double, or, in some cases, Single-Diffusion Breaks (DDB, SDB), required for circuit isolation. With gate dimensions approaching 10nm, scaling SDB to advanced nodes can be challenging, since the isolation is accomplished via a single dummy gate. VTFET devices employ STI for adjacent circuit isolation to achieve a Zero Diffusion Break (ZDB) isolation (Fig. 7) with no loss of active-gate pitches. Fig. 8 shows TEM images from fabricated VTFET devices featuring compact ZDB with self-aligned Active Area and gate features. ZDB formation is compared structurally and electrically vs DDB in Fig. 9 and meets the isolation criteria at higher circuit density.

FinFET Weff quantization is becoming more challenging as high-density libraries move to two, or even one Fin per transistor. VTFET nanosheet length (length ≅ Weff/2) is enabled by EUV single exposure lithography, offering design flexibility for drive, leakage, and capacitance tradeoffs. In the inverter example shown in Fig. 10, three nanosheets are employed. When lower drive or reduced area is desired, e.g., for power/leakage/area savings, the length and/or number of the VTFET nanosheets can be reduced.

VTFET Electrical Characteristics

Excellent Vertical-Transport nanosheet electrostatics are obtained at sub-45nm CGP as shown in Fig. 11 with nFETs achieving SSat=69nV/dec, and pFETs achieving 68 mV/dec respectively. Both polarity devices achieve sub-30mV DIBL. One of the unique aspects of VTFET is S/D resistance asymmetry. Top and bottom S/D are formed in separate modules, unlike conventional self-aligned gate processes. Comprehensive characterization of S/D asymmetry has enabled significant improvement in device symmetry through process optimization. Fig. 12 shows forward and reverse characteristics of saturation ON resistance (Rsat). Both forward and reverse Rsat and Rsat variability have been improved by top and bottom spacer thickness and dopant placement (junction overlap) optimization. Rsat is defined as Vds / Iodsat, where Iodsat is saturation current with constant gate overdrive voltage. The gate stack is a key attribute determining transistor performance. Both interfacial layer (IL) optimization and gate stack engineering have been implemented to provide an overall transistor DC performance improvement.

Innovative I/O device FETs using a combination of vertical and horizontal channels to optimize density, performance, and process compatibility are integrated with VTFET logic devices. Fig. 13 shows the I/O FET schematic and cross section TEM along with the Id-Vg FET characteristics. This design has the freedom to adjust the effective device Lg by modification of the horizontal channel length. Moreover, threshold voltage can also be adjusted by conventional channel doping along with substrate bias.

Functional 101-stage inverter ring oscillator circuits are demonstrated at sub-45nm CGP via the waveforms shown in Fig. 14(a). These results demonstrate both the technological maturity of the VTFET device architecture and confirm the important VTFET capacitance scaling advantage compared to Lateral FETs (Fig. 14(b)). The Ceff models predict a significant reduction (~ 50%) over the scaled Lateral (FinFET) reference. Device Architecture driven circuit level capacitance reduction enables higher frequency and increased circuit count for product performance improvements. Hardware based Ceff extracted from the ring oscillator circuits show good agreement compared to the models and validate the significant Ceff reduction of Vertical -Transport Nanosheet devices.

Conclusion

We have fabricated and characterized the first CMOS VTFET Nanosheet logic devices at sub-45nm Gate Pitch on bulk Si wafers. We have shown that VTFET nanosheets can overcome the gate-pitch-scaling limits faced by lateral transport devices and offer excellent electrostatics and dynamic performance at sub-45nm CGP. VTFET nanosheet electrical results show excellent SS, DIBL, and symmetric device operation. At fixed footprint and aggressively scaled gate pitches, VTFET nanosheets can deliver increased device drive due to a combination of good electrostatics, low parasitic losses, and area savings from the use of zero diffusion breaks. VTFET Nanosheets can avoid Lateral FET scaling limits to deliver an enhanced operating voltage range. VTFET Nanosheets can also provide greater drive strength and flexibility compared to FinFETs and Nanowires. The intrinsic benefit of VTFET circuit capacitance reduction (~ 50%) over scaled Lateral FET has been demonstrated in hardware. Moreover, this Ceff advantage is expected to grow at smaller device dimensions. All these above advantages make Vertical-Transport Nanosheets (VTFETs) a strong candidate for scaling beyond the limits of Lateral-Transport FET architectures.

Acknowledgements

This work was performed by the Research Alliance teams at various IBM Research and Development Facilities. We would like to thank for their executive support: T.C. Chen, M. Khare, D. W. Kim, K. Rim and E. Nowak. We also thank the GLOBALFOUNDRIES research team for their contributions prior to December 2018.

References

[1] D. Yakimets, et al., IEEE Trans. Electron Devices, p. 1433-1439 (2015)
[2] A. Veloso, et al., VLSI Technical Digest, p. 1-2 (2016)
[3] U. Gruening, et al., IEDM, pp. 25-28 (1999)
[4] C.J. Radens, et al., IEDM pp. 349-352 (2000)
[5] N. Loubet, et al., VLSI, pp. 230-231 (2017)

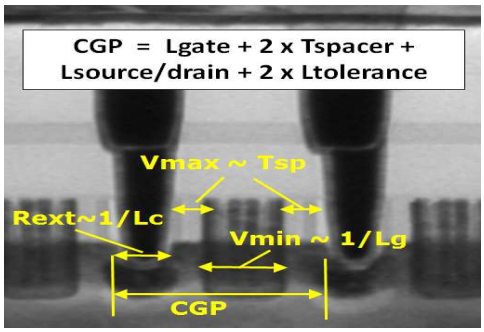

Fig. 1: Lgate, Tspacer, Ls/d, together with tolerance must sum to the Contacted-Gate Pitch (CGP). TDDB from Gate-to-Drain limits Vmax while Ssat and DIBL (Lgate/Dfin) drive Vmin.

Table 1: Maximum Feature Size limited by CGP

	Lgate	Tspacer	Lcontact	Tgate
Lateral Transport	Limited (~0.3xCGP)	Limited (~0.1xCGP)	Limited (~0.3xCGP)	Limited
Vertical Transport	Not limited	Not limited	Limited (~0.7xCGP)	Limited (~0.25xCGP)

VTFETs move Lgate and Tspacer out of the CGP plane, enabling improved optimization; Lcontact can be relaxed to ~0.7 X CGP. Gate-stack thickness (Tgate) is a new pitch scaling component that must be considered for VTFETs.

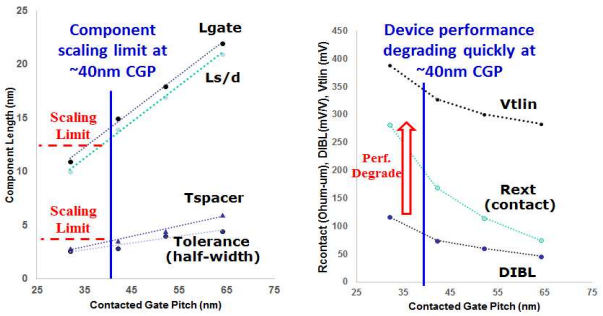

Fig. 2: LTFET scaling must balance Lgate, Tsp, and Ls/d (left), driven by Ssat, Rext, and spacer TDDB. Corresponding DIBL, Vtlin, and Rext are shown (right).

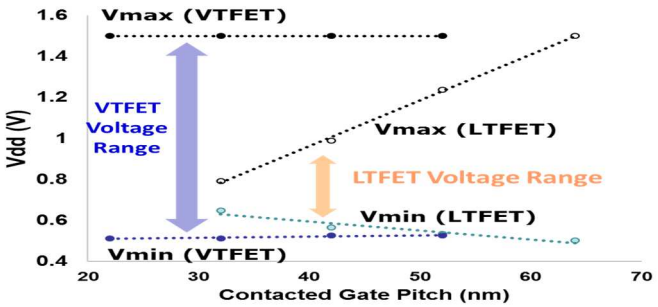

Fig. 3: Lateral-Transport FET operating voltage range shrinks with scaling CGP. Increased Vt (to maintain Ioff) drives increased Vmin while Tspacer drives Vmax (TDDB). Vertical-Transport FET architecture opens up the operating voltage range.

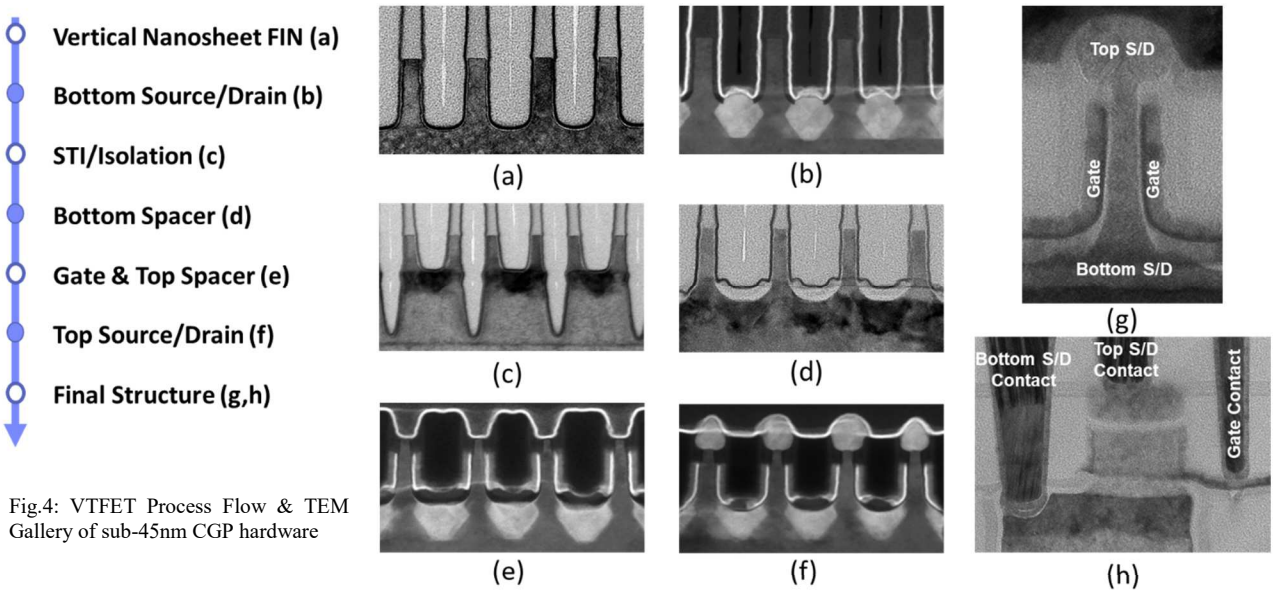

Fig.4: VTFET Process Flow & TEM Gallery of sub-45nm CGP hardware

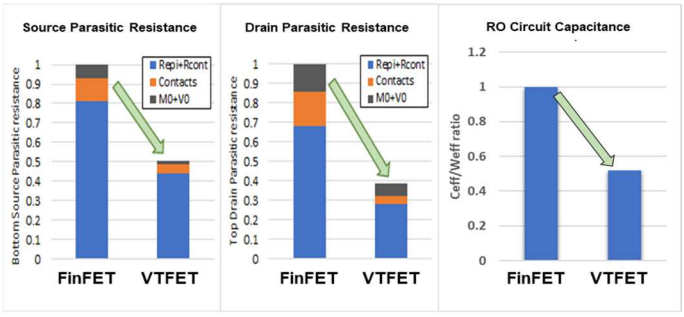

Fig. 5: Simulated device parasitic resistance and circuit capacitance across device architectures

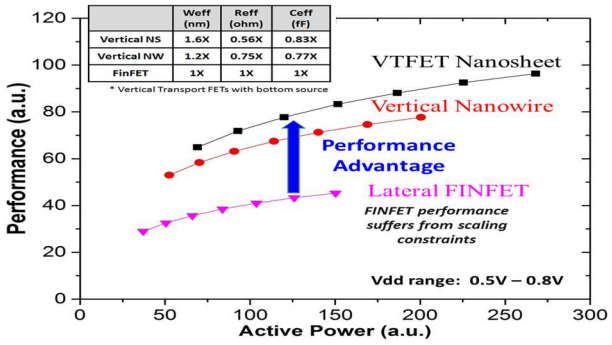

Fig. 6: Simulated Power vs Performance device comparison.

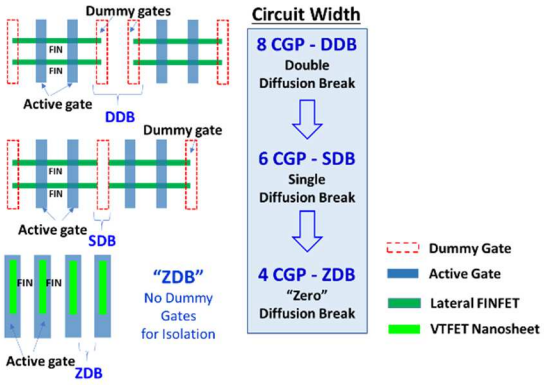

Fig. 7: Lateral transport FETs use Double or Single Diffusion breaks which increase chip area due to the need for dummy gates. Vertical-Transport FETs can reduce chip area by using STI isolation for a Zero Diffusion break (ZDB) solution.

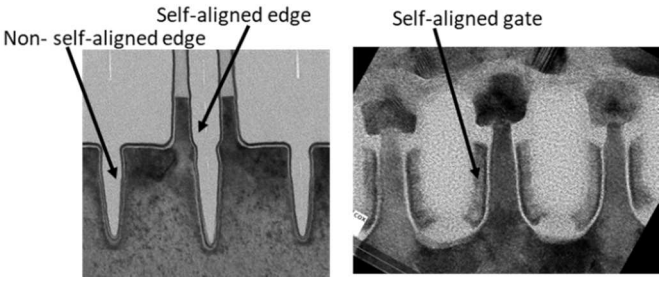

Fig. 8: Cross section TEMs showing self-aligned/non-self-aligned Active Area edges formed from ZDB along with self-aligned gate formation at sub-45nm CGP.

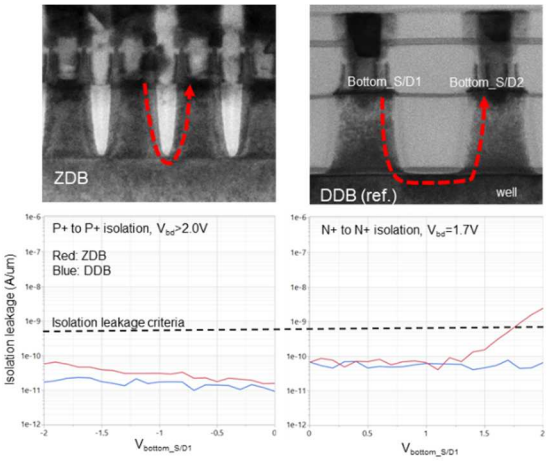

Fig. 9: TEM of Zero Diffusion Break (ZDB) vs DDB with electrical isolation results meeting leakage targets at sub-45 nm CGP.

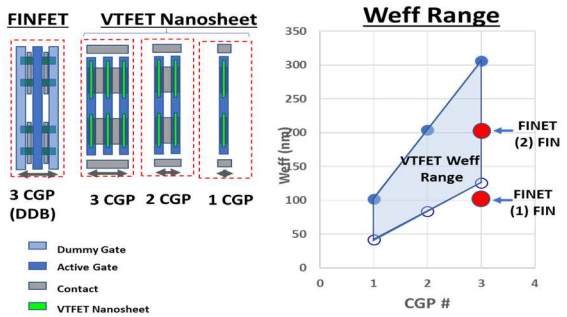

Fig. 10: FINFET Weff is quantized to either a 1 or 2 fin solution (Weff = N*(Weff/Fin)). VTFET Weff can be continuously tuned by changing FIN length and/or flexibly choosing the number of CGPs (FINs) in cell width direction.

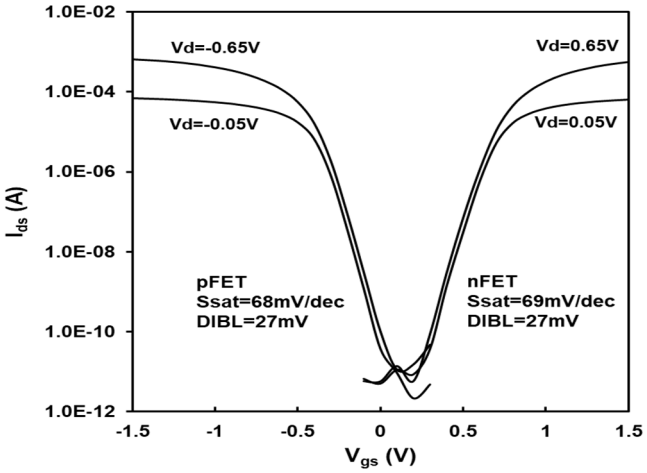

Fig.11: Id-Vg characteristic from sub-45nm CGP devices.

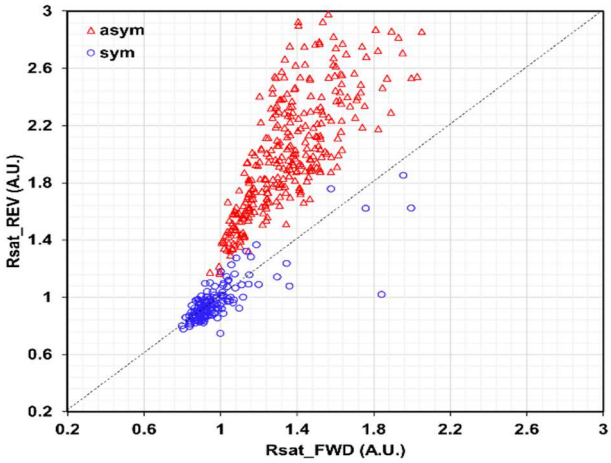

Fig.12: Rsat forward vs reverse characteristics from sub-45nm CGP devices.

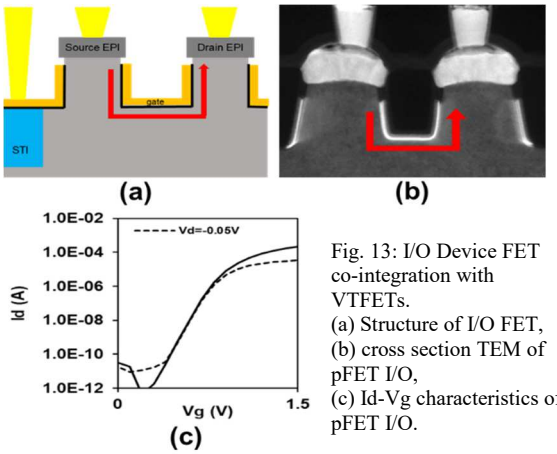

Fig. 13: I/O Device FET co-integration with VTFETs.
(a) Structure of I/O FET,
(b) cross section TEM of pFET I/O,
(c) Id-Vg characteristics of pFET I/O.

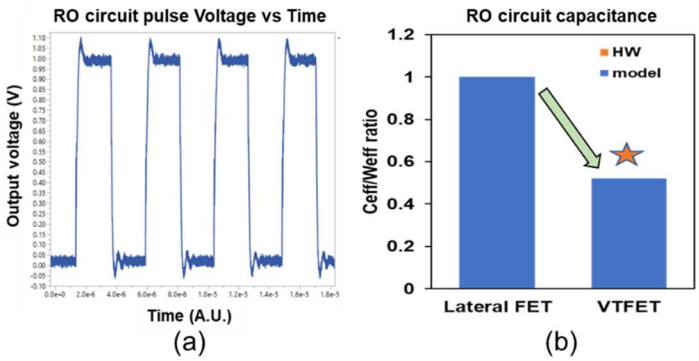

Fig.14: (a) Waveform from 101-stage VTFET Ring Oscillator (b) Ceff comparison of Lateral and VTFET architectures. VTFET circuit Ceff is significantly improved (~50%) over FINFET reference. Sub 45-nm CGP VTFET hardware confirms the Ceff advantage over lateral FETs and is close to model estimates.