2T0C electrical assessment

Attilio Belmonte

imec partner technical week

ACTIVE MEMORY

R105

NOW IN COURSE:

2T0C electrical assessment

Attilio Belmonte

OPEN TO:

Globalfoundries, Intel, Sony, TSMC, Samsung, Micron, SKHynix, Qualcomm, Kioxia, Western Digital, Huawei, KU Leuven, UGent

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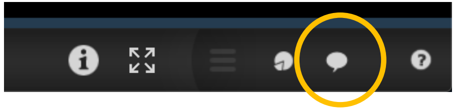
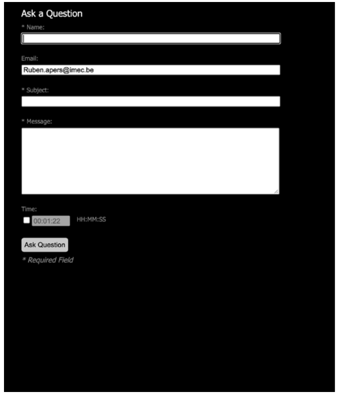
If you have questions?

3 min Q&A slot at the end of each presentation

Online Viewers

You can post your questions during the presentation by clicking on the 'text balloon'





The session chair will handle all questions 'Live' at the end of the presentation.

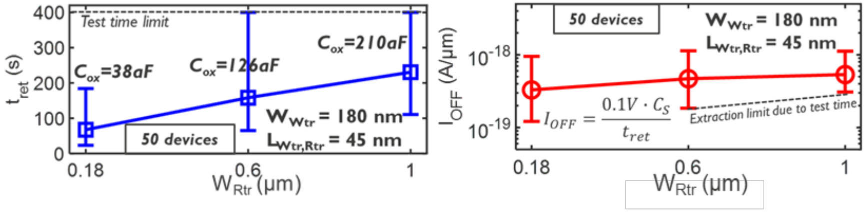
If you are watching in delay, you can still post your questions. These questions will be answered by email.

6-months progress

300-mm FRONT-GATED IGZO TRANSISTORS

PTW April 2021

2T0C retention & I_{OFF}

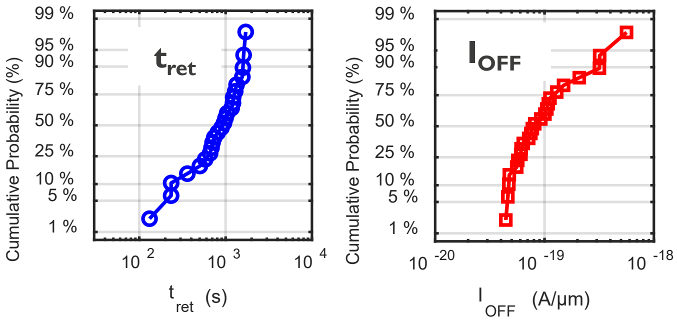


- 2T0C implementation for Gate-Last devices
  - Median retention time > 900s for C_{ox}=127aF (Gate-Last with oxygen-tunnel)
- First assessment of 2T0C retention for spinel and ALD a-IGZO

2T0C Gate-First structures:

- First reliable assessment of:
  - retention time →~ 150s for C_{ox}=126aF
  - I_{OFF} = 3x10^{-19}A/μm

Gate-Last with oxygen tunnel



PTW October 2020

Outline

- Introduction: Previous 2T0C results on Gate-First Devices
- 2T0C results in Gate-Last devices
  - Effect of oxygen-tunnel on retention / off-current
- Gate First: 2T0C structures with different IGZO phase / deposition method
  - CAAC / Spinel IGZO
  - ALD a-IGZO
- Conclusions

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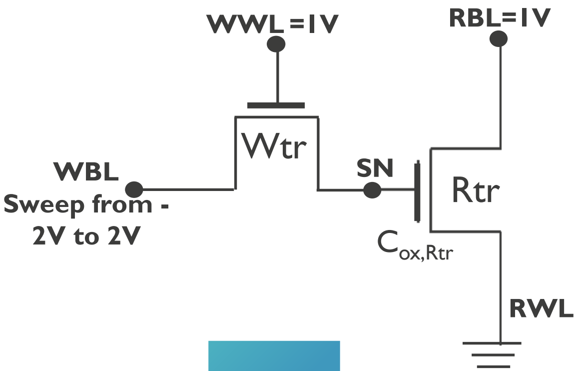
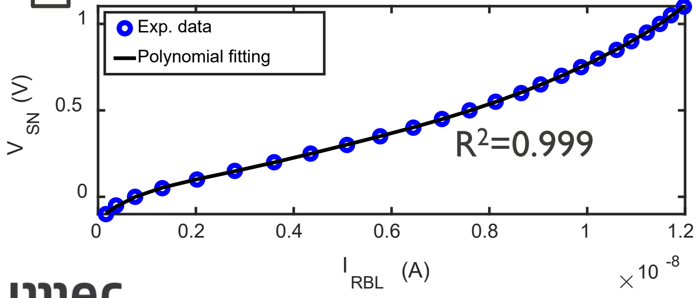
Retention assessment method

Indirect monitoring of the storage-node voltage evolution

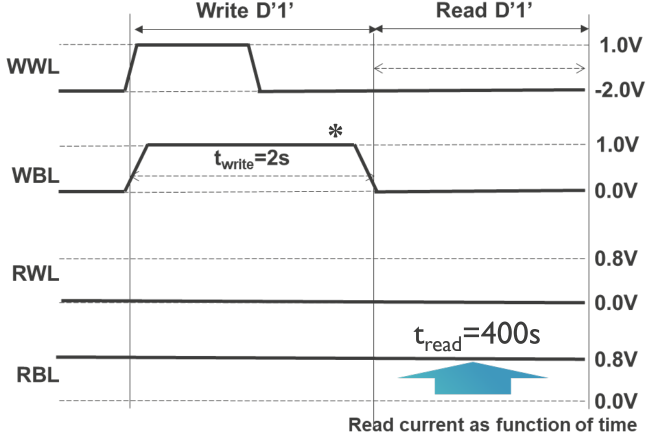
1 I_{RBL}-V_{SN} curves collection



2 Polynomial fitting of experimental I_{RBL}-V_{WBL}

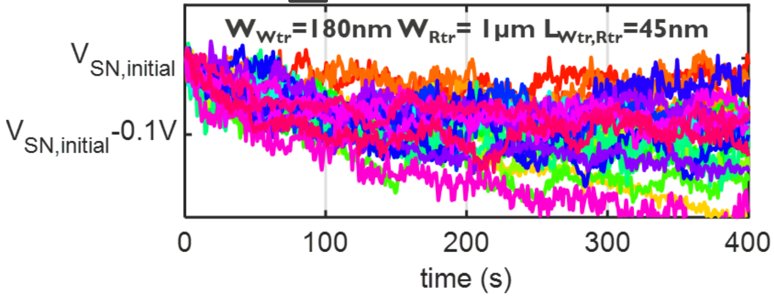


3 Write/Read Timing Diagram



*WBL=1V for 1s after WWL transition: Avoiding C discharge during WWL transition

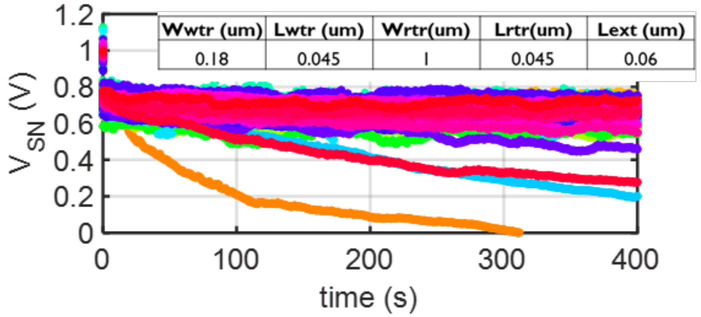
4 Retention test

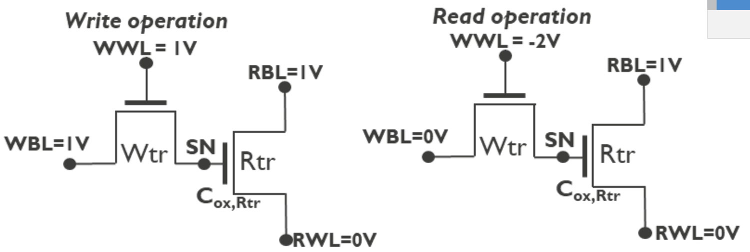


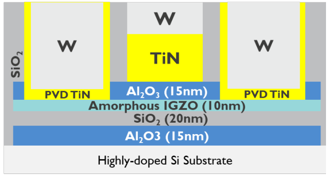
I_{RBL} is translated into V_{SN} by the polynomial fitting

Retention test: retention time scales with C_{ox}

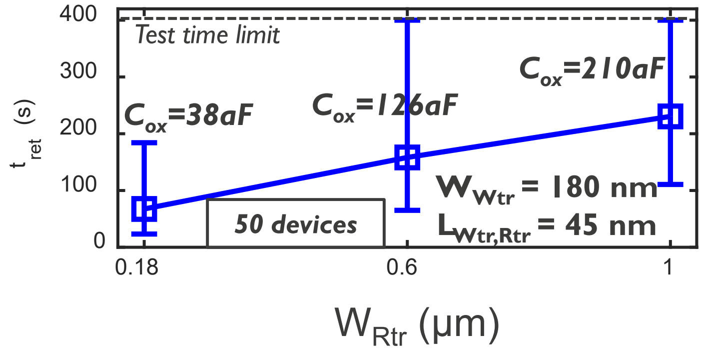
Retention assessment - 50 devices tested





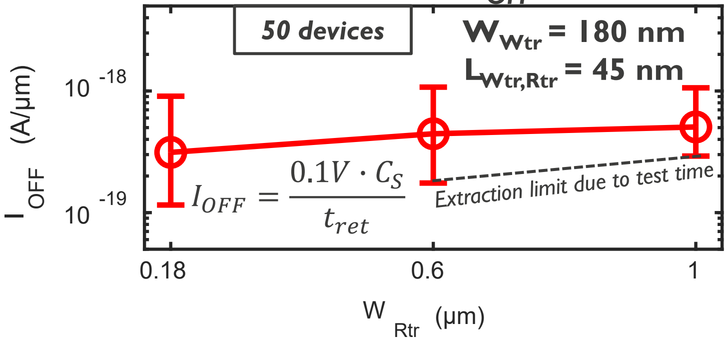


Retention time statistics



Extracted I_{OFF}

R104, PTW 10/2020
A. Belmonte et al., IEDM 2020

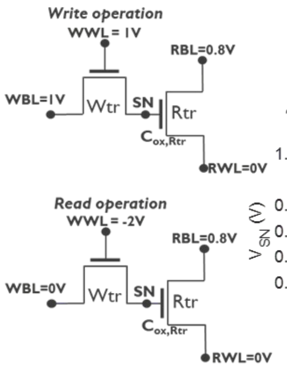


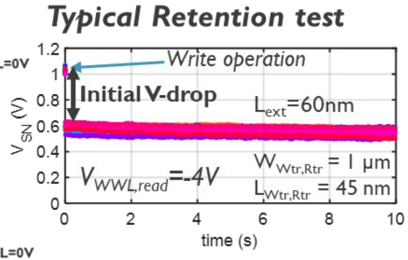
Median t_{ret} **>60s** achieved for C_{ox}=38aF

W_{Rtr}=1µm and L_{Rtr}=45nm → **>25% of the bits show t_{ret}>400s**

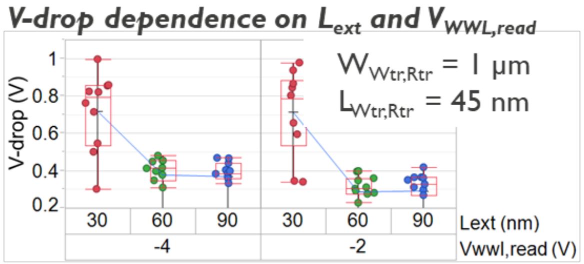
High gate-drain capacitance may hinder 2T0C retention assessment in Gate-Last

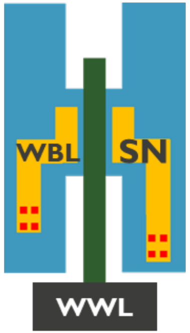
PTW 10/2020 R104





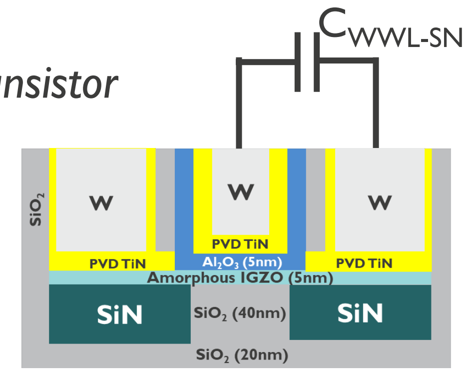
Initial V-drop always observed in the write/read transition





- Strong dependence of V-drop on $\mathbf{L_{ext}}$ **and** $\mathbf{V_{WWL,read}}$
- Capacitive coupling between SN and WWL
  → V_{WWL} transition from 1V to -2V induces partial SN discharge

Write Transistor



C_{GD} is expected to be higher in Gate-Last configuration
→ C_{GD} increases for thinner gate dielectric

Low V_{SN} after the transition between write and read?

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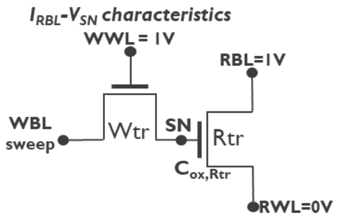
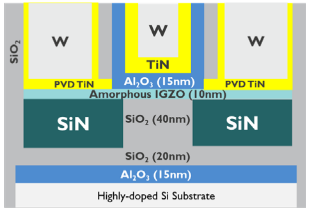
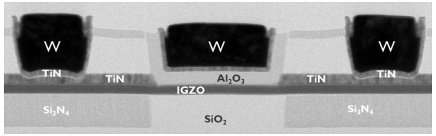
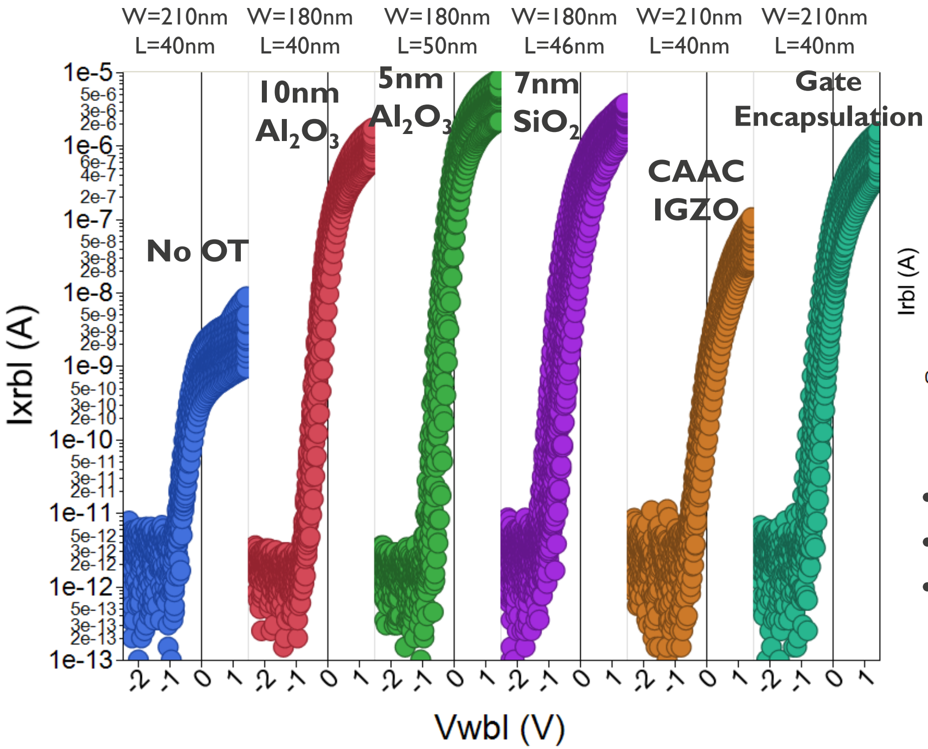
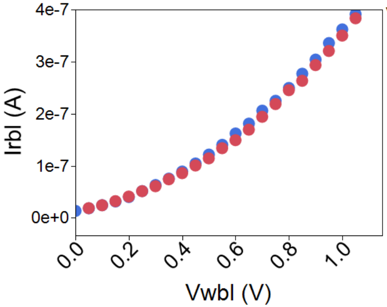
Id-Vg characteristics of read transistors











RBL → Rtr drain
$V_{WBL}=V_{SN}$ → Rtr gate

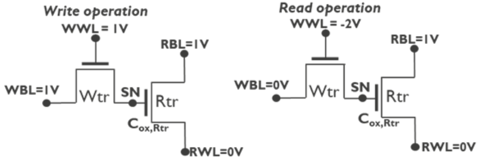
- Anneals were optimized to have similar V_{th} in all split
- Gate-Last reproducibility observed also for 2T0C structures
- Slight V_{th} degradation after 400-s stress on read transistor
  - → Polynomial fitting of a single I_D-V_G may be misleading
  - → Weighted average between the two I_D-V_G curves*

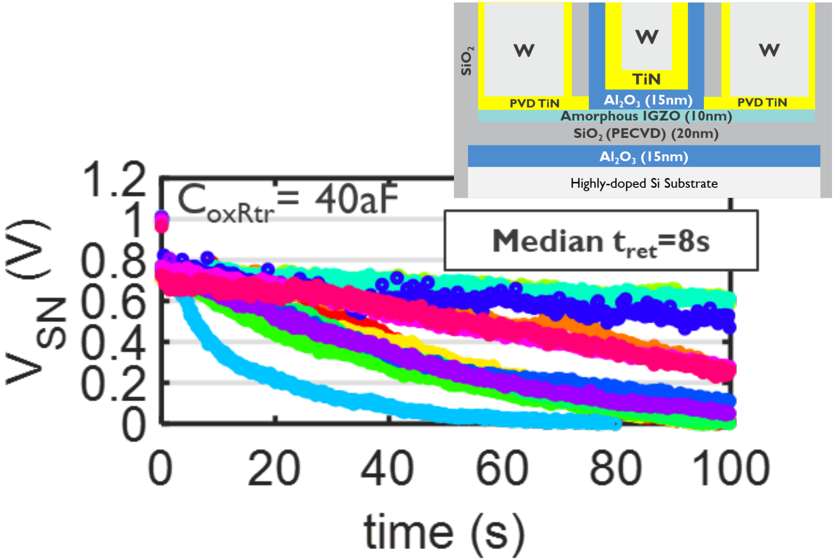
* See backup slides

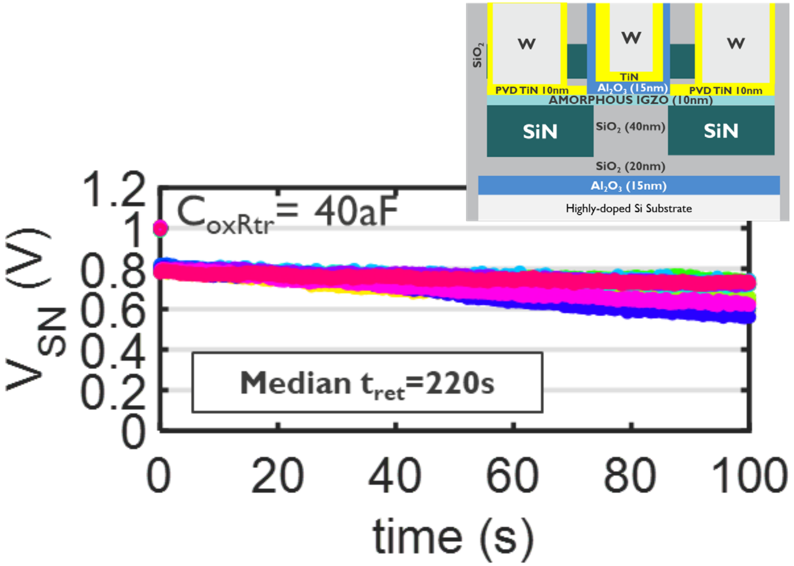
Effect of Oxygen Tunnel on 2T0C retention

W=210nm - L=40nm

25 devices – different colors → different dies

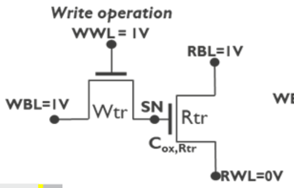


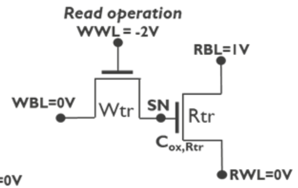




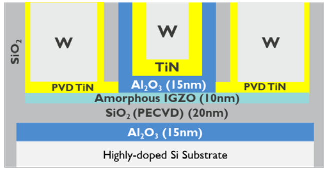
Strong improvement in 2T0C retention thanks to the oxygen tunnel
→ More efficient defect passivation in the channel

Benchmarking against reference Gate-First



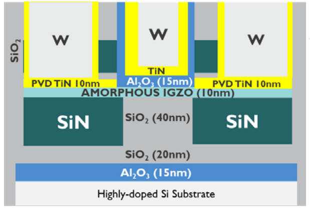


Gate-Last



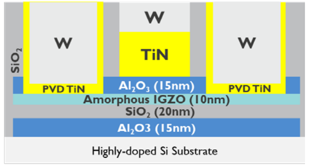
W=210nm
L=40nm
$C_{ox,Rtr}$=40 aF

Gate-Last - OT

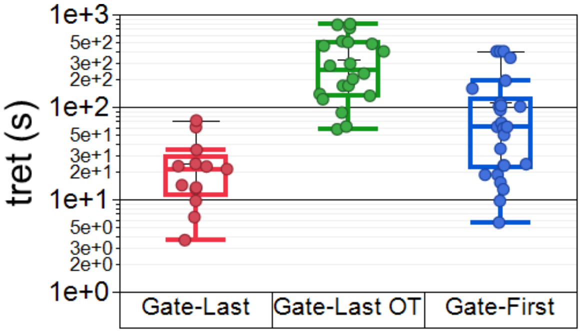


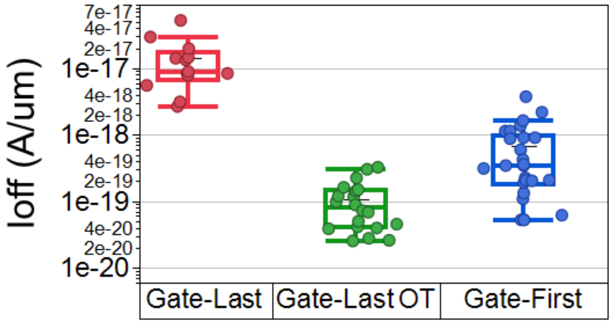
W=210nm
L=40nm
$C_{ox,Rtr}$=40 aF

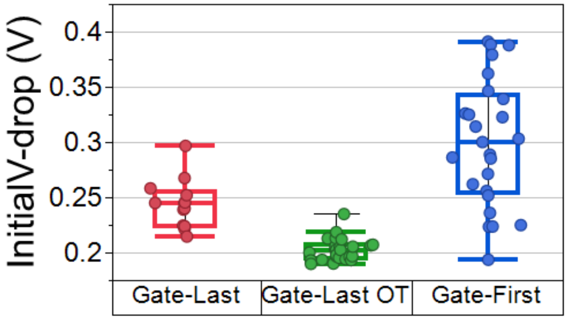
Gate-First



W=180nm
L=45nm
$C_{ox,Rtr}$=38 aF

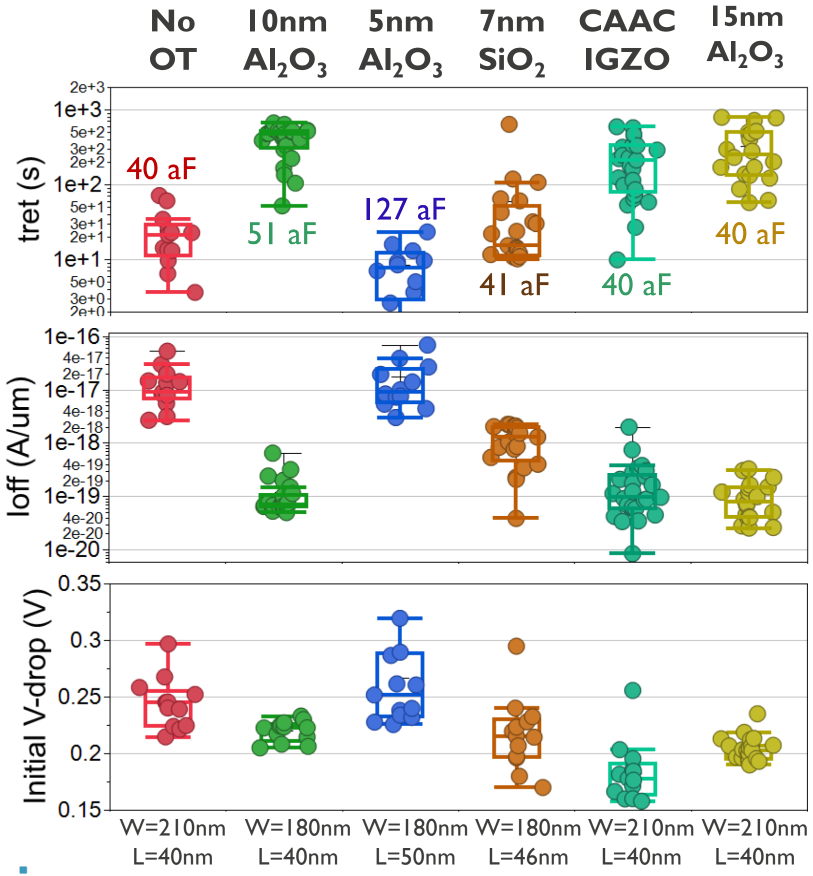


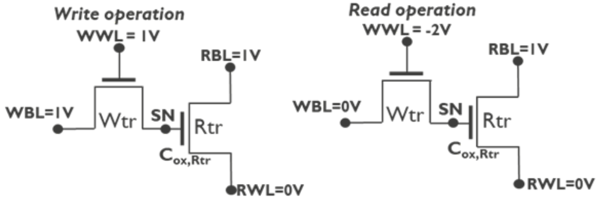


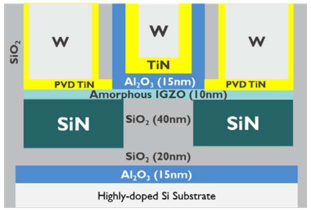


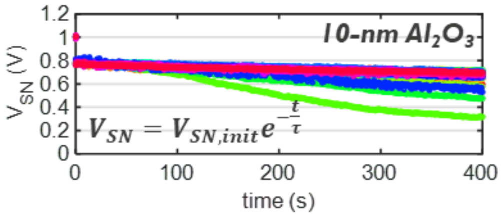
- Gate-Last with oxygen tunnel enables longer retention thanks to lower I_{OFF}
  →More efficient defect passivation in write transistor channel
- Initial V-drop is lower than in Gate-First → to be investigated

2T0C retention GL - Summary









- t_{ret}>400s in some structures
→ t_{ret} and I_{OFF} extrapolated from V_{SN} exponential decay

$$t_{ret} = ln\left(\frac{V_{SN,init}}{V_{SN,init} - 0.1V}\right) \cdot \tau \qquad I_{OFF} = \frac{V_{SN,init} \cdot Cox_{\,Rtr}}{\tau \cdot W_{Wtr}}$$

- Longest retention time (>400s) and lowest I_{OFF} achieved with 10-nm Al_2O_3 gate dielectric + oxygen tunnel
- Initial V-drop depends on gate dielectric thickness
  - Dependence on material (CAAC vs amorphous) to be investigated
- High I_{off} extracted for 5-nm Al_2O_3 → High I_{gate} at -2V?
  - Lower V_{WWL} to prove the impact of I_{gate}

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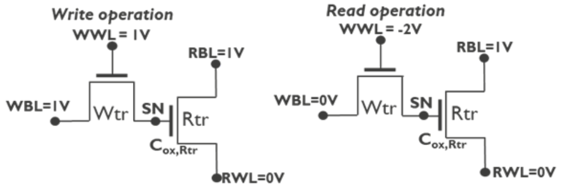
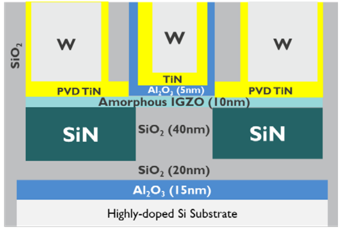
Effect of $V_{WWL,read}$ on retention time

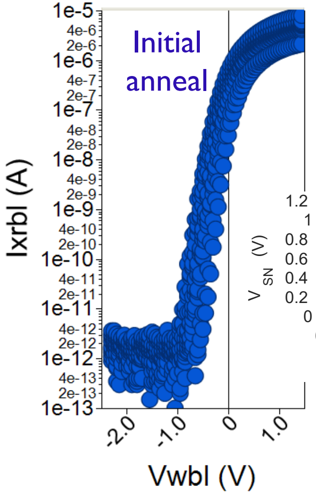
5nm Al_2O_3 with oxygen-tunnel

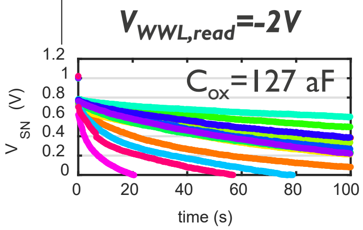




25 devices – different colors → different dies

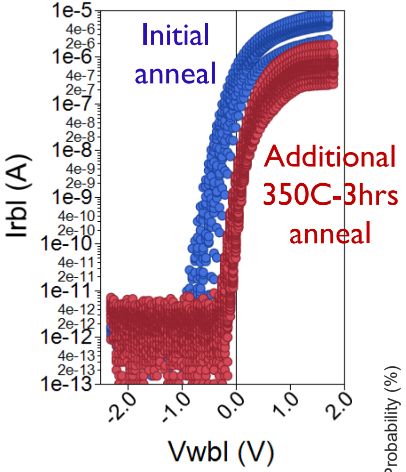
W=180nm L=50nm





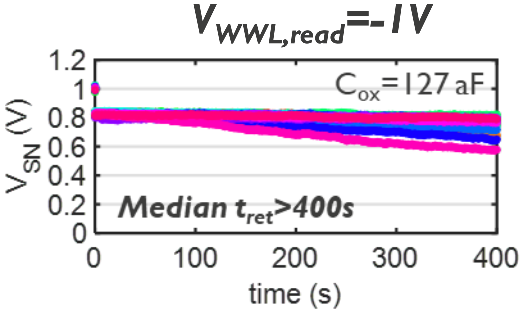
Median t_{ret}= 8s

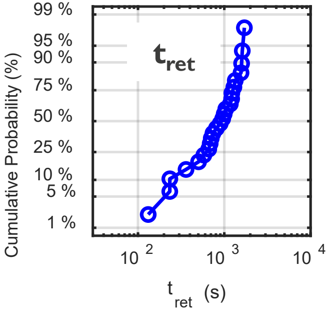
W=180nm L=50nm

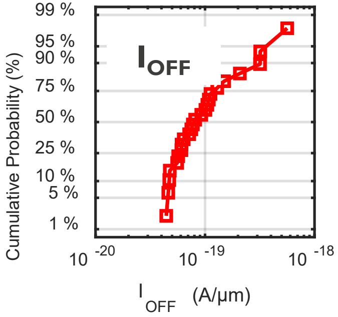


V_{th}≈0

$V_{WWL,read}$=-1V can be applied







- V_{th} <-0.5V

→Less negative $V_{WWL,read}$ cannot be applied

→Additional anneal to increase V_{th}

- Lower $|V_{WWL,read}|$ → best retention ever
- Benefit of higher $C_{ox,Rtr}$ without penalty in I_{OFF}

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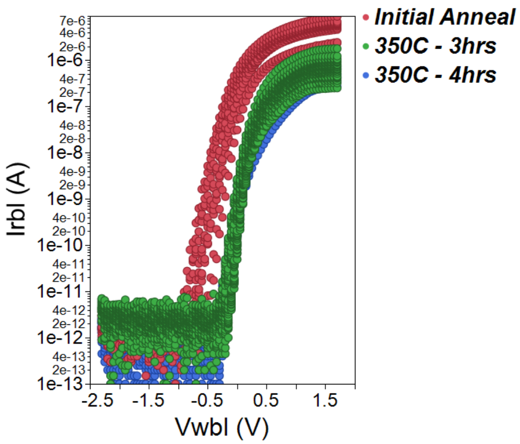
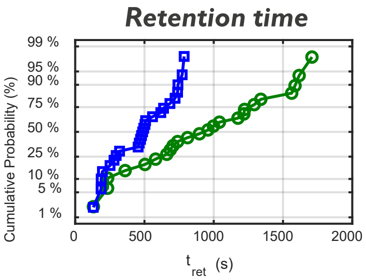
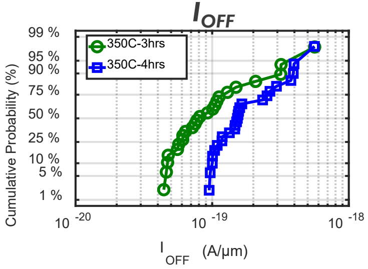
confidential

Effect of additional O_2-anneal and retention at high temperature

W=180nm L=50nm

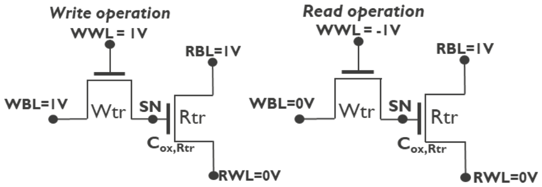


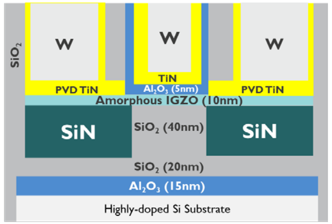




Additional anneal does not improve V_{th}

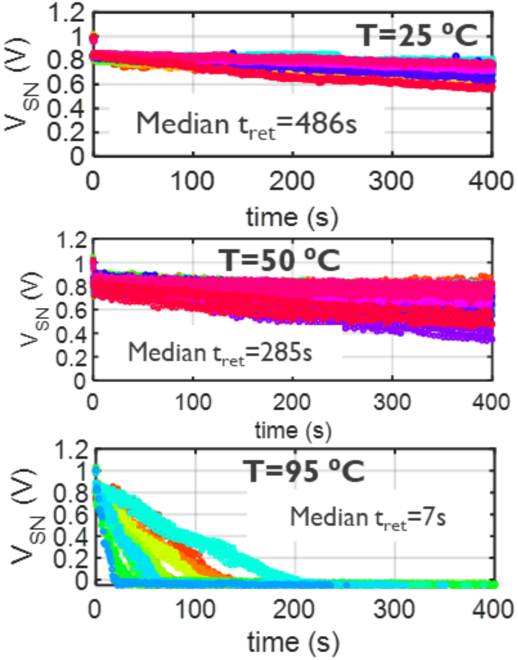
→ But it induces I_{OFF} and t_{ret} degradation





Retention at high temperature

25 devices – different colors → different dies



Current fluctuation at high temperature

→ Retention can still be assessed

Strong V_{SN} discharge at 95 °C

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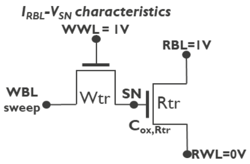
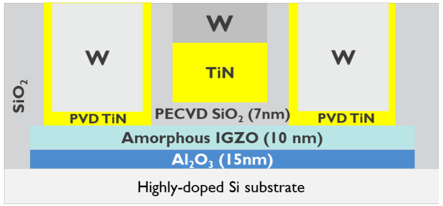
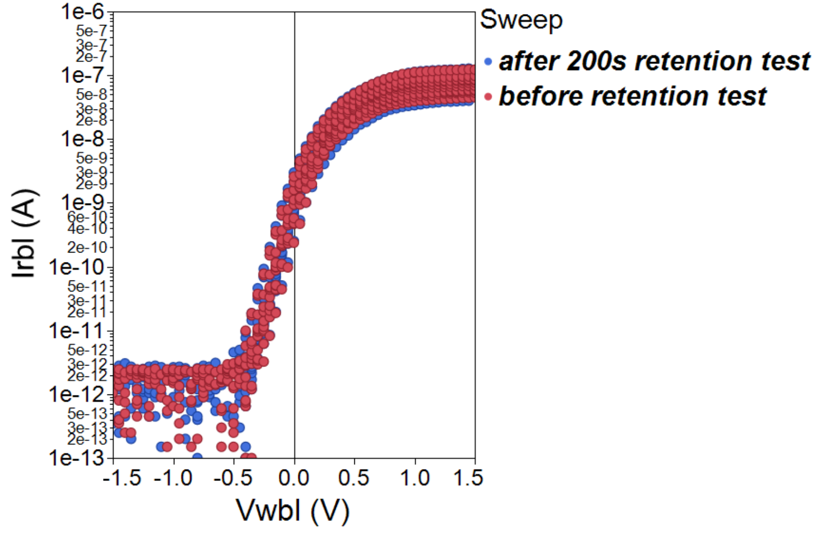
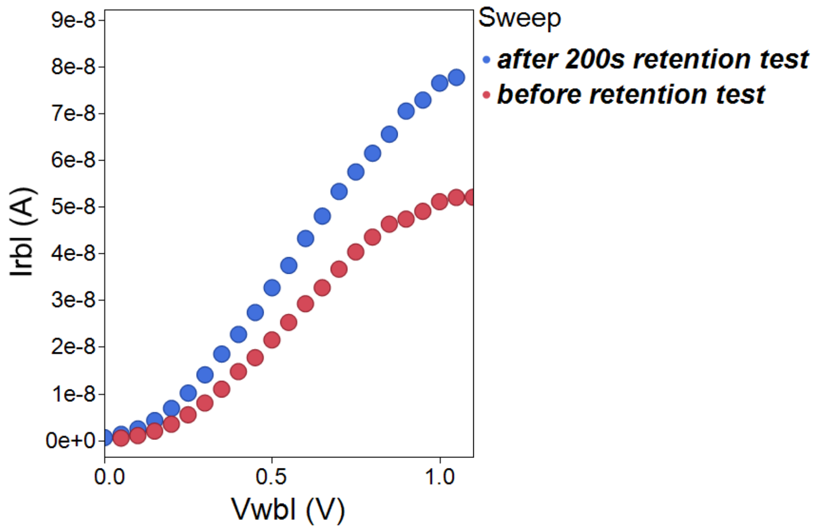
Significant V_{th} degradation after retention test in Gate-First devices

W=180nm L=45nm









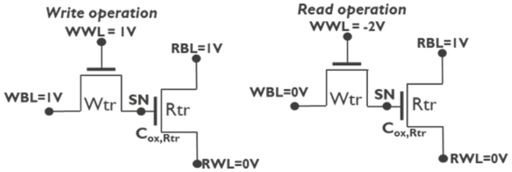
- Strong V_{th} degradation induced by H diffusion from PECVD SiO_2 → see R106 / R107
- Weighted average between the two I_{RBL}-V_{WBL} curves necessary to have valid retention assessment*
  → Unstable test-vehicle limits the learning for Gate-First devices

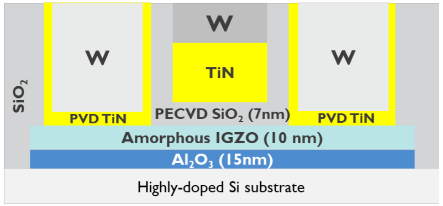
* See backup slides

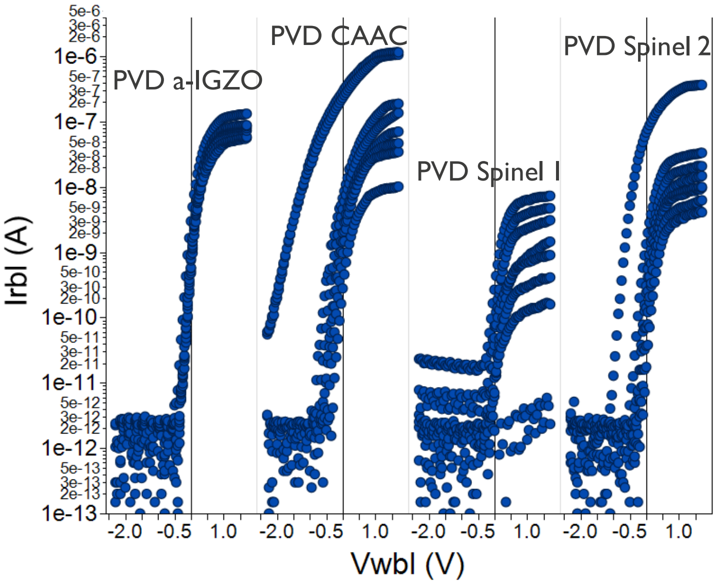
Impact of IGZO Phase

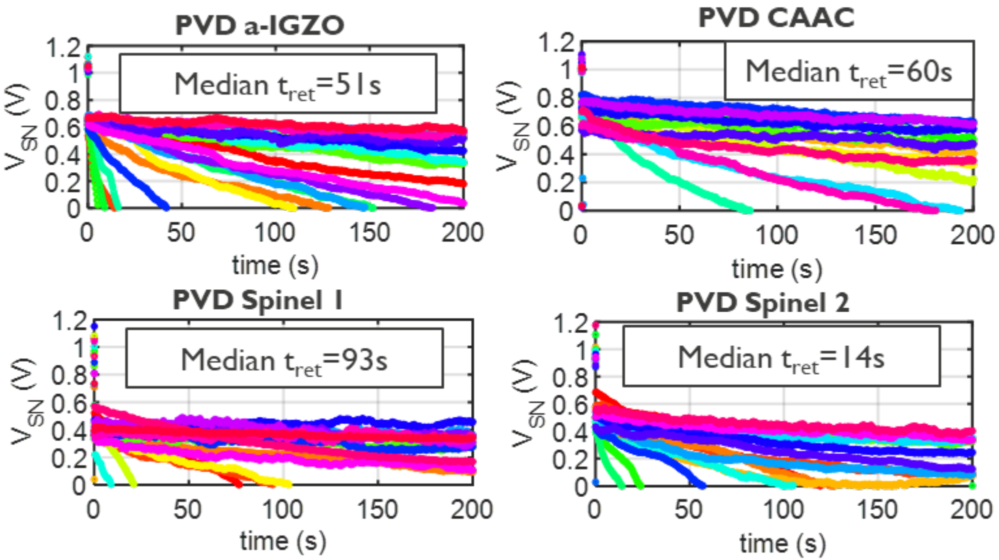
W=180nm L=45nm; $C_{ox,Rtr}$=40aF

13 devices – different colors → different dies









- Large variability in transfer characteristics (PTW 10/2020 R106) → large variability in 2T0C retention
- No major impact of IGZO phase on retention
- Strong variability also for initial V-drop

s-IGZO 1	GZO 6 nm template: IGZO 90% O_2, RT
s-IGZO 2	GZO 6 nm template: IGZO 90% O_2, RT - O_2 anneal 500 °C

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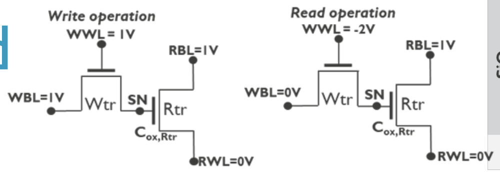
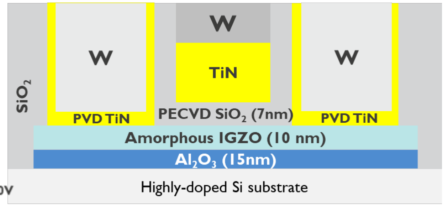
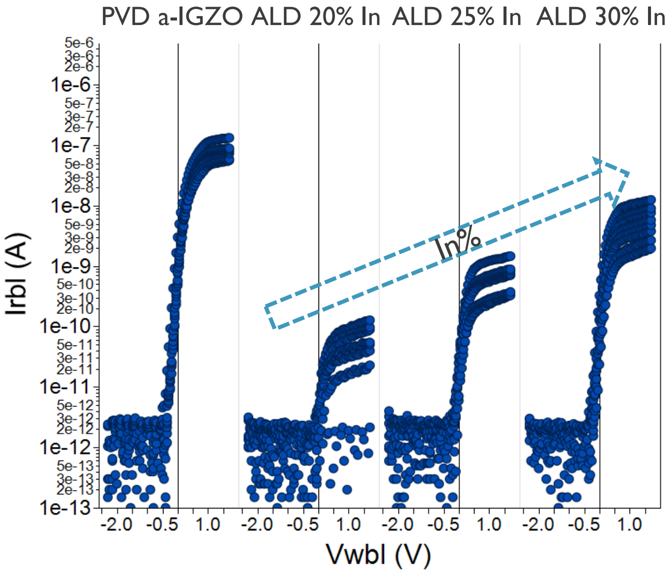
Impact of IGZO Deposition method

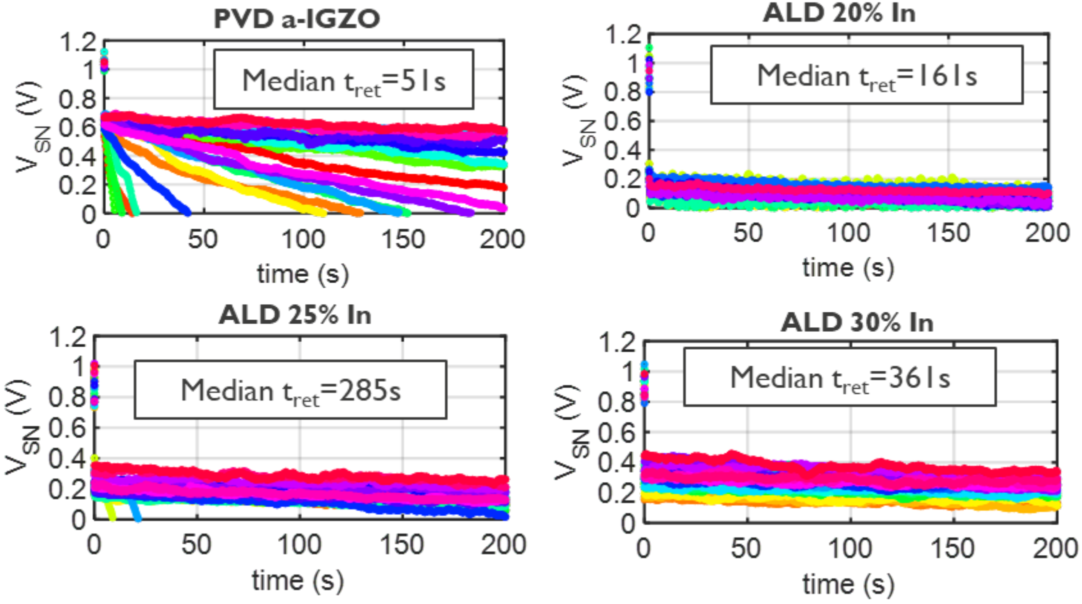
W=180nm L=45nm; $C_{ox,Rtr}$=40aF

13 devices – different colors → different dies



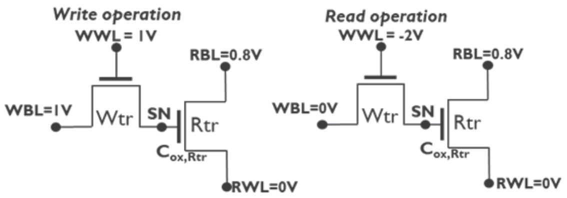


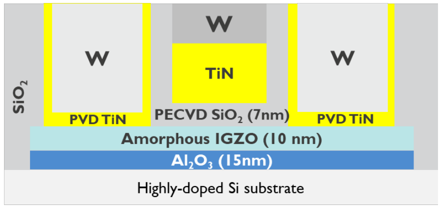


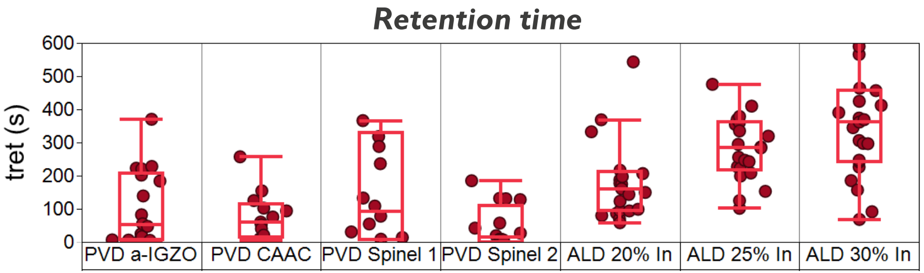


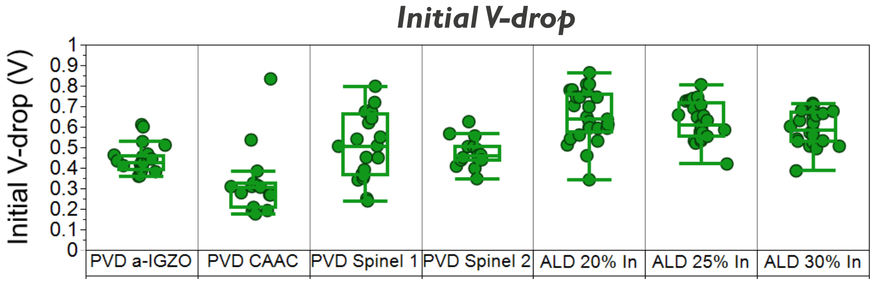
- Strong initial V-drop for ALD IGZO → V-drop not only due to WWL-SN capacitive coupling
- Promising retention with ALD IGZO → to be assessed on Gate-Last

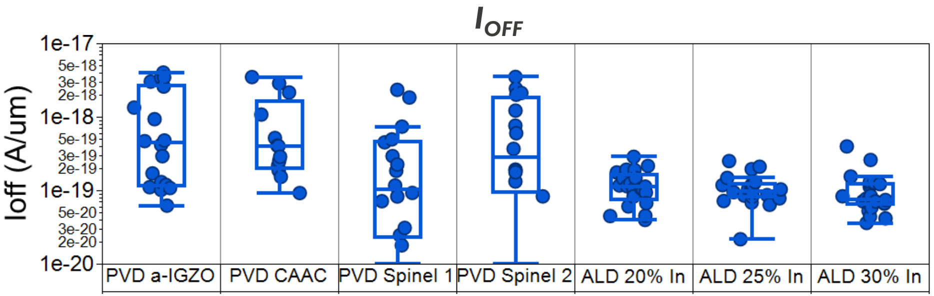
Summary of Gate-First results





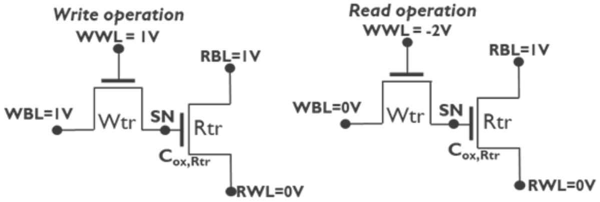


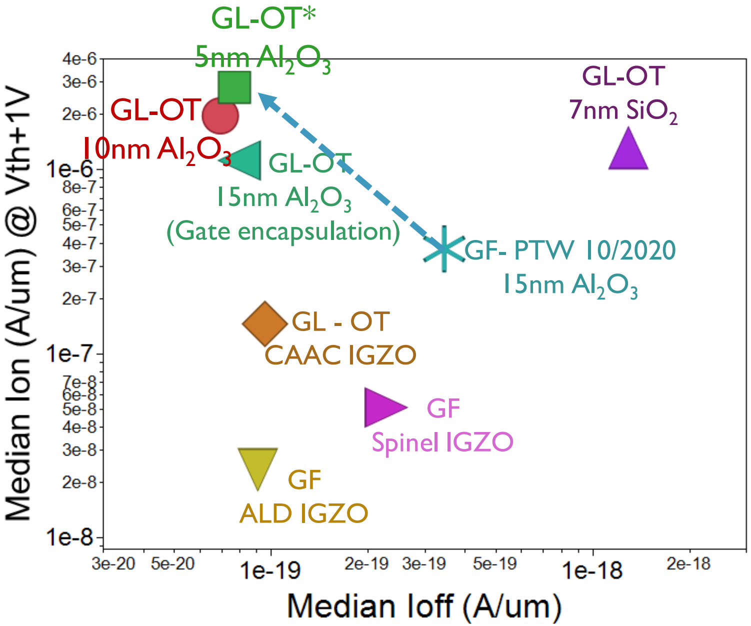


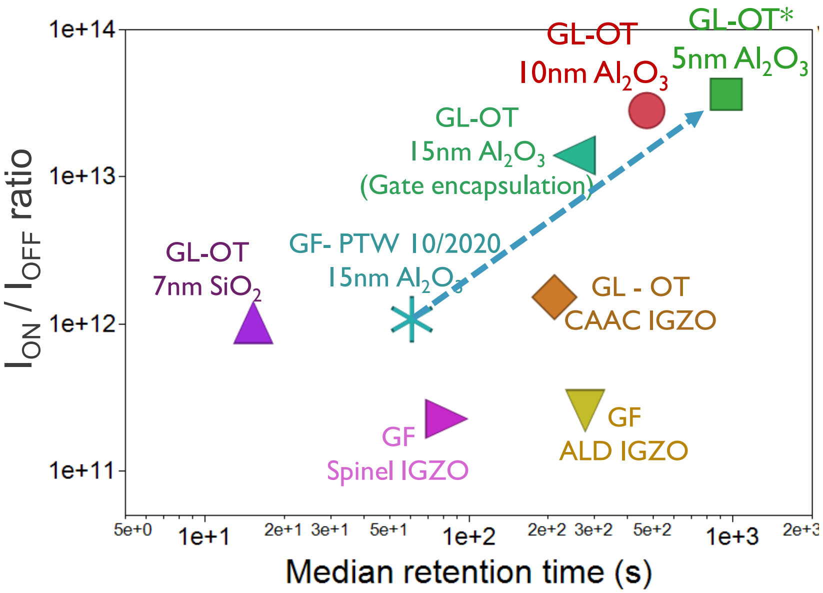


- Large variability hinders the learning for different channel materials
- V-drop dependence on channel material to be investigated
- Promising retention with ALD IGZO
  → To be re-assessed in Gate-Last devices

Summary of I_{ON} / I_{OFF} / retention time



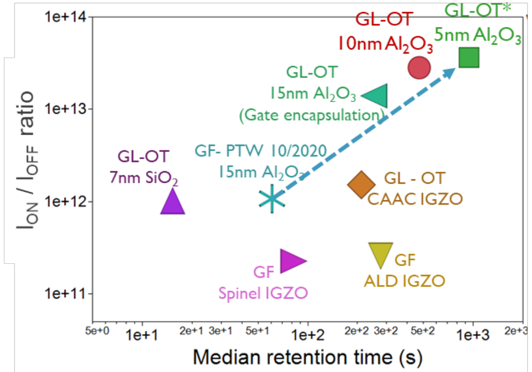




$*V_{WWL,read} = -1V$

Conclusions

- 2T0C retention assessed on Gate-Last (w. and w/o Oxygen Tunnel) and Gate-First with different IGZO phase / deposition method
- Gate-Last with oxygen tunnel ensures better retention thanks to lower I_{OFF}
- Initial V-drop depends on device architecture and channel material
- 5nm Al_2O_3 gate dielectric:
  - Retention and I_{OFF} can be improved by reducing $V_{WWL,read}$
- Gate-Last is a more reliable test-vehicle for 2T0C assessment:
  - Lower initial V-drop
  - Better reproducibility across the wafer



Outlook

- Focus on understanding the trends observed in Gate-First and Gate-Last
  - Impact of architecture and channel material on initial V-drop
  - Effect of gate V-stress on 2T0C retention
- AC test implementation
- 2T0C and 2T1C implementation for best Gate-Last and Gate-First devices with oxygen tunnel

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2T0C characterization

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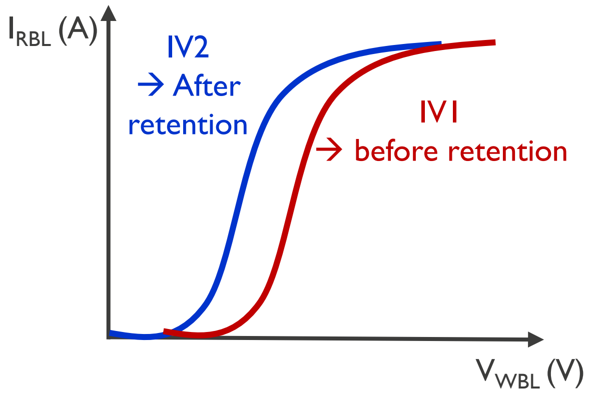
GLOBALFOUNDRIES intel SAMSUNG SK hynix tsmc Panasonic Micron KIOXIA Western Digital SONY HUAWEI Qualcomm

Backup Slides

Weighted average between I_{RBL} before retention and after retention

Purpose: consider V_{th} degradation in the V_{SN} calculation

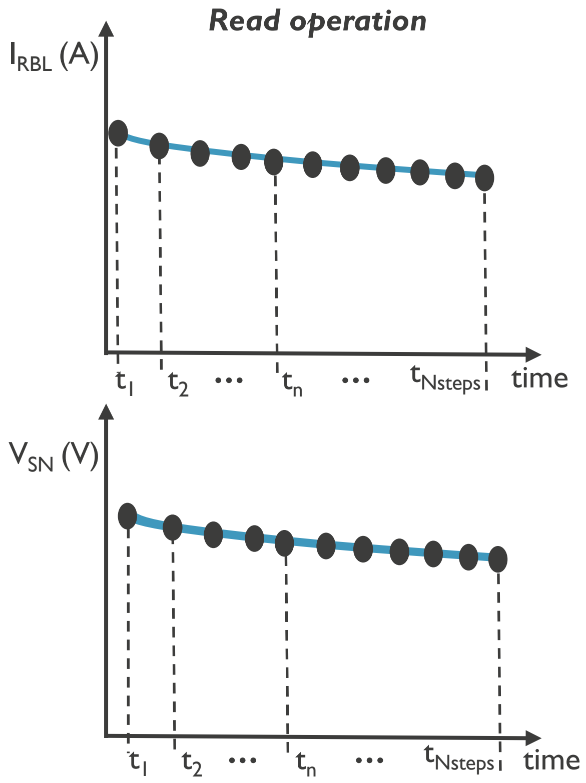


N_{steps} = total number of time steps during read operation

For each time step t_n:

$f_{p,n}$ = polynomial fitting of IVavg(t_n)

$$V_{SN}(t_n) = fp_{,n}(IRBL(t_n))$$



For each time step t_n, the weighted average between the two I_{RBL}-V_{WBL} curves is calculated:

$$IVavg\,(t_1) = \frac{(IV1 \cdot N_{steps}) + (IV2 \cdot 0)}{N_{steps}}$$

First time step → only IV1 is considered

$$IVavg\,(t_n) = \frac{(IV1 \cdot (N_{steps} - n)) + (IV2 \cdot n)}{N_{steps}}$$

Time step n → weighted average between IV1 and IV2

$$IVavg\,(t_{Nsteps}) = \frac{(IV1 \cdot 0) + (IV2 \cdot N_{steps})}{N_{steps}}$$

Last time step → only IV2 is considered

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