Breakthrough of Selector Technology for cross-point 25-nm ReRAM

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***Abstract*—In this paper, the authors report for the first time the outstanding selector performance from an innovative oxide selector. SiO_2, one of conventional and common materials in semiconductor industry, was chosen as a matrix oxide material. Metal atoms which are non-mobile and easy to handle were injected into the oxide films. Off-current and threshold voltage (V_{th}) could be controlled by using arsenic (As), which doping method and concentration were carefully investigated to achieve threshold switching behavior. Finally ReRAM (Resistance switching Random Access Memory) cell array consisted of one selector-one resistor (1S1R) was successfully demonstrated with the full integration of the newly developed selector.**

I. Introduction

The limit of scale-down that semiconductor technology is facing in the near future requires next generation memories such as STT-MRAM, PCRAM, and ReRAM. One of these candidates, ReRAM showed several satisfactory properties for wide range of application targets in terms of various characteristics.

As described in Fig. 1, high-efficient cross-point array can be realized by using a stacking of selector and resistor in order to control sneak current through unselected cells. Recently it has been reported that electrical metallization cells showed volatile resistance states, which can be utilized as a selector component in cross-point array structure to control off-state current [1,2]. Mobile atoms such as Cu and Ag generated volatile conducting paths when certain amount of voltage was applied on the devices and then the cells showed good off-current characteristics. However, there are several problems in applying to 1S1R devices; At first, threshold voltage is too low to obtain enough operating window at large array of 1S1R cell (Fig. 2). Secondly it's well known that Ag and Cu are not only difficult materials to proceed reactive ion etch process but also contaminant materials in semiconductor fabrication facilities. OTS (Ovonic Threshold Switching) selector [3,4] can be a good choice for non-volatile memory with the structure of cross-point array. But thermal instability and the increase of V_{th} with time should be solved in order to achieve reliable writing and sensing operation. Therefore the development of new selector is essential to overcome these disadvantages and to achieve non-volatile memory chips with high-density cross-point array structure.

In this work, we profoundly investigated that SiO_2 which is one of conventional dielectric materials and has been used commonly in semiconductor fabrication process could be applied as a selector showing volatile threshold switching behavior with high enough V_{th} when some kinds of defects were precisely controlled by material engineering with As ion-implantation. Consequently it was verified that the selector is adequate to operate large arrays consisted of 25 nm-tech 1S1R ReRAM devices.

II. Experimental

SiO_2 film with the thickness of 10 nm was deposited on a TiN bottom electrode at first and then As atoms were injected into the SiO_2 film by using ion implantation method with adequate implant energy and dose. Consecutive fabrication processes such as TiN top electrode, patterning, and encapsulation processes follows by using 25-nm standard CMOS technology on 300 mm wafers. Figure 3 shows the cross-sectional TEM image of As-implanted SiO_2 selector cell. As-deposited As-SiO_2 films are amorphous and keep the state even after the post-process at the temperature as high as 400^{o}C. Metal layers from M0 to M4 and transistors were fabricated under the word lines (WL). WL and bit line (BL) decoders were implemented underneath cell array region to improve cell efficiency. Test patterns of devices integrated with transistors as previously reported [5] were utilized to control compliance current in AC response. Typically selector performance has been measured for reflecting real situation with the pulse duration shorter than 1us. Finally array performance from one selector-one resistor cross-point array was demonstrated with 16 Kb (128x128).

III. Results

A. Material properties

Figure 4 shows a typical I-V curve representing electrical characteristics of the As-SiO_2 selector. As mentioned previous, threshold switching can be observed even though the selector underwent high thermal budget as high as 400^{o}C during the fabrication process. The device provides symmetric bidirectional volatile switching even with different compliance current at both sides (30 uA on (+) side vs. 70uA on (-) side). The selector shows quietly low off-current of 80 pA at the half voltage of V_{th} in sub-threshold region and sudden increase of current over V_{th}.

As shown in Fig. 5 of chemical state analysis of As-SiO_2 selector films, As atoms uniformly dispersed in SiO_2 matrix after the As implantation process. It's remarkable that most of As atoms remains unoxidized and some of Si-O bonds were broken into SiO_{2-x} due to the damage from the implantation of heavier As atoms and on the other hand the majority of Si was kept in fully oxidized state (Fig.6).

B. Device characteristics

Electrical analysis was performed at various implantation doses of As to obtain better threshold switching performances. In order to observe the effect of the implantation dose of As on electrical characteristics of the oxide films, 4 different dose of As atoms were implanted into the SiO_2 films. In the As concentration range of 90%~140% of reference concentration, all of devices show good threshold switching characteristics in similar V_{th} and I_{off} (Fig. 7). V_{th} and hold voltage (V_h) were characterized by using triangular pulse (Fig. 8 (a)). Input voltage and output current should be generated and measured by the combination of a pulse generator and a remote amplifier. Figure 8 (b) represents the distribution of V_h and V_{th} distributions. The median values of V_{th} and V_h are estimated to 3.0V and 2.5V, respectively.

Figure 9 exhibits that the device can quickly response to the applied voltage pulse in both of on-state and off-state. The transition time to on-state and off-state were measured to less than 52 ns and 23 ns, respectively, which are relatively faster than others based on electrical metallization cell [2,6]. As can be seen in Fig. 10, this selector doesn't show memory behavior even with 120 uA of input current. It is explained that compliance current doesn't affect the natural behavior of the As-SiO_2 materials and there is no permanent conducting path such as a metallic filament when voltage is removed. Consequently the new selector can supply high on-current density (J_{on}) upto 25 MA/cm^2 in sustaining selector characteristics.

It's well known that the increase of V_{th} with time which is called "Drift" can be easily observed in OTS selector consisted of disordered materials. This phenomenon is not proper in the view of array operation because of narrowing V_{rd} window with time in 1S1R cell structure. On the other hand As-SiO_2 selector doesn't show any change in V_{th} with interval time as shown in Fig. 11. As a result, the selector can offer reliable switching as well as reading operation owing large enough V_{rd} window. The selector device can repeatedly switch more than 10^5 cycles in maintaining the large selectivity (Fig. 12).

Figure 13 (a) shows the typical short pulse I-V characteristics of the resistor. The resistor is composed of a metal layer as a role of oxygen vacancy reservoir on an oxide switching layer. The resistor needs forming process at the first sweep of I-V measurements. Figure 14 shows the TEM image of the integrated 1S1R cell structure. The resultant short-pulse I-V of 1S1R device is shown in Fig. 13 (b). Preventing consumption of write-driver current in unselected cells, half bias of 1S1R V_{sw} should not exceed V_{th} of selector in cross-point array and appropriate combination of selector and resistor is important. The half of V_{sw} is less than V_{th} of the selector so that the 1S1R device can be switched to the both of set and reset state without sneak current through unselected cells as expected.

C. Array performances

Figure 15 shows the optical microscope image of a test chip fabricated by 25 nm CMOS process technology. The test chip has several blocks with different array size to investigate the cell performances in the variation of circumstance, for example, sneak current and IR drop. The bit map of set and reset programming and the cumulative distributions of I_{HRS} (read current of high resistance state) and I_{LRS} (read current of low resistance state) acquired from 16Kb (128×128) array cells are illustrated in Fig. 16. The bit map image shows that more than 92% of cells from the array can be switched to set and reset state. The integrated 1S1R cell array shows wide sensing window between I_{LRS} and I_{HRS}. It is hopefully expected that the size of array can be enlarge enough to satisfy high-density non-volatile memory chips when further improvement is conducted in terms of cell characteristics and process conditions.

IV. Conclusion

For the first time our experimental result showed that threshold switching using non-mobile and fab-friend As-included SiO_2 films can be obtained. 1S1R cell integrated with the selector was successfully demonstrated owing to the wide operating windows of current and voltage. Finally compared with other selectors reported previously, As-SiO_2 selector revealed outstanding and reliable performances in terms of off-current, on-current, and V_{th} (Fig. 17).

References

[1] S. G. Kim, et al., "Improvement of Characteristics of NbO_2 Selector and Full Integration of $4F^2$ 2x-nm tech 1S1R ReRAM", *IEDM Tech. Digest*, pp.249-252, 2015.

[2] J. V. D. Hurk, et al., "Volatile resistance states in electrochemical metallization cells enabling non-destructive readout of complementary resistive switches", *Nanotechnology*, 25(42), 425202, 2014.

[3] R. Midya, et al., "Anatomy of Ag/Hafnia-based selectors with 10^{10} nonlinearity", *Advanced materials*, 1604457, 2017.

[4] S. R. Ovshinsky, "Reversible electrical switching phenomena in disordered structures", *Phys. Rev. Lett.* 21 1450, 1968.

[5] B. Govoreanu, et al., "Thermally stable integrated Se-based OTS selectors with >20MA/cm^2 current drive >3.10^3 half-bias nonlinearity, tunable threshold voltage and excellent endurance", *VLSI Technology Digest*, T92-T93, 2017.

[6] S. H. Jo, et al., "3D stackable crossbar resistive memory based on field assisted superlinear threshold (FAST) selector", *IEDM Tech. Digest*, pp.160-163, 2014.

[7] R. S. Shenoy, et al., "Endurance and Scaling Trends of Novel Access-Devices for Multi-Layer Crosspoint-Memory based on Mixed-Ionic-Electronic-Conduction (MIEC) Materials", *VLSI Technology Digest*, pp.94-95, 2011.

[8] Akifumi Kawahara1, et al., "An 8Mb Multi-Layered Cross-Point ReRAM Macro with 443MB/s Write Throughput", *ISSCC Dig. Tech. Papers*, pp. 432-434, 2012.

[9] M. J. Lee, et al., "Highly-Scalable Threshold Switching Select Device based on Chaclogenide Glasses for 3D Nanoscaled Memory Arrays", *IEDM Tech. Digest*, pp.33-35, 2012.

[10] L. Zhang, et al., "High-Drive Current (>1MA/cm^2) and Highly Nonlinear (>10^3) TiN/Amorphous-Silicon/TiN Scalable Bidirectional Selector with Excellent Reliability and Its Variability Impact on the 1S1R Array Performance", *IEDM Tech. Digest*, pp.94-95, 2014.

[11] J. Woo, et al., "Electrical and Reliability Characteristics of a Scaled (~30nm) Tunnel Barrier Selector (W/Ta_2O_5/TaOx/TiO_2/TiN) with Excellent Performance (J_{MAX} > 10^7A/cm^2)", *VLSI Technology Digest*, pp.978-979, 2014.

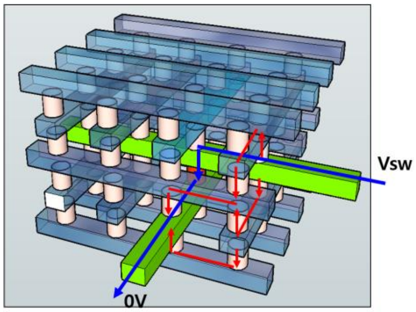

Fig. 1. Schematics of multi-stacked cross-point array structure in which sneak current flows through unselected cells. Sneak current can be minimized by the introduction of a highly nonlinear selector element.

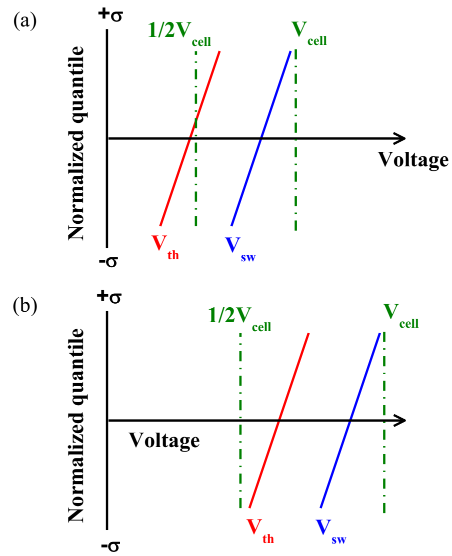

Fig. 2. Schematics of relationship between voltages (V_{th}, V_{sw}, V_{cell} and $1/2V_{cell}$) and normalized quantile in 1S1R array. V_{cell} $1/2V_{cell}$ are the voltages applied on selected cells and half selected cells, respectively. (a) If V_{th} is too low, selector can't prevent sneak current from flowing into unselected cells because of $1/2V_{cell} > V_{th}$, (b) higher V_{th} has ability to control sneak current without disturbing unselected cells.

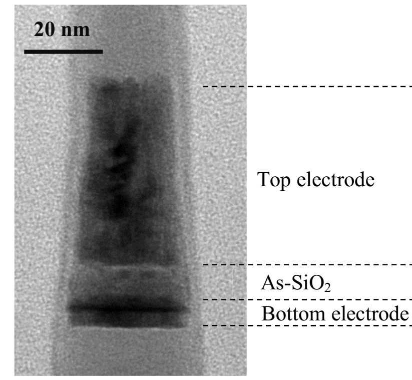

Fig. 3. Cross-sectional TEM image of TiN/As-SiO_2/TiN selector fabricated by 25 nm CMOS technology.

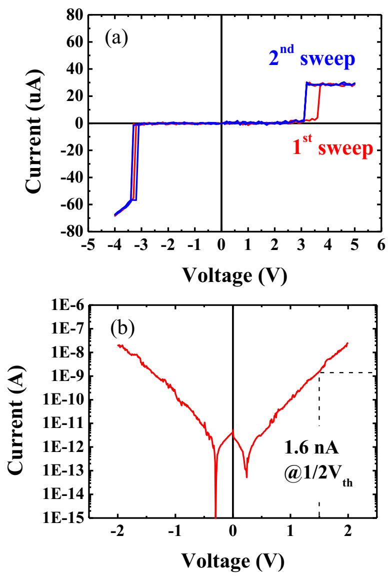

Fig. 4. (a) Threshold switching behavior of As-SiO_2 selector device with symmetric bipolar characteristics even with difference compliance current (measured by short-pulse I-V sweep, 300 ns of duration), (b) DC I-V curve of subthreshold region.

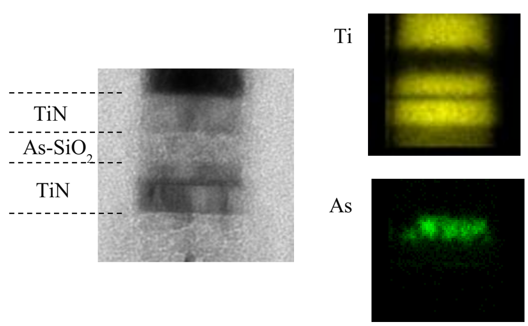

Fig. 5. Analysis of special distribution of As in As-SiO_2 film by using EDS. It can be observed that As atoms uniformly disperse in SiO_2 matrix

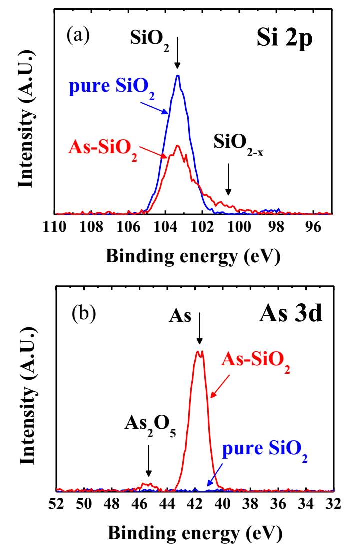

Fig.6. XPS result of chemical bonding state of Si and As. Most of As atoms exist in unoxidized state and only a little Si-O bonds is observed.

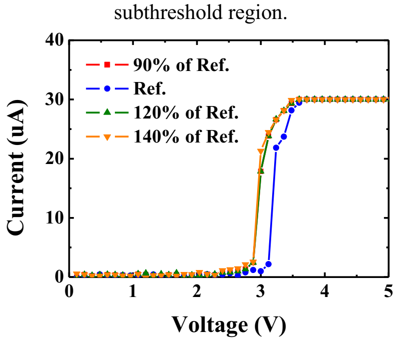

Fig. 7. Observation of the effect of the implantation dose of As on electrical characteristics of the oxide films. 4 different doses of As atoms were implanted into the SiO_2 films.

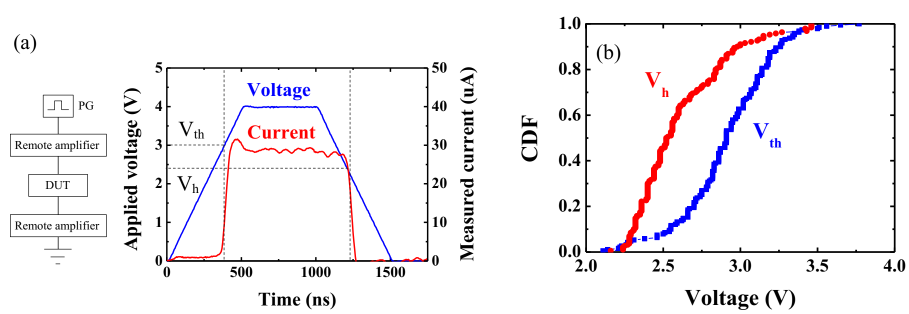

Fig. 8. (a) Configuration of apparatus and the method to measure V_{th} and V_h, (b) cumulative distributions of V_{th} (blue) and V_h (red) measurement (38 cells repeatedly measured 5 times).

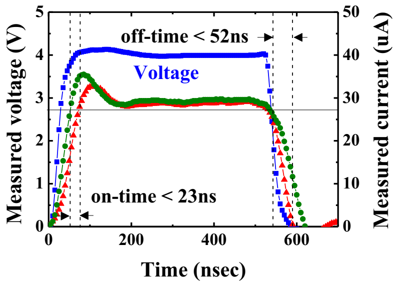

Fig. 9. Measurement of transition time in As-SiO_2 selector device with the sweep rate of 7×10^8 V/sec. In order to subtract RC delay of signal, test pattern with (red line) and without selector (green line) were measured and compared. The transition time were measured to less than 52 ns.

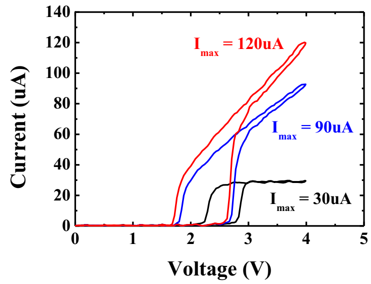

Fig. 10. I-V curves under different compliance current this selector. The selector doesn't show memory behavior even under 120 uA in on-state region. As a result, maximum on-current density (J_{on}) is calculated to 25 MA/cm^2.

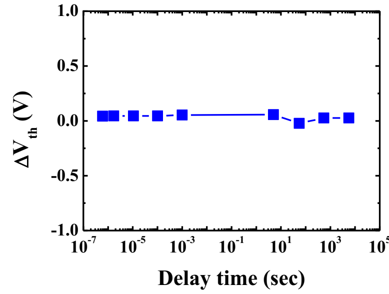

Fig. 11. Variation of V_{th} change (difference between initial V_{th} and V_{th} measured at different interval time). No change in V_{th} with time is observed from As-SiO_2 selector and it means that the selector has capability to offer reliable switching and reading operation owing keeping wide V_{rd} window.

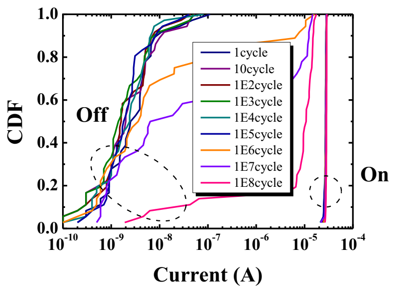

Fig. 12. Measured endurance characteristics of the As-SiO_2 selector devices. (Applied voltage = 4V, pulse duration = 300ns, compliance current = 30uA). Read currents of Off-state and on-state were measured at 1.5V and 4V, respectively.

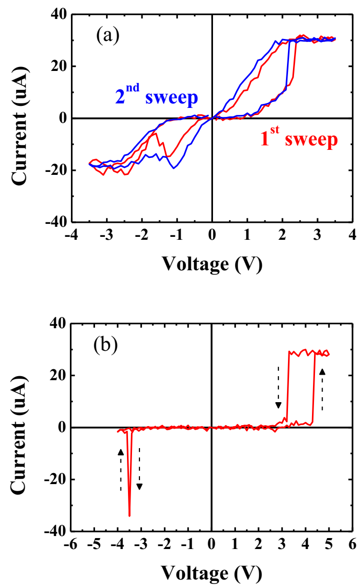

Fig. 13. (a) short pulse I-V curves of resistor used in this experiment. The resistor is composed of a metal layer as a role of oxygen vacancy reservoir on an oxide switching layer. (blue : 1st sweep, red : 2nd sweep), (b) short-pulse I-V curve of 1S1R ReRAM cell.

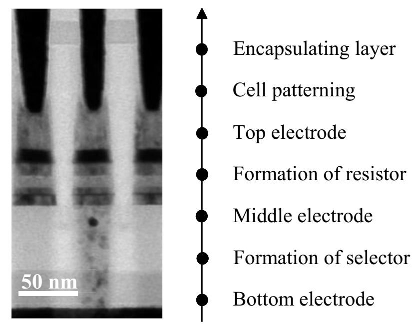

Fig. 14. Cross-sectional TEM image of TiN/As-SiO_2/TiN 1S1R device and process flow with 25 nm CMOS technology.

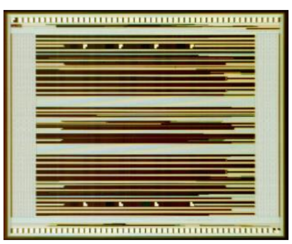

Fig. 15. Optical microscope image of the test chip fabricated by 25 nm CMOS process technology. The test chip has differently functionalized blocks in order to investigate the various cell performances.

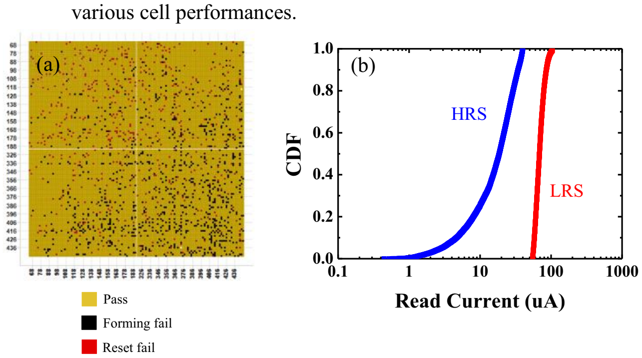

Fig. 16. (a) Bit map image of 16 Kb (128×128) array and (b) cumulative distributions of the I_{LRS} and I_{HRS} after set and reset programming. The programming of the arrays was performed at 25°C.

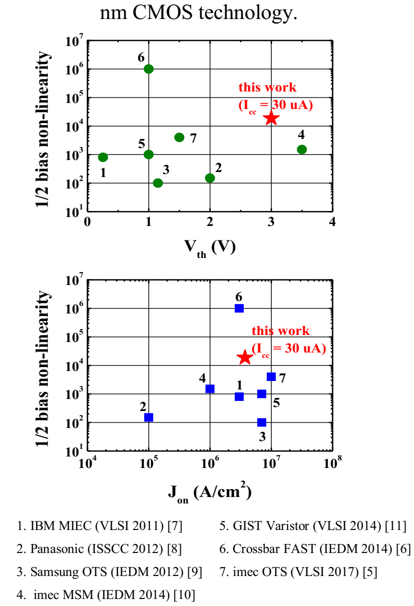

Fig. 17. Comparison of on-current density (J_{on}), V_{th} and off-current characteristics from various selectors [5]. The selector form this work satisfies all of requirement of J_{on}, V_{th}, and nonlinearity at a time.