A Read Voltage Modulation Technique for Leakage Current Compensation in Cross-Point OTS-PRAM

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***Abstract*—In this paper, a read voltage modulation technique (RVM) is proposed to compensate for leakage current in a cross-point phase change random access memory with an ovonic threshold switch (OTS-PRAM). The leakage current, the sum of off-state current (I_{OFF}) of OTS selectors, causes the voltage drop and increases the variation of sensing voltage (V_{SENSE}) which is the electric potential difference between a selected bit line (BL) and a word line (WL). Eventually, the voltage drop reduces the sensing margin (SM). To compensate for the BL voltage drop, the proposed RVM reduces the V_{SENSE} variation by applying an adaptive voltage to the selected WL. Thus, a sufficient SM is guaranteed. HSPICE simulation results with industry-compatible 65-nm model parameters show that the cross-point OTS-PRAM with the proposed RVM achieved a remarkable improvement in SM (from 105 mV to 395 mV) in high BL leakage current condition (51.3 uA).**

Keywords—Cross-point array, leakage current compensation, off-state current, ovonic threshold switch (OTS), phase change memory (PRAM), read voltage modulation (RVM)

I. Introduction

Phase change random access memory (PRAM) is one of the promising storage class memory (SCM) candidates to overcome both the slow latency of flash memory and the short-term data retention of dynamic random access memory. Since the prototype 3D cross-point PRAM with an ovonic threshold switch (OTS-PRAM) in [1] was introduced, high-density 3D cross-point OTS-PRAM has been developed by major semiconductor vendors [2], [3]. Owing to an OTS with low temperature processing, a multi-stackable cell structure is enabled in a cross-point array, unlike diode selectors that require high temperature processing such as dopant activation [4], [5]. Accordingly, various OTS alloys have been studied [4], [6]–[9]. However, when the OTS material exhibits poor off-state current (I_{OFF}) characteristic, the high I_{OFF} causes problems in read and write operations [2]. Especially, as the array size increases, the effect of I_{OFF} on the read and write operations increases [10], [11]. In this study, a new technique is proposed to resolve the high I_{OFF} issue in the cross-point OTS-PRAM during the read operation.

This paper is organized as follows. In Section II, the effect of the high I_{OFF} on the read operation is verified. Section III describes a novel read voltage modulation technique (RVM) for resolving the high I_{OFF} issue. Subsequently, results of various experiments are compared in Section IV. Finally, Section V provides the conclusion in this paper.

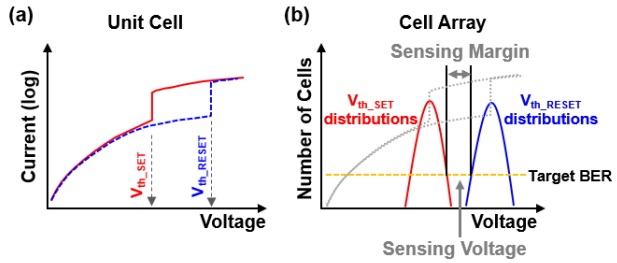

Fig. 1. (a) I-V curves of OTS-PRAM cell in SET and RESET state. (b) V_{TH_SET} and V_{TH_RESET} distributions in an array.

II. Effect of I_{OFF} on Read Operation

A. OTS-PRAM Cell Characteristics

An OTS-PRAM cell consists of an OTS selector and a storage element GeSbTe (GST). The OTS has only an irreversible amorphous phase, while the GST has two different phases: crystalline phase for a SET state (low resistance state) and amorphous phase for a RESET state (high resistance state) [1].

Fig. 1(a) shows the current-voltage (I-V) curve of the OTS-PRAM cell and Fig. 1(b) shows the threshold voltage (V_{th}) distribution of a cell array, where V_{th_SET} and V_{th_RESET} are V_{th} of OTS-PRAM cells in the SET and RESET state, respectively. The sensing margin (SM), a key factor to estimate the yield of a product, is the voltage difference between V_{th_SET} and V_{th_RESET} distributions. To sense the data, the applied sensing voltage (V_{SENSE}) which is the electric potential difference between a selected bit line (BL) and a word line (WL), is normally middle voltage between the V_{th_SET} and V_{th_RESET} distributions, as shown in Fig. 1(b). When the V_{SENSE} is applied to the selected cell with the SET state during the read operation, a snapback phenomenon occurs in the OTS [12]. The phenomenon causes the excessive current, which flows to a sense amplifier (SA). Whereas in the case of a cell with the RESET state, the snapback phenomenon does not occur and only the I_{OFF} of the cell is transferred to the SA. As a result, the data of the selected cell is extracted due to the snapback phenomenon.

B. OTS-PRAM Core Operation and I_{OFF} Issue

A 1/2 V_{BIAS} scheme in read and write operations is well known for preventing a sneak current and minimizing standby power consumption in the cross-point OTS-PRAM with a bidirectional symmetric I-V characteristic of OTS [10], [11]. In case of a $x \times y$ cell array, x-1 and y-1 half-selected cells in the selected BL and WL exist, respectively. Thus, as the array size increases, the number of half-selected cells increases.

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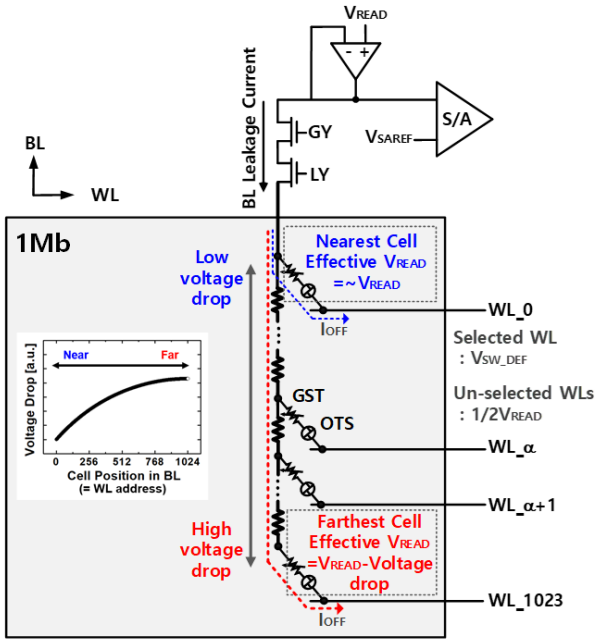

Fig. 2. Description of voltage drop induced by the BLC, the sum of I_{OFF} of half-selected cells in a selected BL in an 1 Mb array (1 Kb × 1 Kb). The inset shows an example of the voltage drop depending on a cell postion.

As shown in Fig. 2, when the selected BL is precharged to a read bias voltage (V_{READ}) and the selected WL is discharged to V_{SW_DEF} in the read operation, the middle voltage between V_{READ} and V_{SW_DEF}, typically half voltage of V_{READ} (1/2 V_{READ}), is applied to half-selected cells in the selected BL. The I_{OFF} of the half-selected cells flows from the selected BL to the un-selected WLs, and the sum of the I_{OFF} is called the BL leakage current (BLC). As the number of cells per BL increases, the BLC increases and eventually the voltage drop increases. If the BLC induces the voltage drop, V_{READ} is not fully transmitted to the far cell. Thus, the effective V_{th} of a cell detected by a sense amplifier (SA) is higher than the intrinsic V_{th} due to the voltage drop. The inset of Fig. 2 shows the voltage drop depending on the cell position in a BL. As the WL address increases, the voltage drop becomes saturated. This is because the effective V_{READ} of the far cells is reduced, thereby reducing the I_{OFF}.

C. *Verification of SM Degradation due to Leakage Current*

Based on an 1 Mb array (1 K/WL × 1 K/BL), a HSPICE simulation with OTS and GST models was performed to verify the effect of the I_{OFF} on the SM degradation [13]-[15]. In particular, the V_{th_SET} and V_{th_RESET} were modified by controlling the amorphous chalcogenide thickness parameter. The V_{th_SET} and V_{th_RESET} were extracted 10^6 times through a Monte-Carlo simulation, where the mean of V_{th_SET} is 3.4 V, the standard deviation of V_{th_SET} ($\sigma\_V_{th\_SET}$) is 100 mV, the mean of V_{th_RESET} is 4.6 V, and the standard deviation of V_{th_RESET} is 100 mV. To extract the effective V_{th} depending on the cell position in a BL, several BL sheet resistance (Rs) were assumed (from 5 Ω/sq to 20 Ω/sq) and OTS models with various I_{OFF} were used (from 100 pA to 100 nA). Fig. 3 compares the V_{th_SET} and V_{th_RESET} extracted using the Monte-Carlo simulation when a BL Rs is assumed to be 10 Ω/sq and the OTS models with I_{OFF} = 100 pA and 100 nA are used. Fig. 3(a) shows the V_{th_SET} and V_{th_RESET} depending on the cell position in a BL. In the case of the 100 pA I_{OFF}, there

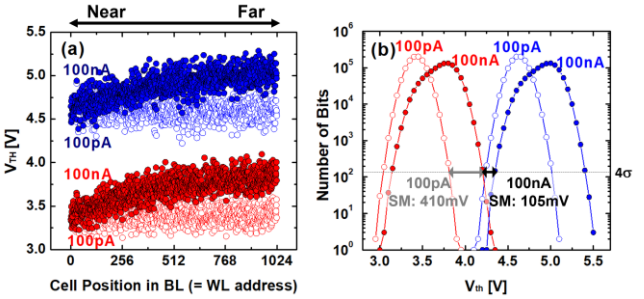

Fig. 3. (a) Simulated V_{th_SET} and V_{th_RESET} of a cell with I_{OFF} = 100 pA and 100 nA depending on the cell position in a BL, respectively. (b) Simulated V_{th} distribution of an 1 Mb array with I_{OFF} = 100 pA and 100 nA, respectively.

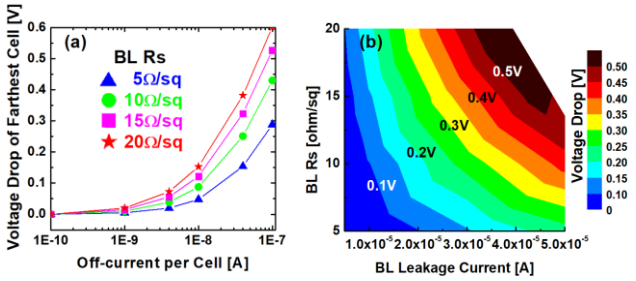

Fig. 4. (a) Voltage drop of farthest cell depending on various I_{off} and BL Rs. (b) Voltage drop of farthest cell depending on various BLC and BL Rs.

is no cell position dependency in the effective V_{th}. However, in the case of the 100 nA I_{OFF}, the increase in the effective V_{th} at the far cells is clearly observed. The effective V_{th} in the farthest cell increases by 0.430 V compared to the intrinsic V_{th}. Fig. 3(b) shows the V_{th} distribution of an 1 Mb array. The SM at 4σ is 410 mV and 105 mV when the I_{OFF} is 100 pA and 100 nA, respectively. The huge SM degradation is observed under the condition with I_{OFF} = 100 nA.

To achieve a high production yield, a sufficient SM should be guaranteed. As shown in Fig. 4(a), to avoid the SM degradation, it is necessary to use the OTS with I_{OFF} < 1 nA. In addition, the BLC should be less than 5 uA, as shown in Fig. 4(b). If the OTS exhibits the high I_{OFF} (over 1 nA), alternatives are needed to prevent the SM degradation. Thus, we focus on the I_{OFF} compensation circuit technique.

III. Read Voltage Modulation Technique (RVM)

In this section, we introduce the BLC monitoring method and the technique to compensate for the voltage drop based on the measured BLC.

A. *BLC Monitoring*

To measure the BLC, a dummy BL with cells is placed on the edge of the 1 Mb array (1 K/BL × 1 K/WL) and a pad to measure the BLC is connected to the dummy BL. The BL coupled with the pad causes timing skew during read operations. This is due to the parasitic capacitance and resistance induced by circuits and extra wiring for leakage current measurement. Thus, the pad is not connected to an actual BL. The BLC is measured by applying V_{READ} (4 V) to the pad when the voltages of un-selected BLs and all WLs are 1/2 V_{READ} (2 V). The voltage drop can be estimated by comparing the measured BLC with the simulation results shown in Section II. If the I_{OFF} of a cell at 1/2 V_{READ} is 100

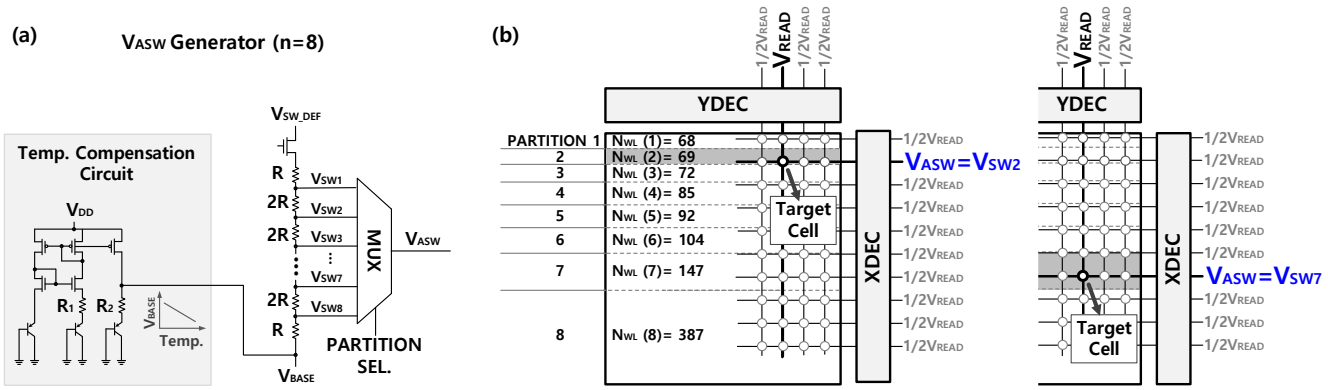

Fig. 5. (a) V_{ASW} generator with 3 parts for the proposed RVM: temperature compensation circuit [17], voltage divider, and MUX. (b) WL partitioning example and V_{ASW} for each partition.

TABLE I.
I_{OFF}, BLC, AND VOLTAGE DROP AT T = –25 °C, 25 °C, AND 85 °C.

	I_{OFF} per cell [nA]	BLC [uA]	Voltage drop in the farthest cell [V]
85 °C	100.0	51.3	0.430
25 °C	15.4	12.1	0.123
–25 °C	3.9	3.7	0.038

nA, the 51.3 uA BLC will be measured in the pad. With the known BL Rs and the measured BLC, it can be estimated that the voltage drop in the farthest cell is 0.430 V.

As temperature increases, the I_{OFF} of the OTS increases exponentially and the voltage drop also increases. Thus, it is essential to check the relation between voltage drop and temperatures. Table I shows the I_{OFF}, the BLC, and the voltage drop in the farthest cell at T = –25 °C, 25 °C, and 85 °C. Commonly, I_{OFF} is proportional to exp(–1/T) × sinh(1/T), where T is the absolute temperature [12], [13]. When the temperature rises from –25 °C to 85 °C, the voltage drop increases more than 10 times. Thus, the BLC temperature coefficient should be extracted by measuring the BLC at various temperatures and considered in the BLC compensation technique.

B. Read Voltage Modulation Technique (RVM)

A conventional method for a BL voltage drop compensation is to control the BL bias voltage [16]. However, the variation of the BL bias voltage affects the BLC and eventually results in the BL voltage drop variation. Therefore, the control of the BL bias voltage is not a suitable method for the BL voltage drop compensation. In order to effectively compensate for the BL voltage drop, a robust RVM that is an adaptive control method of the selected WL voltage is proposed. The proposed RVM reduces the V_{SENSE} variation by controlling the selected WL voltage. Compared with the conventional BL voltage control, the proposed RVM does not affect the I_{OFF} of the half-selected cells in the selected BL during read operations because there is no variation in the electric potential difference between the selected BL and un-selected WLs.

Fig. 5 shows adaptive selected WL voltages (V_{ASW}) generator for the proposed RVM, WL partitioning example, and the V_{ASW} for each partition. As shown in Fig. 5(a), the

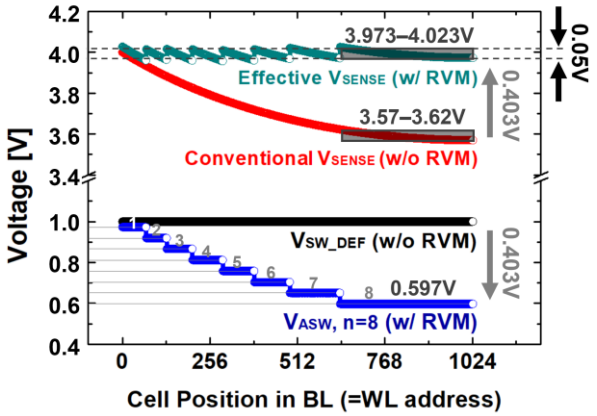

Fig. 6. Conventional V_{SENSE}, Effective V_{SENSE}, V_{SW_DEF}, and V_{ASW} (n=8) depending on the cell position in a BL.

V_{ASW} generator consists of 3 parts: a bandgap type temperature compensation circuit [17], a voltage divider, and a MUX. To generate a reference voltage called V_{BASE}, the bandgap type temperature compensation circuit is used. Because the voltage drop induced by the BLC is temperature dependent, V_{BASE} should also be temperature dependent. The target V_{BASE} for each temperature is controlled by the ratio of R_1 to R_2. In addition, to compensate for the voltage drop in the farthest cell, the potential difference between V_{BASE} and V_{SW_DEF} should be equal to the voltage drop in the farthest cell. Subsequently, evenly distributed multiple voltages are generated using the voltage divider. Finally, the V_{ASW} is applied to the selected WL based on the target cell address information during read operations. The V_{ASW} is expressed as follows:

$$V_{ASW} = V_{SW\_DEF} - \left\{ \frac{V_{BASE}}{n} \times \left(m - \frac{1}{2} \right) \right\} \quad (1)$$

, where V_{SW_DEF} is the default voltage of the selected WL, n is the number of partitions, m is the partition number. The WLs in an 1 Mb array are divided into n partitions and the V_{ASW} are applied to the partitions, as shown in Fig. 5(b). In the case of n=8, the eight V_{ASW} (from V_{SW1} to V_{SW8}) are required. If the cell in the seventh partition is selected during read operations, V_{SW7} is applied to the selected WL.

Fig. 6 compares the selected WL voltage and the V_{SENSE} with and without the RVM (n=8) when the voltage drop in

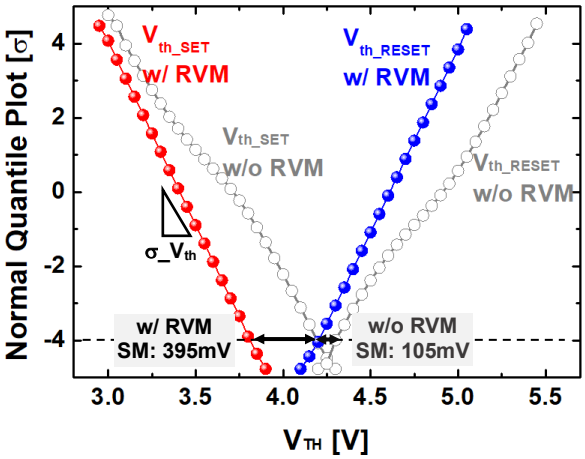

Fig. 7. Comparison of normal quantile plot w/o and w/ RVM (n=8).

TABLE II. RESULTS OF VARIOUS EXPERIMENT

	I_{OFF}: 100 pA (w/o RVM)	I_{OFF}: 100 nA (w/o RVM)	I_{OFF}: 100nA (w/ RVM)			
			n=2	n=4	n=8	n=16
Mean of V_{th_SET} [V]	3.40	3.71	3.44	3.42	3.41	3.40
σ_V_{th_SET} [mV]	100	160	118	105	101	100
SM at 4σ [mV]	410	105	300	370	395	400

the farthest cell is 0.430 V. The selected BL is precharged to V_{READ} (5 V, not shown in Fig. 6) and the selected WL is discharged to V_{SW_DEF} (1 V). Thus, the target V_{SENSE} is 4 V. Without the RVM, the reduction of the conventional V_{SENSE} is observed as the WL address increases. For example, the reduced conventional V_{SENSE} in the eighth partition varies between 3.57 V and 3.62 V, as shown in Fig. 6. However, with the proposed RVM, the selected WL voltage is replaced from the V_{SW_DEF} to the V_{ASW}. Accordingly, the V_{SW8} (0.597 V) calculated in (1) is applied to the eighth partition. Since the selected WL voltage is replaced by 0.597 V from 1 V, the effective V_{SENSE} in the eighth partition is in the range 3.973 V to 4.023 V, close to the target V_{SENSE} (4V). As a result, with the proposed RVM, the variation of the effective V_{SENSE} is less than 0.05V regardless of the cell position in a BL, as shown in Fig. 6. By reducing the V_{SENSE} variation, the effective V_{th} of a cell detected by a SA is very close to the intrinsic V_{th}.

IV. EXPERIMENTAL RESULTS

In the case of I_{OFF} = 100 nA, Fig. 7 shows a comparison of a normal quantile plot with and without the RVM (n=8). The high I_{OFF} causes σ_V_{th} increase (a slope of graphs shown in Fig. 7), resulting in the SM degradation. However, with the proposed RVM, it is possible to compensate for the voltage drop induced by the high I_{OFF} and to achieve the improved SM. Despite the high I_{OFF}, the SM has extended from 105 mV to 395 mV with the RVM.

Table II compares the results of various RVM cases, where the number of partitions is 2, 4, 8, and 16. As the number of partitions increases, the RVM is more effective. Eventually, both σ_V_{th} and SM become closer to the intrinsic characteristics of cells. However, when comparing n=8 with n=16, there is no remarkable improvement in the results. Thus, considering the area efficiency and the circuit complexity for the RVM, the eight partitions are a reasonable choice.

V. CONCLUSION

This paper proposed the RVM to significantly reduce the effect of the leakage current, the sum of I_{OFF} of OTS selectors, in the cross-point OTS-PRAM. The OTS selector enables multi-stackable cell arrays, but the SM degradation is caused by the voltage drop due to the leakage current. The proposed RVM to resolve the BL voltage drop issue reduces the V_{SENSE} variation by applying the adaptive voltage to the selected WL. Even though this technique requires additional circuits for the BLC measurement and the V_{ASW} generation and the modified core decoder, the proposed RVM has high immunity to the leakage current as compared to a conventional read method. As a result, we successfully improved the SM (from 105mV to 395 mV) in the cross-point array with the high leakage current using the proposed RVM. With the proposed RVM, the cross-point OTS-PRAM will be more valuable for the cost-effective SCM application.

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