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A physics-based compact model for phase-change memory considering the ratio of vertical to lateral crystal growth rate for the design of cross-point storage-class memory

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ABSTRACT

A physics-based compact model for phase-change random access memory (PcRAM) was proposed considering the ratio of vertical-to-lateral crystal growth rate (α) and it was incorporated into HSPICE via Verilog-A. The proposed model was verified by using the experimental results taken from the 256 × 256 cross-point (X-point) PcRAM cell array with the $Ge_2Sb_2Te_5$ 2z-nm technology node. The proposed compact model successfully reproduced the measured PcRAM cell resistance (R_C) depending on the SET pulse width and amplitude after a background RESET, which is a challenging issue in the X-point PcRAM as the promising candidate for a

1. Introduction

With the advent of the memory-centric computing era, the demand for storage-class memory (SCM) with large capacity and high performance for data centers and cloud computing systems has exploded [1-4]. The SCM requirements, such as low latencies, byte-addressability, long-endurance, and persistency at low cost, are unable to be satisfied by the current NAND and DRAM technology [5]. Among the emerging nonvolatile memories with low latency and fair reliability, phase-change memory (PCM) has attracted much attention as a promising SCM candidate which can fill the performance gap between DRAM and 3-D NAND Flash [6]. Therefore, the read latency and cost-effectiveness of PCM need to be improved further to play the role of an SCM [7]. However, simple downscaling of the conventional PCM cannot achieve these improvements. Cross-point (X-point) PCM has emerged as a solution for these issues since it has not only an ultimate areal density of $4F^2$ and 3-D stackability for superior cost-effectiveness but also a low read latency [8].

Since the Intel-Micron announced the successful development and mass production for stackable 3-D X-point memory using an amorphous selector [9], many efforts have been made not only for the technological optimization for the PCM and selector materials but also in perspective of the compact model for the X-point-level memory design including the thermal/electrical disturbance and/or an analog modulation of PCM cell resistance in the viewpoint of neuromorphic application [10-11]. Very recently, the Hynix announced the successful development of high-performance and cost-effective X-point 2z-nm PCM technology for two-deck 128 Gb SCM with very low latencies of write (set < 300 ns) and read (< 100 ns) [12].

From the viewpoint of the compact modeling for the design of the X-point PCM, three issues need to be emphasized. First, there is a need for modeling that reflects the physical meaning while reducing the computational burden for heat distribution and thermal disturbance. The traditional line-type (L-type) PCM caused an asymmetric thermal disturbance due to the different thermal conductivity of phase-change material (along the bit line), oxide, and the interface (along the word line). In other words, the L-type PCM resulted in a more severe thermal disturbance since the accumulated heat was distributed more along the line direction than the other direction [2], [13-14]. And then, via the confined structures (C-type) of PCM for reducing the RESET current (I_{RESET}) and thermal disturb, the X-point PCM was spotlighted as abovementioned. Efforts to precisely calculate the structure-dependent thermal distribution would be significantly compromised with the compactness and computation efficiency (including acceptable convergence) of the models for the X-point PCM design. An efficient and natural approach to solving the trade-off among the precision, physics-based, and compactness is considering the ratio of vertical-to-lateral crystal growth rate.

Secondly, in the C-type or X-point PCM, which use the solid-phase crystallization, the SET operation is much more challenging rather than I_{RESET} in the perspective of the write latency and power consumption because the SET operation takes a much longer time than the RESET operation [15-16]. Thus, the resistance of PCM cell needs to be carefully characterized and reproduced by the compact model-based simulation, mainly depending on the SET pulse width and amplitude.

Finally, either the continuous change of PCM cell resistance or the dynamic variables such as a crystallization ratio and the size of conducting filament (CF), needs to be considered according to a write pulse. This model property is essential, especially in the PCM-based neuromorphic circuit simulations.

In this paper, we proposed a physics-based compact model for PcRAM (phase-change random access memory) considering the ratio of vertical-to-lateral crystal growth rate (α), incorporated it into HSPICE via Verilog-A, and verified it through the experimental results taken from the 256 × 256

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X-point PcRAM cell array with $Ge_2Sb_2Te_5$ (GST) 2z-nm t
successfully reproduced the measured PcRAM cell resistance (R_C) depending on the SET pulse width and amplitude while capturing the essence of physical meaning via the multi-domain simulation, including the threshold switching, electrical, thermal, and phase-change modules.

Furthermore, the proposed model was described as a voltage-driven model rather than a current-driven model because the input in a real circuit and the solution method in a circuit simulator usually take voltage as an input other than current.

2. Physics-based compact model for PcRAM simulation

2.1. Description of crystal volume, geometry, and the ratio of vertical-to-lateral crystal growth rate (α)

The structure and fabrication process was the same as [12] except excluding the selector. The 256 × 256 X-point PcRAM cell array with GST 2z-nm technology node was fabricated as a test pattern. The length (L_{gst}) and width (W_{gst}) of GST in the X-point PcRAM test pattern were 78 nm and 100 nm. The area of GST was 100 nm × 100 nm (W_{gst}^2).

After fully resetting (background RESET process), the crystal volume (V_c: CF volume) increases during the SET process. The SET time-evolution of V_c and the ratio of vertical-to-lateral crystal growth rate (α) were taken into account as shown in Fig. 1.

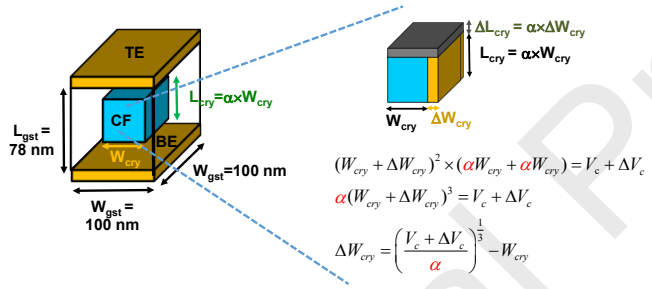

Fig. 1. Schematic view of the PcRAM cell structure illustrating the SET time evolution of the crystal CF volume.

If the V_c at a specific time spot ($t = t_0$) is $L_{cry}\times W_{cry}^2 = \alpha\times W_{cry}^3$, the V_c at the next time spot ($t = t_0+\Delta t$) is determined by both ΔL_{cry} ($= \alpha\times\Delta W_{cry}$) and ΔW_{cry}. Here, L_{cry}, W_{cry}, and α ($= L_{cry}/W_{cry} = \Delta L_{cry}/\Delta W_{cry}$) are the length of crystal CF, the CF width, and the ratio of vertical-to-lateral crystal growth rate, respectively.

2.2. Threshold switching

The ovonic threshold switching (OTS) is the most critical physical mechanism on PcRAM operation. Many studies suggest that OTS occurs in specific threshold electric fields of amorphous chalcogenide materials; various mechanisms have been introduced to address this [17-19]. We used a ballistic tunneling mechanism for OTS [20-21].

In the initial state of amorphous GST, steady-state electrons are trapped in the deep state (E_{T1}) near the Fermi level, as shown in Fig. 2(a). In this state, when a voltage is applied across amorphous GST, the electric field can be calculated by dividing the voltage by the length of amorphous GST length (L_{am}). The electric field supplies the energy for the electrons to facilitate tunneling from E_{T1} to the shallow state (E_{T2}) near the conduction band as shown in Fig. 2(b).

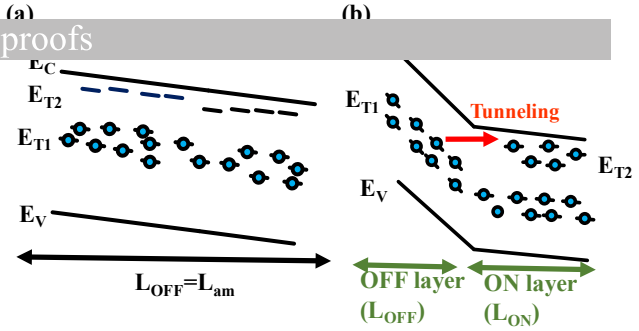

Fig. 2. Energy band of amorphous GST (a) before and (b) after OTS occurs.

Here, the tunneling rate can be defined as (1) [21]

$$\frac{d\Delta n_{t2}}{dt} = G_0 \exp\left(\frac{-B}{F_{OFF}}\right) - \frac{\Delta n_{t2}}{\tau_n} \tag{1}$$

where τ_n denotes an effective time for electron relaxation from E_{T2} to E_{T1}, B represents the Fowler–Nordheim tunneling characteristic constant [22], G_0 indicates maximum tunneling rate, F_{OFF} is the electric field across the OFF layer, and n_{t2} denotes electron density at E_{T2}. As the tunneling rate increases in a strong electric field, the electron concentration at the E_{T2} level increases, and the amorphous state becomes a high conductance state; thus, OTS occurs. Therefore, as shown in Fig. 2(b), electric field discontinuity occurs between the layers where electron concentration in E_{T2} is high (ON layer) and low (OFF layer). At this time, since E_{T2}–E_{T1} is the tunneling barrier, the length of the OFF layer (L_{OFF}) in which tunneling occurs can be defined as (2), and the length of the ON layer (L_{ON}) can be subsequently determined by (3).

$$L_{OFF} = \frac{E_{T2} - E_{T1}}{qF_{OFF}} \tag{2}$$

$$L_{ON} = L_{GST} - L_{OFF} \tag{3}$$

2.3. Electrical model

For amorphous GST, the electron transport model is based on the Poole–Frenkel emission model, and two activation energies are considered according to different trap levels of E_{T1} and E_{T2}, as shown by (4) [21], [24].

$$I_{am} = 2A_a\times q\times\frac{\Delta z_a}{\tau_0}n_{t1}\times\exp\left(-\frac{E_C-E_{T1}}{kT}\right)\times\sinh\left(\frac{qF\Delta z_a}{2kT}\right) + 2A_a\times q\times\frac{\Delta z_a}{\tau_0}n_{t2}\times\exp\left(-\frac{E_C-E_{T2}}{kT}\right)\times\sinh\left(\frac{qF\Delta z_a}{2kT}\right) \tag{4}$$

where q denotes unit charge, kT denotes thermal energy, n_{t1} indicates the trap concentration at E_{T1}, A_a denotes an amorphous area, Δz_a denotes an average distance between traps in amorphous GST, E_C means the conduction band minimum energy level, τ_0 indicates the electron characteristic time, and F denotes electric field (F_{OFF} before OTS and F_{ON} after OTS). Before/after OTS, the electric field of the current model (4) is defined differently, as shown by (5).

Journal Pre-proofs

$$= \frac{V}{L_{ON}} \quad (\text{Before OTS})$$

$$= \frac{V}{L_{am}} \quad (\text{Before OTS})$$

After OTS, F_{OFF} is obtained by inverting the current equation, as shown by (6); it can be used again to define the tunneling rate (1) and L_{OFF} (2).

$$F_{OFF} = \frac{2kT}{q\Delta z}\sinh^{-1}\left(\frac{\tau_0 I_{am}}{2A_a q\Delta z_a n_{t1}\times\exp\left(-\frac{E_C - E_{T1}}{kT}\right)}\right) \tag{6}$$

When OTS occurs, although the GST is in an amorphous state, the current increases to a sufficiently high value for the GST to reach crystallization temperature. When crystallization occurs, the electron transport model of GST is changed into the ohmic model, defined by (7) [25].

$$I_{cry} = A_c \times \frac{q\mu n_c}{L_{cry}} \times \exp\left(\frac{-E_{a\_c}}{kT}\right) \times V \tag{7}$$

where μ denotes the electron mobility in crystalized GST, n_c denotes electron concentration in the crystalized GST, L_{cry} denotes the length of crystal CF, and E_{a_c} indicates the activation energy of the crystal GST resistivity. Depending on the state of the GST phase, amorphous or crystal current models (I_{am} or I_{cry}) can be used, which will be discussed in Section 2.6.

2.4. Thermal model

The thermal model is based on Fourier's law [26], which is defined by (8)

$$T = T_0 + P \times R_t \tag{8}$$

where T is temperature as the function of position, T_0 is the temperature at a reference position, P is the dissipated power between the T and T_0 positions, and R_t is thermal resistance. The temperature is distributed spatially point by point, and then the P is calculated spatially and time-by-time depending on R_t.

P can be calculated by the current flowing through the GST and the voltage applied between the top electrode (TE) and the bottom electrode (BE). Besides, T_0 plays the role of boundary condition, which can be, for example, the temperature outside the GST. By updating the equivalent R_t according to the SET time-evolution of CF, we can simplify the complicated effect of thermal distribution, capturing the essence of the influence of thermal distribution on the direction-dependent crystallization rate of GST. It relieves the computing burden of a compact model without losing the physical parameters and their meanings, which will be explained the Section 2.6.

2.5. Phase change model

The phase change model consists of melting, cooling, and crystallization, and two types of crystallization mechanisms, i.e., nucleation and growth, need to be addressed [27-28]. [illegible], if the cooling process is performed rapidly under crystallization temperature, the GST hardens into an amorphous state [29]. These mechanisms can be expressed by (9) and (10), respectively,

$$\frac{dV_m}{dt} = \frac{\gamma_m}{1+\exp(-\frac{T-T_m}{H_m})} \tag{9}$$

$$\left(\frac{dV_a}{dt}\right)_{cooling} = \frac{\gamma_c}{1+\exp(\frac{T-T_c}{H_c})} \quad (V_m > 0) \tag{10}$$

where γ_m and γ_c denote the melting and cooling probability. T_m and T_c also denote the melting and crystallization temperature, and V_a and V_m mean the amorphous and melted volume of GST, respectively. H_m and H_c are the fitting parameters describing the melting and cooling, respectively.

Then, the nucleation rate of GST is given by (11),

$$\left(\frac{dV_c}{dt}\right)_{nucle} = P_{n0}\exp\left\{-\frac{1}{kT}\left(E_{a\_n} + \frac{\beta_n^2}{\left(1-\frac{T}{T_m}\right)^2}\right)\right\} \times V_{GST} C_a \tag{11}$$

where V_c denotes the crystal volume, P_{n0} means the crystallization probability by nucleation mechanism, E_{a_n} denotes nucleation activation energy, β_n denotes the fitting parameter, V_{GST} denotes the GST volume, and C_a means the amorphous volume ratio and is given by V_a/V_{GST} with V_a = the amorphous volume. The nucleation mechanism originates from the nucleus of amorphous GST, and the crystallization rate with the nucleation mechanism is proportional to the volume of amorphous material V_a, as shown in (11).

On the other hand, the growth rate of GST is given by (12),

$$\left(\frac{dV_c}{dt}\right)_{gro} = v_{g0}\times\exp\left(-\frac{0.8T_m}{T_m - T}\right)\times\left[1-\exp\left(-\frac{\Delta G}{kT}\right)\right] \times\exp\left(-\frac{E_{a\_g}}{kT}\right)\times\frac{S_a}{S_{a\max}} \tag{12}$$

where v_{g0} denotes the fitting parameter, ΔG denotes the excess Gibbs free energy of the amorphous phase over the crystalline solid, E_{a_g} denotes growth activation energy, S_a denotes amorphous-crystal cross-section area, and S_{amax} denotes the maximum amorphous-crystal cross-section area. Noticeably, since the growth-based crystallization occurs at the boundary between amorphous and crystal GST, the growth-based crystallization rate is proportional to the interface area of the two material states, as shown by (12).

The equations (9)-(12) describe the time-temperature-transformation (TTT) characteristic curve, which expresses the phase transformation in combination with time and temperature. From the TTT curve, the phase change of GST can be traced time-wise, depending on temperature and time. In our transient simulation, the SET

time-evolutions of L_{cry} and W_{cry} are calculated by updating V_c a

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$$\Delta V_c = \left[\left(\frac{dV_c}{dt} \right)_{nucle} + \left(\frac{dV_c}{dt} \right)_{gro} - \left(\frac{dV_a}{dt} \right)_{cooling(V_m>0)} \right] \Delta t \quad (13)$$

where Δt denotes the time step in a transient simulation.

2.6. Compact model-based multi-domain simulation

It is assumed that in a C-type structure without a heater, the internal temperature of the GST increases from the GST center position. Therefore, the phase change also begins at the center of the GST, as shown in Figs. 3(a) and (d). Then, we can describe the shape of the crystal structure determined by the complex thermal distribution using parameter α.

Thanks to α, we can reflect a variety of possibilities for the phase-change rate varied depending on the direction, temperature distribution, and X-point aspect ratio, as shown in Fig 3.

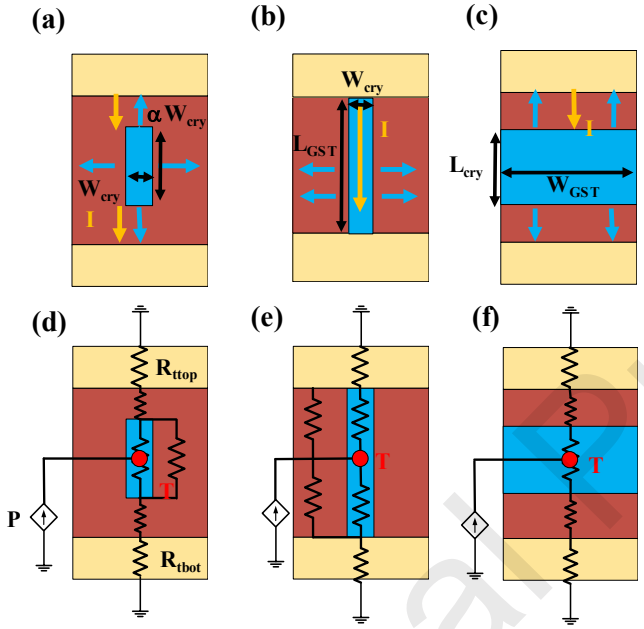

Fig. 3. The SET time-evolution of CF in the viewpoint of the electrical (a), (b), (c) and thermal (d), (e), (f) model. (a), (d) The crystal volume reaches neither the electrode nor the GST wall. (b), (e) The crystal volume reaches the electrode first (large α). (c), (f) The crystal volume reaches the GST wall first (small α).

After a background RESET, the SET time-evolution of CF is illustrated from the viewpoint of the electrical model in Figs. 3(a)-(c). If the crystallization rate in the vertical direction is relatively high (large α), the CF evolves from Fig. 3(a) to Fig. 3(b). In contrast, when the crystallization rate along the lateral direction is relatively high (small α), it evolves from Fig. 3(a) to Fig. 3(c). When the CF reaches the electrode first [Fig. 3(b)], amorphous and crystal volumes form in parallel, so the amorphous current with low conductance is ignored, and the crystal current model is followed. In the other case, the amorphous and crystal volumes are connected in series [Fig. 3(c)], so the amorphous current model is followed, as shown by (14).

$$I = \begin{cases} I_{am} & (L_{cry} < L_{GST}) \\ I_{cry} & (L_{cry} = L_{GST}) \end{cases} \quad (14)$$

From the viewpoint of the thermal model, the SET the case of the electrical model, if the crystallization rate in the vertical direction is relatively high (large α), the CF evolves from Fig. 3(d) to Fig. 3(e). In contrast, when the crystallization rate along the lateral direction is relatively high (small α), it evolves from Fig. 3(d) to Fig. 3(f). Thus, the effect of thermal distribution can be concisely calculated by updating R_t in (8) and by tracking the temperature in the center of GST, as shown by (15)

$$R_t = R_{ttop} + R_{tbot} + \frac{1}{2}\left[\sigma_a \frac{L_{GST} - L_{cry}}{W_{GST}^2} + \left(\sigma_a \frac{L_{cry}}{W_{GST}^2 - W_{cry}^2} \| \sigma_c \frac{L_{cry}}{W_{cry}^2} \right) \right] \quad (15)$$

where σ_a and σ_c denote the thermal conductivities of amorphous and crystal states, and R_{ttop} and R_{tbot} mean the thermal resistances of top and bottom electrodes.

The SET time-evolution of CF is calculated as follows. The crystal volume is determined by both the updated ΔV_c from (13) and parameter α. If the CF reaches neither the electrode nor the GST wall ($L_{cry} < L_{GST}$ and $W_{cry} < W_{GST}$), the CF is updated, as shown by (16) and Fig. 4(a).

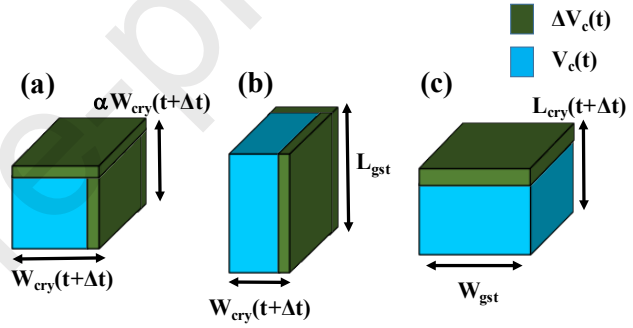

Fig. 4. The SET time-evolution of CF during the SET time step Δt in crystallization. (a) When CF reaches neither the electrode nor the GST wall, (b) when CF reaches the electrode first, and (c) when CF reaches the GST wall first.

$$W_{cry}(t+\Delta t) = \left(\frac{V_c(t) + \Delta V_c}{\alpha} \right)^{\frac{1}{3}} \quad (16)$$

Furthermore, if the CF reaches the electrode first ($L_{cry} = L_{GST}$ and $W_{cry} < W_{GST}$), the CF evolves, as shown by (17) and Fig. 4(b).

$$W_{cry}(t+\Delta t) = \sqrt{\frac{V_c(t) + \Delta V_c}{L_{gst}}} \quad (17)$$

Finally, if the CF reaches the GST wall first ($L_{cry} < L_{GST}$ and $W_{cry} = W_{GST}$), the CF is updated, as shown by (18) and Fig. 4(c).

$$L_{cry}(t+\Delta t) = L_{cry}(t) + \Delta L_{cry} \quad (18)$$

Figure 5 shows the simulation sequence of the proposed multi-domain compact model. Furthermore, Fig. 6 shows the simulated I-V characteristic of PcRAM cell depending on temperature. The snap-back is well reproduced. Here, it should be noted that the threshold switching voltage is independent of temperature, which is reasonable because, in

our model, the OTS occurs by the temperature-independent b

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characteristic agrees well with the measured one, which

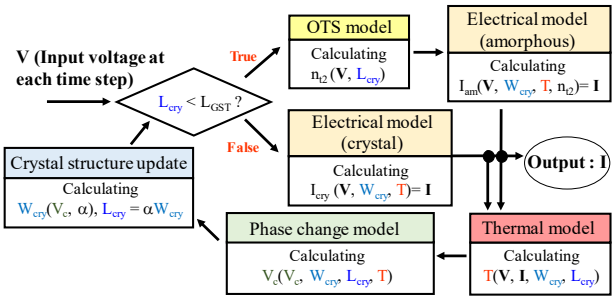

Fig. 5. Simulation sequence of the proposed multi-domain compact model.

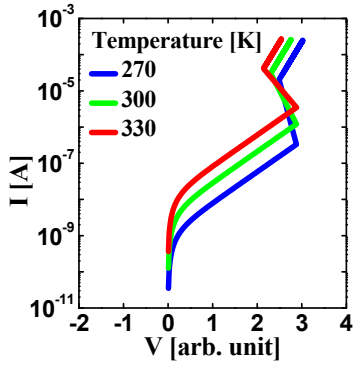

Fig. 6. Simulated I-V characteristic of PcRAM cell depending on temperature.

Figure 7 shows the simulated quenching time-dependence of R_C during RESET operation. As the quenching time (t_Q) increases, the R_C after RESET decreases. It is because the longer t_Q, the more time margin for the amorphization process is performed. In other words, the PcRAM cell has the duration enough to be further amorphized.

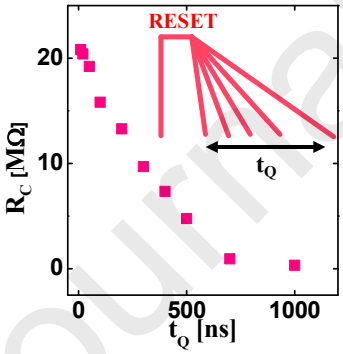

Fig. 7. (a) simulated quenching time-dependence of RC during RESET operation

Our results suggest that our multi-domain model is reliably computing the electrical and thermal as well as the phase-change and OTS properties of GST material and PCM cell.

3. Model verification by comparing experimental results

To verify our model, we compare the simulation results with the measured ones. Extracted parameters are summarized in Table I.

Figure 8 shows the I-V characteristic of the PcRAM cell in the center position of the 256 × 256 cell array. The parasitic resistance from the metal pad to the PcRAM cell (from the bit line pad via the target cell to the word line pad) in the X-point array was extracted to be 10 kΩ. The simulated I-V

Table I. Extracted model parameters

Domain	Parameter	Value	Unit
-	α	1.55	-
	Δt	1	ns
Electrical model (Amorphous)	q	1.6×10^{19}	C
	n_{t1}	1×10^{19}	cm^{-3}
	Δz_a	2	nm
	τ_0	5×10^{-14}	s
	E_C-E_{T1} and E_C-E_{T2}	0.25 and 0.01	eV
Electrical model (Crystal)	E_{a_c}	0.14	eV
	n_c	1×10^{22}	cm^{-3}
	μ	4.69×10^{3}	$cm^2/(V\cdot s)$
OTS	τ_n	1	ns
	B	4×10^{5}	cm/V
	G_0	1×10^{27}	cm^{-3}/s
Thermal model	σ_a and σ_c	0.01 and 0.015	W/(cm·K)
	R_{ttop} and R_{tbot}	6×10^6 and 6×10^6	K/W
Phase change model	γ	7.73	(J/cm^2)
	$E_{a,n}$ and $E_{a,g}$	0.94 and 0.73	eV
	P_{n0}	3.84×10^{11}	s^{-1}
	v_{g0}	13.35	$cm\cdot s^{-1}$
	β	1	-
	r_m and r_c	1×10^{-11} and 1×10^{-11}	$cm^3\cdot s^{-1}$
	H_m and H_c	5 and 5	K
	T_m and T_c	889 and 450	K
	Δh_1	453	J/cm^3

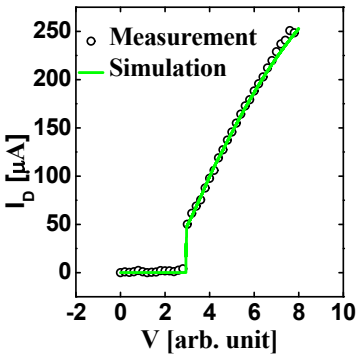

Fig. 8. The simulated and measured I-V characteristic of the PcRAM cell in the center position of the 256 × 256 cell array.

In order to further verify the proposed model, the resistance of PcRAM cell R_C was characterized depending on the SET pulse width and amplitude after a background RESET. As mentioned in the Introduction, in the X-point PCM, the SET operation is much more challenging rather than I_{RESET} in the perspective of the write latency and power consumption. Thus, the R_C needs to be carefully characterized and reproduced by the compact model-based simulation, depending on the SET pulse width and amplitude.

The measurement sequence is illustrated in Fig. 9.

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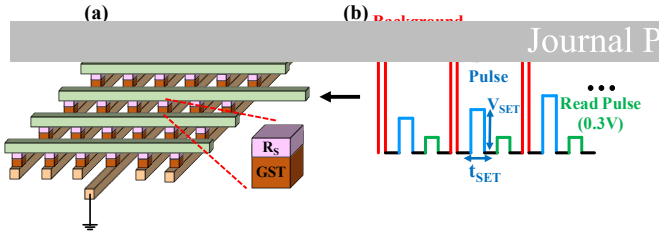

Fig. 9. (a) 256 × 265 cell array with series resistance R_S and GST stacked and (b) the pulse sequence of the background RESET → SET → Read, where both the amplitude and width of the SET pulse were changed. R_C is readout by applying V= 0.3 V.

Pulse measurements were performed with series resistance (R_S) to suppress excessive current, as shown by Fig. 9(a). For pulse measurement, the pulse sequence consists of background RESET pulse, SET pulse, and read pulse, as shown by Fig. 9(b). The background RESET pulse was used to ensure the GST was fully amorphized. In fully amorphous GST, crystallization is performed by applying SET pulse. We split the amplitude of the SET pulse (V_{SET}) and the width of the SET pulse (t_{SET}). After SET pulse, a Read pulse of 0.3 V was applied to measure the GST current. We calculated the GST resistance R_C at this point, which allowed us to analyze the crystallization properties.

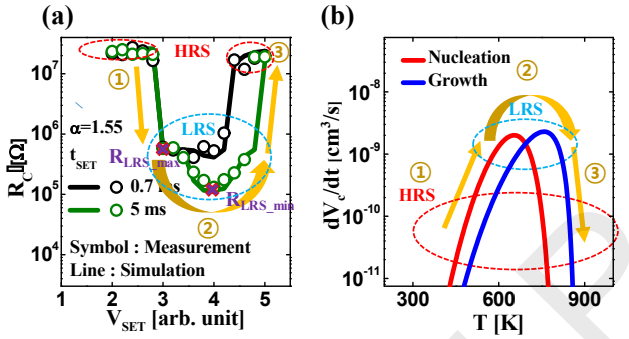

Fig. 10. (a) Measured and simulated R_C depending on V_{SET} and t_{SET}. (b) TTT curve is defined by (11) and (12).

Figure 10(a) shows the pulse measurement and simulation results. In the write operation, where V_{SET} and t_{SET} are determined, the following behavior exists: The larger the crystal volume, the lower the GST R_C taken from the 0.3-V Read pulse. By analyzing the trend of the measured data, it is evident that R_C follows a U-shape according to V_{SET}, as shown by Fig. 10(a) ①→②→③. This is because, when V_{SET} increases, the temperature inside the GST increases, so it follows the trend of the TTT curve of Fig. 10(b) ①→②→③. Regardless of pulse width, the R_C changes from the high resistance state (HRS) to the low resistance state (LRS) abruptly, as shown in Fig. 10(a) ①. From this trend, since OTS occurrence is independent of t_{SET}, we can assume that OTS occurs in Fig. 10(a) ①, and crystallization occurs in the GST. However, the voltage that changes from LRS to HRS (as seen in Fig. 10(a) ③) increases as t_{SET} increases.

When a long SET pulse is applied (longer t_{SET}), crystallization time increases, but overall resistance reduces. By analyzing Fig. 10(b) ③, it is interpreted that the crystallization rate decreases as temperature increases, which suggests that, when t_{SET} is long, the GST is in the LRS.

Undoubtedly, it is essential to use an appropriate value of α to reproduce the trend of Fig. 10(a) in the simulations. The α value was extracted as follows. First of all, R_{LRS_min} is taken ned that the GST is 100% crystal when $R_C = R_{LRS\_min}$ in Fig. 10(a). Then, R_{LRS_max} is taken from the maximum R_C in the LRS domain in Fig. 10(a), and it is assumed that the crystal immediately reaches both electrodes. Since the cross-sectional area of the crystal pillar (W_{cry}^2) and R_C is inversely proportional, the crystal pillar width and the α can both be calculated by (17).

$$\alpha = \frac{L_{GST}}{W_{cry\_init}} = \frac{L_{GST}}{W_{GST}\sqrt{\frac{R_{LRS\_min}}{R_{LRS\_max}}}} \quad (17)$$

where W_{cry_init} denotes the crystal pillar width when $R_C = R_{LRS\_max}$. In this way, the α was extracted to be 1.55.

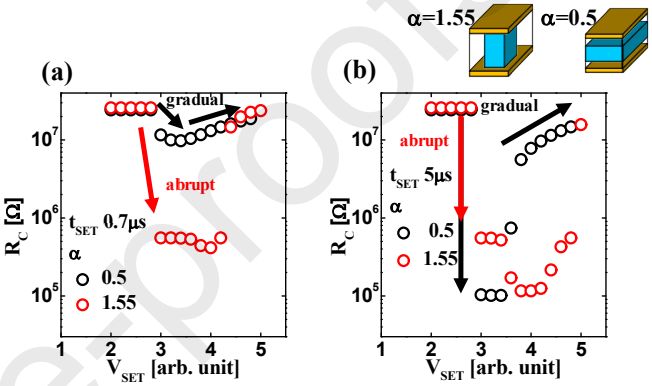

Fig. 11. R_C -V_{SET} simulation result with α=1.55, α=0.5 and different t_{SET}. (a) t_{SET} =0.7μs and (b) t_{SET} =5μs.

We can also simulate the effect of α on the R_C –V_{SET} characteristics. Figure 11 compares the R_C –V_{SET} curves for α = 1.55, where the CF reaches the electrodes in the SET process, as well as for α = 0.5, where the CF reaches the GST wall in different t_{SET} = (a) 0.7 μs and (b) 5 μs. As shown in Fig. 11(a), when α = 1.55, crystal and amorphous GST form in parallel, and abrupt switching characteristic is observed; when α = 0.5, crystal and amorphous GST form in series, and gradual switching characteristic is observed.

However, as shown in Fig. 11(b), since t_{SET} is long enough for the GST to be entirely crystallized, abrupt characteristics are observed for both α = 0.5 and α = 1.55. Moreover, in Fig. 11(b), when α = 0.5, under the condition of low crystallization rate, the gradual characteristic is observed for the same reason as the case of α = 0.5 in Fig. 11(a).

These results suggest that by employing the ratio of vertical-to-lateral crystal growth rate α, the R_C in the 2z-nm technology node X-point PcRAM can be reproduced depending on the SET pulse width and amplitude without a heavy computing burden. Furthermore, it is found that the V_{SET}-dependent abrupt/gradual change of R_C is sensitive to α, which means that α should be carefully optimized for the PCM-based neuromorphic applications.

4. Conclusion

A physics-based compact model for PcRAM was proposed considering the ratio of vertical-to-lateral crystal growth rate α, and it was incorporated into HSPICE via Verilog-A. The proposed model was verified by using the experimental results taken from the 256 × 256 PcRAM cell array with 2z-nm GST X-point technology. The proposed

compact model successfully reproduced the measured I
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and amplitude while capturing the essence of physical meaning via the multi-domain simulation, which includes the threshold switching, electrical, thermal, and phase-change modules.

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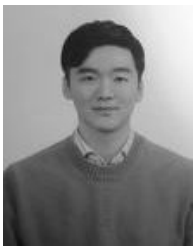

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Highlight

- ✓ We proposed a physics-based compact model for phase-change random access memory (PcRAM).
- ✓ The ratio of vertical-to-lateral crystal growth rate (α) was incorporated into HSPICE via Verilog-A.
- ✓ The proposed model was verified by using the experimental results taken from the 256×256 cross-point (X-point) PcRAM cell array with the $Ge_2Sb_2Te_5$ 2z-nm technology node.
- ✓ Furthermore, we found that the SET pulse-dependent abrupt/gradual change of PcRAM resistance is sensitive to α.

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