Non-Resistance Metric based Read Scheme for Multi-level PCRAM in 25nm Technology

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***Abstract* — A non-resistance readout scheme for high density multi-level PCRAM is described. Non-resistance read metric with drift resilient nature is enhanced to be suitable for high density memory array with large parasitic time constant. 1G PCM cells in 25nm technology are structured in the form of a single bank of a 16G cell chip with the hierarchical bit-line scheme. Furthermore, 32 instances of 6bit SAR-ADC per bank are built-in with specific logic for adaptive data detection as a sense-amplifier. Experimental results for a bank of 2Gb multi-level density are demonstrated with total read latency of 450ns including word-line settling and the adaptive data detection scheme.**

***Index Terms* — high density multi-level PCRAM, temporal drift mitigation, temperature compensation.**

I. Introduction

Phase change random access memory (PCRAM) has emerged as one of the leading candidates for non-volatile memory (NVM) technology due to its high bandwidth, endurance and scalability. Considering cost-effectiveness, which is key requirement to be competitive in newly emerging memory market, i.e. storage class memory system, the multi-level cell (MLC) capability of phase change material (PCM) makes PCRAM more attractive for increasing memory density and reducing cost-per-bit [1]. Despite the promising MLC capability of PCRAM, most of previously demonstrated high density PCRAM designs have proposed single-level cell (SLC) operation [2]. This is mainly because of the temporal drift of stored resistance levels which causes overlap between stored levels over time resulting in shorter retention. Recently, a non-resistance based read metric (M-metric) has been shown to be resilient to temporal drift. In our work, a 32Gbit-ready multi-level PCRAM which adopts 'M-metric' is described. The 'M metric' based read scheme has been further enhanced to be suitable for high density cell array (~1G cells per bank).

II. Non-Resistance Read Metric

Conventionally, the PCM cell state as well as many of other resistive memories are read by sensing the current when the fixed low voltage (V_{READ} in Fig. 1 (a)) is applied. This traditional resistance metric, also known as the 'low field electrical resistance metric (R-metric)' suffers from severe temporal-drift of its programmed resistance. The drift effect has been modeled by power-law empirically, i.e. $R(t)/R(t_0)=(t/t_0)^{\nu}$, where the exponent ν is the drift coefficient. Typical value of the drift coefficient for R-metric is in the order of 0.1 for high resistive states, which makes it challengeable to realize MLC capability of PCM [3]. As an alternative read metric to mitigate the temporal drift effect, the 'M metric' has been proposed [4] where the fixed read current (I_{DET} in Fig. 1 (b)) is forced through the PCM cell and the voltage across the cell, i.e., the 'M-metric' value, is sensed. The M-metric value is weak function of the activation energy, the variation of which is believed to cause temporal drift. In case of M metric, the drift effect can also be modeled by power-law, $M(t)/M(t_0)= (t/t_0)^{\nu}$ and its exponent is in the order of 0.01. Despite of its merits, 'M metric' has an inherent drawback of long latency, mainly because the tiny current of ~1uA is not sufficient to settle the voltage of the bit-line with large parasitic capacitance within practical time.

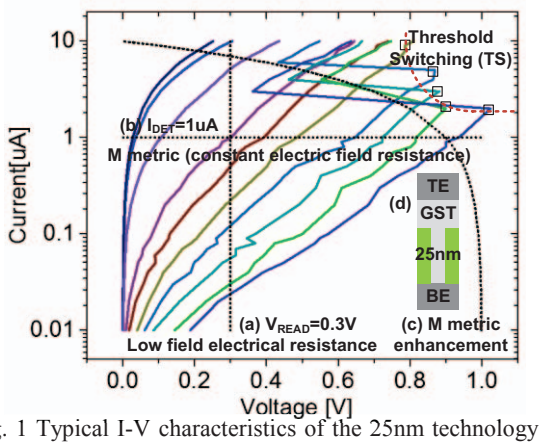

Fig. 1 Typical I-V characteristics of the 25nm technology PCM cell are shown with various read metric line, (a) low field electrical resistance metric (b) constant electric field resistance (M-metric) and (c) enhancement of 'M metric'. The squares denote threshold switching (TS) point. The PCM cell structure is sketched in (d).

A. M-metric enhancement

When determining the value of V_{READ} or I_{DET}, the most important criterion is preventing the read disturbance

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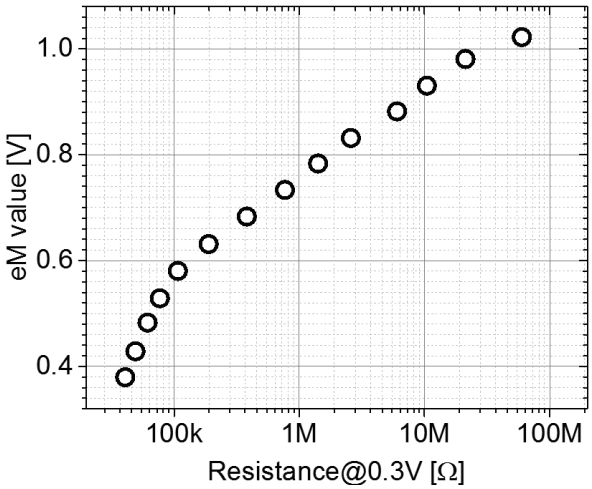

Fig. 2 The measured eM-metric values are scattered versus the traditional low field electrical resistance metric. Both are measured with selector device and ~15KΩ parasitic resistance.

caused by the sensing-line crossing with the TS line. As shown in Fig.1 (a), (b), the constant voltage or current for read operation should have enough margin to the TS level as well as the molten level (not shown in the graph). This makes the read voltage (~0.3V) or current (~1uA) too small, and results in noisy sensing and long latency. Of interest is how the read voltage/current can be increased while having sufficient margin between sensing-line and molten/TS level. To enhance the latency of M-metric, increasing read current is essential as well as decreasing its time constant. For this purpose, 10 times larger current (10uA) is adopted in enhanced M-metric. To secure enough margin between the sensing-line and TS line, a resistor of 100KΩ (called bleeding resistor) is connected with the bit-line in parallel and bleeds the excess current to common ground [5]. This enhancement makes the sensing-line linear with negative slope, as shown in Fig.1 (c) on logarithmic axis. Increasing read current helps achieving much shorter settling time as well as more-resilience to temporal drift and noise. Fig.2 shows the enhanced M-metric values (called eM-metric) versus traditional resistance metric. Compared with normal M-metric which is perfectly linear function of log(resistance), slight distortion is introduced on lowest and highest resistance region by enhancement. This slightly distorted characteristics of enhanced M-metric causes the sensing range to shrink a little. However, the slightly reduced sensing range rarely affects proper MLC binning and sense-amp operation.

B. Performance of enhanced M metric

To verify the drift-resilient nature of eM-metric, pristine cells are programmed and grouped to the various voltage

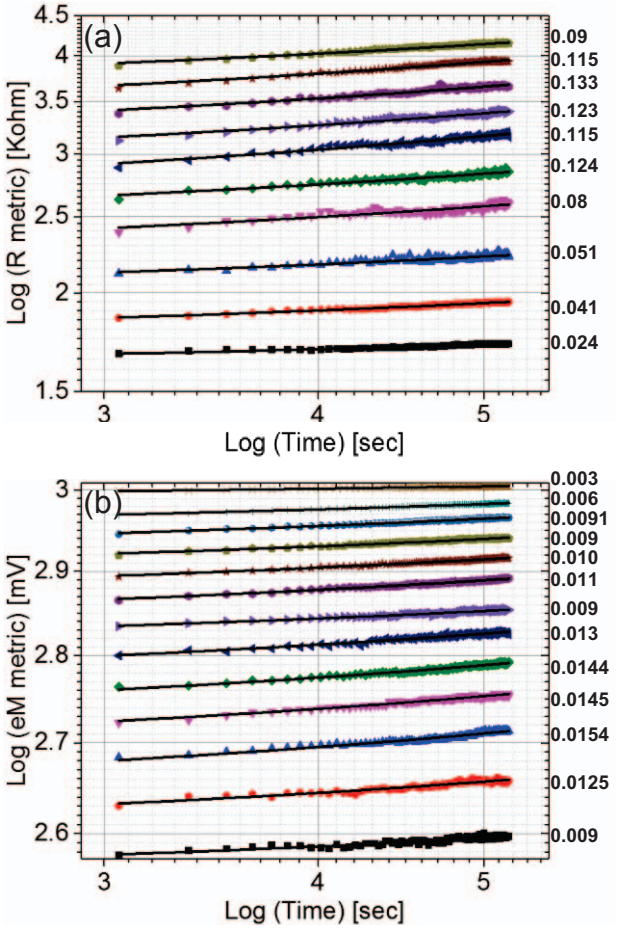

Fig. 3 The temporal drift of (a) low field electrical resistance metric and (b) eM-metric are measured. The extracted drift exponent of each metrics and each levels are denoted at the right of the graph.

levels and measured over time by eM-metric and R-metric at nearly the same time. Fig.3 shows the experimental results of drifted metric over time. Along bi-logarithmic axis, both metric values can be fitted to the straight line, where the slope of the linearly fitted line is the drift exponent of each metric. Note that the drift exponent depends on the corresponding initial programmed level. The extracted drift exponent of R-metric varies up to 0.133, whereas on the other hand, that of eM-metric is less than 0.0154 as shown in Fig.3 (a), (b).

C. Temperature Dependency

The temperature dependency of the PCM cell state is one of the crucial challenges to be overcome to achieve MLC functionality. In case of the eM-metric, the resistance of the bleeding resistor which consists of n+ doped silicon increases proportionally to the temperature, while the PCM cell which consists of chalcogenides material (its current flows could be described by Poole-

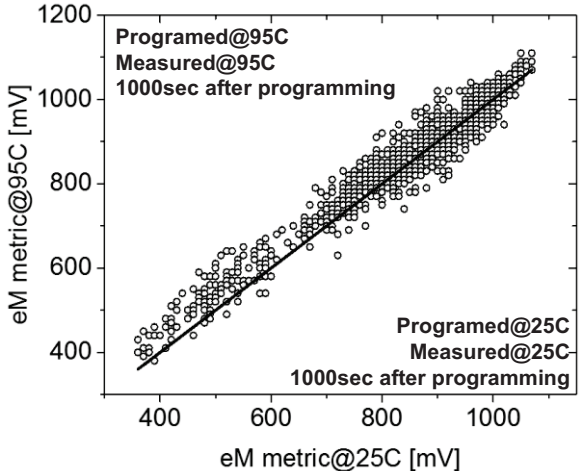

Fig. 4 The same PCM cells are programmed with identical current pulses at 95C and 25C each and its eM-metric values are measured at 1000sec after programming and scattered with insensitive line with unit slope.

Frenkel conduction.) exhibits lower resistivity as the temperature increases. By connecting these complementary materials in parallel, the dependency on the temperature can be effectively compensated. Fig. 4 shows the measured sensitivity of the eM-metric on the temperature. The PCM cells are programmed and measured at room temperature and at high temperature identically. Despite the intra-cell variability (the metric value fluctuation of identical cell even though identical program pulses are applied) and slightly up-biased results of SET-like region, the measured eM-metric values at high temperature are analogous to those of room temperature to be scattered on the line with unit slope as shown in Fig. 4.

III. Chip Architecture, Read Circuitry and Measurement

A. Chip Architecture

The proposed PCRAM chip is fabricated in 25nm PCM cell technology. The memory element is composed of 1 access device and 1 PCM cell, where the PCM cell is a cylindrical confined structure of the Ge-Sb-Te material and formed between top and bottom electrodes (TE, BE) as shown in Fig. 1(d). The bank of 2Gb density, which has physical 1G cells in multi-level (2 bits/cell) scheme, is structured into 128 tiles, 8 by 16 arrays. One tile is a matrix of 4K bit-lines (BLs) and 2K word-lines (WLs) for the size of 8Mb (excluding redundant elements). The PCM cells reach the sense amplifier through the hierarchical bit-line structure i.e. vertical global bit-line (GBL), horizontal local bit-line (LBL) and bit-line,

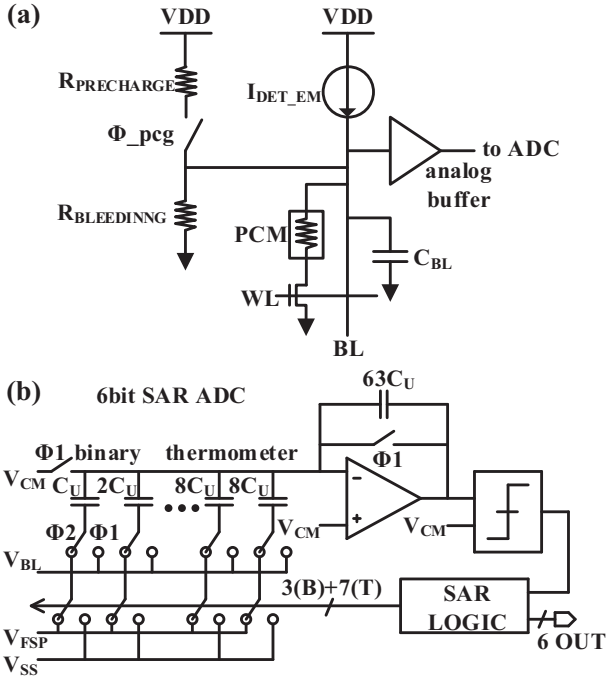

Fig. 5 (a) The readout circuitry for enhanced-M metric. (b) 6bit SAR-ADC which is adopted as a sense amplifier consists of capacitive DAC using VNCAP, comparator and SA logic circuit.

respectively. Each bank has 32 GBLs laid over the whole bank vertically. (4 GBLs per one tile) The GBL is connected to the LBLs which are laid over the whole bank horizontally and shared by every 2 tiles in WL direction. Subsequently, the LBL is connected to the BLs which are laid to be shared by every 2 tiles in BL direction. Note that the shared and hierarchical LBL & BL scheme can reduce the number of switch, however it leads the heavy parasitic RC to the chain of bit-line. Most of parasitic resistance (25KΩ) comes from the bit-line which has minimum metal width (~25nm) across the length of 2K word-lines. And GBL/BL has large parasitic capacitance (slightly less than 2pF) which has long length/narrow space over the vertical direction of whole bank/tile. As a consequence, it is important to overcome the huge parasitic RC of this high density memory chip architecture.

B. Read Circuitry

Fig. 5 (a) shows the readout circuitry for enhanced M-metric. To elevate the voltage of bit-line much faster, one more additional resistor ($R_{PRECHARGE}$) is introduced in read circuitry. When the voltage of bit-line starts to elevate, the bit-line is forced to VDD through $R_{PRECHARGE}$ for pre-charging phase, where the bit-line voltage accelerates to be close to the finally-settled value. The duration of the pre-charging phase should be carefully set to have enough margin between the pre-biased level and molten/TS level.

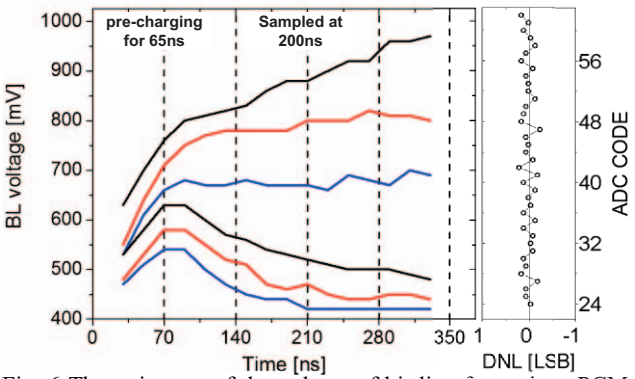

Fig. 6 The trajectory of the voltage of bit-line for various PCM state. The right graph shows the measured differential non-linearity of 6bit SAR-ADC.

After the pre-charging phase, the current source of I_{DET} is forced through the bit-line and settles the bit-line voltage (V_{BL}) to be proportional to the PCM cell's state. Note that V_{BL} does not need to be fully-settled but to be sufficient to resolve 2b states at the endmost read process. To resolve 2bit data from eM-metric values without reference cells, a frame of 32 PCM cells which should be read or programmed simultaneously is introduced. Every cell in a frame drifts with temporally and statistically similar manner because they are programmed at the same time. The eM-metric values of 32 cells in a single frame are converted into 6bit digital code by SAR-ADC per GBL (Fig. 5 (b)) and the converted codes are fed to a logic that implements adaptive data detection (details can be found in [6]) The key requirement of the ADC (c-DAC) for successful data detection is the monotonicity. The 6bit capacitive DAC of SAR-ADC is segmented to 2bit-binary (LSB) and 4bit-thermometer (MSB) code but the vertical natural capacitor array is not split to take precisely-matching property of the common-centroid layout.

IV. Measurement

Fig. 6 shows the tracked voltage of the bit-line over time for several typical states of PCM cell. Regarding the full dynamic-range of MLC state which means the range from the lowest SET to the highest RESET, the voltage of bit-line can be settled to be sampled at 200ns including 65ns pre-charging phase. Note that the highest state does not need to be fully-settled. With 40ns for the WL settling and 60ns for the ADC operation (not shown in Fig. 6), 300ns is needed to get 6bit code of the raw data of eM-metric. Subsequently, 6bit code is decoded to 2bit data by a logic circuit spending another 150ns. Totally the read latency (from WL to data-out) can be achieved to be 450ns. Fig. 6 also shows the typical DNL of one of 32 ADCs in a bank over the whole input range of MLC PCM.

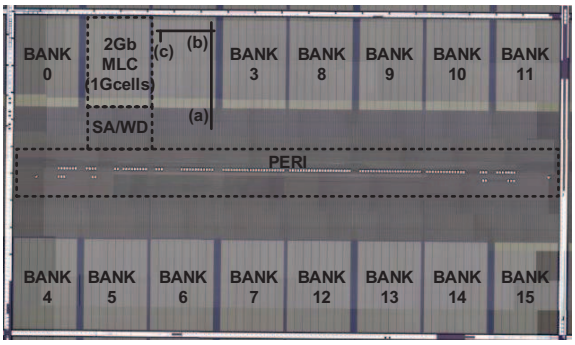

Fig. 7 The micro-photography of the fabricated die. The direction of the hierarchical bit-line structure is briefly denoted as (a) GBL, (b) LBL and (c) BL, respectively.

It shows that the measured DNL is less than 0.5LSB, which means that the monotonic characteristics are achieved. Fig. 7 shows the micro-photography of the fabricated die. The full chip has 16 banks of 1G cells each within practical die size, exhibiting 32Gb multi-level density.

V. Conclusion

The non-resistance read metric (called eM-metric) to mitigate the temporal drift for the high density multi-level PCRAM is demonstrated using a 1G cells bank of PCM chip. The enhanced-M metric shows drift resilient nature and temperature insensitivity with total 450ns read latency despite large parasitic time constant arising from the high density cell array.

Acknowledgement

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