Signal Integrity Design and Analysis of 3-D X-Point Memory Considering Crosstalk and IR Drop for Higher Performance Computing

Kyungjune Son, *Student Member, IEEE*, Kyungjun Cho, Subin Kim, Shinyoung Park, Daniel H. Jung, Junyong Park, Gapyeol Park, Seongguk Kim, Taein Shin, Youngwoo Kim, *Member, IEEE*, and Joungho Kim, *Fellow, IEEE*

***Abstract*— In this article, we, for the first time, used signal integrity (SI) to design and analyze 3-D X-Point memory, including a phase-change memory (PCM) cell, ovonic threshold switch (OTS) selector, interconnection lines, and peripheral circuits. With the narrow space and the long interconnection lines that come with 20-nm process technology, crosstalk and IR drop can degrade the voltage margin of the memory cell and affect the memory operation. For SI analysis considering crosstalk and IR drop, the unit size of the memory array tile was considered in designing the interconnection lines. Crosstalk and IR drop are analyzed using full 3-D electromagnetic and circuit simulations. To cover practical conditions, the PCM cell and OTS selector are modeled as behavior models using Verilog-A modules, respectively. Also, the word lines (WLs) and bit lines (BLs) of 3-D X-Point memory are modeled to resistance and capacitance by ANSYS Q3D extractor. The core peripheral circuits, such as decoder, sense amplifier, and analog-to-digital converter, are included in the circuit simulation. To verify the proposed design and analysis, a transient simulation was conducted considering crosstalk and IR drop of 3-D X-Point memory. A tradeoff relationship between crosstalk and IR drop in the interconnection designs was verified. Additionally, to suppress crosstalk and reduce IR drop, the new design of the interconnection lines considering the tradeoff between SI issues is proposed. The newly proposed interconnection design shows 30% improvement in the voltage margin considering the IR drop issues and under 10% enhancement of crosstalk noise. It is expected that the SI analysis and design methodologies could be widely applied in other new memory developments.**

***Index Terms*— 3-D X-Point memory, crosstalk, interconnection, IR drop, new memory, ovonic threshold switch (OTS), phase change memory (PCM), signal integrity (SI).**

Manuscript received March 23, 2020; accepted March 26, 2020. Date of publication March 30, 2020; date of current version May 11, 2020. This work was supported by the International Collaborative R&D Program (funded by the Ministry of Trade, Industry and Energy (MKE), Korea) [N0000899, Glass interposer based RF FEM for Next Generation Mobile Smart Phone], in part by the National Research Foundation of Korea Grant funded by the Korean Government under Grant 2019M3F3A1A03079612, in part by the Research and Development Convergence Program of Ministry of Science, ICT and Future Planning (MSIP), and in part by the National Research Council of Science and Technology (NST) of the Republic of Korea under Grant B551179-12-04-00. Recommended for publication by Associate Editor W. T. Beyene upon evaluation of reviewers' comments. *(Corresponding author: Kyungjune Son.)*

The authors are with the TeraByte Interconnection and Package Laboratory, School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, South Korea (e-mail: kyungjuneson@kaist.ac.kr).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2020.2984268

I. Introduction

RECENTLY, the demands for high bandwidth and high-density memory have increased the demands for the high performance server platforms needed for artificial intelligence (AI) and big data processes. In the memory/storage hierarchy, the memory performance gap between DRAM and NAND flash memory is widening because of the fast growth of semiconductor processing technology [1]. To fill the memory performance gap between DRAM and NAND flash memory, memory cells are now stacked in three dimensions with a large number of data inputs/outputs (I/Os), like high bandwidth memory (HBM). Moreover, the storage-class memory (SCM) was developed using new materials with high performance and nonvolatility. However, the 3-D cross-point (X-Point) memory, which is the three-dimensionally stacked SCM, is the most promising memory solution.

Phase change random access memory (PCRAM) consists of chalcogenide alloy materials with nonvolatility and develops high-performance SCM [2]–[4]. The 3-D X-Point memory stores the data using phase change memory (PCM) and an ovonic threshold switch (OTS) selector with a compact two-stacked cross-point array structure [5]. Fig. 1(a) shows a conceptual view of the 3-D X-Point memory. PCM stores the data "0" and "1" in GeSbTe (GST) material by changing its state. The GST material varies from an amorphous state to a crystalline state with temperature variation [6]–[8]. OTS uses an AsTeGeSiN material that has characteristics similar to those of the PCM. OTS also uses the Ovshinsky's effect, which is a nonlinear switching effect of electrical resistance [9]–[11]. OTS determines the ON/OFF state of the memory cell with the threshold voltage and current. A conceptual view of the memory cells is shown in Fig. 1(b). Using these new materials, the 3-D X-Point memory is nonvolatile, 1000 times faster and endurable than the NAND flash memory, and ten times denser than the DRAM.

As previously mentioned, the 3-D X-Point memory is a high-density and high-performance SCM. Because of the narrow space and long interconnection lines of the 20-nm process technology, crosstalk and IR drop could be severe during memory operation. Therefore, it is important to analyze the SI issues of the 3-D X-Point memory like the SI issues in other memory applications [12]–[17]. The voltage margin is a

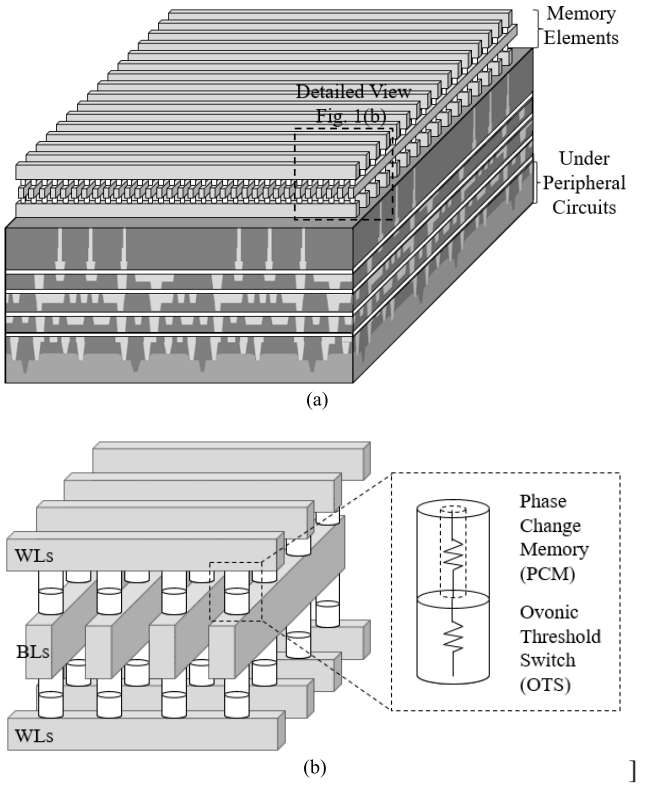


Fig. 1. (a) Conceptual view of 3-D X-Point memory. The memory elements have a cross-array structure and the peripheral circuits for memory operation (read/write) are located under the memory elements. (b) Conceptual view of 4×4 unit memory cell elements of 3-D X-Point memory. The WLs and BLs are intersected and PCM and OTS are located at the cross point of interconnection lines.

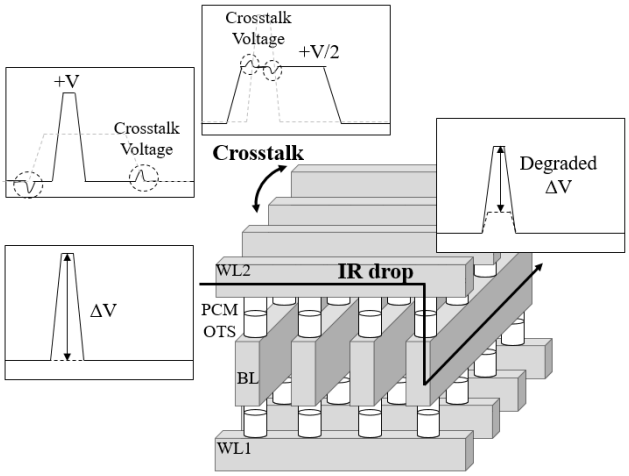


Fig. 2. Signal integrity issues of 3-D X-Point memory are depicted. During read/write operation, crosstalk between interconnection lines leads to voltage coupling and IR drop through interconnection lines leads to degradation of the voltage margin.

very important factor in memory operation. When insufficient voltage is applied to a memory cell, without the proper voltage margin, the memory cells could not read or write data, and this caused an operational error. Crosstalk and IR drop can degrade the voltage margin of a memory cell. The conceptual view of crosstalk and IR drop in the 3-D X-Point memory is shown in Fig. 2. When the voltage is applied to the word lines (WLs) and bit lines (BLs), a few volts are coupled to the adjacent WLs and BLs because of the crosstalk noise. At that moment, the unexpected voltages are applied to the adjacent memory cells, which could turn on the nontarget memory cells. Therefore, the endurance of the irrelevant memory cells could be decreased during operation cycles, which in turn reduces the overall lifetime of the memory cells.

3-D X-Point memory is a single-level cell (SLC) memory. It stores 1 bit in a memory cell that is located at an intersection of WL and BL. For high density, the peripheral circuits for operation, such as decoder, read/write driver, sense amplifiers, and other circuits, are connected to the ends of the WLs and BLs. Because of the parasitic factors of interconnections, best case and worst case operation of the memory cells exists. Some memory cells are close to the peripheral circuits and other memory cells are far from the peripheral circuits. The IR drop through the interconnection lines degrades the voltage margin and the targeted cells cannot be turned on. Therefore, the memory does not write/read the data to the target cell data, which causes an operational error.

There have been several papers on PCM research. In previous PCM studies, various methods for modeling PCM cells were proposed and passive devices such as transistors and diodes were used as selector elements. Moreover, the interconnections of PCM have not been considered for signal integrity (SI) analysis. In [18], a 3-D X-point memory array was proposed, and the capacitive coupling effect was verified in the time-domain simulation. However, passive resistor memory elements were used and selector elements were not included. Moreover, the size of the memory array structure was only 32×32 which is too small for the practical memory size. Therefore, this is an inadvisable approach to the SI analysis of 3-D X-Point memory.

In this article, we, for the first time, designed and analyzed the SI issues of the 3-D X-Point memory including crosstalk and IR drop for high performance. For the SI analysis, we designed a core structure of the 3-D X-Point memory. The unit memory array tile (MAT) size was defined, and the memory elements (PCM, OTS, and interconnection) and peripheral circuits were designed considering practical conditions. Based on the design, the PCM and OTS were behaviorally modeled with nonlinear characteristics, interconnection RC model, and peripheral circuit models. With the proposed model, we simulated and verified that the SI issues crosstalk and IR drop issues degraded the voltage margin, which could lower the memory performance.

We verified the tradeoff relationship between crosstalk and IR drop issues in the interconnection design. Also, a newly designed 3-D X-Point memory with improved SI performance is simulated and analyzed in the time-domain simulation. The newly proposed interconnection design shows 30% improvement in the voltage margin considering the IR drop issues and under 10% enhancement of crosstalk noise with same memory chip size. Moreover, we proposed the methodology to reduce the crosstalk and IR drop issues in the future memory design.

II. Proposed Structure of 3-D X-Point Memory With PCM and OTS

For the new memory design, there are many considerations with accuracy and reasonability [18], [19]. In this section,

we designed the structure of the 3-D X-Point memory including a unit size of MAT, memory elements, interconnections, and peripheral circuits.

A. Proposed Unit MAT Size of 3-D X-Point Memory

For the SI analysis of 3-D X-Point memory, at first, it is important to define the unit MAT size of 128-Gb 3-D X-Point memory. The unit MAT size is determined by the parasitic values of components and the maximum amount of reset current.

At first, we defined the maximum reset current for memory operation. The chalcogenide alloy should be melted for reset operation by the current. We assumed the memory cell structure of the 3-D X-Point memory to the pillar structure. Therefore, the melting area (F^2) is proportional to the reset power (I^2_{reset}). The size of the technology node and reset current are linear, and we can assume the amount of the reset current in 3-D X-Point memory cell which is using 20-nm process technology to be 100 μA [20].

With the I–V curve of OTS, PCM, and PCM+OTS, we can define the resistance of the memory cell [5]. The voltage distribution of PCM is 1.5 times higher than the voltage distribution of OTS. It shows that the resistance of PCM is 1.5 times higher than the resistance of OTS. Therefore, the resistance of PCM and OTS are specified to 10.8 and 7.2 kΩ, respectively.

We assumed the voltage distribution of 3-D X-Point memory during memory operation for each component: V_{dd}, current driver, WL, PCM, OTS, BL, and V_{ss}. In common, the V_{dd} is assumed to be 5 V and we designed the current driver which drives 1.8 V. The voltage drops in PCM and OTS are 1.08 and 0.72 V, respectively, with calculation of reset current and resistance. Therefore, the proper voltage drop in interconnection lines is derived to be 0.72 V. It means the resistance of interconnection lines including WL and BL is 6–8 kΩ. In 3-D X-Point memory, 20-nm process technology is used, so we fixed the width and the space of WL and BL to 20 nm. Considering the cross-point structure, we finally conclude the unit MAT size to 2k $\times$ 2k.

3-D X-Point memory using 20-nm processing technology consists of a 16-bank system, which is shown in Fig. 3(a). Each bank consists of 1024 MATs and 1 MAT stores 8 Mb (2k $\times$ 2k $\times$ 2) of data. Detailed views of the unit bank and unit MAT are shown in Fig. 3(b).

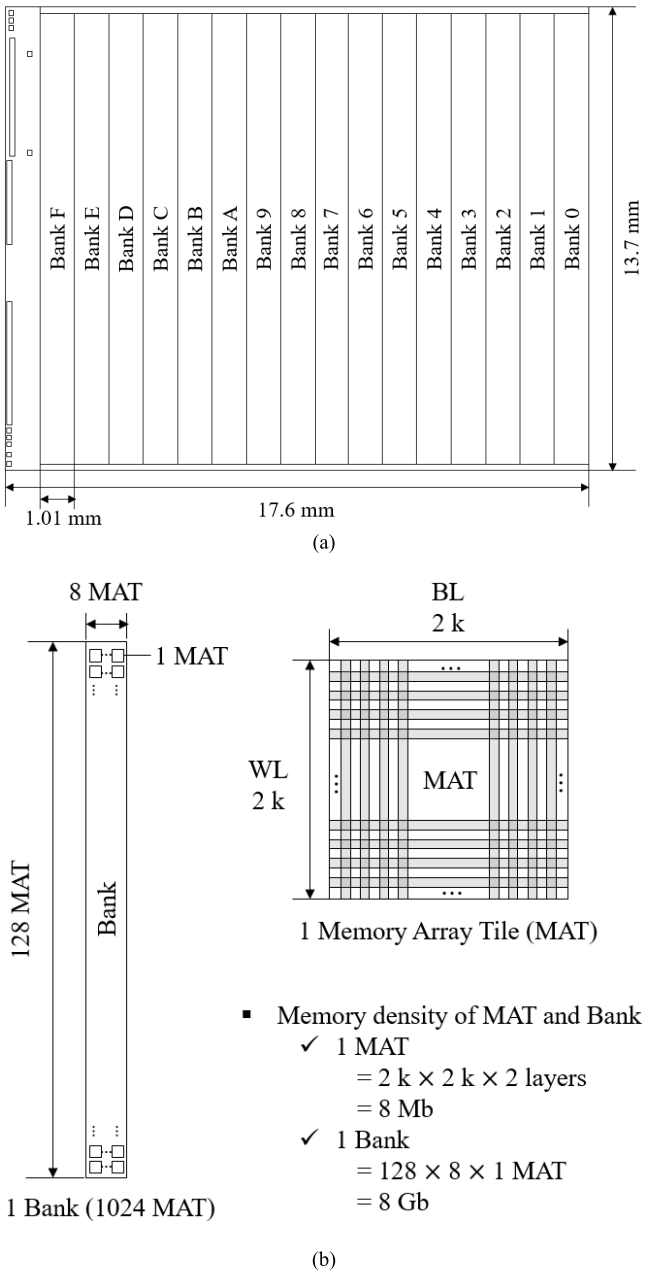


Fig. 3. (a) Conceptual view of overall size of 3-D X-Point memory: 128-Gb 3-D X-Point memory in 16 bank system. (b) 2k of WLs and BLs with two stacks shows 8-Mb MATs and 1024 MATs leads to 1 bank with 8 Gb.

B. Components of 3-D X-Point Memory Structure

As mentioned above, the 3-D X-Point memory uses a PCM cell and an OTS selector as the memory elements. The chalcogenide materials, which alloys with chalcogenide anions and electropositive elements, are used in the PCM cells. The chalcogenide alloy exhibits reversible transition between the disordered (amorphous) and ordered (crystalline) atomic structures, which are determined by temperature variation. In a 3-D X-Point memory cell, the $Ge_2Sb_2Te_5$(GST) material is used. The structure of the PCM cells for 3-D X-Point memory is shown in Fig. 4. With a pillar-structure PCM, the insulator confines the thermal effect, unlike the mushroom-type structure, and reduces the amount of write current.

The key operations of PCM are write (reset), write (set), and read. The reset operation in PCM is write the data "1" to "0". A high voltage pulse is applied to the memory cell and the heater heats the GST material to the melting point. After the GST material is melted, the memory discharges the applied voltage rapidly and the GST material cools rapidly within 15 ns. Then, the GST material changes to an amorphous state which is disordered and has high electrical resistance, with a value is more than 1 MΩ. The set operation in PCM is write the data "0" to "1". A low voltage is applied to the memory cell relatively longer, about 80 ns, and the heater

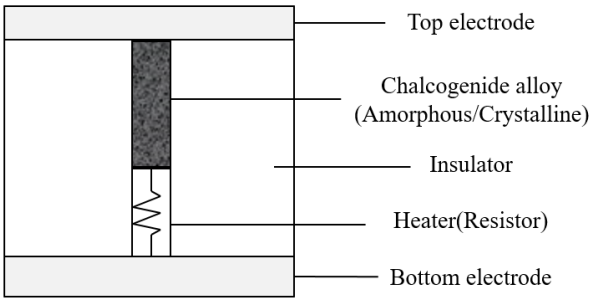


Fig. 4. Conceptual view of a pillar-type PCM cell. The voltage is applied to each top and bottom electrodes and the heater converts the electrical energy to thermal energy. Then, the physical state of the chalcogenide alloy is determined by the amount of thermal energy.

heats the GST material to the crystallization point. After the GST material is fully crystallized, the memory discharges the voltage and the GST material cools slowly. Then, the GST material changes to its crystalline state which is ordered and it has low electrical resistance, with a value less than 10 kΩ. The read operation in PCM is read the data "0" or "1". The low voltage pulse is applied to the memory cell and it senses the amount of current flow through the memory cells. When the memory cell material is amorphous, the amount of current through the memory cell is only several nA scales, and the data are read as "0". Otherwise, when the memory cell material is crystalline, the amount of current through the memory cell is hundreds of μA scales, and the data are read as "1".

Like the role of transistors in DRAM, selector elements are needed for PCM to achieve high performance. In the past several years, the most critical problem of PCM chips has been the sneak current issue [22], [23]. Unlike conventional memory, such as DRAM and NAND flash memory, the PCM stores the data along with the resistance status. During the read/write operation in PCM, a small amount of current can be leaked through the interconnection and adjacent memory cells because the memory elements have resistor characteristics. With high-density PCM, it leads to the existence of many leakage current paths. Therefore, the sneak current issue is more critical, so the selector elements should be utilized with PCM.

OTS is a promising solution for dealing with the sneak current issue in PCM [11], [22]. An OTS is made of AsTeGeSiN, which is easy to alloy with chalcogenide materials. OTS uses Ovshinsky's effect, which is a nonlinear effect of electrical resistance that occurs in thin film amorphous glass mixed with other materials (e.g., As, Ge). The I–V characteristic of OTS is nonlinear. Moreover, OTS increases the threshold voltage of the integrated PCM, by which it guarantees the memory cells sufficient voltage margins.

The WLs and BLs, which are tungsten, are stacked in two layers in a cross-array structure. With the 20-nm processing technology, the resistivity of the thin tungsten is about three to four times higher than the resistivity of the typical tungsten [24]. In the case of 3-D X-Point memory, 20-nm processing technology is used to manufacture the interconnections. Therefore, the width of the WLs and BLs (described as w_{WL} and w_{BL}) and the space between the interconnections (described as d) are 20 nm. The thickness of the WLs (described as t_{WL}) is 40 nm and the BLs (described as t_{BL}) is 105 nm. The vertical distance between the WLs and BLs (described as h) is 90 nm. The physical dimension parameters of interconnections are shown in Fig. 5 and the values are summarized in the Table I.

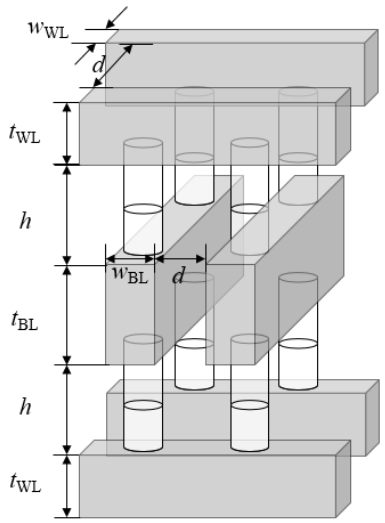


Fig. 5. Detailed physical dimension of 3-D X-Point memory interconnections. The width and space of the WLs and BLs are designed to 20 nm using fine processing technology.

TABLE I
PHYSICAL DIMENSIONS OF 3-D X-POINT MEMORY INTERCONNECTIONS

Parameter	Symbol	Value
Width of WL and BL	w_{WL}, w_{BL}	20 nm
Space of WLs and BLs	d	20 nm
Thickness of WL	t_{WL}	40 nm
Thickness of BL	t_{BL}	105 nm
Height between WL and BL	h	90 nm

Fig. 6 shows the overall circuit view for core operation in the 3-D X-Point memory. For a read/write operation, the core peripheral circuits must be designed to include WLs, BLs decoders, read/write drivers, sense amplifiers, and analog-to-digital converters [25], [26]. The whole peripheral circuits are located under the memory elements layer.

III. ELECTRICAL MODELS OF 3-D X-POINT MEMORY CELLS AND INTERCONNECTIONS

For SI analysis of the proposed 3-D X-Point memory, the memory components were modeled to the behavior of SPICE models, and interconnection lines were modeled to equivalent RC models and simulated to circuit system. The PCM and OTS selector are behaviorally modeled to Verilog-A modules in HSPICE. The interconnections of the 3-D X-Point memory are modeled with resistance and capacitance using 3-D electromagnetic simulation tools. Under-peripheral circuit

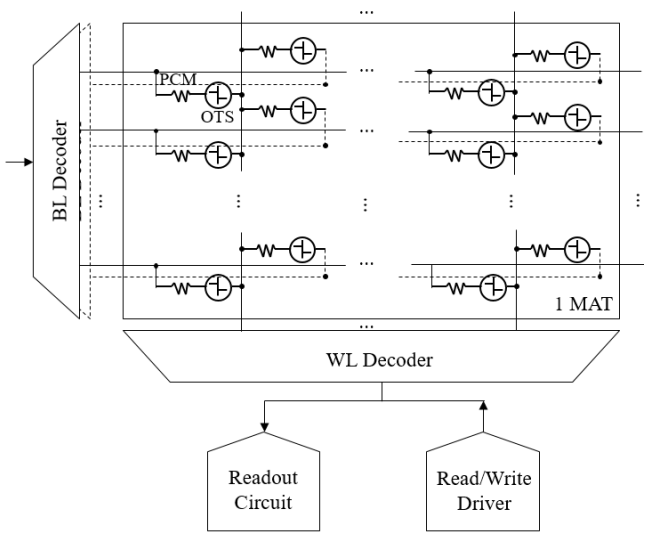


Fig. 6. Block diagram of peripheral circuits for core operation in 1 MAT sized 3-D X-Point memory. Each WL and BL is designated by decoders and read/write driver to apply the voltage to each line. Current sense amplifier and analog-to-digital converter are included in the readout circuits.

models are designed and performed to the SPICE model using the CMOS transistor.

A. Electrical Behavior Model of 3-D X-Point Memory Cells

The PCM cells were modeled to the electrical behavior model using Verilog-A modules [27], [28]. Fig. 7(a) shows the core Verilog-A modules of the PCM cells.

The heat generation module uses the energy conservation principle. When the voltage is applied to the memory cell module, it converts the voltage to temperature by calculating the following equation:

$$\int \left(I^2 R_{\text{write}} - \frac{\Delta T}{R_T} \right) dt = C_T \Delta T. \tag{1}$$

The phase change control module determines the read, write (set), and write (reset) operations. When the amount of temperature from the heat generation module is lower than the crystallization point, the module determines the read operation. When the heat generation module raises the temperature higher than the crystallization point and lower than the melting point, the module determines to the set operation. When the heat generation module raises the temperature above the melting point, the module determines to the reset operation.

With the determined operation, next module calculates the radius of the amorphous region. In the set operation, the GST material crystallizes perfectly, in which case, the radius of the amorphous region has the value 0. However, in the reset operation, the radius of the amorphous region can vary the resistance.

The resistance calculation module calculates the resistance based on the amount of the amorphous region. In this model, as shown in Fig. 7(b), the low resistance with a crystalline state is 6 kΩ and the high resistance with an amorphous state is 1.5 MΩ.

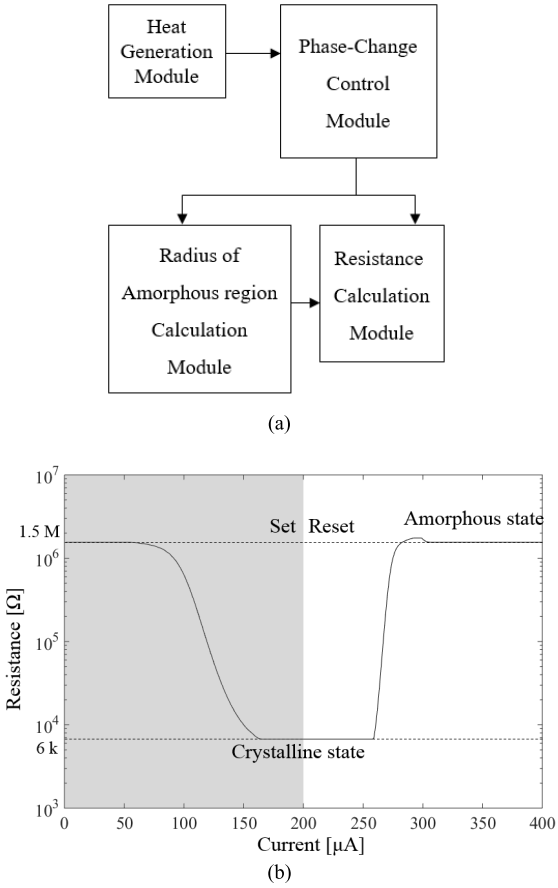


Fig. 7. (a) Block diagram of proposed PCM cell model with Verilog-A modules. The applied voltage is converted to heat, then, the amount of amorphous region is calculated and resistance obtained. (b) *R–I* curve of PCM cell behavior model.

Similarly, the OTS selector was also modeled to the electrical behavior model using Verilog-A modules. Fig. 8(a) shows the electrical behavior and core Verilog-A modules of the OTS selector.

OTS is controlled ON and OFF by its own threshold voltage and threshold current with nonlinearity. Below the threshold point, the module acts as high resistance and OFF state. Above the threshold point, the module acts as low resistance and ON state. As shown in Fig. 8(b), the OTS cell model shows nonlinear characteristics in the dynamic region.

B. Electrical RC Model of 3D X-Point Memory Interconnections

The RC value of the interconnections for unit-sized 3-D X-Point memory is extracted from 3-D electromagnetic simulation tools. RC values are extracted from interconnections of the unit MAT size and divided into the unit memory cell size. Fig. 9 shows the unit parasitic R and C for the interconnections of 3-D X-Point memory. The resistance of unit WLs and BLs (described as $R_{\text{WL\_Unit}}$ and $R_{\text{BL\_Unit}}$) is 10 and 3.81 Ω, respectively. The capacitance of unit WLs and BLs (described as $C_{\text{WL\_Unit}}$ and $C_{\text{BL\_Unit}}$) is 2.7 and 7.2 aF, respectively. The capacitance between BLs is greater than the capacitance between WLs because of their greater thickness.

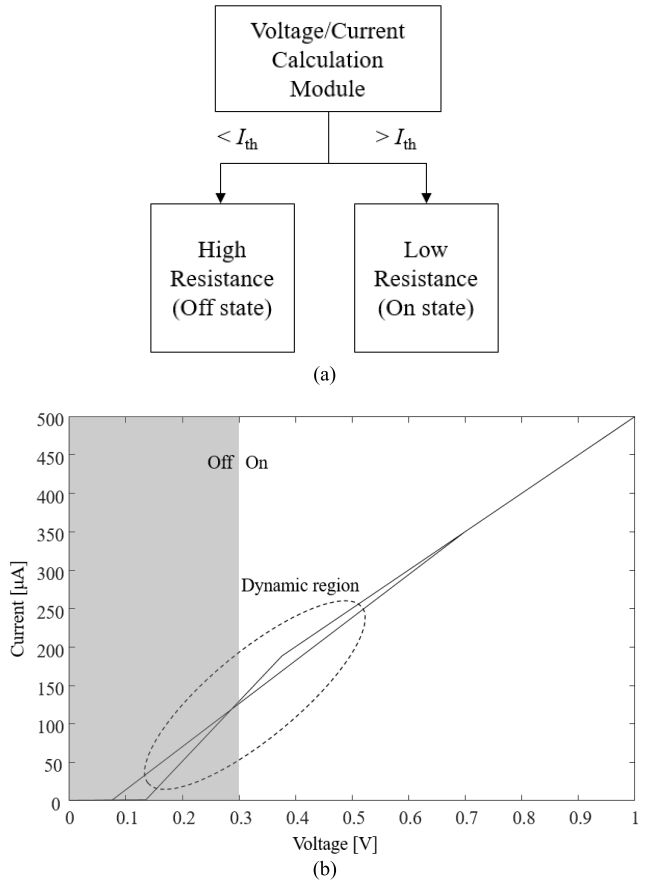


Fig. 8. (a) Block diagram of proposed OTS selector model with Verilog-A modules. The module determined the amount of resistance by referring the applied voltage and amount of the current flow to threshold values. (b) I–V curve of OTS selector behavior model.

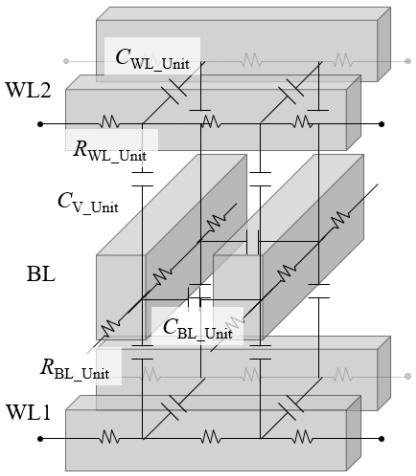


Fig. 9. A unit block consisting of R and parasitic C for the interconnections of 3-D X-Point memory. The values of R and parasitic C were obtained using 3-D EM simulation tools.

We considered the adjacent capacitance only, because the capacitance except the adjacent capacitance is so small that the amount of degradation is below 10% considering crosstalk and IR drop. The capacitance between the vertical interconnection lines (described as C_{V_Unit}) is 1.2 aF. The parasitic component values of the 3-D X-Point memory interconnections are summarized in Table II.

TABLE II
PARASITIC COMPONENT VALUES OF 3-D X-POINT MEMORY INTERCONNECTIONS

Parameter	Symbol	Value (per 20 nm)
Unit resistance of WL	R_{WL_Unit}	10 Ω
Unit resistance of BL	R_{BL_Unit}	3.8 Ω
Unit capacitance of WL	C_{WL_Unit}	2.1 aF
Unit capacitance of BL	C_{BL_Unit}	7.2 aF
Unit vertical capacitance between WL and BL	C_{V_Unit}	1.2 aF

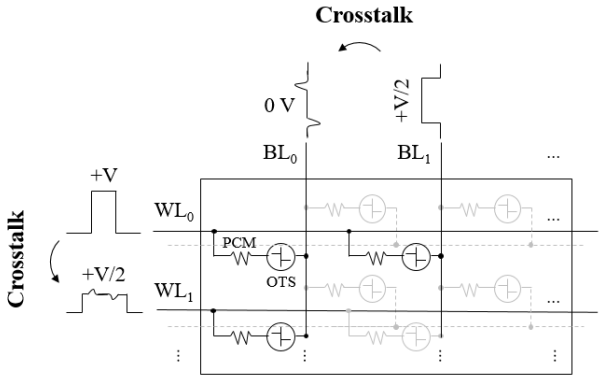


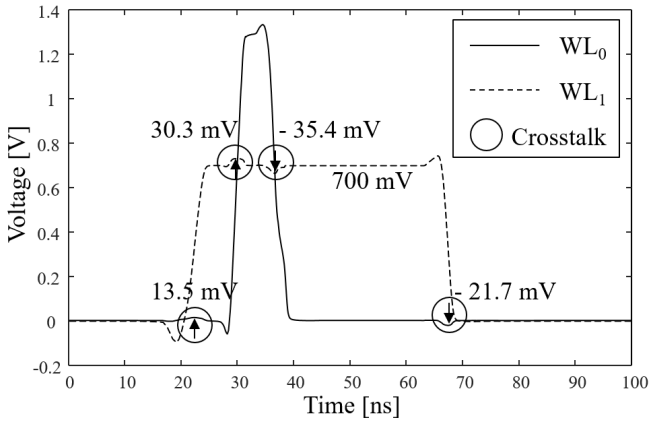
Fig. 10. Schematics of crosstalk in unit MAT sized 3-D X-Point memory. When the voltage is applied to the targeted WL and BL, a small amount of voltage is coupled by the crosstalk and degrades the voltage margin between memory cells. With the degraded voltage margin, the adjacent memory cells can be turned ON and affect the memory endurance.

IV. SI ANALYSIS OF 3-D X-POINT MEMORY CONSIDERING CROSSTALK AND IR DROP

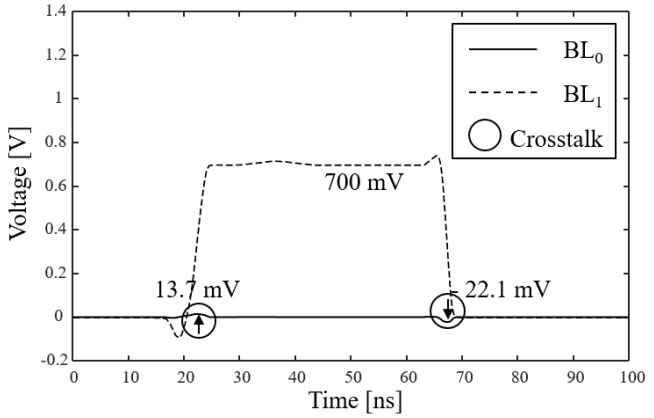
During the read/write operation in the 3-D X-Point memory, half-voltage is applied to the WLs and BLs, except on the selected lines to minimize the operating power consumption. Along the selected lines, about half-selected memory cells exist, and the selector controls the ON/OFF status of the cells. For the selected memory cell, the proper voltage margin is needed; and for the half-selected memory cell, a half-voltage margin is needed. In this article, the simulations were focused on the reset operation because the reset pulse, which involves high voltage and short time, leads to more SI issues than the other operations.

A. Analysis of Crosstalk Between the Interconnection Lines of 3-D X-Point Memory

Analysis of crosstalk can be conducted and verified from the transient simulations. The schematic of the crosstalk simulation is shown in Fig. 10. The half-voltage is applied to all WLs and BLs, except the interconnection line of the targeted memory cell. Then, the reset voltage is applied to the targeted memory cell's interconnection line. The time-domain simulation results of crosstalk are shown in Fig. 11. At the targeted WL, 13.5 and −21.7 mV are coupled from the adjacent WL, to which the half-voltage is applied. In addition,



(a)



(b)

Fig. 11. Time-domain simulation results of crosstalk noise in each WL and BL. (a) At a WL, crosstalk appears at the rising and falling edge of each pulse. (b) At a BL, crosstalk appears at ground voltage. Crosstalk does not substantially affect the voltage margin in this design.

at the neighboring WL, 30.3 and −35.4 mV are coupled from the targeted WL, which is shown in Fig. 11(a). Likewise, at the targeted BL, 13.7 and −22.1 mV are coupled from the neighboring BL by crosstalk, which is shown in Fig. 11(b). As shown in the simulation results, crosstalk appears at the edge of the voltage pulse. With the rising edge, the coupled voltage increases in adjacent lines; and with the falling edge, the coupled voltage decreases and vice versa. Crosstalk is predominantly affected by the capacitance between the interconnection lines. Although we applied the half-voltage to the adjacent interconnection lines to minimize the power consumption and to act as a reference line, the rising and falling edges of the voltages pulse that have a high frequency factor causes the voltage-coupling noise. The crosstalk noise in this interconnection design is not substantial; however, with even finer-scale processing technology, the space between the interconnection lines could be decreased. Moreover, with higher density, the total length of interconnection lines could be increased. Therefore, the capacitance between the interconnection lines will increase and the crosstalk noise will increase. In this case, the adjacent memory cells could be turned on and could cause operational errors and decrease the memory endurance.

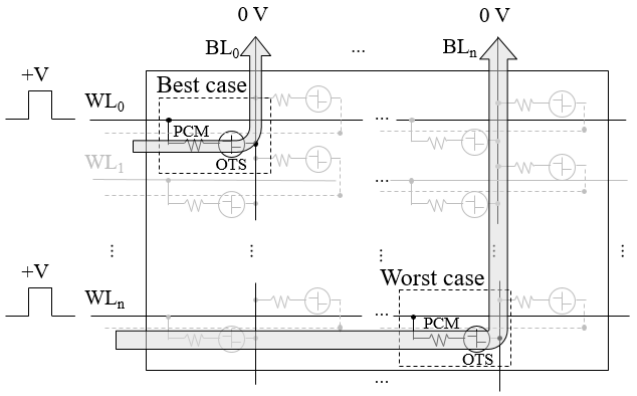


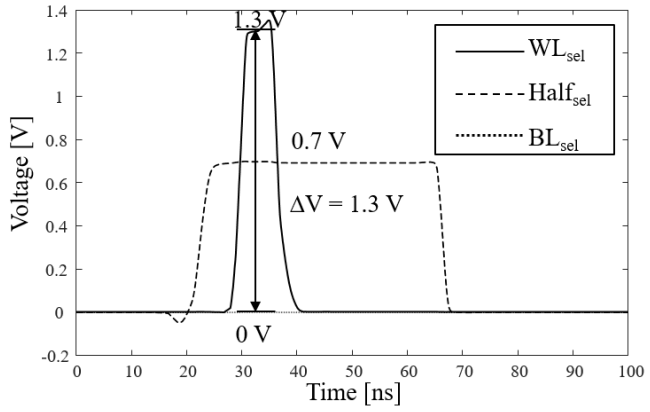
Fig. 12. Schematics of IR drop in unit MAT sized 3-D X-Point memory. With the high-density characteristics, the best case of memory cell, which is close to the peripheral circuits and the worst case of memory cell, which is far from the peripheral circuits are existed. In the worst case, IR drop degrades the voltage margin of the memory cell. Because of the degraded voltage margin, the targeted memory cells cannot be turned ON and cause operational error.

B. Analysis of IR Drop through Interconnection Lines in Best and Worst Cases

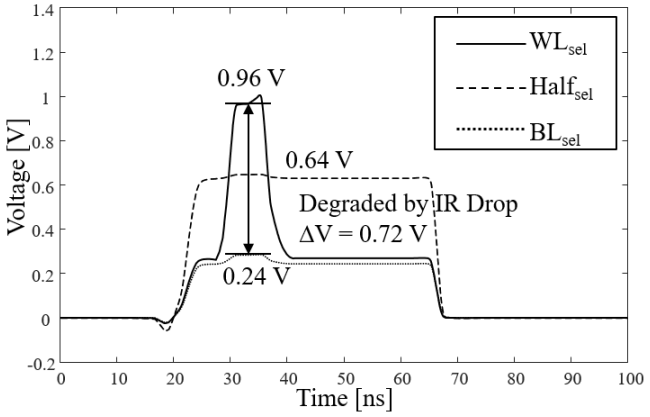
In the high-density memory with long interconnection lines, IR drop is inevitable. The core peripheral circuits used for memory operation can be located in limited positions. Therefore, the distance between the peripheral circuits and memory cells is different. Fig. 12 shows the best case of a memory cell, which is closest to the peripheral circuits, and the worst case of a memory cell, which is the farthest from the peripheral circuits. During the reset operation, the proper voltage margin of a memory cell should be applied. The time-domain simulation results of the IR drop are shown in Fig. 13. The voltage margin of the best case of the memory cell is 1.3 V, which is shown in Fig. 13(a). However, in the worst case, the voltage margin of the memory cell is decreased to 0.72 V, which is shown in Fig. 13(b). The IR drop is predominantly affected by the resistance through the interconnection lines. The IR drop in this interconnection design is dominant at the worst case of a memory cell. In addition, with finer-scale processing technology and high-density memory development, the total length of the interconnection line could increase. Therefore, the resistance through interconnection lines could increase and the IR drop be more severe with a degrading voltage margin. With a degraded voltage margin, the worst case memory cell could not operate and would cause data error.

C. Analysis of Revised Design for High Performance Considering Crosstalk and IR Drop

For high performance considering crosstalk and IR drop, a revised design for the 3-D X-Point memory was needed. The revised design rule was to maintain the same structure and area. Fig. 14 shows the percentage of the degraded voltage margin with the ratio of the interconnection space to width and thickness by crosstalk and IR drop. When the ratio increases, crosstalk noise is enhanced slightly, but the IR drop is suppressed. These SI issues are caused by the tradeoff



(a)



(b)

Fig. 13. Time-domain simulation results of IR drop in each WLs and BLs. (a) In the best case, an IR drop does not appear and the proper voltage margin is maintained. (b) In the worst case, the IR drop affects both WL and BL, and degrades the voltage margin. The IR drop predominantly affects the voltage margin.

relationship, and the tradeoff point is a ratio of about 10. However, 10 is not a reasonable value for fabricating the memory. By using 10-nm processing technology, it would be hard to fabricate this memory, with the same chip area. The width and space of the WLs and BLs would be revised from 20/20 nm to 30/10 nm, respectively, and the ratio of the interconnection space to width would be changed from 1 to 3, respectively. With this revision, the capacitance between interconnections would slightly increase, and the resistance through the interconnections would significantly decrease. Considering the processing technology limitation, the thickness of the interconnections should be increased for high performance considering crosstalk and IR drop. With increased thickness, performance would be improved. However, it is impossible to increase the thickness of interconnections continuously considering the aspect ratio of the 3-D X-Point memory. Therefore, the interconnection design including both WLs and BLs are revised to double thickness considering the aspect ratio reasonably, and the ratio was changed from 3 to 6.

With the revised design, the time-domain simulation results of crosstalk are shown in Fig. 15. At the targeted WL, 13.6 and −21.9 mV are coupled from the adjacent WL, to which half-voltage was applied. In addition, at a neighboring WL,

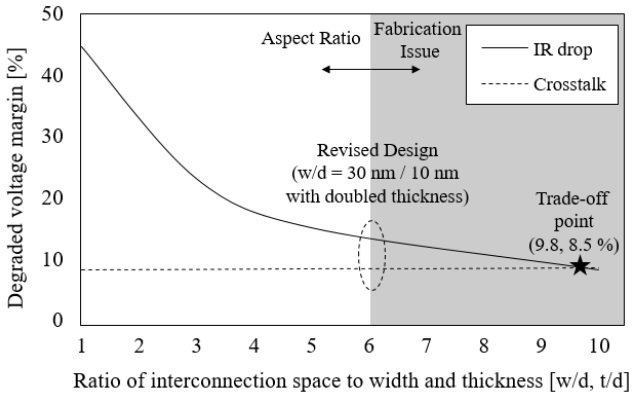


Fig. 14. Percentage of degraded voltage margin with ratio of the interconnections by crosstalk and IR drop. With the higher ratio of interconnections, IR drop can be decreased and crosstalk noise are almost same. Considering the aspect ratio of interconnection lines, the interconnection is revised to ratio 6 (w/s = 30/10 nm with doubled thickness).

33.5 and −36.4 mV are coupled from the targeted WL, which is shown in Fig. 15(a). Likewise, at the targeted BL, 14.3 and −22.6 mV are coupled from the neighboring BL by crosstalk, which is shown in Fig. 15(b). As mentioned above, with the decreased space between the interconnection lines the capacitance increased, so the crosstalk would be slightly enhanced below 10% of the voltage margin. However, with the IR drop, the revised design improved the voltage margin from 0.72 to 1.21 V as shown in Fig. 16. The voltage margin was improved by more than 30% of the design revision. From the above results, the revised design shows better SI performance considering crosstalk and IR drop.

V. Discussion

We analyzed crosstalk and IR drop of the 3-D X-Point memory including the PCM cells, OTS selector, interconnection lines, and peripheral circuits for core operation. The key feature of the SI analysis of the 3-D X-Point memory is that we can apply this approach diversely. We can expand this research using finer process technology or other types of memory using behavioral models of memory components and can suggest the interconnection design for better SI performance of the memory. In this article, we assumed 20-nm process technology and a two-layer stack for memory elements in 3-D X-Point memory. With the latest technology, the interconnection line and memory elements can be integrated below 10 nm and four- and eight-layer stacks. Therefore, the SI issues would be more critical in memory operation and the SI analysis would also be more important.

3-D X-Point memory is an SLC memory because it takes a long time for chalcogenide material transition. For low latency, the materials of PCM and OTS selector can be replaced by new chalcogenide materials which show fast transition between amorphous and crystalline states with low power. We can easily analyze the SI with newly behavior model and it is helpful to develop multi-level cell (MLC) 3-D X-Point memory.

3-D X-Point memory uses PCM which shows different characteristics by heat. We only considered the heat to the

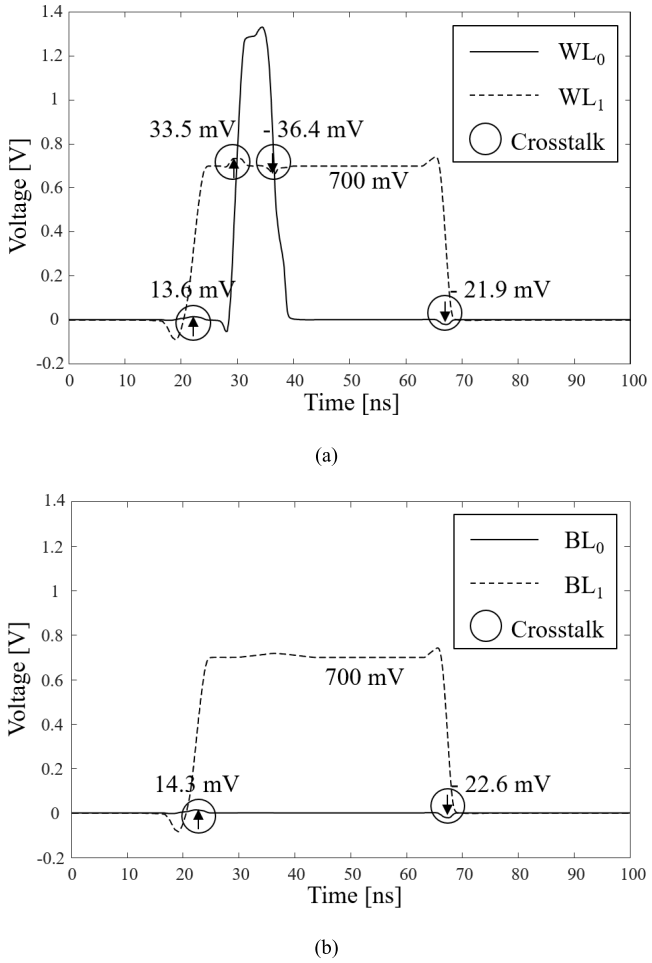


Fig. 15. Time-domain simulation results of crosstalk noise in each WLs and BLs with revised design. (a) At the WL, crosstalk are appeared at the rising and falling edge of each pulses. (b) At the BL, crosstalk is appeared at ground voltage. Crosstalk is more severe in the revised design. However, it does not affect the voltage margin dominantly.

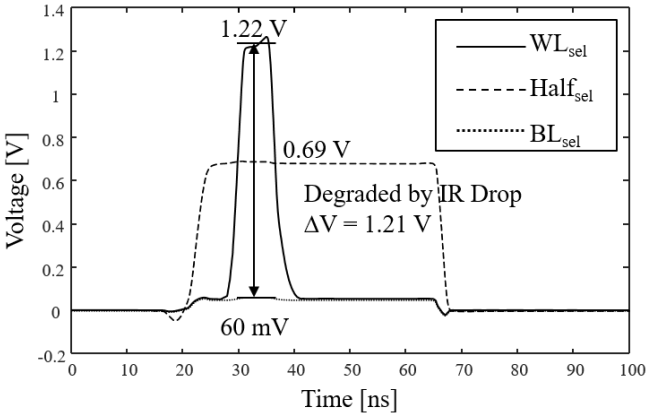


Fig. 16. Time-domain simulation results of IR drop in each WL and BL for the revised design. In the worst case, the IR drop decreases and the voltage margin increases. With the revised design, the IR drop is improved.

PCM; however, the electrical characteristics of the interconnection lines can be affected by the heat. Fors future work, the thermal and SI cosimulation of 3-D X-Point memory should be conducted for accuracy and these methodologies of design and analysis of 3-D X-Point memory can be applicable.

The unit MAT size is determined by voltage distribution of memory components as mentioned in Section II. For the peripheral circuit design, we assumed the decoder, read/write driver, current sense amplifier, and ADC are located under the memory elements layer. However, we were unconcerned about the layout area of the peripheral circuits because we focused on the SI issues of the 3-D X-Point memory by interconnection line design. For more practical consideration, the layout area of the peripheral circuits also is critical factor in unit MAT assumption. For sufficient voltage distribution to each memory component, the limited layout area can act a constraint in the memory design. Therefore, the memory designers should be placed under the peripheral circuits through several layers because the area of the unit MAT size is quite small. As 3-D X-Point memory is SLC, sharing the peripheral circuits between neighbored banks can be a good solution to reduce the layout area.

For the optimal power consumption, 3-D X-Point memory uses the half-voltage scheme to apply the half-voltage to the adjacent interconnection lines of the targeted memory cell. However, in practical condition, the half-voltage cannot be applied uniformly because of its resistive characteristics of the interconnection lines. To operate with less loss of power, the read/write driver should apply the additional voltage to compensate the IR drop according to the position of the targeted memory cell.

In this article, we proposed a new memory interconnection design considering the tradeoff relationship between crosstalk and IR drop in the same memory elements area. For the improvement of SI performance in the 3-D X-Point memory, to suppress crosstalk and IR drop, the interconnection design factors were various and we discuss the methodologies to reduce these SI issues.

A. Crosstalk Reduction Method

With the simulation results, about 10% of voltage margin is degraded by the crosstalk in the original and proposed design, and it is not a critical issue but rather a IR drop issue. However, with a finer process technology, the density of memory will be increased and the space between the interconnection lines would be closer and the parasitic capacitance of the interconnection line will be increased. Therefore, with less than 10-nm technology, the crosstalk noise can degrade the voltage margin by 20% and in turn lower the memory performance.

We figured out that the crosstalk noise is predominantly affected by the capacitance between interconnection lines. The space between the interconnection lines should be increased; however, the length of the interconnection lines should be decreased. Due to the cross-point structure, the length is proportional to the sums of space and width. Therefore, for high density, the space and width have a tradeoff relationship and are designed to be the same size. With the same chip height, it is better to increase the amount of the memory stack with smaller thickness. In addition, using low-k dielectric material, the capacitance between interconnection lines could be decreased. With the physical dimension revision of interconnection line considering crosstalk reduction results to IR

drop enhancement, it is important to figure out the portion of voltage margin degradation. For example, with original 3-D X-Point memory, the crosstalk issue is less effective than the IR drop issue; we should design the memory interconnection lines to suppress IR drop issues rather than crosstalk issue, like reducing resistance characteristics or even increasing parasitic capacitance characteristics.

To minimize the crosstalk in 3-D X-Point memory, a nonsimultaneous operating scheme which applies voltage to the memory cell at different timings is used. Without timing difference, the crosstalk noise can be enhanced, and this causes an operational error by coupled voltage.

B. IR Drop Reduction Method

In the original design of the 3-D X-Point memory, the voltage margin in worst case is degraded by 46% in the IR drop, and this is critical in memory operation. The IR drop is predominantly affected by the resistance of the interconnection lines. Without the design limitation, three main interconnection factors could lower the IR drop. First, the width of the interconnection lines should be increased, and second, the thickness of the interconnection lines should be increased. These factors are proportional to the area of the interconnection lines and these changes would reduce the resistance of lines. Third, the length of the interconnection lines should be decreased. As mentioned above, the length is proportional to the sums of space and width and they have a tradeoff relationship. From the point of view of IR drop reduction, it is better to increase the thickness of the interconnection lines. However, for the change in thickness, we should carefully consider the aspect ratio for metal material and possibility of fabrication. The interconnection line can be collapsed with unbalanced proportion of width and thickness.

In addition, using a low resistivity material rather than tungsten, such as copper, etc., the resistance parameter of interconnection lines could be decreased. However, copper has higher thermal conductivity and diffusivity than tungsten. Therefore, with high temperature, copper can easily affect and diffuse to other components such as PCM, OTS, and so on. With thermal issue, tungsten is used for PCM rather than copper even though it has lower resistivity. The compound of copper and tungsten with proper ratio would be better material for interconnection lines in thermal and SI viewpoint.

VI. Conclusion

3-D X-Point memory is a promising SCM with high density and high performance. It is important to design and analyze the core memory operation system including the memory elements, interconnections, and circuits considering SI issues. Based on the 20-nm processing technology used for the memory, we proposed a unit MAT size of the 3-D X-Point memory for core operation. In addition, memory elements including a PCM cell and OTS selector were behaviorally modeled, and interconnection lines were modeled for R and parasitic C with a 3-D EM solver. The circuit simulation of this system was conducted and the crosstalk and IR drop issues were verified. Moreover, we verified the tradeoff relationship between crosstalk and IR drop issues with the interconnection design parameters. We proposed and simulated a revised interconnection design of the 3-D X-Point memory for high performance considering SI issues. The time-domain simulation results for the revised interconnection design of 3-D X-Point memory show the effective improvement. Therefore, in this article, we successfully designed and analyzed the SI issues in the 3-D X-Point memory and proposed the revised design for higher SI performance. We also proposed the methodology to reduce the crosstalk and IR drop issues in the future memory design.

Acknowledgment

The authors would like to acknowledge the technical support from ANSYS (ANSYS Q3D Extractor).

References

[1] J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*. San Mateo, CA, USA: Morgan Kaufmann, 2012.
[2] K. Kim and G. H. Koh, "Future memory technology including emerging new memories," in *Proc. 24th Int. Conf. Microelectron.*, Niš, Serbia, vol. 1, May 2004, pp. 377–384.
[3] S. W. Fong, C. M. Neumann, and H.-S.-P. Wong, "Phase-change memory—Towards a storage-class memory," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4374–4385, Nov. 2017.
[4] W. Reohr *et al.*, "Memories of tomorrow," *IEEE Circuits Devices Mag.*, vol. 18, no. 5, pp. 17–27, Sep. 2002.
[5] D. C. Kau *et al.*, "A stackable cross point phase change memory," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4.
[6] H.-S. P. Wong *et al.*, "Phase change memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, Dec. 2010.
[7] G. Burr *et al.*, "Phase change memory technology," *J. Vac. Sci. Technol. B*, vol. 28, no. 2, pp. 223–262, Jan. 2010.
[8] D. Ventrice, P. Fantini, A. Redaelli, A. Pirovano, A. Benvenuti, and F. Pellizzer, "A phase change memory compact model for multilevel applications," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 973–975, Nov. 2007.
[9] S. R. Ovshinsky, "Reversible electrical switching phenomena in disordered structures," *Phys. Rev. Lett.*, vol. 21, pp. 1450–1453, Nov. 1968.
[10] W. Czubatyj and S. J. Hudgens, "Invited paper: Thin-film ovonic threshold switch: Its operation and application in modern integrated circuits," *Electron. Mater. Lett.*, vol. 8, no. 2, pp. 157–167, Apr. 2012.
[11] G. W. Burr *et al.*, "Access devices for 3D crosspoint memory," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron., Mater., Process., Meas., Phenomena*, vol. 32, no. 4, Jul. 2014, Art. no. 040802.
[12] K. Son, K. Cho, S. Kim, G. Park, K. Song, and J. Kim, "Modeling and signal integrity analysis of 3D XPoint memory cells and interconnections with memory size variations during read operation," in *Proc. IEEE Symp. Electromagn. Compat., Signal Integrity Power Integrity (EMC, SI PI)*, Long Beach, CA, USA, Jul. 2018, pp. 223–227.
[13] H.-H. Chuang *et al.*, "Signal/power integrity modeling of high-speed memory modules using chip-package-board coanalysis," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 381–391, May 2010.
[14] C.-K. Chen, W.-D. Guo, C.-H. Yu, and R.-B. Wu, "Signal integrity analysis of DDR3 high-speed memory module," in *Proc. Electr. Design Adv. Packag. Syst. Symp.*, Seoul, South Korea, Dec. 2008, pp. 101–104.
[15] K. Cho *et al.*, "Signal integrity design and analysis of differential high-speed serial links in silicon interposer with through-silicon via," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 1, pp. 107–121, Jan. 2019.
[16] G. Zhu *et al.*, "Study on high-density integration resistive random access memory array from multiphysics perspective by parallel computing," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1747–1753, Apr. 2019.
[17] S. Li *et al.*, "Fully coupled multiphysics simulation of crosstalk effect in bipolar resistive random access memory," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3647–3653, Sep. 2017.
[18] D. M. Mathew *et al.*, "RRAMSpec: A design space exploration framework for high density resistive RAM," in *Proc. Embedded Comput. Syst., Archit., Model., Simul.*, 2019, pp. 34–47.

[19] A. Levisse, P. Royer, B. Giraud, J. P. Noel, M. Moreau, and J. M. Portal, "Architecture, design and technology guidelines for crosspoint memories," in *Proc. IEEE/ACM Int. Symp. Nanosc. Archit. (NANOARCH)*, Newport, RI, USA, Jul. 2017, pp. 55–60.
[20] E. Ou and S. S. Wong, "Array architecture for a nonvolatile 3-dimensional cross-point resistance-change memory," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2158–2170, Sep. 2011.
[21] Y. Fujisaki, "Review of emerging new solid-state non-volatile memories," *Jpn. J. Appl. Phys.*, vol. 52, no. 4R, Apr. 2013, Art. no. 040001.
[22] S. Kannan, J. Rajendran, R. Karri, and O. Sinanoglu, "Sneak-path testing of crossbar-based nonvolatile random access memories," *IEEE Trans. Nanotechnol.*, vol. 12, no. 3, pp. 413–426, May 2013.
[23] M. A. Zidan *et al.*, "Memristor-based memory: The sneak paths problem and solutions," *Microelectron. J.*, vol. 44, no. 2, pp. 176–183, 2013.
[24] W. Steinhögl *et al.*, "Tungsten interconnects in the nano-scale regime," *Microelectron. Eng.*, vol. 82, nos. 3–4, pp. 266–272, Dec. 2005.
[25] J.-W. Kwon *et al.*, "A low-power TDC-configured logarithmic resistance sensor for MLC PCM readout," *IEEE Sensors J.*, vol. 16, no. 14, pp. 5524–5535, Jul. 2016.
[26] D. Jin *et al.*, "A 15 μm-pitch, 8.7-ENOB, 13-Mcells/sec logarithmic readout circuit for multi-level cell phase change memory," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2431–2440, Oct. 2015.
[27] Z. Xu, K. B. Sutaria, C. Yang, C. Chakrabarti, and Y. Cao, "Hierarchical modeling of phase change memory for reliable design," in *Proc. IEEE 30th Int. Conf. Comput. Design (ICCD)*, Sep. 2012, pp. 115–120.
[28] K. C. Kwong, L. Li, J. He, and M. Chan, "Verilog—A model for phase change memory simulation," in *Proc. 9th Int. Conf. Solid-State Integr.-Circuit Technol.*, Oct. 2008, pp. 492–495.

Kyungjune Son (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2016 and 2018, respectively, where he is currently pursuing the Ph.D. degree.

His current research interest includes the design and analysis of 3-D X-point memory for high-performance server platform considering signal integrity.

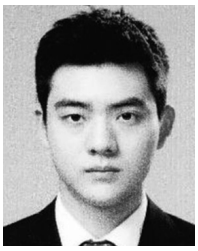
Kyungjun Cho received the B.S. degree in electronic engineering from Ajou University, Suwon, South Korea, in 2014, and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2016, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interest includes the design and analysis of silicon interposer for high-bandwidth memory considering signal integrity and power integrity.

Subin Kim received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree.

His current research interests include on-interposer active PDN and integrated voltage regulator design.

Shinyoung Park received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2015 and 2017, respectively, where she is currently pursuing the Ph.D. degree with a focus on ground integrity analysis in mixed-mode systems.

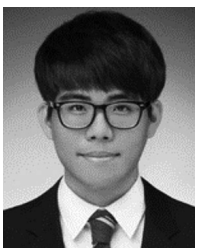


Daniel H. Jung received the B.S. degree in electrical engineering from Case Western Reserve University, Cleveland, OH, USA, in 2010, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2013 and 2018, respectively.

His current research interests include through-silicon via (TSV) defect analysis methods and self-repair redundancy configuration in TSV-based 2.5-D/3-D integrated circuit.

Junyong Park received the B.S. degree in electronic and electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2014, and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2016, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research focuses on advanced eye-diagram estimation methods for high-speed systems.

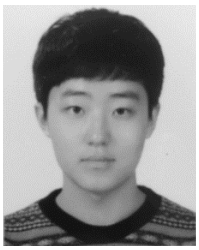


Gapyeol Park received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2016 and 2018, respectively, where he is currently pursuing the Ph.D. degree.

His current research interest includes the modeling and analysis of glass interposer for RF and digital systems.

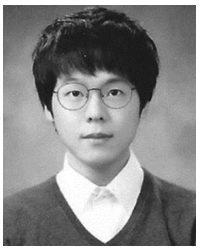
Seongguk Kim received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2018. He is currently pursuing the M.S. degree in electrical engineering with the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea.

His current research interests include signal integrity design and analysis of interconnection in processing-in-memory (PIM) systems based on high-bandwidth memory for high-performance computing.



Taein Shin received the B.S. degree in mechanical engineering from the Gwangju Institute of Science and Technology (GIST), Gwangju, South Korea, in 2018. He is currently pursuing the M.S. degree in electrical engineering with the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea.

His current research interest includes the design and analysis of 3-D interconnection for neuromorphic systems.



Youngwoo Kim (Member, IEEE) received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2013, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015 and 2018, respectively.

He is currently a Post-Doctoral Researcher with the KAIST Information and Electronic Institute. His research focuses on system-level signal/power integrity simulation and analysis, statistical signal integrity analysis considering power noise, and interposer technologies for 2.5-D/3-D integration.

Joungho Kim (Fellow, IEEE) received the B.S. and M.S. degrees from Seoul National University, Seoul, South Korea, in 1984 and 1986, respectively, and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA, in 1993, all in electrical engineering.

He joined the Memory Division, Samsung Electronics, Suwon, South Korea, in 1994, where he was involved in gigabit-scale DRAM design. In 1996, he joined the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea. He is currently a Professor with the Department of Electrical Engineering, KAIST. He is also the Director of the 3-D Integrated Circuit (IC) Research Center supported by SK Hynix, Inc., Icheon, South Korea, and the Smart Automotive Electronics Research Center supported by KET, Inc., Incheon. He has given more than 219 invited talks and tutorials in academia and related industries. He has authored or coauthored more than 404 technical papers in refereed journals and conference proceedings. He has authored a book entitled *Electrical Design of Through-Silicon-Via* (Springer, 2014). In particular, his major research interests include chip package printed circuit board (PCB) codesign and cosimulation for signal integrity, power integrity, ground integrity, timing integrity, and radiated emission in 3-D-IC, through-silicon via (TSV), and interposer. His current research interests include electromagnetic compatibility (EMC) modeling, design, and measurement methodologies of 3-D-IC, TSV, interposer, system-in package, multilayer PCB, and wireless power transfer (WPT) technology for 3-D-IC.