INTEL INVENTION DISCLOSURE

DWWRUQH\0FOLHQW#SULYLOHJHG#FRP P XQLFDWLRQ

Disclosure#84827

4/5/2011 (WW15)

Inventors

Inventor Name	WWID	Badge Type	Site Code	Resident Country	Email
NDX/#GHUFKDQJ	433::8<<	EE	VF	XVD	ghufkdqj1ndxC lqwho#frp
VSDGIQL/#JIDQSDROR#SDROR,	439<64<<	EE	VF	XVD	jldqsdror1vsdgiqlC lqwho#frp

Organization/Division(s)

Lqwho#Frusrudwlrq#D#QDQG#P HP RU\#GLY

Disclosure Details

Disclosure Title:

P hp ru|#Dffhvv#lq#d#Furvv#Srlqw#Duud|

Key words to describe the technology area of the invention:

RXP #SUDP #SFUDP #Furvv#Srlqw#QYP #JUDP /#SFP #SFP V#RWV

What technology/product/process (code name) does your invention relate to (be specific if you can):

SFP V

Specify any keywords that describe the technology area of the invention: (Characters "(" and ")" and words such as "and", "or" and "to" should not be used and will be removed.)

RXP #SUDP #SFUDP #Furvv#Srlqw#QYP #JUDP /#SFP #SFP V#RWV

Under which of the following classifications does this invention predominantly fall?

K ljk#Yroxp h#Dufklwhfwxuh=#Lqyhqwlrqv#hp erglhg#lq#frp sxwhu#v|vwhp #dufklwhfwxuh#ihdwxuhv#) #lqwhuidfhv p dgh#lq#kljk#yroxp hv1# Hqfrp sdvvhv#D/#ghylfhv#h1j1#wudqvlwruv,#dqg#dvvrfldwhg#p ij#surfhvvhv1

Was the substantive portion of the invention made outside the United States?

Qr

If yes, specify the country where the substantive portion of the invention was made.

If a description of your invention has been (or is planned to be) published outside of Intel, was the manuscript submitted for pre-publication approval through the Author Incentive Program?

Qr

If a description of your invention has been (or is planned to be) published outside of Intel, identify the publication.

If a description of your invention has been (or is planned to be) published outside of Intel, identify the date published.

If your invention has been sold or used internally or externally, or there are plans for sale or use of the invention internally or externally, what is the first date it was or will be used or sold by Intel or others?

If the subject matter of this disclosure has been disclosed or plans to be disclosed to any standard setting organization (JEDEC, IEEE, etc), provide the name of the organization.

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If the subject matter of this disclosure has been disclosed or plans to be disclosed to any standard setting organization (JEDEC, IEEE, etc), provide the date when it was disclosed.

If the invention is embodied in a semiconductor device, what is the actual or anticipated date of tapeout?

If the invention is Software, specify the actual or anticipated date of any beta tests or other distribution outside Intel?

If the invention was conceived or constructed in collaboration with anyone other than an Intel employee or as part of a project involving entities other than Intel (e.g. government (US or EU under FP7 or otherwise), companies, universities or consortia), provide the name of the individual or entity.

Is the invention related to any other invention disclosure that you have recently submitted? If so, please give the Title, Inventors and if possible, the assigned disclosure #.

Does this disclosure relate to a special harvesting project? If so, select the project.

lease provide a description of the invention and include the following information:

A. THE INVENTION

. Describe your invention:

a. What problem(s) does your invention solve?

To reduce decoder footprint of multi-stack cross point memory array.

b. What is the invention, what are the components, and how does it work?

A column driver is connected to a row of OTS switches. The OTS switches is cross connected to the columns in the cross point PCMS array. One small footprint decoder connected to each of columns in the array serves as the trigger to select the column uniquely. When the column decoder is triggered, the OTS switch is turned on, The selected column voltage is boosted to column driver level. The access of single memory cell can be achieved. The same technique is also applicable to row decoder.

2. How is your invention new:

a. How is the problem currently being solved?

Dedicated column and row decoders with large device footprint to deliver the current drive required for the access of a single memory cell in the cross point array.

b. What does your invention do to solve the problem differently from current solutions?

. One column drivers (large footprint)for entire array + dedicated column triggers (small footprint) for each column vs. dedicated column drivers 2. Multi-stack using common row drivers + dedicated column trigger vs. shared column and row drivers with bi-layer architecture. 3. This same method is also applicable to reduce row driver/decoder footprint.

c. What specific components/features of your invention are not present in current solutions?

Embedded OTS Switch in PCMS memory technology.

d. To the best of your knowledge, identify any other pertinent information related to your invention.

None available.

e. Describe any aspect(s) of your invention relating to unusual results or unusual functions of the components/techniques in the invention, OR check the box below.

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3. You MUST include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.

State of the art (POR) cross point memory array is formed with fully decoded drivers for bitlines, BD_y and wordlines, WD_x. BD_y and WD_x devices size need to be sufficiently large to deliver the voltage and current required for read/write operations. (Fig.)

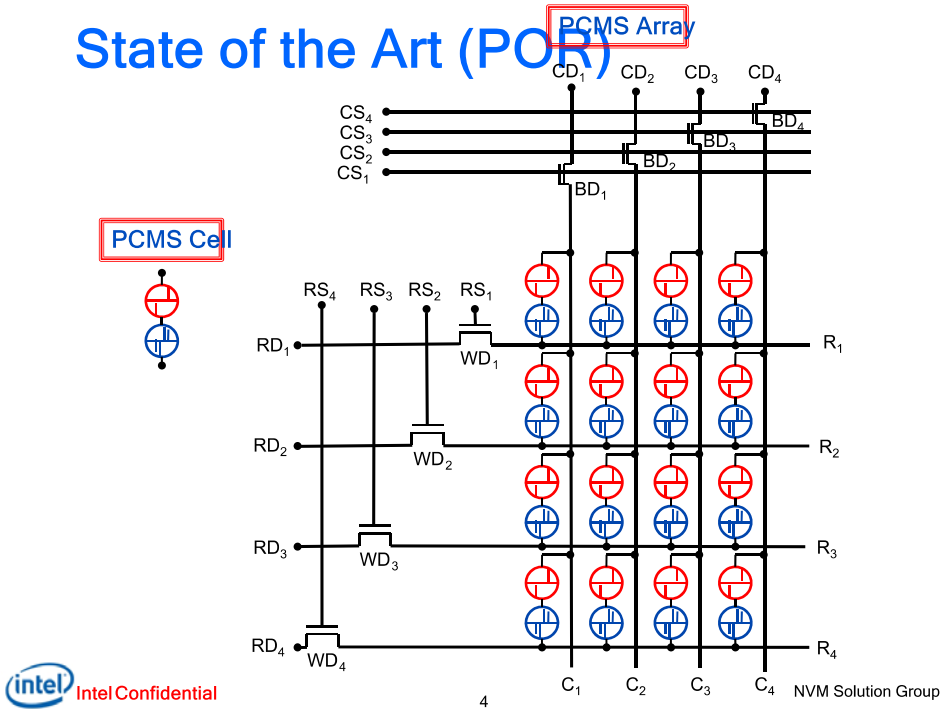

Fig. State of the art cross point memory array such as PCMS.

This invention is to reduce the footprint required for bitline and wordline drivers. It uses a smaller decoded transistor for each of bitlines (BT_x) and one driver circuit shared with all the bitlines. shown in Fig 2. The same technique is applicable to the wordline transistor (WT_y) selection scheme. Shown in Fig 3, the schematics illustrates the circuit topology on both bitline and wordline selection using the same triggering mechanism.

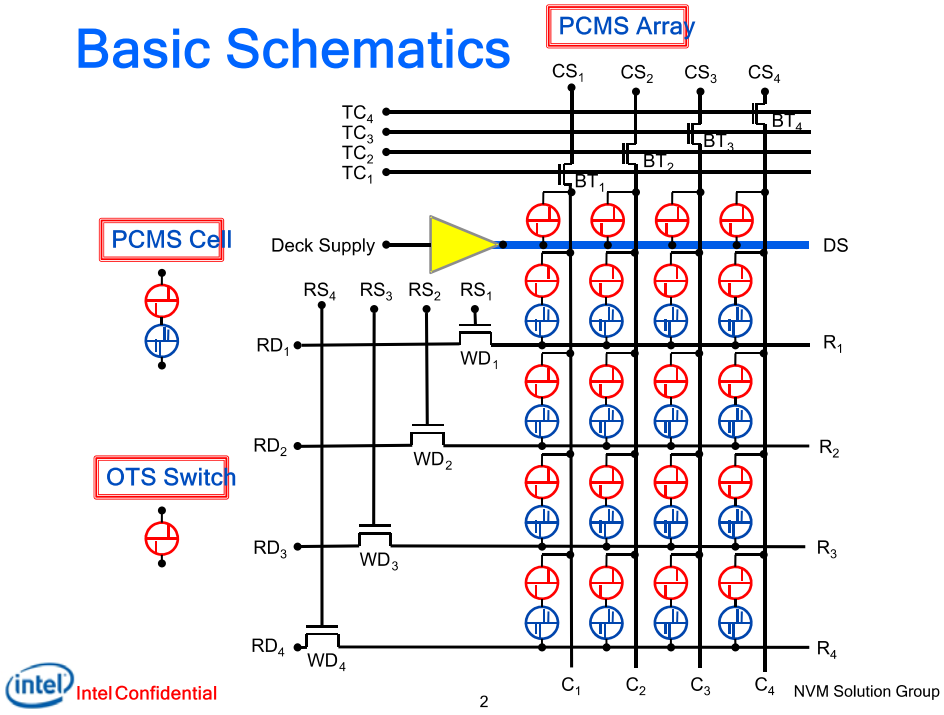

Fig 2. Basic schematics of this invention. It uses a row of OTS switches cross connected to each column. The size of the column selection transistors, BT_y, is smaller than column drivers in the current art cross point memory array.

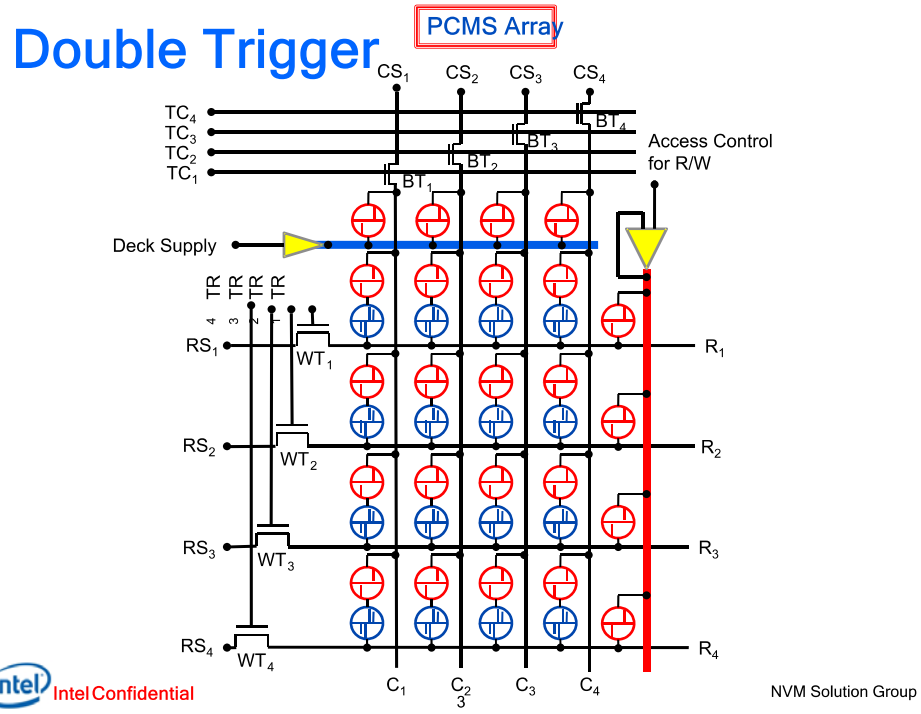

Fig. 3. Deploying the same concept of select trigger mechanism, the embodiment illustrates smaller select transistors on both column and row decoder.

There are several methods making OTS switches, shown in Fig. 4. In one embodiment, OTS switch can be made by shorting multiple rows and/or shorting multiple columns in a PCMS array. In another embodiment, the switch can be made by a wider row and/or wider column. Due to larger cross point area of those devices than that of a PCMS cell, PCM remains in crystalline state subject to normal operating condition. Thus a OTS switch is formed.

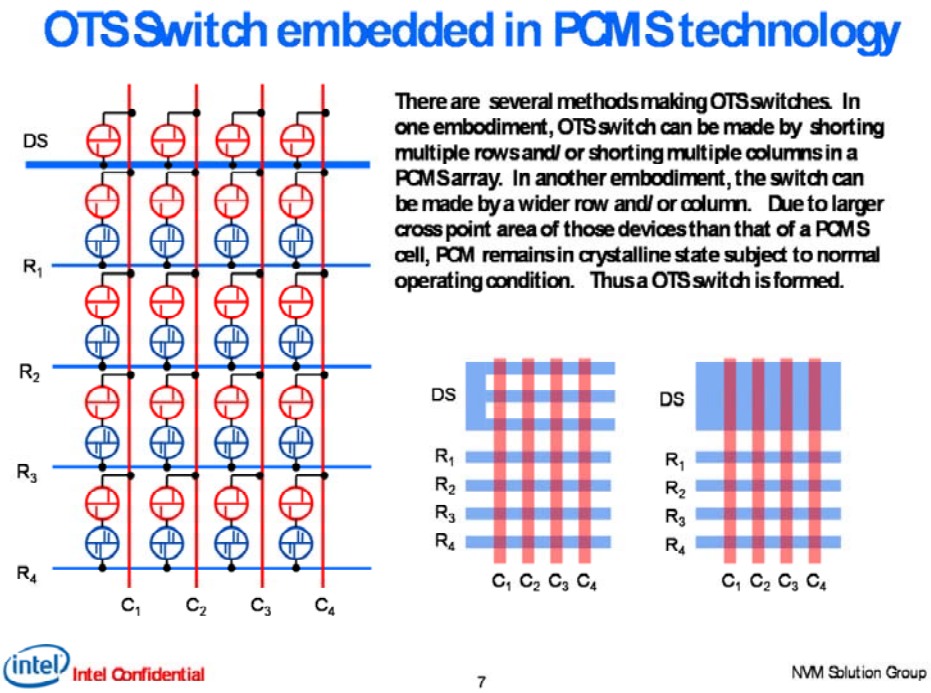

Fig 4. Forming OTS switch in a PCMS technology.

We will use the basic schematics as shown in Fig 2 to illustrate how to select one bit in a array. To select cell C_4R_4, array bias is shown in Fig.5. The column selection is done by pulsing TC_4 node. As soon as, OTS on C_4 is turned on, the "Deck supply" will pull up C_4 to 5 volts. The potential drop between C_4 and R_4 will become 0V therefore threshold switch the PCMS cell C_4R_4 to complete the memory access.

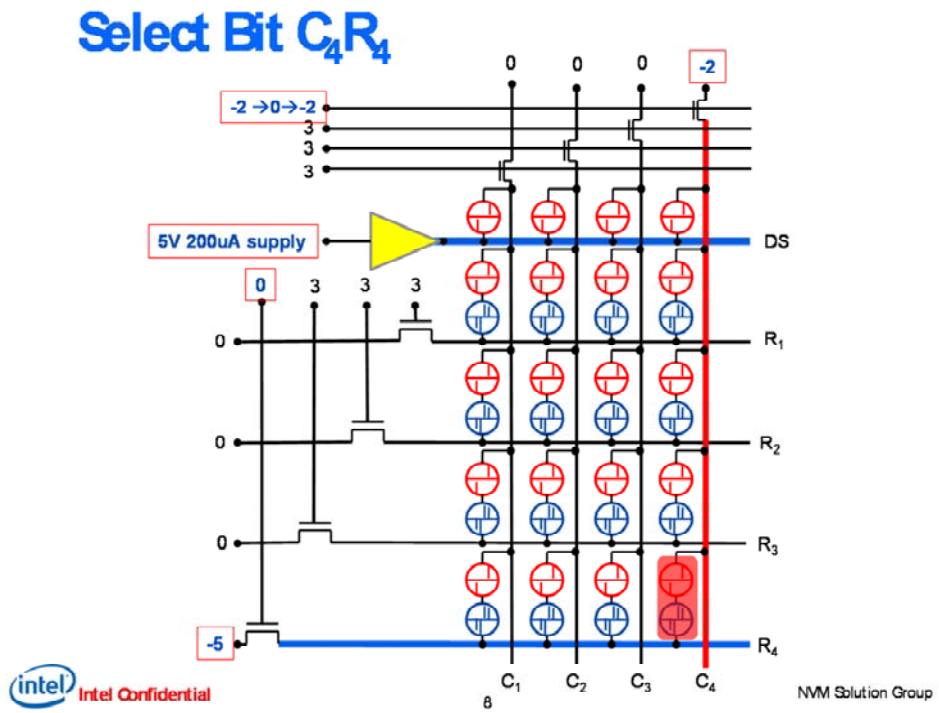

Fig. 5. Select Bit C_4R_4 with column trigger mechanism.

The detailed timing is shown in Fig. 6.

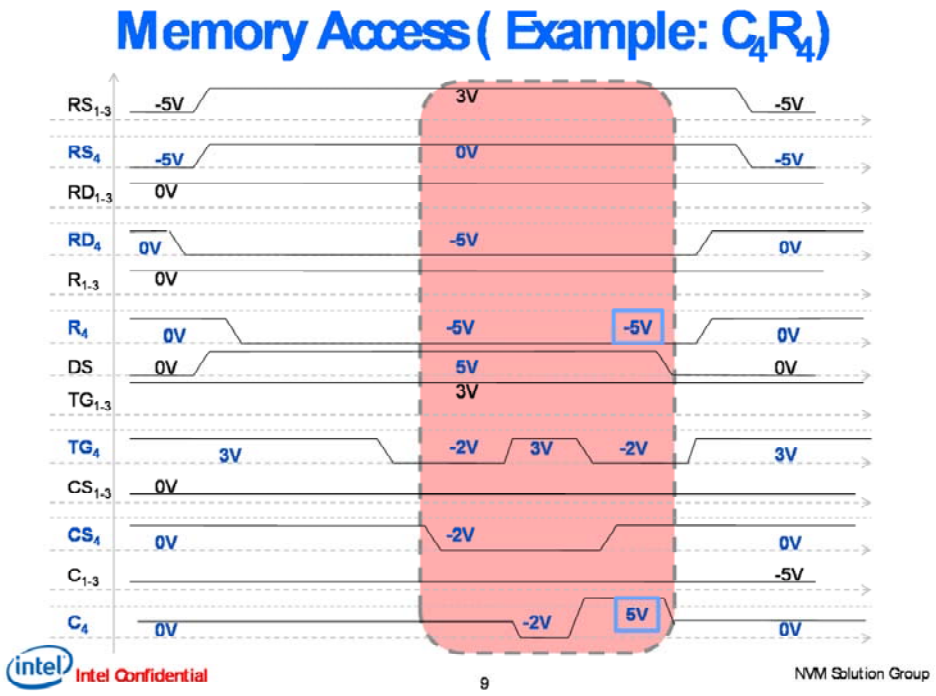

Fig. 6. Timing diagram for the selection of cell C_4R_4 in a column select trigger technique.

To implement column trigger select scheme in a multi-deck cross point memory array, three embodiments are illustrated, as shown in Fig.7, Fig.8 and Fig.9.

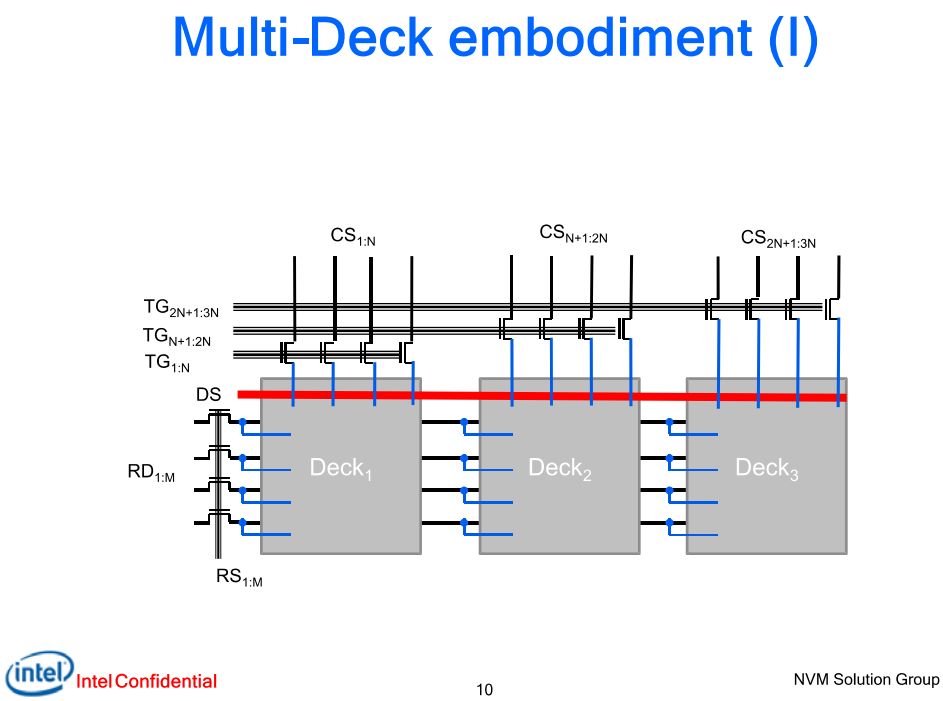

Fig. 7. Fully decoded column select.

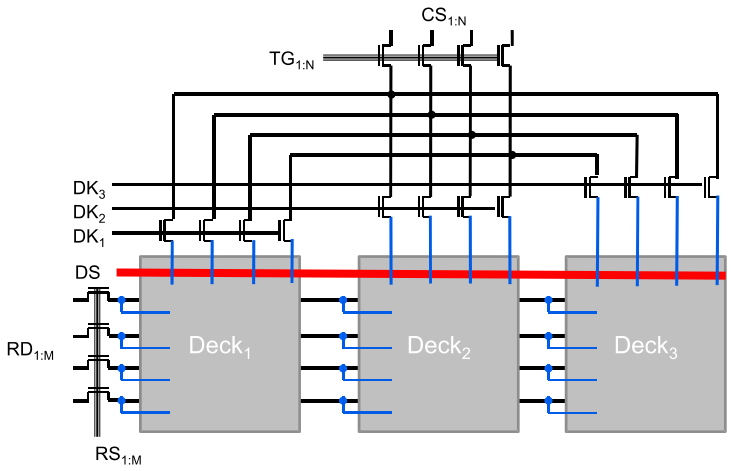

Fig. 8. Sharing column decode circuit between decks with deck isolation transistors.

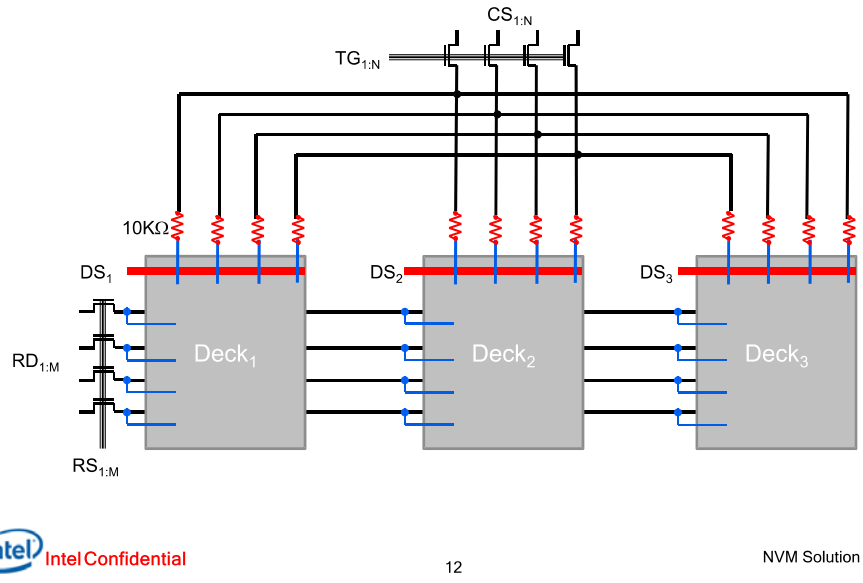

Fig. 9. Sharing column decode circuit between decks with deck isolation resistors.

In one embodiment of double trigger scheme (both column and row), Fig. 0 illustrates the bias to access the cell C_4R_4 in the array. In this example, column select is triggered by

pulsing TC_4 and bitline C_4 is therefore pulled up to 5V. Likewise, row select is triggered by pulsing TR_4 and wordline R_4 is pulled down to -5V. Once the voltage at cross point is higher than the threshold voltage of the cell, cell C_4R_4 is successfully threshold and accessed.

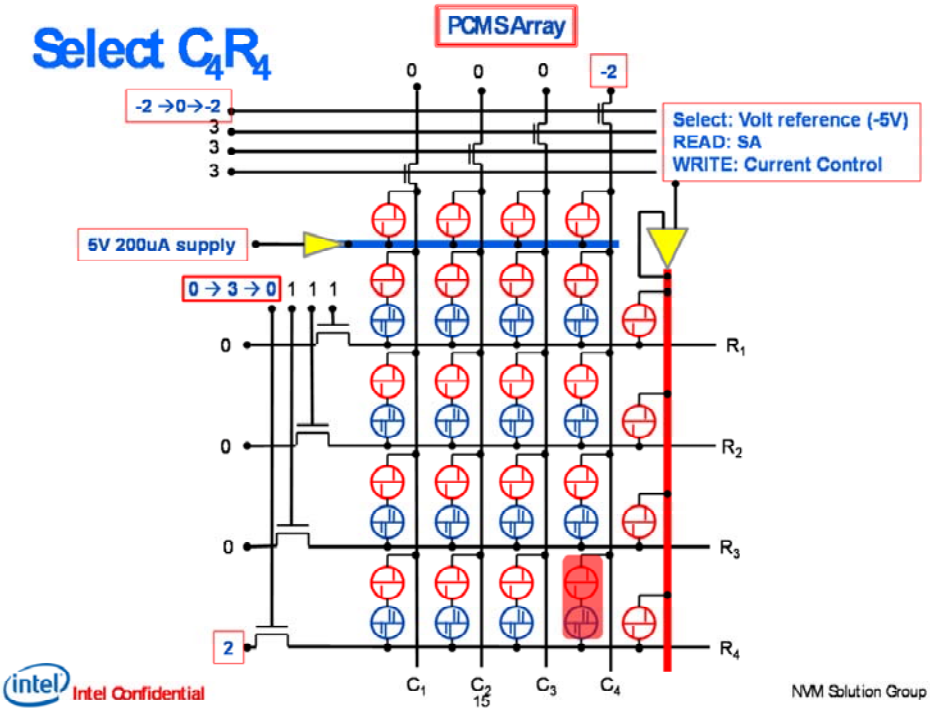

Fig. 0. Both columns and rows use select trigger mechanism for access one cell

B. VALUE RO OSITIONS AND DETECTABILITY

. Value of your invention to Intel (how will it be used by Intel or a competitor).

A candidate for 4 stacks PCMS implementation for smaller tile density without degrading array layout efficiency.

2. Who is likely to want to make, use or sell this invention?

DRAM and NAND Incumbents and new players.

3. How would use of the technology by others be detected (i.e. how would you determine whether someone else was using your invention)?

Operating spec and SEM.