INTEL INVENTION DISCLOSURE

ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

Disclosure#80682

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Inventors

Inventor Name	WWID	Badge Type	Site Code	Resident Country	Email
KAU, DERCHANG	10077599	BB	SC	USA	derchang.kau@intel.com

Organization/Division(s)

Intel Corporation - NAND MEMORY DIV

Disclosure Details

Disclosure Title:

Program Verification of PCMS

Key words to describe the technology area of the invention:

Drift, Glass Relaxation, OTS, OUM, OUMS, PCM, PCMS, Program Verify, Read window

What technology/product/process (code name) does your invention relate to (be specific if you can):

PCMS

Under which of the following classifications does this invention predominantly fall?

High Volume Architecture: Inventions embodied in computer system architecture features & interfaces made in high volumes. Encompasses IA, devices (e.g., transistors) and associated mfg. processes.

If a description of your invention has been (or is planned to be) published outside of Intel, was the manuscript submitted for pre-publication approval through the Author Incentive Program?

If a description of your invention has been (or is planned to be) published outside of Intel, identify the publication.

If a description of your invention has been (or is planned to be) published outside of Intel, identify the date published.

If your invention has been sold or used internally or externally, or there are plans for sale or use of the invention internally or externally, what is the first date it was or will be used or sold by Intel or others?

If the subject matter of this disclosure has been disclosed or plans to be disclosed to any standard setting organization (JEDEC, IEEE, etc), provide the name of the organization.

If the subject matter of this disclosure has been disclosed or plans to be disclosed to any standard setting organization (JEDEC, IEEE, etc), provide the date when it was disclosed.

If the invention is embodied in a semiconductor device, what is the actual or anticipated date of tapeout?

If the invention is Software, actual or anticipated date of any beta tests or other distribution outside Intel?

If the invention was conceived or constructed in collaboration with anyone other than an Intel employee or as part of a project involving entities other than Intel (e.g. government (US or EU under FP7 or otherwise), companies, universities or consortia), provide the name of the individual or entity.

Is the invention related to any other invention disclosure that you have recently submitted? If so, please give the Title, Inventors and if possible, the assigned disclosure #.

Please provide a description of the invention and include the following information:

A. THE INVENTION

1. Describe your invention:

   a. What problem(s) does your invention solve?

Due to the relaxation of PCMS, both SET and RESET threshold voltages will increase in time, a.k.a. "Drift." This disclosure presents a "Program Verification" strategy to improve write cycle time and throughput.

   b. What is the invention, what are the components, and how does it work?

Demarcation READ time interval:

In a PCMS memory array, the SET and RESET threshold voltage distributions are delineated by a demarcation voltage, V_{DM}. V_{DM} is hence used to interrogate the state of the memory. When a memory threshold voltage is lower than V_{DM}, the memory cell thresholds and the interrogation returns the "1" state; likewise, if the memory dose not threshold and the interrogation will return the "0" state. Therefore 'SET' and 'RESET' threshold voltage distributions of a PCMS memory array cannot be overlapped (See fig. 1 below.)

Due to the glass relaxation physics of PCMS, both SET and RESET threshold voltages will increase in time, a.k.a. "Drift." As illustrated in fig 2, the threshold voltage drifts linearly proportional to the log of time, R_{Drift}.

$$R_{Drift} = \left[V_t @ t_2 - V_t @ t_1\right] \Big/ \left[\log(t_2) - \log(t_1)\right]$$

The drift timer of each memory cell is re-initialized immediately followed by the event of threshold. This event can be a reading of a memory in SET-State or writing a memory. In order to distinguish "1" and "0" of PCMS, the RESET threshold voltage must be higher than the SET threshold voltage retained a period time after READ or WRITE. Therefore, there exists a finite time window to ascertain the states of memories. This time window is between the shortest time, t_{init}, after RESET and longest time, t_{fin}, after SET or READ. A typical t_{init} is 3msec and a typical t_{fin} is 1 year.

Verfication and level and timing:

A RESET pulse width of PCMS is 10s nsec or faster. To take advantage of the high speed operation, a demarcation read verify should be done within 10s nsec after RESET pulsing. This is typically a few decades faster than t_{init} for read window budget

allocation. Applying READ demarcation level to RESET verification will result in over RESET.

Lower demarcation level based on shorter time to verify:

In PCMS, verification is only needed for RESET operation. Due to 'self inhibiting, shown in table 1, the RESET intended memory cells will threshold for RESET only if resident data is in SET-state. That is, if bit doesn't threshold, it is in RESET state. For the bits perform RESET operation, drift time counter is 're-initialized' due to 'threshold event' incurred by 'RESET' operation. Verification is done with a fixed timing after RESET incurred threshold. The corresponding drift time is fixed (Fig. 3). Regardless the successfulness of RESET pulsing, the drift timer will be re-initiated subject to threshold event. Also the corresponding threshold voltages are lower due to less drift at verification timing (~10nsec). Consequently, a window exists between failed and succeeded RESET after a fixed drift time. Therefore, V_{Verify} is lower than V_{READ} due to time to verify after RESET pulse is shorter than time to first READ operation.

2. How is your invention new:

   a. How is the problem currently being solved?

PCMS Cross Point Memory Array is a new class of memory/storage component. The knowledge of PCMS threshold voltage drift is not available outside Intel/Numonyx JDP. The author are not aware of any current art solving the new class of memory/storage components.

Alternatively, amorphous PCM exhibits similar resistance "Drift" characteristics in sub-threshold regime. There may be similar technique used for RESET program verification for resistance detection mechanism in a PCM or RRAM.

   b. What does your invention do to solve the problem differently from current solutions?

This is based on the threshold detection and drift property of both SET and RESET state of PCMS. There is no known technology based on this method.

   c. What specific components/features of your invention are not present in current solutions?

   d. To the best of your knowledge, identify any other pertinent information related to your invention.

This disclosure explores the opportunity of improving PCMS program cycle time subject to 'Drift'. The Drift properties of glass material are well known behavior. The invention may be applicable to other class of Resistive memory with thin film selector such as OTS or oxide-based diode in threshold detection and/or resistance read scheme.

e. Describe any aspect(s) of your invention relating to unusual results or unusual functions of the components/techniques in the invention, OR check the box below.

☐ The unique combination of components/techniques in this invention provides an improvement over previously known structures and techniques.

3. You MUST include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.

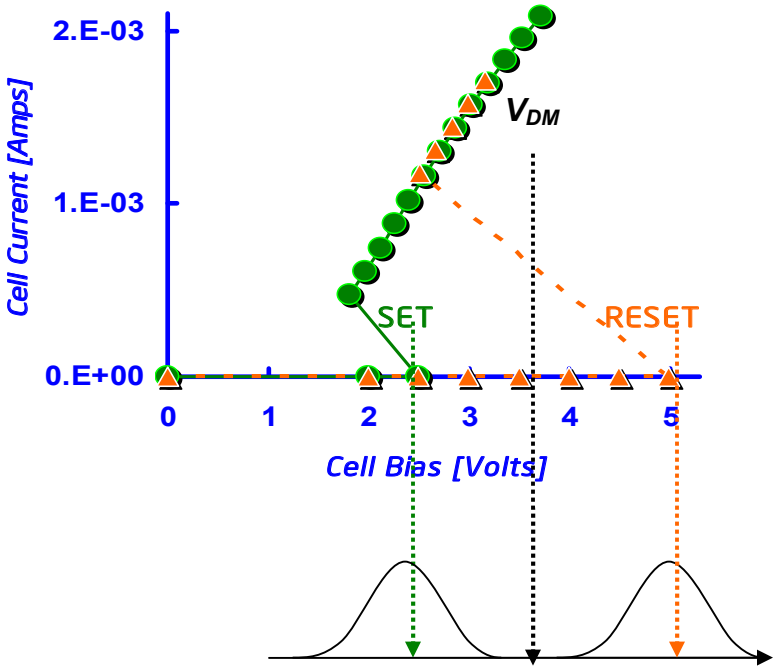

Fig 1. The SET and RESET threshold voltage distributions cannot be overlapped and are delineated by a demarcation voltage, V_{DM}.

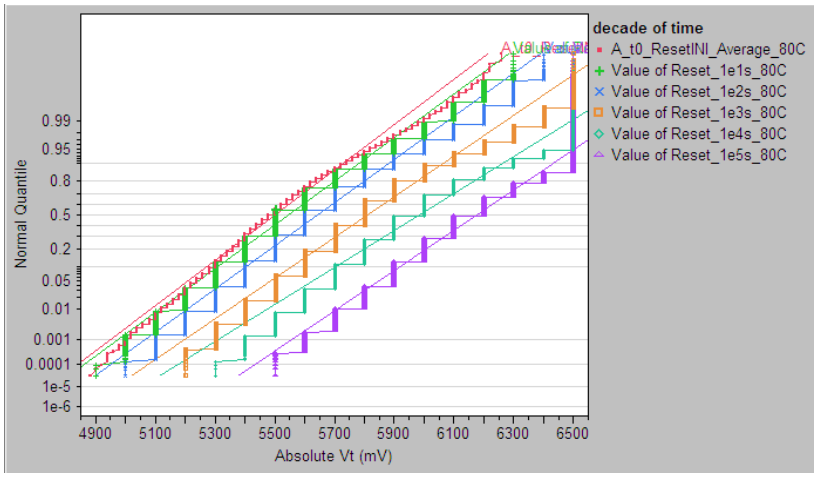

Fig 2. The threshold voltage drifts linearly proportional to the log of time

Table 1. An example of WRITE Operation of PCMS: RESET is requested for Bit-0, -2 ,-5, -6. Resident data of bit-2 and bit-5 are in RESET state. Therefore, the RESET operation is inhibited at both locations (blue marked cells). Only bit-0 and bit-6 will perform RESET operation.

Bit Location	0	1	2	3	4	5	6	7	Number of Operable bits
DQin	0	1	0	1	0	0	1	1	8
Resident Data	1	0	0	1	1	0	1	0	8
RESET									
RESET Pattern	0		0		0	0			4
Selection	X		X		X	X			4
RESET operation	X				X				2
Post RESET Data	0	0	0	1	0	0	1	0	
SET									
SET Pattern		1		1			1	1	4
Selection		X						X	2
SET operation		X						X	2
Post SET Data	0	1	0	1	0	0	1	1	8

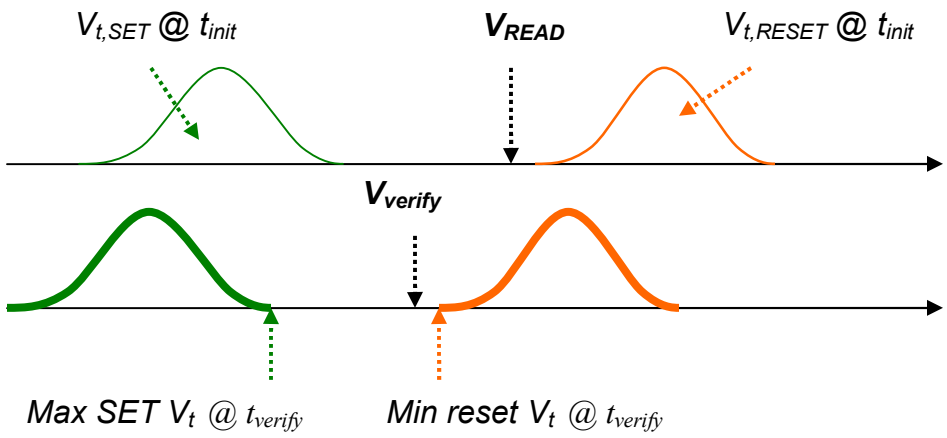

Fig 3. V_{Verify} is lower than V_{READ} due to time to verify after RESET pulse is shorter than time to first READ operation. Regardless the successfulness of RESET pulsing, the drift timer will be re-initiated subject to threshold event.

B. VALUE PROPOSITIONS AND DETECTABILITY

1. Value of your invention to Intel (how will it be used by Intel or a competitor).

RESET Verification is a vital procedure to warrant low WRITE failure probability. The proposed program verification algorithm improves WRITE cycle time therefore write-throughput.

2. Who is likely to want to make, use or sell this invention?

PCMS memory chip manufacturers and/or memory chip controllers.

3. How would use of the technology by others be detected (i.e. how would you determine whether someone else was using your invention)?

Product Spec and/or Micro-Probe of chip.