INTEL INVENTION DISCLOSURE

ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

Disclosure#80667

5/8/2010 (WW19)

Inventors

Inventor Name	WWID	Badge Type	Site Code	Resident Country	Email
KAU, DERCHANG	10077599	BB	SC	USA	derchang.kau@intel.com
FAZIO, ALBERT	10029929	BB	SC	USA	al.fazio@intel.com

Organization/Division(s)

Intel Corporation - NAND MEMORY DIV

Disclosure Details

Disclosure Title:

PCMS Wear Leveling --- Managed READ Access

Key words to describe the technology area of the invention:

OTS, OUM, OUMS, PCM, PCMS, Read window, Wear-leveling

What technology/product/process (code name) does your invention relate to (be specific if you can):

PCMS

Under which of the following classifications does this invention predominantly fall?

High Volume Architecture: Inventions embodied in computer system architecture features & interfaces made in high volumes. Encompasses IA, devices (e.g., transistors) and associated mfg. processes.

If a description of your invention has been (or is planned to be) published outside of Intel, was the manuscript submitted for pre-publication approval through the Author Incentive Program?

If a description of your invention has been (or is planned to be) published outside of Intel, identify the publication.

N/A

If a description of your invention has been (or is planned to be) published outside of Intel, identify the date published.

If your invention has been sold or used internally or externally, or there are plans for sale or use of the invention internally or externally, what is the first date it was or will be used or sold by Intel or others?

If the subject matter of this disclosure has been disclosed or plans to be disclosed to any standard setting organization (JEDEC, IEEE, etc), provide the name of the organization.

If the subject matter of this disclosure has been disclosed or plans to be disclosed to any standard setting organization (JEDEC, IEEE, etc), provide the date when it was disclosed.

If the invention is embodied in a semiconductor device, what is the actual or anticipated date of tapeout?

If the invention is Software, actual or anticipated date of any beta tests or other distribution outside Intel?

If the invention was conceived or constructed in collaboration with anyone other than an Intel employee or as part of a project involving entities other than Intel (e.g. government (US or EU under FP7 or otherwise), companies, universities or consortia), provide the name of the individual or entity.

Is the invention related to any other invention disclosure that you have recently submitted? If so, please give the Title, Inventors and if possible, the assigned disclosure #.

Please provide a description of the invention and include the following information:

A. THE INVENTION

1. Describe your invention:

   a. What problem(s) does your invention solve?

Due to the glass relaxation of PCMS, both SET and RESET threshold voltages increase in time, a.k.a. "Drift." This disclosure presents a PCMS media management strategy for data integrity subject to Drift.

   b. What is the invention, what are the components, and how does it work?

Drift of PCMS

Due to the relaxation of glass material, threshold voltages will increase in time. The threshold voltage drifts linearly proportional to the log of time, with a slope of R_{Drift}.

$$R_{Drift} = \left[V_t @ t_2 - V_t @ t_1\right] \Big/ \left[\log(t_2) - \log(t_1)\right]$$

The drift behavior is observed in both in OTS and PCM therefore SET and RESET states of a PCMS memory cell, as illustrated in Fig. 1. The drift clock is re-initialized immediately followed by the event of threshold. This event can be a reading of a memory in SET-State or writing a memory.

READ after Drift

In a PCMS memory array, the SET and RESET threshold voltage distributions are delineated by a demarcation voltage, V_{DM}. V_{DM} is hence used to interrogate the state of the memory. When a memory threshold voltage is lower than V_{DM}, the memory cell thresholds and the interrogation returns the "1" state; likewise, if the memory dose not threshold and the interrogation will return the "0" state. In order to distinguish "1" and "0" of PCMS, the RESET threshold voltage must be higher than the SET threshold voltage during a period time. Therefore, there exists a finite time window to ascertain the states of memories. This time window is between the shortest time, t_{init}, after RESET and longest time, t_{fin}, after SET or READ. (Fig. 2)

Method 1: As a part of READ Window

Due to the threshold drift, a Vt separation between SET and RESET at initial state must be established to allow "Drift" between t_{init} and t_{fin}. Therefore the addition of RESET threshold voltage, ΔVt_{Drift}, at t_{init} must be equal to or higher than the SET threshold drift voltage from t_{init} and t_{fin}. (Fig 3)

$$\Delta Vt_{Drift} \geq R_{Drift.SET} \cdot \log(t_{fin}/t_{init}),$$ where $R_{Drift.SET}$ is the rate of SET Vt Drift in [V/dec]

The time window between t_{init} and t_{fin} restricts useable memory access latency. An example of memory lock-out from read access is illustrated below. A typical 5-volt PCMS storage spec requires 1 yr retention. The Window budget capability for 10 decades drift consumes 2.5V, 50% of operating voltage range. And, for retention spec of t_{fin} = 1 yr (3e7 sec) , t_{init} is 3 msec. That is, there is a 3msec lock-out time for READ access of the memory after WRITE (Fig 4.)

Method 2: Invoking a tracking mechanism

Coupled with Method 1, a tracking mechanism can be deployed to widen the time window with a controller chip. The widened time window is characterized with the faster initial time t_0 and longer retention time t_1. A intermediate time, t_{ref}, is chosen such that $t_1/t_{ref} = t_{fin}/t_{init}$. Hence, the Vt window component consumed by SET Drift, ΔVt_{Drift}, is the same as Method 1. To read the memory cells between t_0 and t_{ref}, a lower demarcation voltage is required in account for lower RESET Vt drift. In addition, the address of the lower drift memories is time stamped. When drift timer exceeds t_{ref}, the marked address is expired and the register becomes available for the newly initialized memories, by READ or WRITE. The maximum numbers of the tracking registers are t_{ref}/t_0. (Fig. 5)

Method 3: Low energy and long retention background refresh

Final drift time, t_{fin}, is driven by

1) the delineation between final drift SET and initial drift RESET and
2) the maximum operable voltage headroom to SET a final drift RESET bit.

The controller can routinely refresh PCMS chips before the expiration of retention (due to drift) clock. A READ operation, ~10pJ/bit, ~10nsec, is able to reinitialized "SET" drift clock and a RESET operation, ~100pJ/bit, ~100nsec, is able to reinitialized "RESET" drift clock. Not SET operation, ~300pJ/bit, ~500nsec, is required for drift refresh. For example of refreshing a 16GB device, the total refresh energy is less than < 10 joules, the total refresh time < 50 seconds. A background "slow" refresh can be deployed with 4μW/die at monthly refreshing rate.

2. How is your invention new:
   a. How is the problem currently being solved?

PCMS Cross Point Memory Array is a new class of memory/storage component. The knowledge of PCMS memory controller is not available outside Intel. The authors are not aware of any current art solving PCMS Drift physics.

   b. What does your invention do to solve the problem differently from current solutions?

c. What specific components/features of your invention are not present in current solutions?

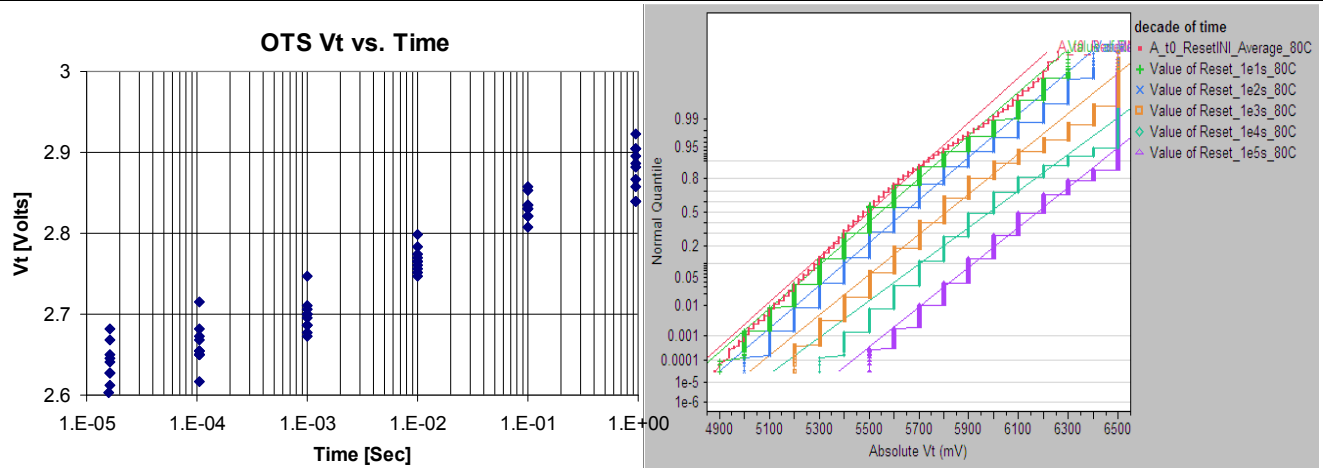
d. To the best of your knowledge, identify any other pertinent information related to your invention.

This disclosure explores the opportunity of extending PCMS data retention and the corresponding time window subject to the 'Drift'. The Drift properties of glass material are well known behavior. The invention may be applicable to other class of Resistive memory with thin film selector such as OTS or oxide-based diode.

e. Describe any aspect(s) of your invention relating to unusual results or unusual functions of the components/techniques in the invention, OR check the box below.

☐ The unique combination of components/techniques in this invention provides an improvement over previously known structures and techniques.

3. You MUST include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.



(A) (B)

Fig 1. (A) Threshold voltage vs, time of a single cell OTS. (B) The threshold voltage distributions of RESET PCMS array a time after RESET.

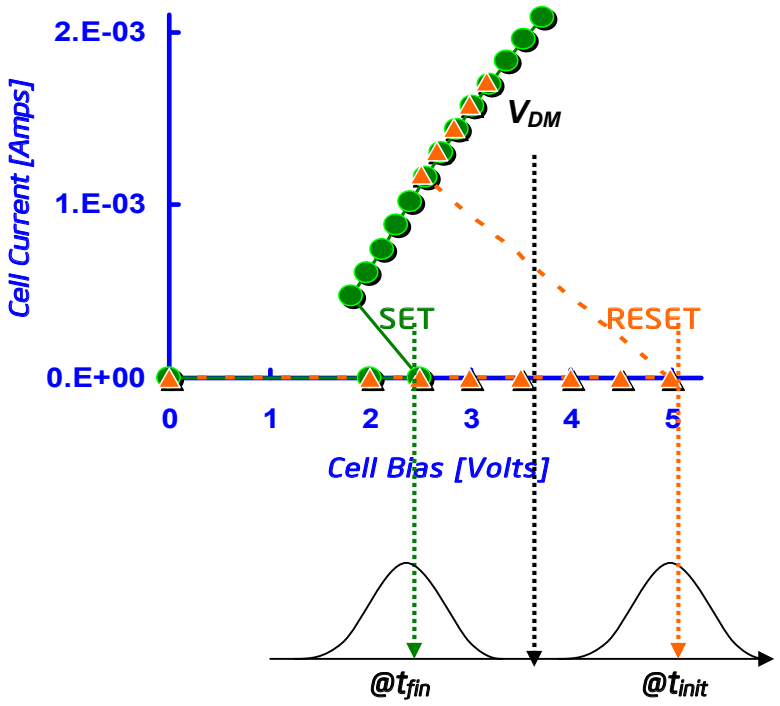


Fig 2. To distinguish RESET and SET distribution from t_{init} to t_{fin}, the RESET threshold at t_{init} after WRITE must be higher than the SET threshold voltage retained within t_{fin}.

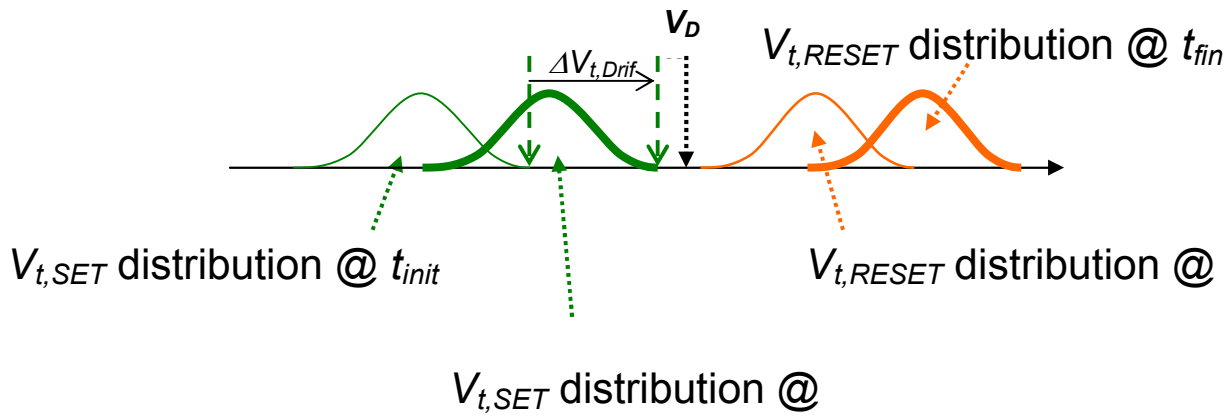


Fig 3. SET Vt drift as a part of Read window budget.

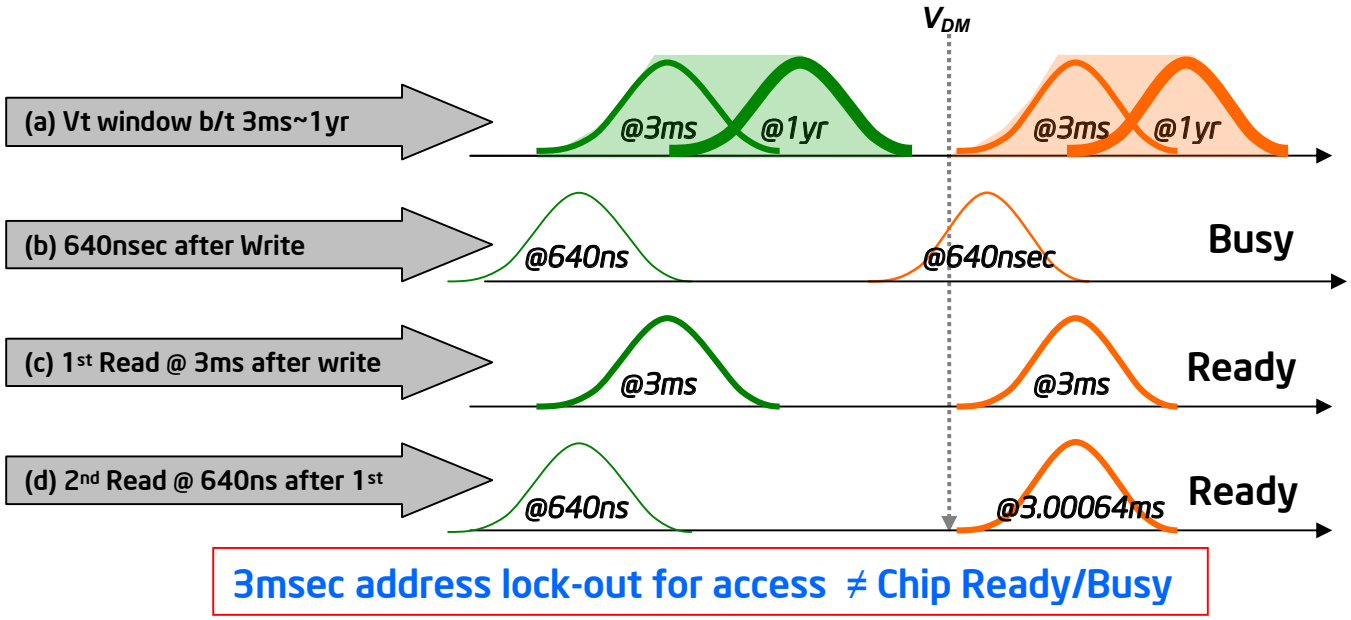


Fig 4. (a) Read window budget allocation. (b) Vt distribution of PCMS immediately after the WRITE cycle. The memory READ/WRITE access cycle time is 640nsec. The reinitialized RESET memory cells exhibited threshold voltage than READ voltage, therefore, the memory cell is lock-out from READ access. (c) After 3msec of lock-out, the memory cells become eligible for READ. (d) There is no access lock-out for the subsequent READ.

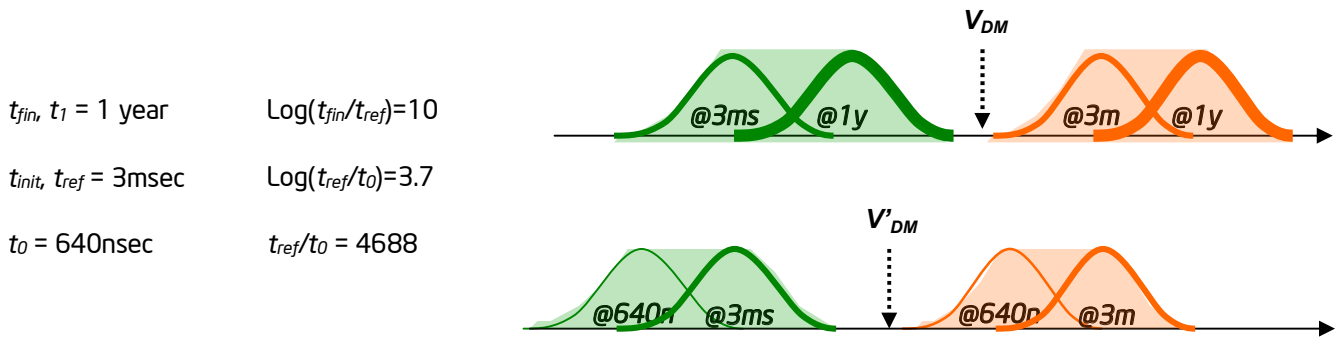


Fig. 5. Tracked by the proposed memory controller, the address of the shorter time drift memory is time stamped. The corresponding demarcation READ voltage, V'_{DM} is lower than the nominal READ voltage, V_{DM}. In this example, READ lock-out can be eliminated by the tracking mechanism using a memory controller with maximum of 4688 tracking registers.

B. VALUE PROPOSITIONS AND DETECTABILITY

1. Value of your invention to Intel (how will it be used by Intel or a competitor).

A wear-leveling function to reading PCMS memory chip can be implemented in a memory controller and host interface chip. The invention discloses an unique capability of improve PCMS read performance and data retention based on the physics of glass material.

2. Who is likely to want to make, use or sell this invention?

Storage and Memory module suppliers.

3. How would use of the technology by others be detected (i.e. how would you determine whether someone else was using your invention)?

Memory controller or host interface usage and timing spec.