Apple A14 in iPhone 12 – First Looks

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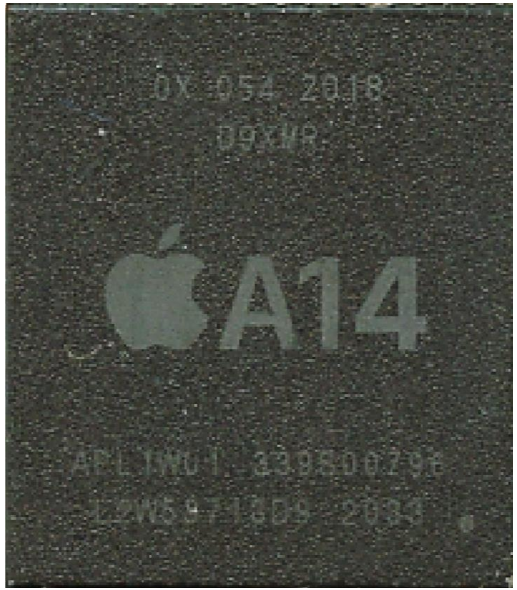
Package Level Image



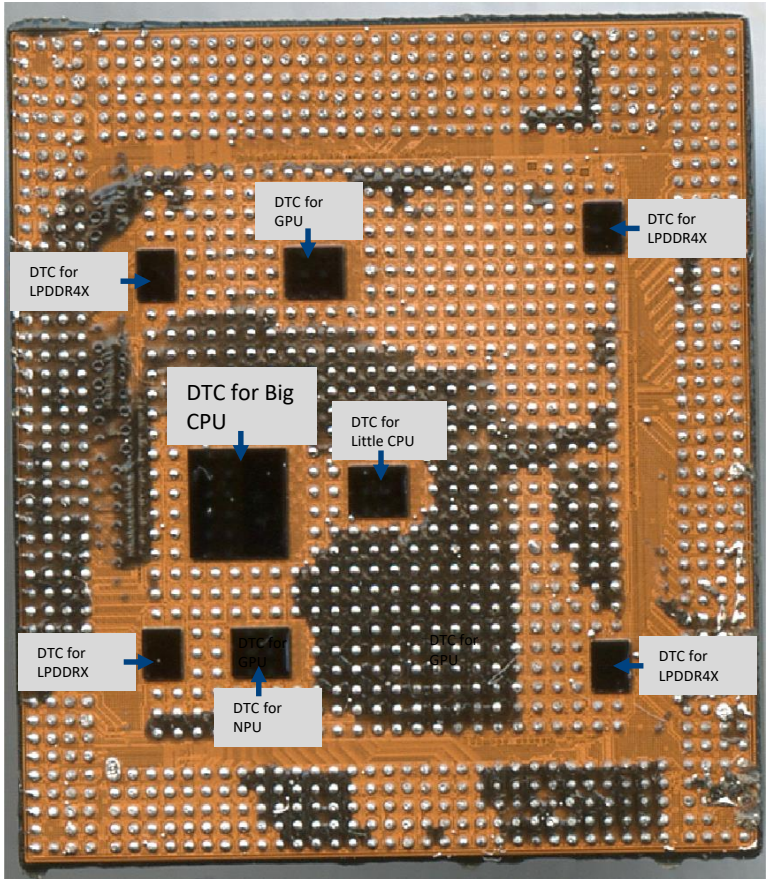
From iPhone

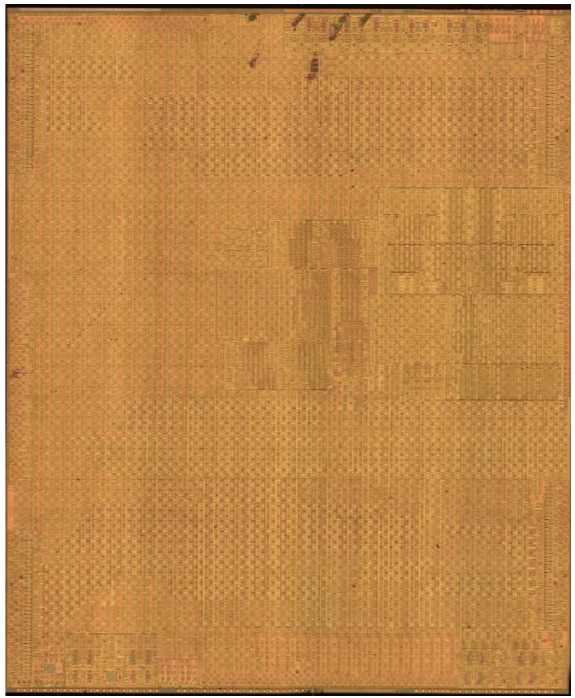
From iPad

Package images show InFOPoP with DRAM sourcing from Micron and SkHynix

Package and RDL Level Image

Physical die size: 8.577 mm x 10.352 mm2 ~ 88.8 mm^2
Within Guard Ring die size: 8.533 mm x 10.183 mm ~ 86.9 mm^2
Minimum bump pitch in IO is 90 µm. In the Core area it is 110 µm





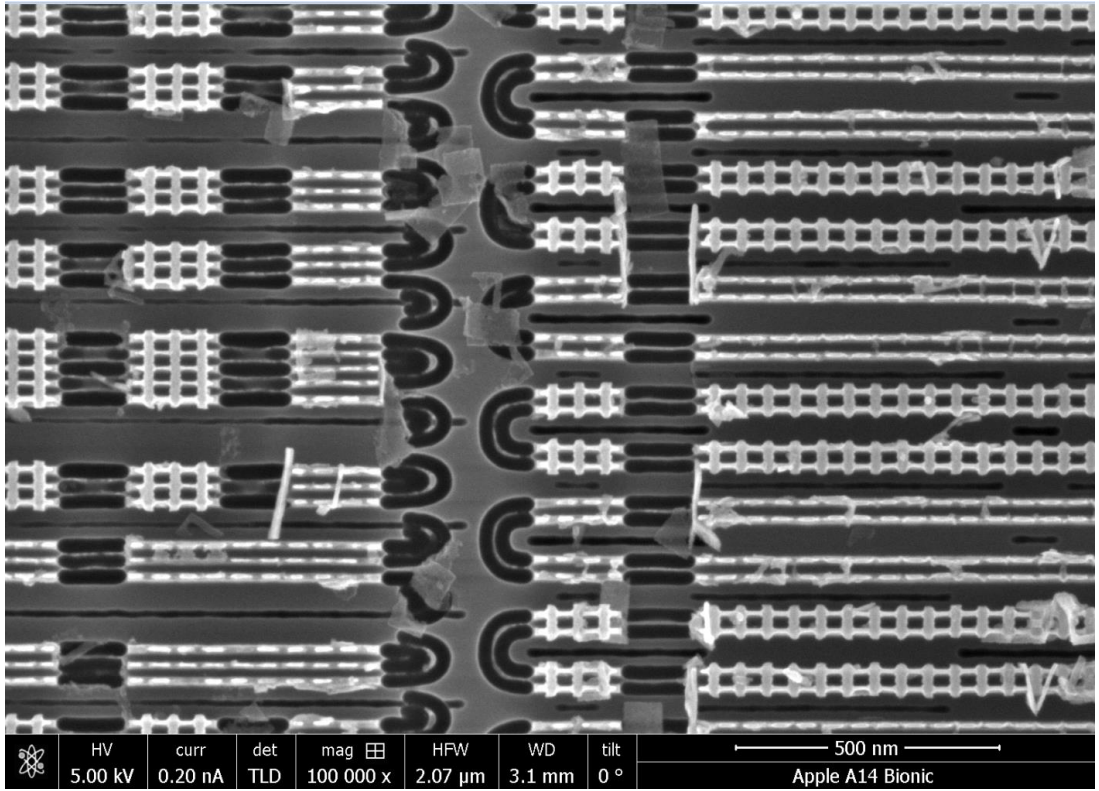
Die ID

Process and layout analysis

TSMC 7 (H240) Vs. TSMC 5 (H210)

Process	N7	N7+	N5
CPP	57 nm	57 nm	51 nm
Diff. Break	DDB	SDB	SDB
M2	40 nm	40 nm	35 nm
M1:Poly Gear ratio	1:1	2:3	2:3
M0	40 nm, Uni-dir 4 M0 tracks	40 nm, Uni-dir 4 M0 tracks	28 nm, Uni-dir 5 M0 tracks
Major Process Change	Co VCN with W VCX	4-5 EUV layers	• SiGe Channel in PMOS • Continuous diffusion with GTD isolation • Full COAG • VCX power rail • MGC instead of PCT

Fin Pattern

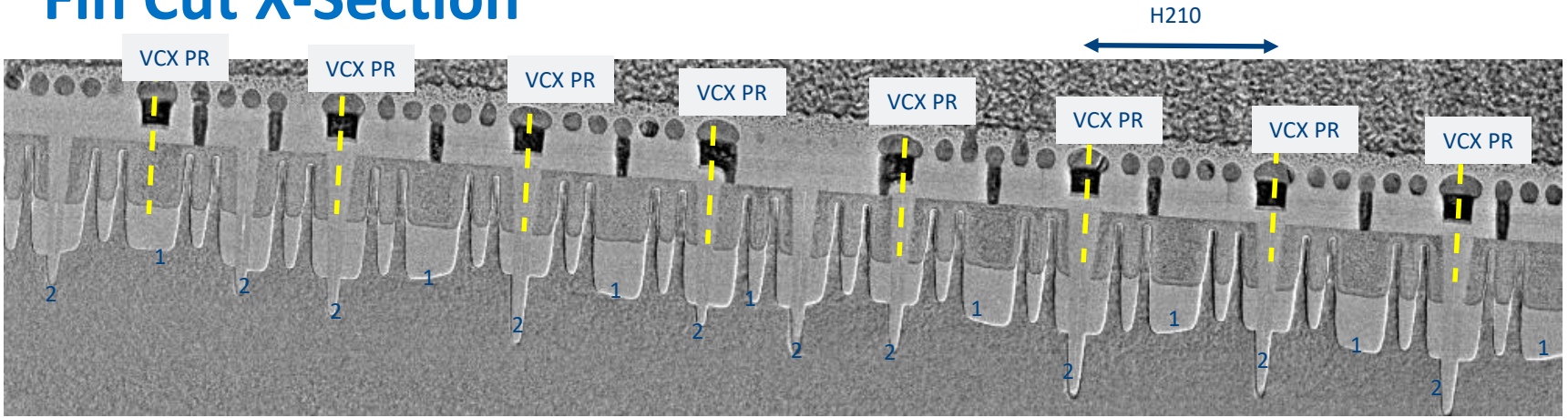


Template based fin patterning at 28 nm pitch (SAQP)

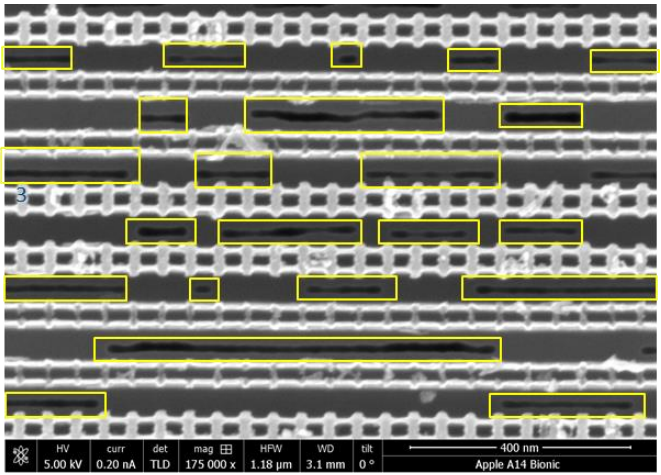
Fin templates used rather than grating (same as TSMC 7 nm)

Within standard cell area both N and P fins are unbroken all the way

Fin Cut X-Section

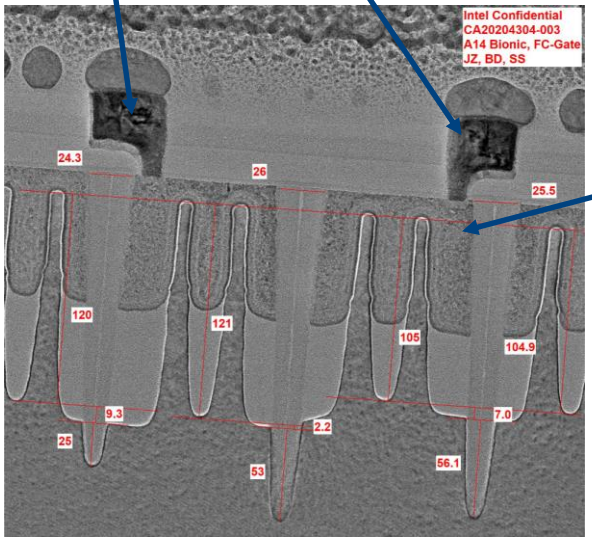


1) Only active fins patterned, no fin removal
2) MG cut formed. Non-uniform etch depth due to etch bias caused by metal gate cut density
3) Deep gauges formed by the MG cut are sometimes off centered. This is due to intentional alignment of VCX and M0



Fin Cut X-section

Gate Tie Down to Supply/Ground

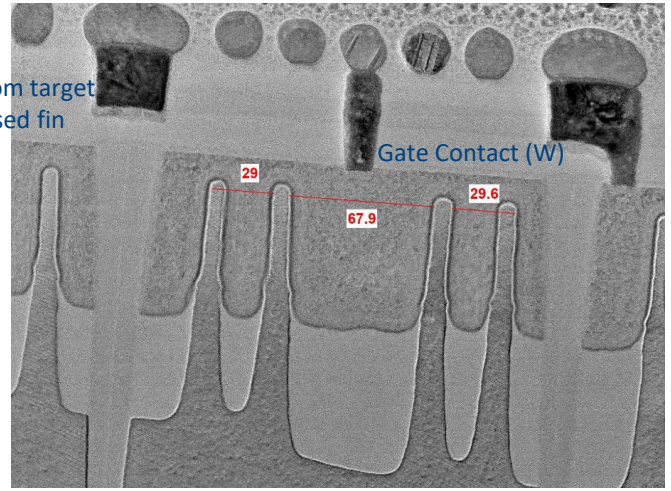


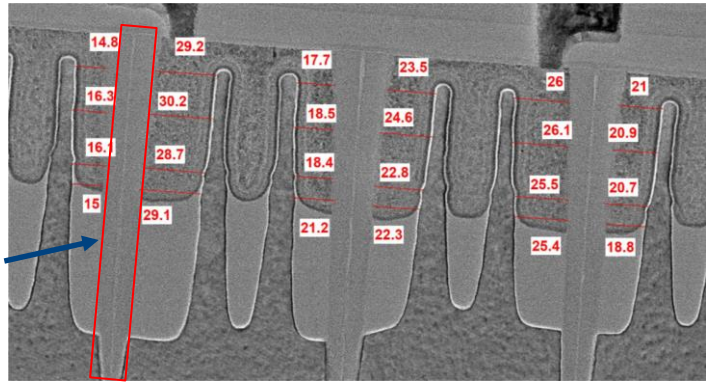
Cut was done after metal gate stack formation

Plug is nitride with oxide in the seam

P to N separation is 68 nm

Fin pitch deviation from target seen for template-based fin patterning

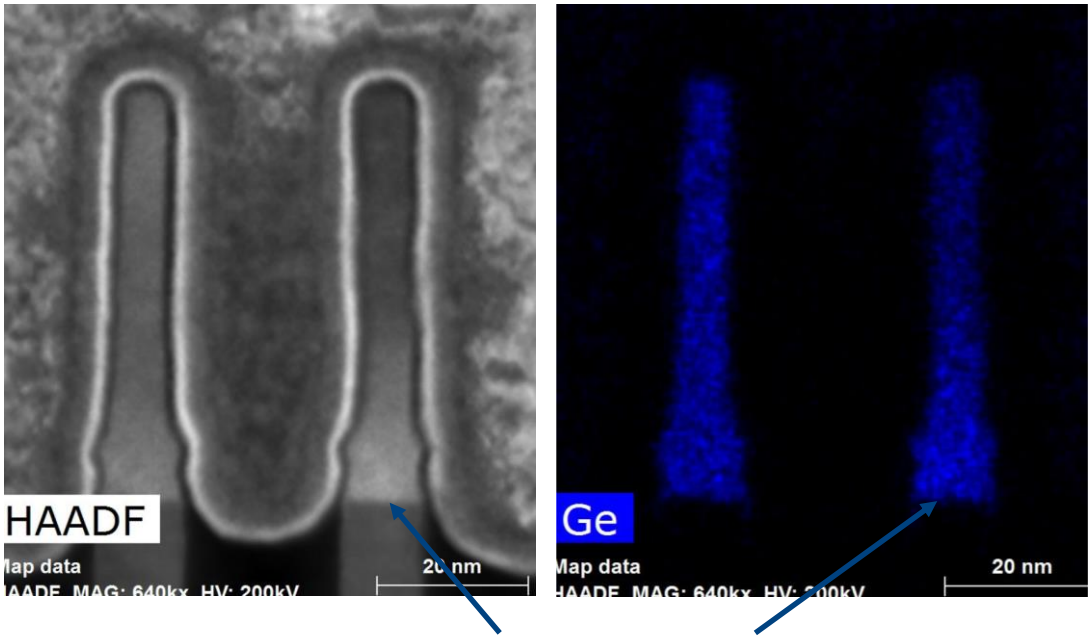


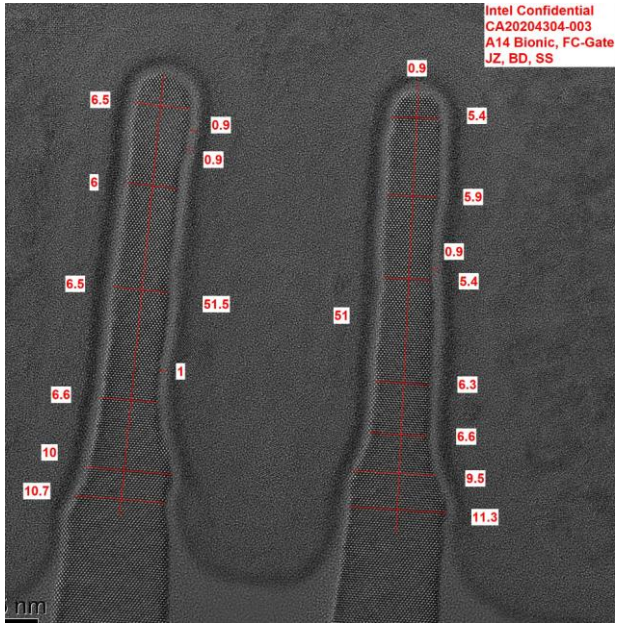


Variation in MGC to accommodate gate contact landing for different M0 hit points. Could be that MG cut mask is EUV SP

Fin Cut X-section

PMOS SiGe Channel



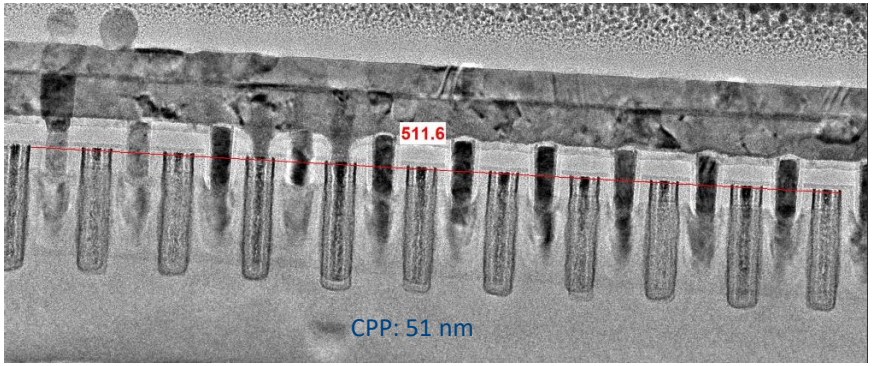


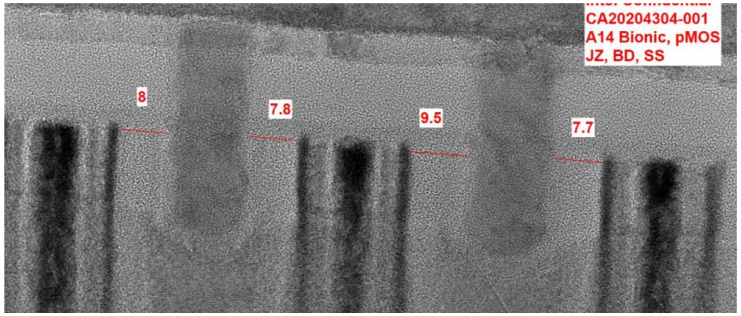
Ge profile makes it looks like an upfront SiGe process

~55 nm high fin with almost uniform profile with width of 6 nm

Gate Cut X-section

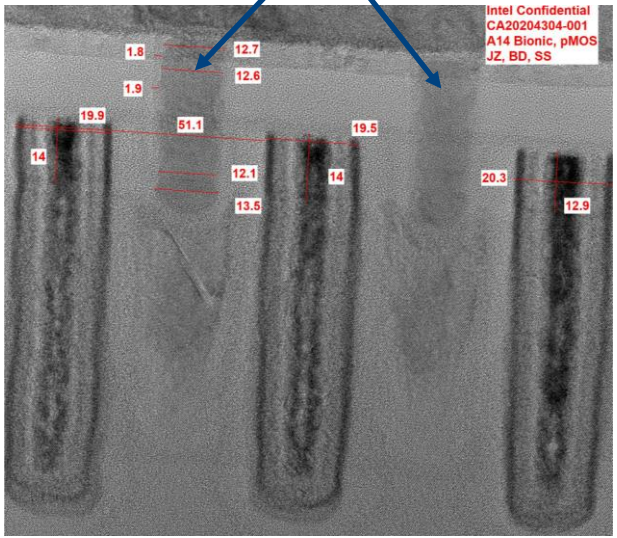
No GILA, TILA.
Space between TCN and gate is around ~8.5



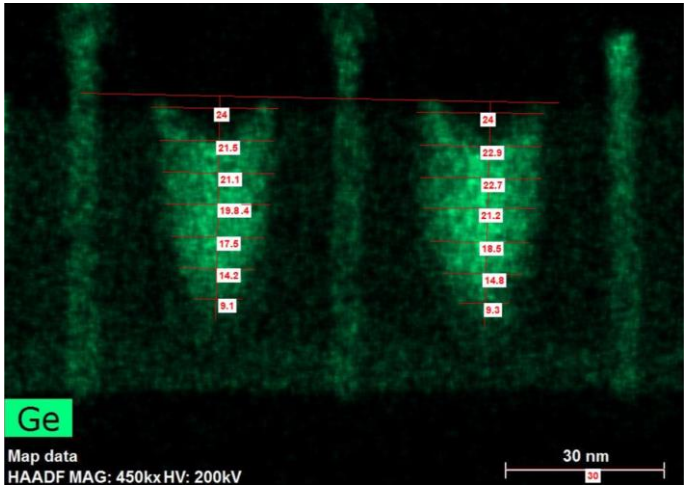


Co TCN: 12-13 nm

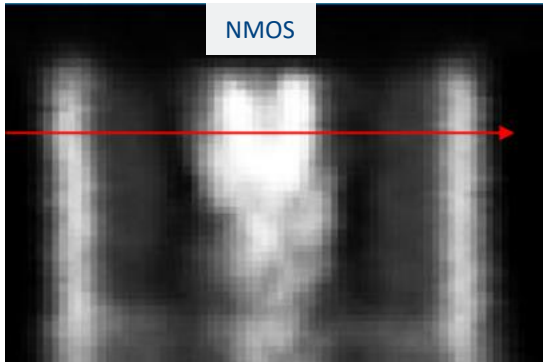
SiGe S/D depth more pulled back from channel depth

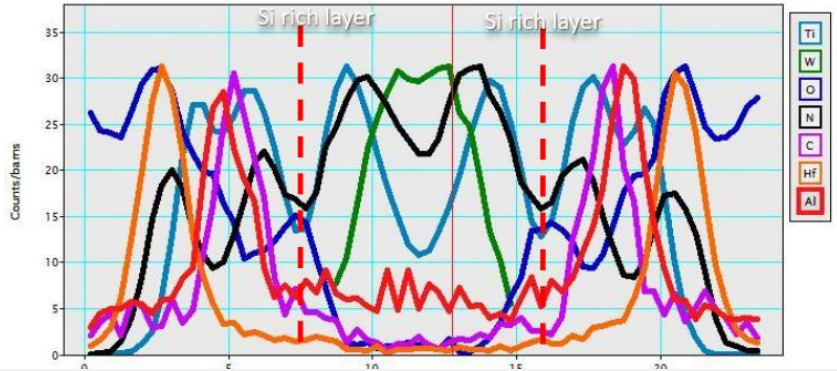


Gate CD ~18-20 nm
MG height: ~14-15 nm

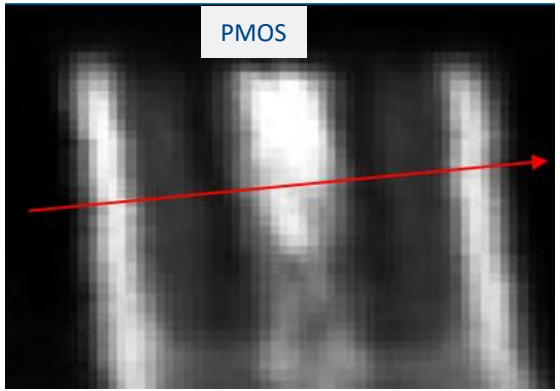


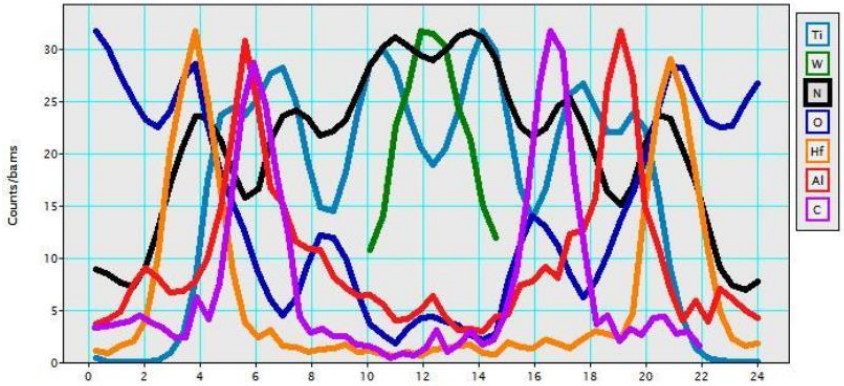
Metal Gate Stack (EELS) – Standard Cell





NMOS: TL/ Dipole/ High K/(with N?) /Al, Ti, N/Al, Ti deficient, C, N deficient/Al, Ti, C, N/Ti, N, O, Si/TiN/W

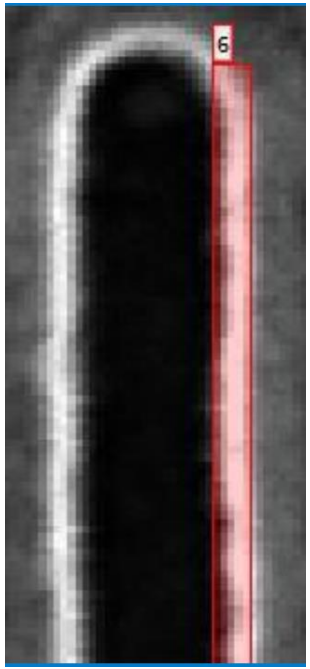


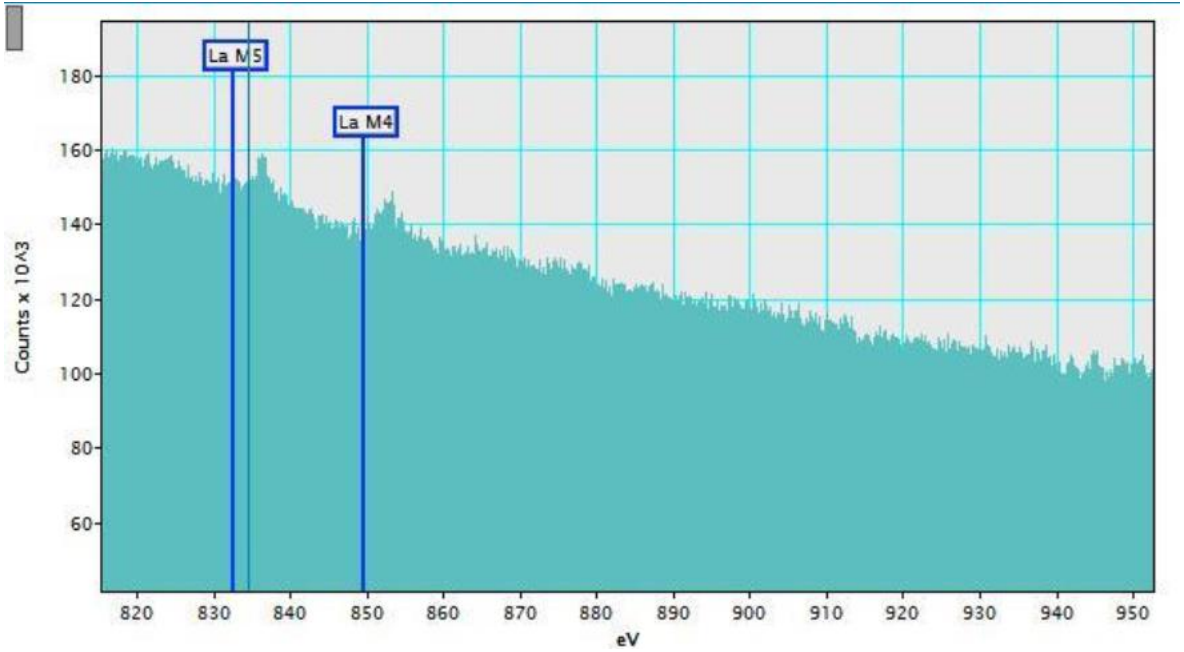


PMOS: TL/High K/(with N?) /Al, Ti, N/Al, Ti deficient, C, N deficient/Al, Ti, C, N/Ti, N, O, Si/TiN/W

J. Zhang

La Dipole in NMOS in Logic





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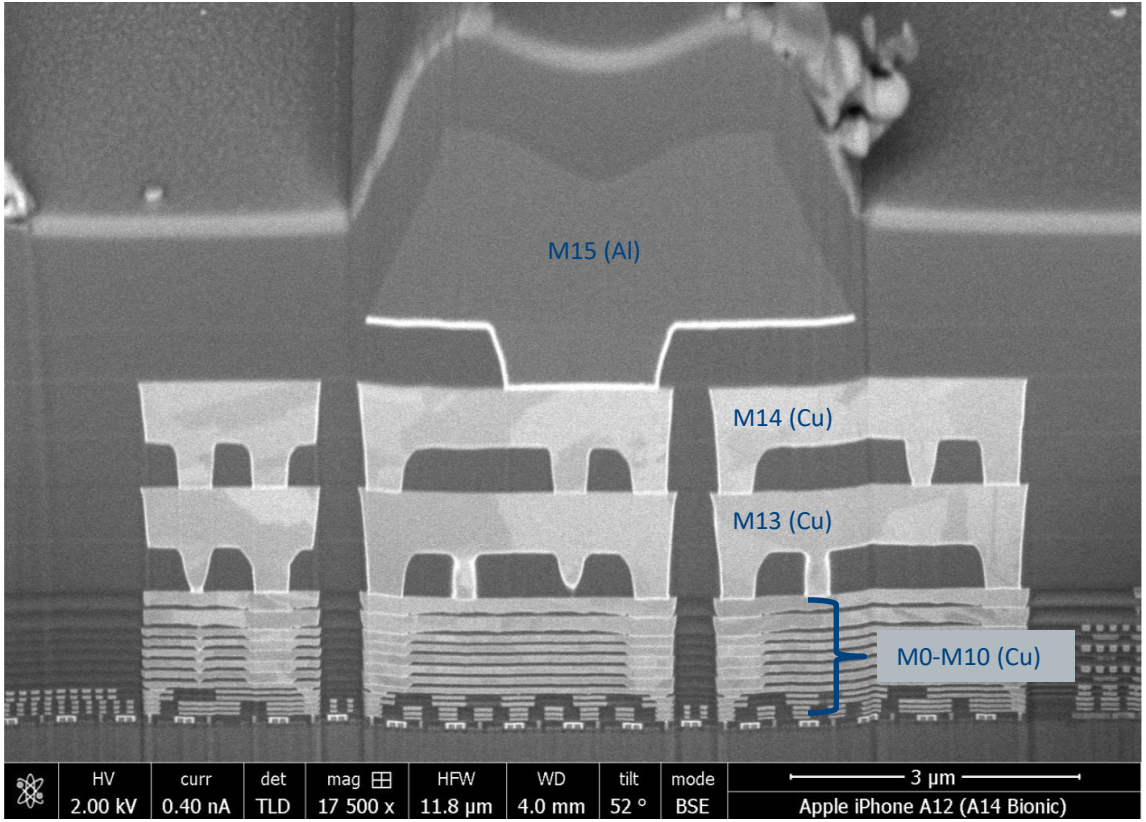
Metal Stack



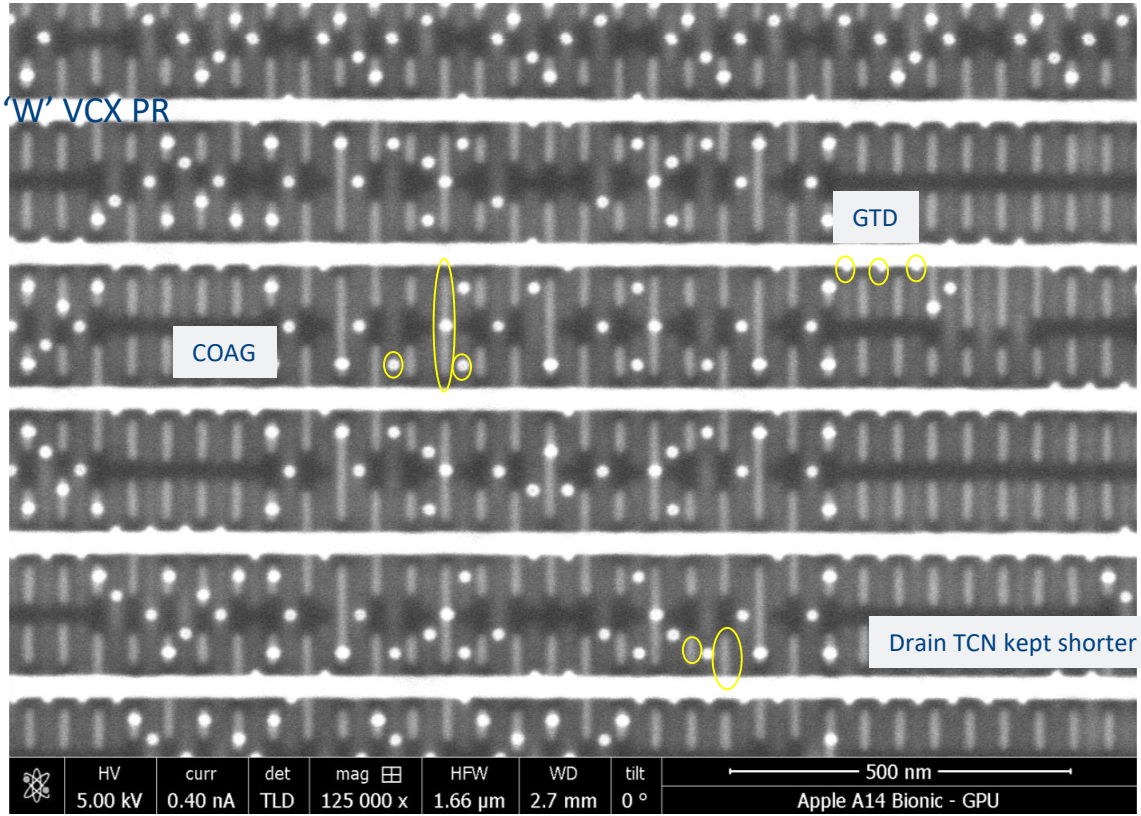
- Total of 15 Cu + 1 Al (RDL) Metal layers

- M0: 28 nm
- M1: 34 nm
- M2: 35 nm
- M3: 42 nm
- M4: 42 nm
- M5: 78 nm
- M6: 78 nm
- M7: 78 nm
- M8: TBD
- M9: TBD
- M10: TBD
- M11: TBD
- M12: TBD
- M13: TBD
- M14: TBD
- M15: TBD

**Pitches are measured in GPU

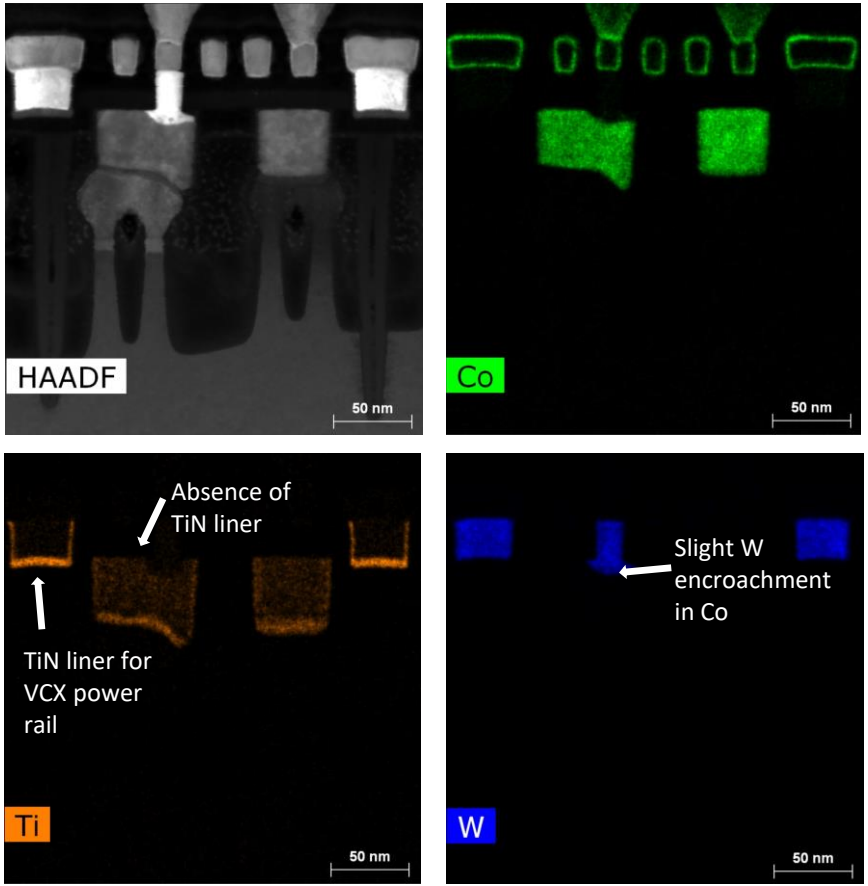
M13-M14 are used for power delivery only

Poly/Contact



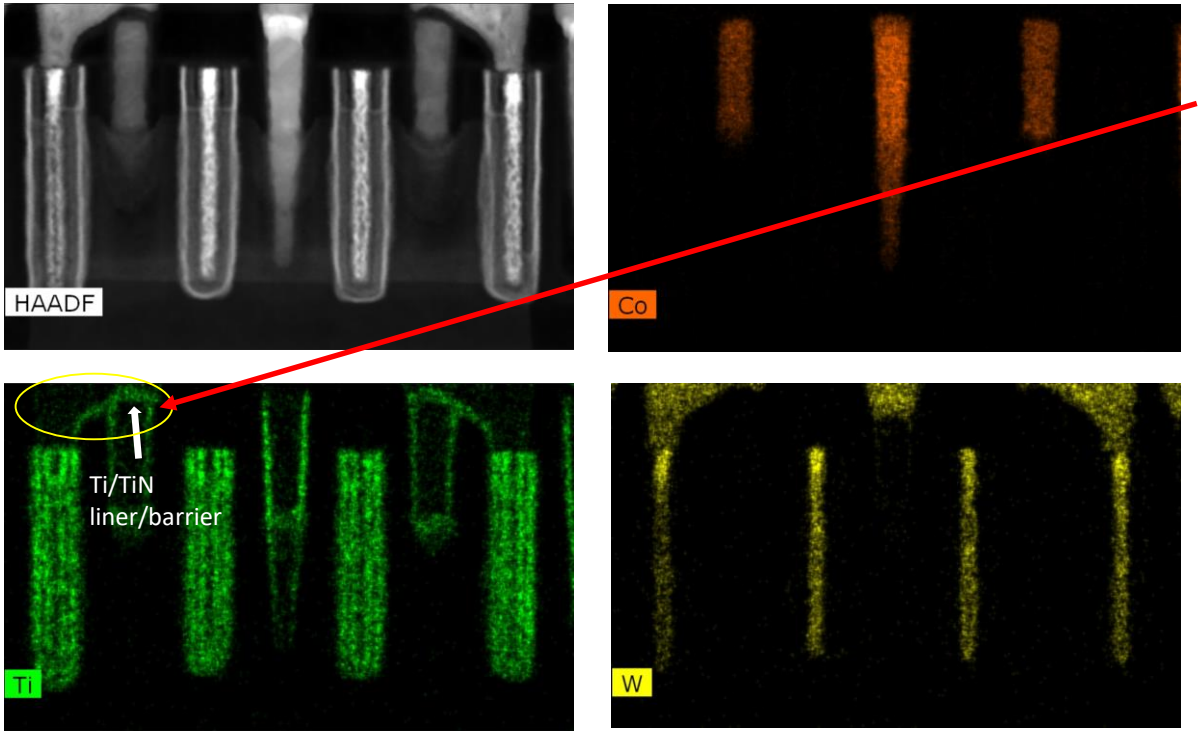
Drain TCN kept shorter than source for cap benefit

MOL: Standard Cell



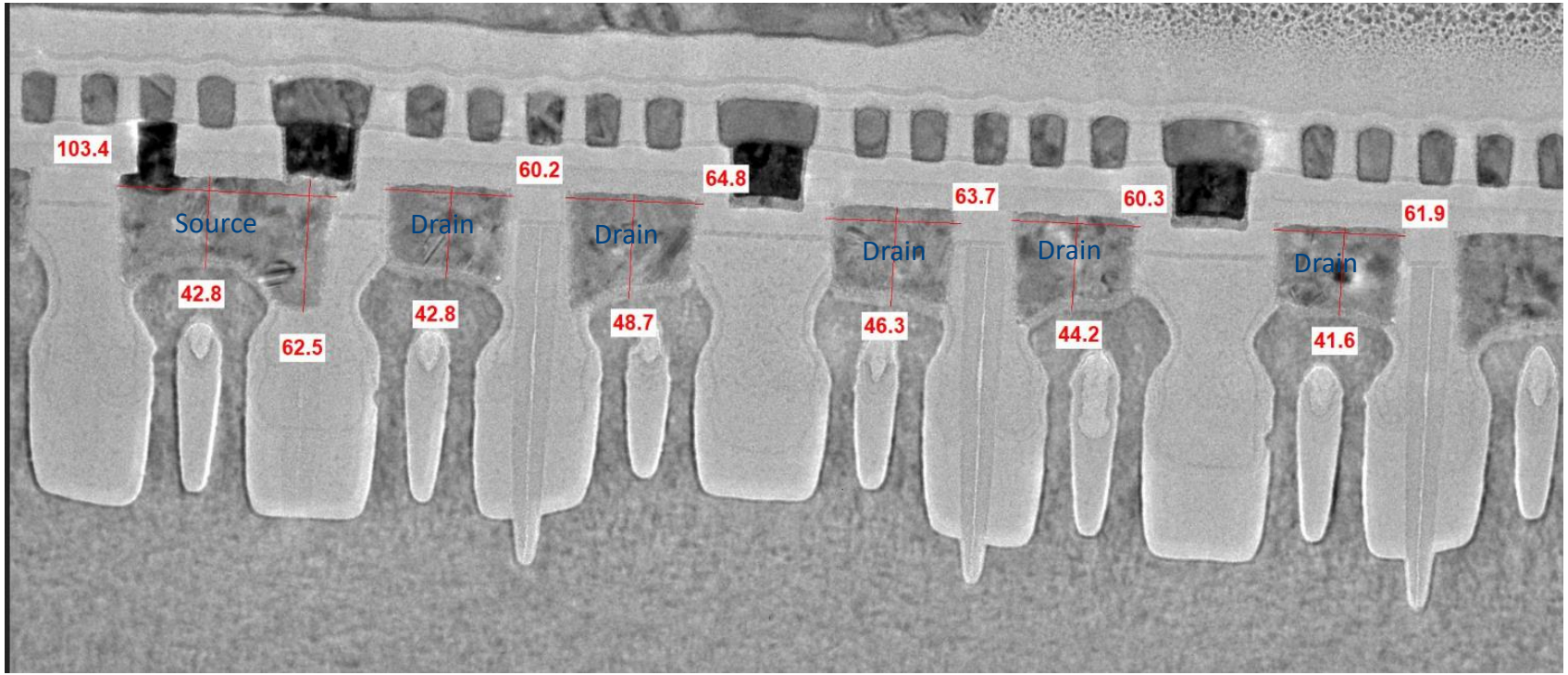
- VCT shows liner/barrier less W on Co TCN
- This indicates selective W deposition seen before in TSMC 7 nm 2nd generation process
- Traditional W deposition using conventional CVD entails having a Ti/TiN liner/barrier with a W nucleation layer, since W cannot grow directly on TiN
- Selective W deposition process involves liner/barrier less CVD deposition where the CVD tool employs atomic-level treatments to the wafer to remove all impurities and then makes tungsten atoms to selectively go to the bottom of the via therefore filling it from the bottom

MOL: SRAM Bit Cell

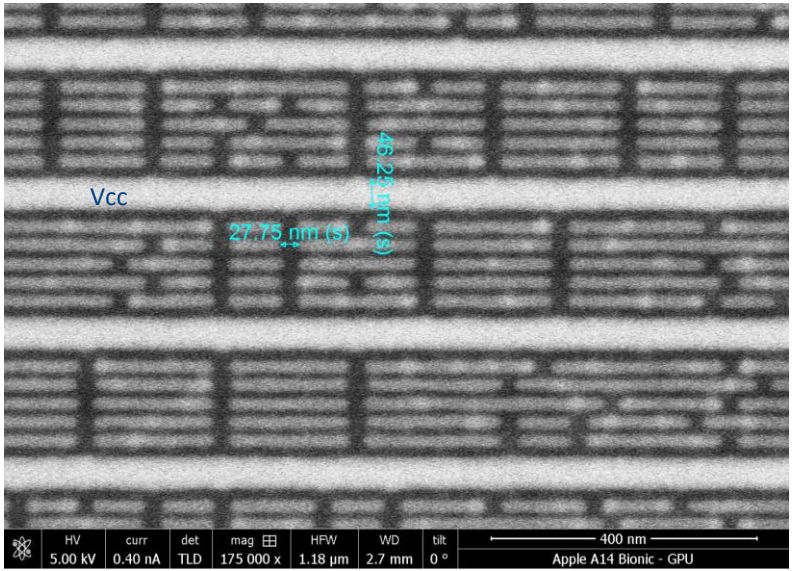


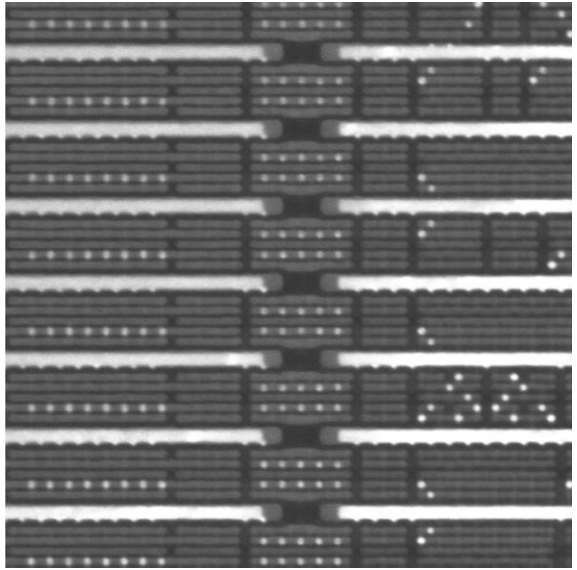
The feedback connection for the latch in SRAM bit cell shows the gate and drain tie down done with W with Ti/TiN liner/barrier. Which means that this W is a conventional CVD deposition

TCN Lengths in Standard Cell



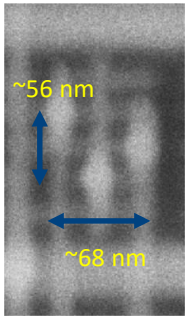
Metal Layers



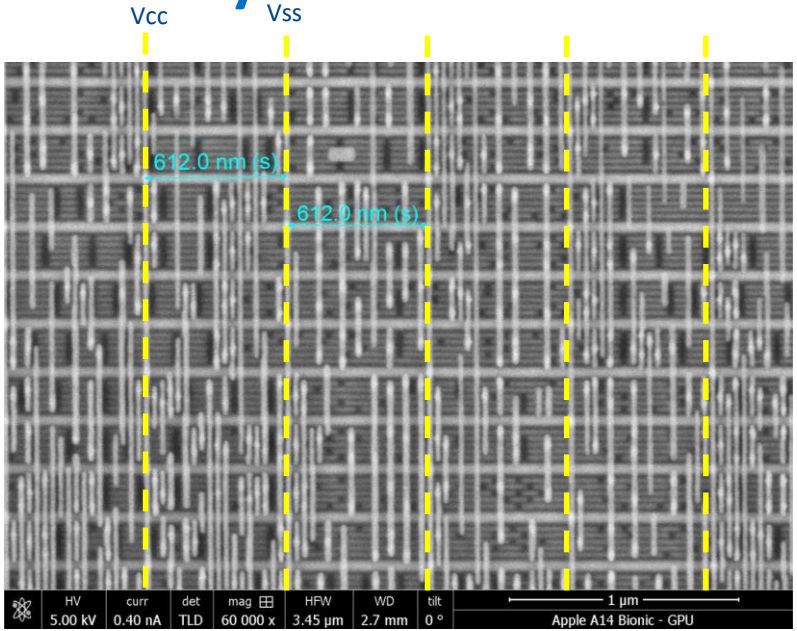


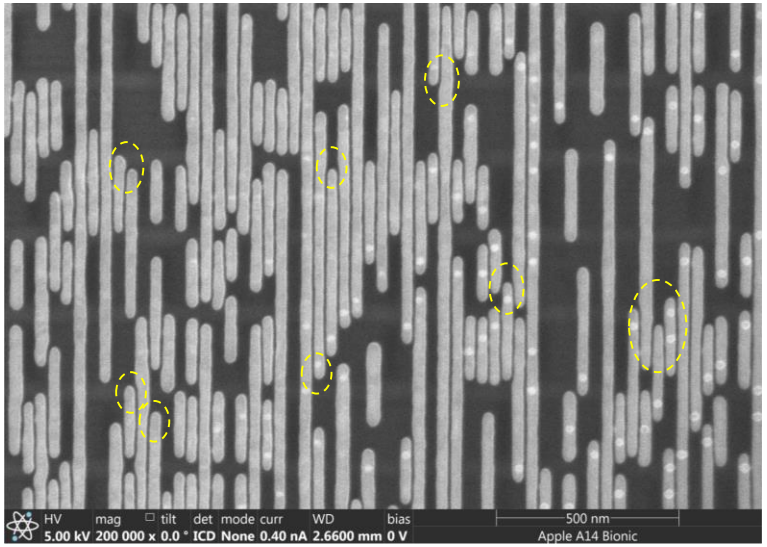
M0: 28 nm. EUV SALELE
At least one plug mask
Via0 is done using EUV

Via0

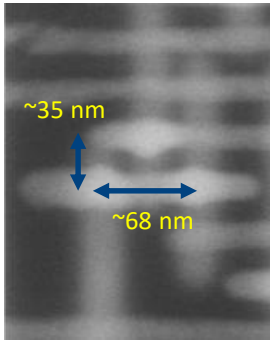


Metal Layers



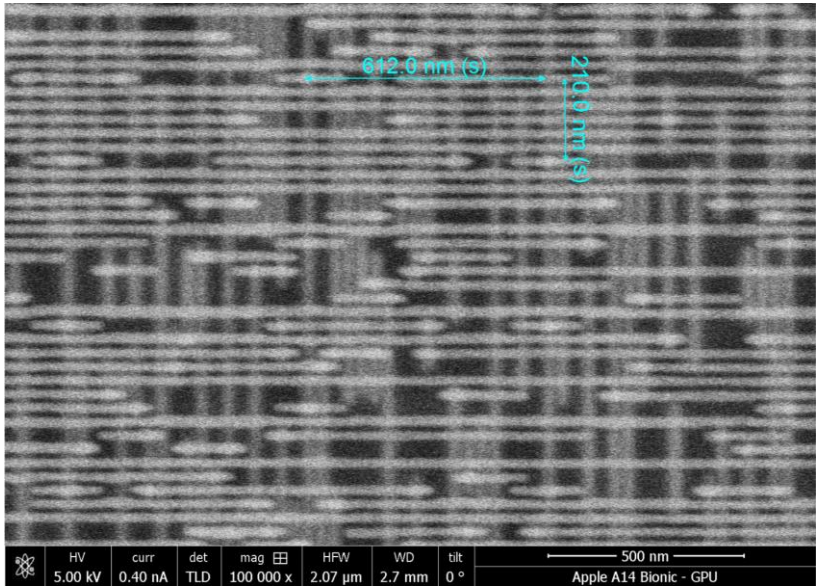


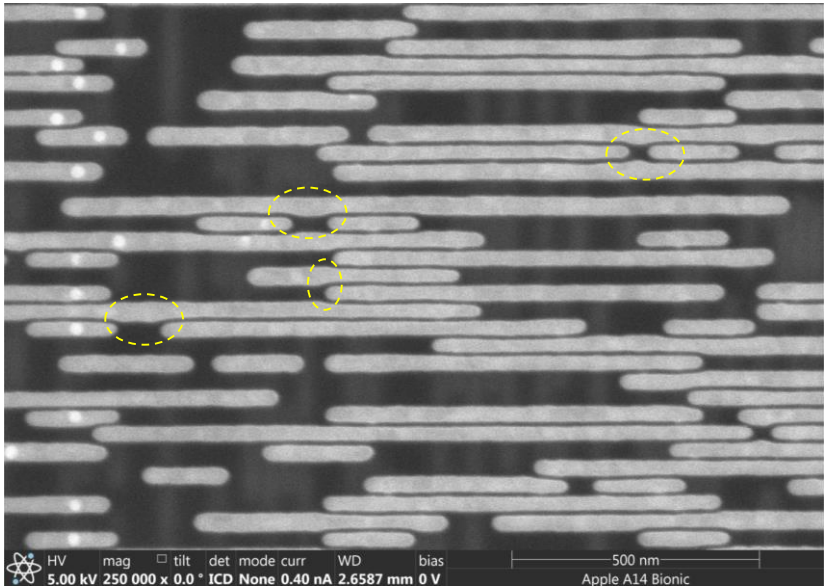
Via1



M1: Vcc PR – Vss PR is 612 nm
18 tracks fit at 612 nm span -> 34 nm pitch
EUV (SALELE) with no plug masks
Via1 could be EUV SP

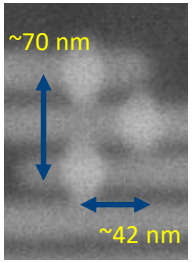
Metal Layers



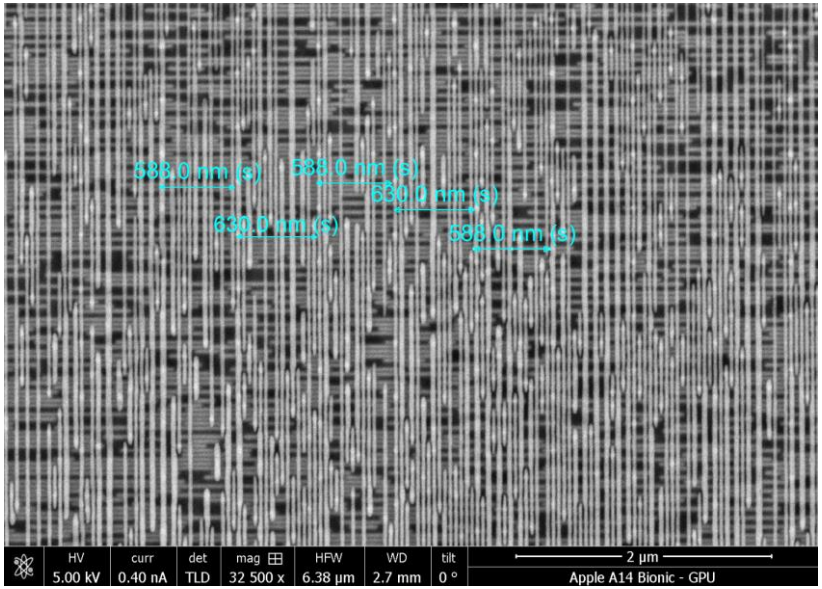


M2: 35 nm
EUV SALELE pattern with no plug masks
Via2 could be EUV SP

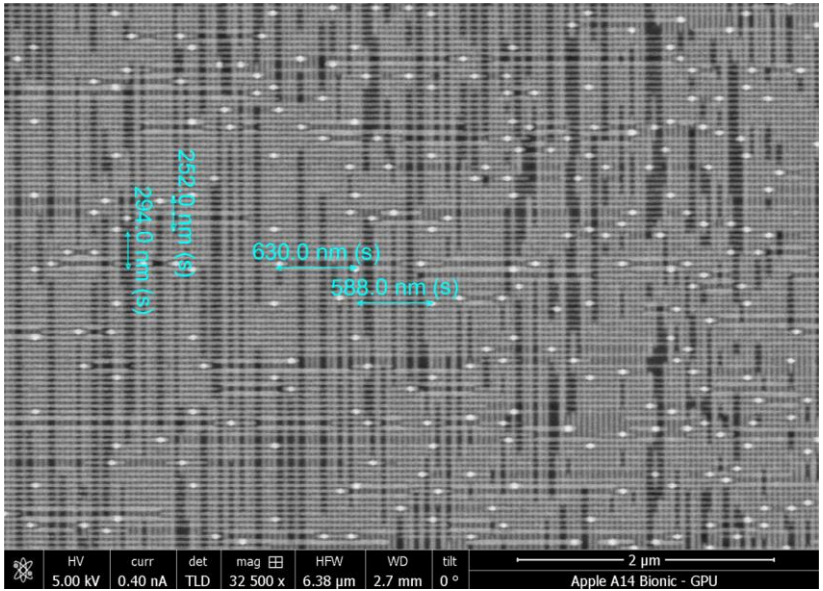
Via1



Metal Layers

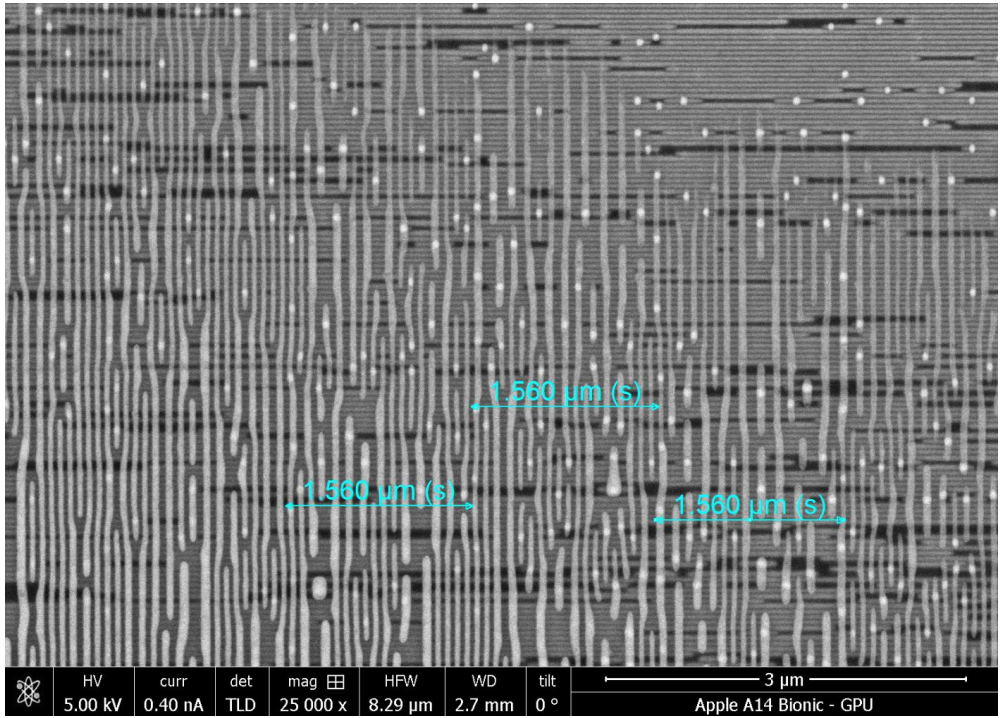


M3: 42 nm. 193i SALELE with no plug masks
Total of 29 tracks fitted within 1218 nm Vss-Vss span



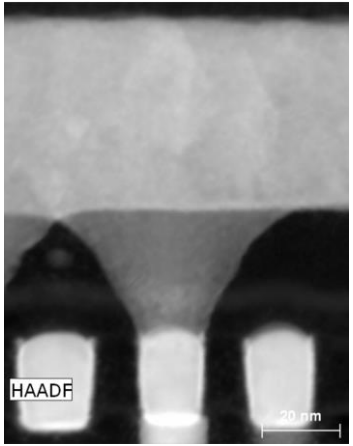
M4: 42 nm. 193i SALELE pattern with no plug masks

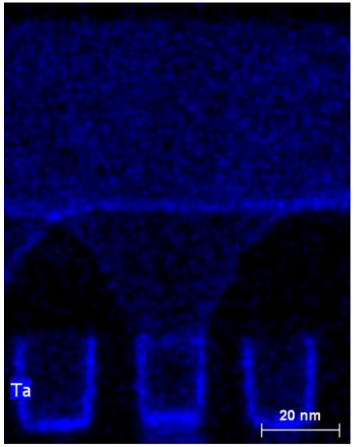
Metal Layers

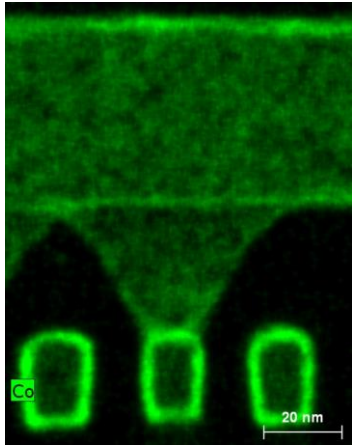


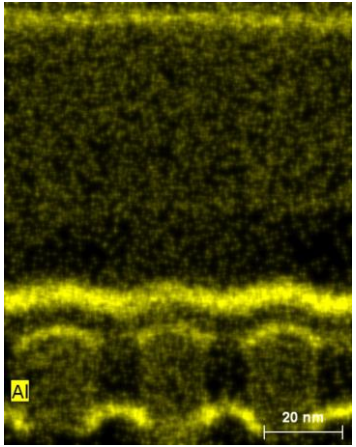
M5: 78 nm. 193i SP (LE) with no plug masks
20 tracks fitted within 1560 Vcc-Vss span

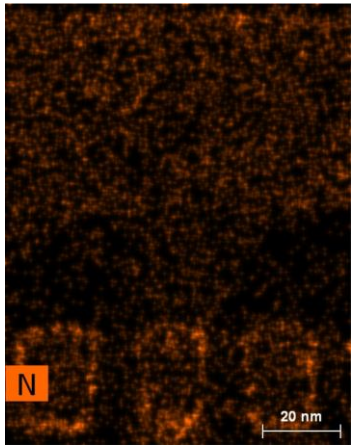
M0 X-section

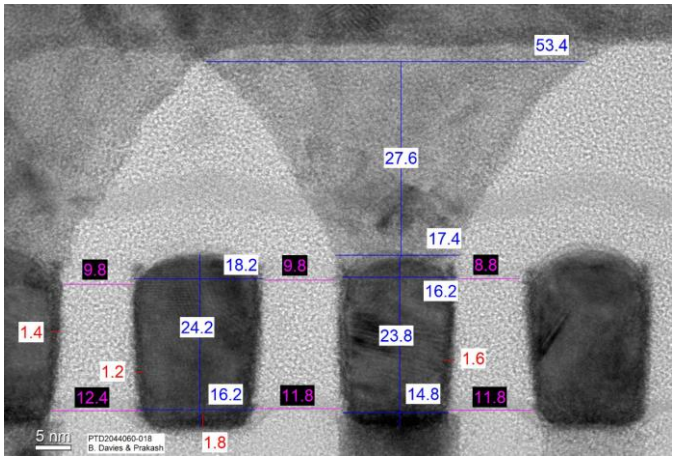








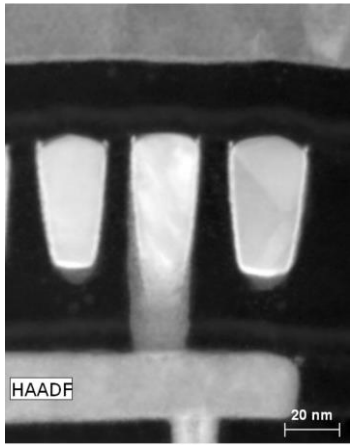


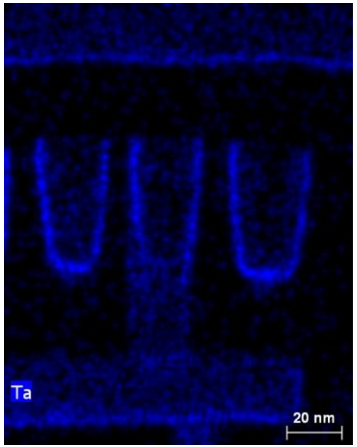


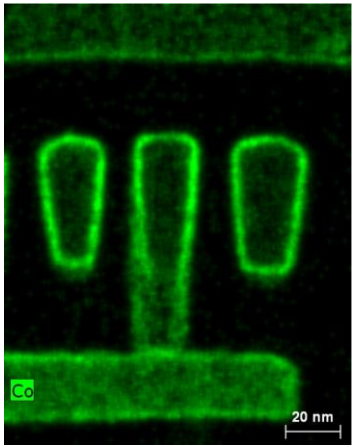
M0:
Height: ~24 nm
Width (Top): 16-18 nm
Width (bottom): 15-16 nm
Sidewall liner/barrier: 1.2-1.6 nm
Bottom liner/barrier: ~1.8 nm
Line space: ~10 nm

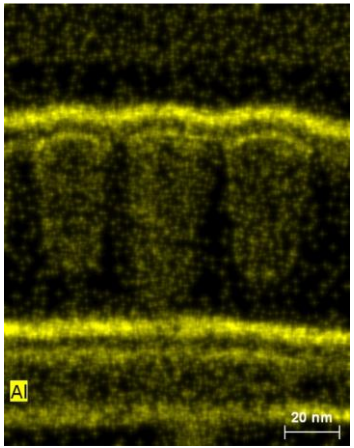
Etch Stop:
AlN+ SiOC + AlxOy

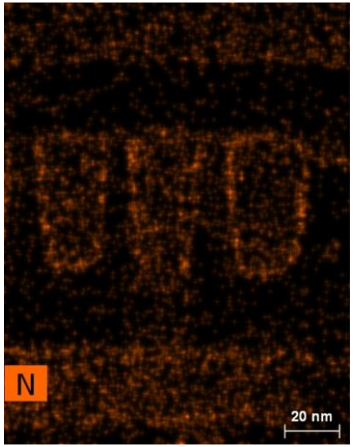
M1 X-section

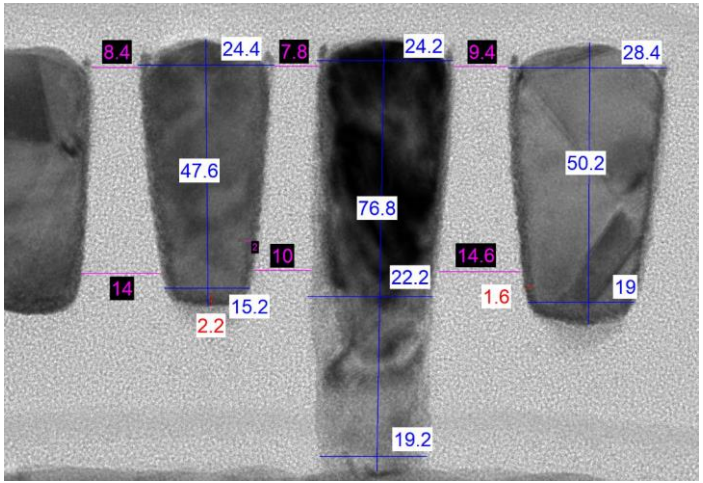








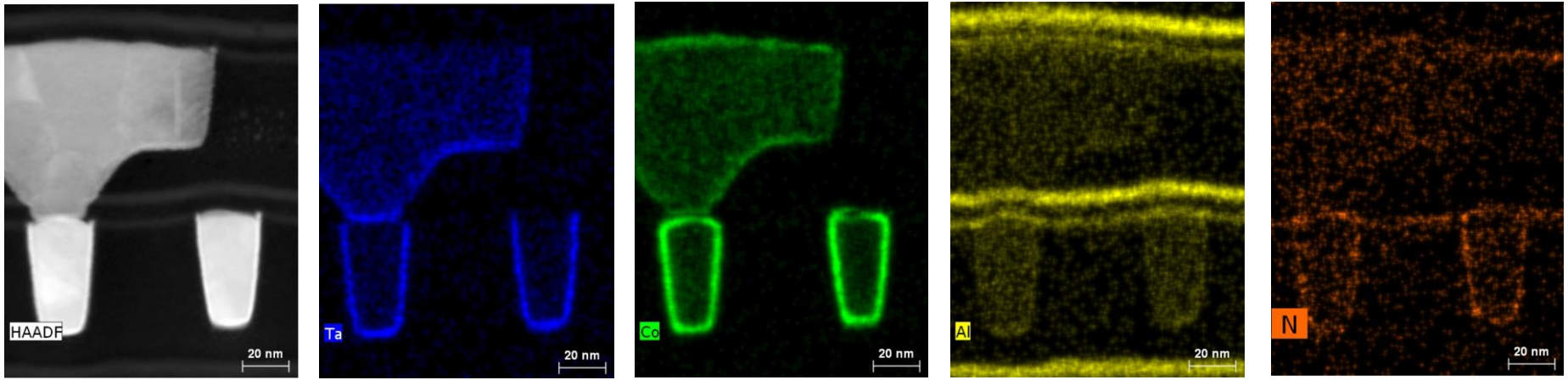


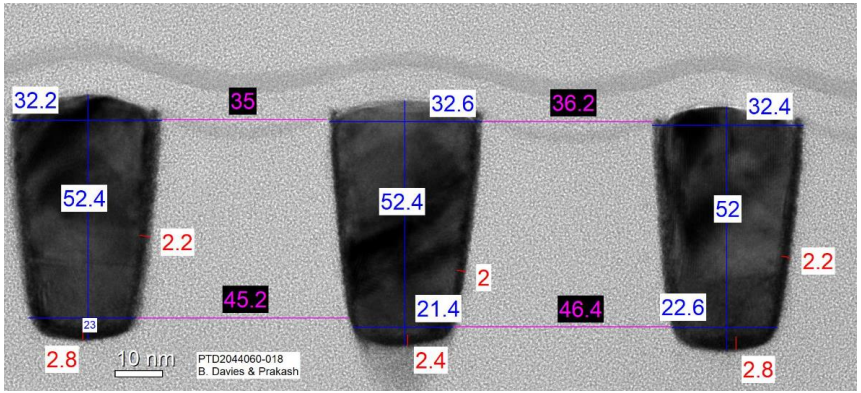


M1:
Height: ~48 nm
Width (Top): 24-28 nm
Width (bottom): 15-19 nm
Sidewall liner/barrier: 1.6-2 nm
Bottom liner/barrier: ~2.2 nm

Etch Stop:
AlN+ SiOC + AlxOy

M2 X-section

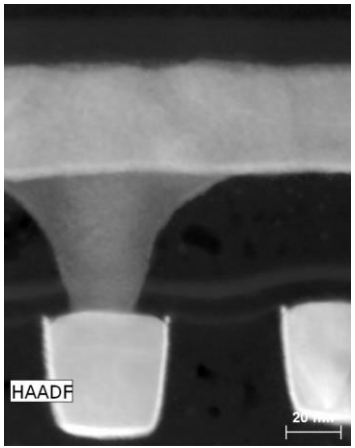


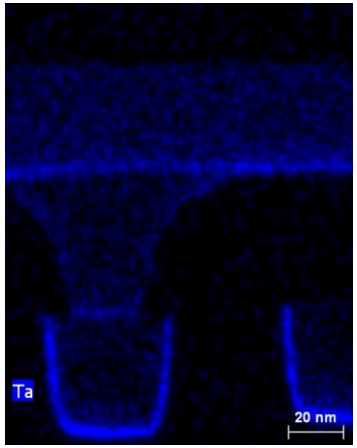


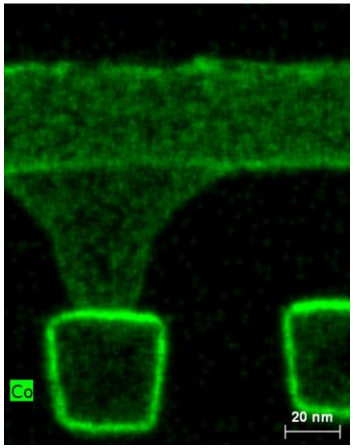
M2:
Height: ~52 nm
Sidewall liner/barrier: 2-2.2 nm
Bottom liner/barrier: ~2.4-2.8 nm

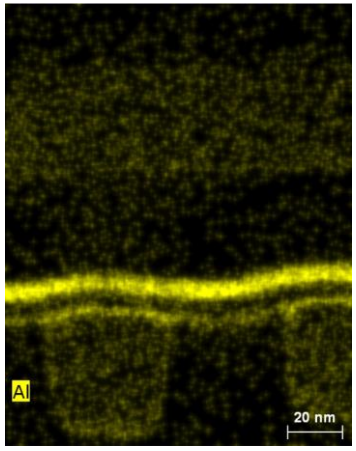
Etch Stop:
AlN+ SiOC + AlxOy

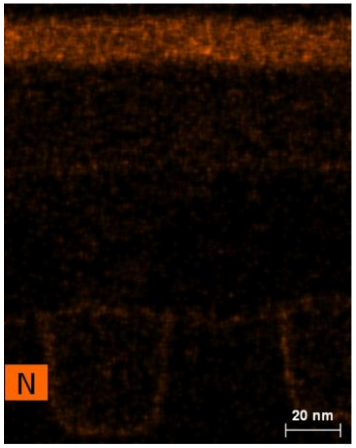
M3 X-section

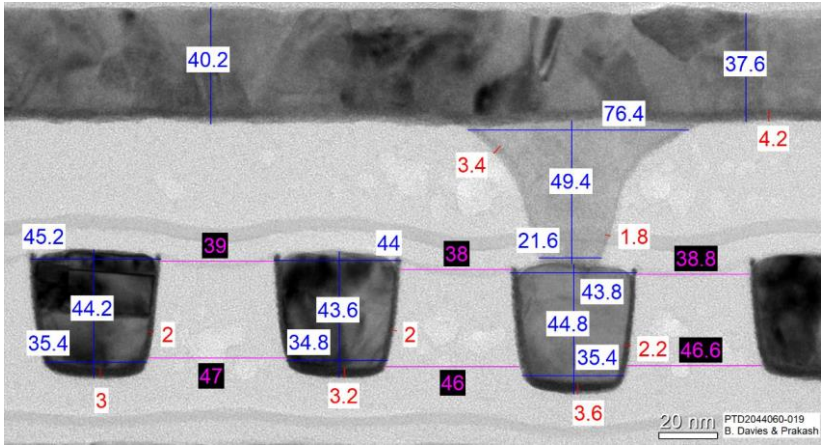








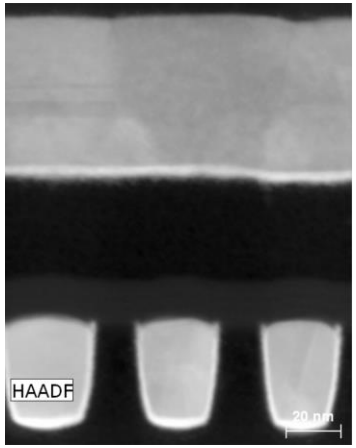


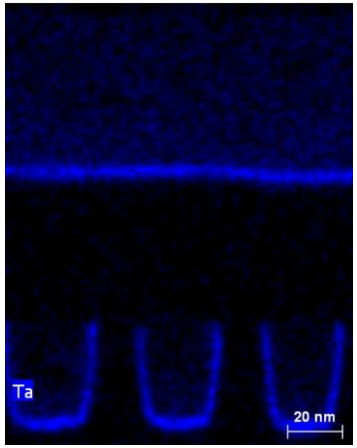


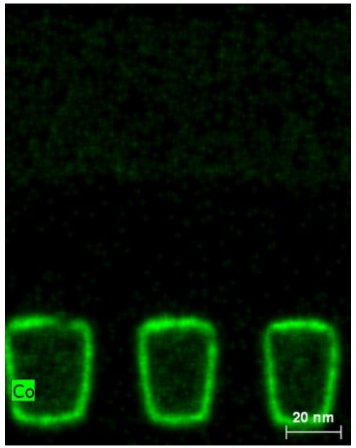
M3:
Height: ~44 nm
Sidewall liner/barrier: 2-2.2 nm
Bottom liner/barrier: ~3-3.6 nm

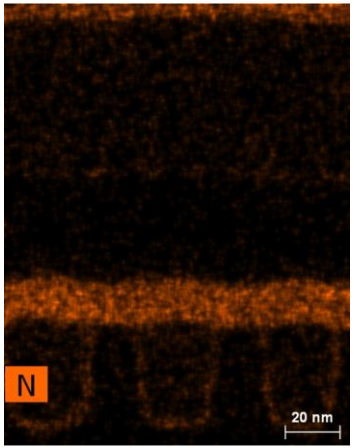
Etch Stop:
AlN+ SiOC + AlOxNy

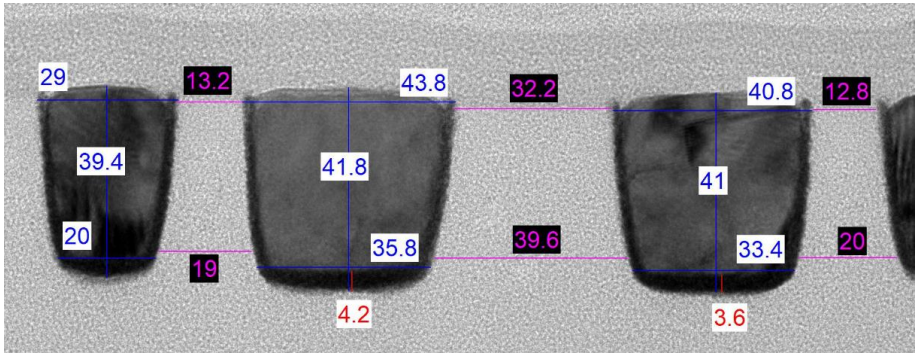
M4 X-section







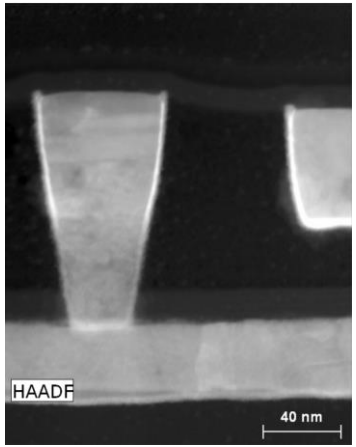


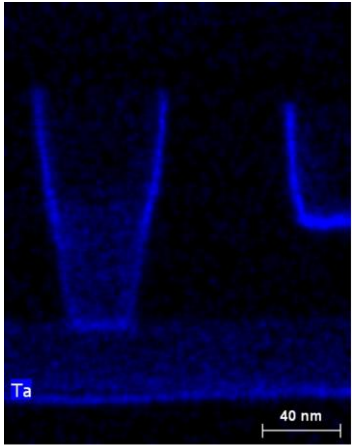


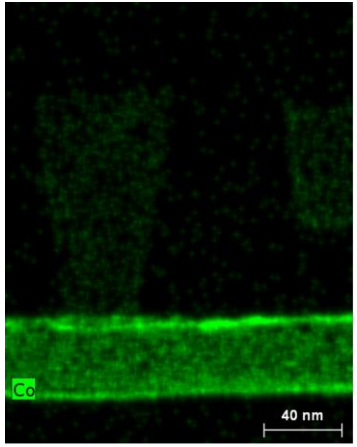
M4:
Height: ~41 nm
Sidewall liner/barrier: 2.6 nm
Bottom liner/barrier: ~3.6–4.2 nm

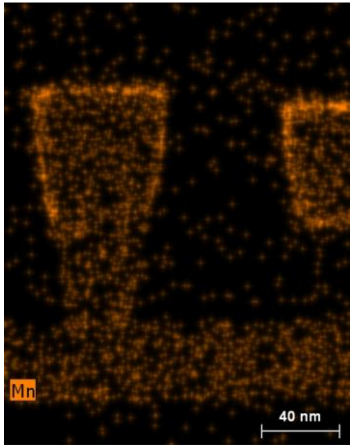
Etch Stop:
SiCN

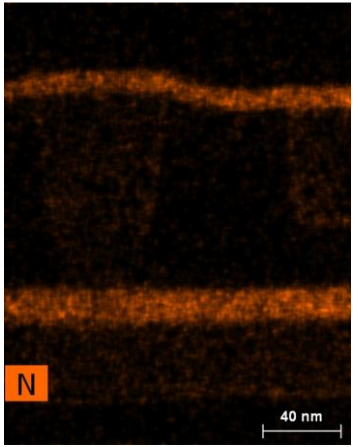
M5 X-section

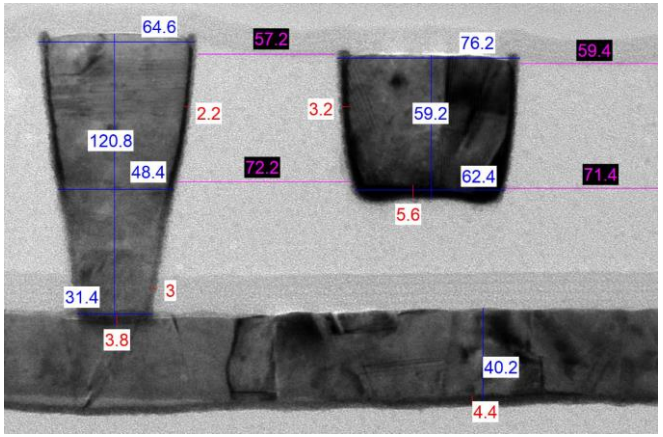












M5:
Height: ~59 nm
Sidewall liner/barrier: ~3 nm
Bottom liner/barrier: 3.4-5.6 nm

Etch Stop:
SiCN

Metal/ILD/ES

T5	Metal	Liner	Cap	ILD	ES below (top to bottom)	Pitch (nm)	Mx Height (nm)	Vx-1 Height (nm)
Via contact	W			SiOx				VCG – 47 VCT/VCR - 32
M0	Cu, SD	TaN+Co	Co	SiOC	AlOx	28	24	
M1	Cu, DD	TaN+Co	Co	SiOC	AlOx/SiOC/AlON	34	48	29
M2	Cu, DD	TaN+Co	Co	SiOC	AlOx/SiOC/AlON	35	52	28
M3	Cu, DD	TaN+Co	Co	SiOC	AlOx/SiOC/AlON	42	44	28
M4	Cu, DD	TaN+Co	Co	SiOC	AlOx/SiOC/AlON	42	41	42
M5	Cu, DD	TaN	CuMn	SiOC	SiN	78	59	53
M6	Cu, DD	TaN	CuMn	SiOC/SiOx	SiN	78		65

Interconnect/ILD/ES are mostly like N7.

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Metal Line CDs

T5	Height (nm)	Top Width (nm)	Bottom Width (nm)	Sidewall Barrier (nm)	Bottom Barrier (nm)	Aspect ratio
M0	24	18	16	1.5	2	1.4
M1	48	24	15	1.5	2	2.5
M2*	52	32	22	2	2.5	1.9
M3*	44	44	35	2	3	1.1
M4*	41	29	20	2	4	1.7

T7	Height (nm)	Top Width (nm)	Bottom Width (nm)	Sidewall Barrier (nm)	Bottom Barrier (nm)	Aspect ratio
M0	40	27	24	2	3.5	1.5
M1	63	38	26	2	3	1.9
M2	48	28	21	2	3	1.9
M3	44	27	19	2	3	1.9
M4	70	50	34	4	5	1.7

* Not from minimum pitch and CD line. Work ongoing

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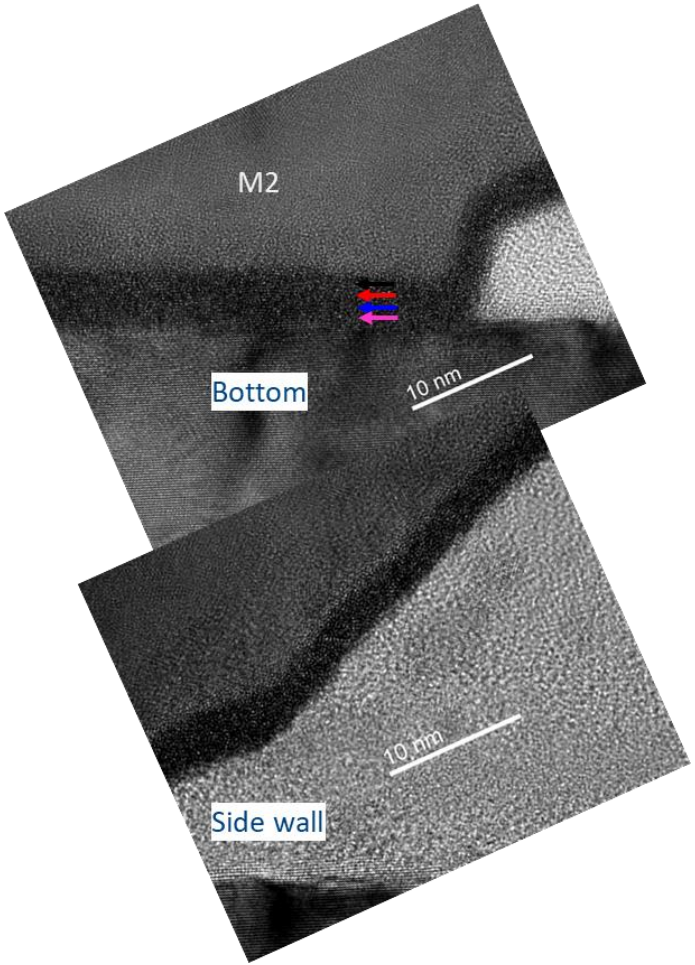
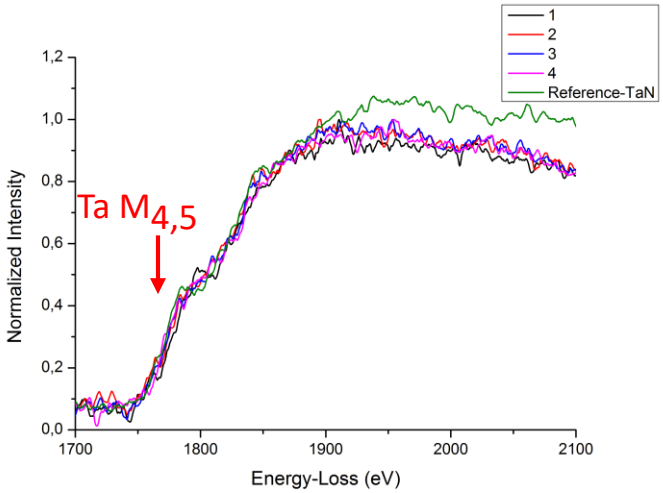
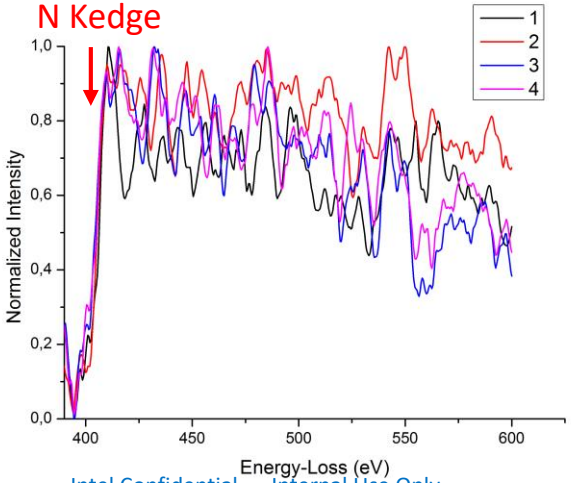
EELS of Barrier







Weak N signal is detected in barrier.

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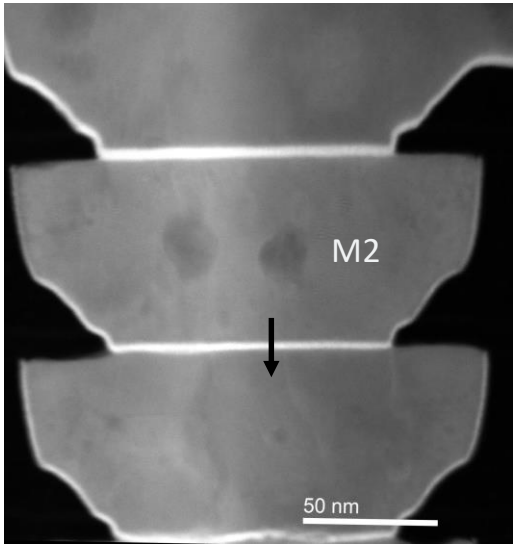
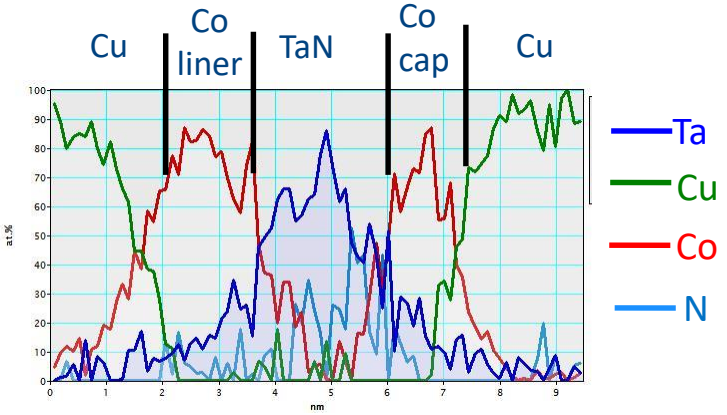
EELS Profile





Barrier is slightly thicker at bottom than sidewall.

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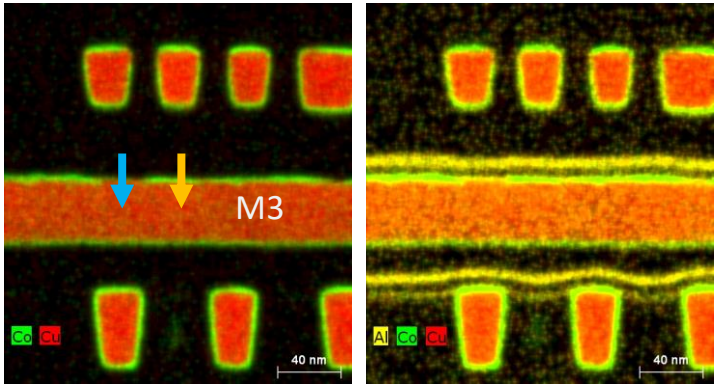
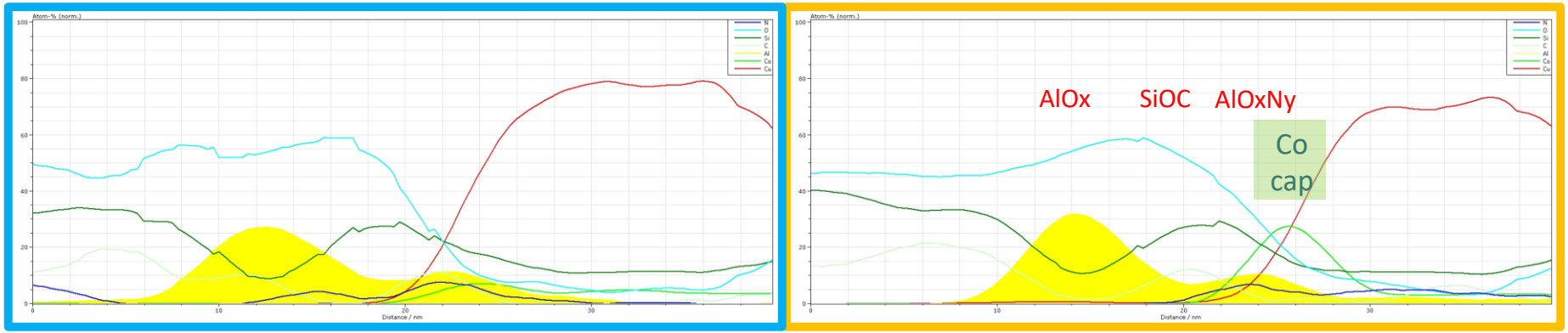
Co Cap Patchiness

Co cap is not uniform across the line



Gap in Co cap



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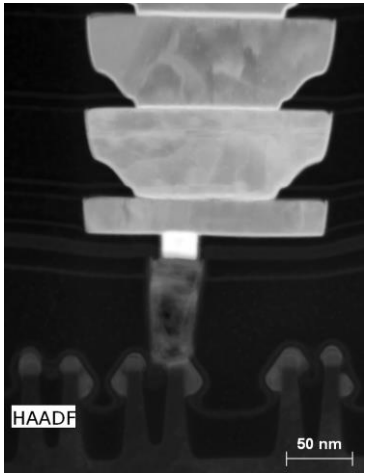
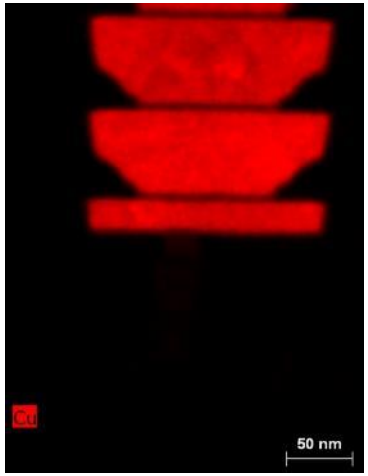
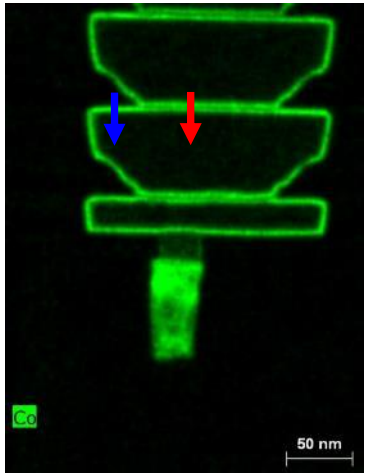
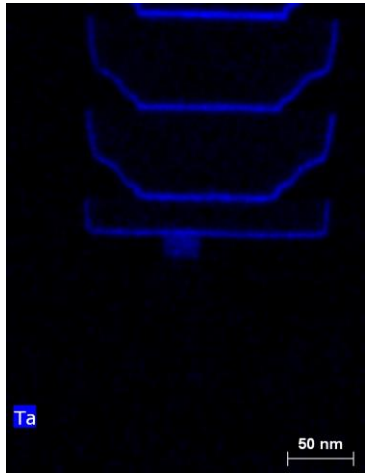
Co Thickness

Guard Ring
Hermetic Seal
Stack

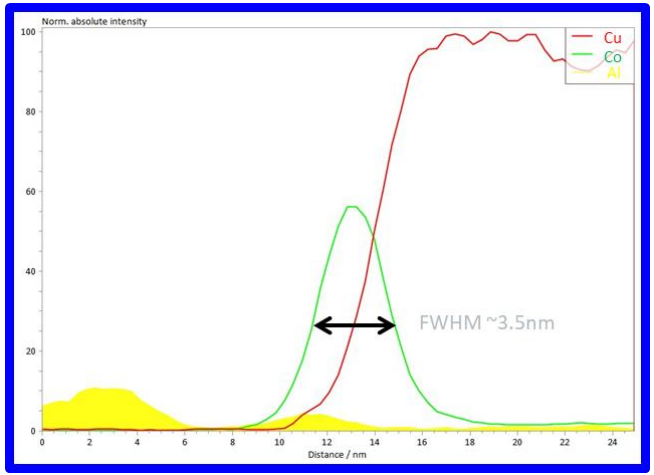


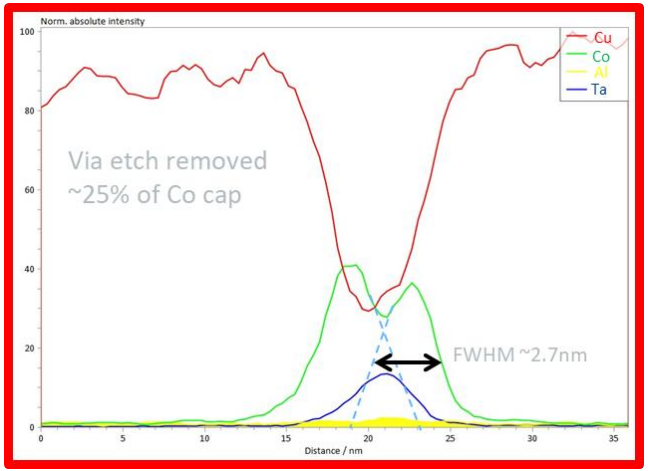






Via etch removed
~25% of Co cap from
the line below.





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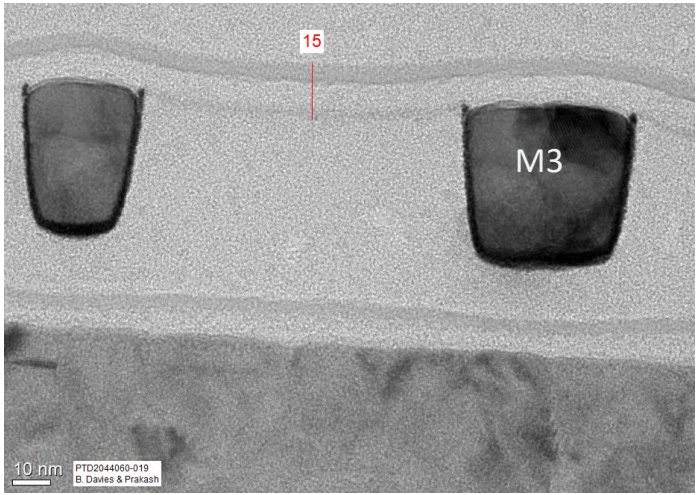
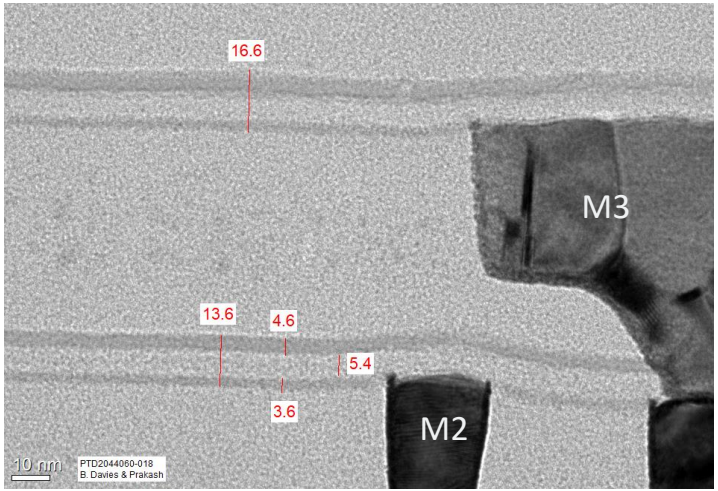
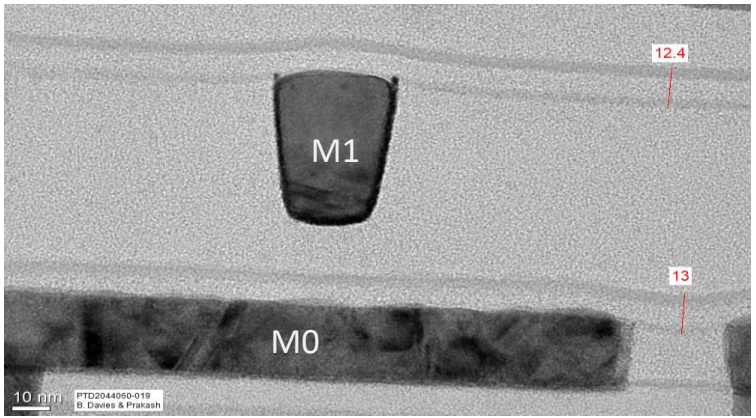
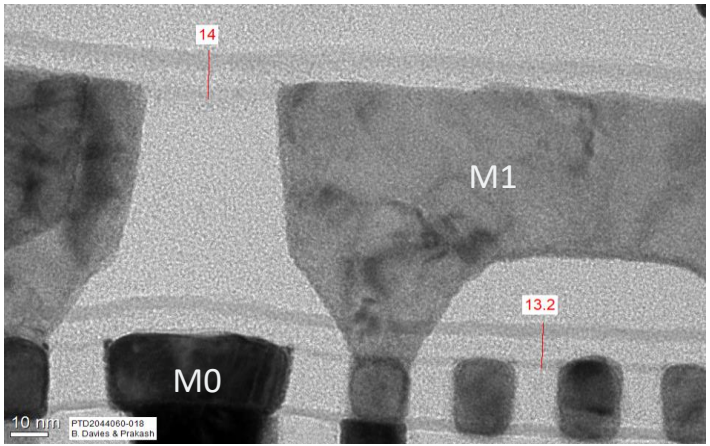
Tri-layer ES

Slightly thicker top AlOx in upper layers than lower layers









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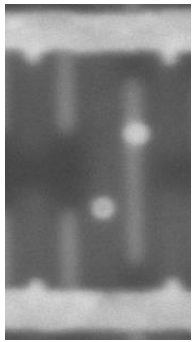
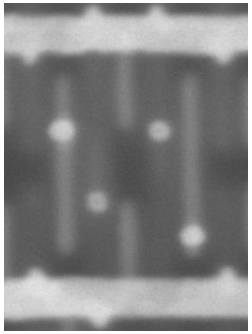
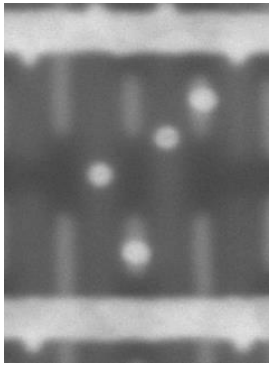
Standard Cells



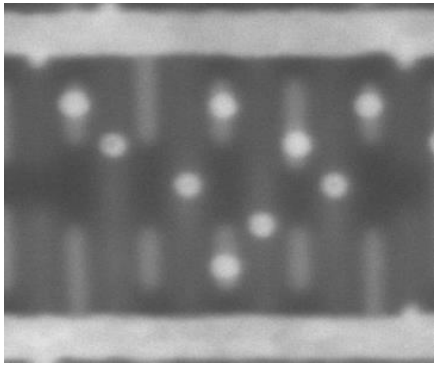
INV (2PP)



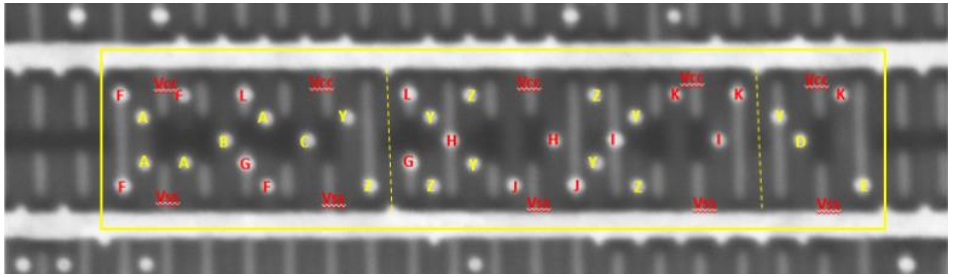
BUF (3PP)



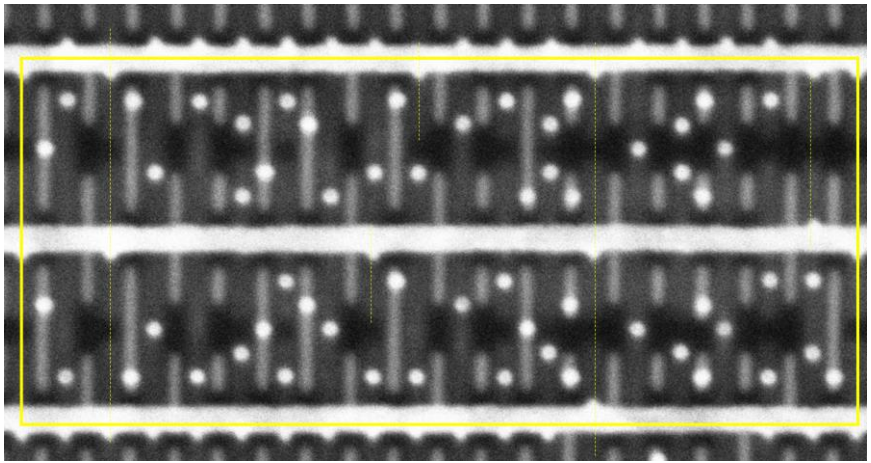
NAND/NOR (3PP)



AOI/OAI (5PP)



SFF (19PP, 32 Tx)



2-bit SFF (19PP, 60 Tx)

Standard Cell Density

H240

Product	**A12 Bionic**
Foundry	**TSMC 7**
Track Height	6
CPP (nm)	57
MxP	40
Utilization	0.75
IP (Theoretical)	GPU

Cell Type	Gate Count NAND2 eq.	Cell Usage (%)	CPP Count	Gate Density (MG/mm2)	Cell Area (um2)
AOI22	2	12.5	6	24.36647	0.08208
OAI22	2	12.5	6	24.36647	0.08208
INV	0.5	12.5	4	9.137427	0.05472
BUF	1	12.5	4	18.27485	0.05472
FF1	8	12.5	26	22.49213	0.35568
FF2	15.25	12.5	25	22.29532	0.684
NAND2	1	12.5	4	18.27485	0.05472
NOR2	1	12.5	4	18.27485	0.05472
Total		100	Weighted Raw	**19.6853**	
			Routed	**14.76397**	

1.23x

H240

Product	**HiSilicon Kirin 990 5G**
Foundry	**TSMC 7+**
Track Height	6
CPP (nm)	57
MxP	40
Utilization	0.75
IP (Theoretical)	GPU

Cell Type	Gate Count NAND2 eq.	Cell Usage (%)	CPP Count	Gate Density (MG/mm2)	Cell Area (um2)
AOI22	2	12.5	5	29.23976608	0.0684
OAI22	2	12.5	5	29.23976608	0.0684
INV	0.5	12.5	2	18.2748538	0.02736
BUF	1	12.5	3	18.2748538	0.05472
FF1	8	12.5	24	24.36647173	0.32832
FF4	30.25	12.5	22	25.12792398	1.20384
NAND2	1	12.5	3	24.36647173	0.04104
NOR2	1	12.5	3	24.36647173	0.04104
Total		100	Weighted Raw	**24.15707237**	
			Routed	**18.11780428**	

1.38x

H210

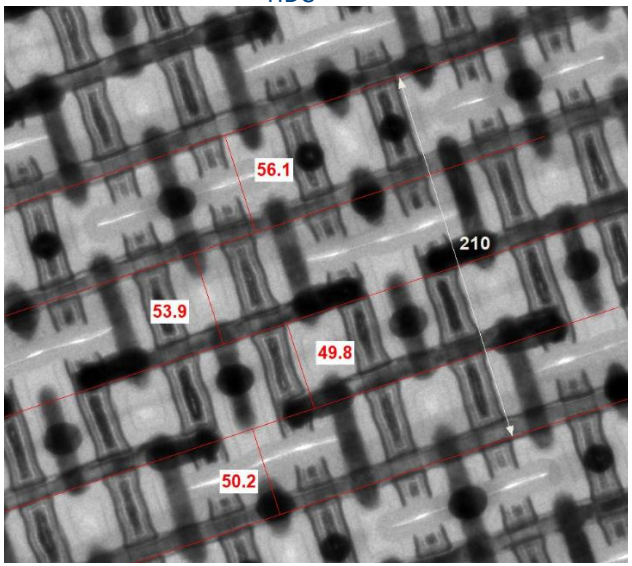
Product	**Apple A14 Bionic**
Foundry	**TSMC 5**
Track Height	6
CPP (nm)	51
MxP	35
Utilization	0.75
IP (Theroretical)	GPU

Cell Type	Gate Count NAND2 eq.	Cell Usage (%)	CPP Count	Gate Density (MG/mm2)	Cell Area (um2)
AOI22	2	12.5	5	37.3482726	0.05355
OAI22	2	12.5	5	37.3482726	0.05355
INV	0.5	12.5	2	23.3426704	0.02142
BUF	1	12.5	3	31.1235605	0.03213
FF1	8	12.5	19	39.3139712	0.20349
FF2	15	12.5	19	36.856848	0.40698
NAND2	1	12.5	3	31.1235605	0.03213
NOR2	1	12.5	3	31.1235605	0.03213
Total		100	Weighted Raw	**33.4475896**	
			Routed	**25.0856922**	

*Cells highlighted in yellow have WM>1

MOL: SRAM Bit Cell

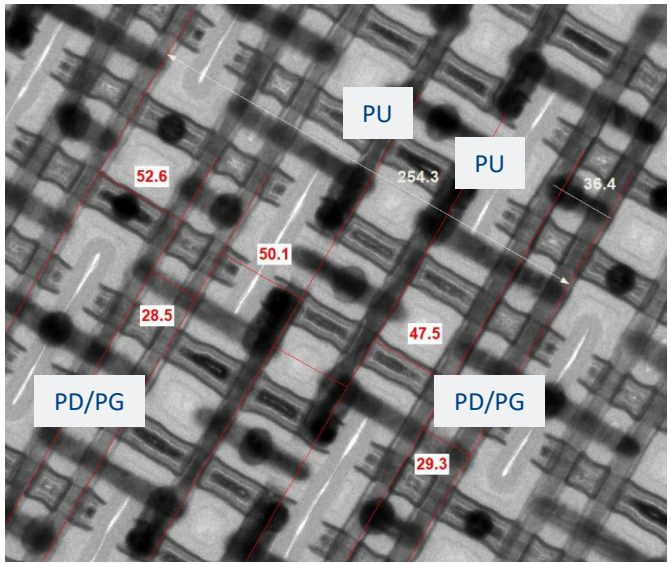
HDC



PU – PD/PG -> ~54 nm
PU – PU -> ~50 nm
PD/PG – PD/PG -> ~56 nm

Total bit cell height: 210 nm

HCC

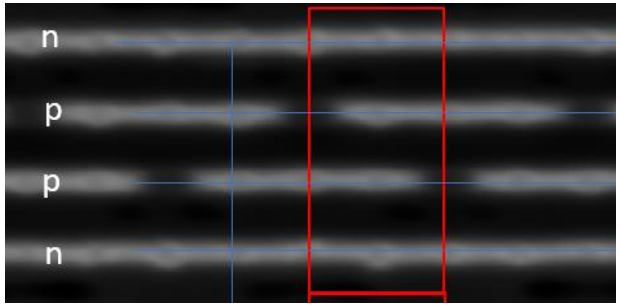


PU – PD/PG -> ~50 nm
PU – PU -> ~47 nm
PD/PG – PD/PG -> ~28 nm
PD/PG – PD/PG -> ~50 nm

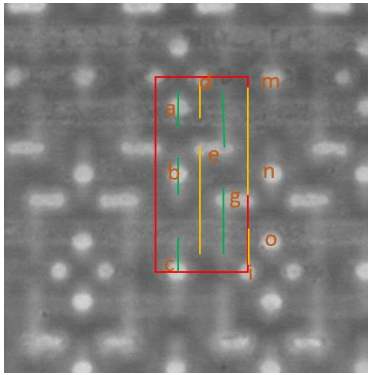
Total bit cell height: 252 nm

Bit cell height shrink came from neighboring cell PD/PG – PD/PG distance reduction

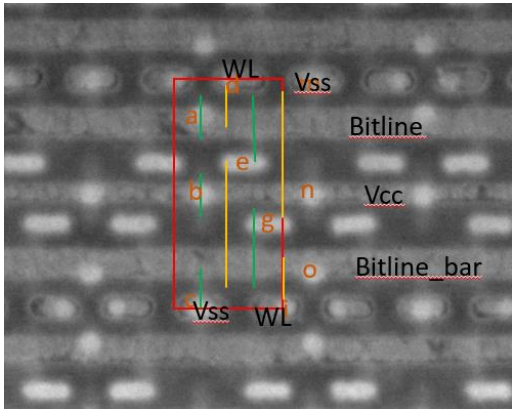
SRAM (HDC)



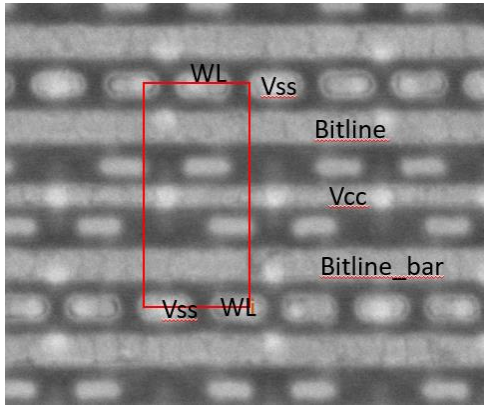
Fin (111)



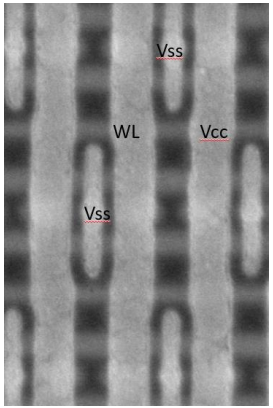
VCX



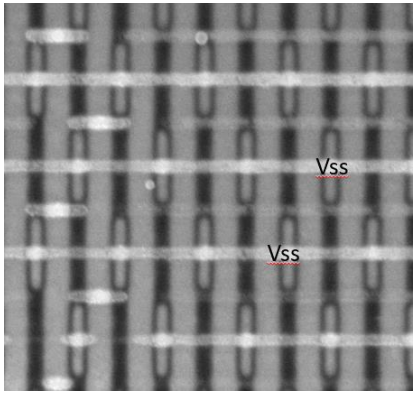
M0



M0

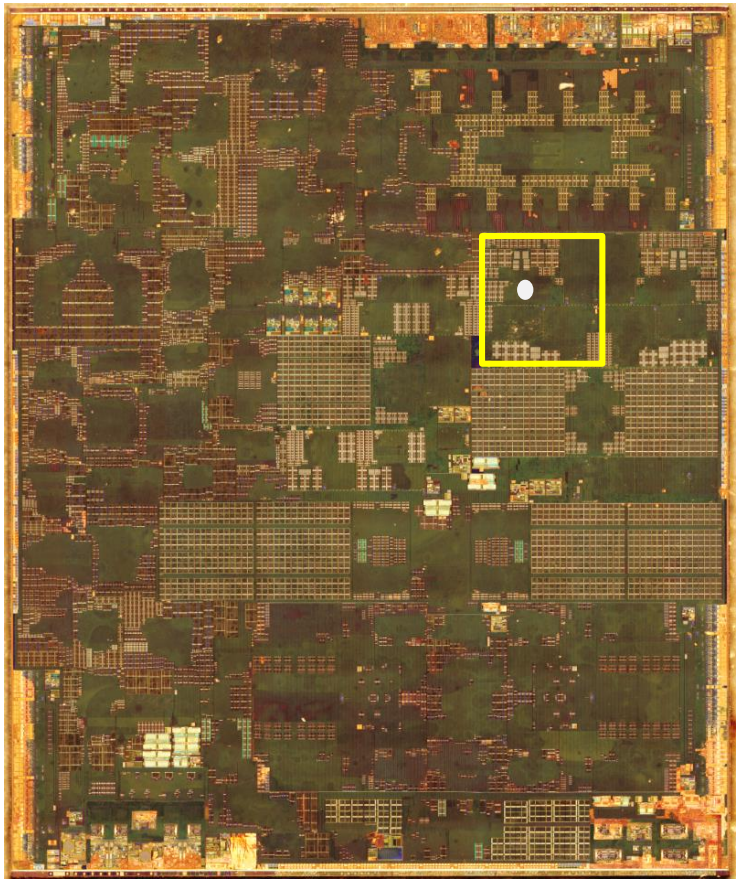


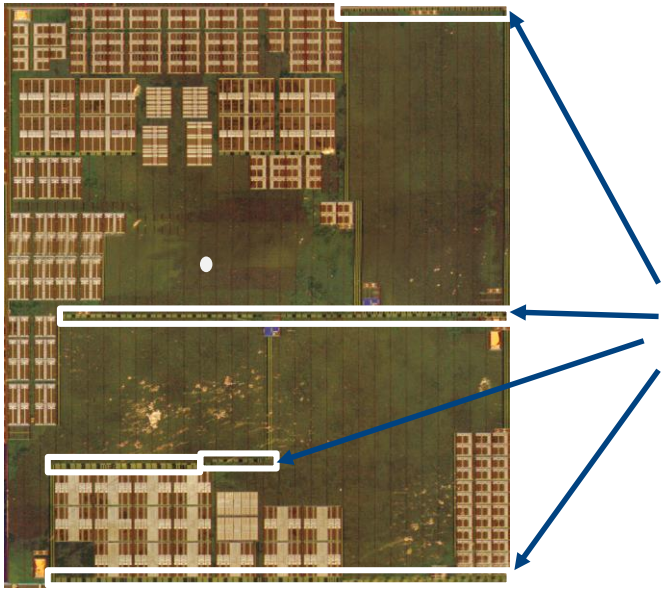
M1



M2

Big Core PDN

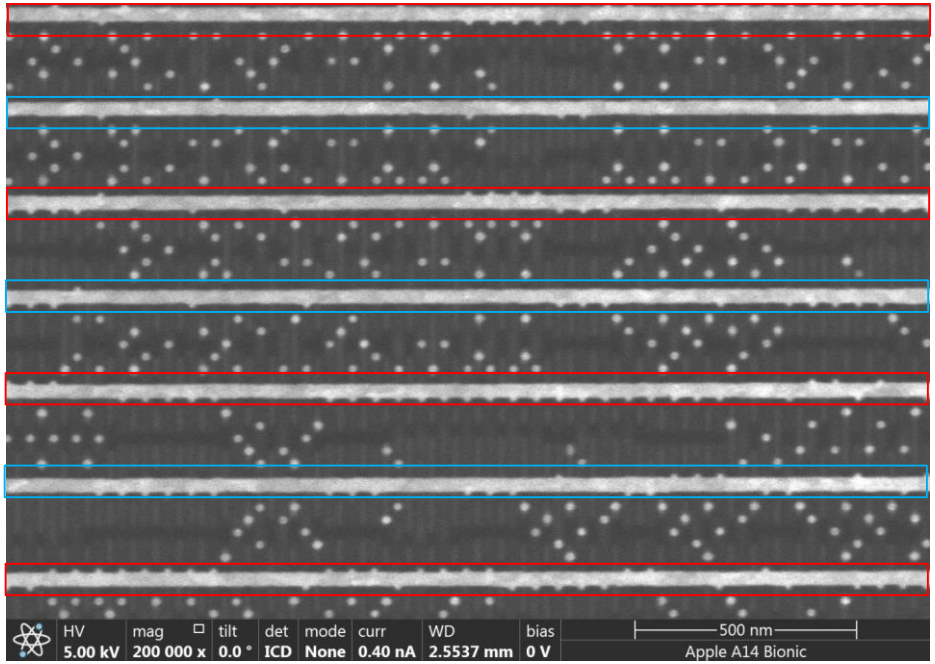




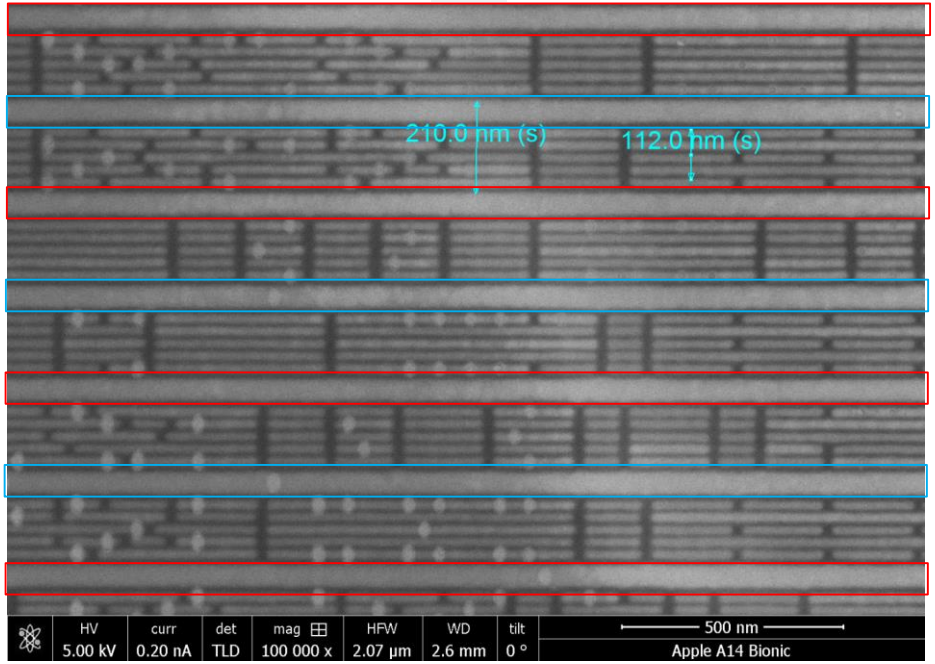
No distributed power gates. Big departure from previous A series CPU cores. Big and Little CPUs, GPU, NPU are all using lumped power gating.

Big Core PDN

VCX

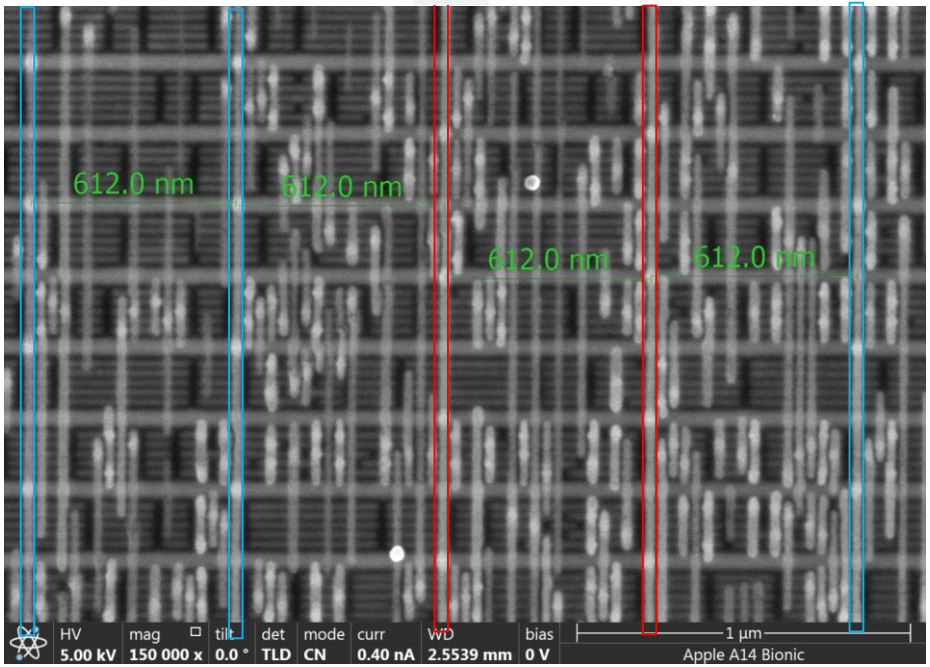


M0

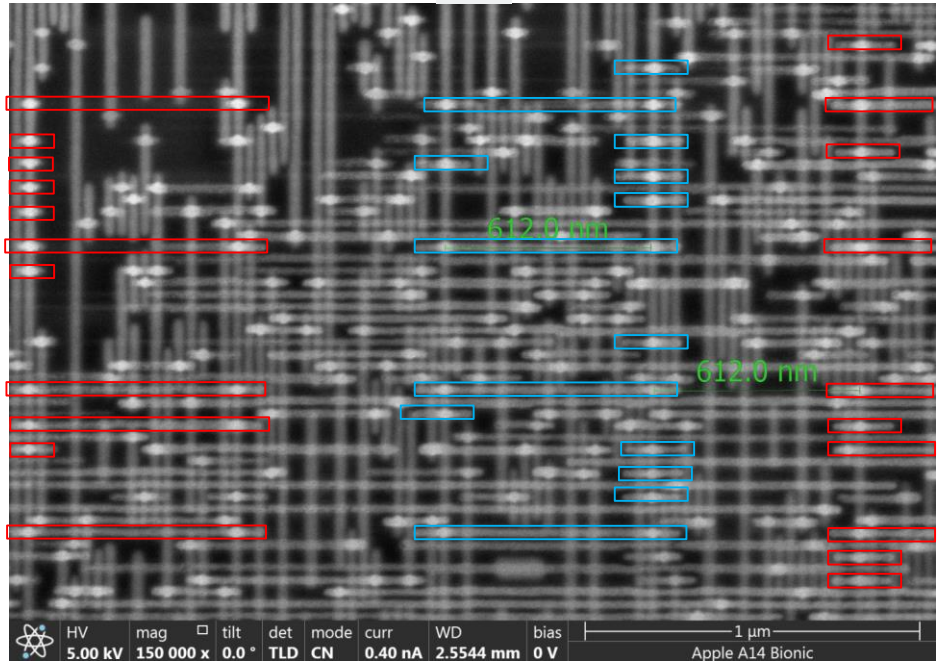


Big Core PDN

M1



M2



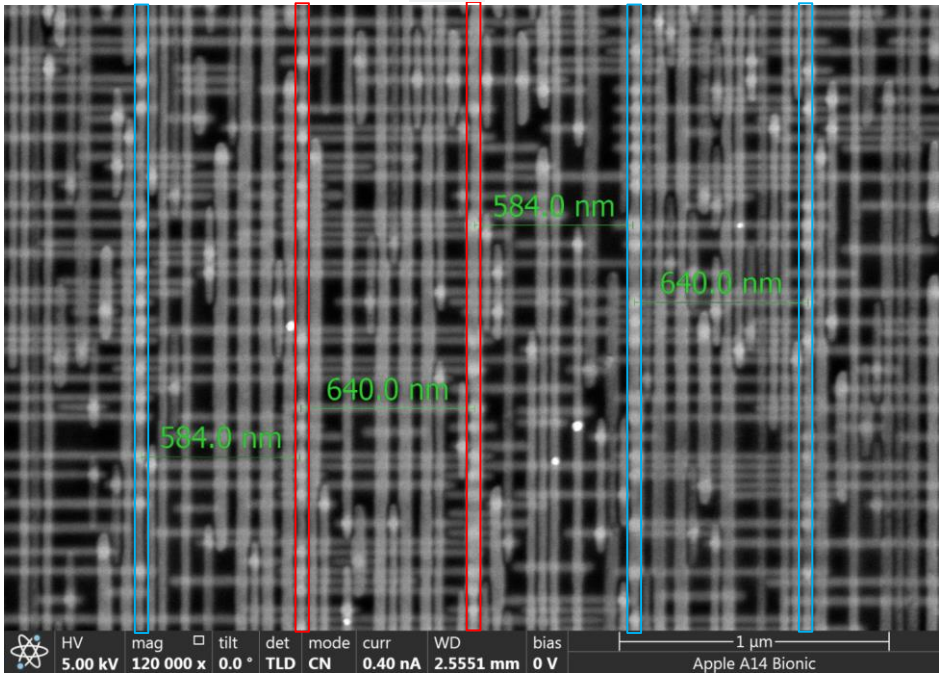
A lot of the even layers have opportunistic staples

Vcc-gated

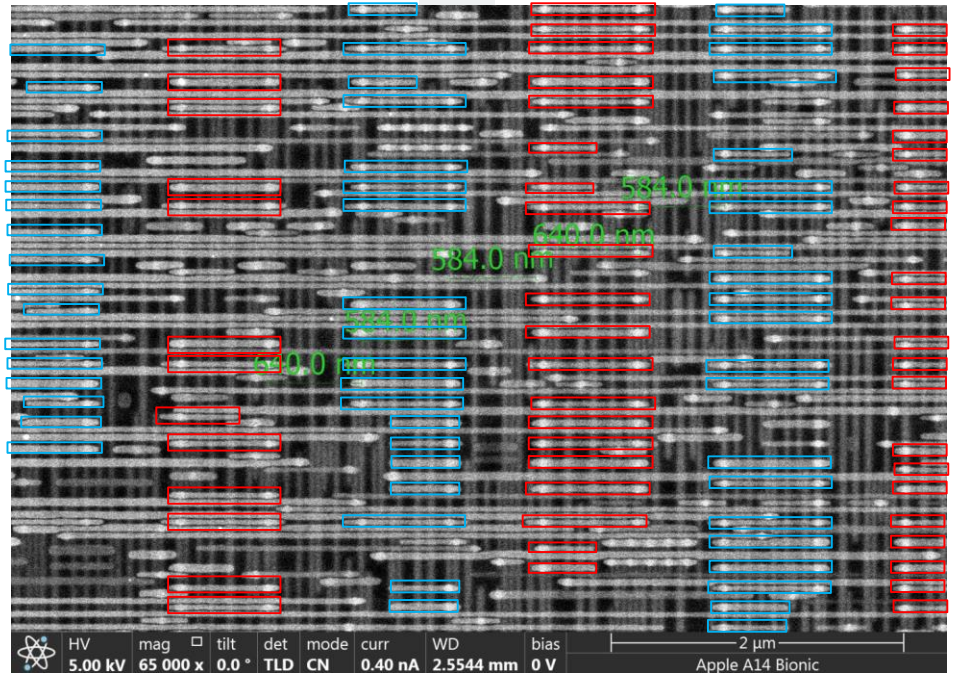
Vss

Big Core PDN

M3



M4



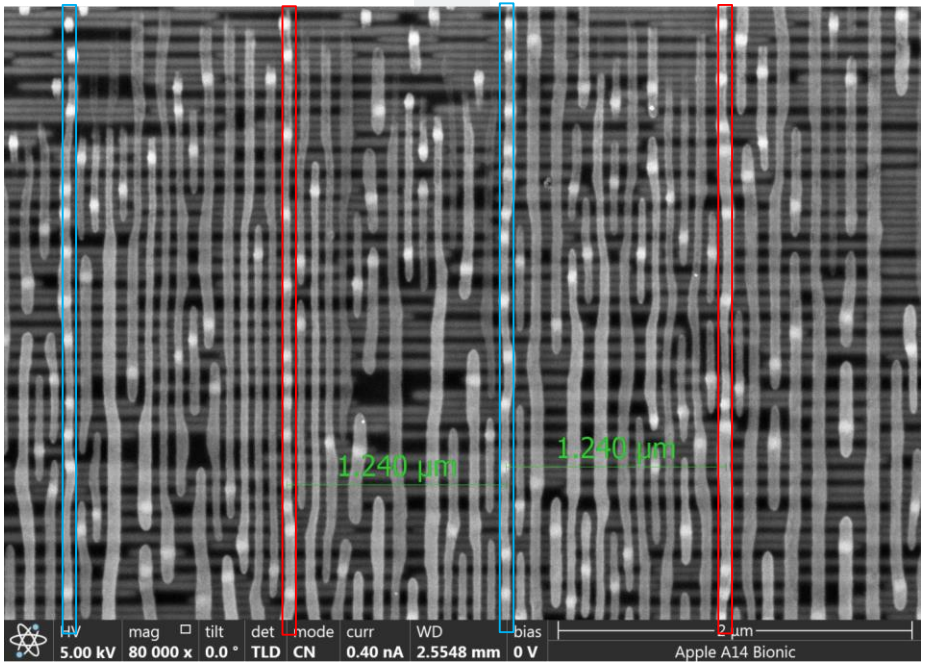
This area in CPU, M4 is severely underutilized due to PDN

Vcc-gated

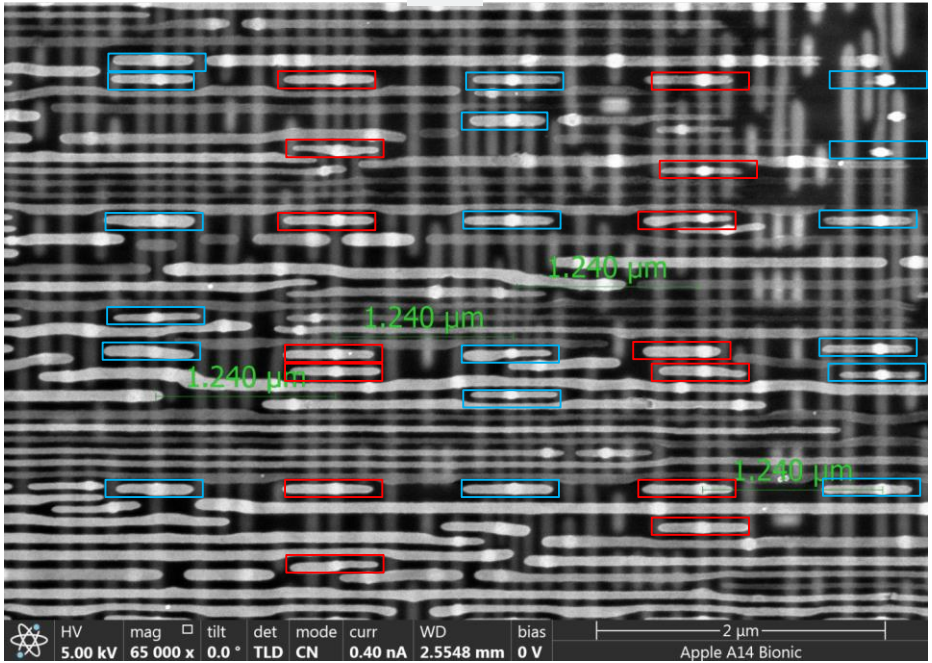
Vss

Big Core PDN

M5



M6

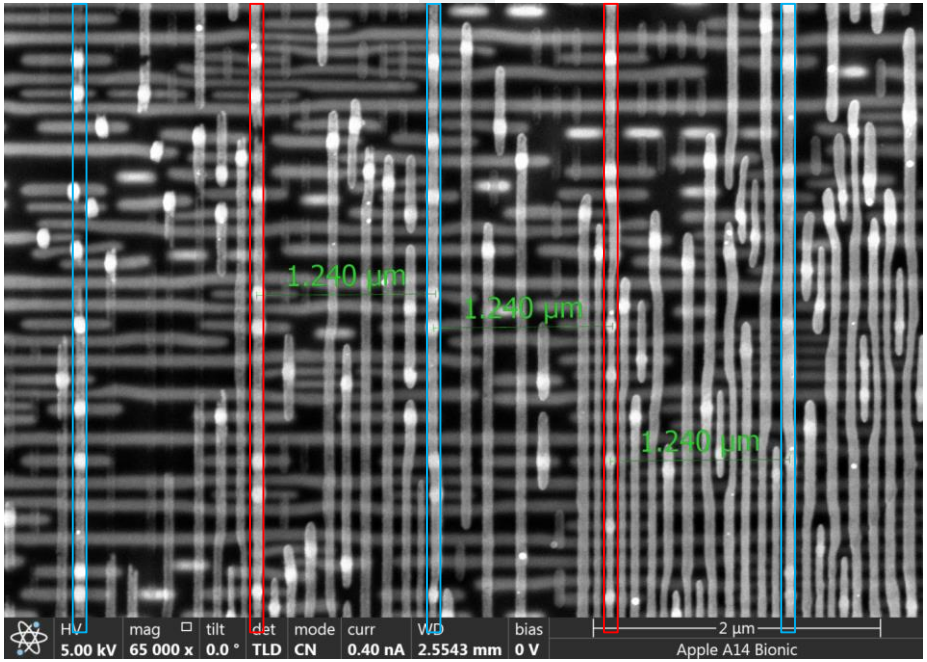


Vcc-gated

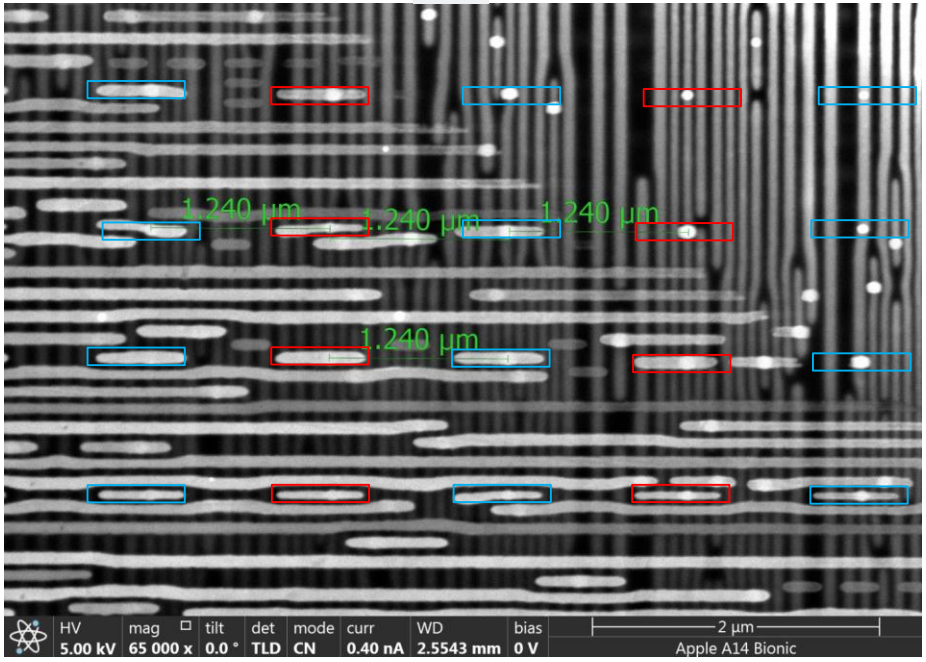
Vss

Big Core PDN

M7



M8

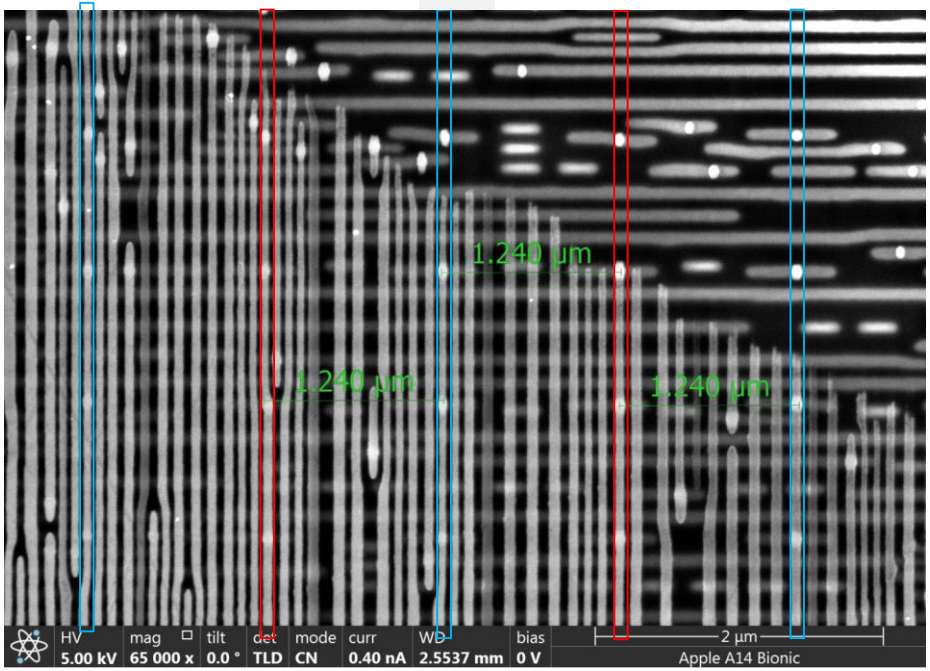


Vcc-gated

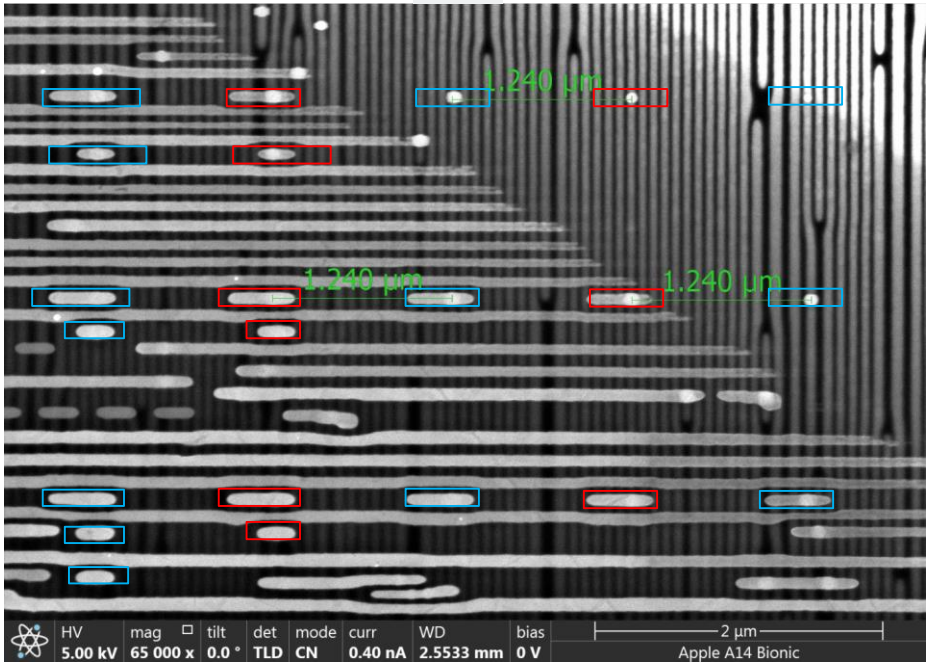
Vss

Big Core PDN

M9



M10

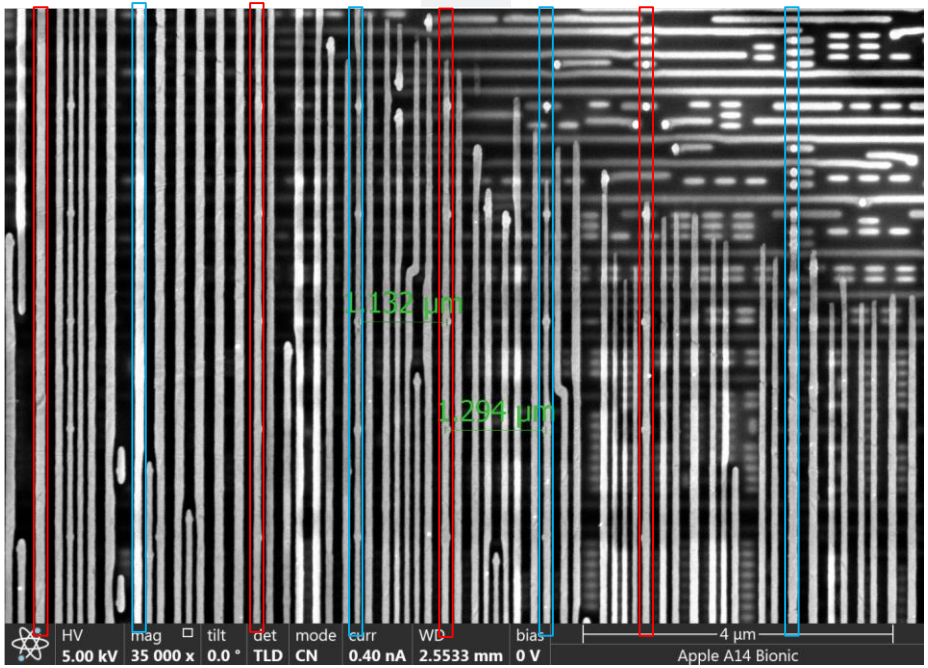


Vcc-gated

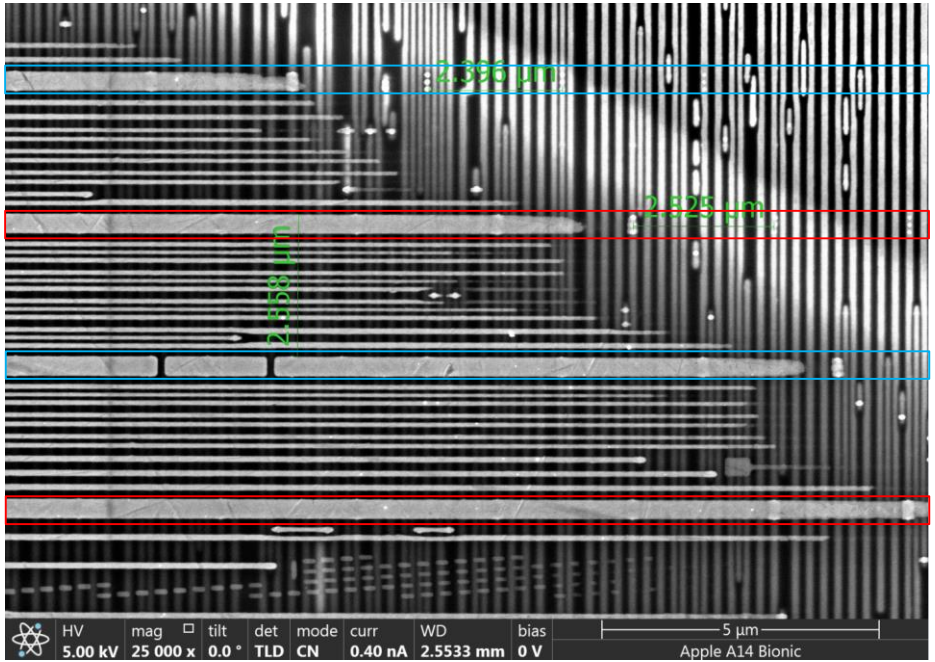
Vss

Big Core PDN

M11



M12

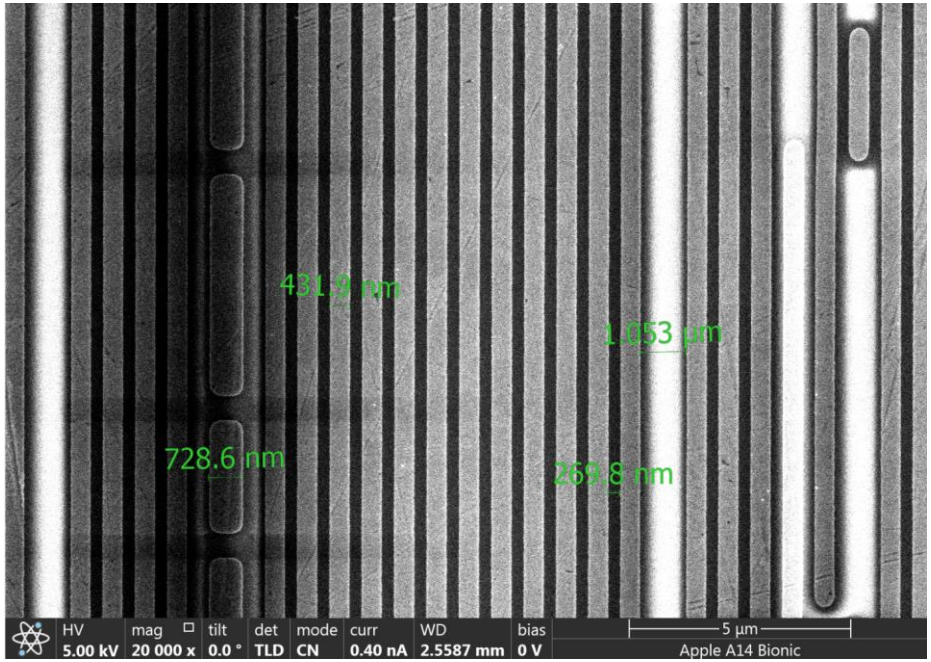


Vcc-gated

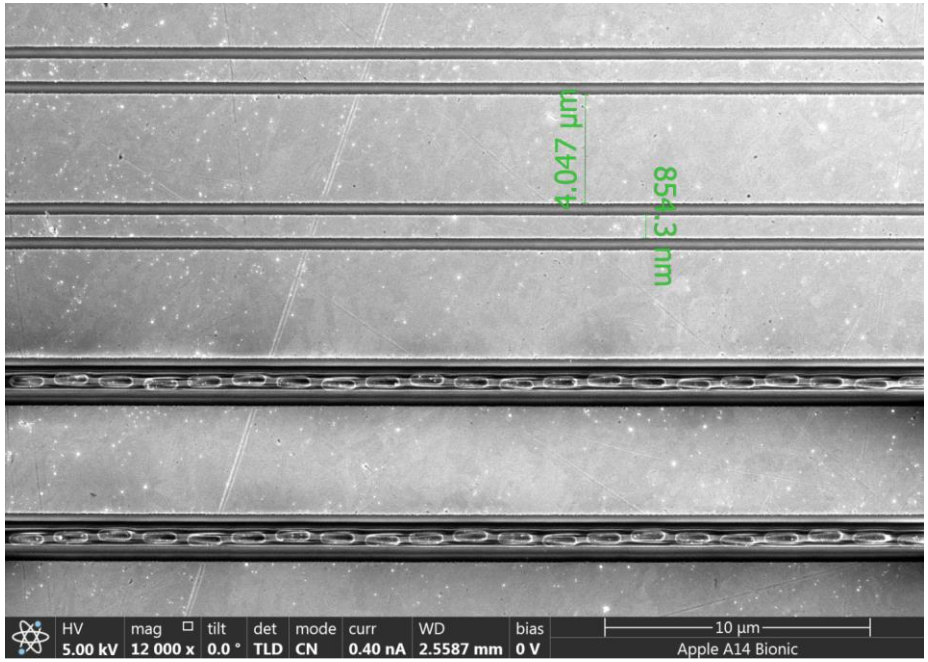
Vss

Big Core PDN

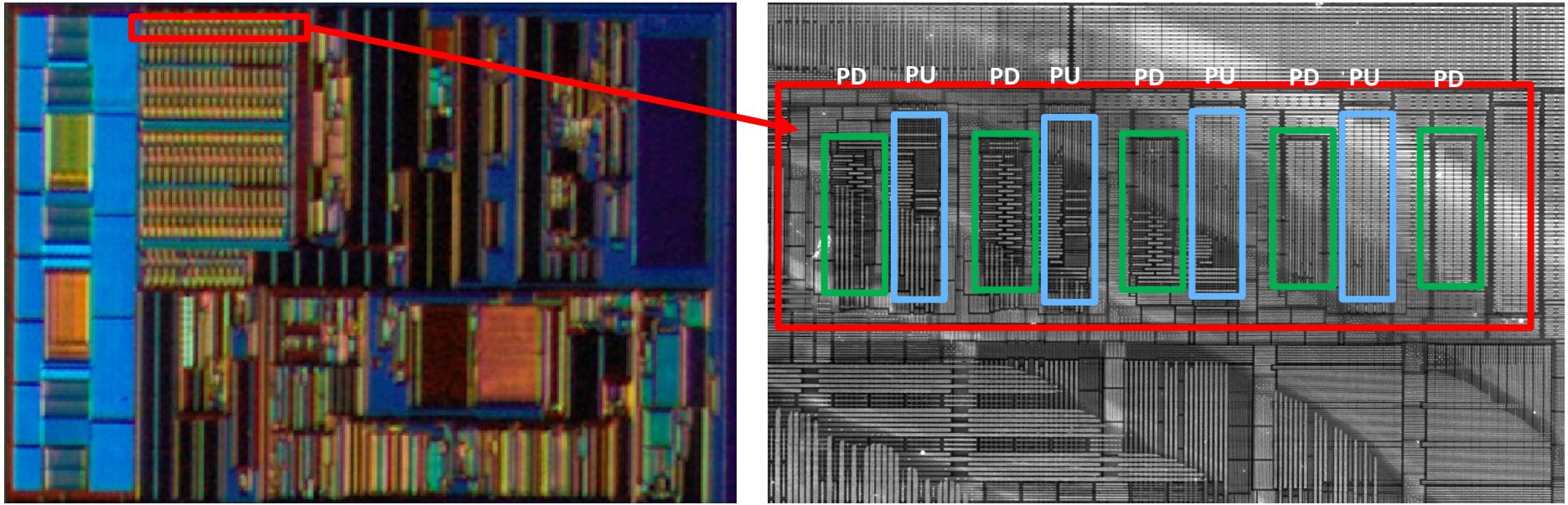
M13



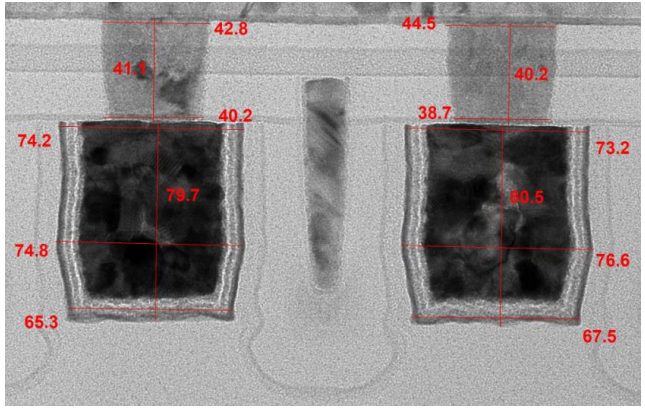
M14

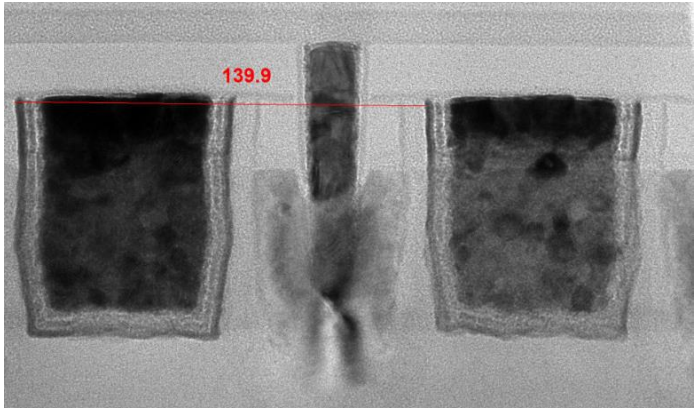


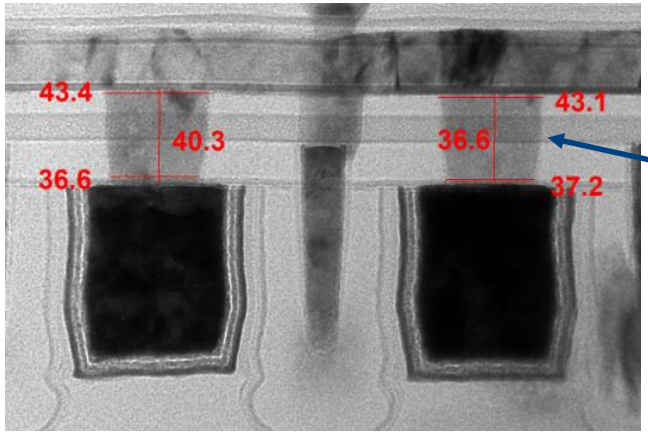
USB Driver Area

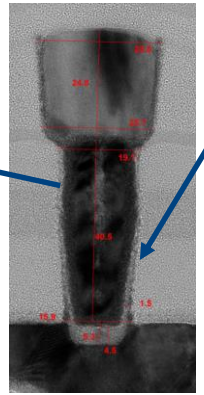


USB Driver Area: Thick Gate



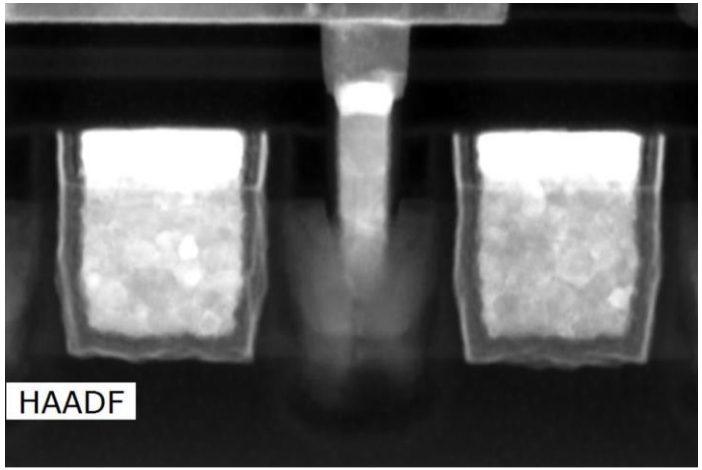


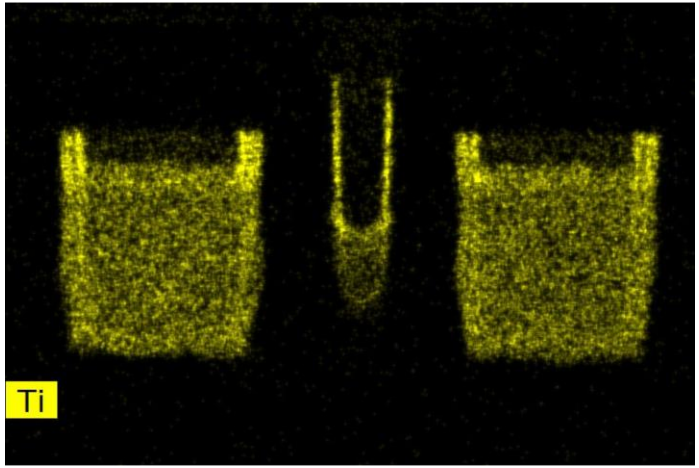


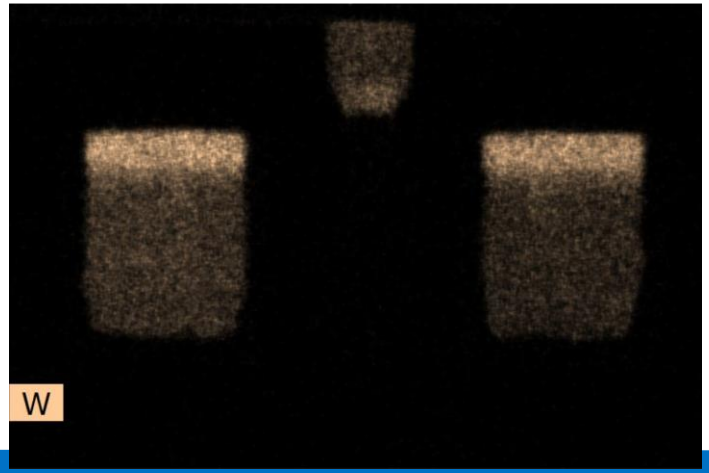


TiN
liner

USB Driver Area: Thick Gate VCT

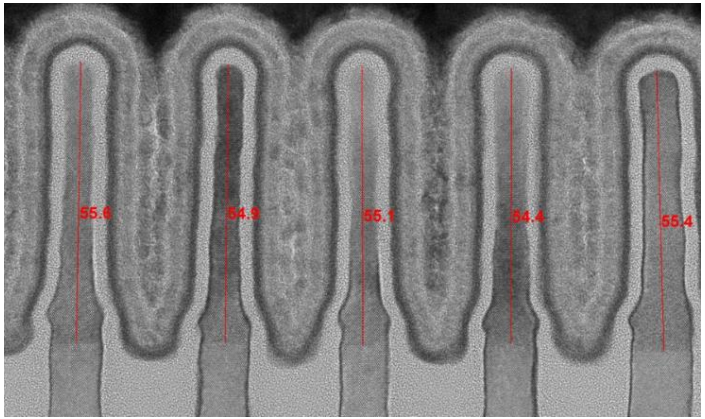


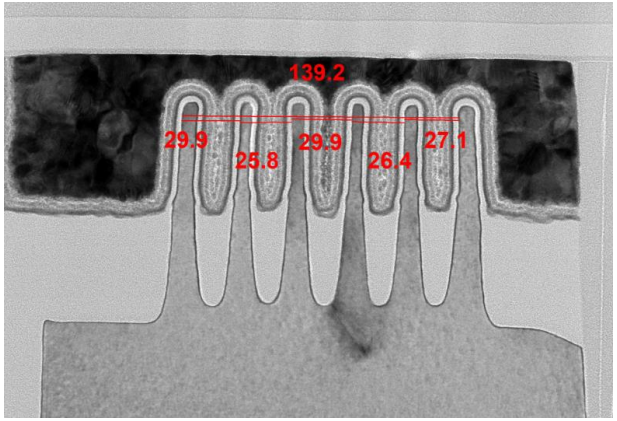


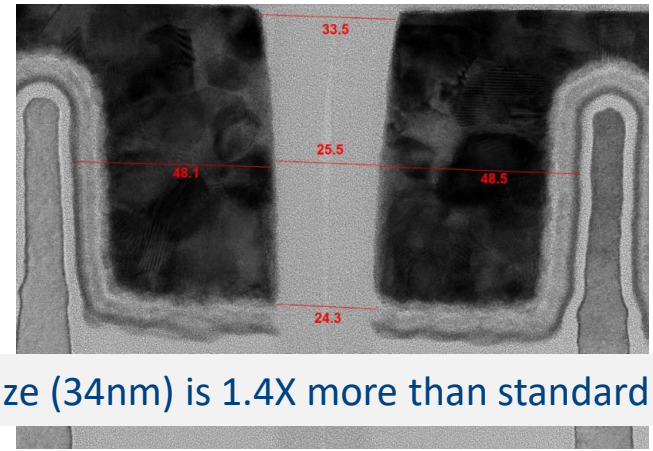


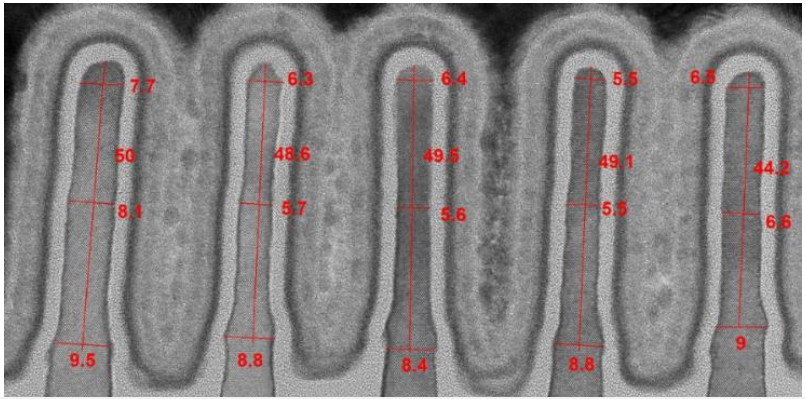
- VCT is again done using selective W CVD deposition
- VCT is different size than that in standard cell

USB Driver Area: Thick Gate Fin





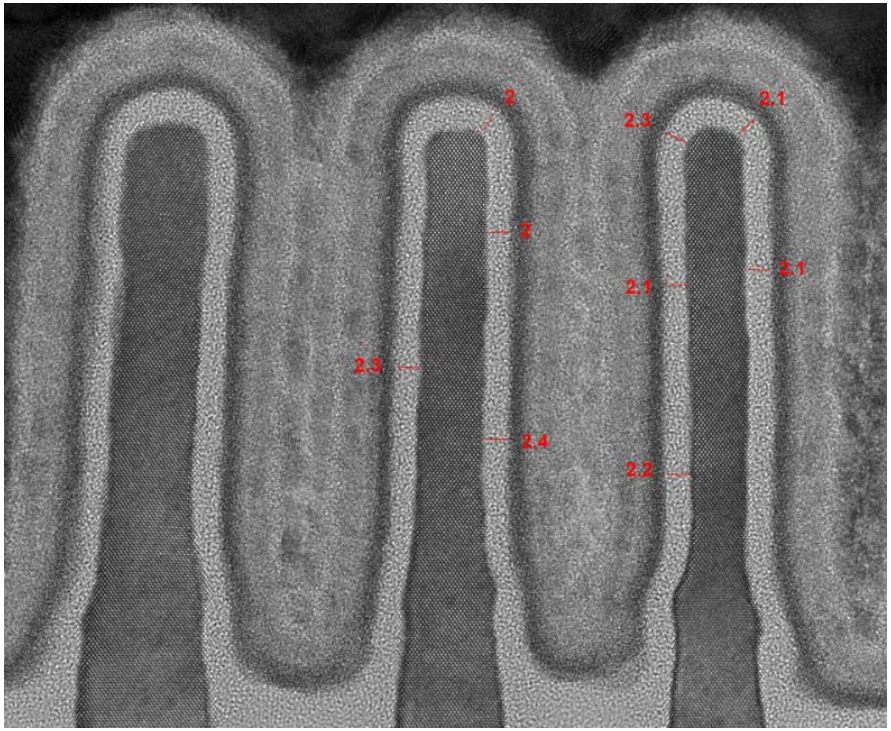


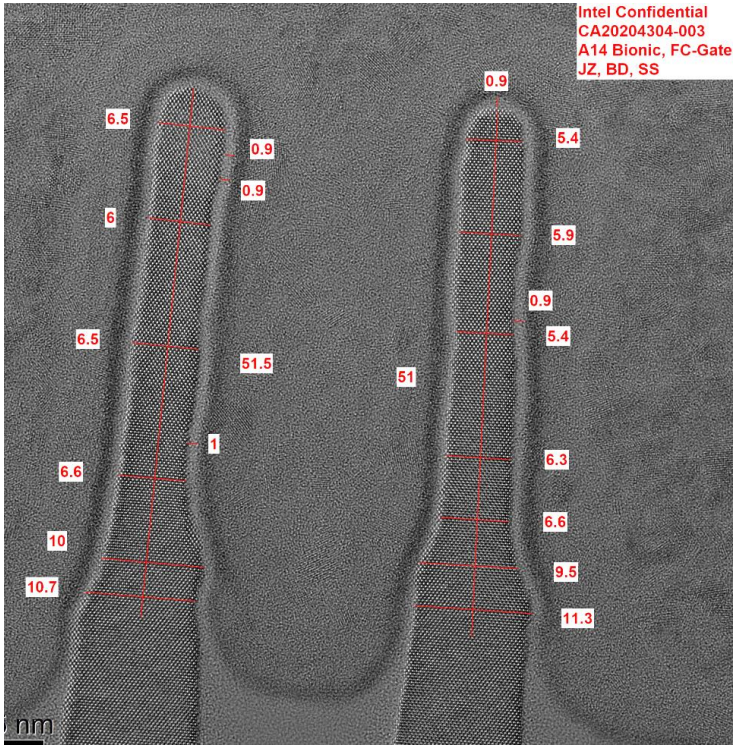


Plug size (34nm) is 1.4X more than standard cells

Fin width is wider for a lot of the outer fins by almost 2 nm

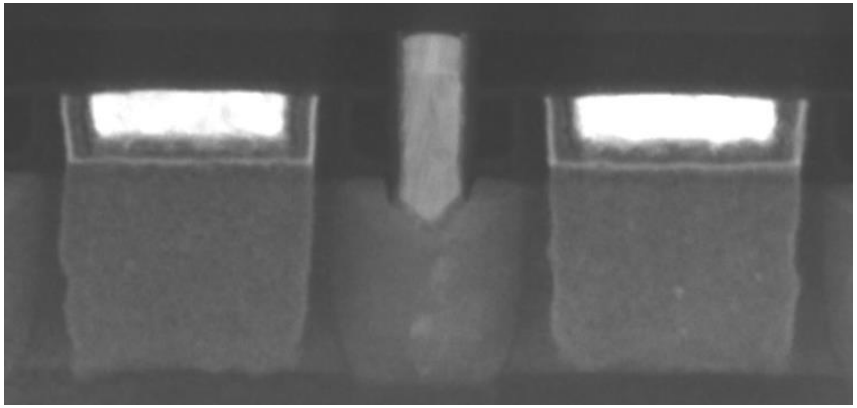
USB Driver Area: Thick gate GOX

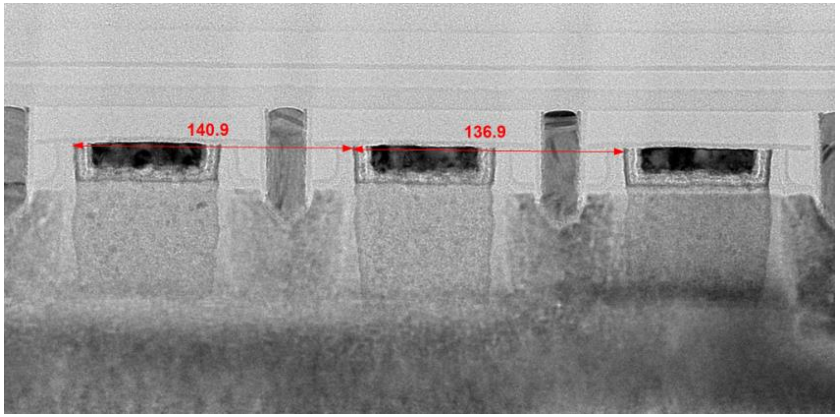


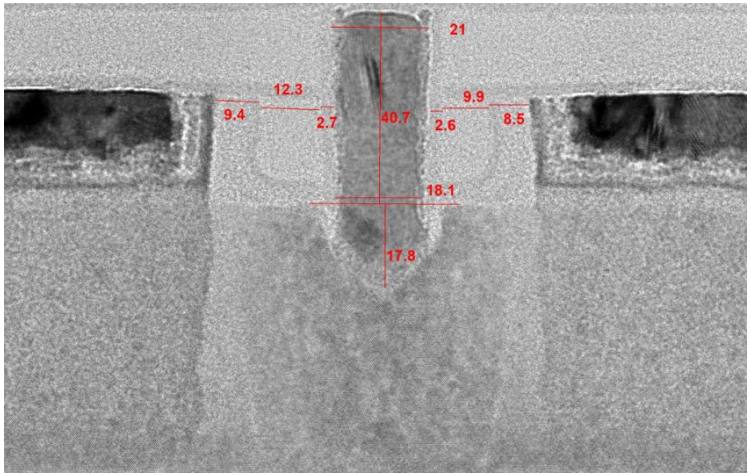


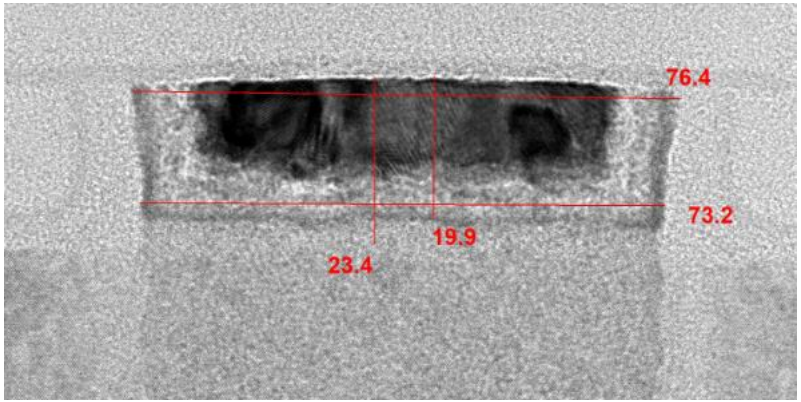
- GOX is about 2.3 nm
- SiOx GOX

USB Driver Area: PMOS

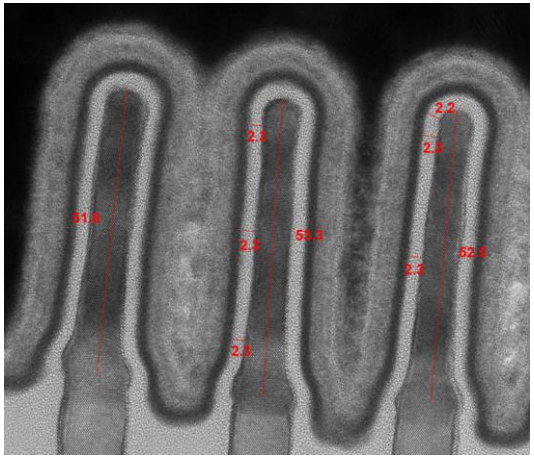


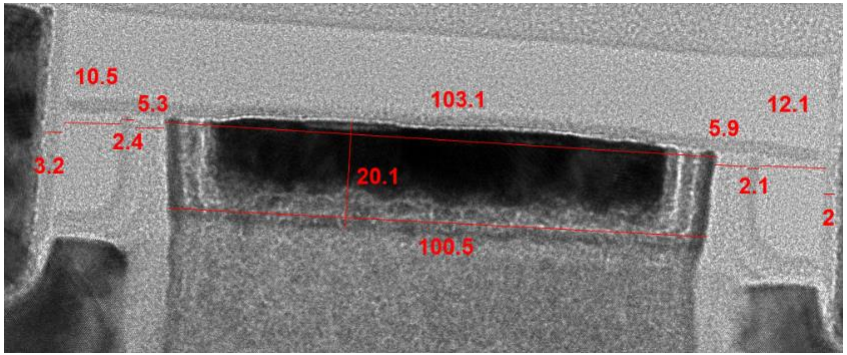


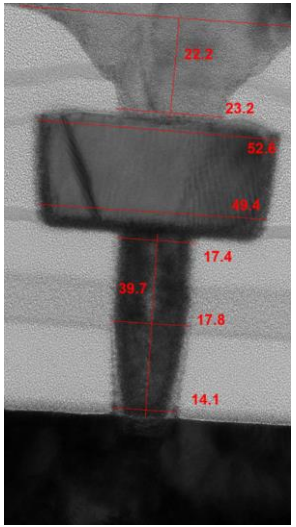


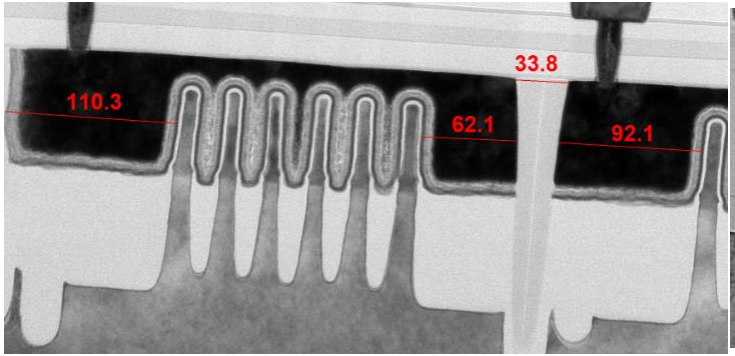


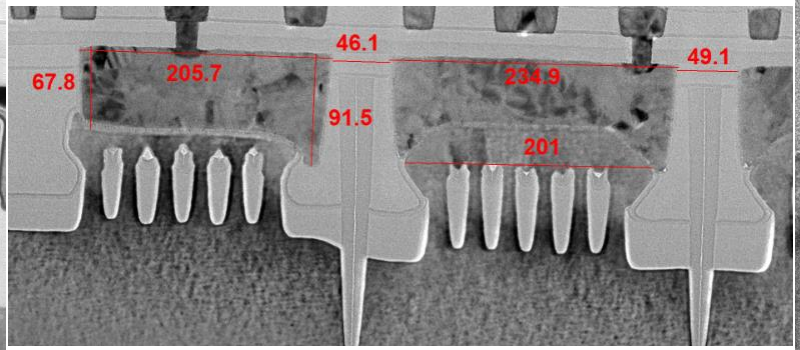
GPIO Area: PMOS (PP 170 nm)

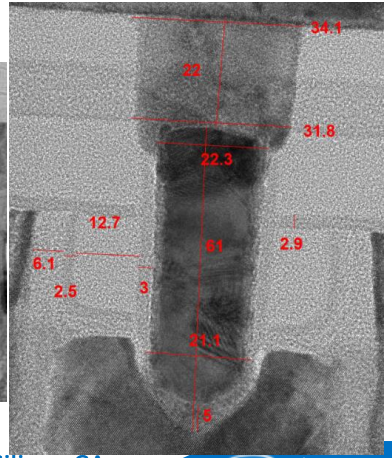










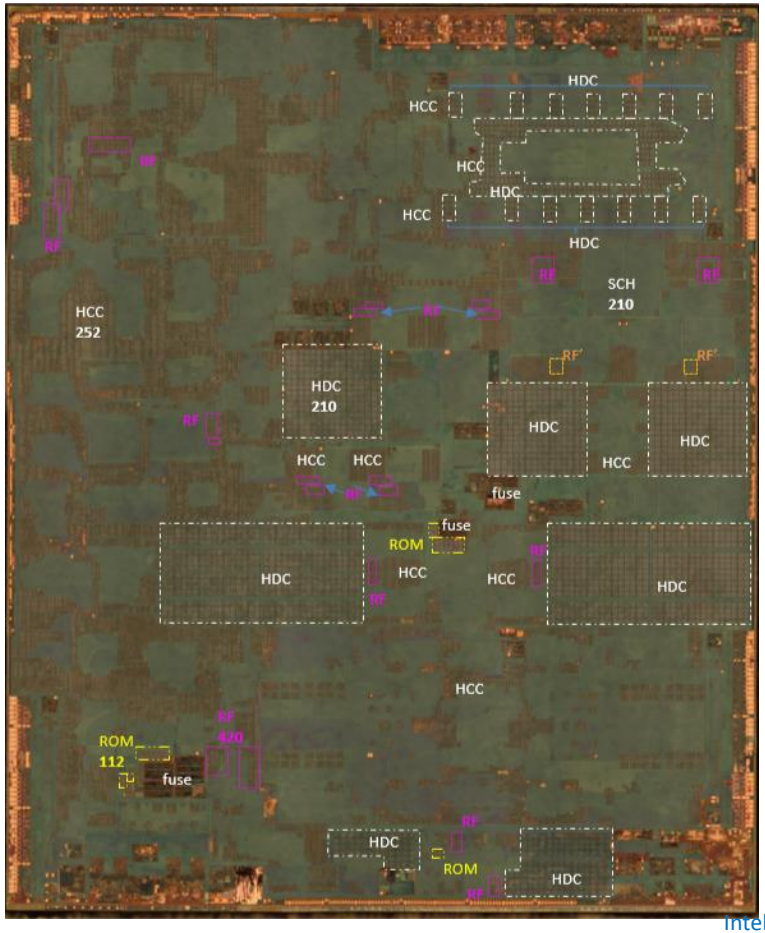


Thick Gate: N5 Vs. N7

Oxide	GOX	2.3	2.3	3.3	3.3	3.3	3.3
Poly	pp	140	170	230	230	180	167
	cd	75	100	150	160	112	100
	ETE	33	32	102			63/125
	End cap	48	62	65			113/74
TCN	cd	19	22	19			
	TCN-Poly space	22-24	22-24	23			

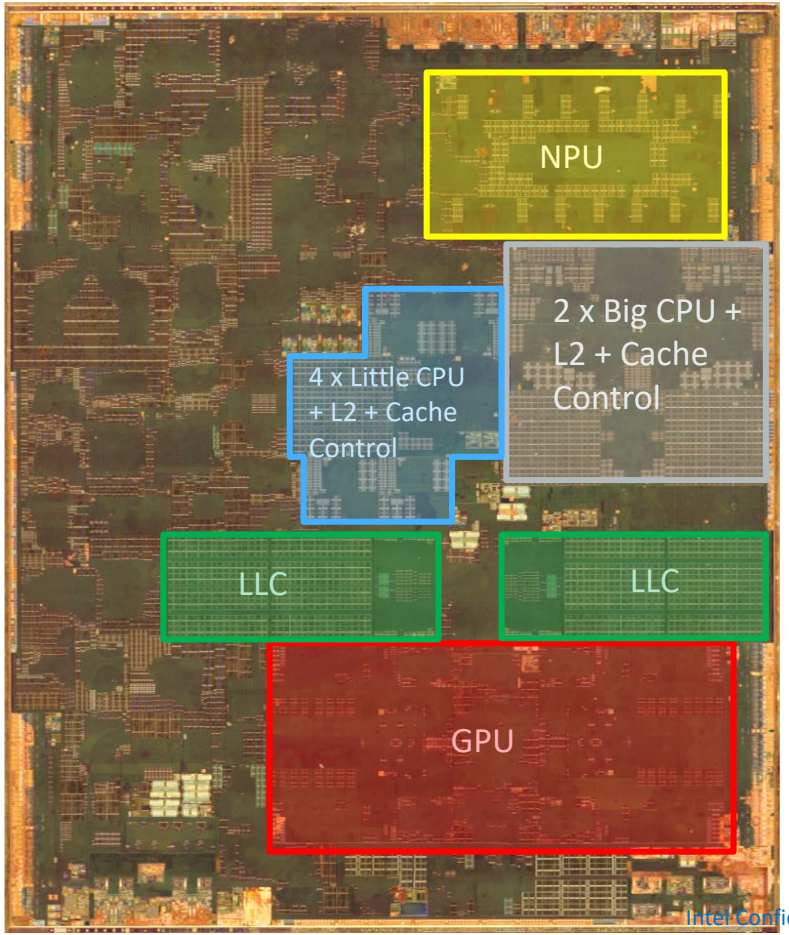
Floorplan analysis

Process map



- Entire chip uses H210 standard cells
- 0.0214 µm^2 HDC (111) usage in LLC, L2, NPU and most likely sense hub
- 0.0257 µm^2 HCC (122) usage most of the digital FUBs
- 0.043 µm^2 TPRF (1223) usage in CPU cores and some other area
- Couple of instances of ROM (bit cell height of 112 nm, width TBD)
- All of the major IPs like CPU, GPU, NPU are lumped power gated

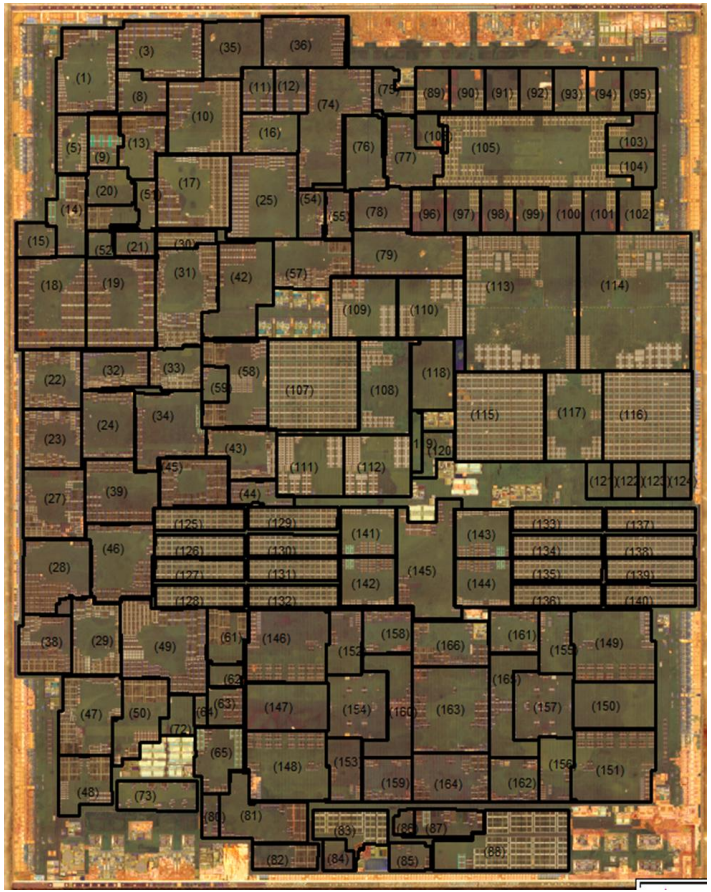
Floorplan: CPU, GPU, NPU, LLC



Total Chip Area: ~ 86.9mm^2
Single Big CPU: 2.26 mm^2
Single Little CPU: 0.59 mm^2
Single NPU: 0.23 mm^2

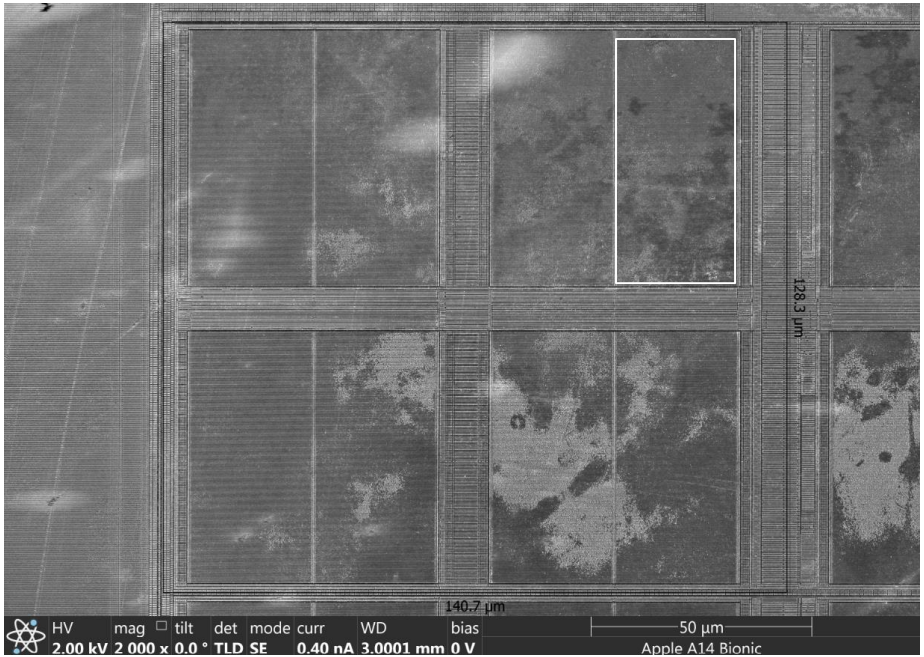
Big CPU L2 Capacity: 8 MB
Little CPU L2: 4 MB
LLC Capacity: 16 MB

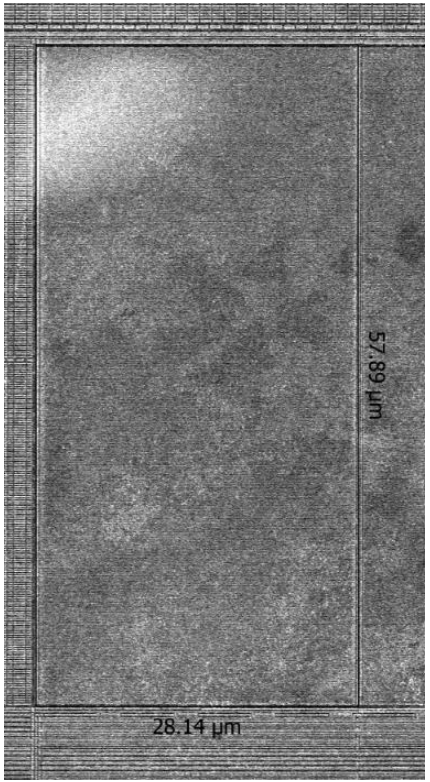
Floorplan: Digital FUBs



Name	ID	Area (mm²)
	1	0.731723
	3	0.684983
	5	0.280621
	8	0.283556
	9	0.245237
	10	0.806457
	11	0.215814
	12	0.217432
	13	0.395652
	14	0.398219
	15	0.193905
	16	0.340834
	17	0.799296
	18	0.932835
	19	0.930822
	20	0.248283
	21	0.15401
	22	0.508747
	23	0.507649
	24	0.527113
	25	0.835296
	27	0.628907
	28	0.650905
	29	0.527098
	30	0.138682
	31	0.82578
	32	0.370649
	33	0.324697
	34	0.69319
	35	0.469894
	36	0.631054
	38	0.450164
	39	0.630605
	42	0.765688
	43	0.450305
	44	0.205825
	45	0.485556
	46	0.692232
	47	0.673177
	48	0.419694
	49	1.007702
	50	0.516331
	51	0.157248
	52	0.101745
	54	0.191741
	55	0.186636
	57	0.531261
	58	0.693244
	59	0.137667
	61	0.309397
	62	0.113793
	63	0.210651
	64	0.06083
	65	0.408816
	72	0.176062
	73	0.341546
	74	0.941798
	75	0.229356
	76	0.421809
	77	0.460769
	78	0.35546
	79	0.732356
	80	0.113156
	81	0.601203
	82	0.251895
	83	0.381282
	84	0.13259
	85	0.170366
	86	0.069835
	87	0.274651
Sense HUB?	88	0.977204
NPU Core	89	0.22535
NPU Core	90	0.22535
NPU Core	91	0.22535
NPU Core	92	0.22535
NPU Core	93	0.22535
NPU Core	94	0.22535
NPU Core	95	0.22535
NPU Core	96	0.22535
NPU Core	97	0.22535
NPU Core	98	0.22535
NPU Core	99	0.22535
NPU Core	100	0.22535
NPU Core	101	0.22535
NPU Core	102	0.22535
NPU Core	103	0.223267
NPU Core	104	0.223668
NPU Common	105	1.868506
	106	0.135099
4 MB L2 Cache for Small CPU Cores	107	1.191738
L2 Cache Controller for Small CPU Cores	108	0.773904
Small CPU Core	109	0.595379
Small CPU Core	110	0.595379
Small CPU Core	111	0.595379
Small CPU Core	112	0.595379
Big CPU Core	113	2.267281
Big CPU Core	114	2.267281
4 MB L2 Cache Controller for Big CPU Cores	115	1.188398
4 MB L2 Cache Controller for Big CPU Cores	116	1.188398
	117	0.755042
	118	0.437948
	119	0.094715
	120	0.18114
AMX?	121	0.139522
AMX?	122	0.139522
AMX?	123	0.139522
AMX?	124	0.139522
1 MB LLC	125	0.290433
1 MB LLC	126	0.290433
1 MB LLC	127	0.290433
1 MB LLC	128	0.290433
1 MB LLC	129	0.290433
1 MB LLC	130	0.290433
1 MB LLC	131	0.290433
1 MB LLC	132	0.290433
1 MB LLC	133	0.290433
1 MB LLC	134	0.290433
1 MB LLC	135	0.290433
1 MB LLC	136	0.290433
1 MB LLC	137	0.290433
1 MB LLC	138	0.290433
1 MB LLC	139	0.290433
1 MB LLC	140	0.290433
Performance Controller Core	141	0.400873
Performance Controller Core	142	0.400873
Performance Controller Core	143	0.400873
Performance Controller Core	144	0.400873
	145	0.892397
GPU Sub-system	146	0.859408
GPU Sub-system	147	0.578169
GPU Sub-system	148	0.832044
GPU Sub-system	149	0.850198
GPU Sub-system	150	0.578169
GPU Sub-system	151	0.855626
GPU Sub-system	152	0.326582
GPU Sub-system	153	0.316127
GPU Sub-system	154	0.57295
GPU Sub-system	155	0.318512
GPU Sub-system	156	0.317677
GPU Sub-system	157	0.572424
GPU Sub-system	158	0.320452
GPU Sub-system	159	0.320452
GPU Sub-system	160	0.503966
GPU Sub-system	161	0.320452
GPU Sub-system	162	0.320452
GPU Sub-system	163	0.508305
GPU Sub-system	164	0.545484
GPU Sub-system	165	0.974621
GPU Sub-system	166	0.504825

A14 L2, LLC (HDC bit cells)





Poly

256 + 16 columns

256 + 16 rows

Macro X and Y: 140.7 µm x 128.3 µm

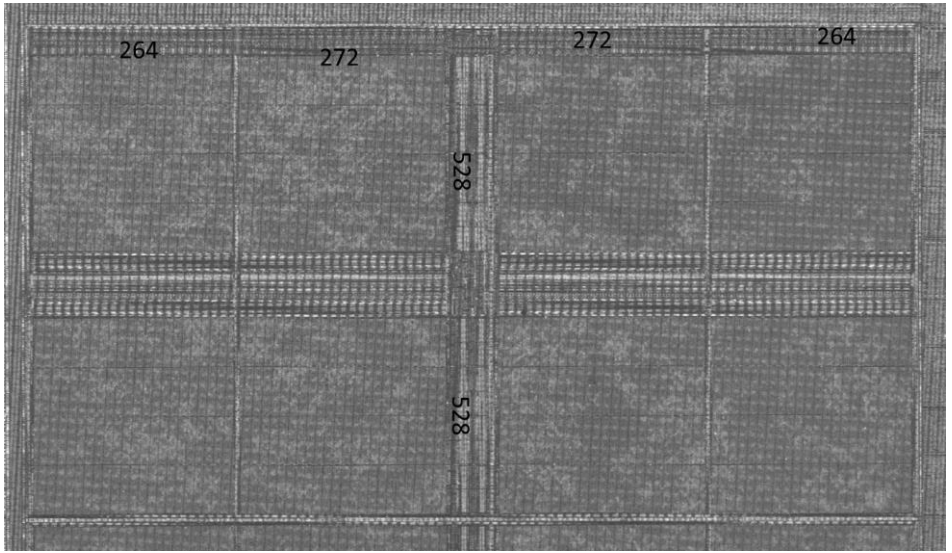
Macro efficiency: ~72%

A13 L2, LLC (HDC bit cells)

L2

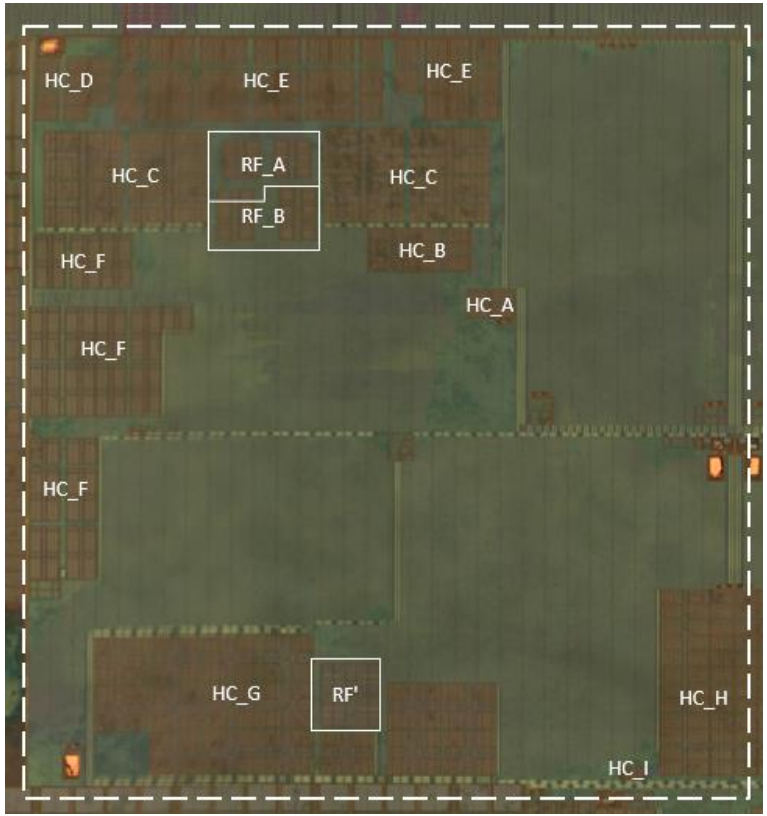
Macro efficiency: ~74.4%

LLC



Macro efficiency: ~71.7%

A14 Big Core Memory Breakdown



ROI	SRAM cell size in um2	Single Sub Array efficiency	Total Capacity (KB)
HC_A	0.025704	0.234947931	6.417031
HC_B	0.025704	0.234947931	19.25109
HC_C	0.025704	0.486901573	291.5498
HC_D	0.025704	0.245161536	18.2873
HC_E	0.025704	0.30106456	151.6316
HC_F	0.025704	0.371455376	204.7159
HC_G	0.025704	0.239377944	187.3892
HC_H	0.025704	0.261231998	63.95869
HC_I	0.025704	0.261231998	1.77663
RF_A	0.04284	0.204742865	8.080337
RF_B	0.04284	0.313357528	12.9912

$I?

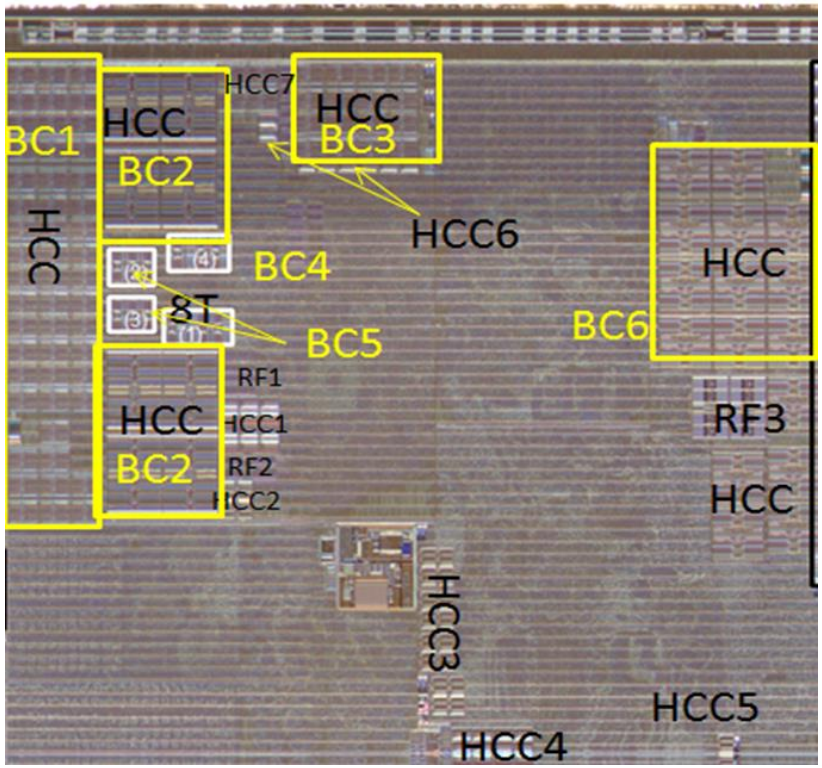
$D?

Verified capacity for

$I = 192 KB

$D = 128 KB

A13 Big Core Memory Breakdown



ROI	Memory type	SRAM cell size in um2	Single Sub Array efficiency	Total Capacity (KB)
BC 1	HC6t	0.035	0.278662609	160.5052
BC 2	HC6t	0.035	0.638577693	81.52734
BC 3	HC6t	0.035	0.278172353	50.38875
BC 4	8t	0.051	0.243790025	5.745605
BC 5	8t	0.051	0.167463857	5.924359
BC 6	HC6t	0.035	0.361013021	79.94206
BC 7	8t	0.140	0.088907235	2.605669
HCC 1	HC6t	0.035	0.206016918	10.5761
HCC 2	HC6t	0.035	0.264099709	5.705946
HCC 3	HC6t	0.035	0.264092775	22.59771
HCC 4	HC6t	0.035	0.20577285	7.135313
HCC 5	HC6t	0.035	0.25240269	1.42715
HCC 6	HC6t	0.035	0.207799329	7.170144
HCC 7	HC6t	0.035	0.300386886	13.29318