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NVIDIA
GV100-400-A1
TSMC 12FFN FinFET Process

Advanced CMOS Essentials

ACE-1801-801

94359OWLG

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Overview

This is an Advanced CMOS Essentials (ACE) Summary document, provided as a companion deliverable for Advanced CMOS Essentials projects. The complete Advanced CMOS Essentials deliverable includes:

- Concise analyst's summary of critical device metrics, TEM-EDS results, and salient features supported by the following image folders:
  - Downstream product teardown
  - Package photographs and X-rays, top metal and poly die photographs
  - SEM bevel
    - SRAM
    - Logic
  - SEM cross section of the general device structure, metals, dielectrics, and detail of the FEOL structures
  - TEM bevel
    - SRAM
    - Logic
  - TEM cross section
    - Orthogonal to transistor fins
    - Orthogonal to transistor gates

Observed Critical Dimensions

Report code	ACE-1801-801
Package dimensions	55 mm x 55 mm x 3.8 mm thick
Manufacturer, part number, downstream	NVIDIA, GV100-400-A1, NVIDIA Titan V graphics card
Wafer size, foundry, process type	300 mm, TSMC, 12FFN finFET high-k metal gate (HKMG) CMOS
Die markings	NVIDIA GV100- (M) 2016 ©
Die size (from die seal)	25.52 mm x 31.97 mm (815.87 mm^2)
Die size (actual)	25.60 mm x 32.23 mm (825.09 mm^2)
Number, type of metals	15 (14 copper (Cu), 1 aluminum (Al))
Contacted logic gate pitch	90 nm
Minimum metal pitch	64 nm
SRAM cell size	0.51 µm x 0.18 µm (0.092 $µm^2$)
Technology generation	16 nm
Feature measured to determine process generation	Metal 2 pitch

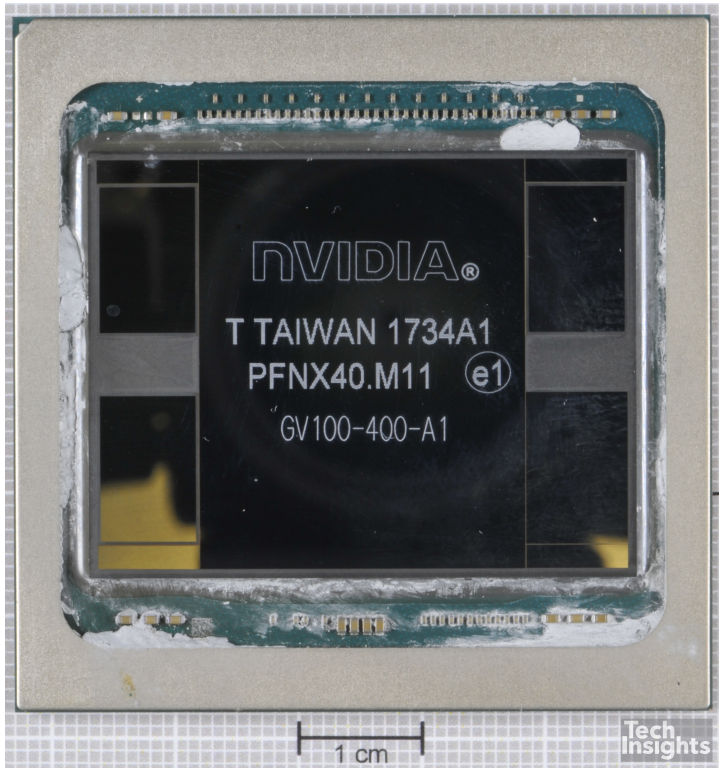
Salient Features

- The NVIDIA GV100-400-A1 was built on 300 mm wafers using TSMC's 12FFN finFET HKMG CMOS process
- Despite the node naming of "12FFN", the technology appears to only be a back end of line (BEOL) update of the previously analyzed TSMC 16FF+ process
- The minimum gate pitch observed in both the standard logic array and memory array is ~90 nm
- The minimum gate length observed is ~25 nm
- The logic fin height is ~42 nm and the fin pitch is ~48 nm. SRAM fins have a variable pitch
- The fin width of ~7 nm, measured at the center of the fin height, is the same for both NMOS and PMOS
- The logic gate height is ~70 nm
- The standard cell width is ~576 nm (equivalent to nine tracks)
- The minimum metal (M2) pitch observed is ~64 nm
- The minimum 6-transistor (6T) SRAM cell size is ~0.092 μm^2
- Metal 1 to metal 5 consist of Cu with a cobalt (Co) cap and liner, metal 6 to metal 12 consist of a Cu with a manganese (Mn) cap, and metal 13 to metal 14 consist of Cu. All the Cu metals have Ta-based liners
- A metal-insulator-metal (MIM) capacitor lies between metal 13 and metal 14 and consists of titanium nitride (TiN)/aluminum zirconium oxide (AlZrO)/TiN stack
- An etch stop layer (AlNO)/(SiOC) was used over metal 1 through metal 5
- An etch stop layer (SiCN)/(SiO) was used over metal 6 through metal 12
- Similar to TSMC's 16FF+ process, the minimum shallow trench isolation (STI) width is reduced to ~30 nm to enable a dummy poly single diffusion break (SDB) between standard cells

Salient Features

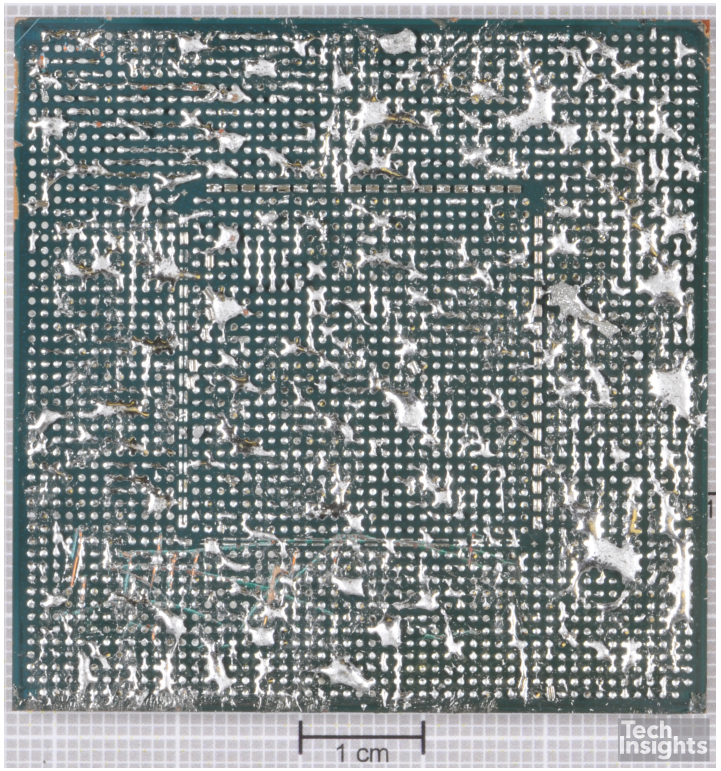
- Source and drain PMOS areas consist of silicon germanium (SiGe) epi, while those of NMOS areas consist of phosphorus (P)-doped Si epi. NMOS epi are unmerged and heavily gouged by the contact etch, while PMOS epi are merged and slightly gouged by the contact etch
- The end fins of multiple (more than two) fins are narrower and more tapered than the middle fin(s), indicating that there is no improvement from previous 16 nm process variants

NVIDIA GV100-400-A1 Package



\2 Package_and_Die_Photographs_X-rays_and_Optical\
GV100-400-A1_Pkg_Top_299982_Cropped.png

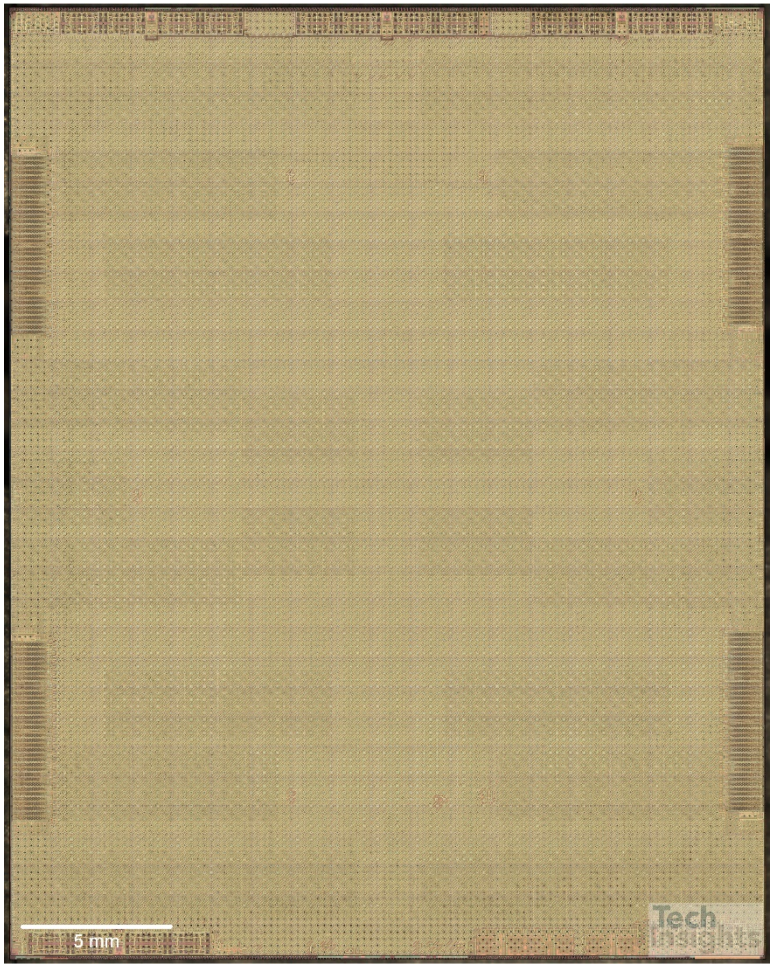
Top



\2 Package_and_Die_Photographs_X-rays_and_Optical\
GV100-400-A1_Pkg_Bot_299982_Cropped.png

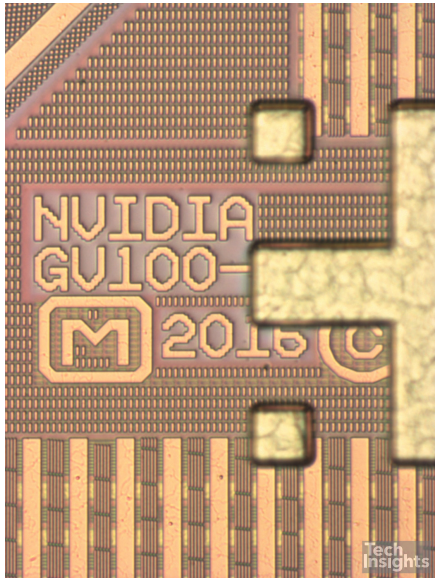
Bottom

NVIDIA GV100-400-A1 Die Photograph and Die Markings



\2 Package_and_Die_Photographs_X-rays_and_Optical\
GV100-400-A1_GV100_300084_Oriented.png

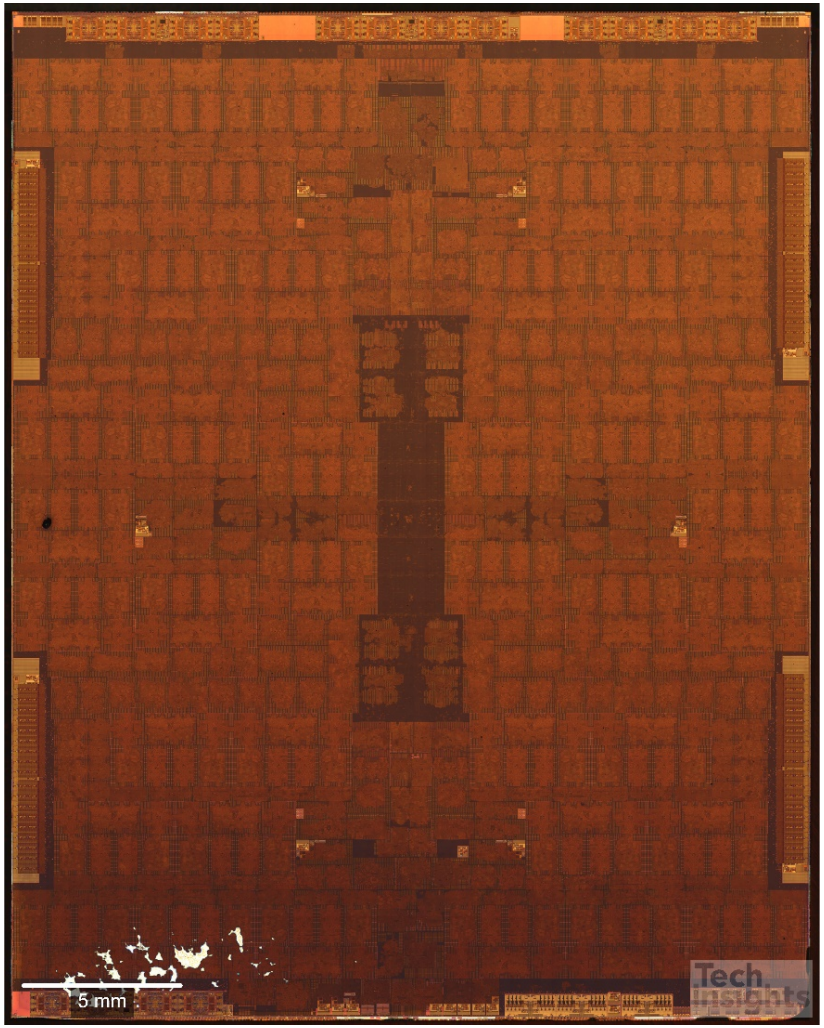
Die Photograph



\2 Package_and_Die_Photographs_X-rays_and_Optical\
GV100-400-A1_GV100_300084_DieMrk-50XRotated.png

Die Markings

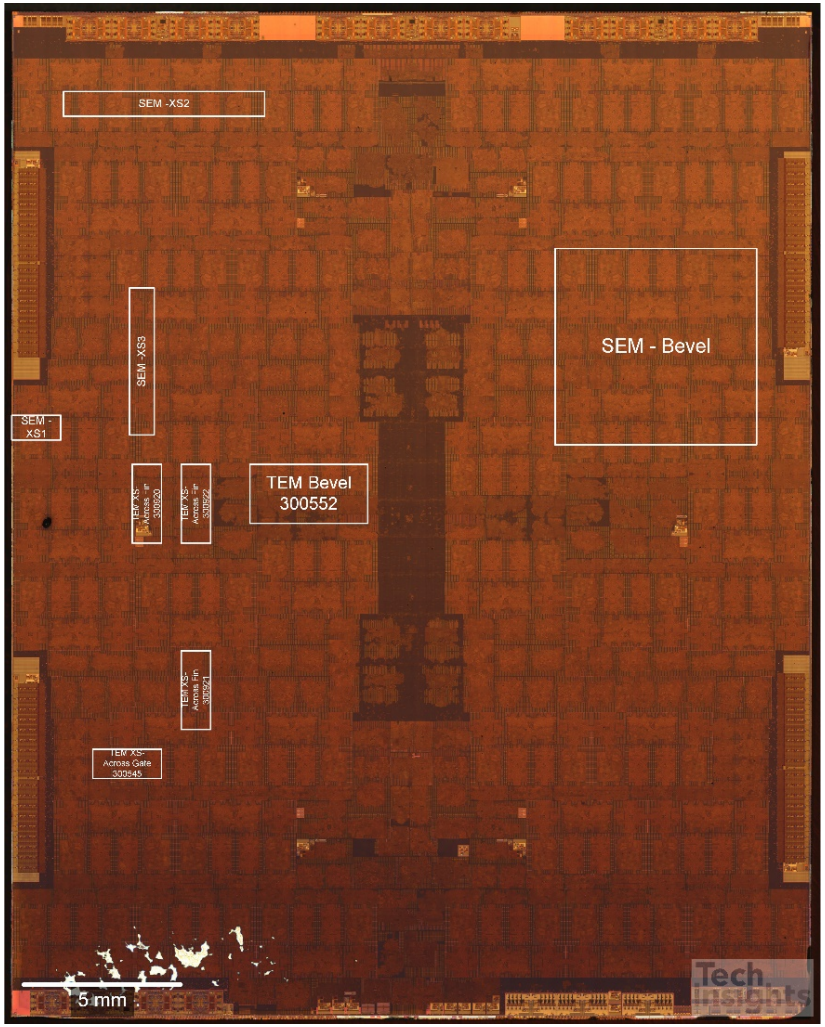
NVIDIA GV100-400-A1 Substrate Die Photograph



\2 Package_and_Die_Photographs_X-rays_and_Optical\
GV100-400-A1_GV100_300084_BPoly.png

Tech Insights

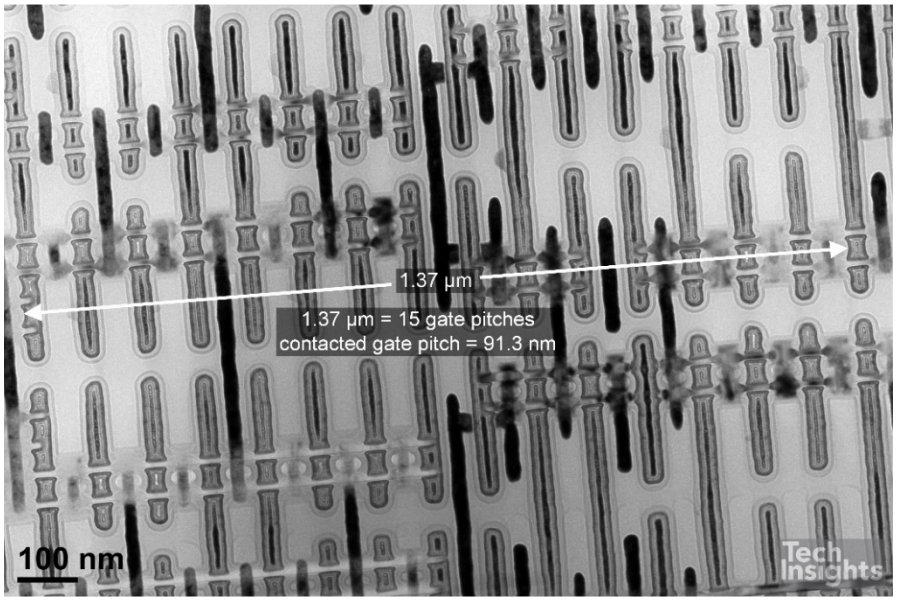
Sample Locations – TEM and SEM



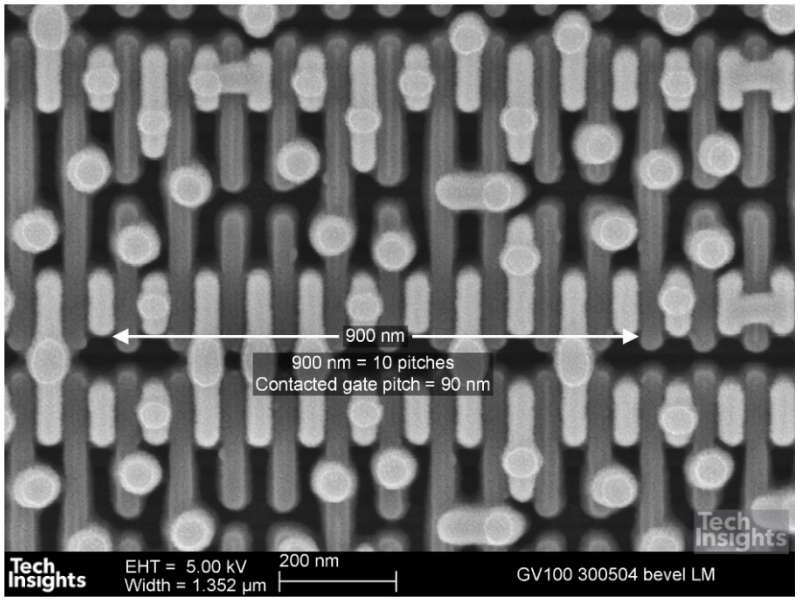
\2 Package_and_Die_Photographs_X-rays_and_Optical\
GV100-400-A1_GV100_300084_BPoly.png

Dimensional Analysis

- The logic contacted gate pitch is ~90 nm



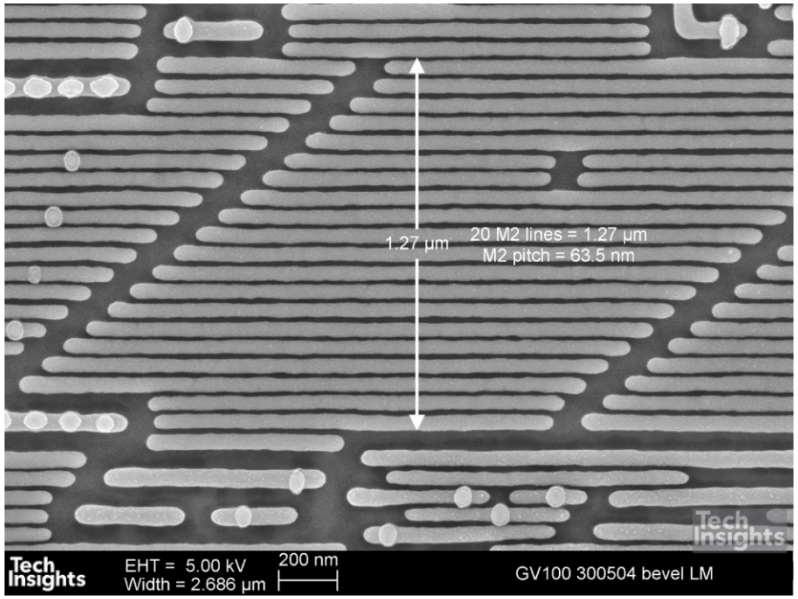
\4 TEM\Bevel\Bottom gate_17,5Kx_B_300552.png



\3 SEM\300504_bevel\406_GV100_300504_bevel_gates.png

Dimensional Analysis

- The minimum metal pitch of ~64 nm is located on the metal 2 level



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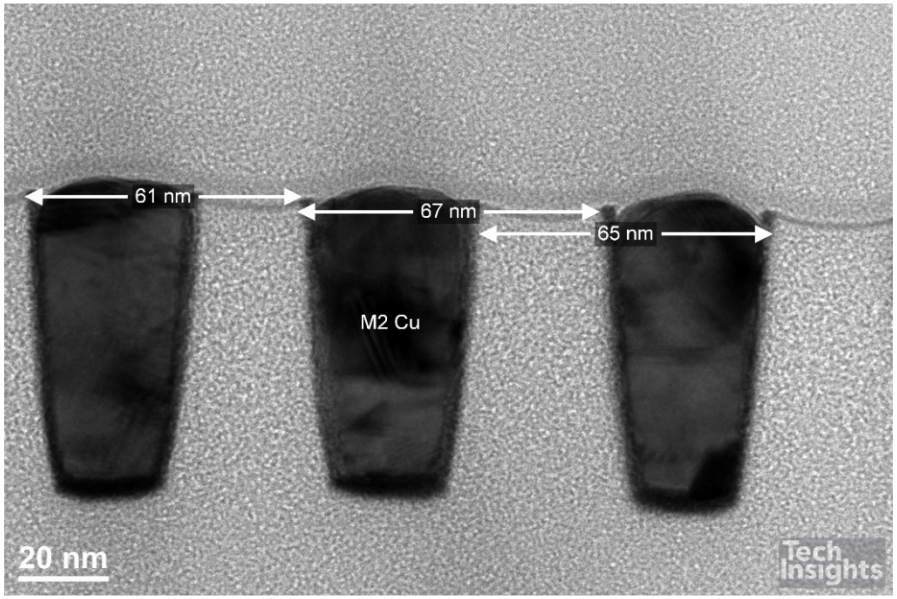
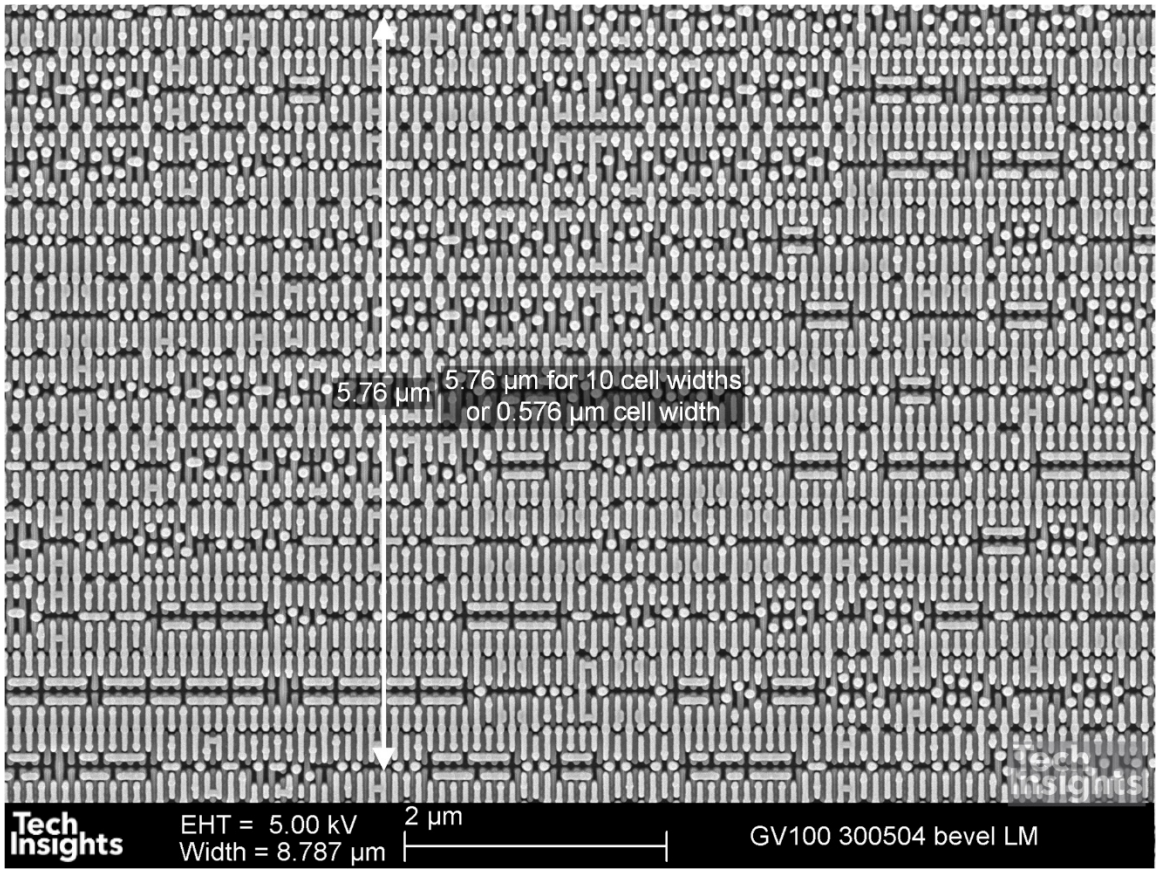


\4 TEM\XS\Interconnect\M2_130Kx_B_300922.png

Dimensional Analysis

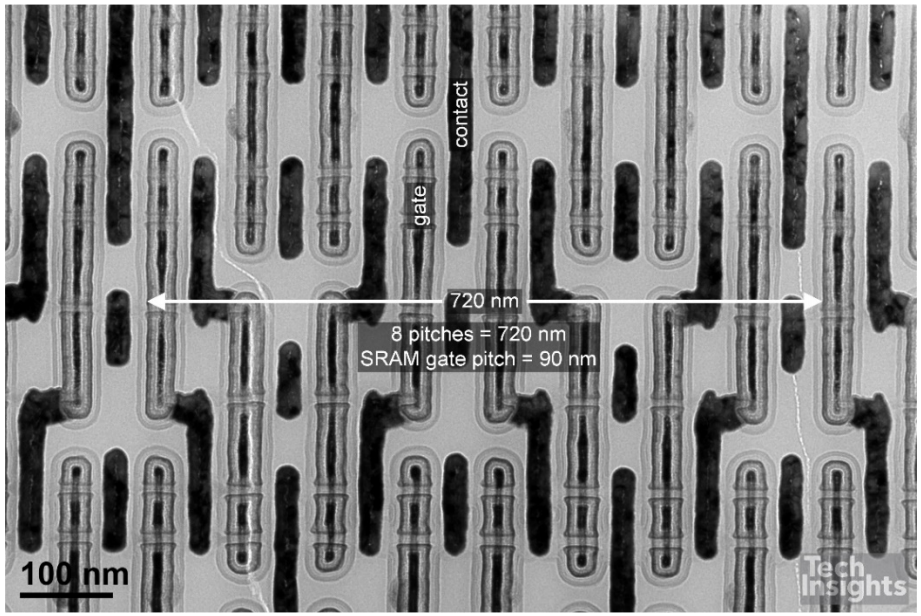
- The standard cell width is ~576 nm (equivalent to nine tracks)



\3 SEM\300504_bevel\402_GV100_300504_bevel_gates.png

Dimensional Analysis

- The SRAM contacted gate pitch is ~90 nm



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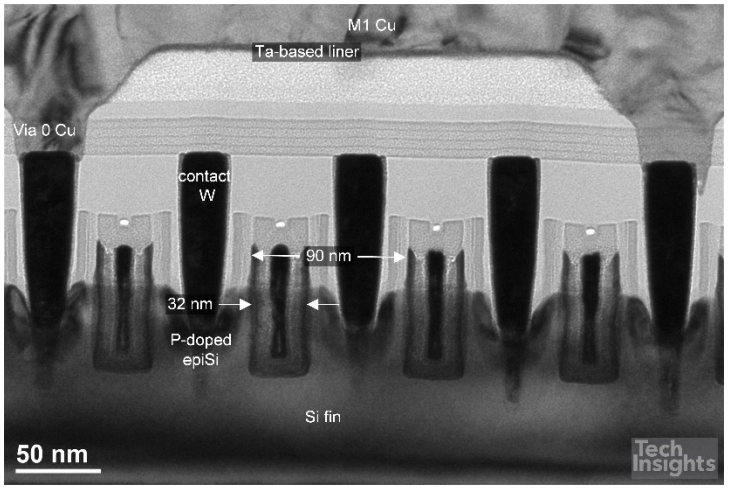
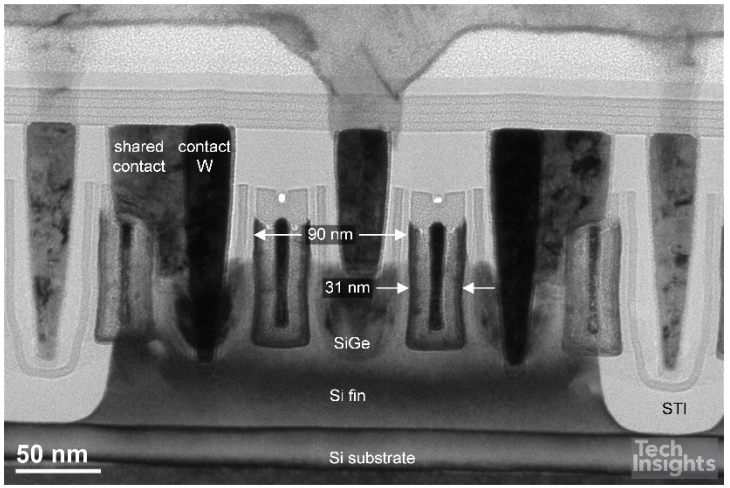


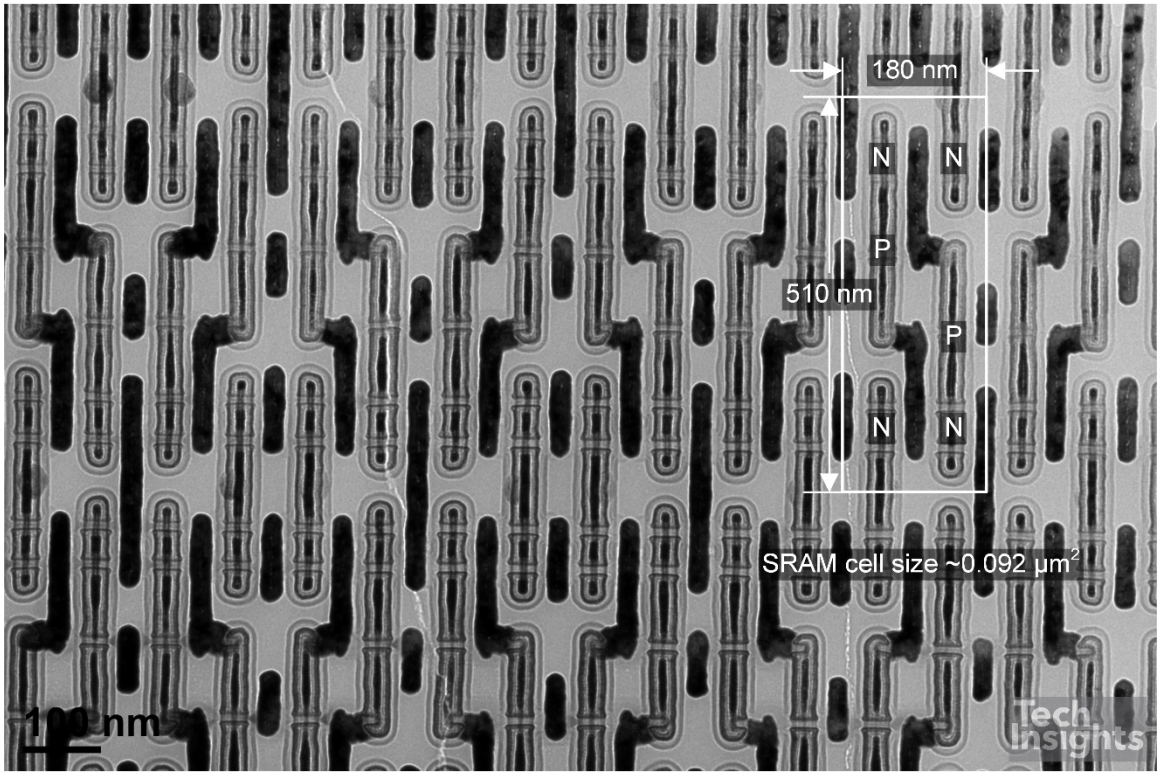
\4 TEM\XS\Across Gate\SRAM_NMOS_64Kx_300545.png



\4 TEM\XS\Across Gate\SRAM_PMOS_64Kx_300545.png

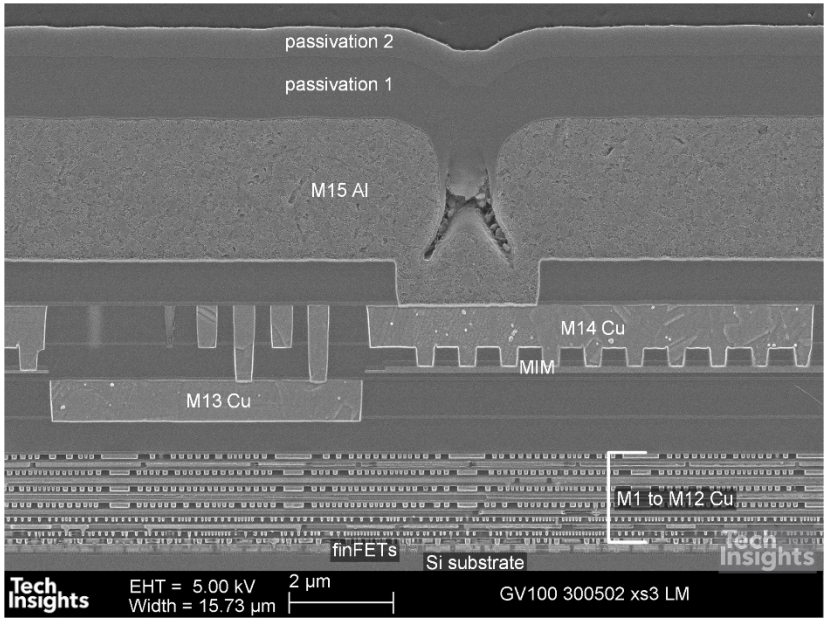
Dimensional Analysis

- The 6T SRAM cell size is ~0.092 µm^2



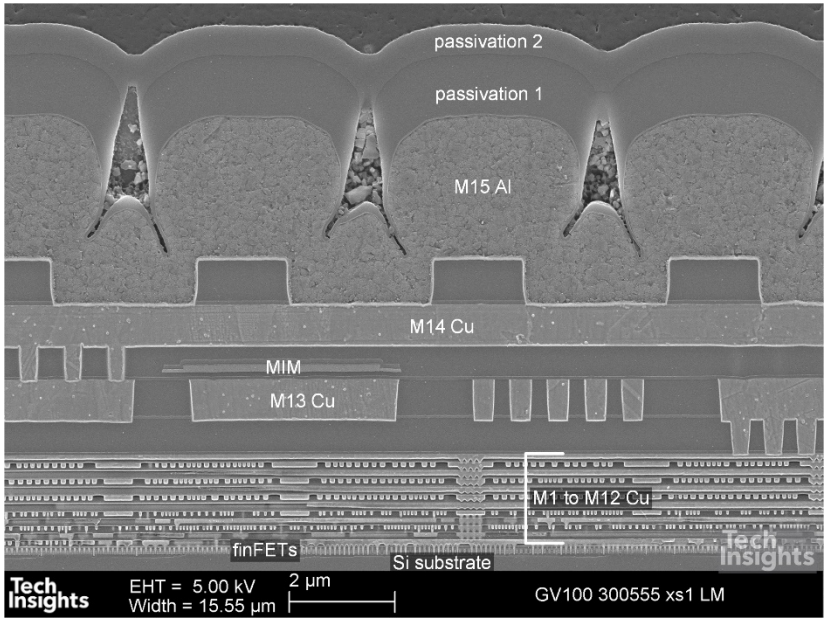
\4 TEM\Bevel\SRAM_17,5Kx_B_300552.png

General Structure – SEM



\3 SEM\300502\553_GV100_300502_xs3_logic_overview.png

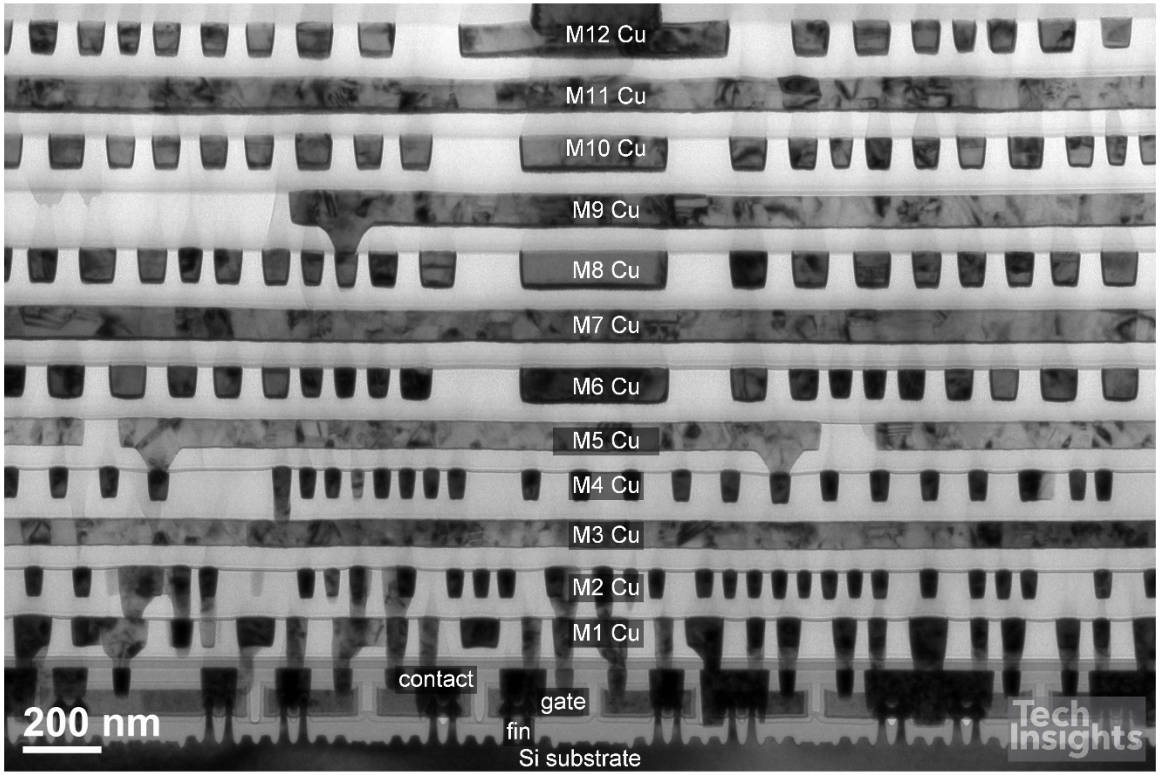
Across the Fins



\3 SEM\300555_XS_across gate\
010_GV100_300555_xs1_overview_all_layers.png

Across the Gates

General Structure – Lower Metals – TEM



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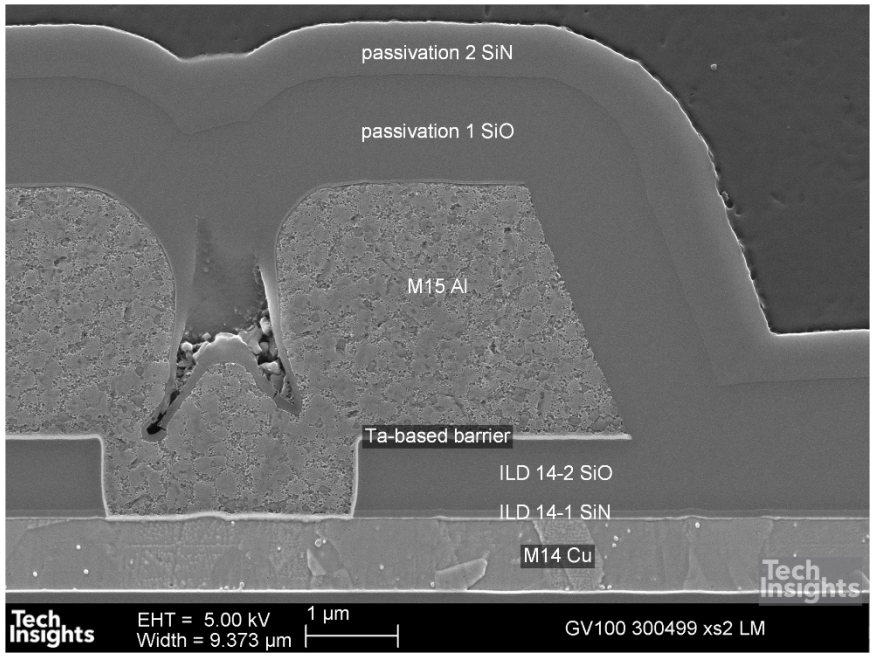
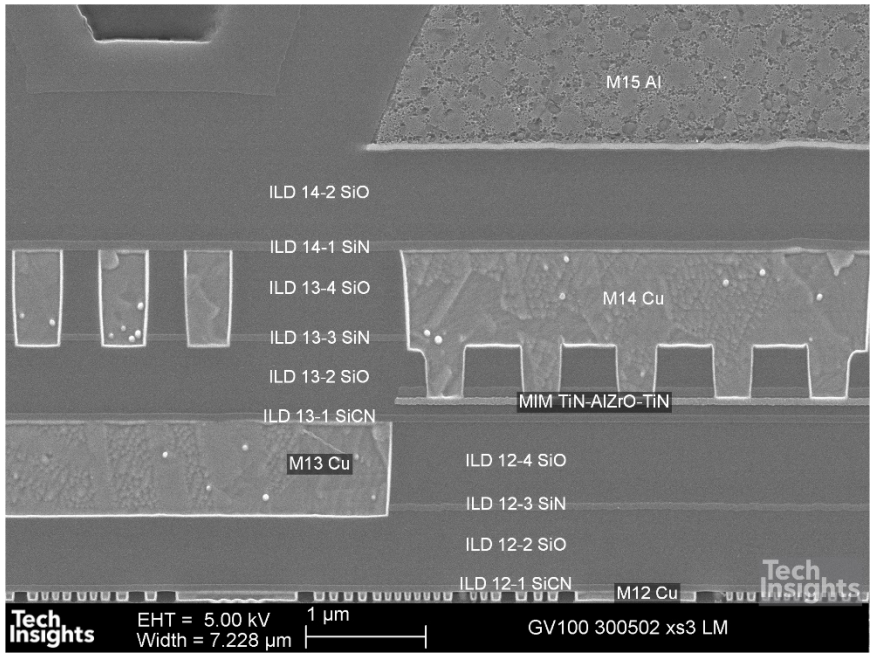
Dielectrics – Materials Analysis



\3 SEM\300499_XS_across_gate\ 414_GV100_300499_xs2_logic_passivation.png

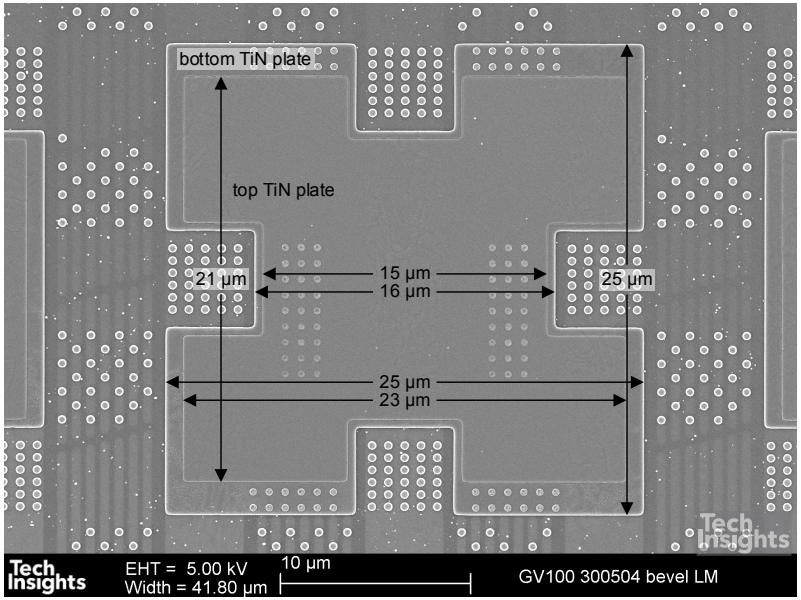
Metal 15



\3 SEM\300502\558_GV100_300502_xs3_logic_ILD_upper.png

Metal 13 and Metal 14

Dielectrics – Materials Analysis – MIM Capacitor



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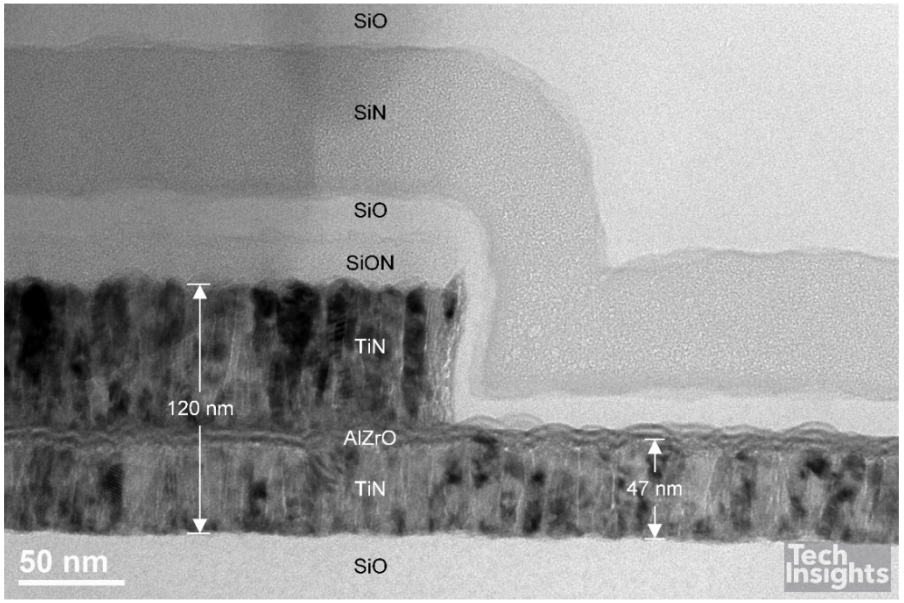
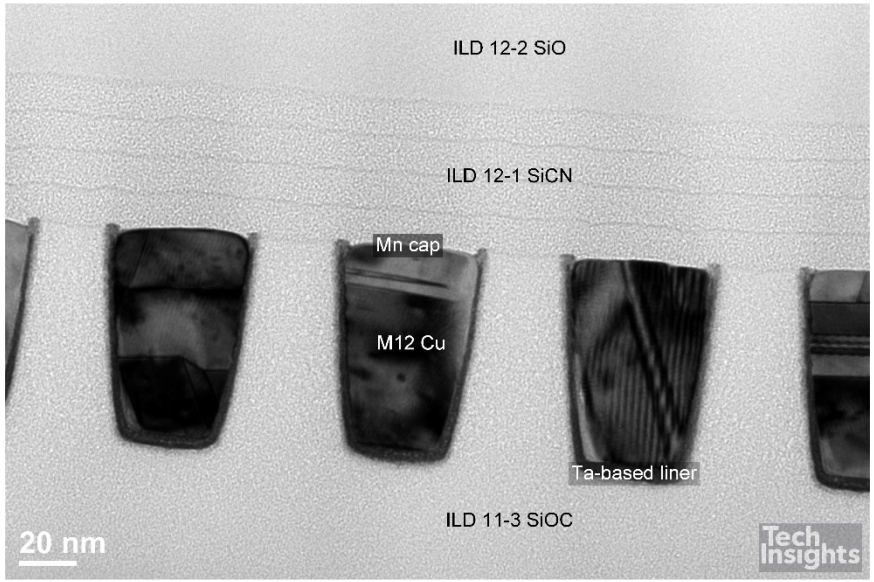


\4 TEM\XS\Interconnect\MIM_64Kx_B_300922.png

Dielectrics – Materials Analysis



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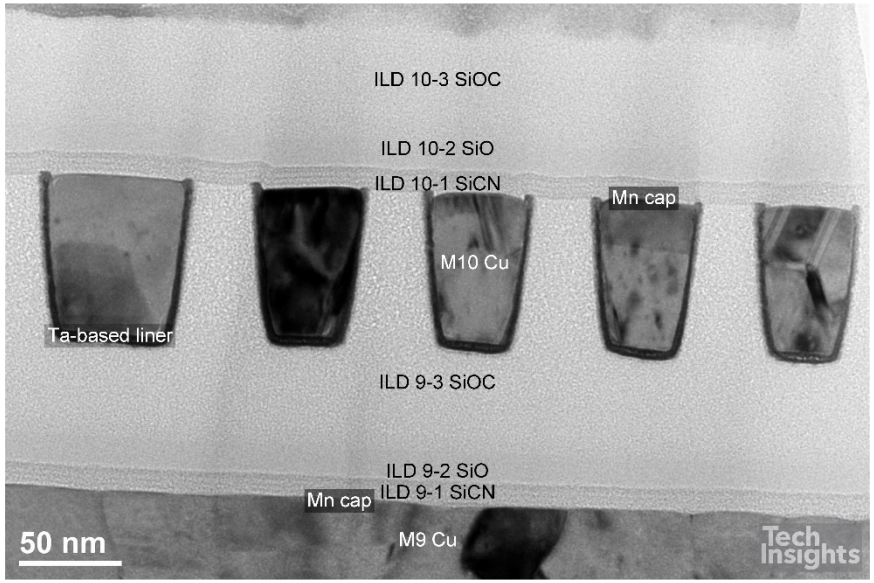
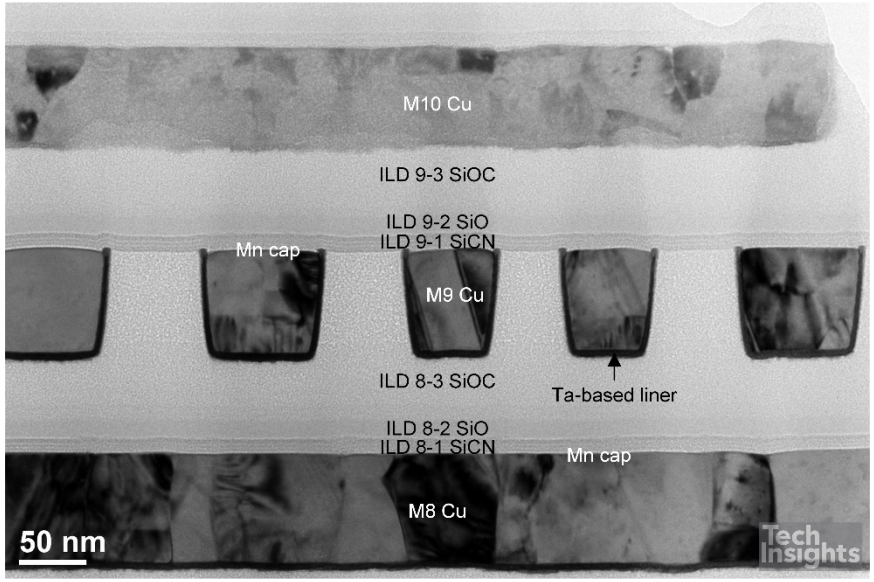
Metal 12



\4 TEM\XS\Interconnect\M10_64Kx_300922.png

Metal 10

Dielectrics – Materials Analysis



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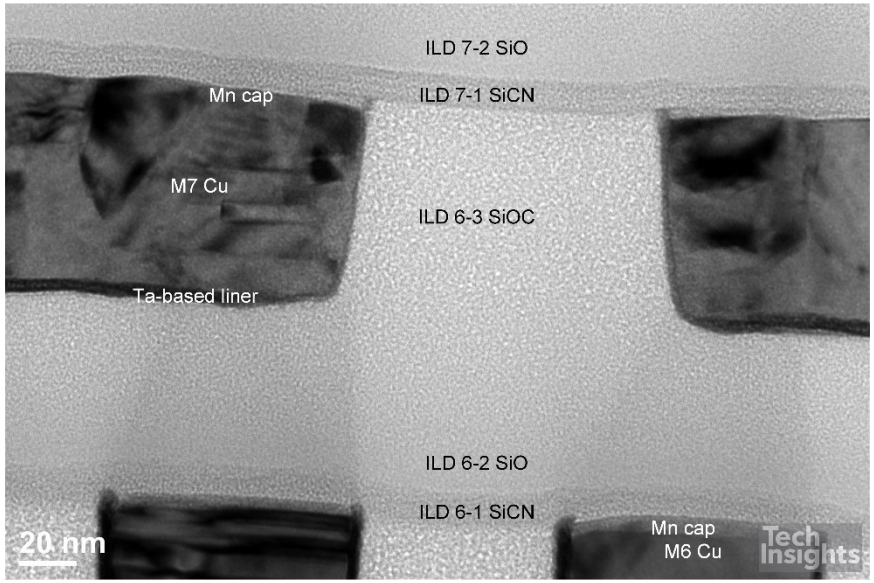
Metal 9



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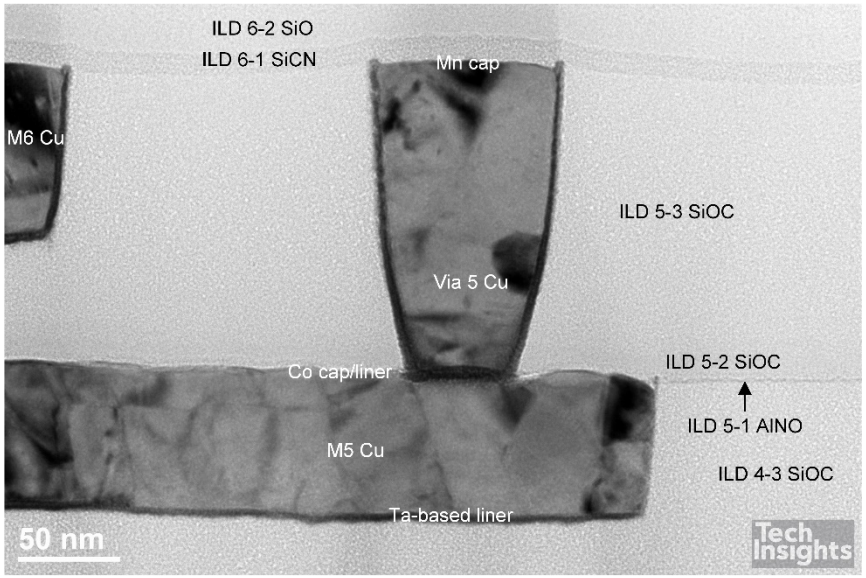
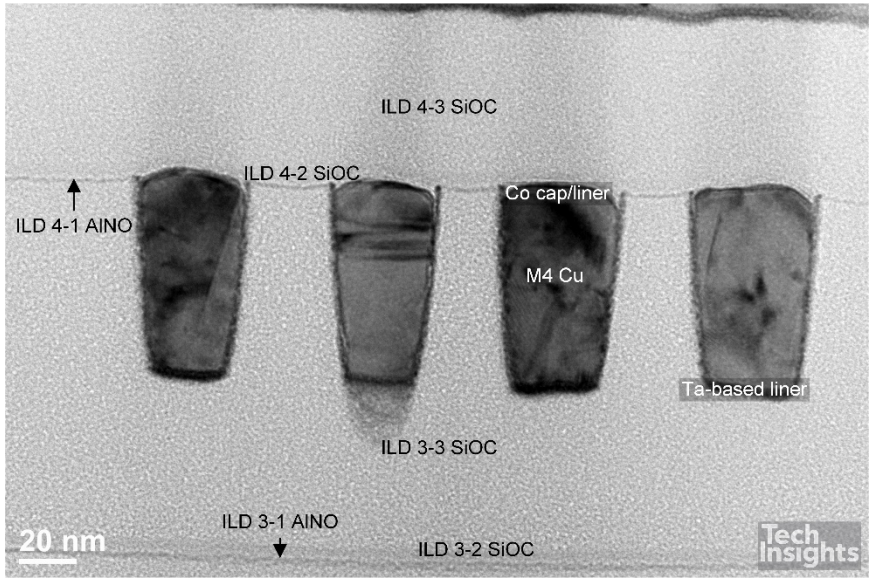
Metal 7

Dielectrics – Materials Analysis



\4 TEM\XS\Interconnect\M5-Via5-M6_64Kx_300922.png

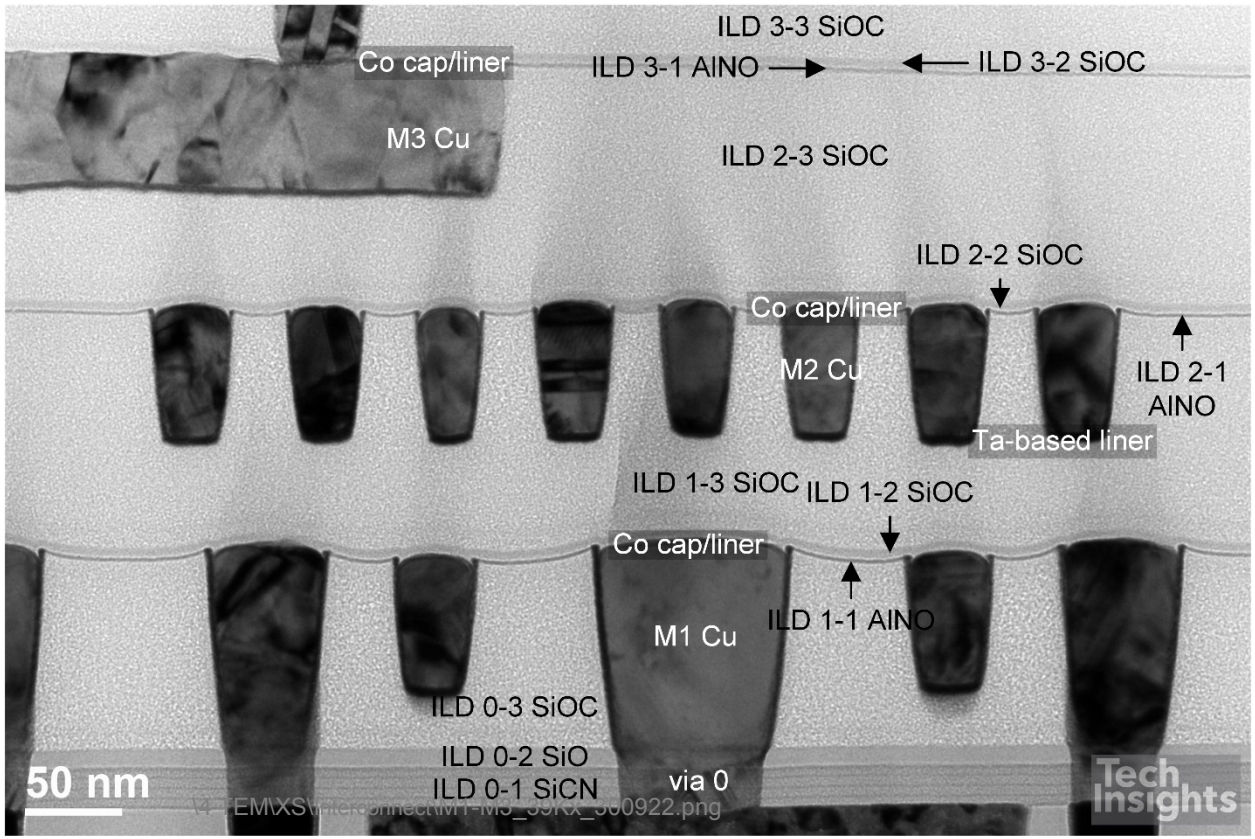
Metal 5 and Metal 6



\4 TEM\XS\Interconnect\M4_88Kx_B_300922.png

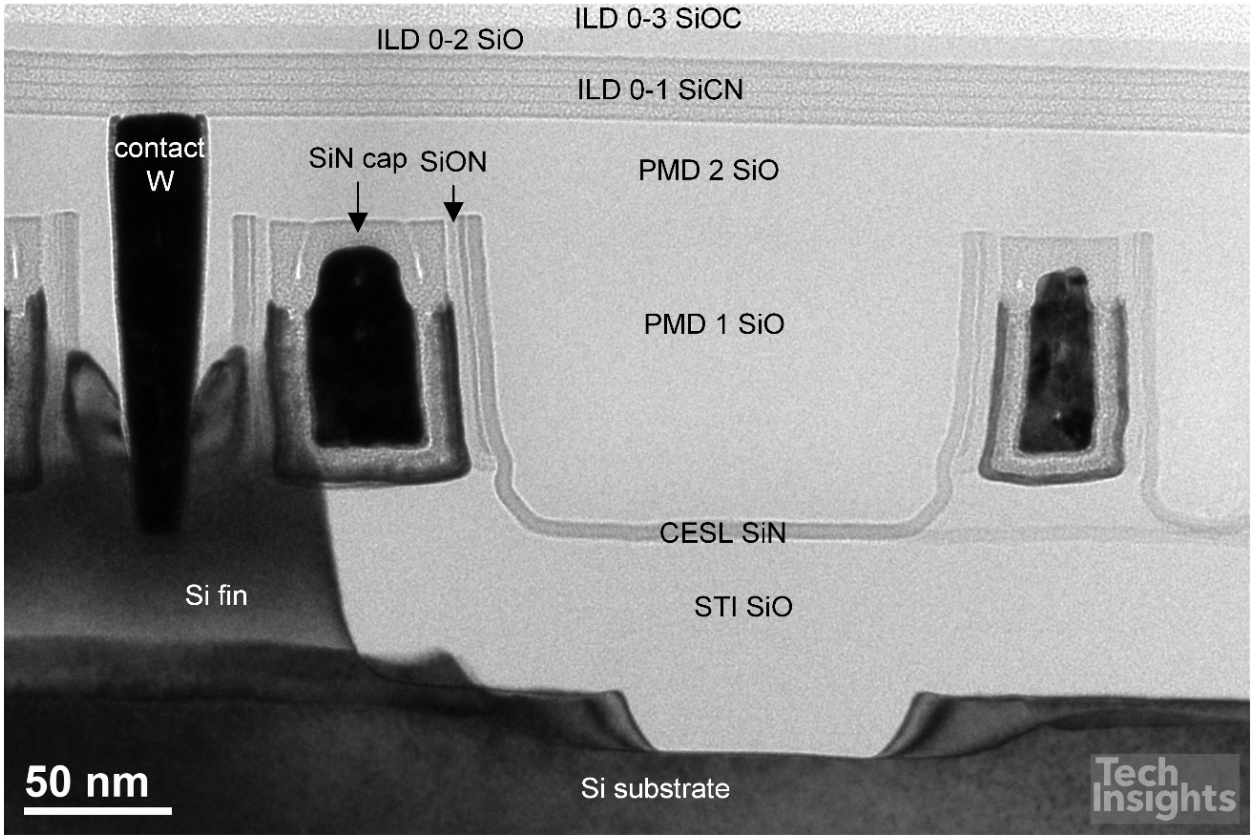
Metal 4

Dielectrics – Materials Analysis



Metal 1 to Metal 3

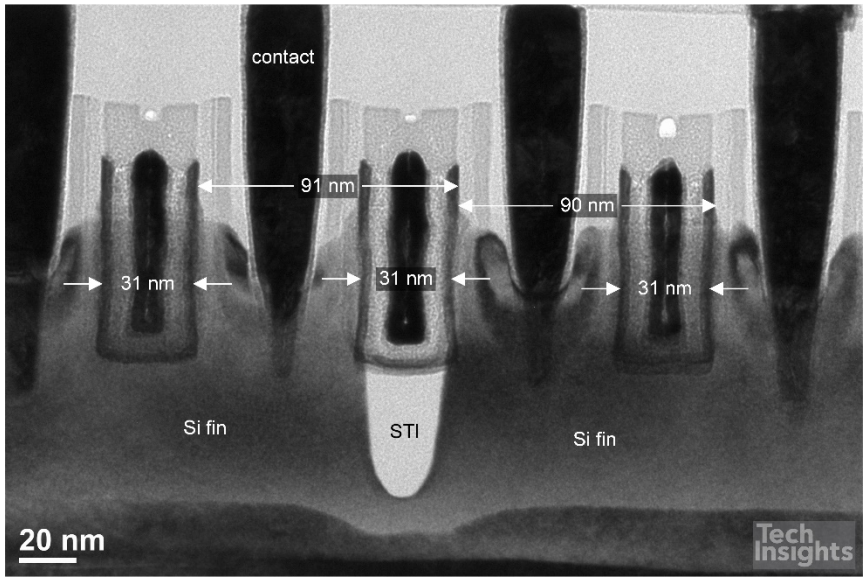
Dielectrics – Materials Analysis



\4 TEM\XS\Across Gate\SRAM_PMOS_edge_64Kx_300545.png

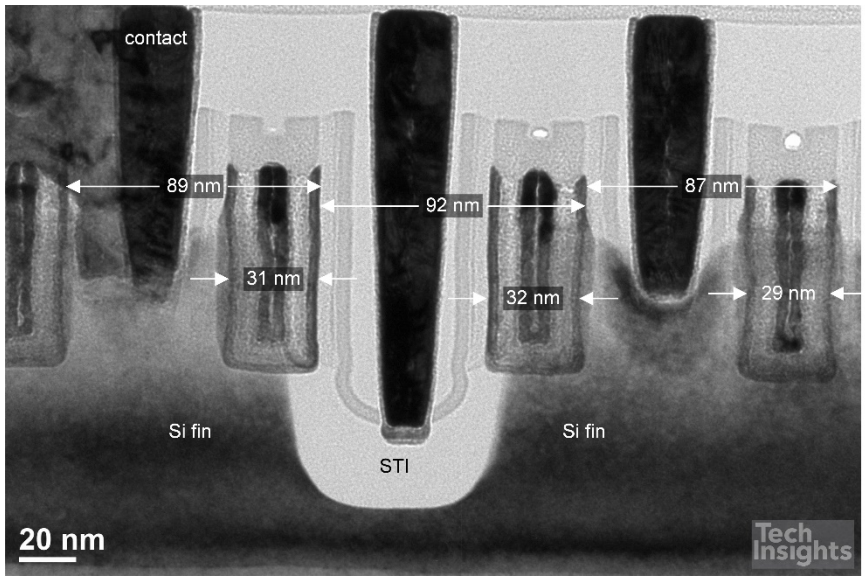
PMD

Logic – Single and Double Diffusion Breaks



\4 TEM\XS\Across Gate\NMOS_singlediffbreak_88Kx_300545.png

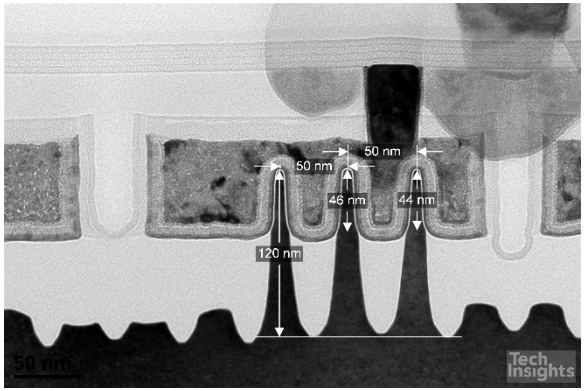
SDB



\4 TEM\XS\Across Gate\Dummy contact_88Kx_300545.png

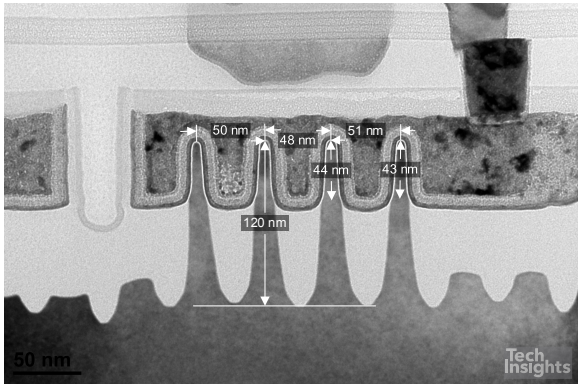
DDB

Logic – Three and Four Fins



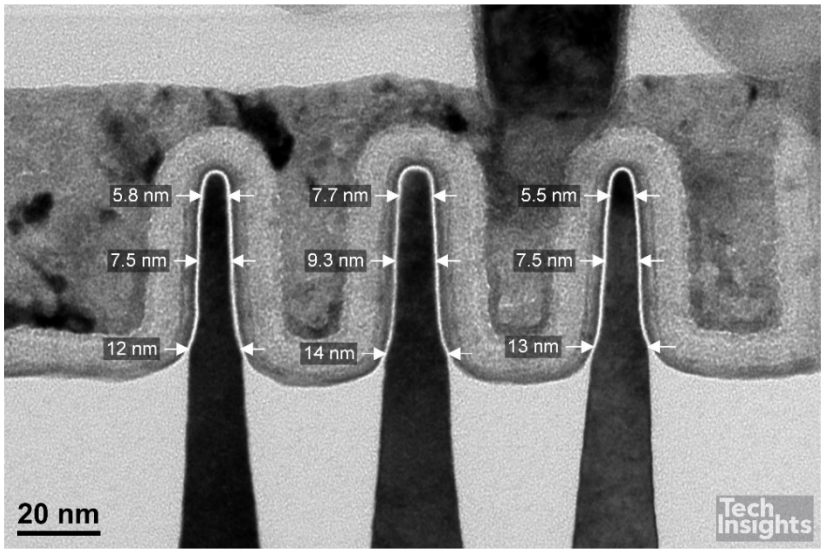
\4 TEM\XS\Across Fin\Three fins_N_64Kx_300920.png

Three Fins

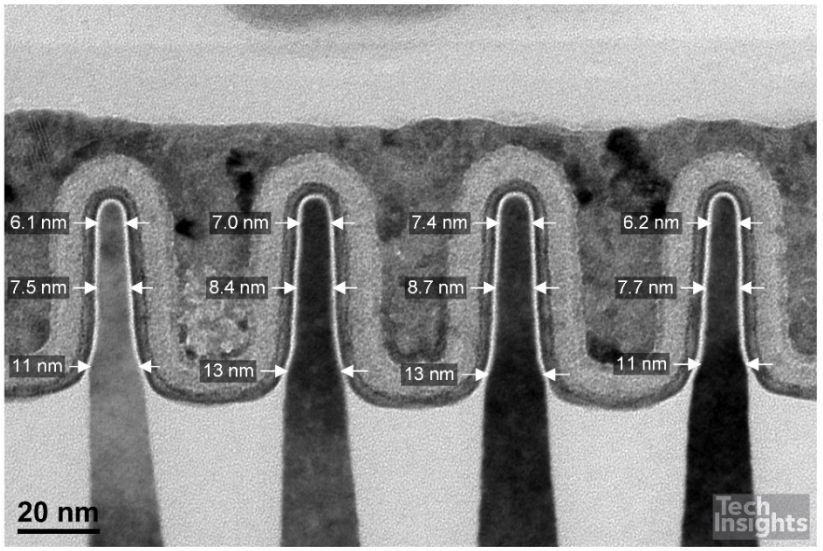


\4 TEM\XS\Across Fin\Four fins_N_64Kx_300920.png

Four Fins

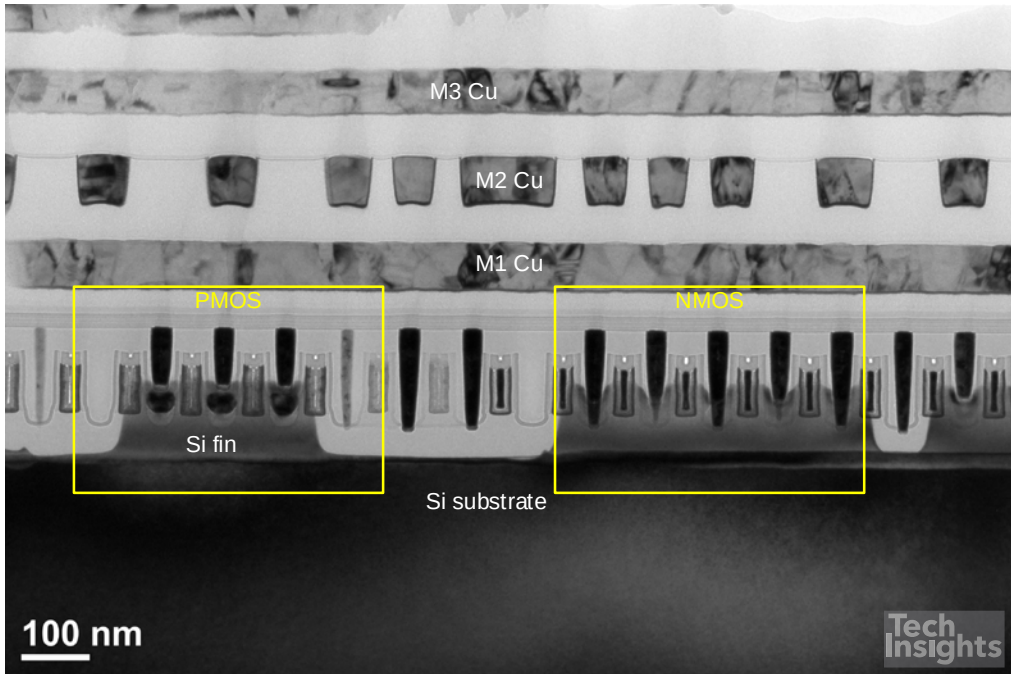


\4 TEM\XS\Across Fin\Three fins_N_130Kx_300920.png



\4 TEM\XS\Across Fin\Four fins_N_130Kx_300920.png

Logic PMOS and NMOS – Across the Gate



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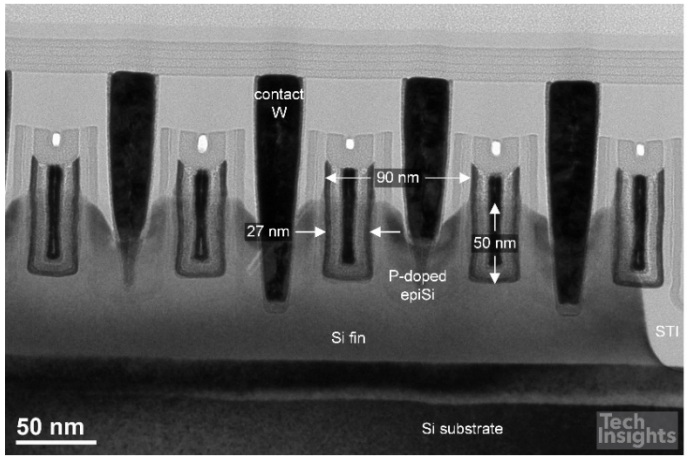
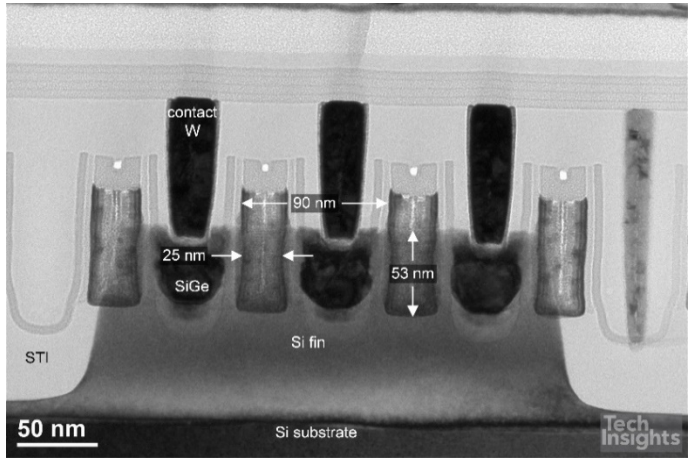


\4 TEM\XS\Across Gate\NMOS_2_64Kx_300545.png

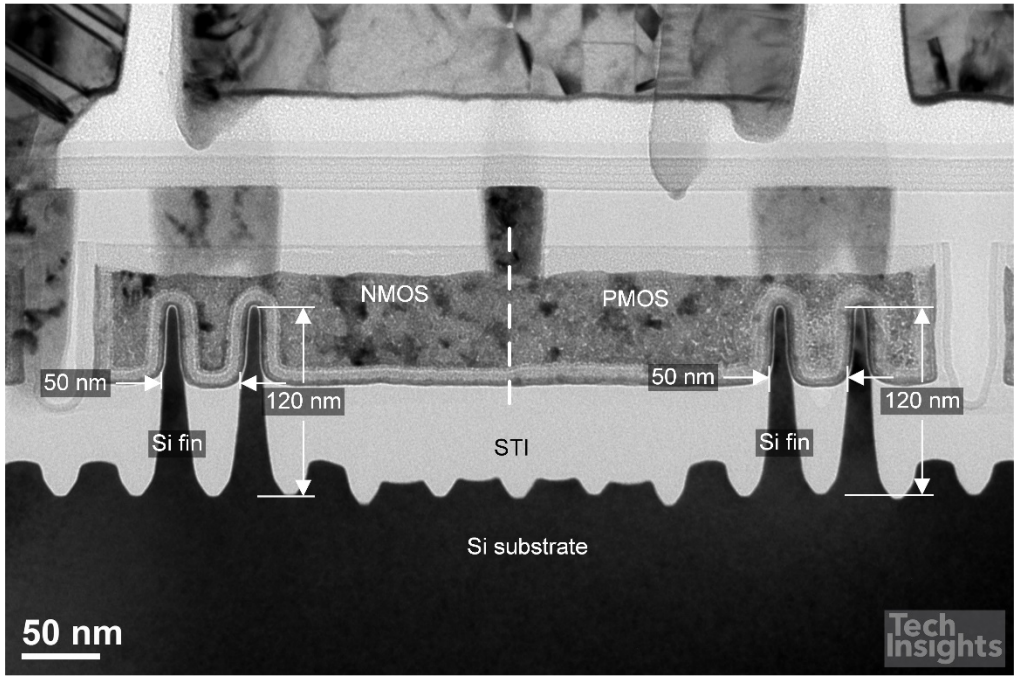
NMOS



\4 TEM\XS\Across Gate\PMOS_64Kx_300545.png

PMOS

Logic PMOS and NMOS – Across the Fins



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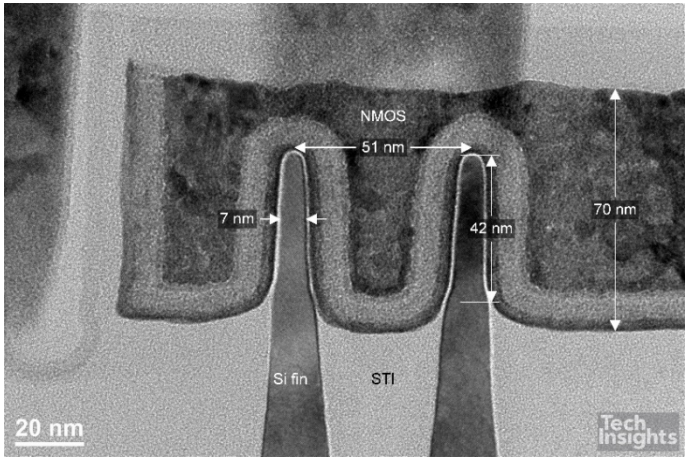
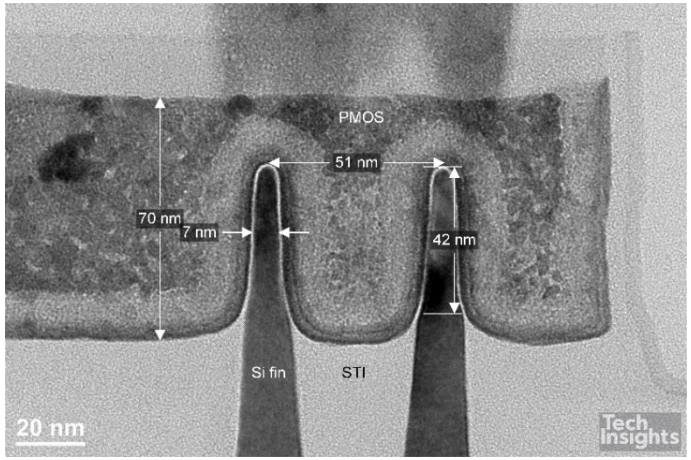


\4 TEM\XS\Across Fin\ NMOS_130Kx_300922.png

NMOS



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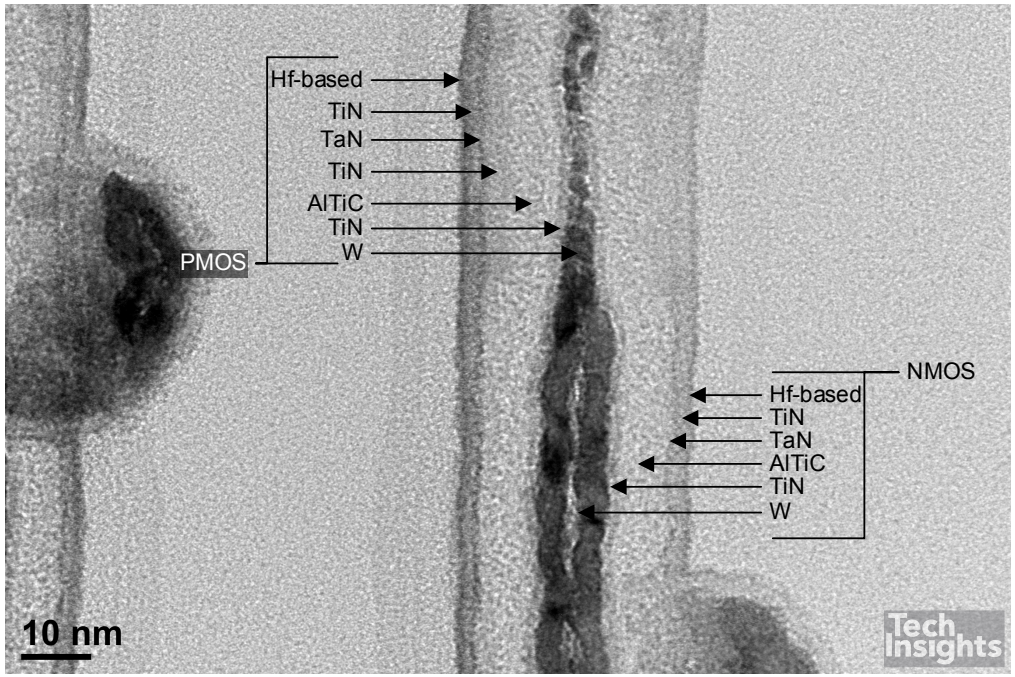
PMOS

Transition Between PMOS and NMOS



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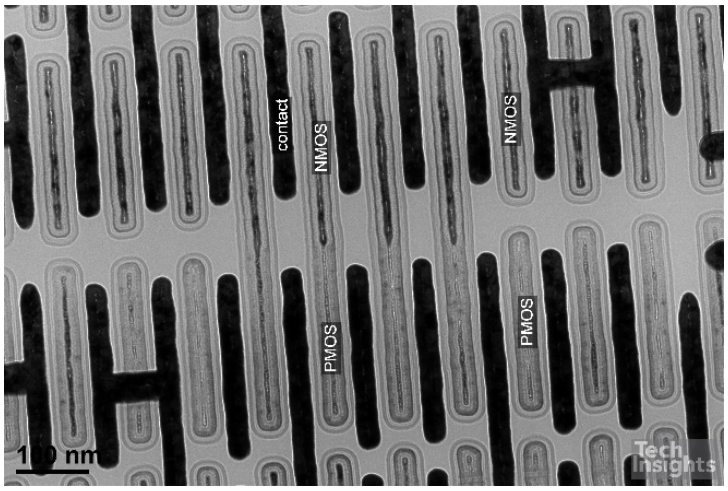

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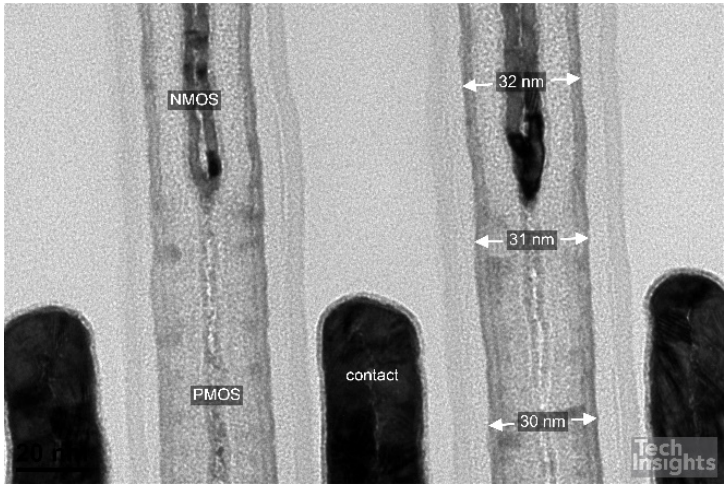
NMOS



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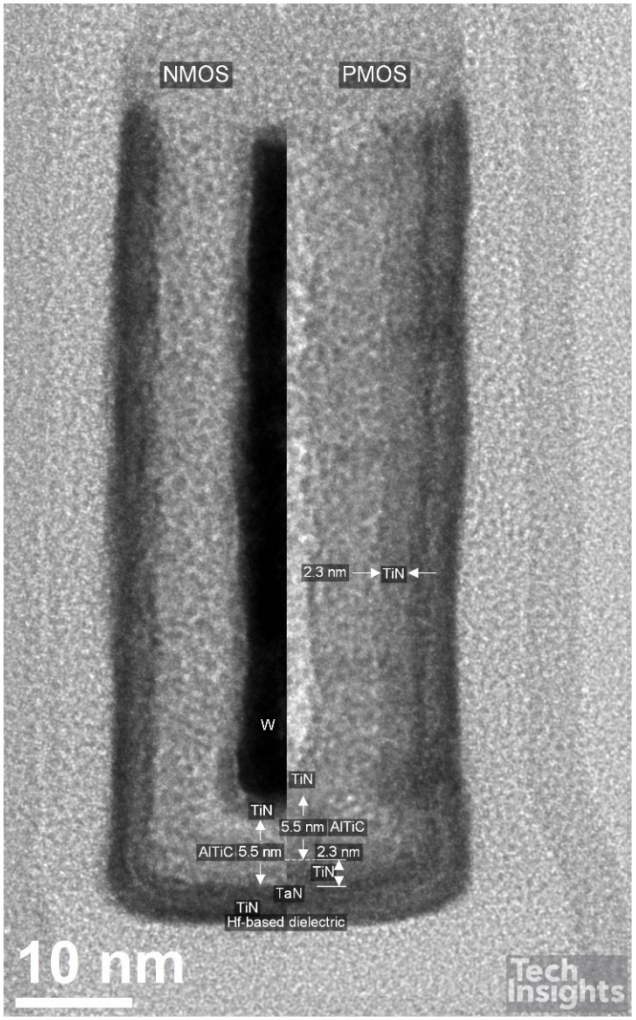
PMOS

Transition Between PMOS and NMOS



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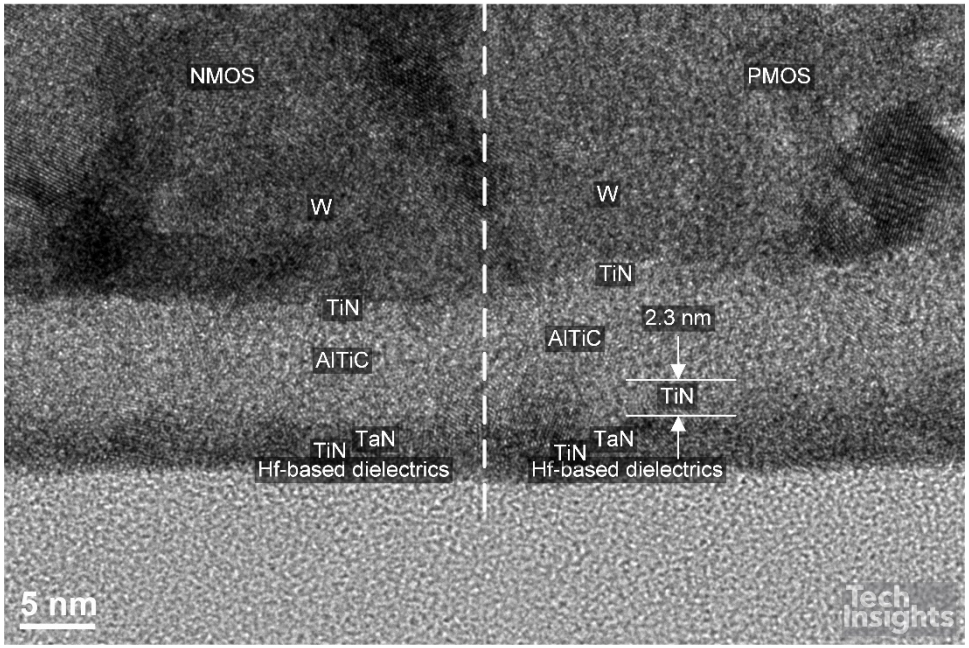

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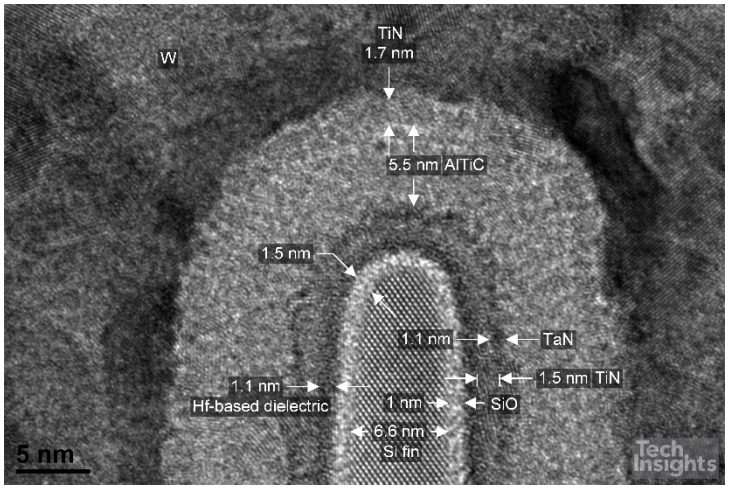
Source and Drain – NMOS and PMOS



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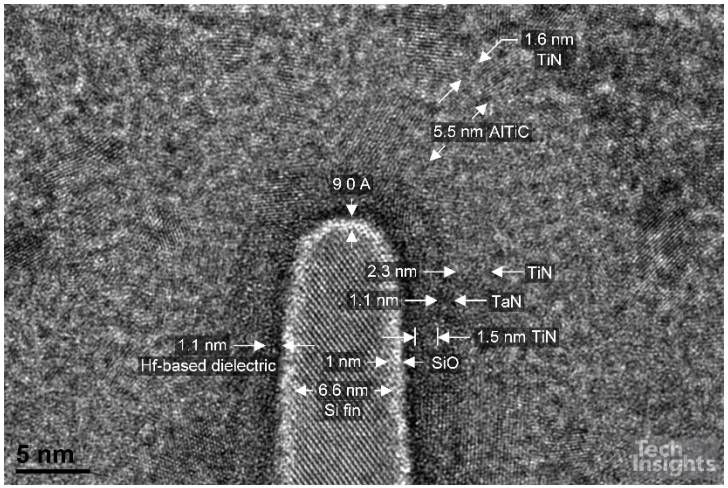
NMOS Cross Section



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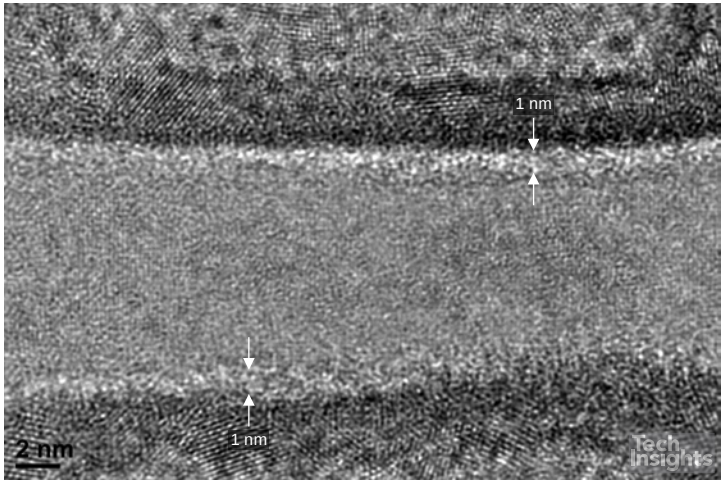
PMOS Cross Section



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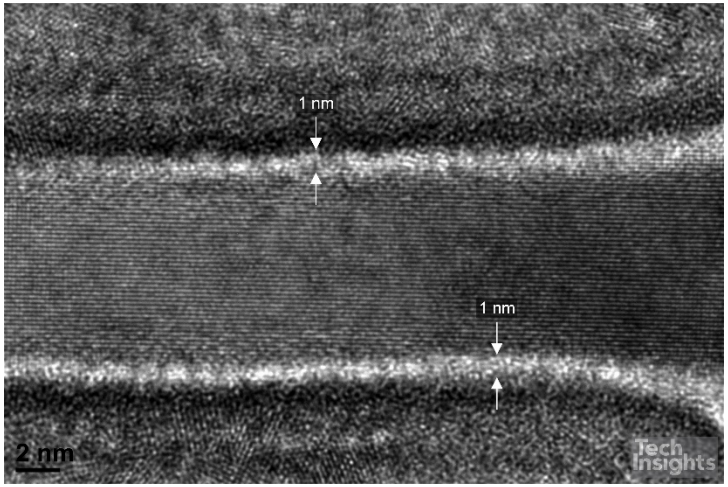
NMOS Planar



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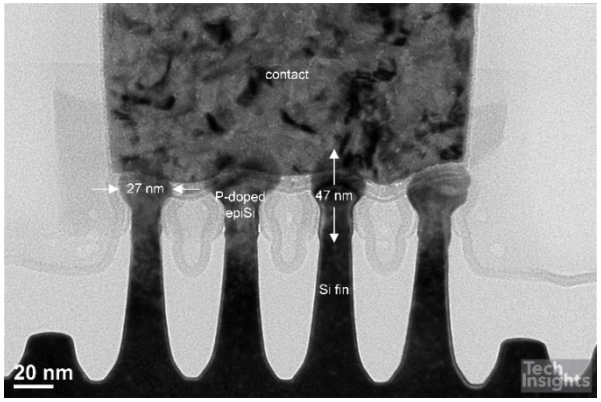
PMOS Planar

Source and Drain – NMOS



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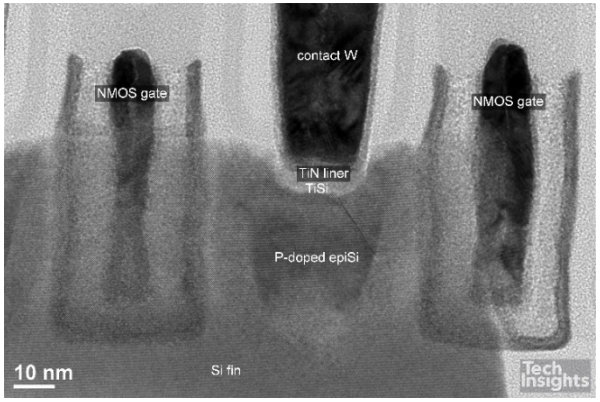

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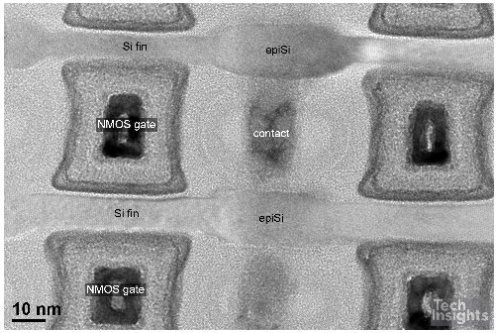

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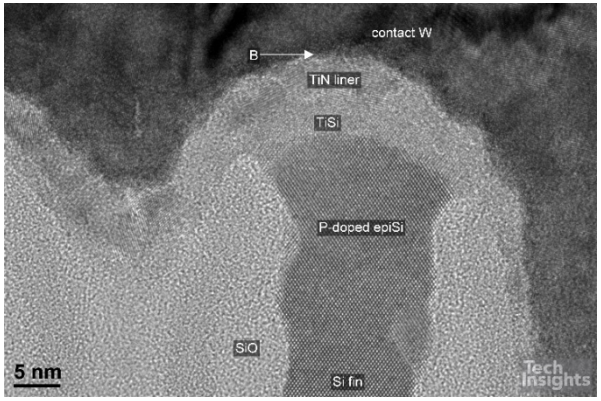

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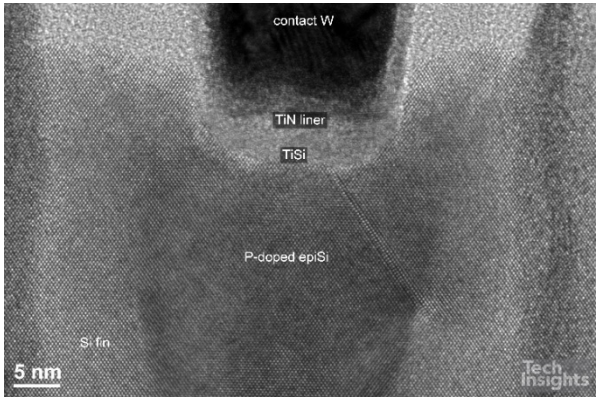

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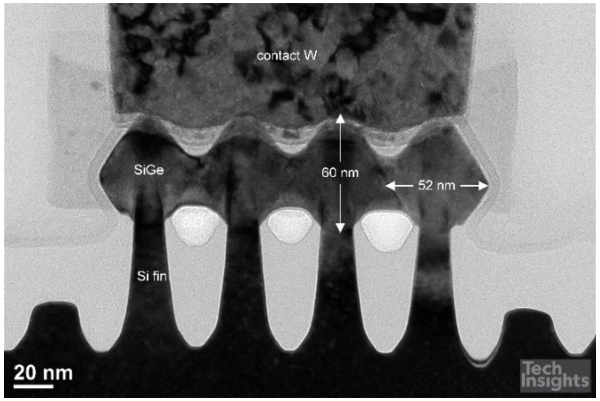
Source and Drain – PMOS



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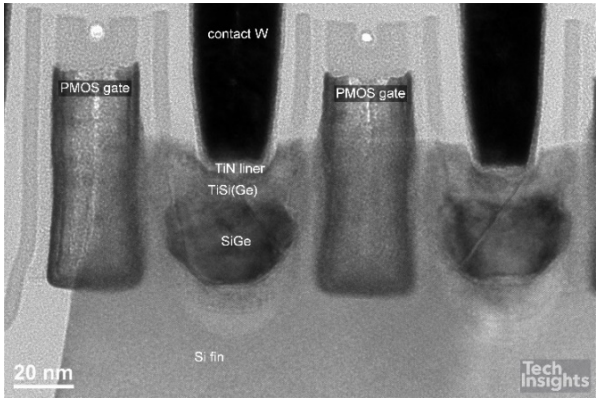

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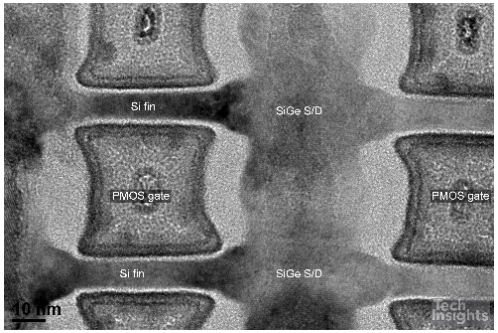

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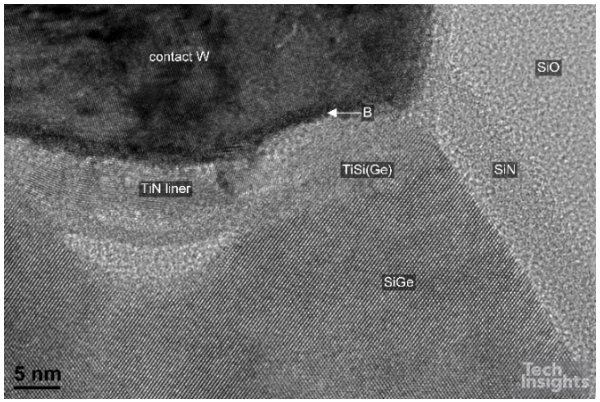

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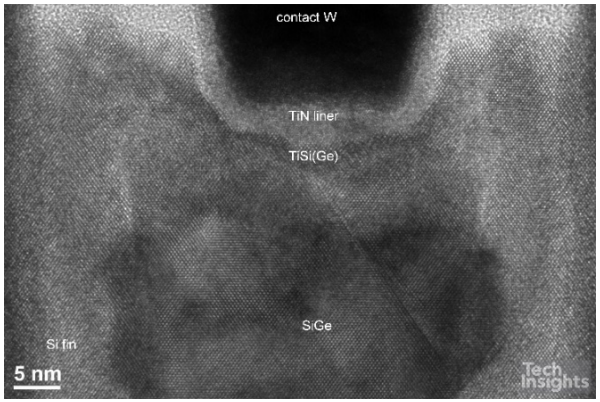

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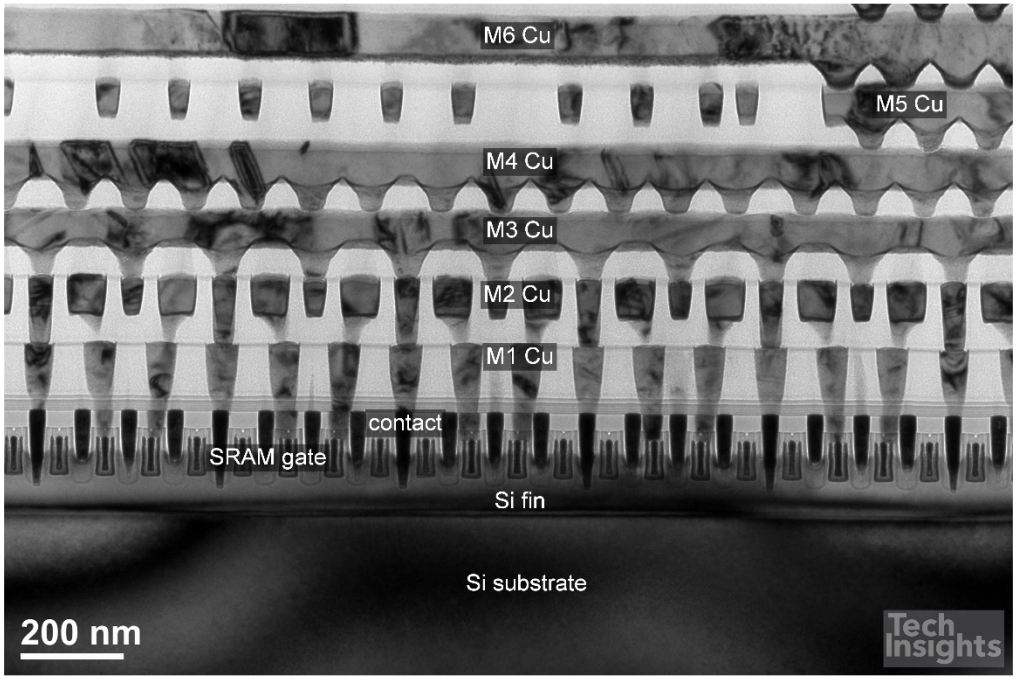
SRAM PMOS and NMOS – Across the Gate



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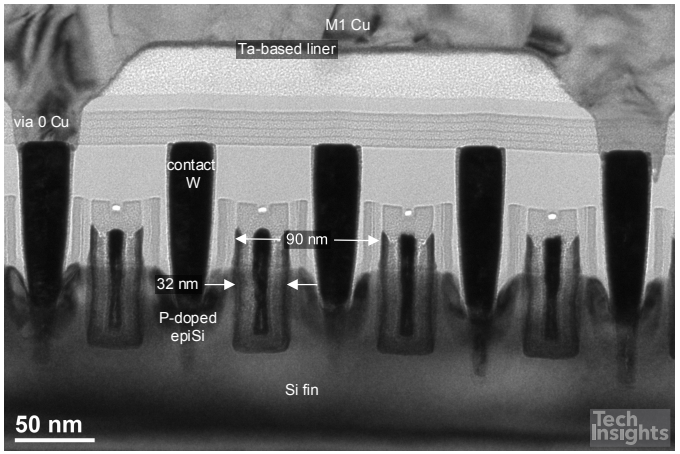

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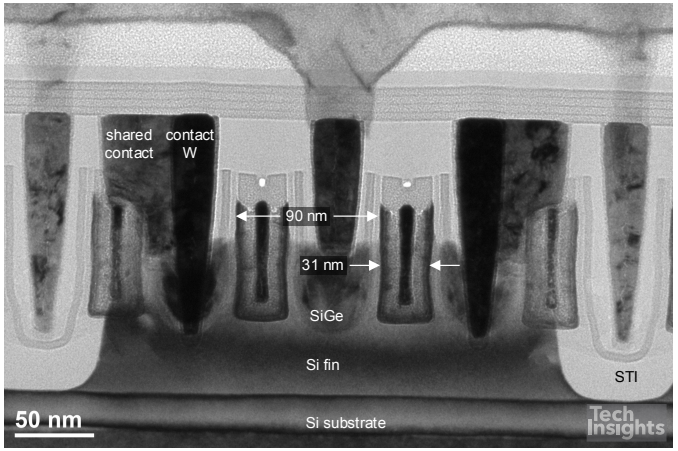
NMOS



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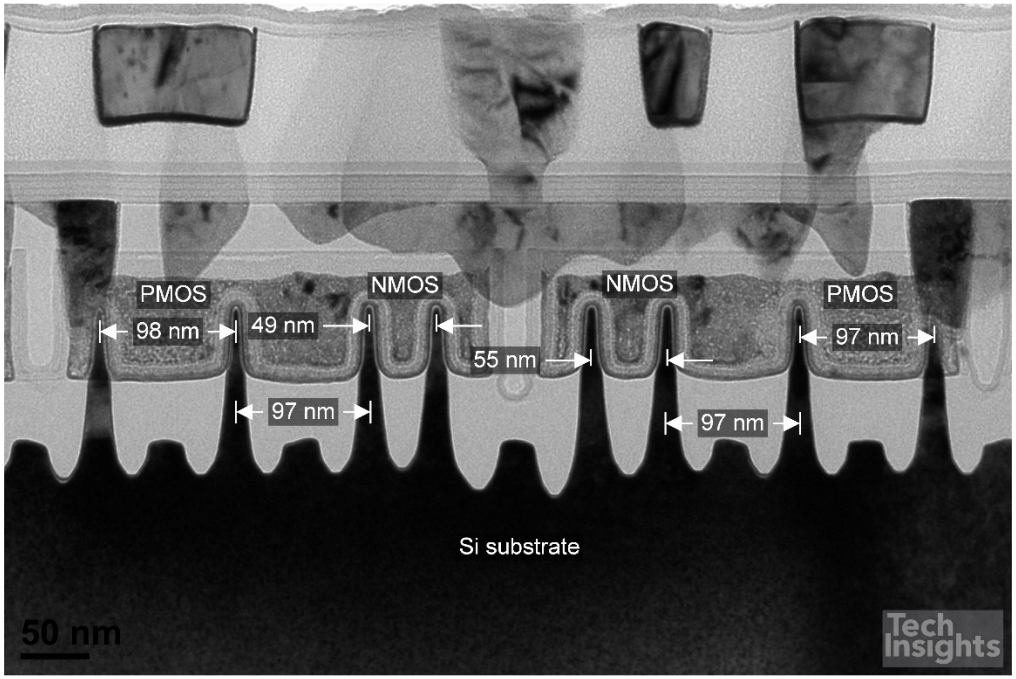
PMOS

SRAM PMOS and NMOS – Across the Fins



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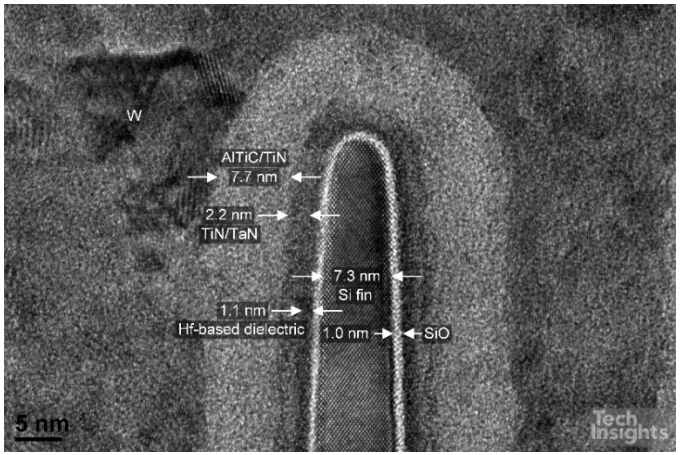
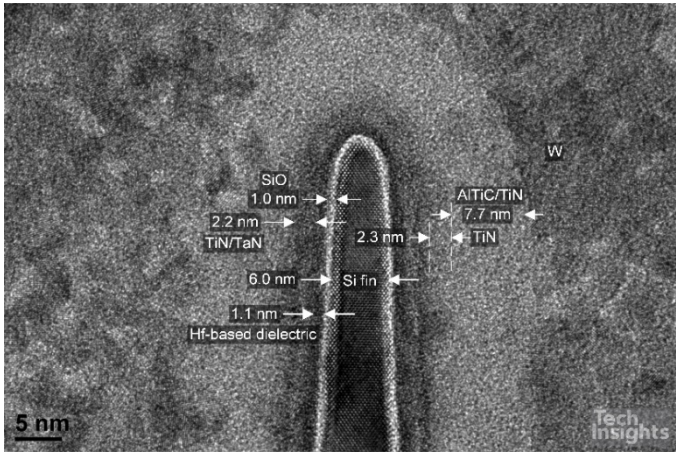


\4 TEM\XS\Across Fin\SRAM-NMOS_360Kx_300920.png

PMOS



\4 TEM\XS\Across Fin\SRAM-PMOS_360Kx_300920.png

NMOS

NMOS and PMOS Gate and Epi Dimensions

NMOS

Structure	Size (nm)
Gate length	~27
NMOS gate fill thickness (TiN)	~1.7
NMOS WF metal (AlTiC) thickness	~5.5
NMOS TiN/TaN cap thickness	1.5/1.1
NMOS logic gate dielectric thickness (Hf-based dielectric/SiO_2)	~2.1 (1.1/1.0)
NMOS source/drain Si epi thickness/width	~47/27

PMOS

Structure	Size (nm)
Gate length	~25
PMOS gate fill thickness (AlTiC/TiN)	~7.1 (5.5/1.6)
PMOS WF metal (TiN) thickness	~2.3
PMOS TiN/TaN cap thickness	1.5/1.1
PMOS logic gate dielectric thickness (Hf-based dielectric/SiO_2)	~2.1 (1.1/1.0)
PMOS source/drain SiGe epi thickness/width	~60/52

Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm (± 1.4%) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within ± 2% of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a stage micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of 0.3 µm (0.3%) for the stage micrometer's 100 µm pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately ± 5% or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis is usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports.

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