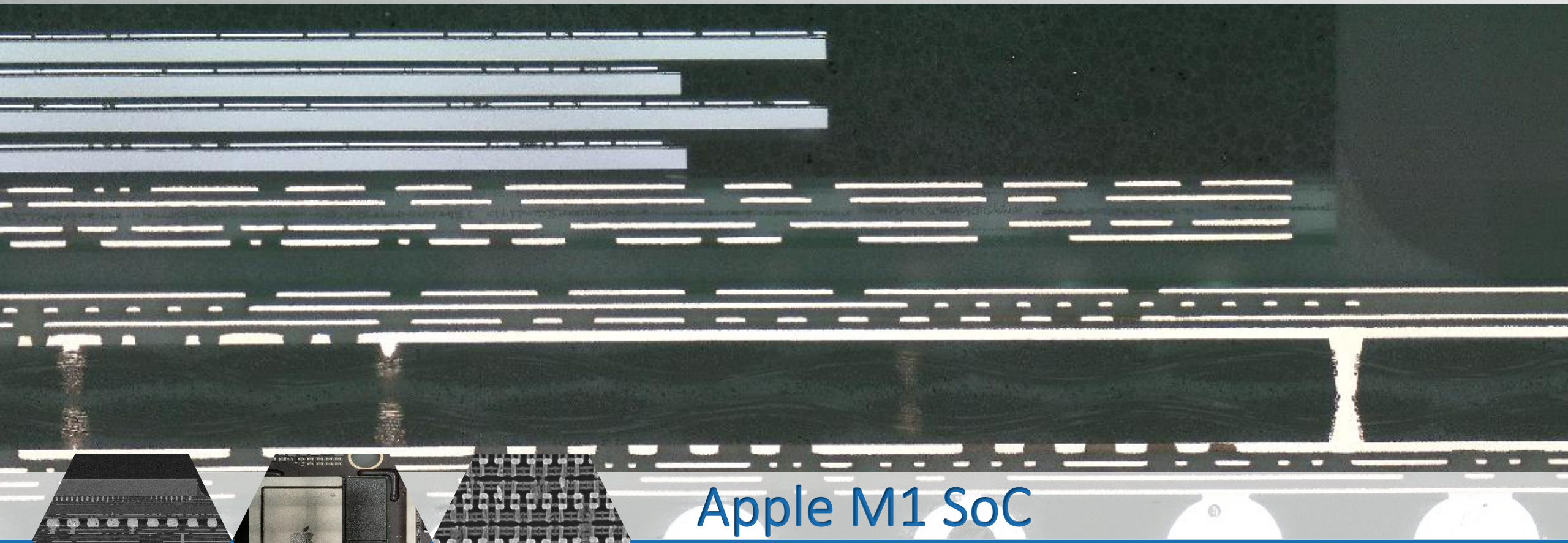

Apple M1 SoC

The Apple's first ARM based processor for Personal Computing

SP20608 - IC report by Belinda Dube, Stéphane Elisabeth and Don Scansen
PHYSICAL ANALYSIS done by Véronique Le Troadec and Don Scansen

December 2020

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Versions of the Report

Version	Date	Updates
Preliminary	17/12/2020	○ Initial release of preliminary report
Technology Analysis	31/12/2020	○ Initial release of Technology Analysis report
Full Report V1	15/01/2021	○ Initial release of Technology Analysis & Cost Analysis Report

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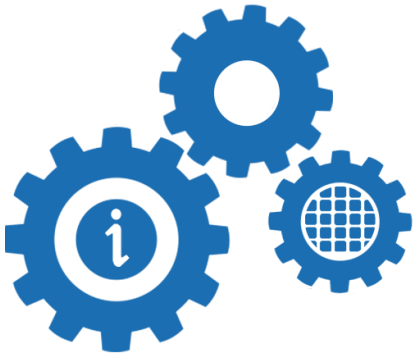


OVERVIEW
METHODOLOGY

Executive Summary

This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the Apple M1 System-on-Chip (SoC).

Back in 2010, Apple managed to get ride of Samsung's Processor to use its own developed ARM core-based processor, the A4. Still produced by Samsung, this was the first of the series to integrate an ARM Cortex-A8 in the iPhone Series. Still developing its own processor, Apple is now supplying the processor from TSMC since 2014. Now coupled with its packaging services including integrated Fan-Out (inFO) technology, TSMC is the only processor supplier for Apple.

Two new Apple Macbook models as well as the Mac mini are now powered by an Apple in-house SoC design, the M1. The transition from Intel x86 processors is creating shockwaves felt throughout the processor and computer world. This new and first SoC for Mac features 4-CPU high-performance cores, 4-CPU high-efficiency cores and 8-GPU cores. The tight software-hardware integration inside Apple enabled a compact, efficient processor for personal computer that outcompetes many premium microprocessors. 16 billion transistors using TSMC 5nm process are used to build it.

On the SoC side, it appears that the die area of the M1 has been optimized for functionality rather than SRAM cache. There is limited on-chip cache, taking cues from mobile SoC designs relying on the universal memory architecture (UMA) concept and external LPDDR4X DRAM. Significant die area is devoted to standard cell functions, which indicate that Apple is leveraging in-house chip design to optimize hardware for the operating system. On the packaging side, the same structure is used for Apple A12X and A12Z, with the integration of the DRAM on the SoC substrate, and embedded silicon capacitors in the substrate.

To reveal all the details for this new exceptional SoC, this report features multiple analyses: Floor plan analysis to understand the high-level chip architecture with IP block area contribution measurements, Front-End construction analysis to reveal the most interesting features of the new TSMC 5nm process, Back-End construction analysis for packaging structure. It also features a detailed study of the die analyses, and cross-sections. In addition to a complete construction analysis using SEM cross-sections, material analyses and delayering, the front-end analysis uses high-resolution TEM cross-section to expose the high mobility channel of the 5nm process and the back-end analysis uses CT-Scan (3D X-Ray) to reveal the layout structure of the package. It contains a complete cost analysis and a selling price estimation of the component.

Executive Summary – Floor Plan Analysis

This floorplan analysis of the Apple M1 system-on-chip is intended to provide critical insights into the chip architecture.

The M1 is the first Apple in-house design for deployment to their personal computer line after many years and iterations of the mobile AX products (most recently A14).

Confirming the Apple marketing material, the M1 SoC contains these major IP blocks:

- Four “Firestorm” high-performance CPU cores
- Four “Icestorm” power efficient CPU cores
- Eight GPU cores
- Machine learning core – “Neural Engine”
- Dual core secure processor – “Secure Enclave”
- PCI Express high speed serial interfaces (X2)
- Display engine

Taking many queues from the mobile architecture, the M1 limits on-chip SRAM to a great extent. The total of L2 SRAM arrays is estimated to be 27.8 MB. The unified memory architecture (UMA) allows sharing of the LPDDR4X DRAM between the monolithic CPU and GPU cores. The incorporation of the DRAM on a common BGA substrate with the M1 silicon is similar in concept to typical mobile application processors (APU). However, the APU for mobile products typically deploys the LPDDR variant in a package-on-package configuration over the APU. The M1 package is more suited to higher performance and higher power consumption applications such as desktops and laptops since heat sinks can be directly applied to the M1 SoC.

Executive Summary

The reverse costing analysis is conducted in 3 phases:

Teardown analysis

Package is analyzed and measured
The dies are extracted in order to get overall data: dimensions, main blocks, pad number and pin out, die marking
Setup of the manufacturing process.

Costing analysis

Setup of the manufacturing environment
Cost simulation of the process steps

Selling price analysis

Supply chain analysis
Analysis of the selling price

Glossary

Acronym	Definition
IC	Integrated Circuit
IHS	Integrated Heat Spreader
BGA	Ball Grid Array
CMOS	Complementary Metal–Oxide–Semiconductor
CPU	Central Processing Unit
CUF	Capillary Underfill
DRAM	Dynamic Random Access Memory
G&A	General & Administrative
GPU	Graphics Processor Unit
IHS	Integrated heat spreader
PCB	Printed Circuit Board
PGDW	Potential Good Dies per Wafer
PTH	Plated through hole
R&D	Research and Development
SEM	Scanning Electron Microscope
Si	Silicon
SiO2	Silicon Oxide
TIM	Thermal Interface Material

COMPANY PROFILE

Company Profile – Apple

Apple Inc.

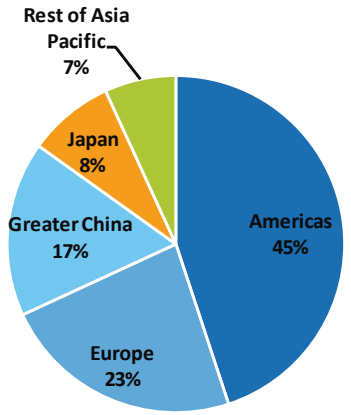
2020 Apple Financial Highlights:

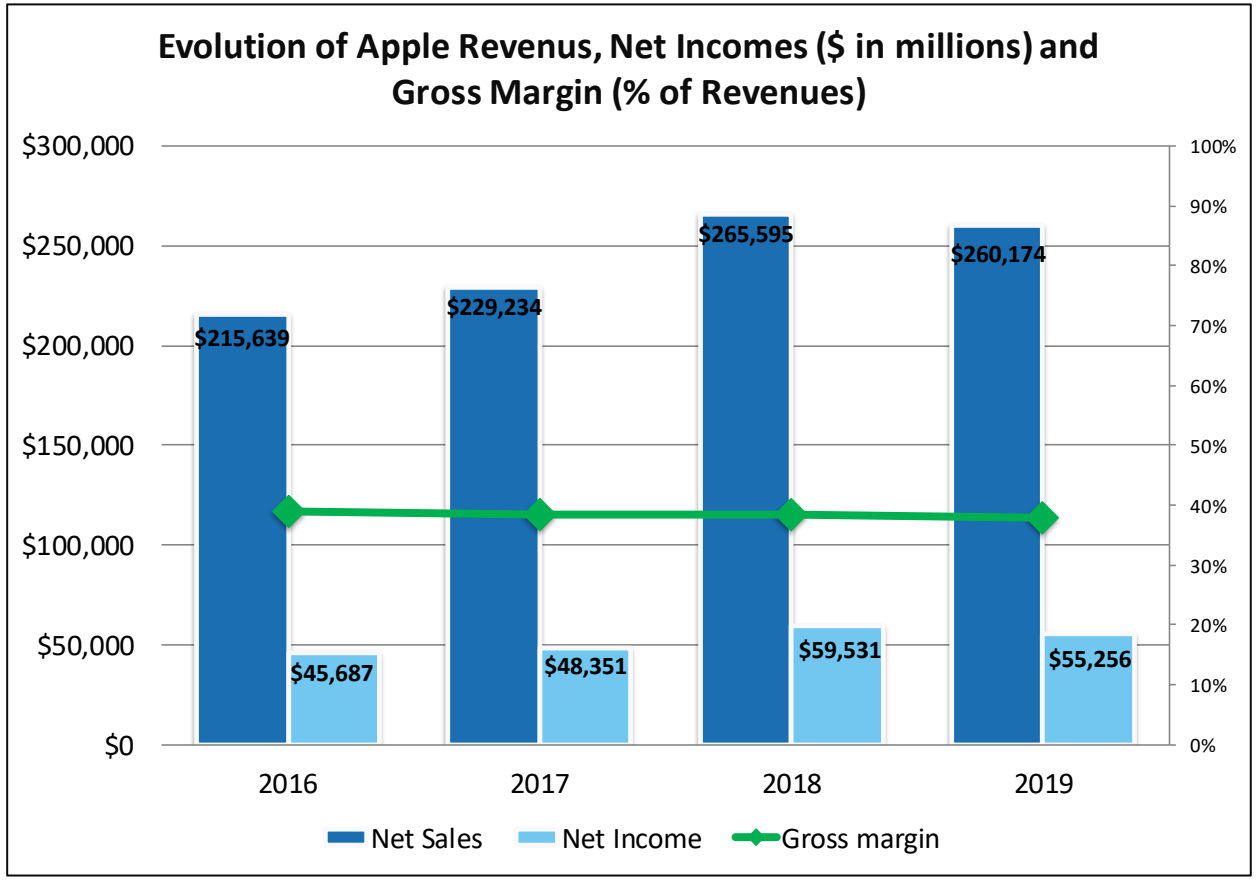
- Sales revenues: $275 Billion
- Gross margin: 38.2 %
- Net income: $57 Billion

Employees:

- Date of Establishment
  - ✓ 1976
- Headquarter:
  - ✓ Cupertino, California, USA
  - ✓ 137,000 employees worldwide (as of 28 September 2019).

Apple's Net Sales Worldwide

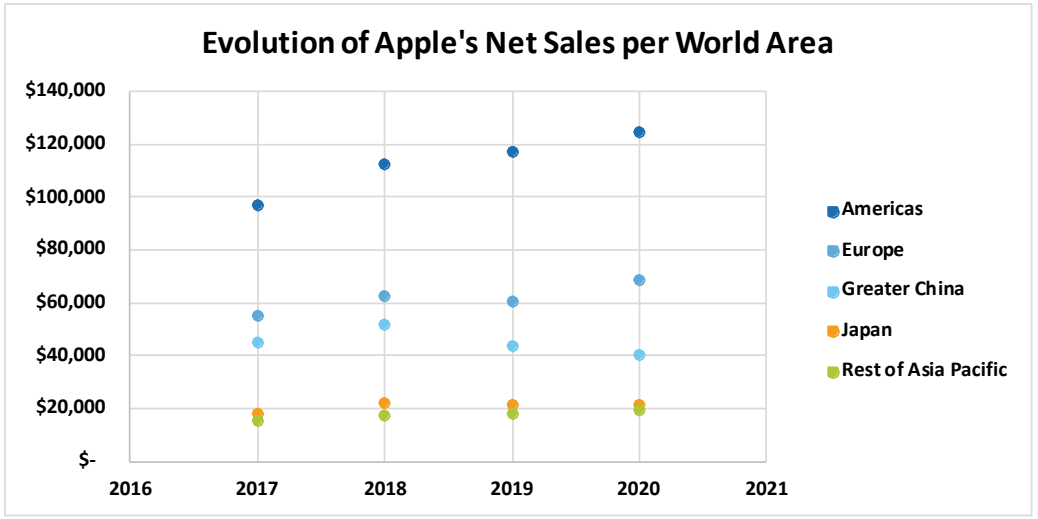


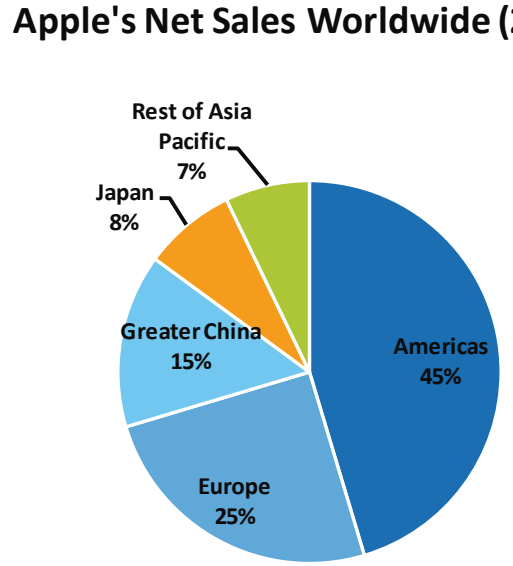


Apple 2020– Financial Results

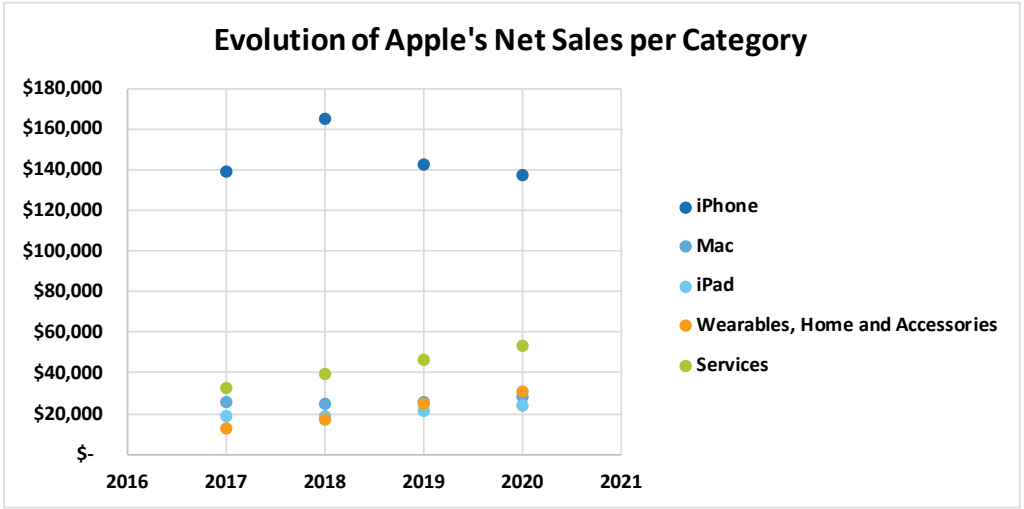
Company Profile – Apple

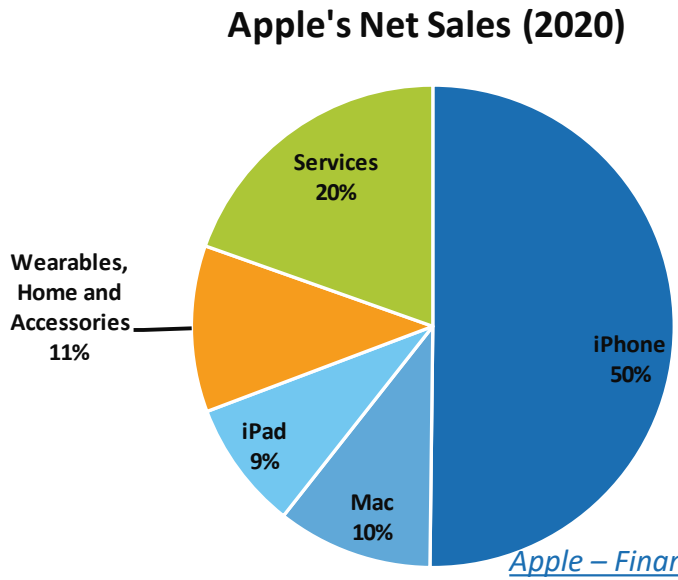
Apple Inc.





- America's net sales increase each year with a slope higher than in Europe. In Japan and Rest of Asia Pacific, the tendency is flat.





- Mac net sales increased in 2020 due to higher net sales of MacBook Pro.
- In 2021, the Apple M1 will potently help to increase the number of the Mac sales.
- Services net sales increased due to higher sells from the App store and cloud services.

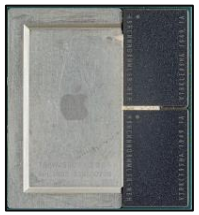
Apple – Financial Results

Company Profile – Apple Processors

Apple Inc.

iPad Pro 4th Gen.

A12Z



Component: **577 mm²**
SoC Die: **129.41 mm²**

iPhone 12 Series

A14

Component: **168 mm²**
SoC Die: **88.79 mm²**

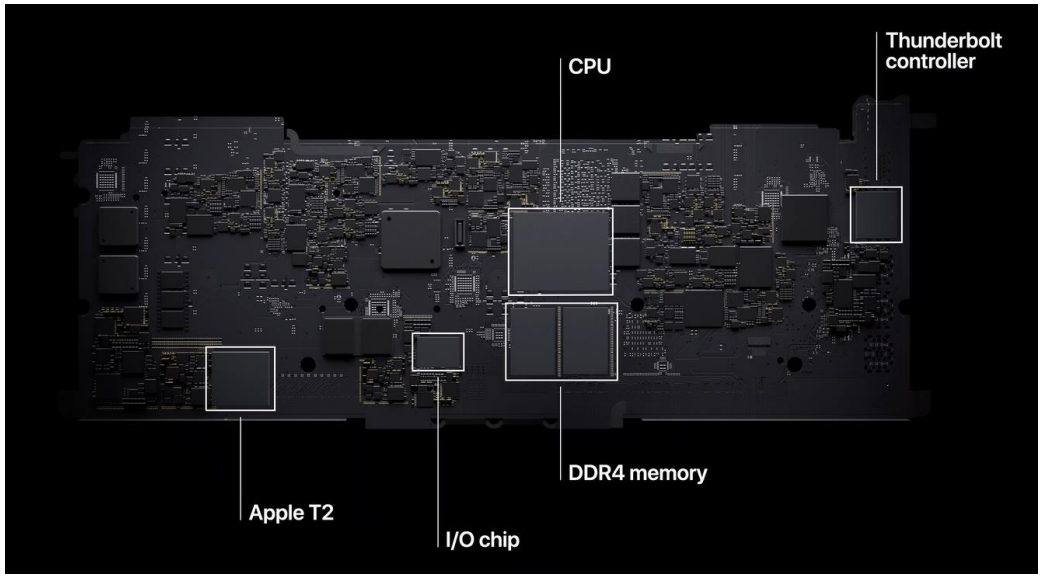
Apple Watch

S6 Chip

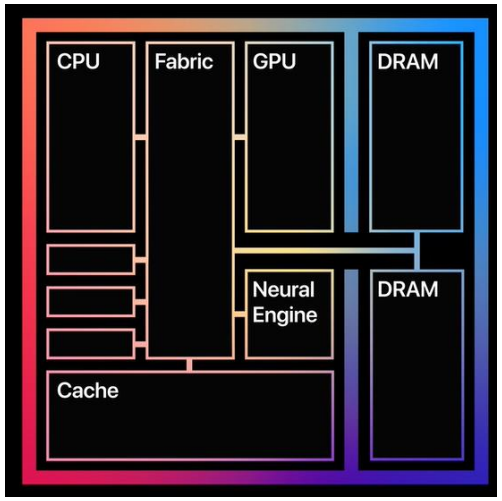
Component: **125.76 mm²**
SoC Die: **39.4 mm²**

Apple Products
Apple

Apple M1 Architecture

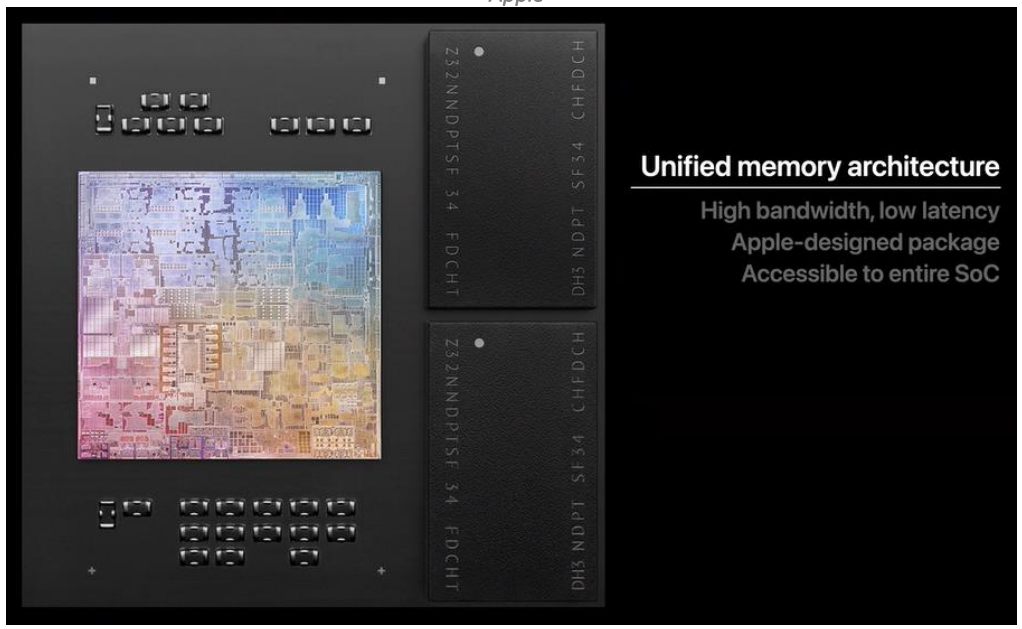


Mac Discrete Implementation
Apple



M1 Functional Block Diagram
Apple

- In the M1, all discrete function (Secure Element, Interface Controller, GPU, ..) are integrated in only one SoC.
- As the memory chip is integrated on the same PCB substrate as the SoC, the system benefit from high-speed processing with High Bandwidth.



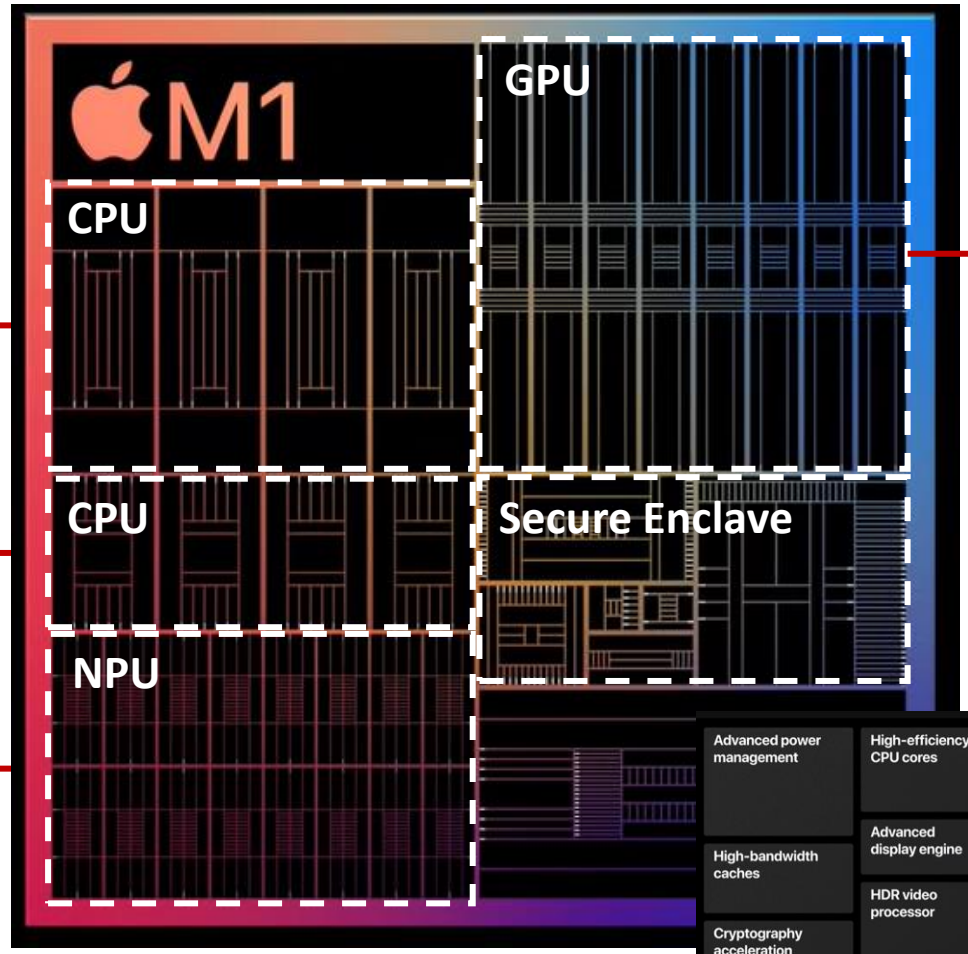
Unified Architecture Implementation
Apple

Apple M1 Architecture

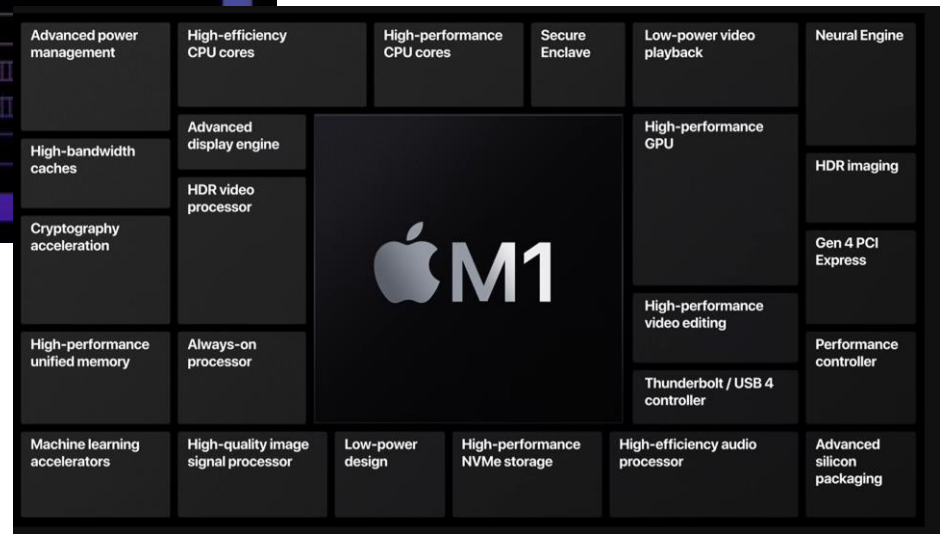
4 High-Performances Cores
Ultra-Wide Execution architecture
192 KB instruction cache
128 KB data cache
Shared 12MB L2 cache

4 High-Efficiency Cores
Wide Execution architecture
128 KB instruction cache
64 KB data cache
Shared 4 MB L2 cache

16 Cores

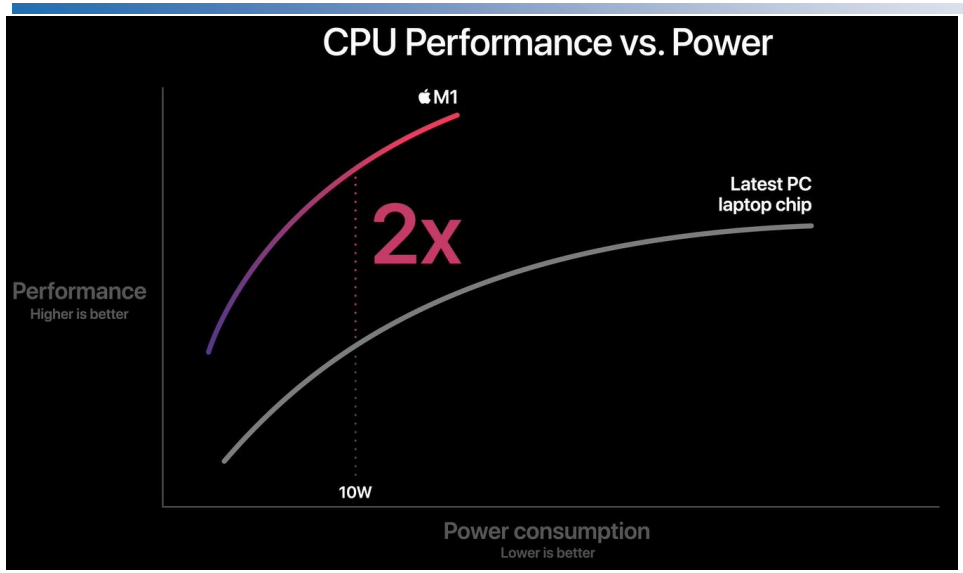


Up to 8 Cores
128 execution units
Up to 24,576 concurrent threads
2.6 teraflops
82 gigatexels/second
41 gigapixels/second

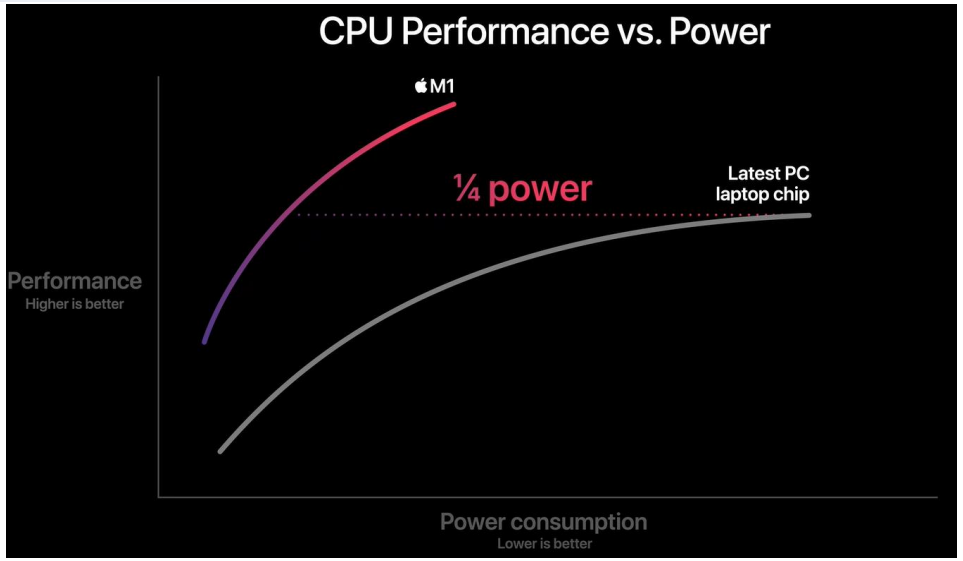


M1 Functional Block Diagram
Apple

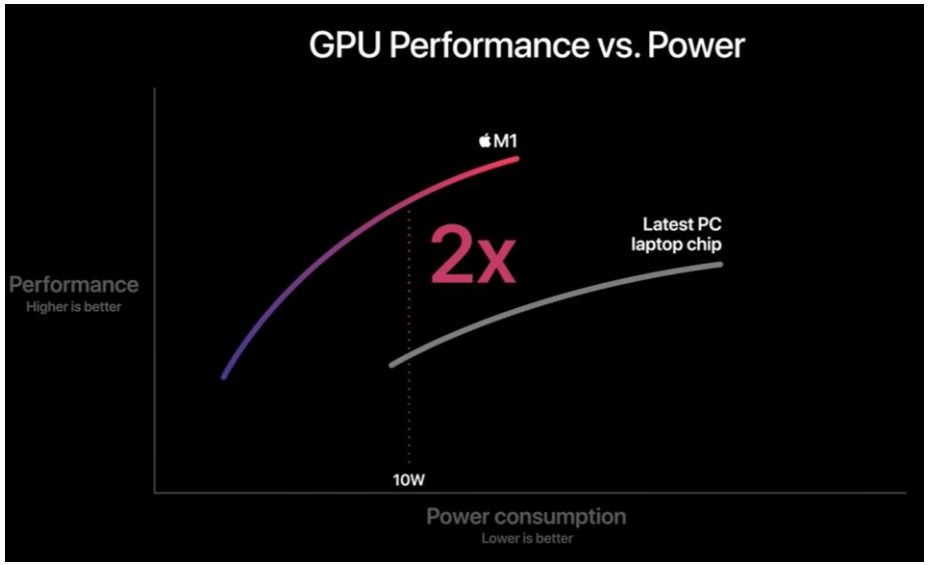
Apple M1 Performances



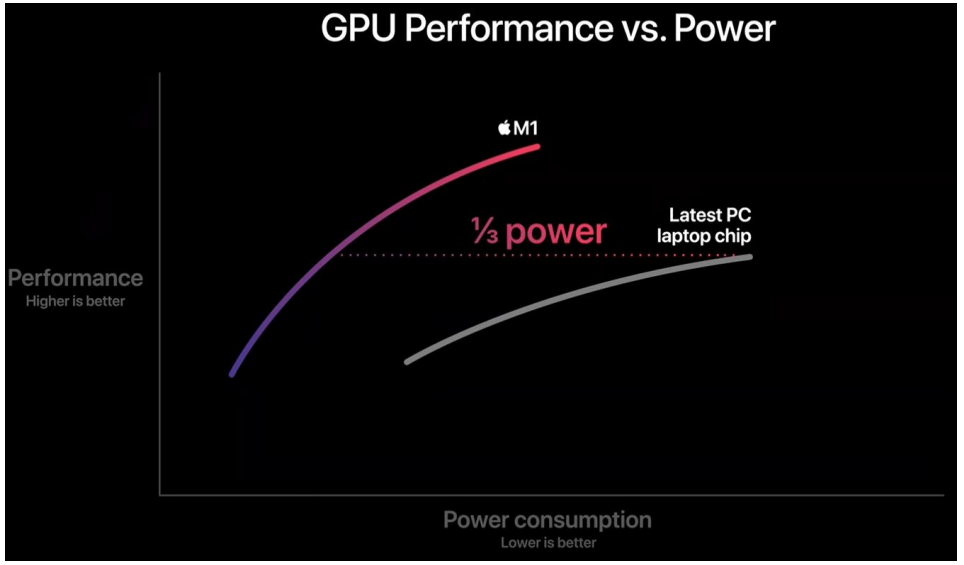
M1 CPU Performance Comparison
Apple



M1 CPU Power Consumption Comparison
Apple



M1 GPU Performance Comparison
Apple



M1 GPU Power Consumption Comparison
Apple

PHYSICAL ANALYSIS

Apple Mac Mini Overview

Apple Mac Mini Top View
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Apple Mac Mini Bottom View
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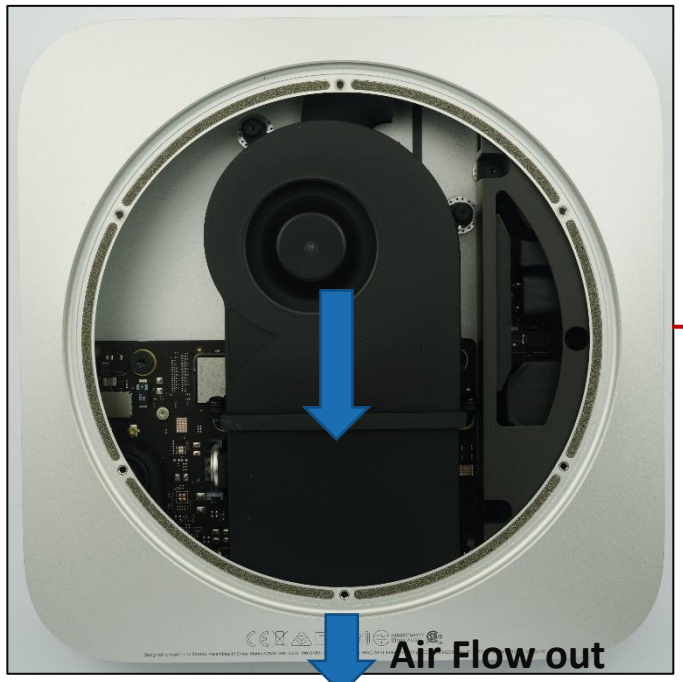
Apple Mac Mini TearDown



Apple Mac Mini Back View
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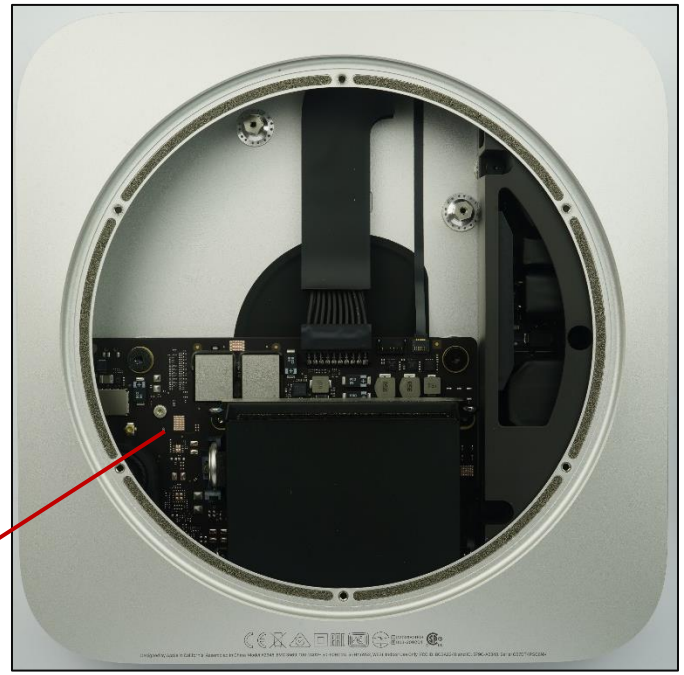
Mac Mini Teardown
(backside cover removal)



Apple Mac Mini Back View
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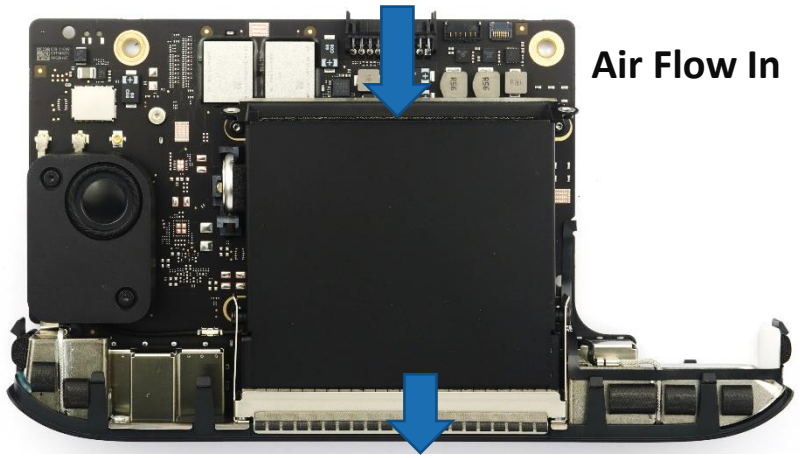
Mac Mini Teardown
(PCB/Board removal)



Apple Mac Mini Board
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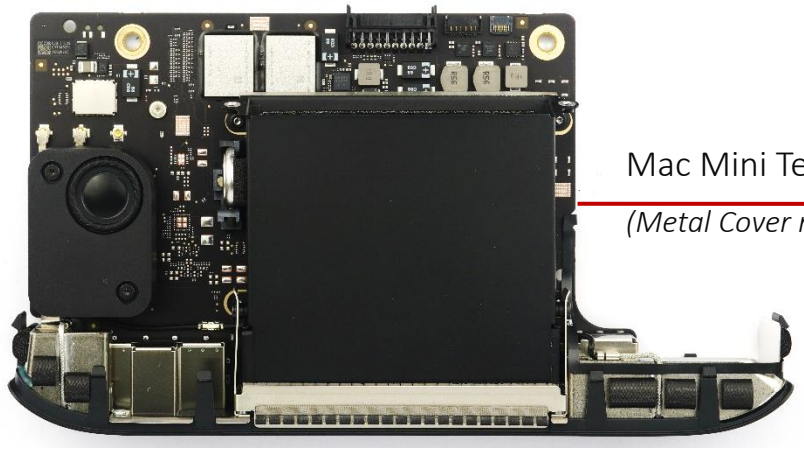
Apple Mac Mini TearDown



Apple Mac Mini Board
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Mac Mini Teardown
(Metal Cover removal)

Apple Mac Mini Board- Metal Cover
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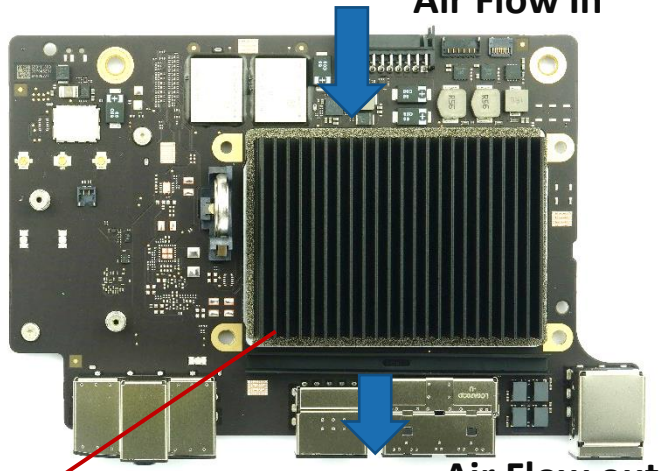

Apple Mac Mini Board
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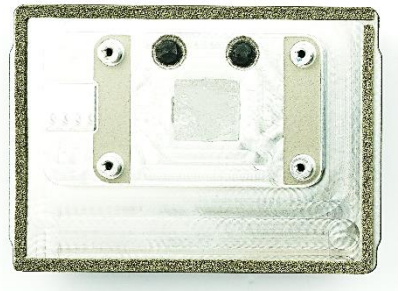
Mac Mini Teardown
(Heatsink removal)



Apple Mac Mini Board- Heatsink
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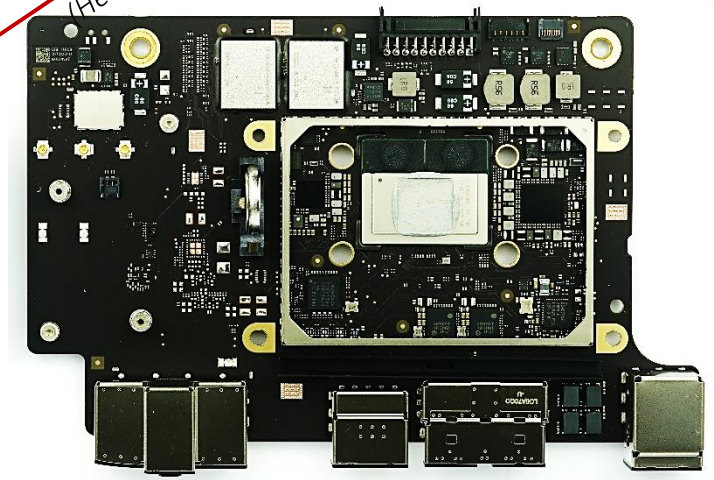

Apple Mac Mini Board
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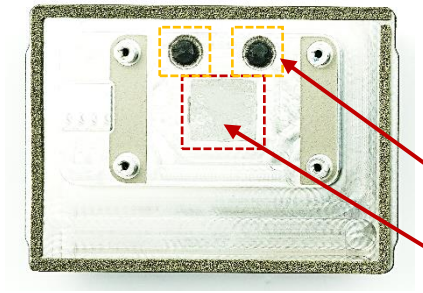
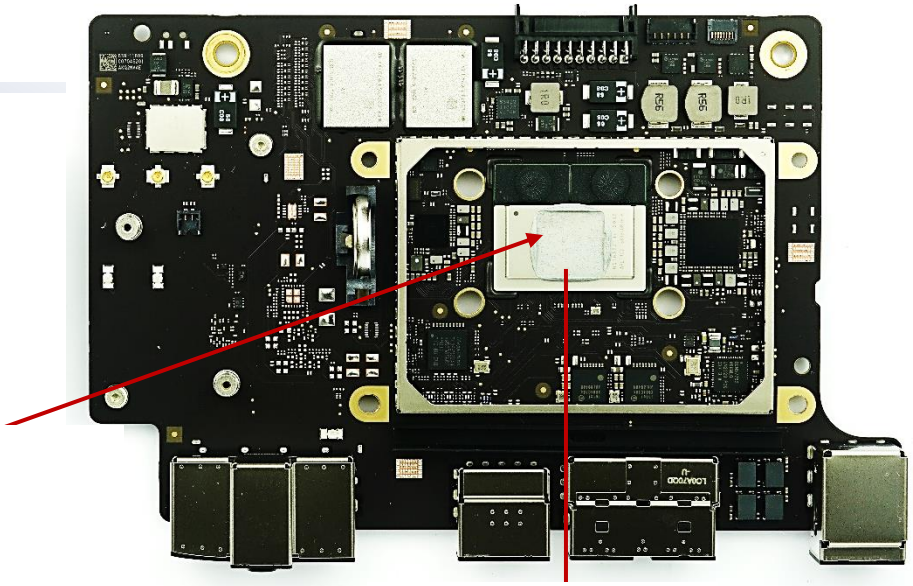
Apple Mac Mini TearDown

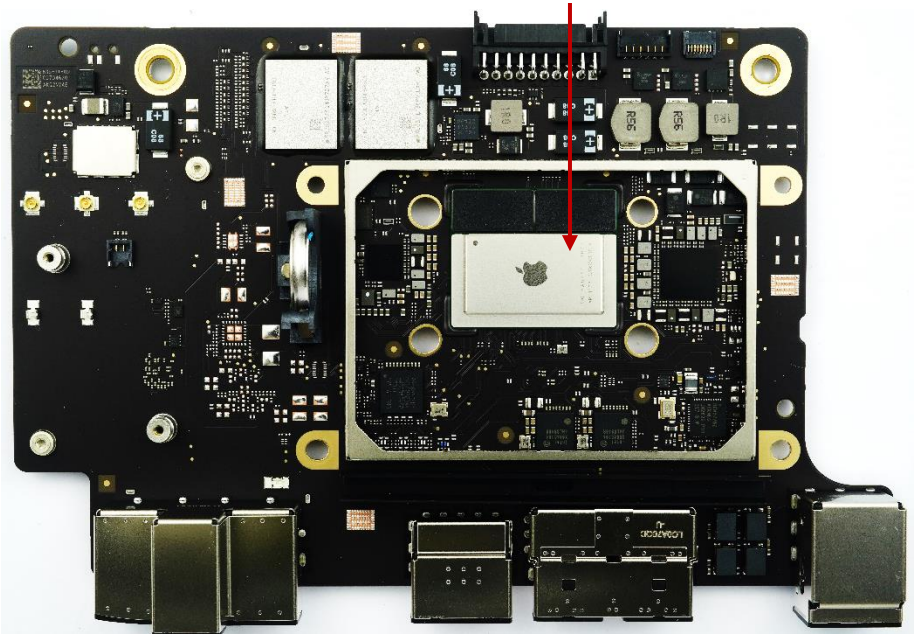


Apple Mac Mini Board Heatsink

TIM Material



TIM Material Removal



Apple Mac Mini Board – Top View

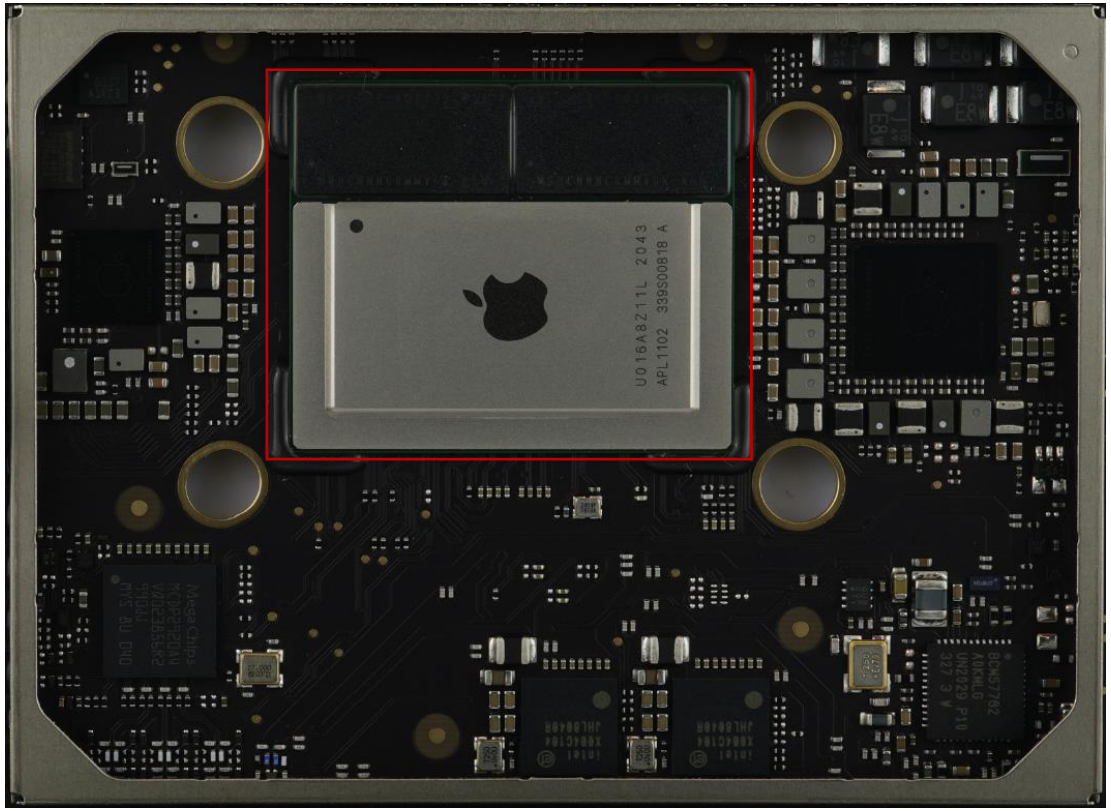
Thermal Interface material (TIM) is used as an interface between:

- the metal cover/heatsink and the Apple M1 Component.
- Between the DRAM Memory and heatsink.

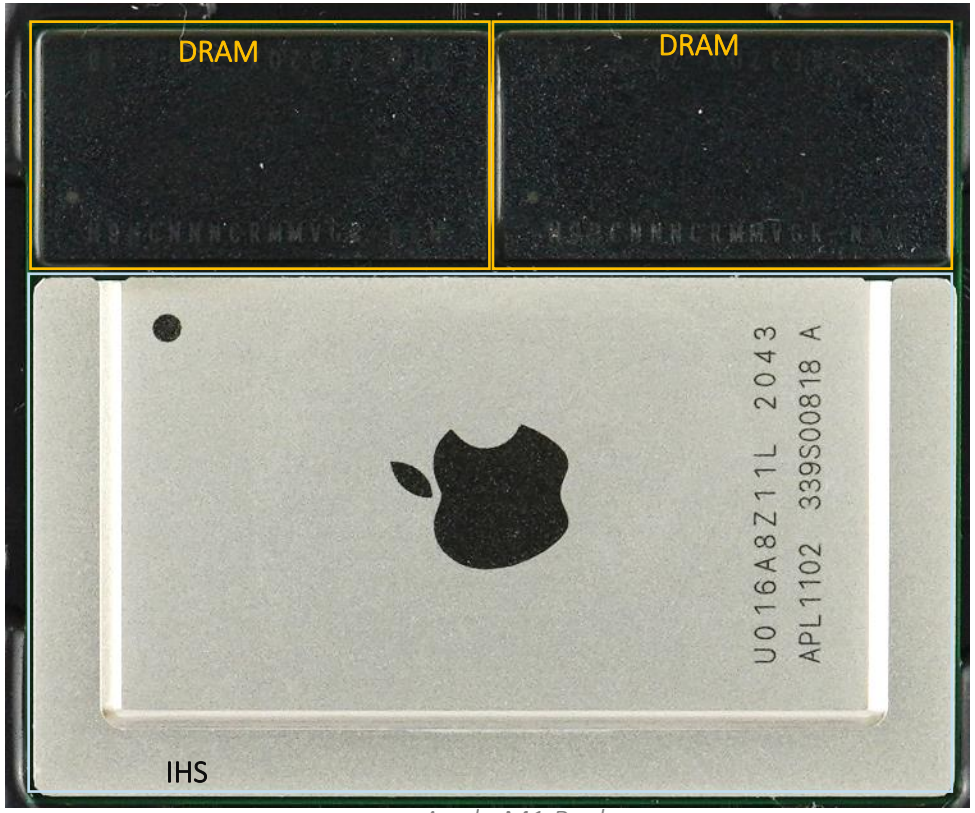
There are two different types of TIM used on the DRAM and on the IHS.

The TIM maximizes heat dissipation.

Apple Mac Mini TearDown

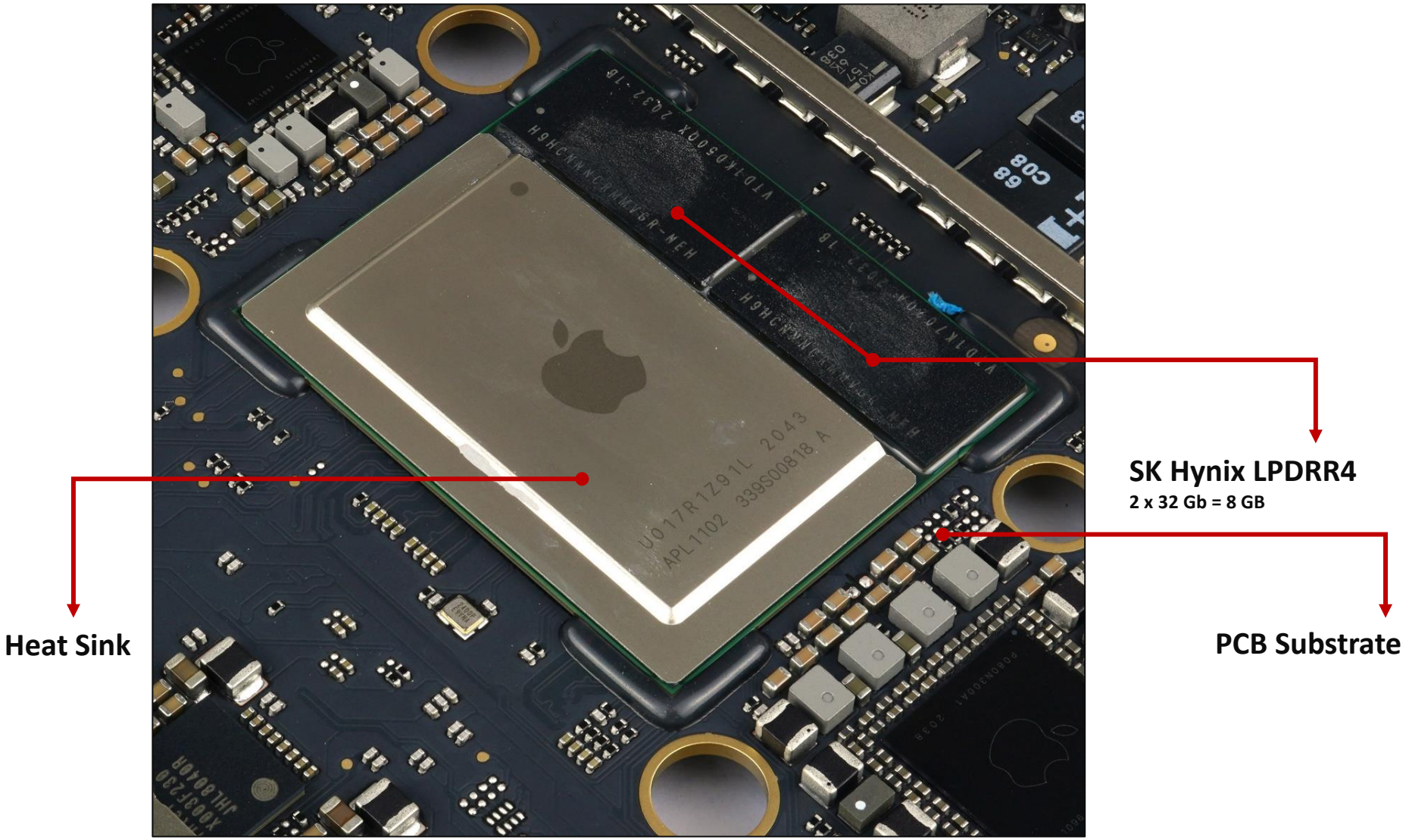


Apple Mac Mini Board



Apple M1 Package

Apple Mac Mini TearDown



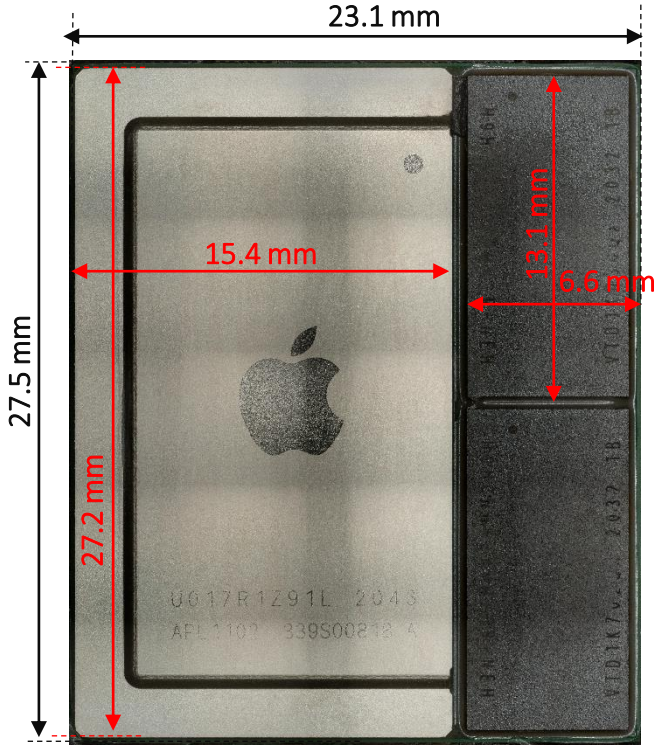
Apple M1 Package Overview

PHYSICAL ANALYSIS
Packaging

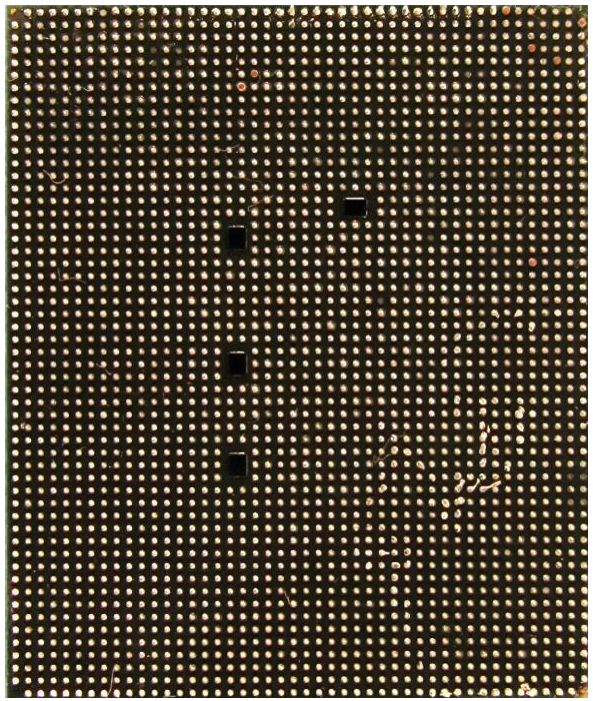
M1 Package Views & Dimensions

- M1 Package: SiP BGA 2,502
- Ball Pitch: 0.5 mm
- Dimensions: 27.5 x 23.1 mm

- DRAM Package
  - Dimensions: 13.1 x 6.6 mm
- IHS Package
  - Dimensions: 27.2 x 15.4 mm

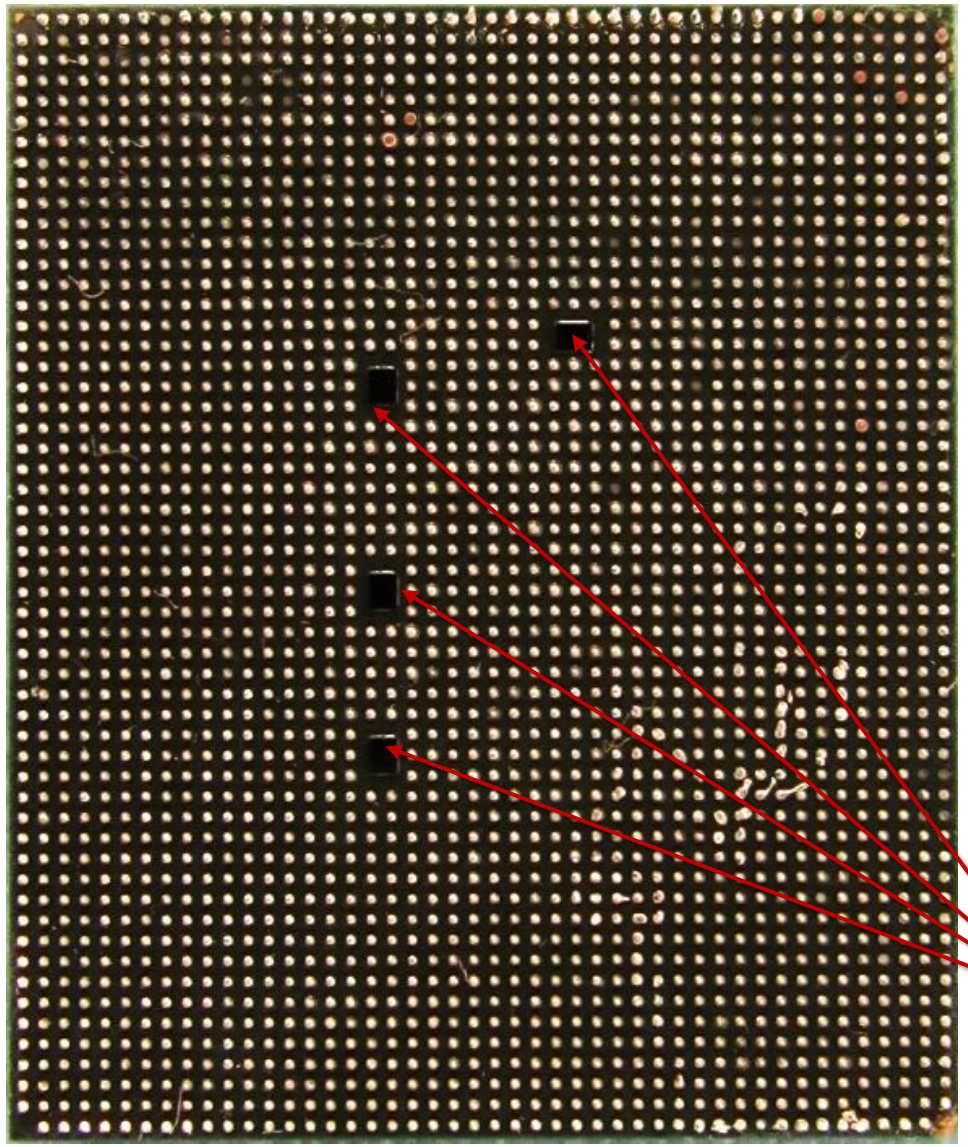


Package Front View



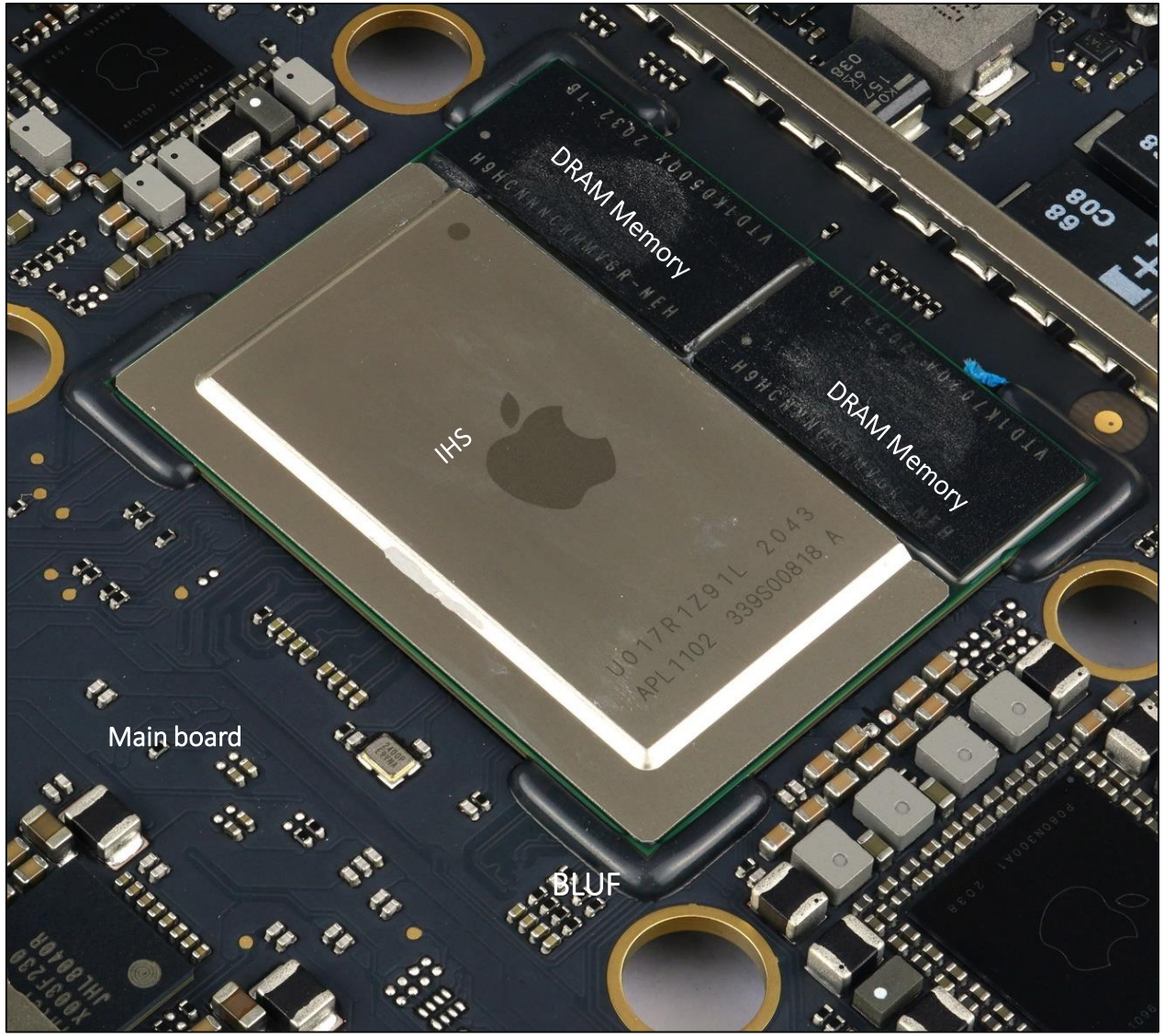
¨Package Back View

M1 Package Views & Dimensions



Package Back View

M1 Package Overview

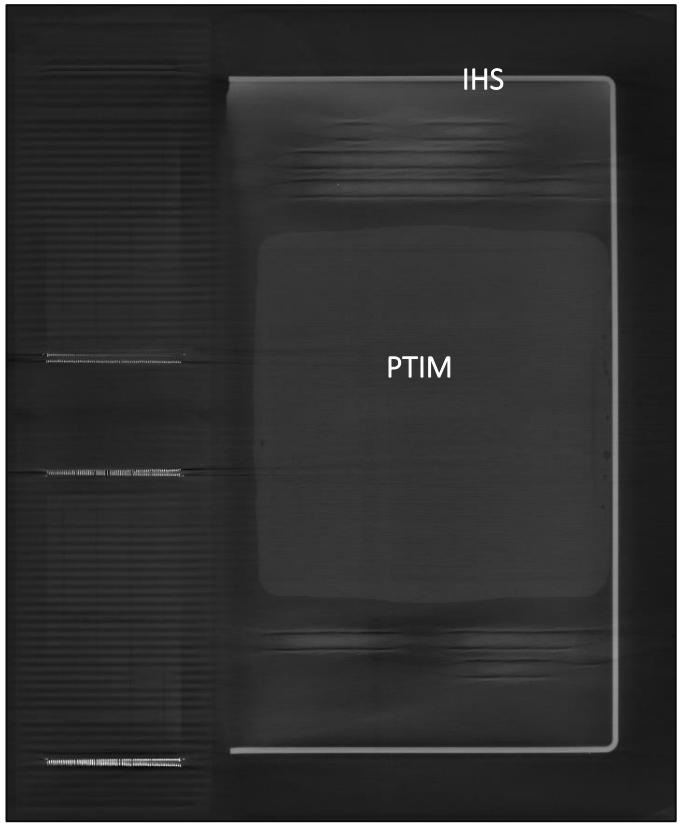


Packaging overview – Optical View

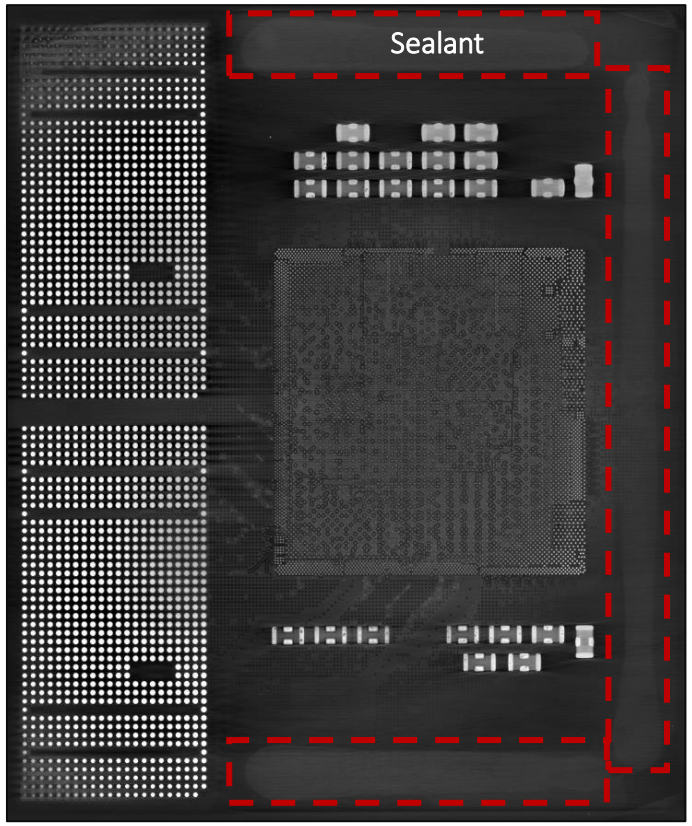
Package Marking

- U017R1Z91L – Trace code
- APL1102 – Product Code
- 2043 – Packaging information (year 2020, week 43)
- 339S00818 A

Package Disassembly – X-Ray



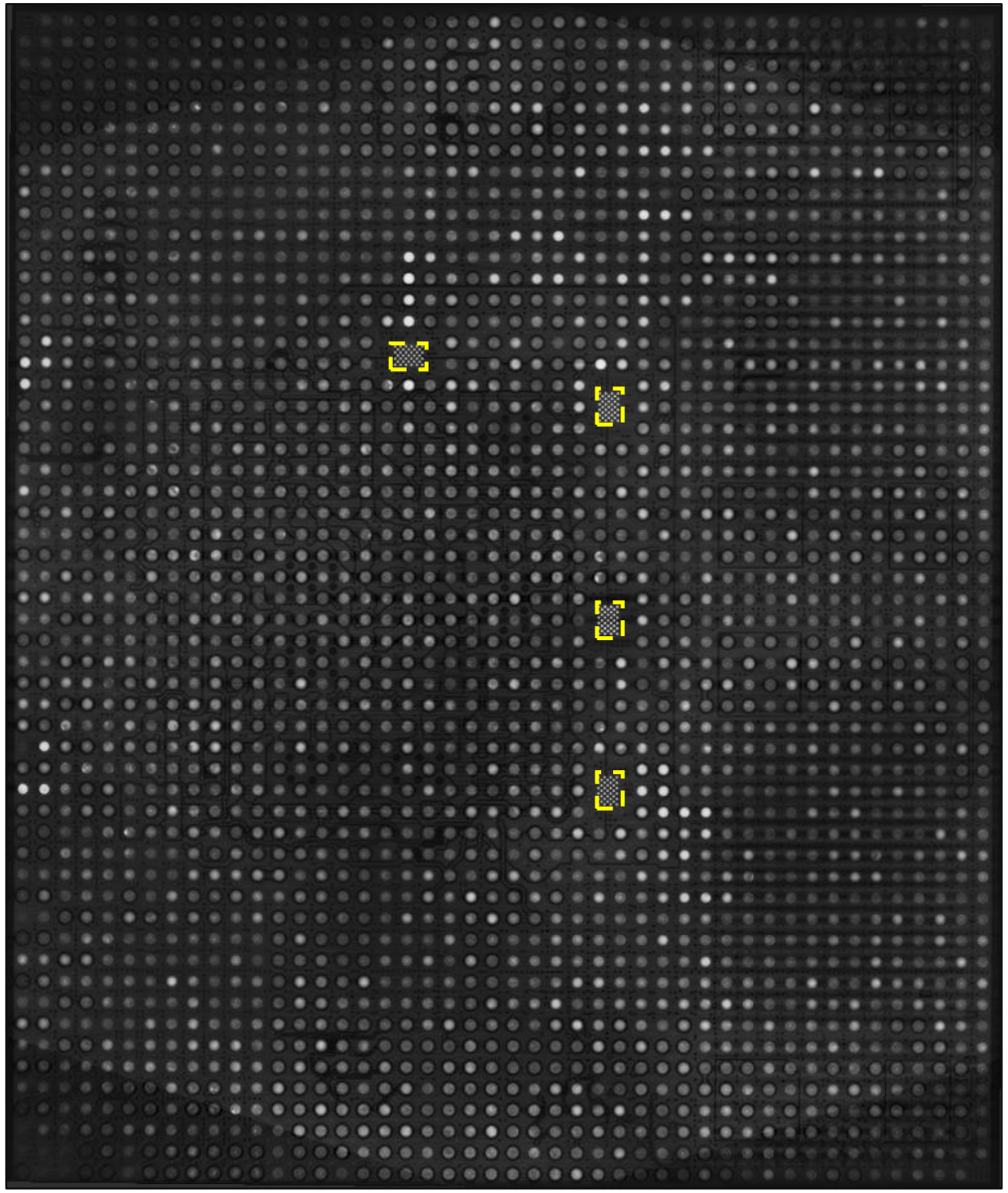
IHS Bottom View – X-Ray View



Packaging Top View w/IHS off – X-Ray View

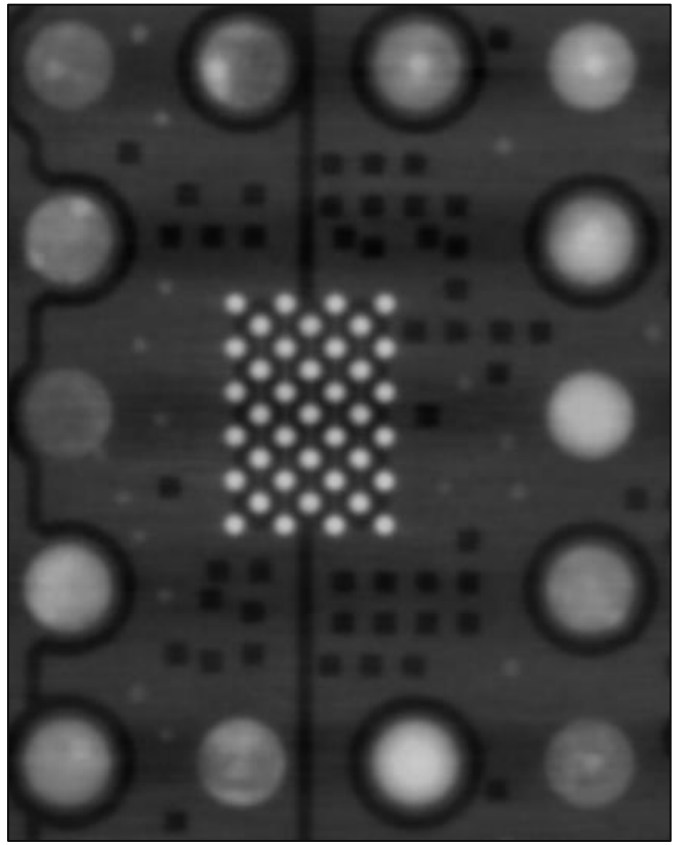
IHS Attributes	Measurements
IHS Form Factor	15 x 27
IHS Foot Width	1.94 mm
IHS Edge to PKG Edge, Min	100 µm
IHS to DRAM	483 µm
Sealant Width (N/S/E) (mm)	(2.07/0.99/1.77)

M1 Interconnect X-Ray



BGA and DTC Interconnect Map – X-Ray View

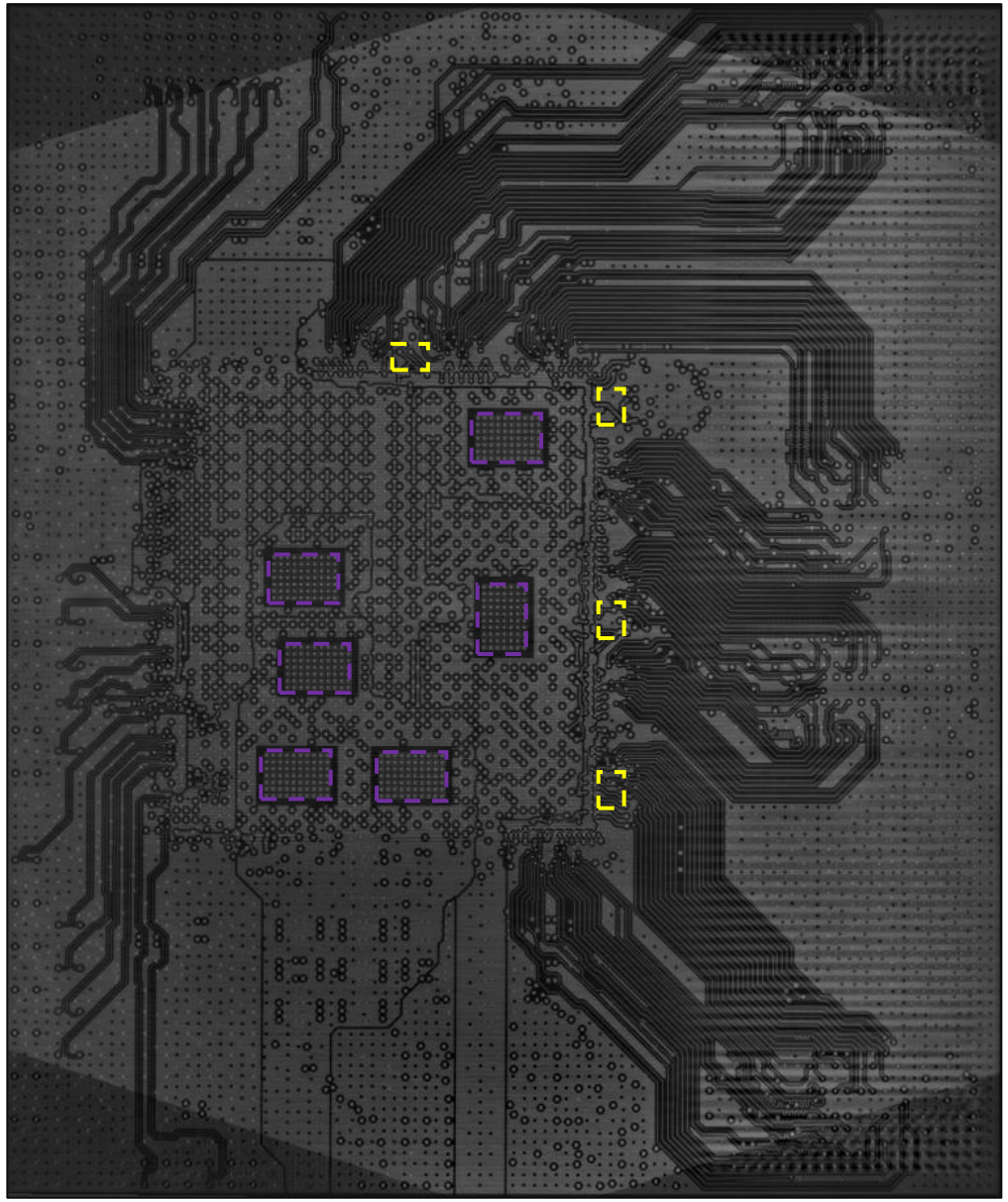
- The M1 has the corners depop'd. BLUF is just deposited at the corner of the component.
- 6 BGA's de-pop'd for each DTC.



DTC Interconnect Map – X-Ray View

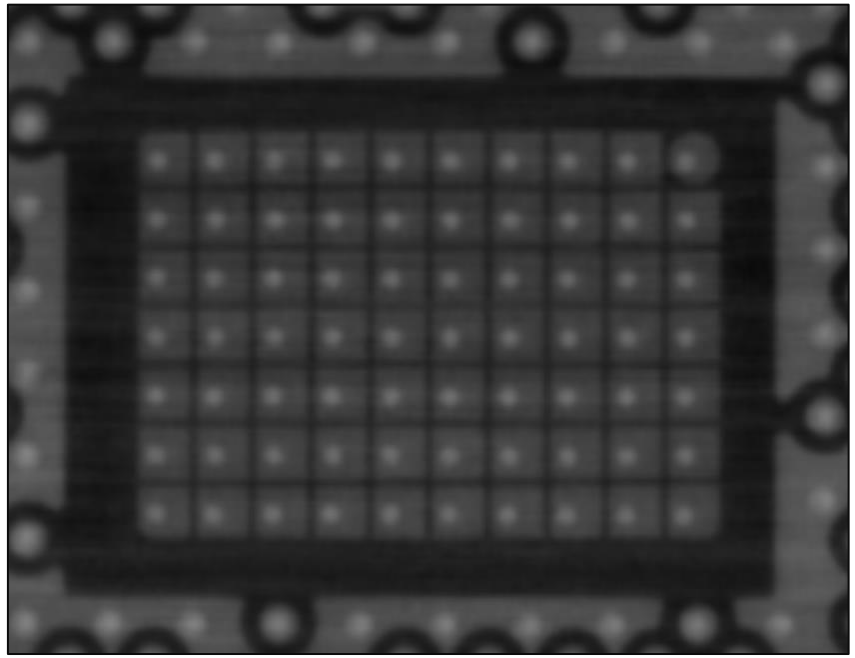
- DTC Ball Number: 39
- DTC Ball pitch: 87.7 µm

M1 Interconnect X-Ray



Embedded Capacitors Interconnect Map – X-Ray View

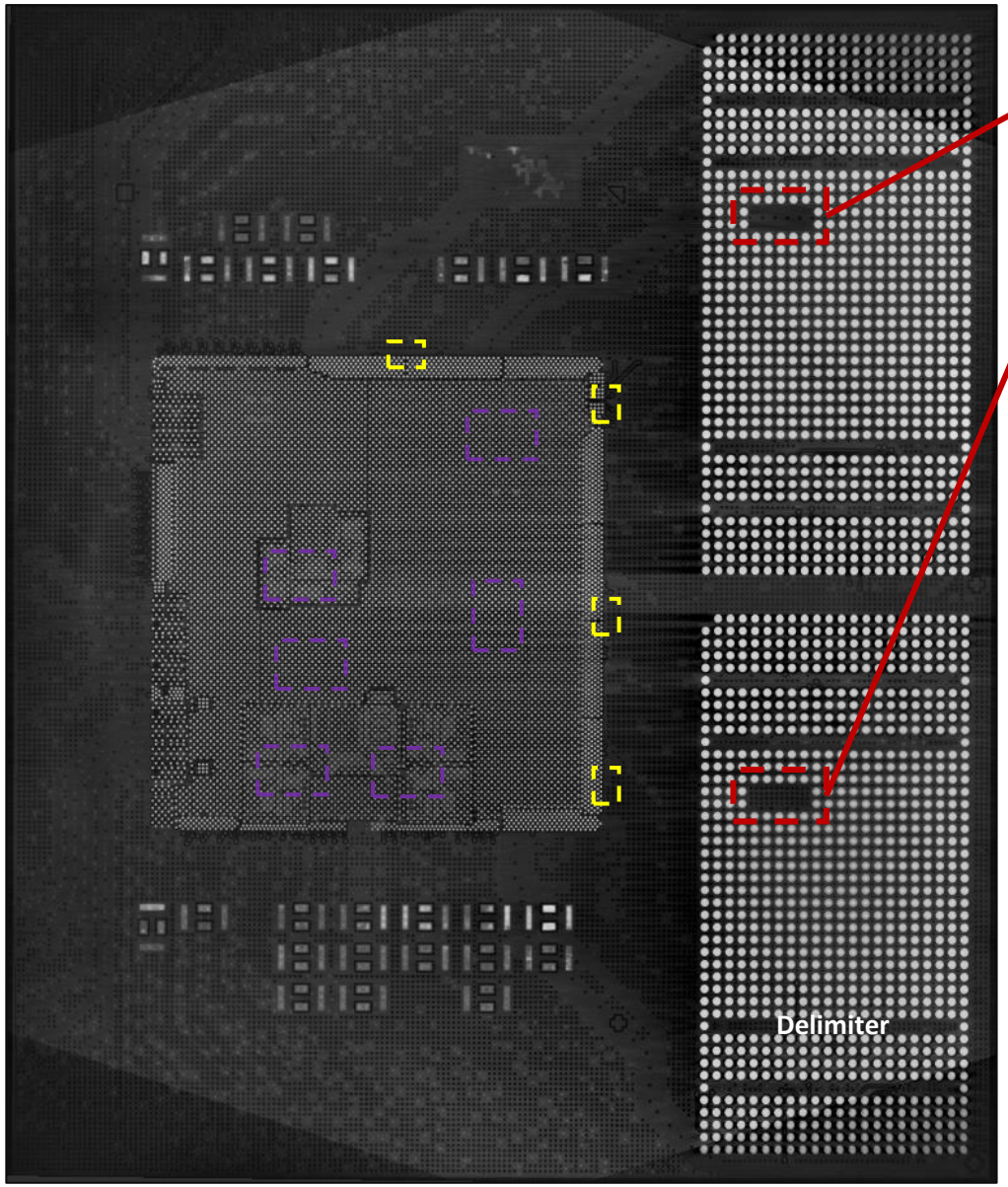
- The M1 has 6 embedded silicon capacitor. The first pad of the capacitor is round whereas the others are rectangular.

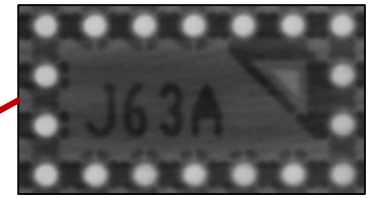


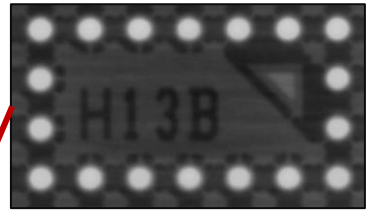
Embedded Capacitor Interconnect Map – X-Ray View

- Embedded Cap. Pad Number: 70
- Embedded Cap. Square Pad size: 0.0196 mm² (0.14 x 0.14 mm)
- Embedded Cap. Pad pitch: 0.15 mm
- Min LTH to pad edge: 17.5 µm

M1 Interconnect X-Ray







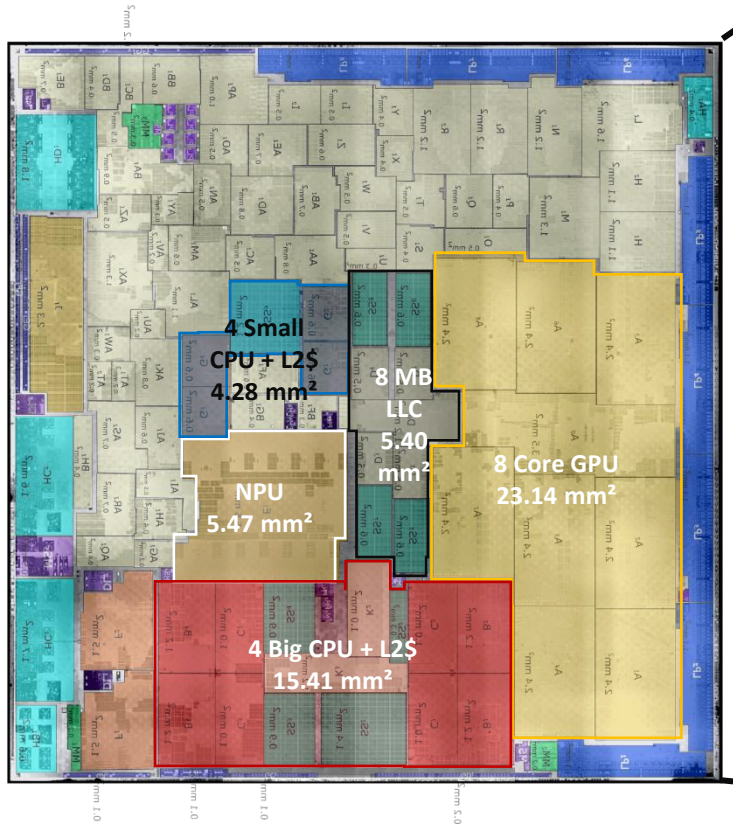
- The DRAM BGA footprint has a de-pop for pin 1 and panel ID plating on the last layer of DRAM package.

	M1	DRAM
BGA Ball Number	2,502	877
BGA Pitch	0.5 mm	0.28 mm
BGA Rows	46 x 55	22 x 44
De-pop	28 (6/DTC & 1/corner)	91 (20/Delimiter), 1/Pin 1 & 10/ID)
Embedded Cap Count	6	N/A
DTC Count/BGA Pitch	6/87.7 µm	N/A

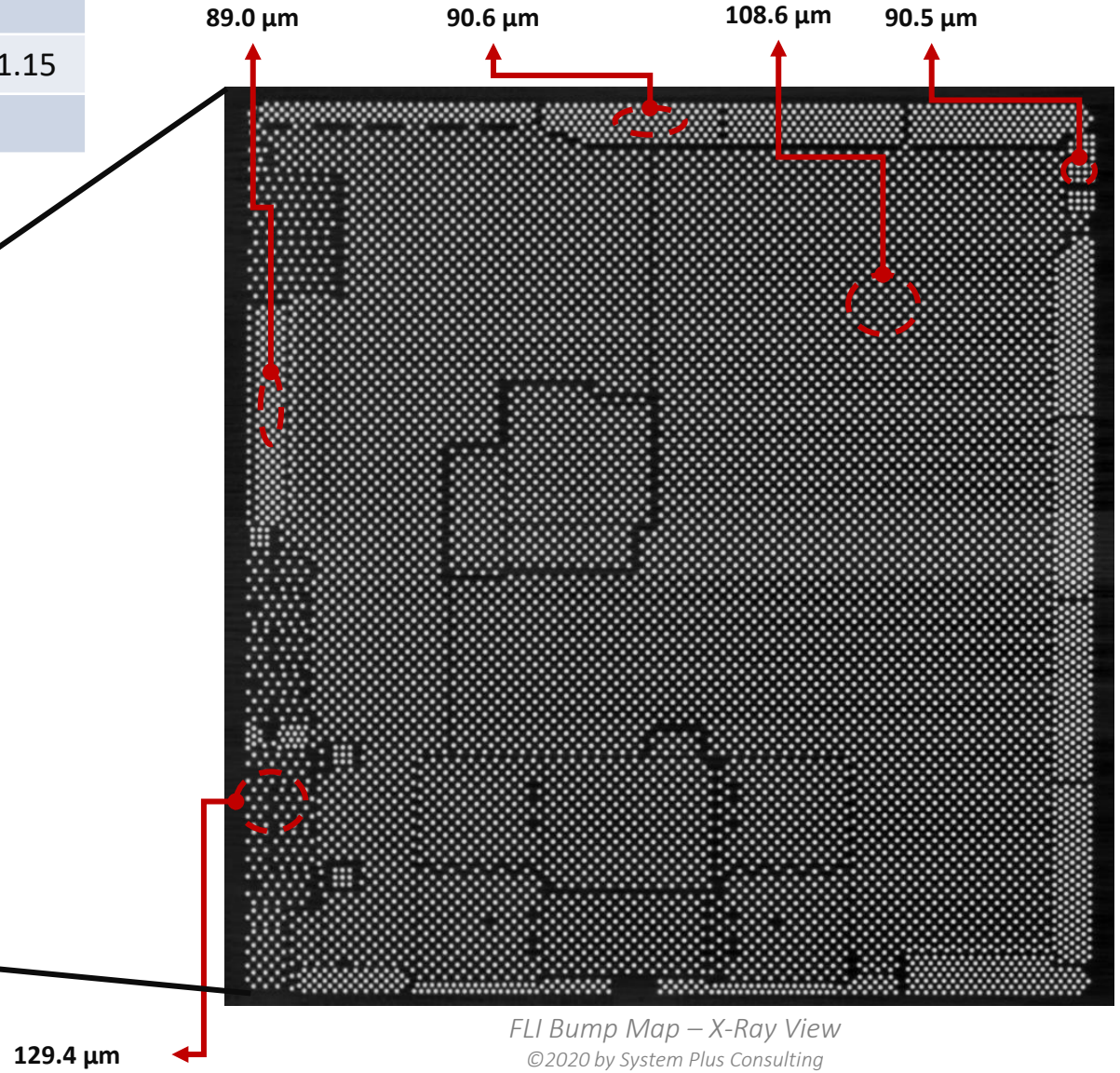
FLI & DRAM Interconnect Map – X-Ray View

M1 FLI Map

Key Attributes			
Foundry	TSMC	***Min FLI Pitch, µm***	90.6 µm
Process node	5 nm	***Die Size (X, Y), mm***	10.57 X 11.15
Metal Layers	16	***Die Area, mm²***	117.8

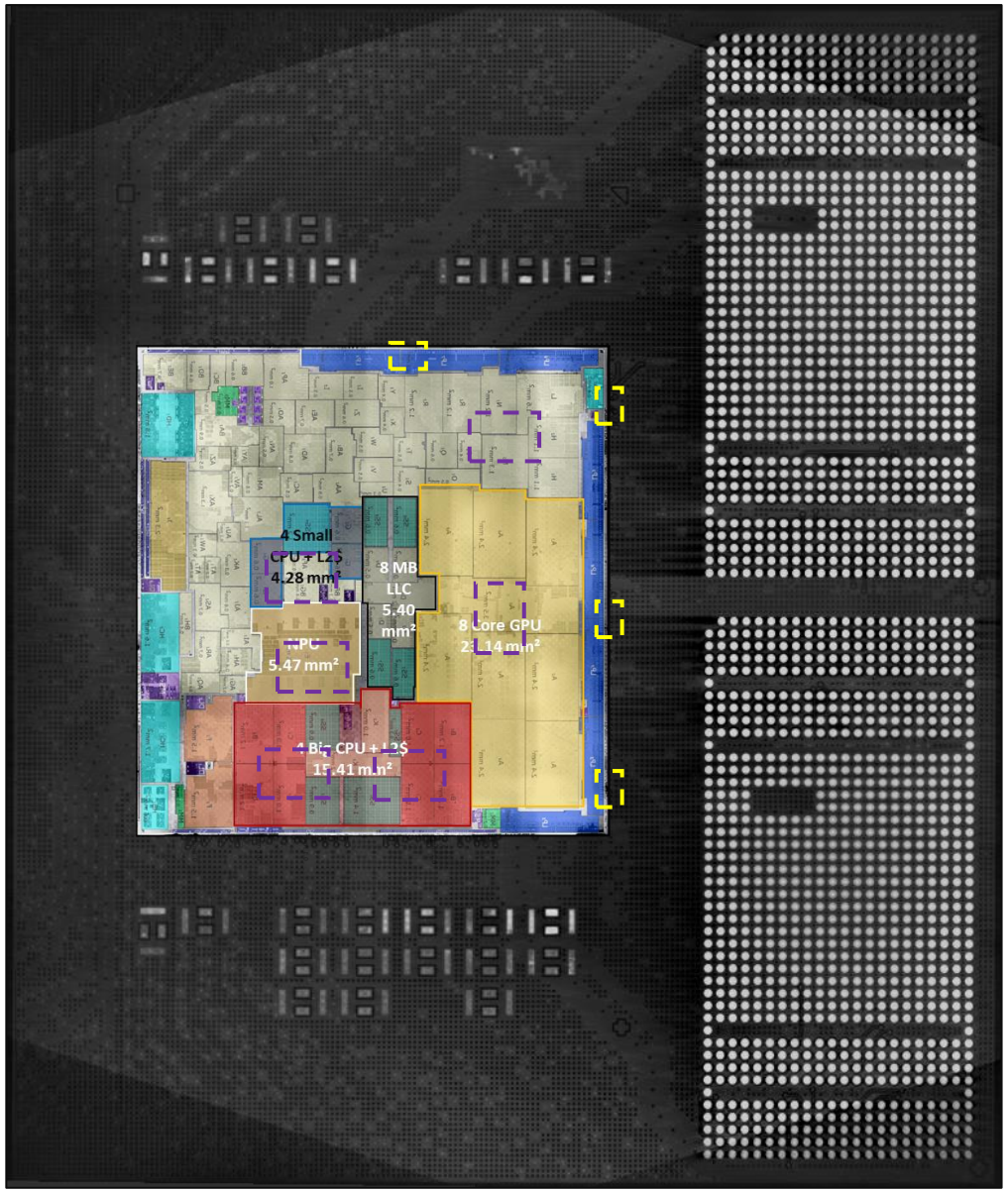


Floor Plan – Schematic View

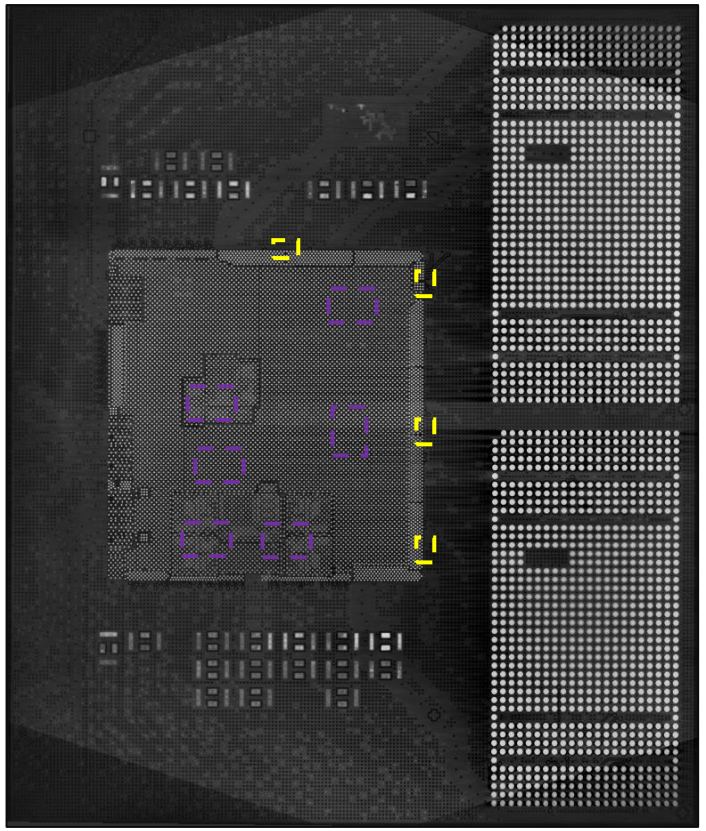


FLI Bump Map – X-Ray View

M1 Interconnect X-Ray



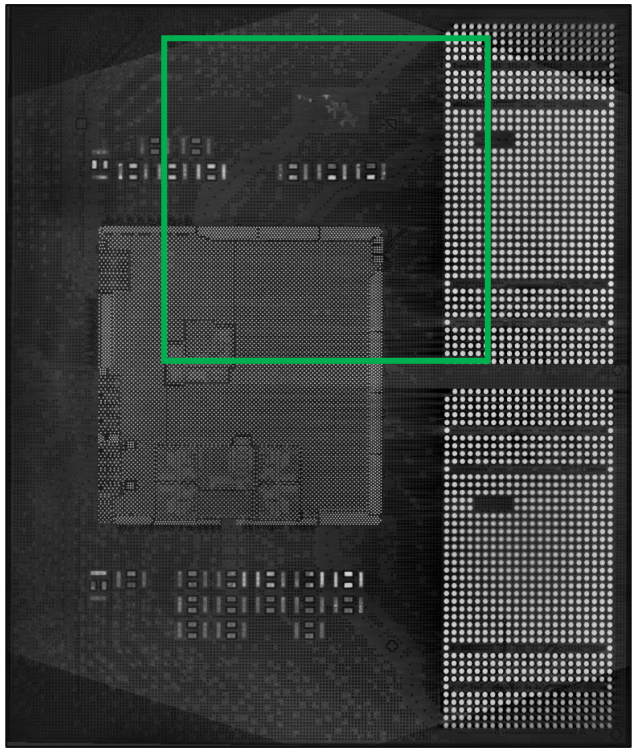
FLI & DRAM Interconnect Map – X-Ray View



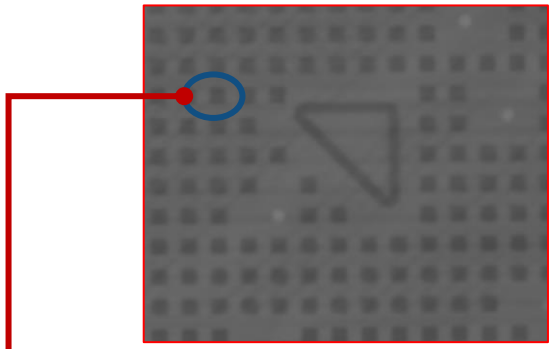
FLI & DRAM Interconnect Map – X-Ray View

- Two embedded capacitors are under the big Core, one is under the GPU, the NPU and the small CPU.
- A last embedded capacitor is placed under the Dual Core ISP and the standard Cell.
- The bottom capacitor is placed directly under the LPDDR4X interface.

M1 PCB Substrate – X-Ray

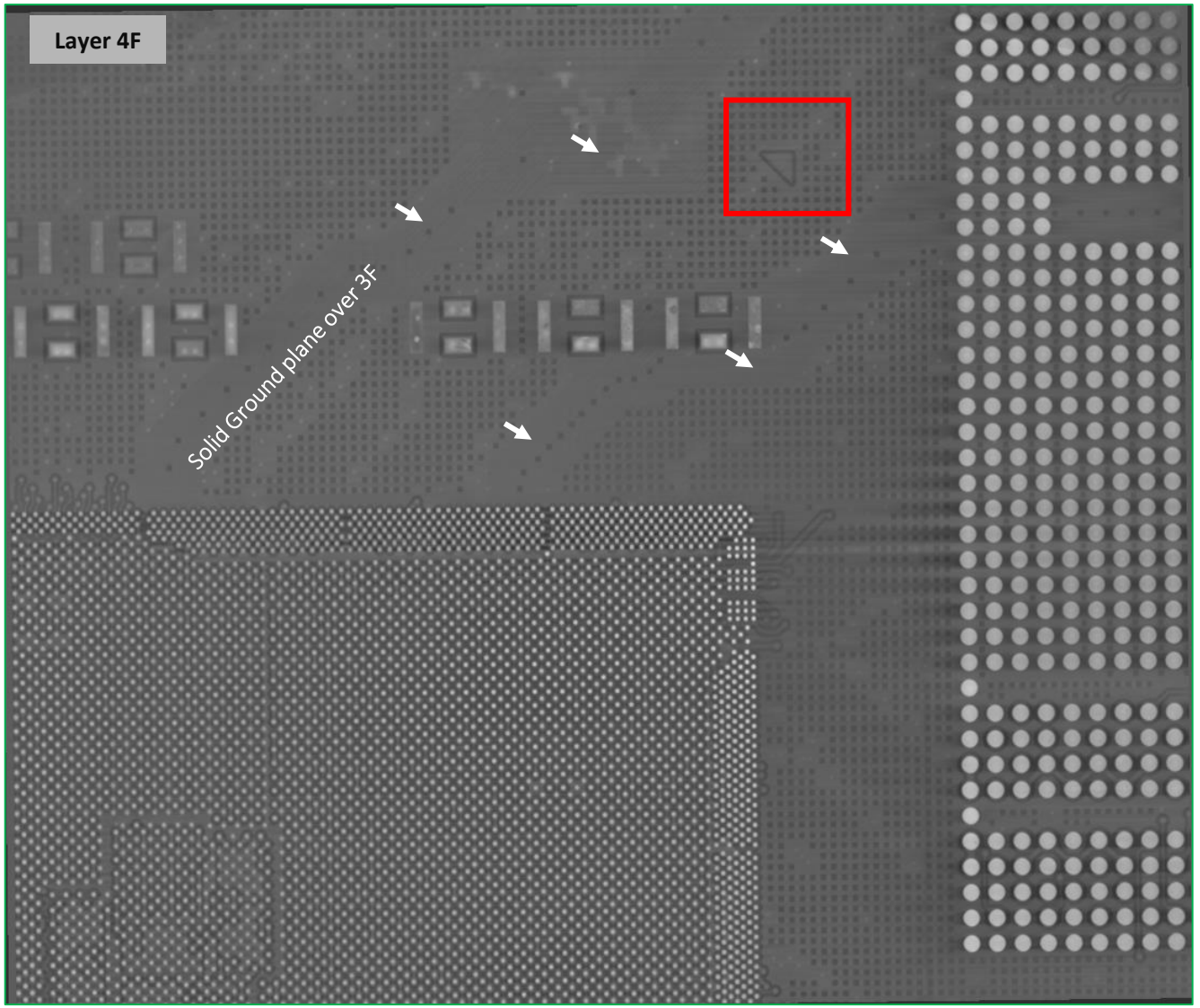


FLI & DRAM Interconnect Map – X-Ray View



Adhesion Square size: **52 µm**

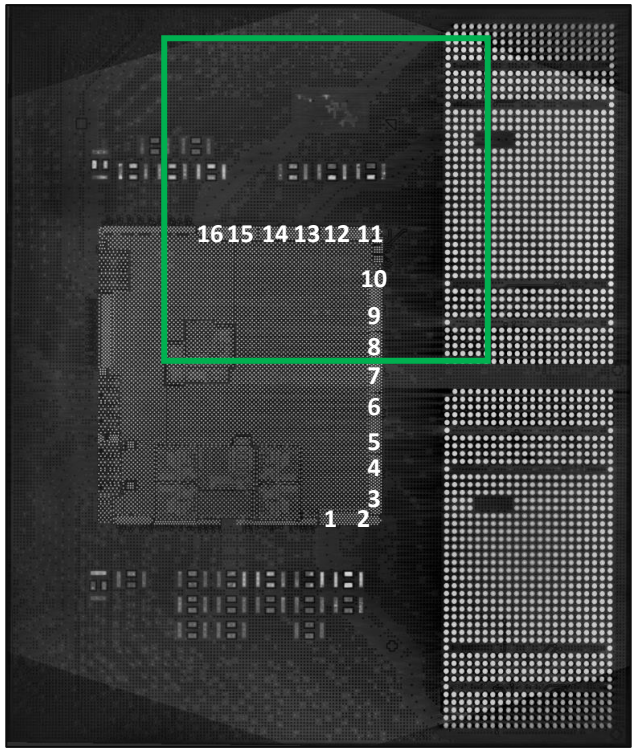
Adhesion Square pitch: **109 µm**



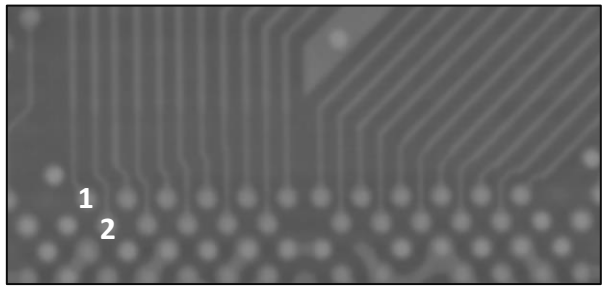
PCB Substrate Layer 4F – X-Ray View

- The PCB has solid ground planes directly over 3F LPDDR Signal for full referencing which should help signal integrity.

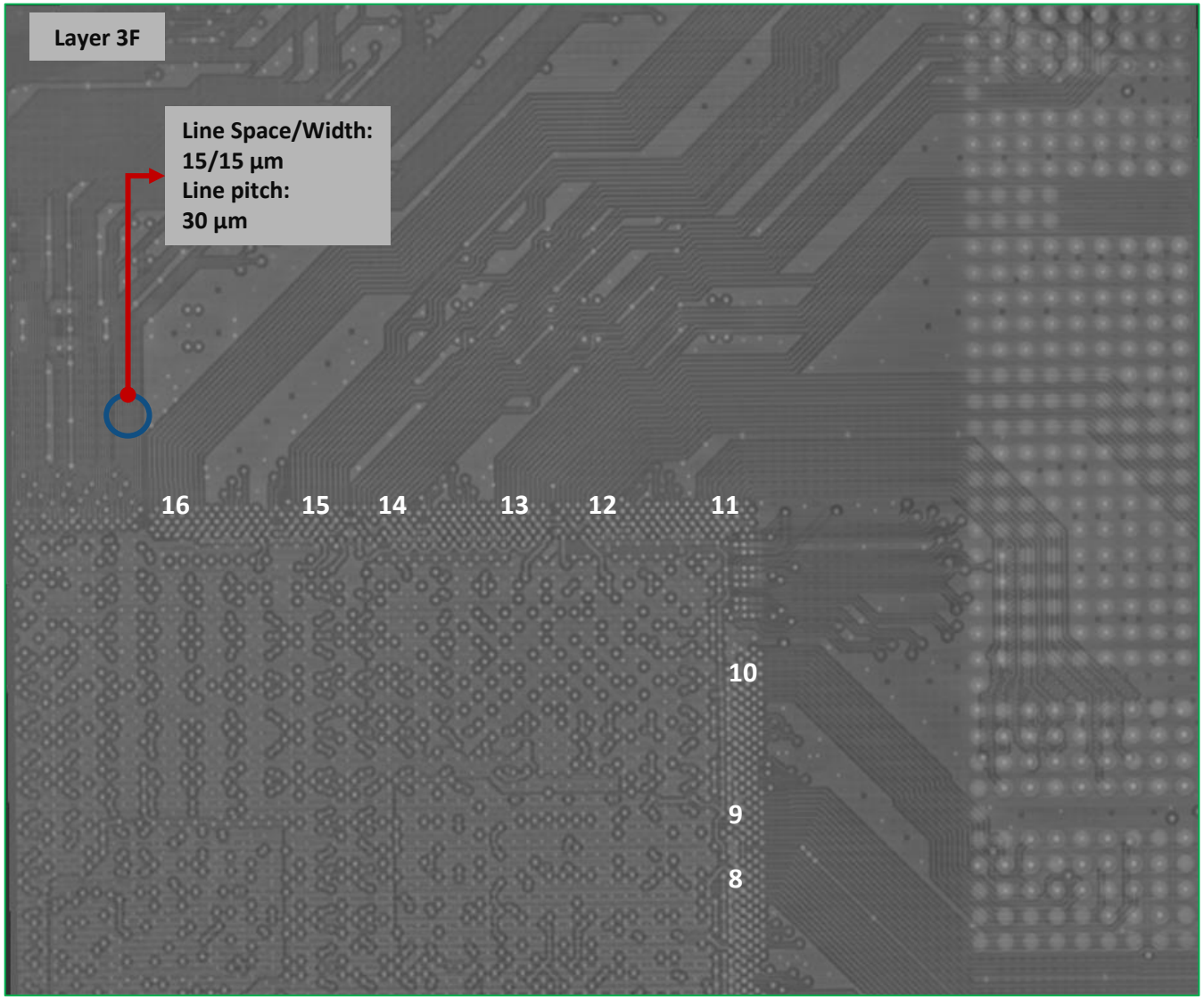
M1 PCB Substrate – X-Ray



FLI & DRAM Interconnect Map – X-Ray View



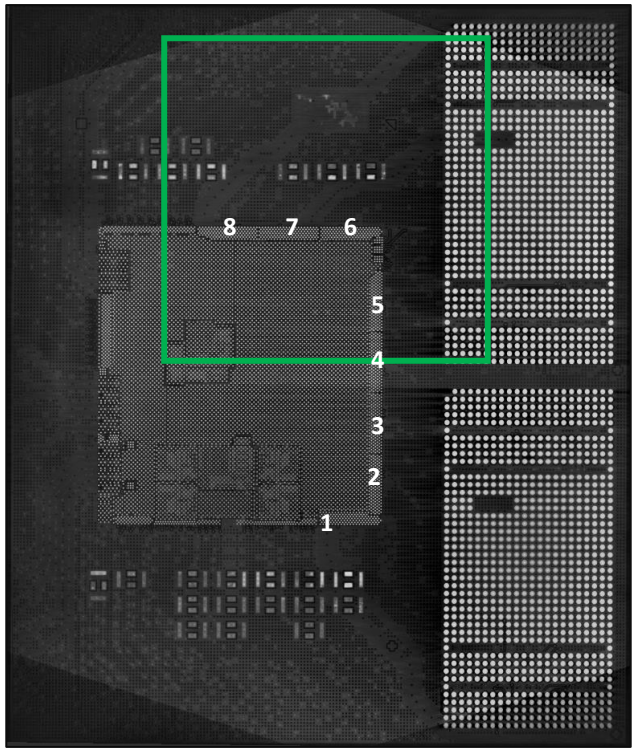
PCB Substrate Layer 3F – X-Ray View



PCB Substrate Layer 3F – X-Ray View

- 16 sets of 11 traces going from die to the DRAMs. 176 total traces. Set to each DRAM PKG, 88 total/DRAM. On the LPDDR area on the die, 2 rows are used for routing.

M1 PCB Substrate – X-Ray

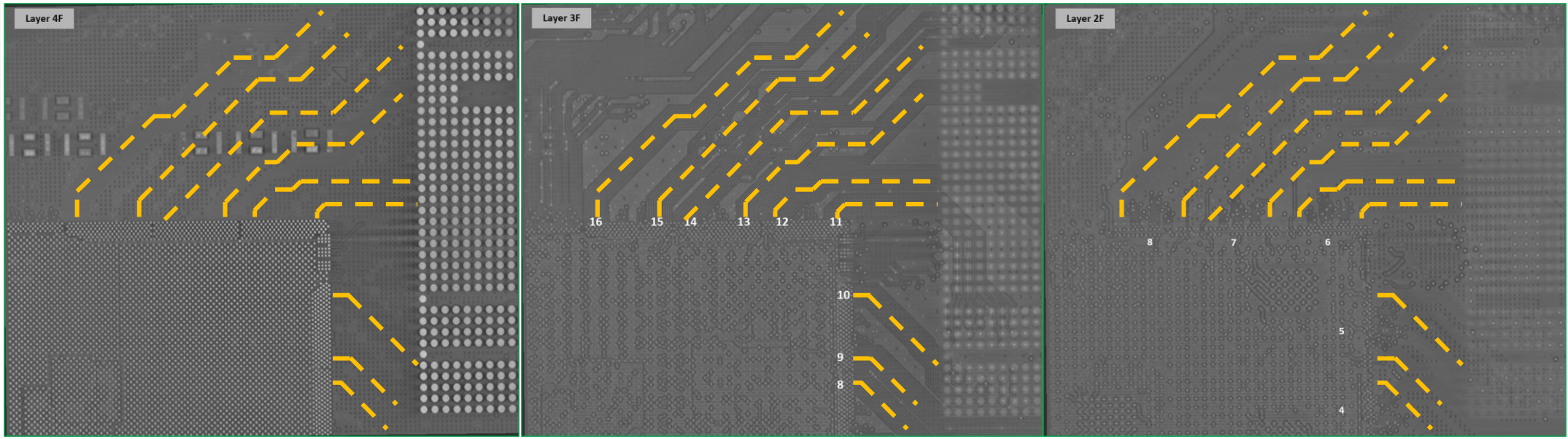


FLI & DRAM Interconnect Map – X-Ray View

- 8 sets of 11 traces exiting through each side of the SoC from the LPDDR IP block.
- The PCB has solid ground planes directly below 3F LPDDR Signal for full referencing which should help signal integrity.

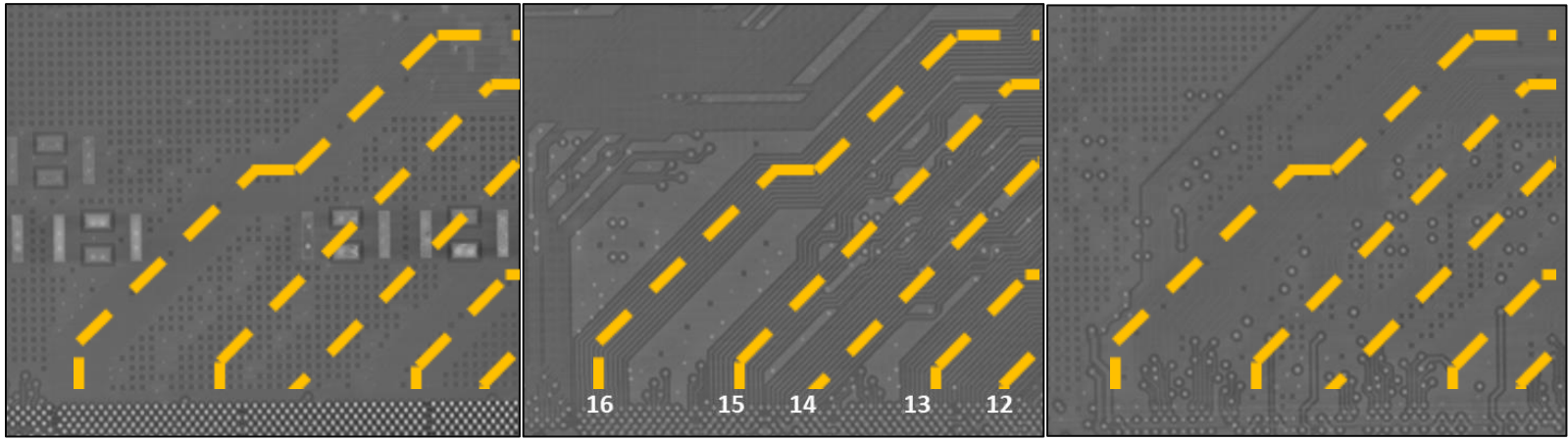
PCB Substrate Layer 2F – X-Ray View

M1 PCB Substrate – X-Ray



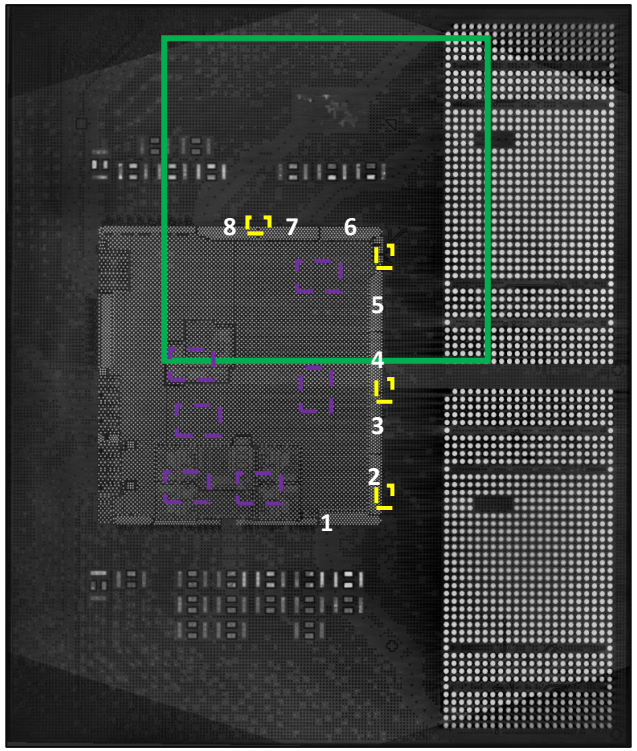
PCB Substrate Layer Full Plane Referencing – X-Ray View

- Not all routing from the SoC die to the DRAM have the same referencing.
- Only the channels 8-2 (16), 7-1 (13), 1-1 (1) has a full plane referencing.
- All other channels have adhesion square feature in the ground plane, but it should be enough to improve the signal integrity.

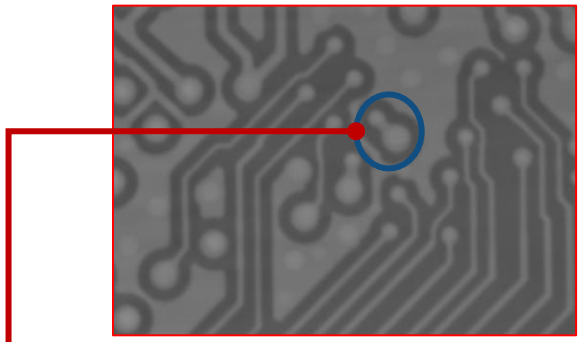


PCB Substrate Layer Full Plane Referencing – X-Ray View

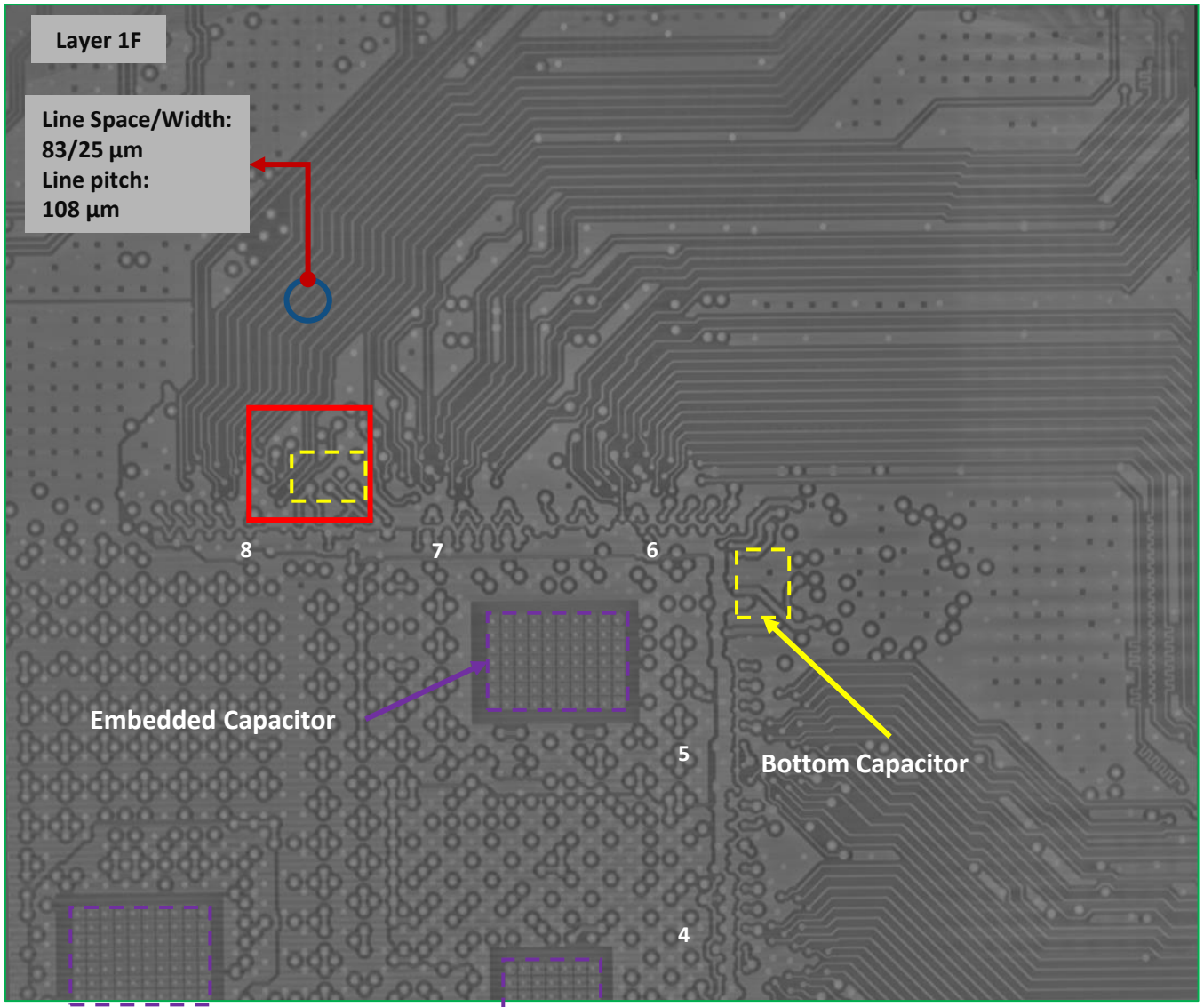
M1 PCB Substrate – X-Ray



FLI & DRAM Interconnect Map – X-Ray View

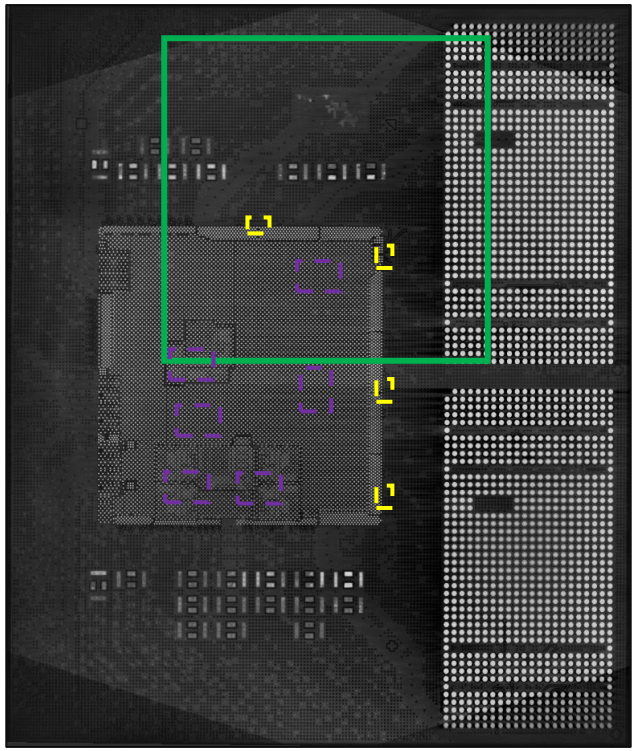


Via pad size: **56 µm**
LTH pad: **100 µm**



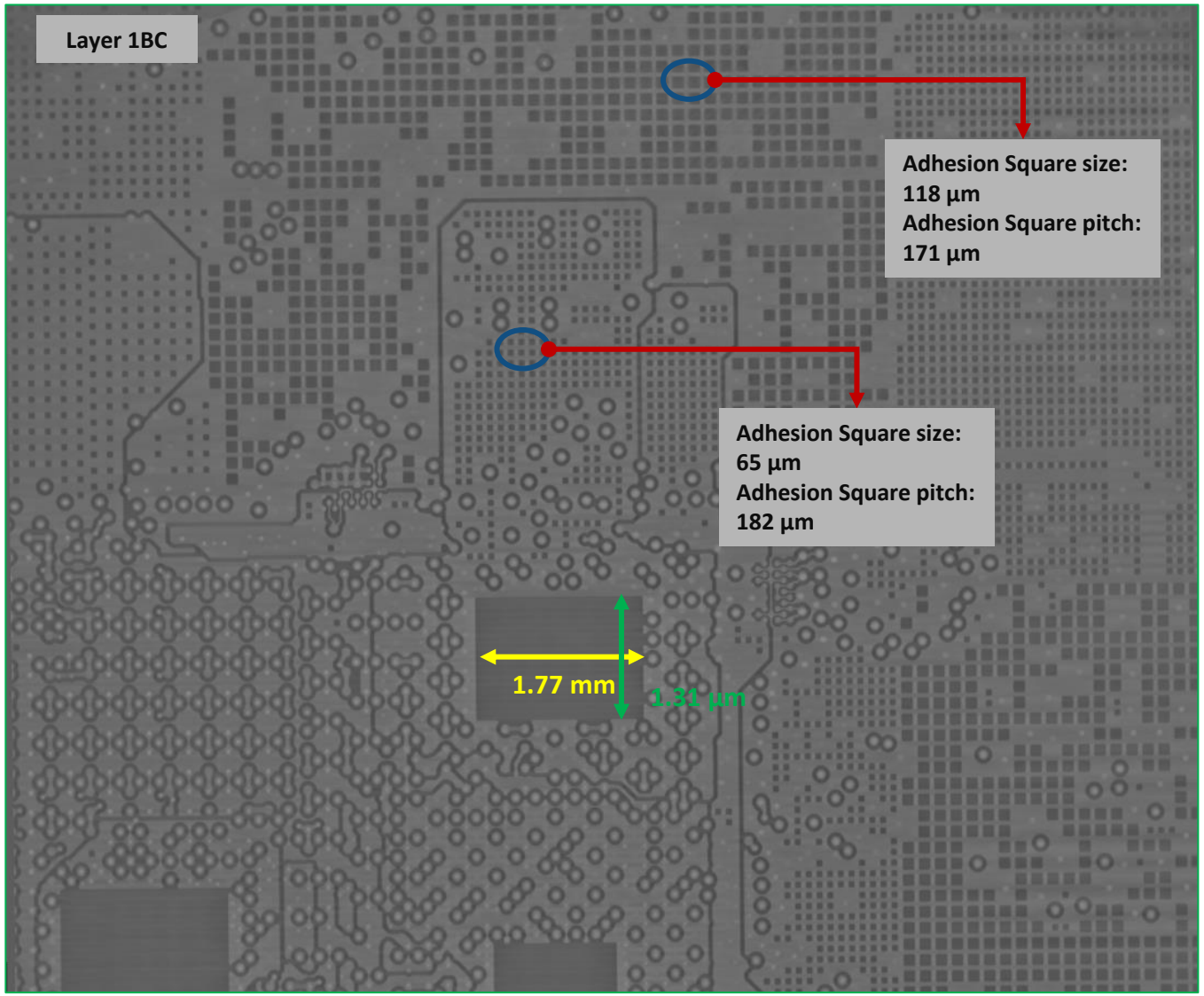
PCB Substrate Layer 1F – X-Ray View

M1 PCB Substrate – X-Ray



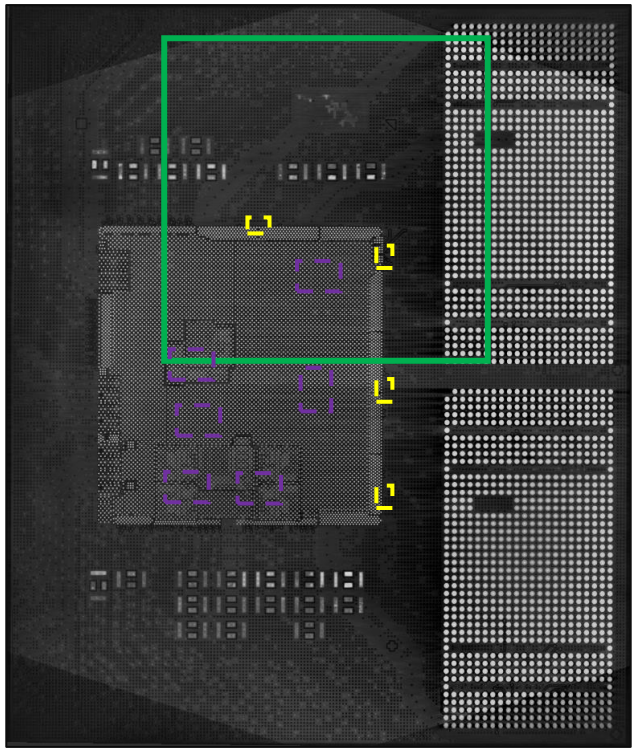
FLI & DRAM Interconnect Map – X-Ray View

- The layer 1BC is not used for routing. Only small lines are trace for LTH-micro-via interconnection.
- Two type of adhesion feature are implemented in the bottom PCB.



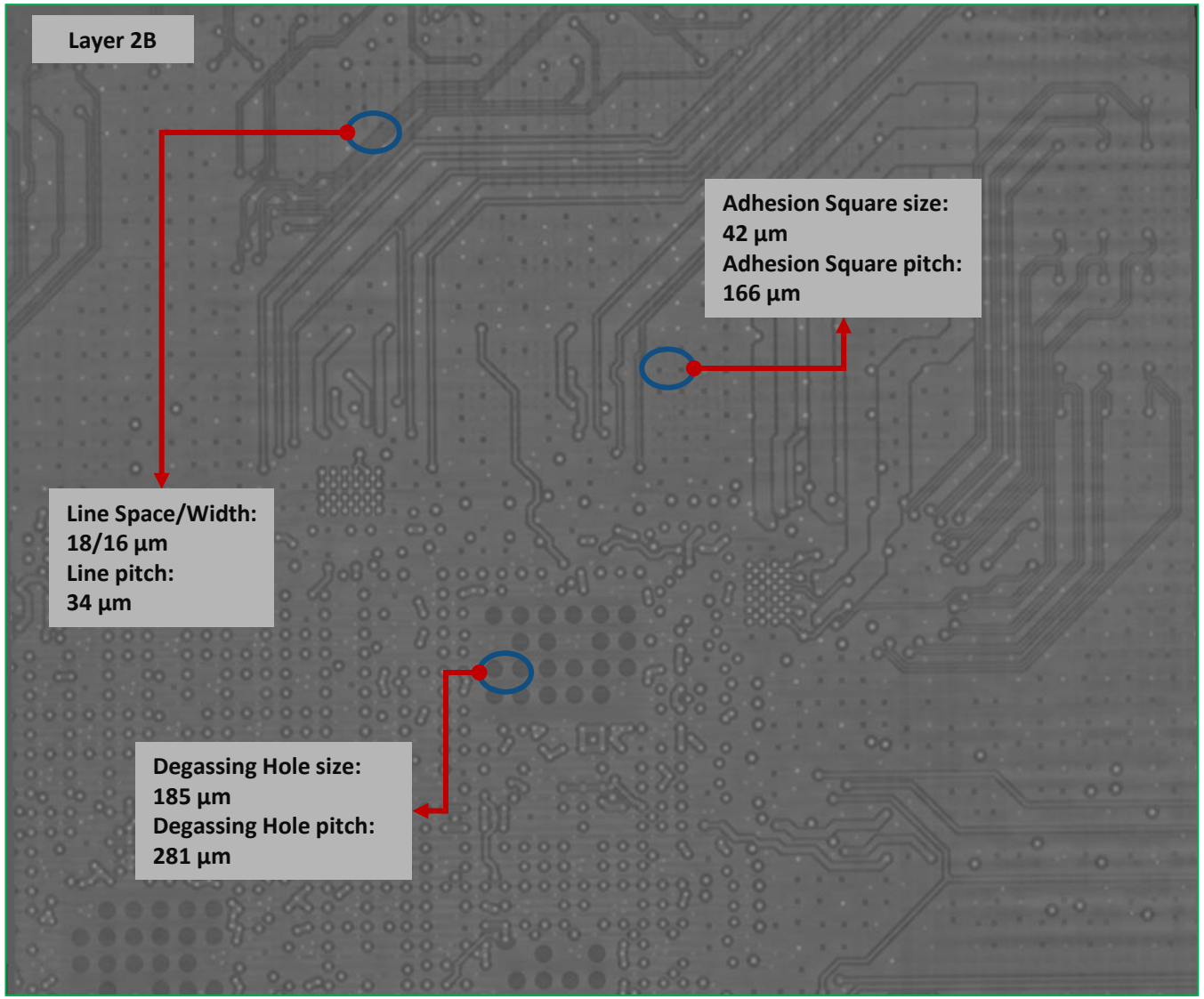
PCB Substrate Layer 1BC – X-Ray View

M1 PCB Substrate – X-Ray



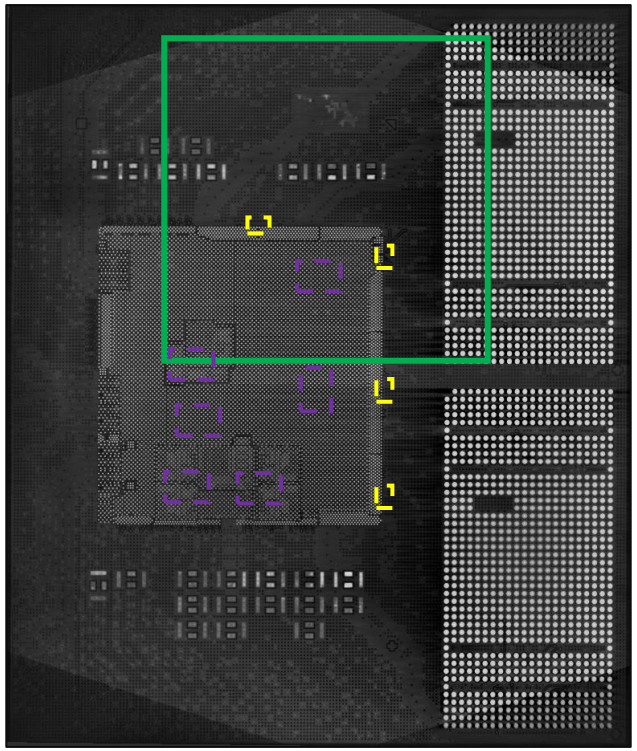
FLI & DRAM Interconnect Map – X-Ray View

- The layer 2B is used for routing.
- Widespread adhesion features are implemented in this layer of the bottom PCB along with large degassing hole below the Silicon capacitor substrate.



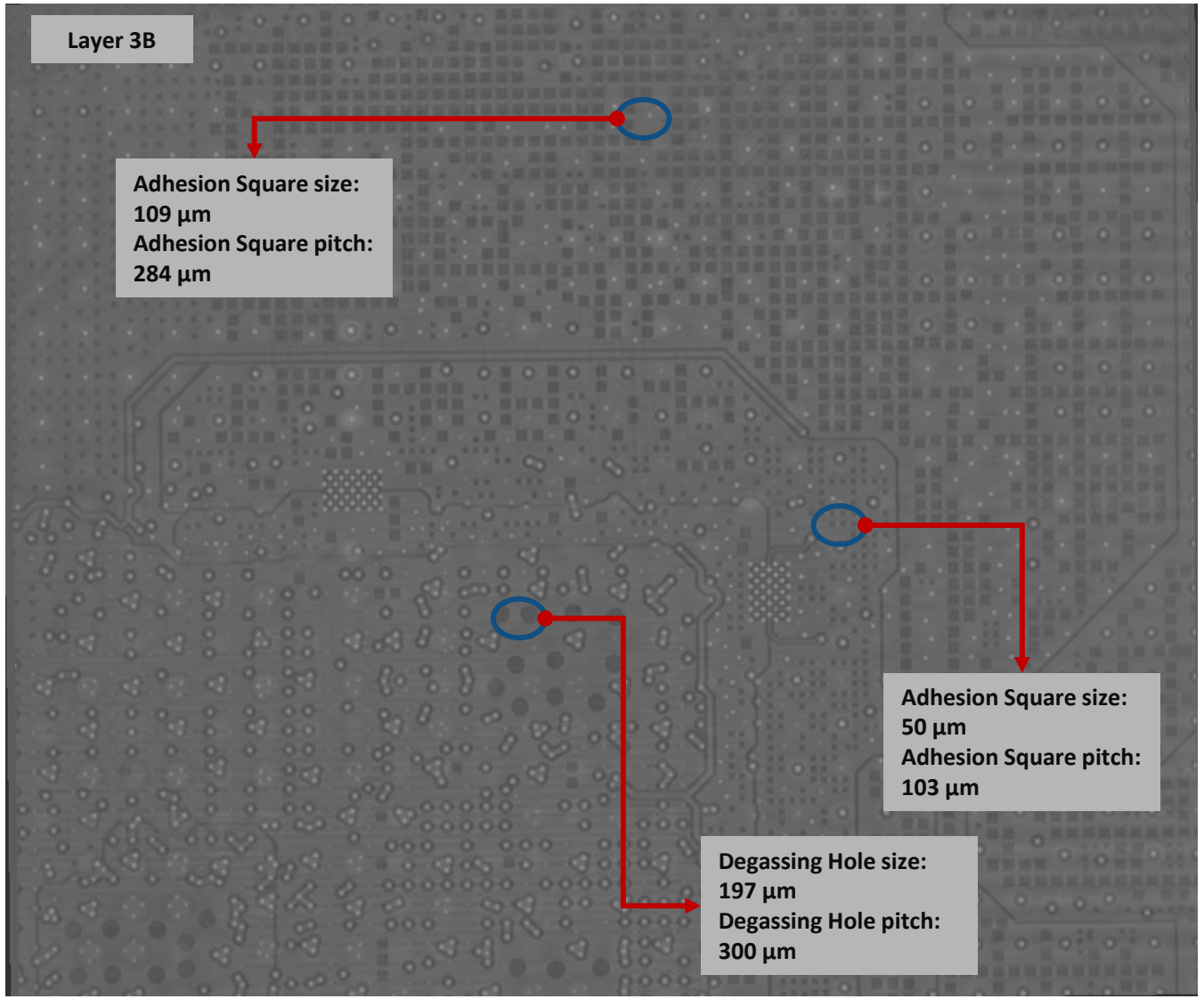
PCB Substrate Layer 2B – X-Ray View

M1 PCB Substrate – X-Ray



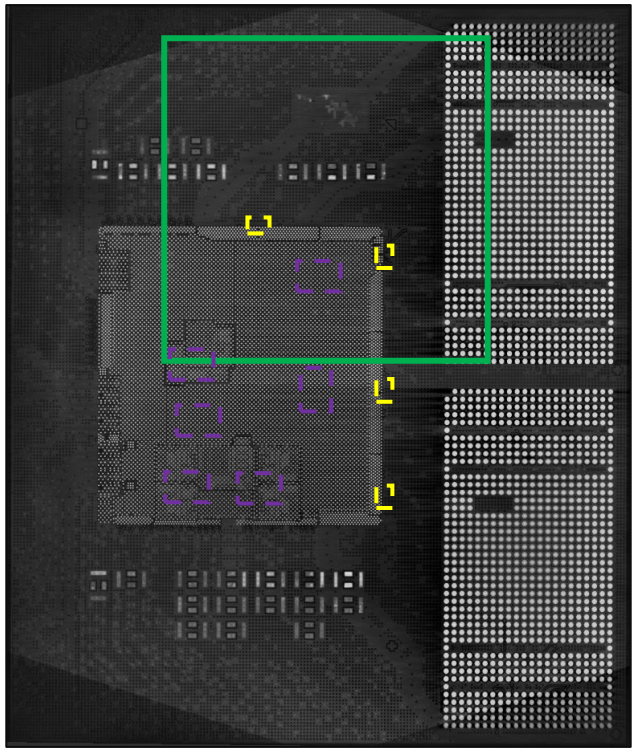
FLI & DRAM Interconnect Map – X-Ray View

- The layer 3B is not used for routing.
- Two type of adhesion feature are implemented in the bottom PCB.
- The orientation of the degassing hole suggests a built-up process.

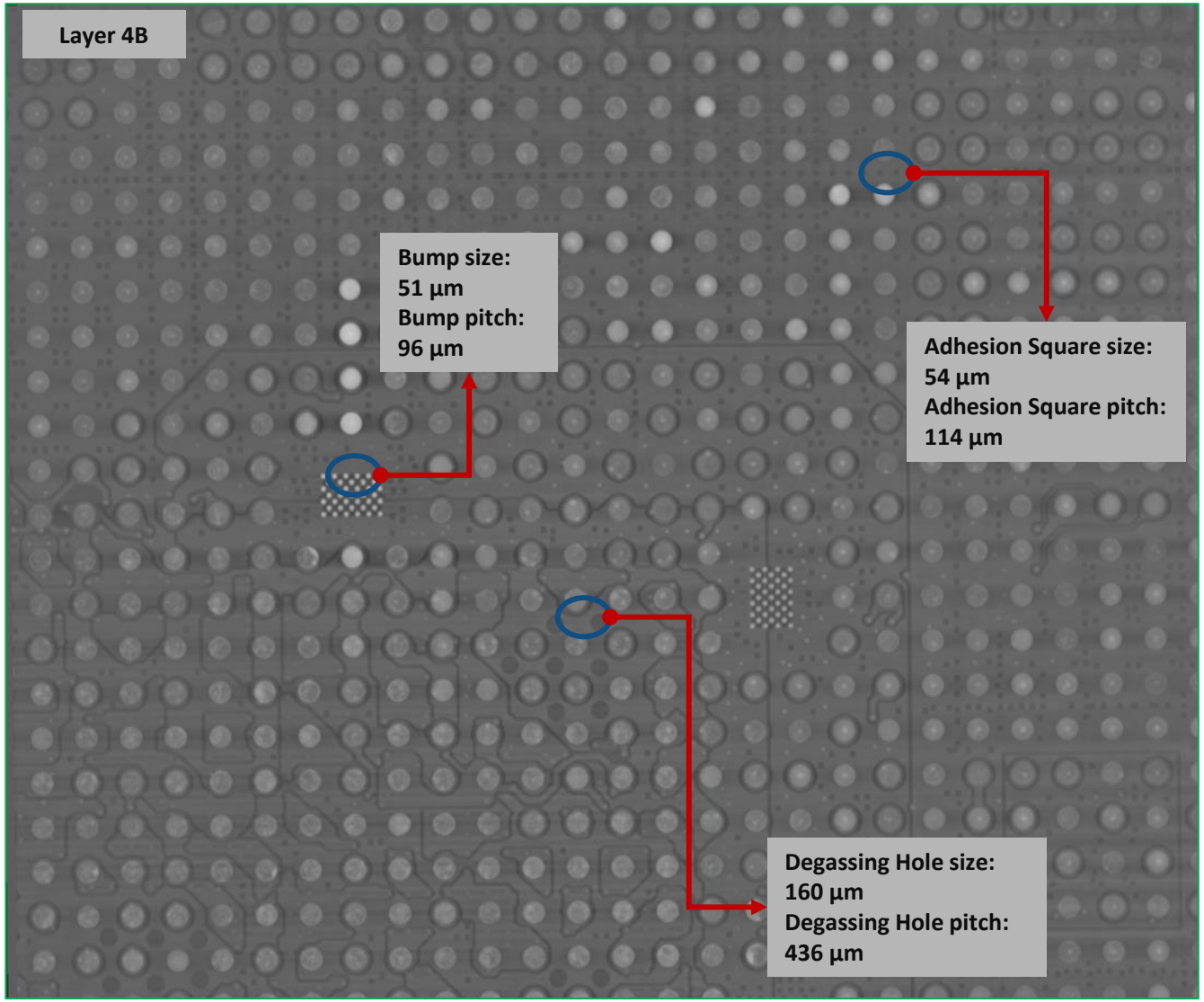


PCB Substrate Layer 3B – X-Ray View

M1 PCB Substrate – X-Ray

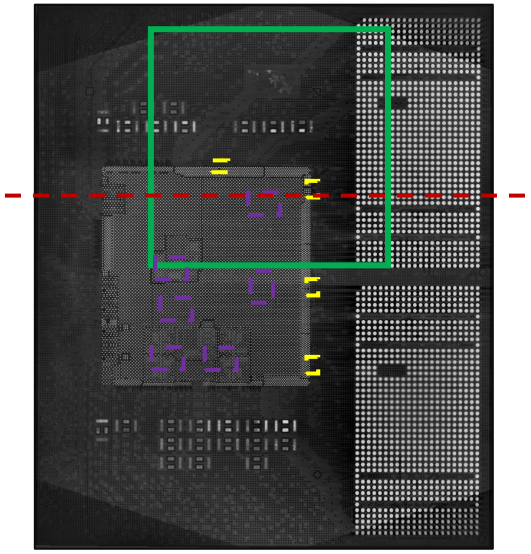


FLI & DRAM Interconnect Map – X-Ray View

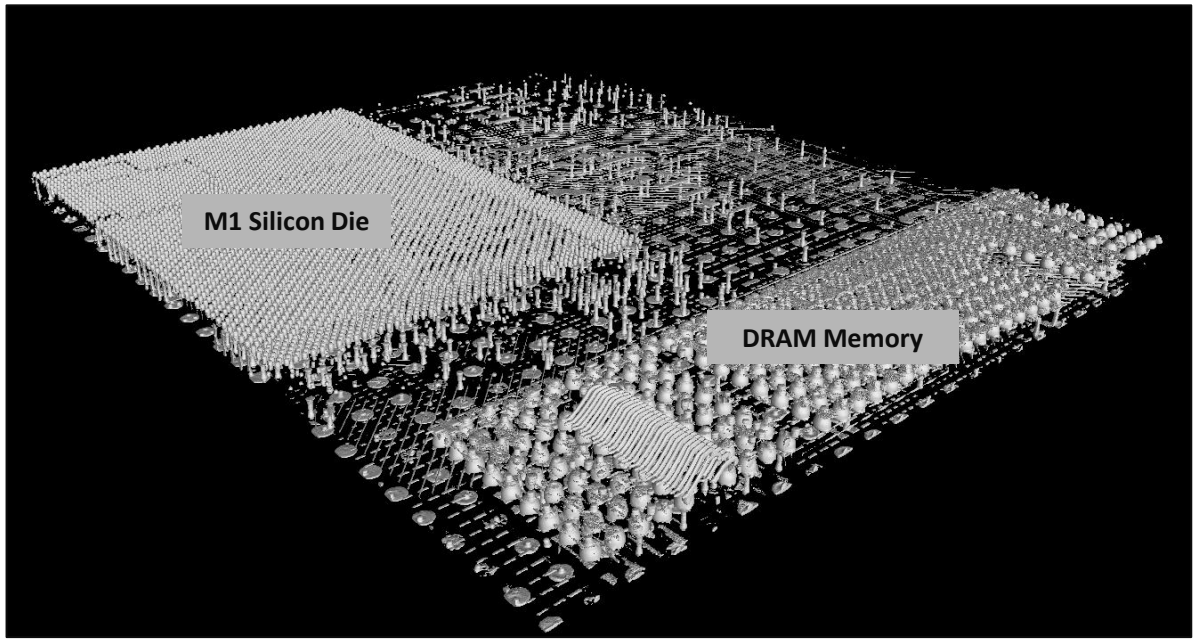


PCB Substrate Layer 4B – X-Ray View

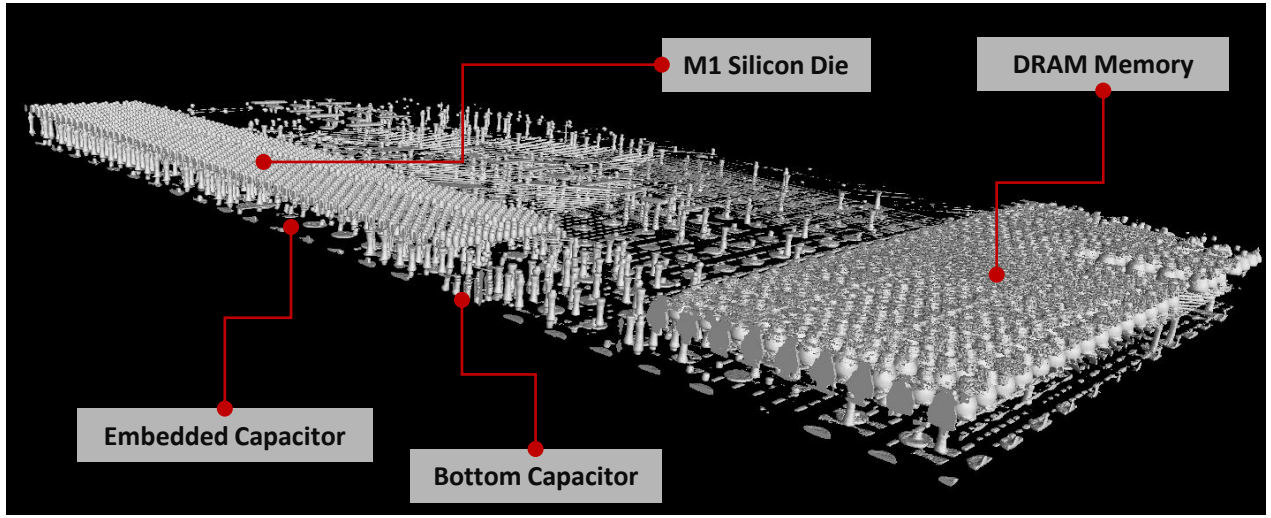
M1 Package Overview- X-Ray



FLI & DRAM Interconnect Map – X-Ray View



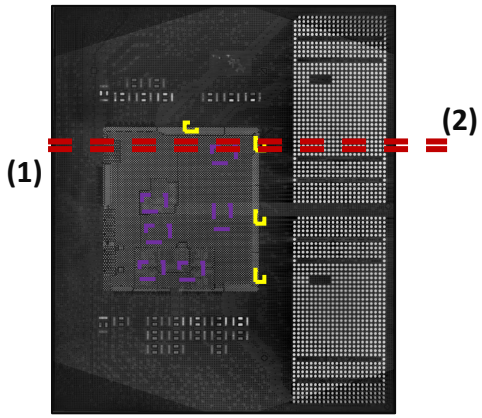
Package overview – X-Ray View



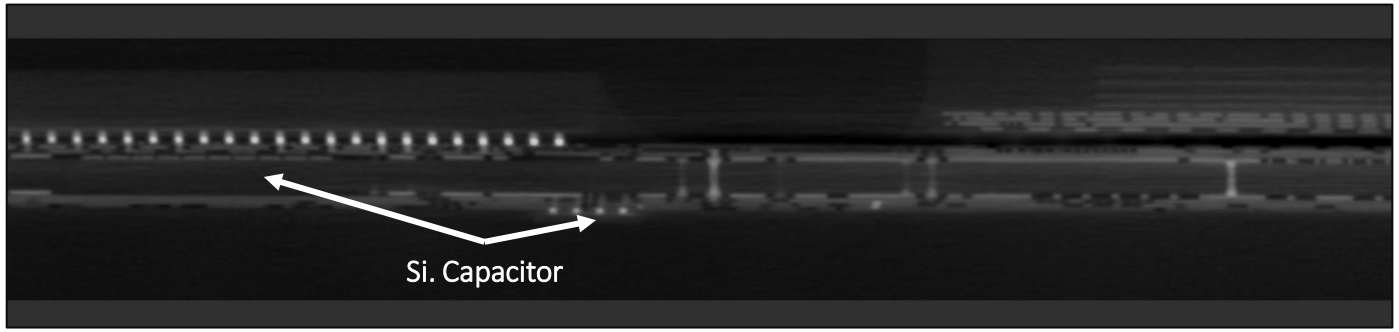
Package overview – X-Ray View

- The DRAM memory uses two line of wire bonding at the North and South side of the component. Additional wire bonding (2/side) are placed at the East and West side of the component

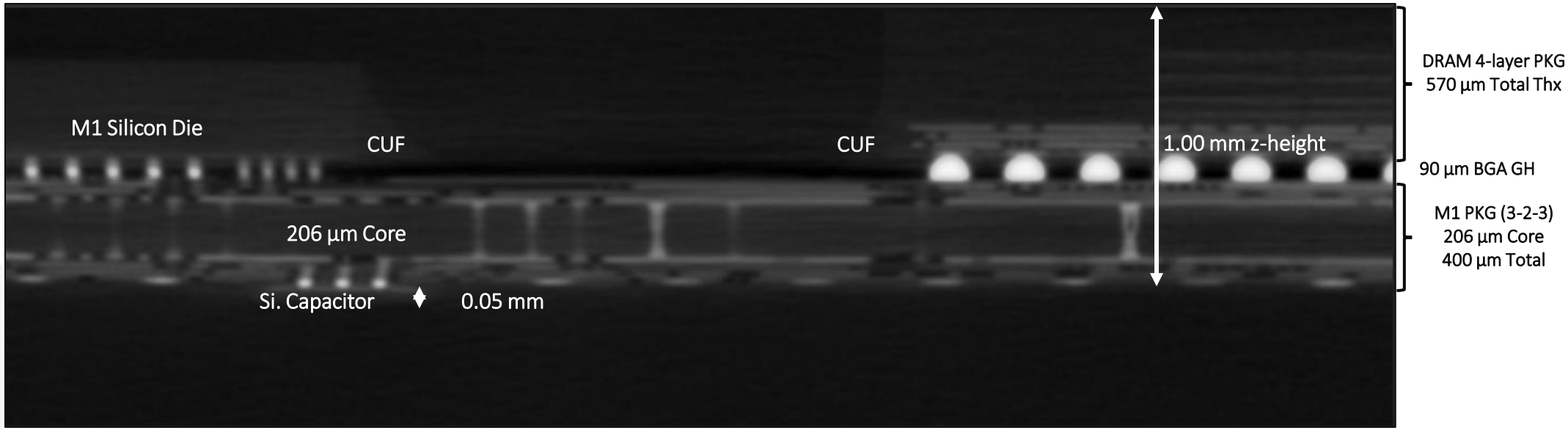
M1 Package Cross-Section - X-Ray



FLI & DRAM Interconnect Map – X-Ray View

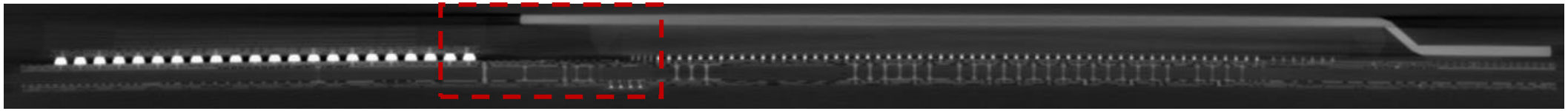


Package Cross-Section (1) – X-Ray View

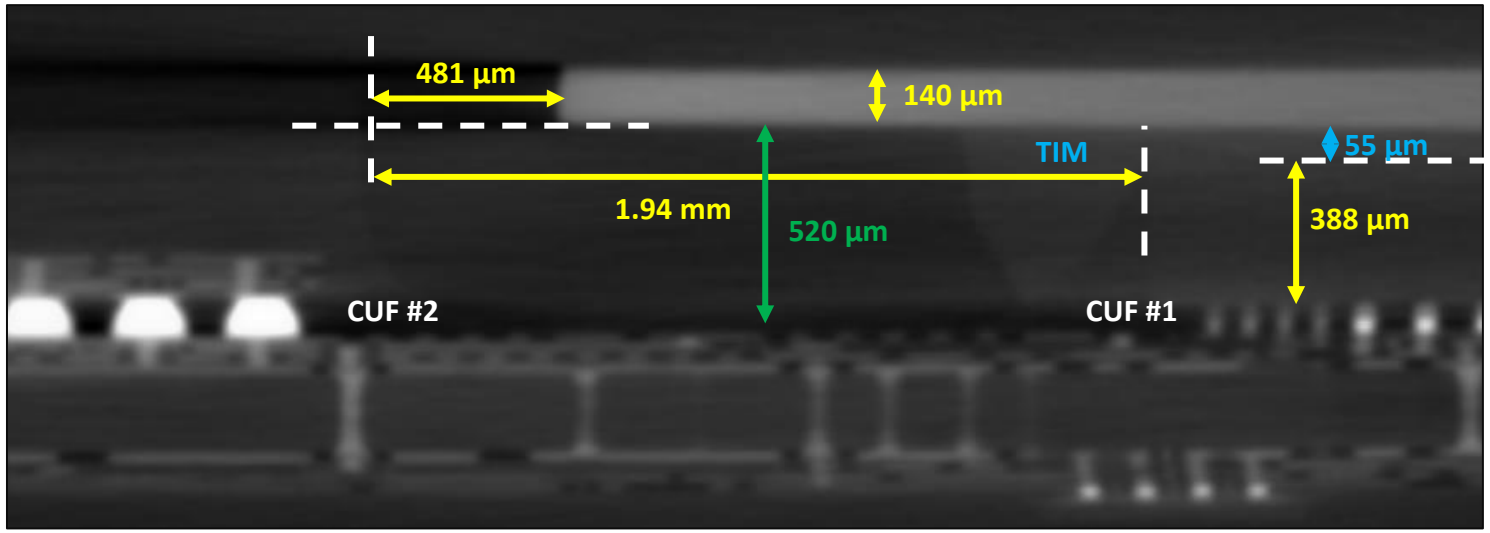


Package Cross-Section (2) – X-Ray View

M1 Package Cross-Section - X-Ray



Package Cross-Section – X-Ray View

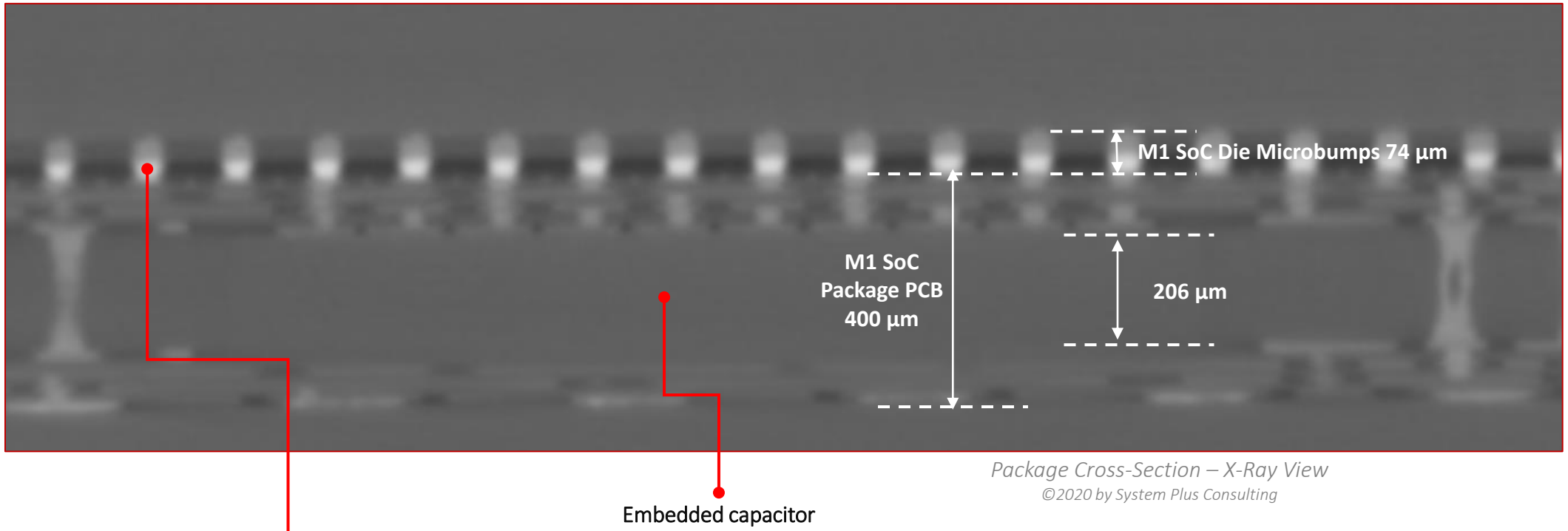


Package Cross-Section – X-Ray View

- IHS Thickness: 140 µm
- TIM BLT: 55 µm
- The M1 SoC die was attached and CUF's prior to the DRAM. The gap between the M1 SoC and the DRAM is large enough to avoid the overlap of the CUFs.
- Dispense location was likely between the two DRAMs.
- The IHS could not necessarily placed last.

M1 Package Cross-Section - X-Ray

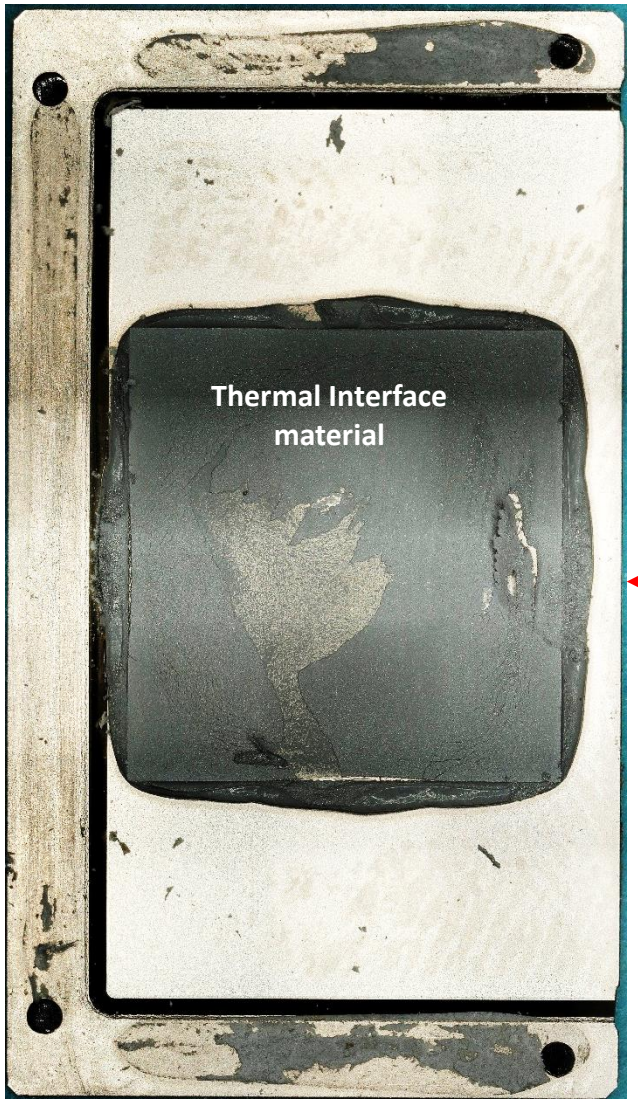
Package Cross-Section – X-Ray View



Package Cross-Section – X-Ray View

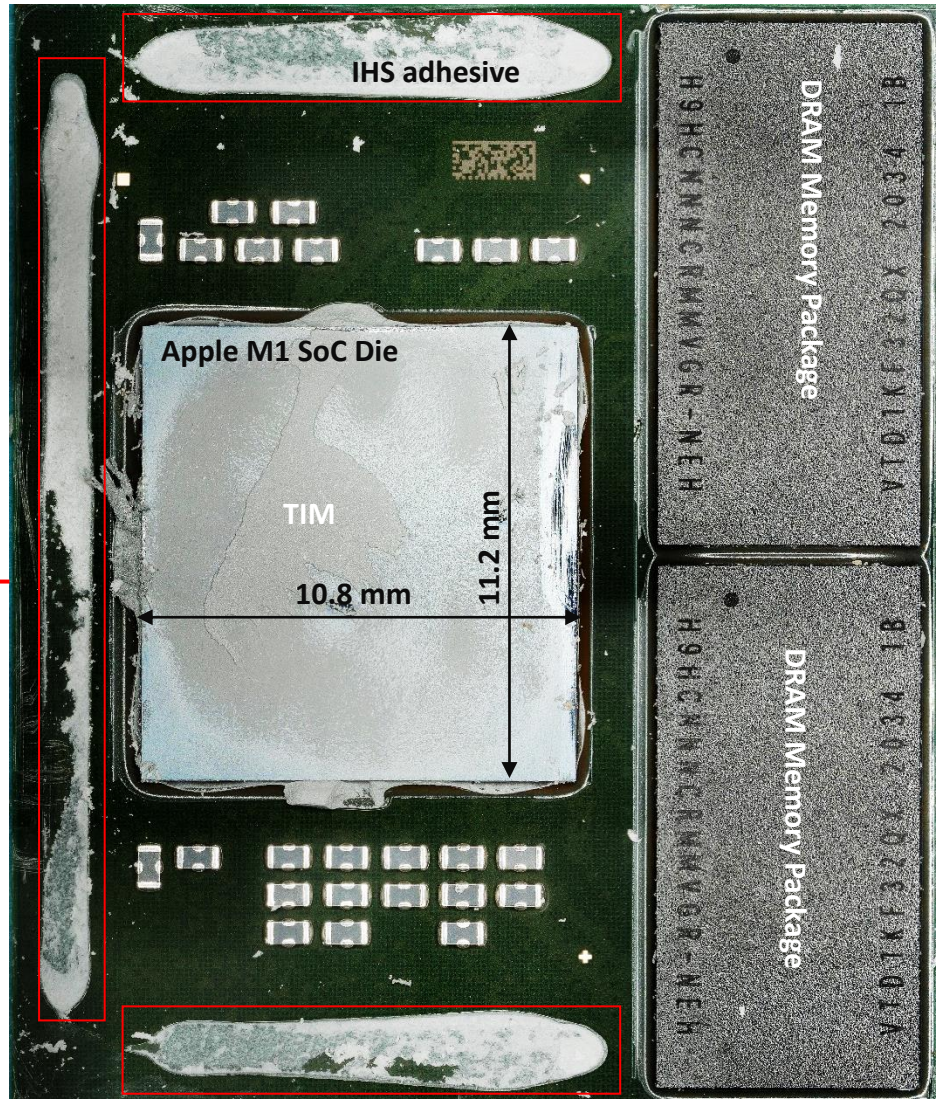
- M1 Die microbump Pitch: 112 µm
- Microbump Diameter: 56 µm

M1 Package Opening



Package Opening/IHS Removal

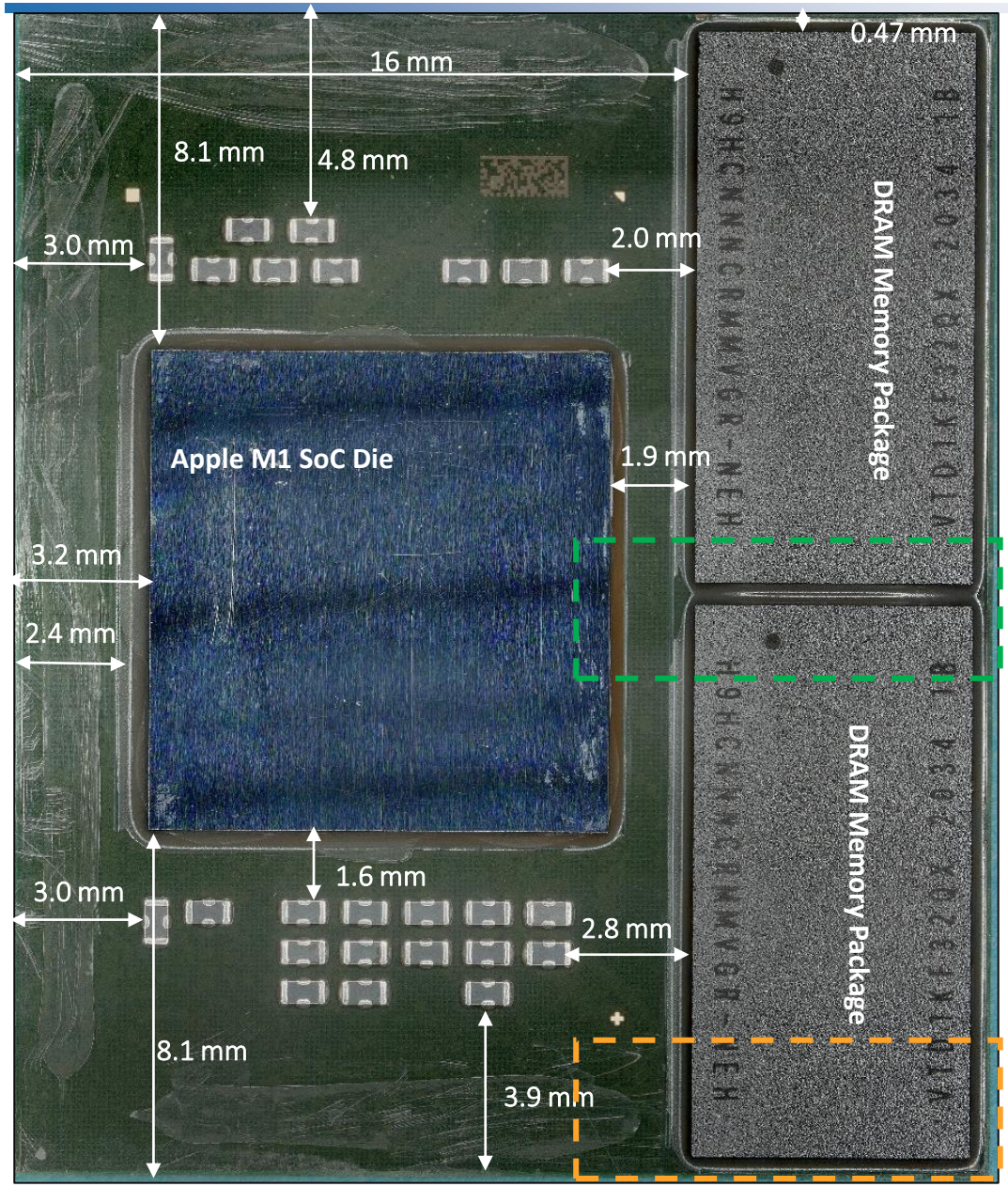
Metal Cover (IHS) Removal



Package Opening/ Metal cover removal

- Thermal Interface material (TIM) is used as an interface between the M1 SoC Die and the top metal cover to maximize heat dissipation.

M1 Package Opening



Package Opening/ Metal cover and TIM removal

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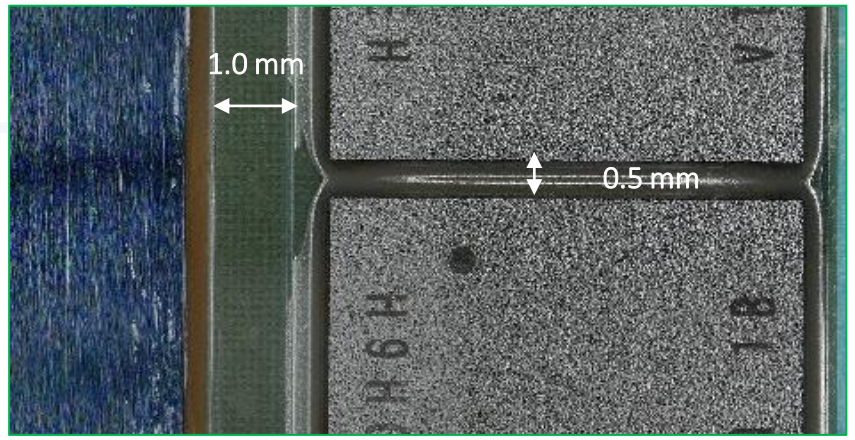

Package Opening

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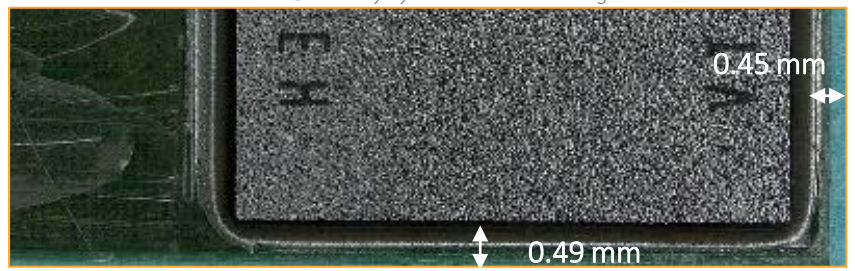

Package Opening

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- The M1 packages contains 24 passive capacitors positioned on the front side of the M1 SoC Package PCB.
- Passive Components on PCB: 24 (0402) Capacitors.

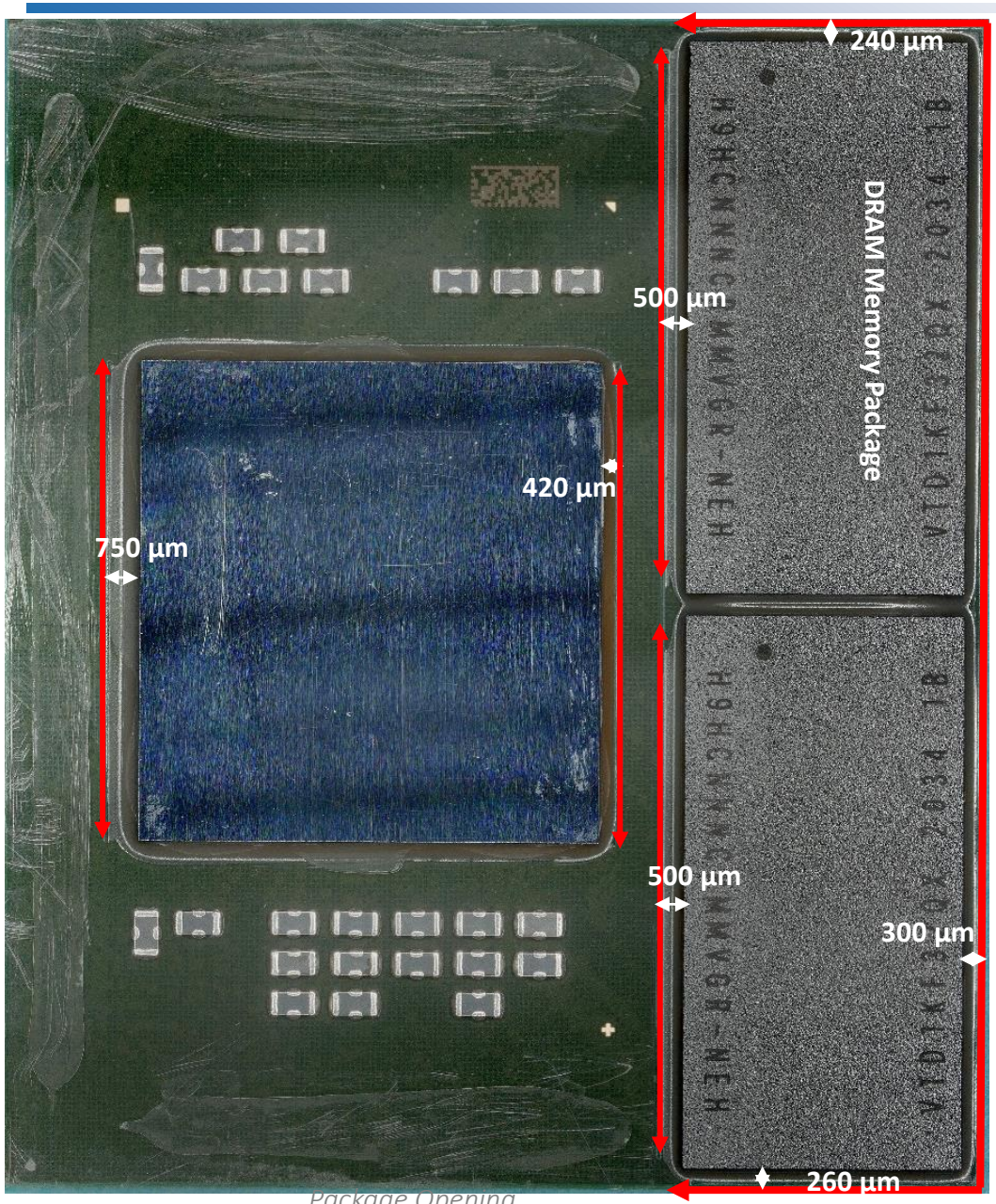
Component to Edge :

- Top DRAM to package substrate : 0.47 mm
- Bottom DRAM to Package substrate edge: 0.49 mm
- DRAM Package to Package substrate edge(x-Axis): 0.45mm
- M1 SoC Die to Package substrate edge (x axis): 3.2 mm
- M1 SoC Die to Package substrate edge (y axis): 8.1 mm

Component to Component

- DRAM Package to DRAM Package : 0.5 mm
- DRAM Package to M1 SoC Die : 1.9 mm

M1 Package Opening



Package Opening
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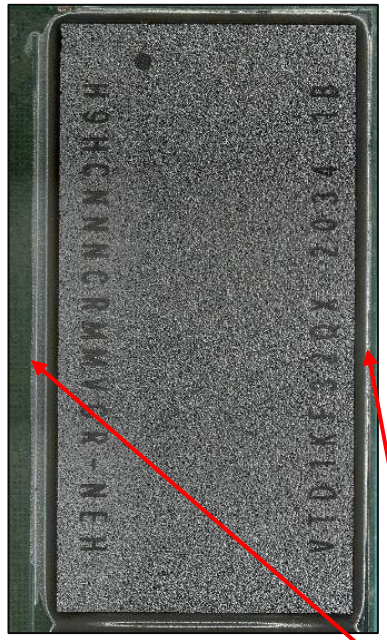
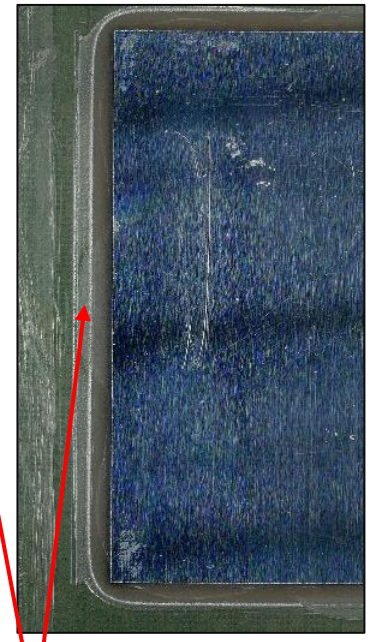


Package Opening
©2020 by System Plus Consulting



Package Opening
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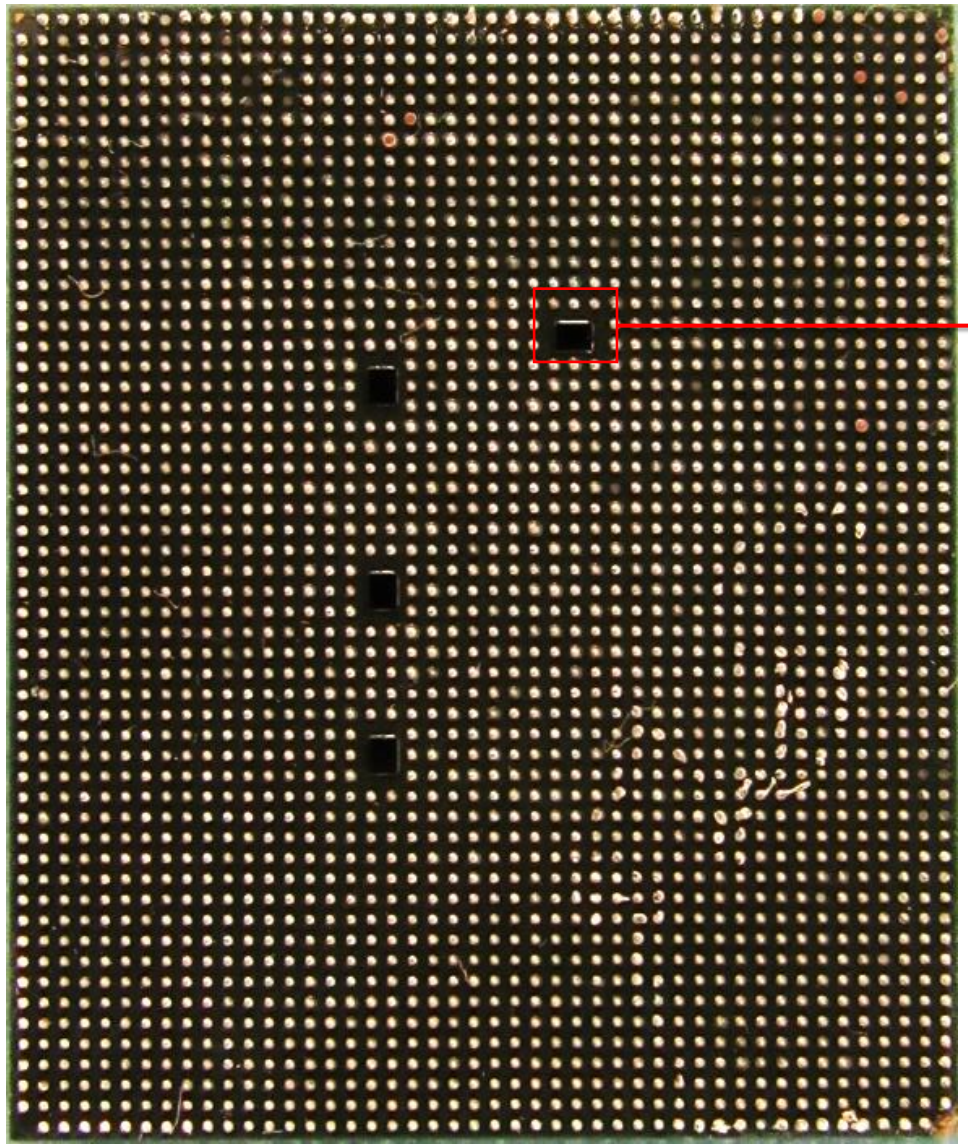
solder resist

Solder resist is deposited to limit underfill diffusion.

- SoC Die to solder resist dam left: 750 µm
- SoC Die to solder resist dam right: 420 µm

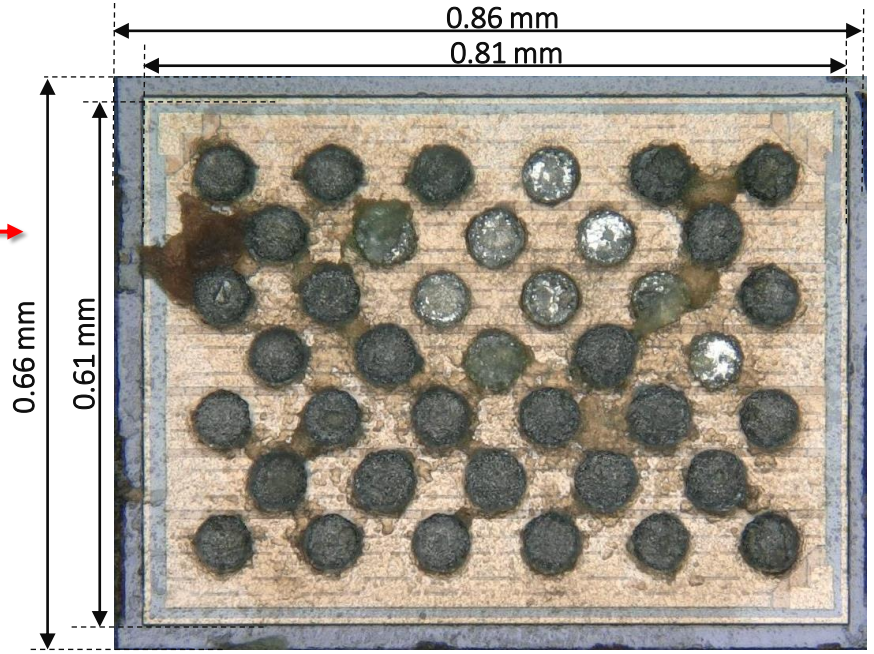
- DRAM Package to solder resist dam y axis top : 240 µm
- DRAM Package to solder resist dam y axis bottom: 260 µm
- DRAM Package to solder resist dam x axis left: 500 µm
- DRAM Package to solder resist dam x axis right: 300 µm

Package Opening



Package Back View

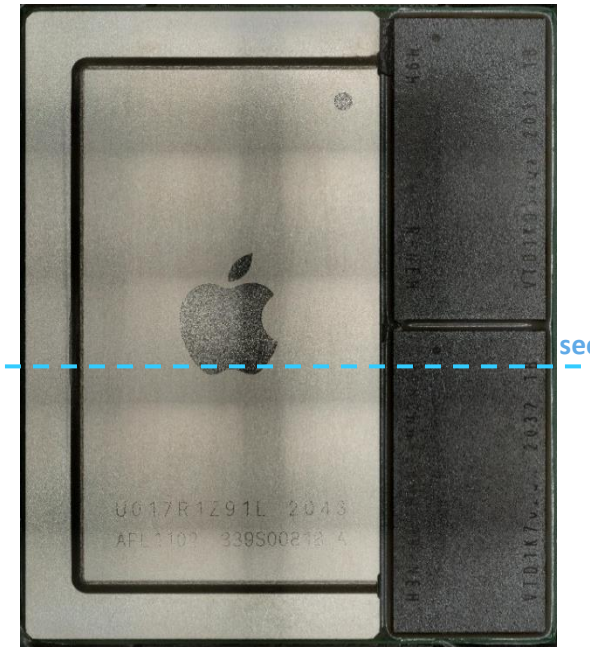
- 4 Capacitor dies are integrated on the Package PCB.



Capacitor Die

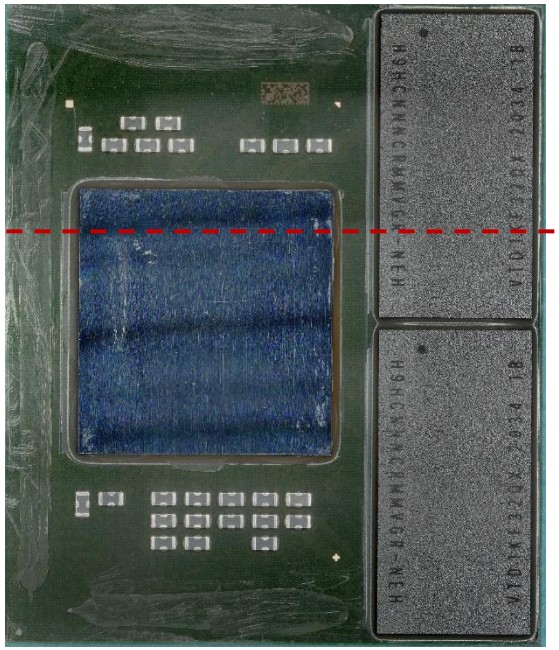
- Die Dimensions: 0.61 x 0.81 mm
- Balls: 39

M1 Package Cross-Section

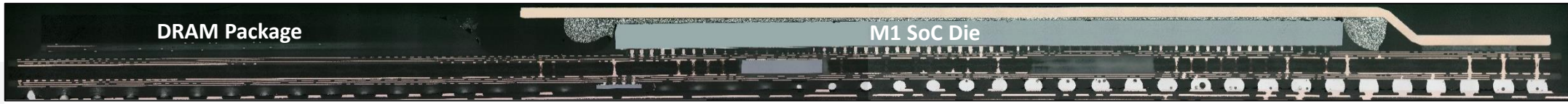


M1 SoC Package (Frontside) Cross Sectioning 1
©2020 by System Plus Consulting

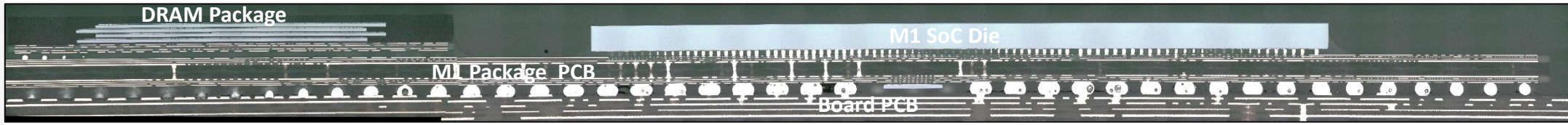
M1 SoC Package (Backside) Cross Sectioning
©2020 by System Plus Consulting



M1 SoC Package (Frontside) Cross Sectioning 2
©2020 by System Plus Consulting

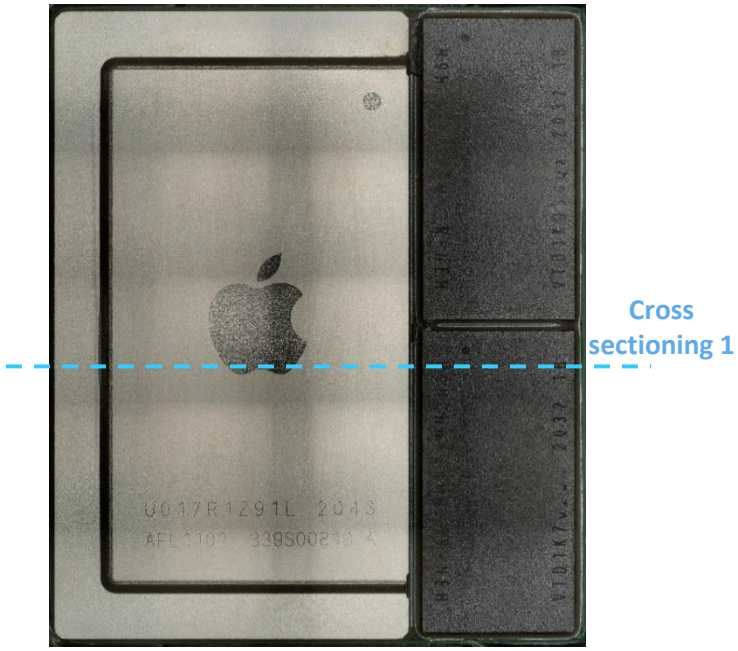


M1 SoC Package Cross Section 1
©2020 by System Plus Consulting

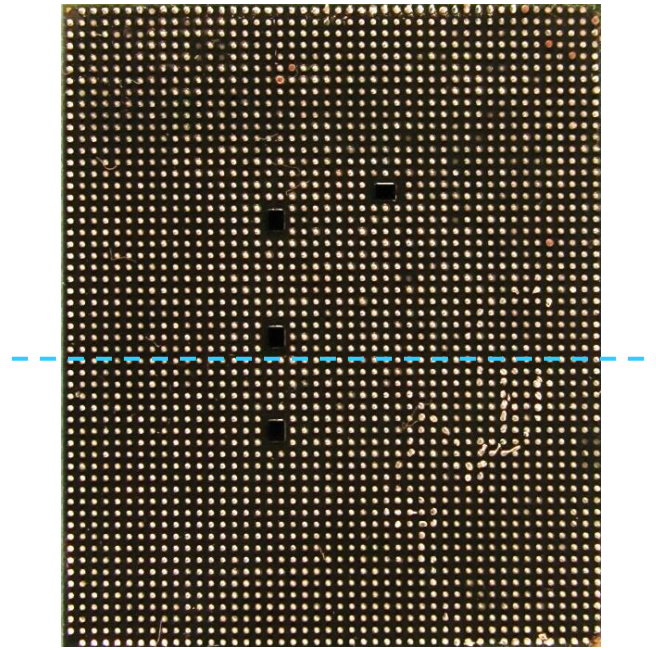


M1 SoC Package Cross Section 2
©2020 by System Plus Consulting

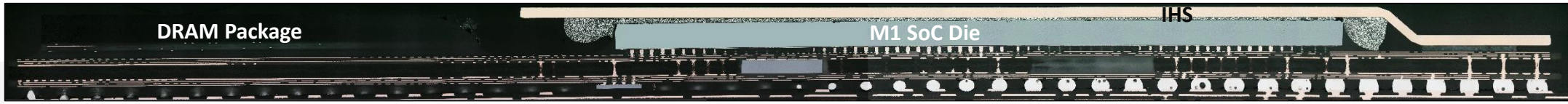
M1 Package Cross-Section 1



M1 SoC Package (Frontside) Cross Sectioning 1

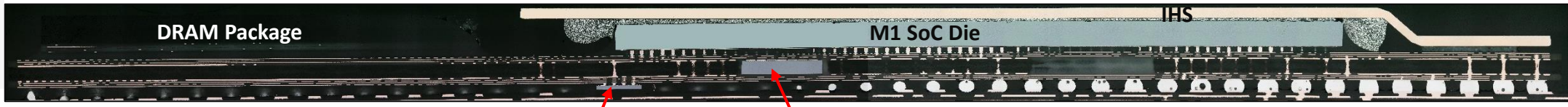


M1 SoC Package (Backside) Cross Sectioning



M1 SoC Package Cross Section 1

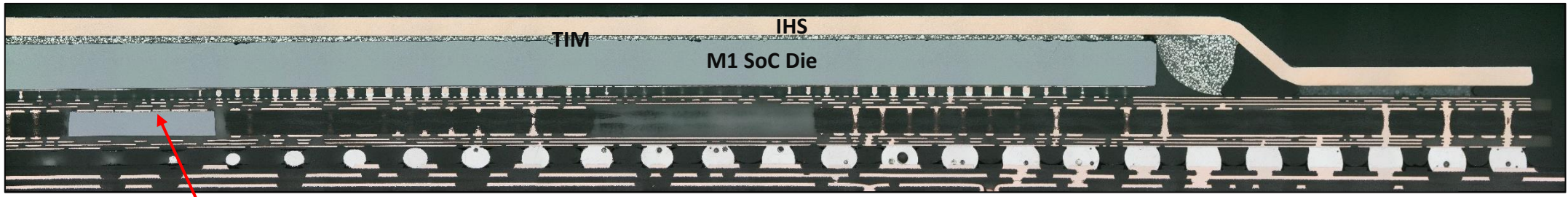
M1 Package Cross-Section 1



M1 SoC Package Cross Section 1

Capacitor on PCB backside

Embedded capacitor

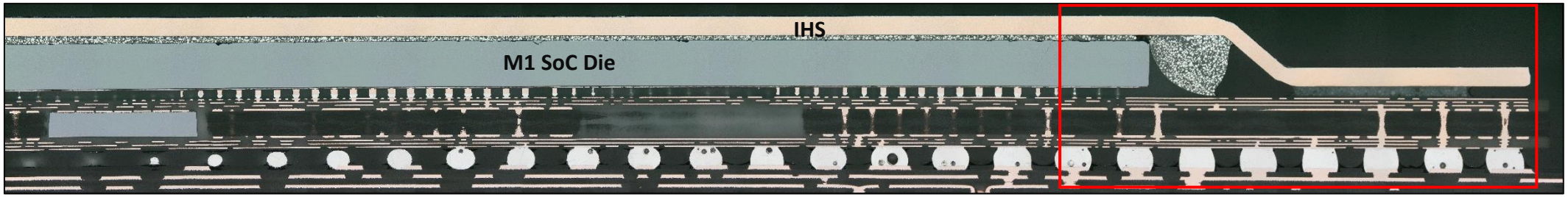


M1 SoC Package Cross Section 1

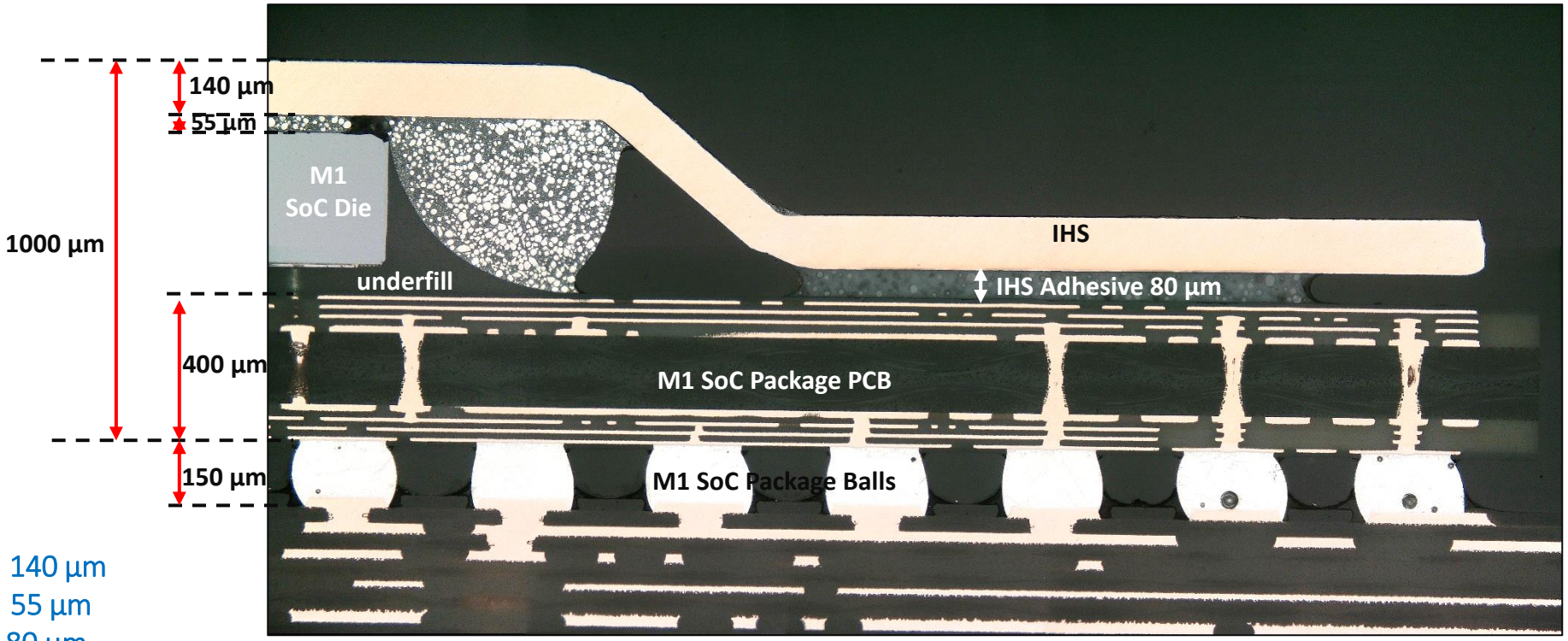
Embedded capacitor

- The IHS covers the M1 SoC Die and not the DRAM Memory Package.
- A TIM Material is placed between the M1 SoC Die that potentially produces heat and the IHS metal cover to enhance the thermal coupling between the die and the IHS.
- Capacitors are embedded in the M1 SoC Package.

M1 Package Cross-Section 1



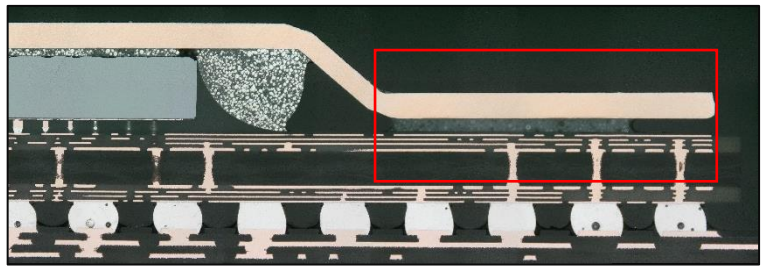
M1 SoC Package Cross Section 1



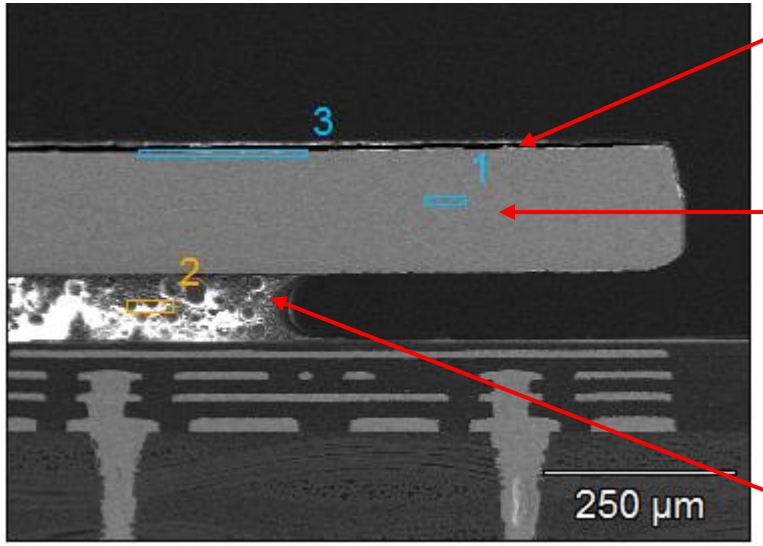
- IHS Thickness: 140 µm
- TIM Thickness: 55 µm
- IHS adhesive: 80 µm

M1 SoC Package Cross Section 1

M1 Package Cross-Section 1



M1 SoC Package Cross Section 1

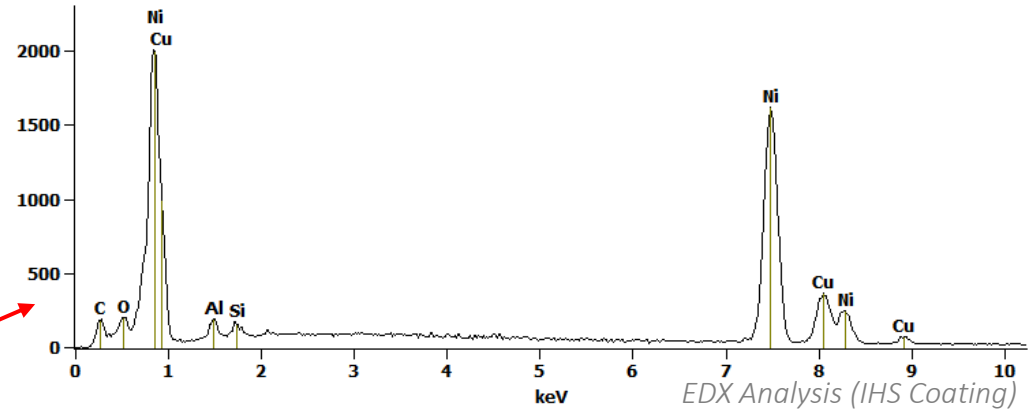


M1 SoC Package Cross Section 1

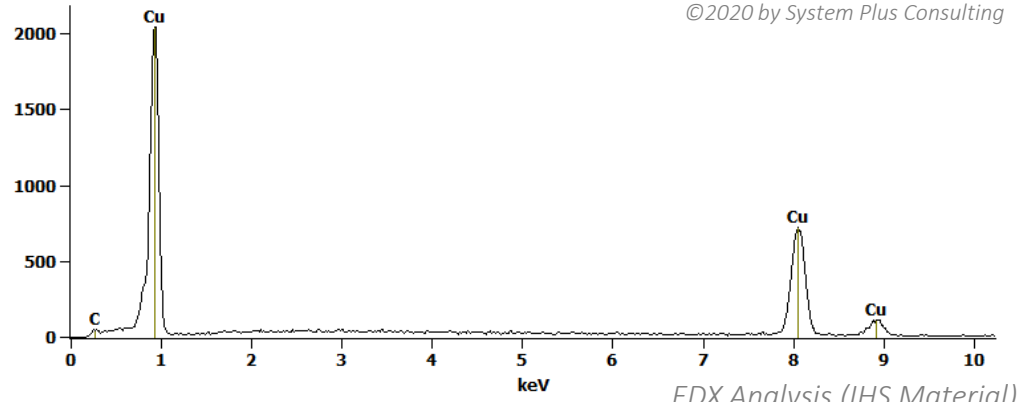
IHS Coating

IHS Material

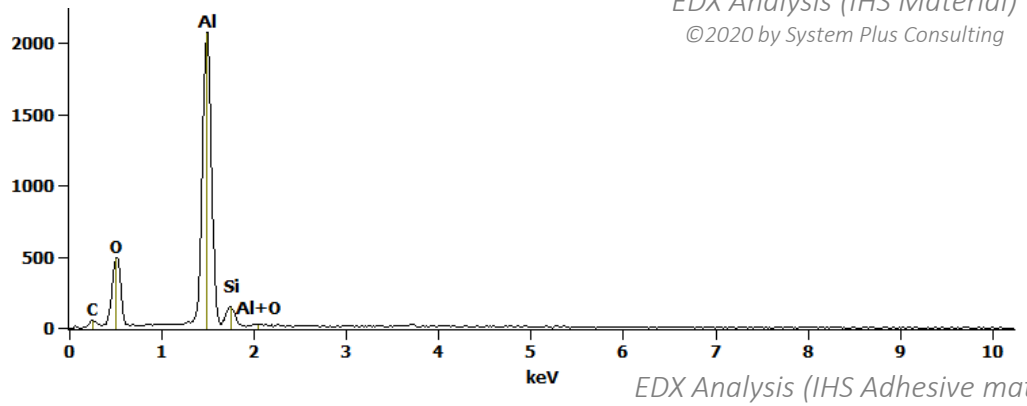
IHS Adhesive



EDX Analysis (IHS Coating)



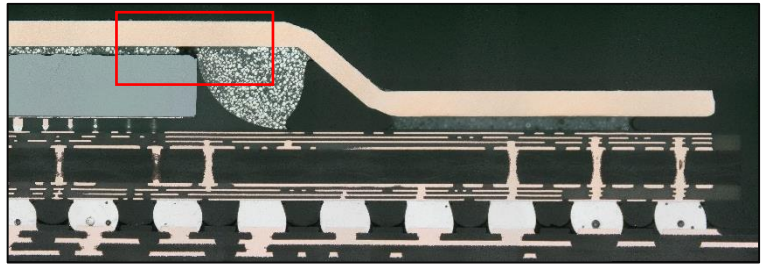
EDX Analysis (IHS Material)



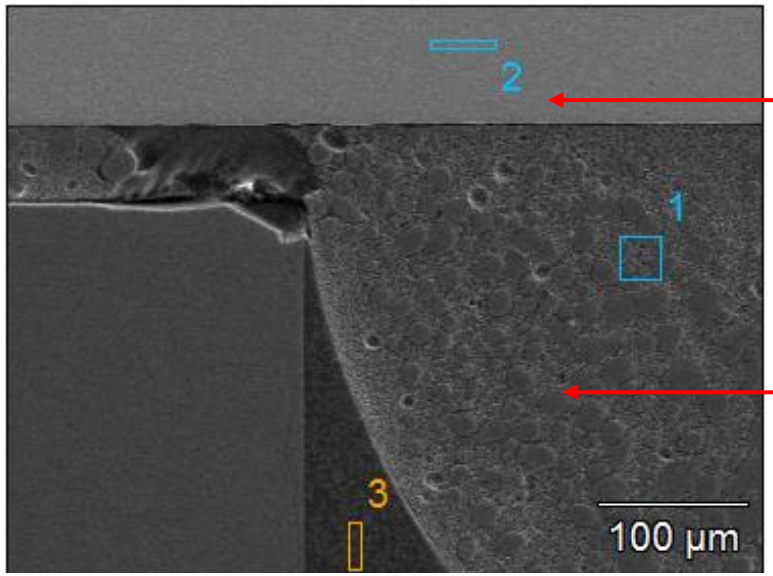
EDX Analysis (IHS Adhesive material)

- The IHS metal cover is made of Copper material.
- A thin layer of Nickel is used to coat the copper IHS.
- The IHS is attached to the Package PCB using an Aluminium/ Aluminium Oxide adhesive compound.

M1 Package Cross-Section 1

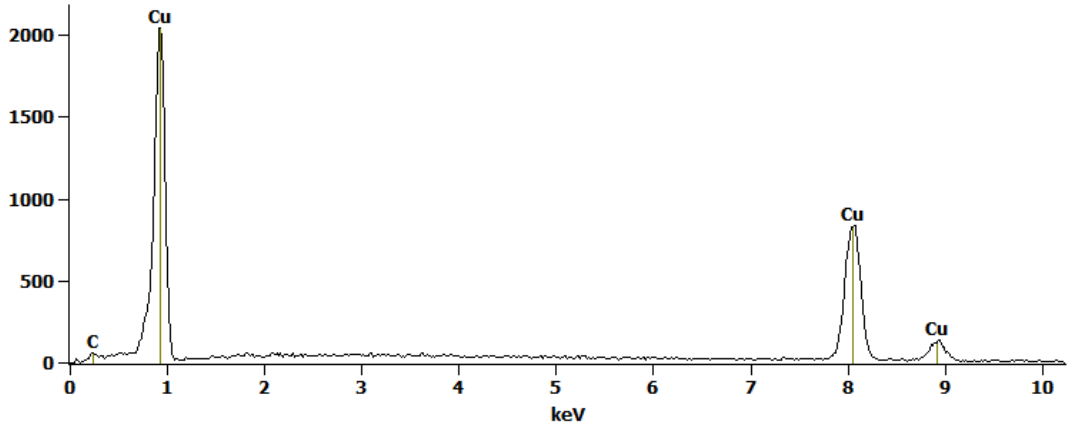


M1 SoC Package Cross Section 1



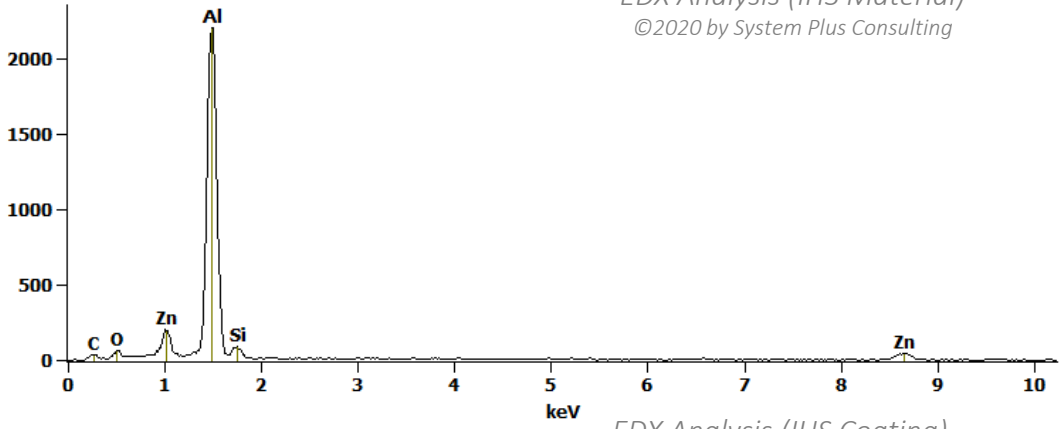
M1 SoC Package Cross Section 1

IHS Material



EDX Analysis (IHS Material)

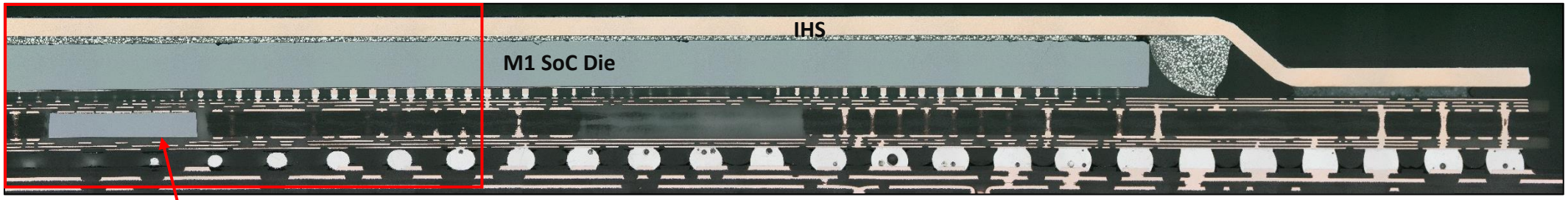
TIM Material



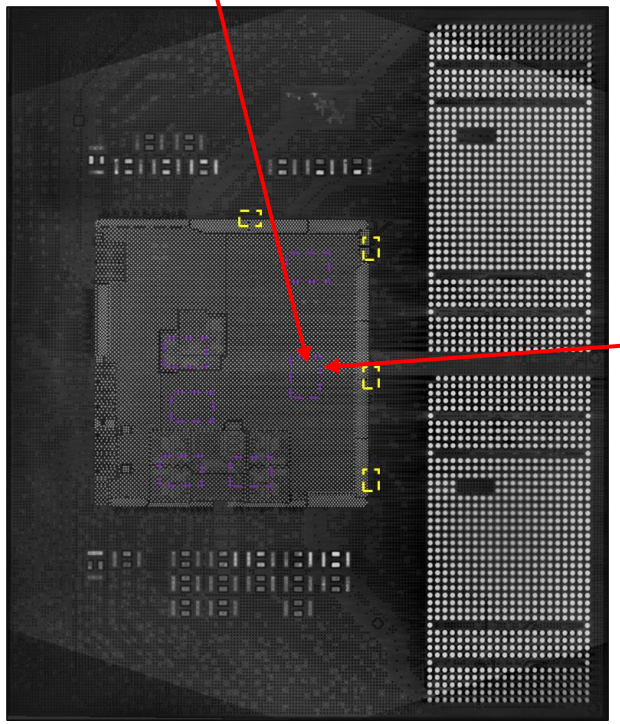
EDX Analysis (IHS Coating)

- The IHS metal cover is made of Copper material.
- The Thermal interface material (TIM) is made of an aluminium based compound with Zn traces.

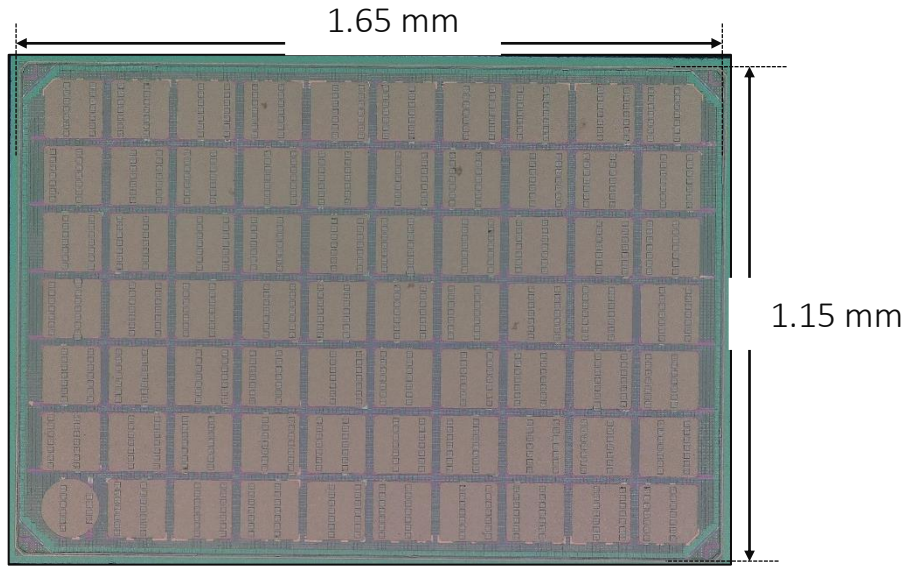
M1 Package Cross-Section 1



M1 SoC Package Cross Section 1



Embedded Capacitors Interconnect Map – X-Ray View



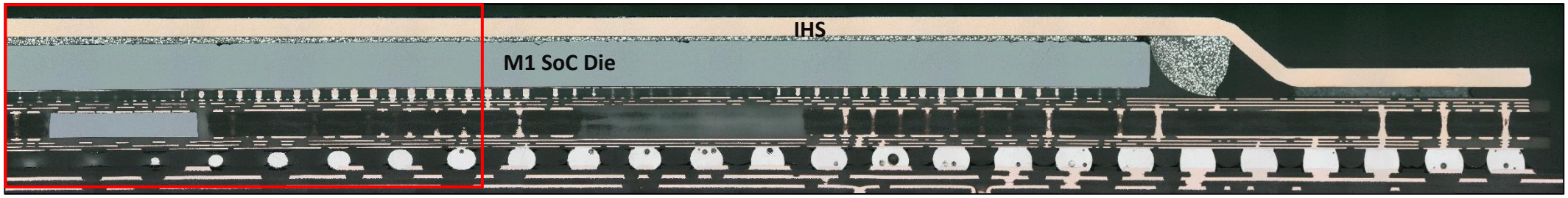
Capacitor Die

6 Capacitors are embedded in the M1 SoC Package PCB.

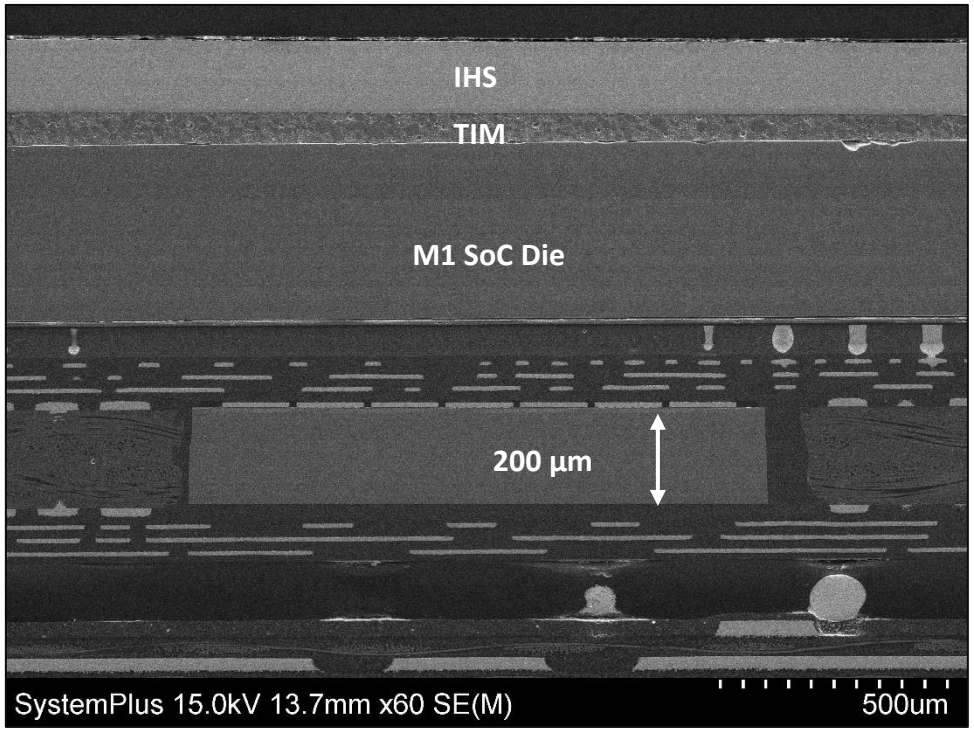
- Capacitor die Dimensions: 1.89 mm² (1.65 x 1.15 mm)

M1 Package Cross-Section 1

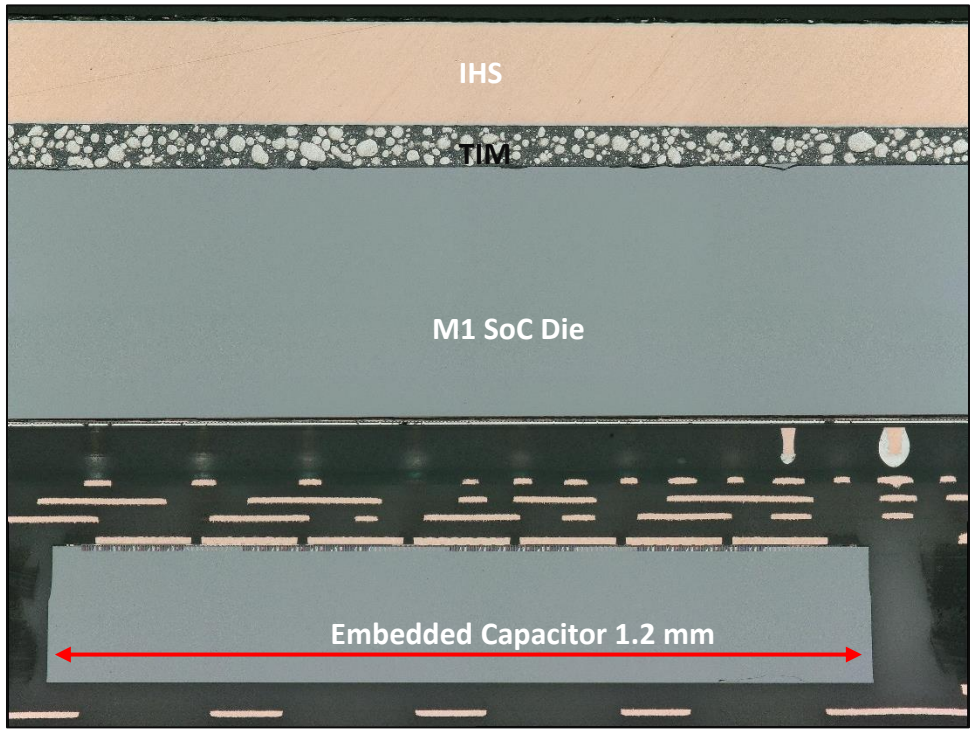
- The embedded capacitor is directly connected to the PCB using a large copper pillar.



M1 SoC Package Cross Section 1

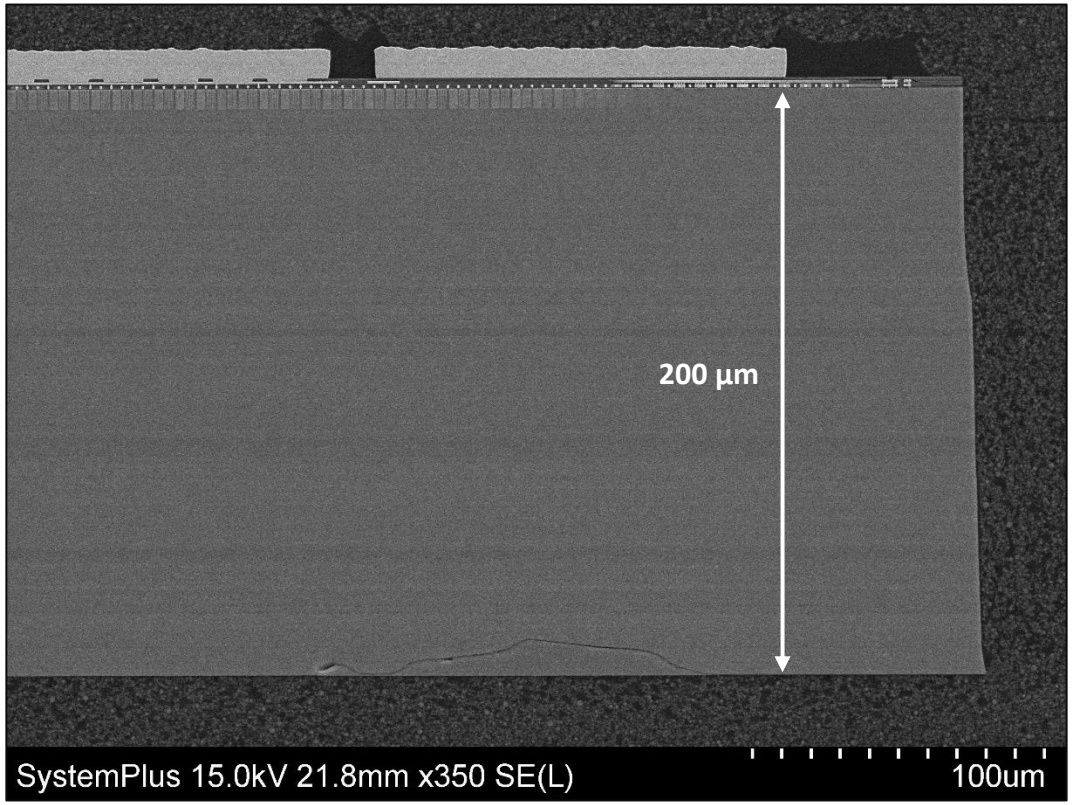


M1 SoC Package Cross Section 1



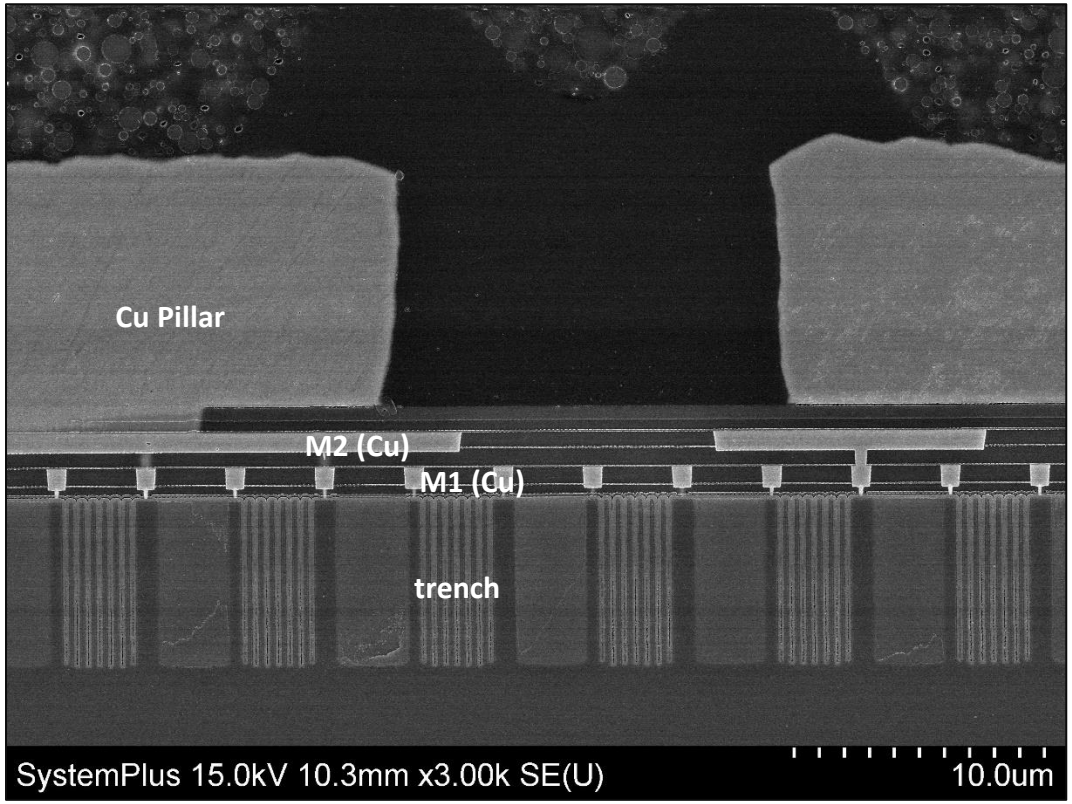
M1 SoC Package Cross Section 1

M1 Package Cross-Section 1



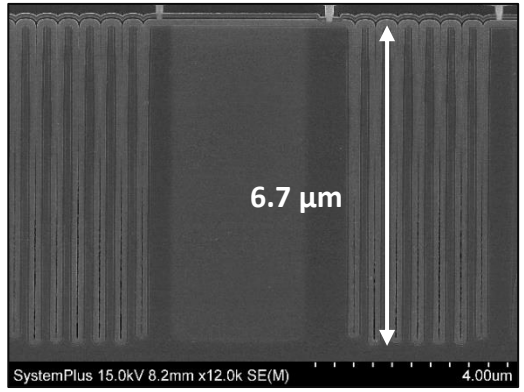
M1 SoC Package Cross Section 1

- Die thickness : 200 µm
- The die process uses 2 Copper metal layers (2 Cu)
- A large copper pillar is used to join the capacitor to the package PCB.

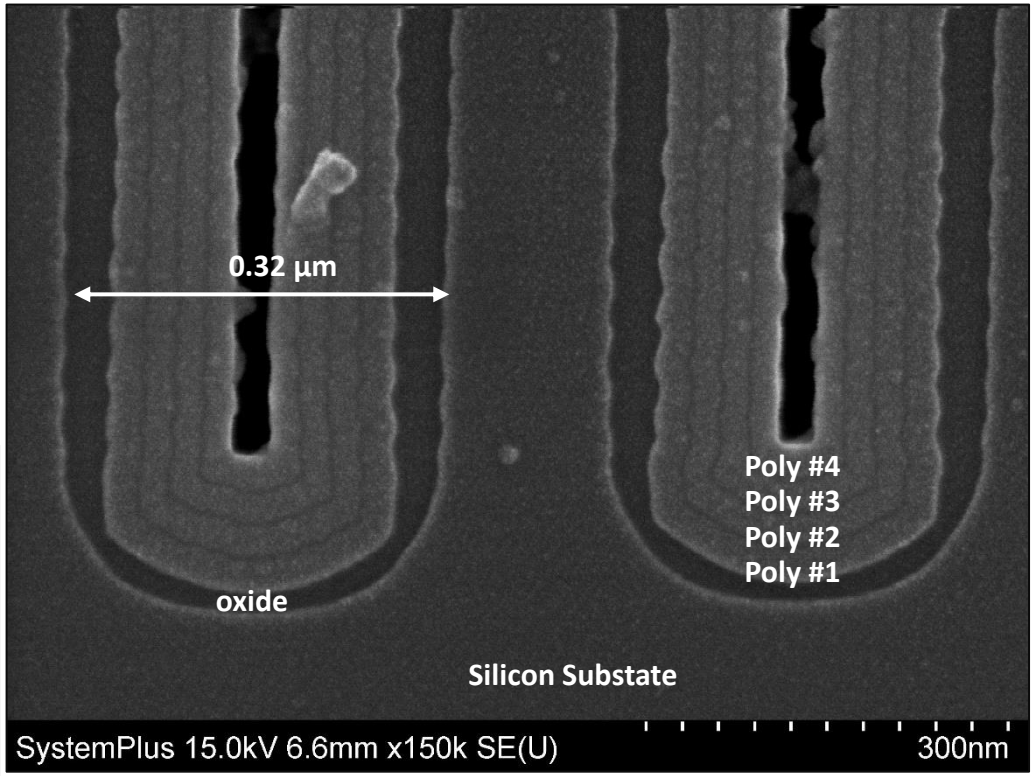


M1 SoC Package Cross Section 1

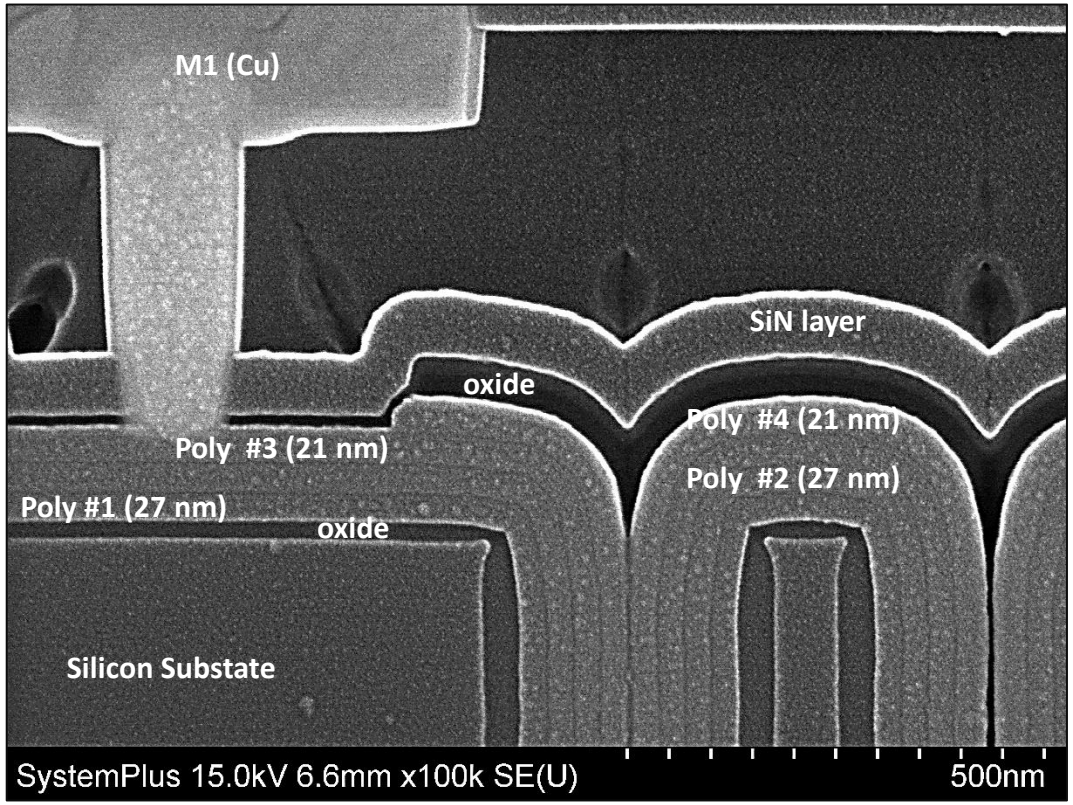
M1 Package Cross-Section 1



M1 SoC Package Cross Section 1



M1 SoC Package Cross Section 1

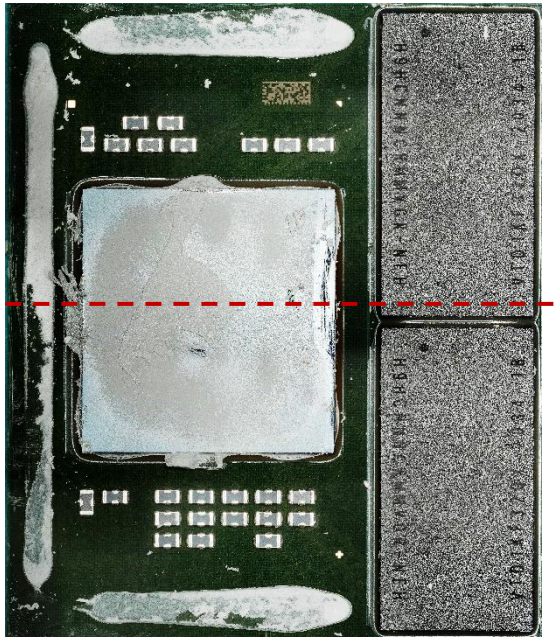


M1 SoC Package Cross Section 1

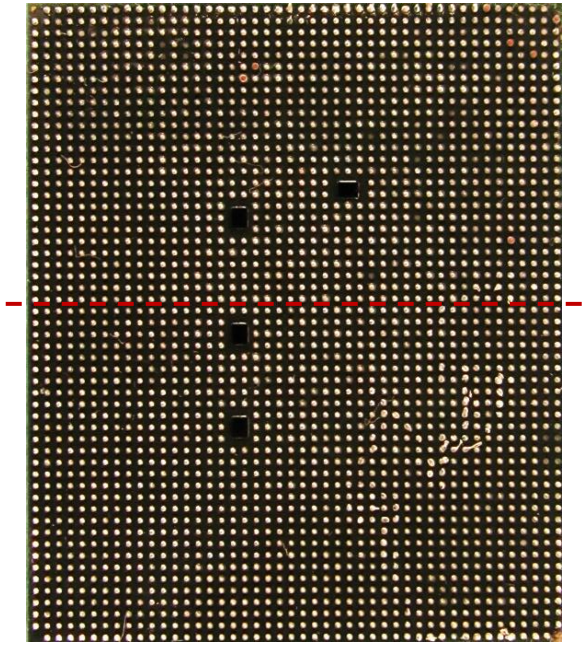
- Trench Depth: 6.7 µm

- 4 layers of polysilicon material are deposited into the trench.
- A dielectric material is deposited between two polysilicon material.
- The trench is then filled with an oxide material.

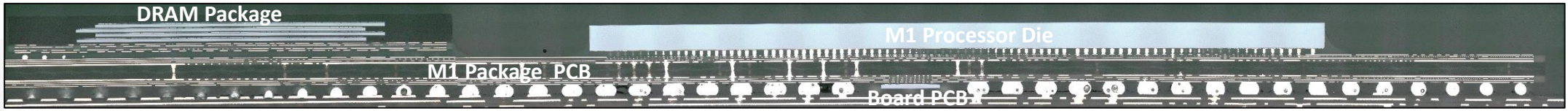
M1 Package Cross-Section 2



M1 SoC Package (Frontside) Cross Sectioning

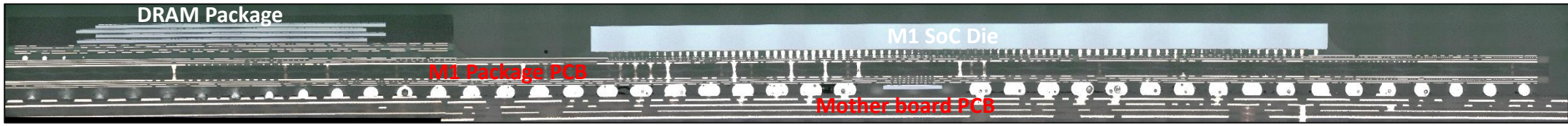


M1 SoC Package (Backside) Cross Sectioning

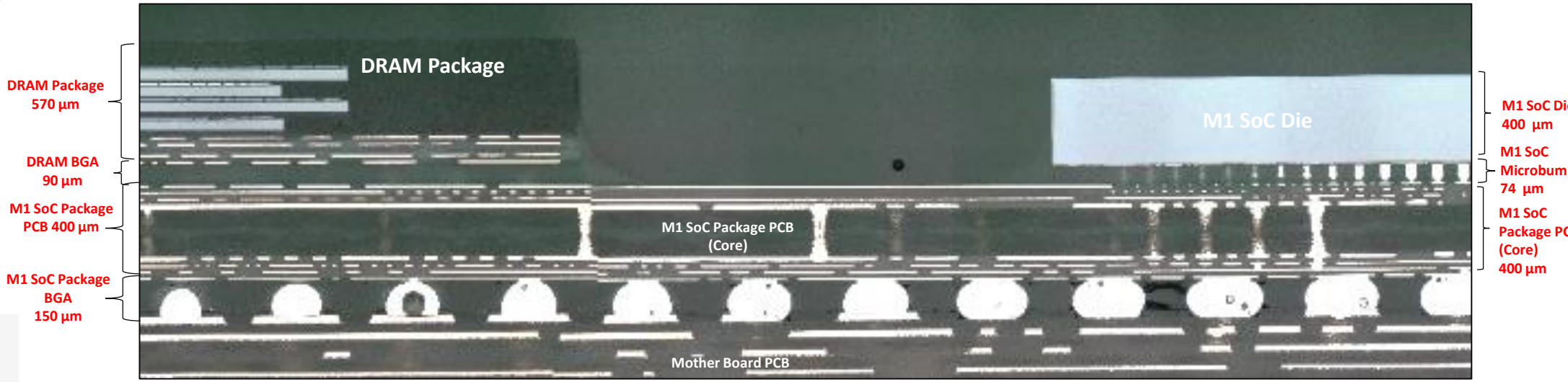


M1 SoC Package Cross Section

M1 Package Cross-Section 2

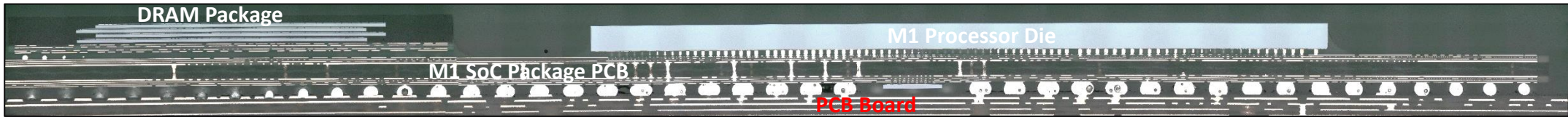


M1 SoC Package Cross Section

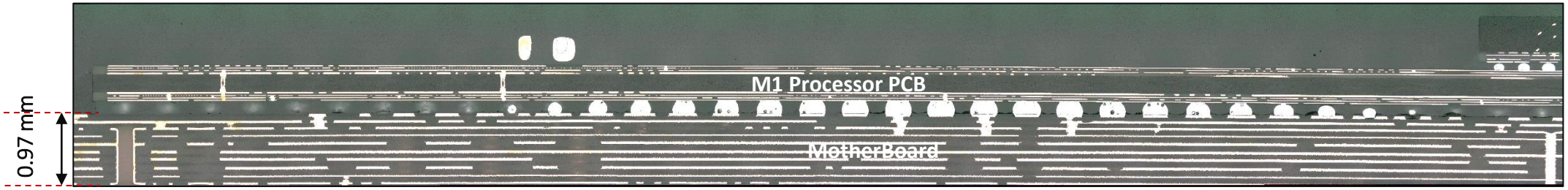


M1 SoC Package Cross Section

M1 Package Cross-Section 2- MotherBoard



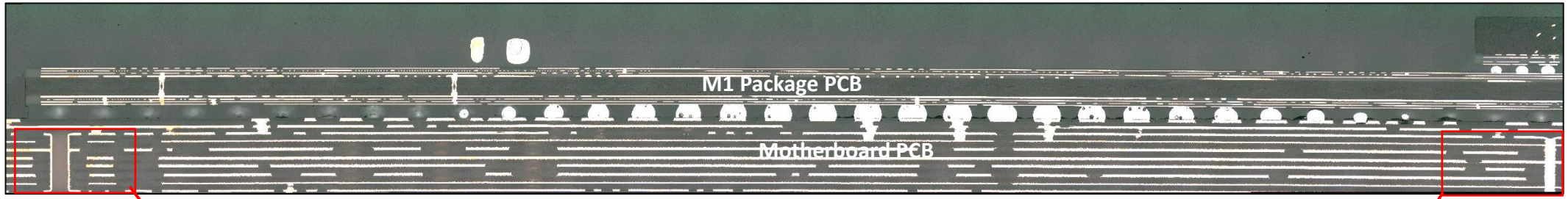
M1 SoC Package Cross Section



M1 SoC Package Cross Section

- The M1 SoC Package is placed on a 12-layer PCB (Motherboard)substrate.
- Motherboard PCB Thickness: 0.97 mm

M1 Package Cross-Section 2- MotherBoard

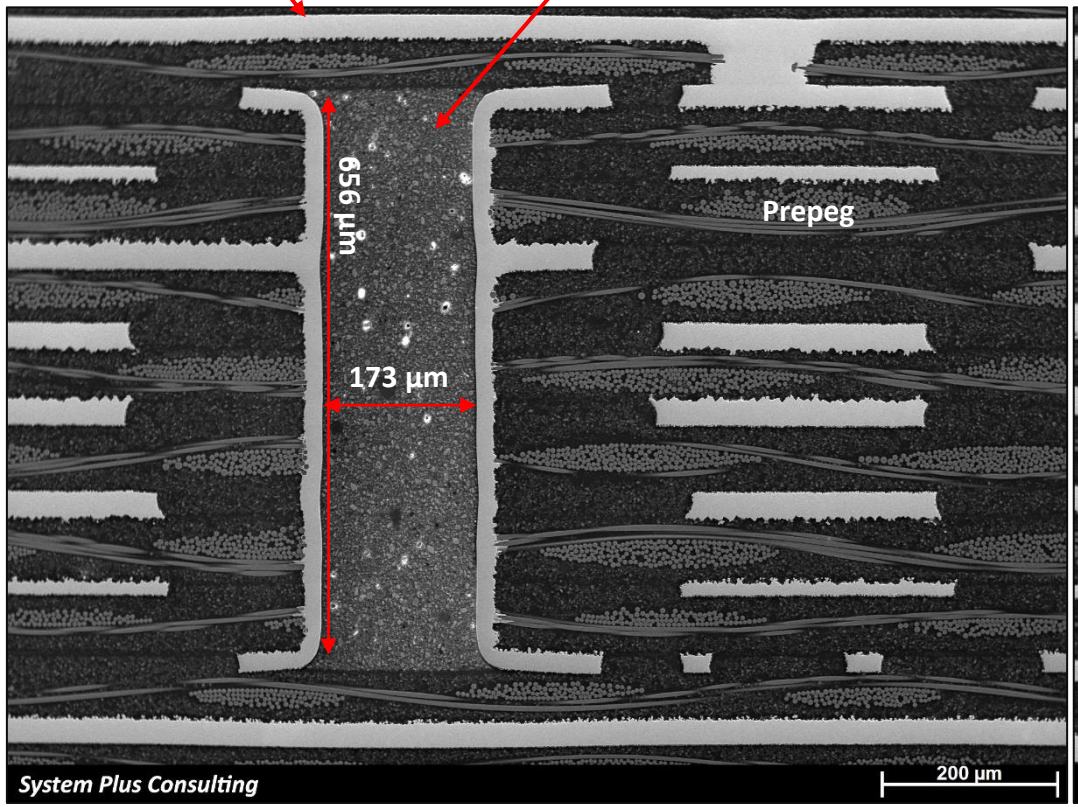


M1 SoC Package Cross Section

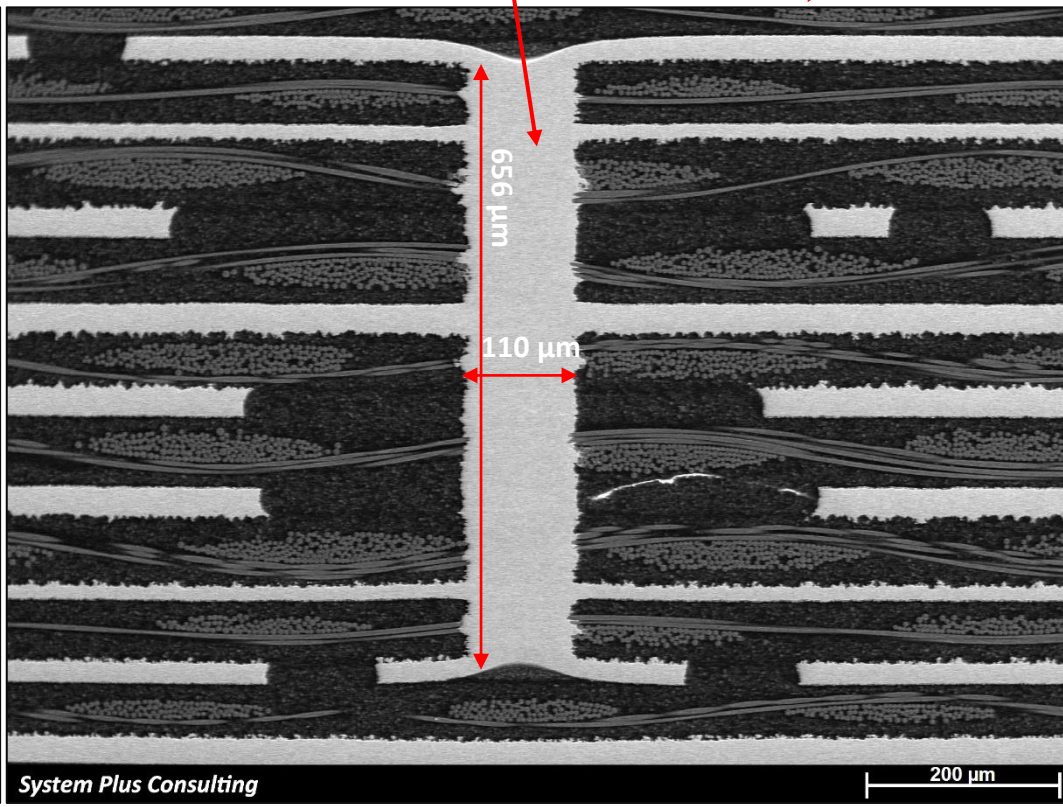
Hidden filled via hole

Buried/hidden via hole

HAR:

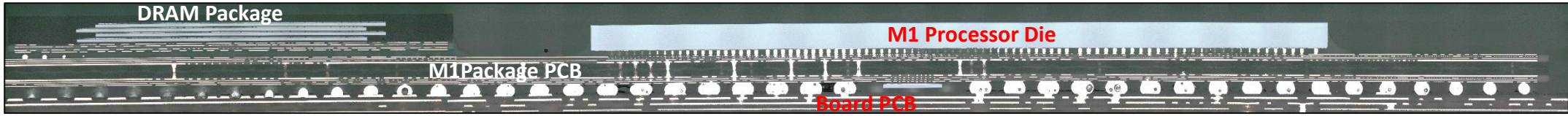


MotherBoard PCB- Cross Section middle of PTH

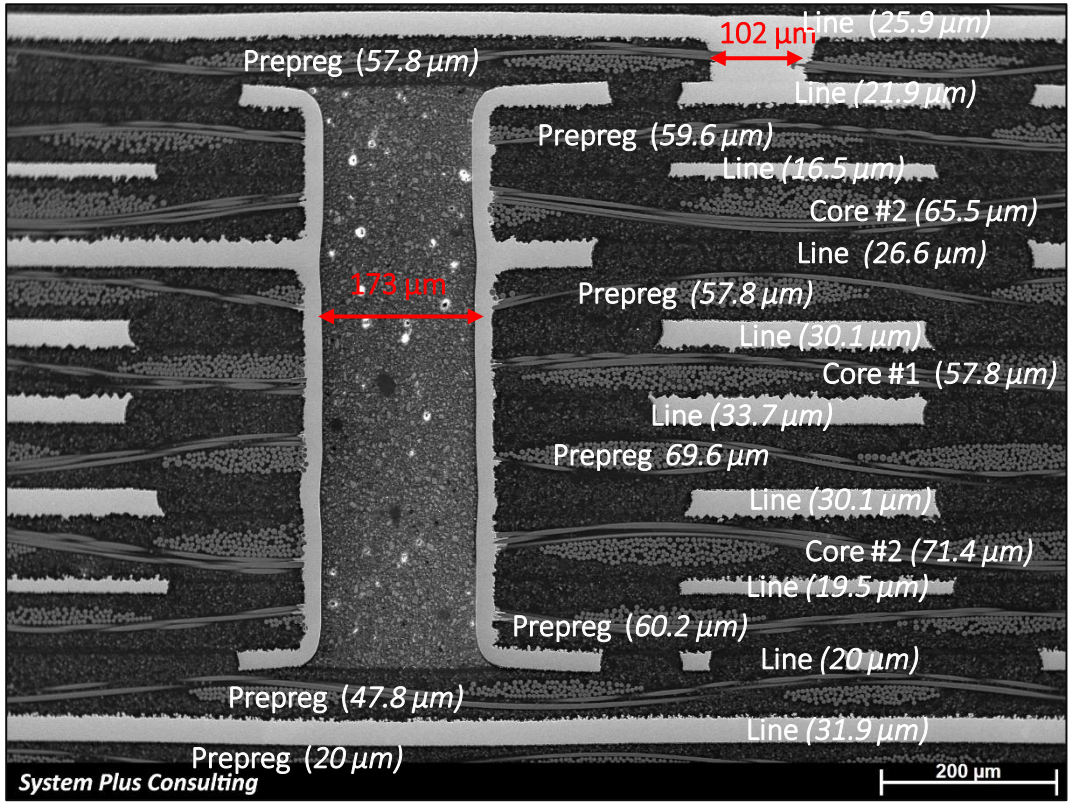


MotherBoard PCB- Cross Section border of PTH

M1 Package Cross-Section 2- MotherBoard

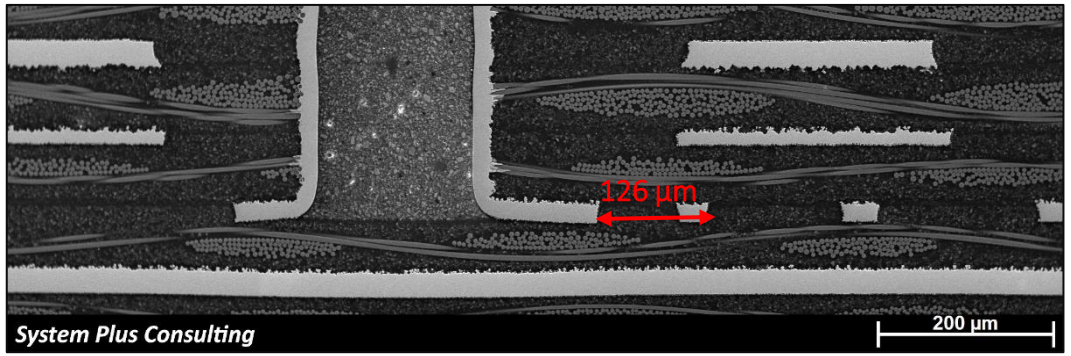


M1 SoC Package Cross Section



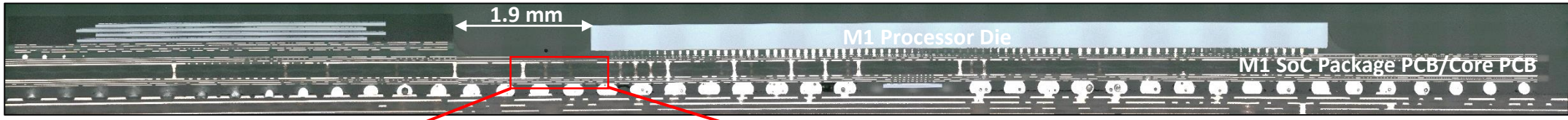
Motherboard PCB Cross Section

- Measured Line/Space Pitch : 126 µm
- Smallest Line 28 µm

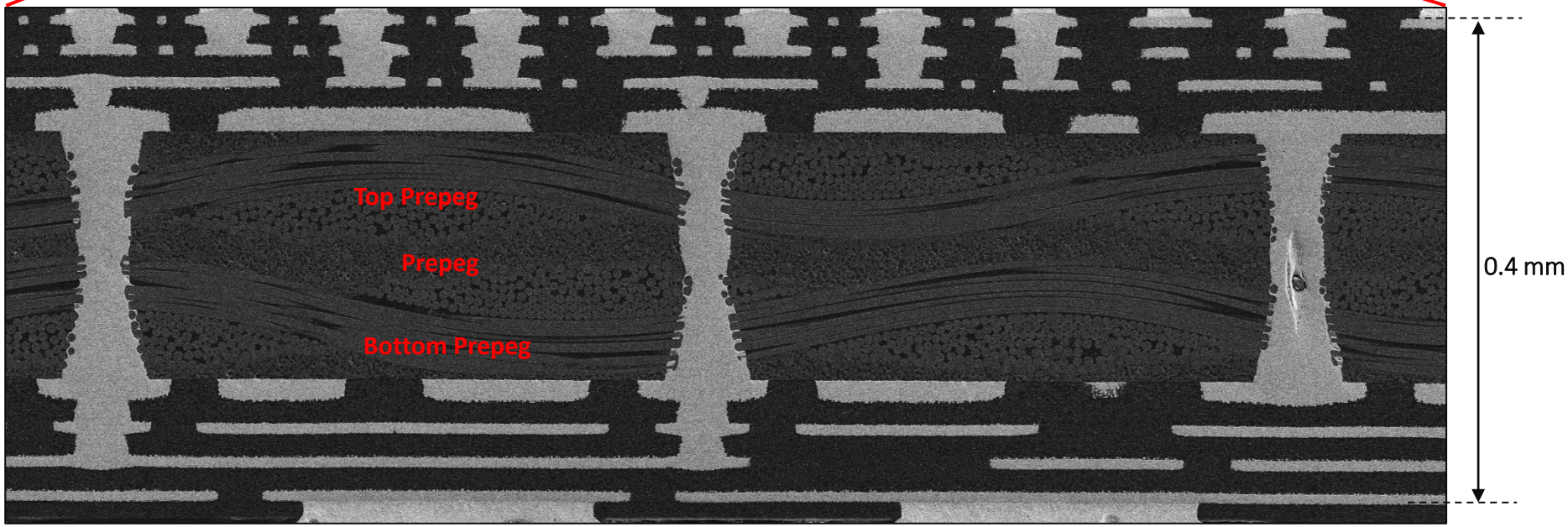


Motherboard PCB Cross Section

M1 Package Cross Section 2 – Core PCB



M1 Package Cross Section



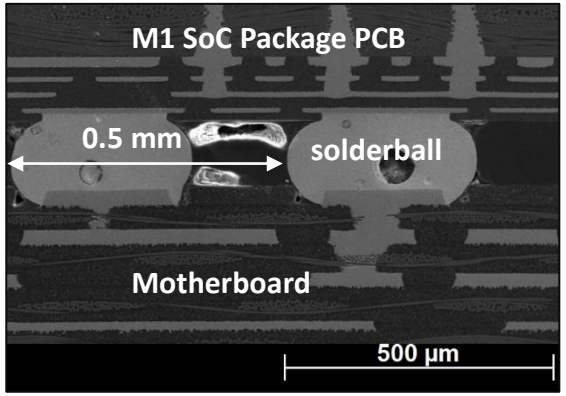
M1 Package PCB Cross Section

- The Apple M1 SoC package includes substrate with 8 Copper layers.
- Substrate thickness: 0.4 mm

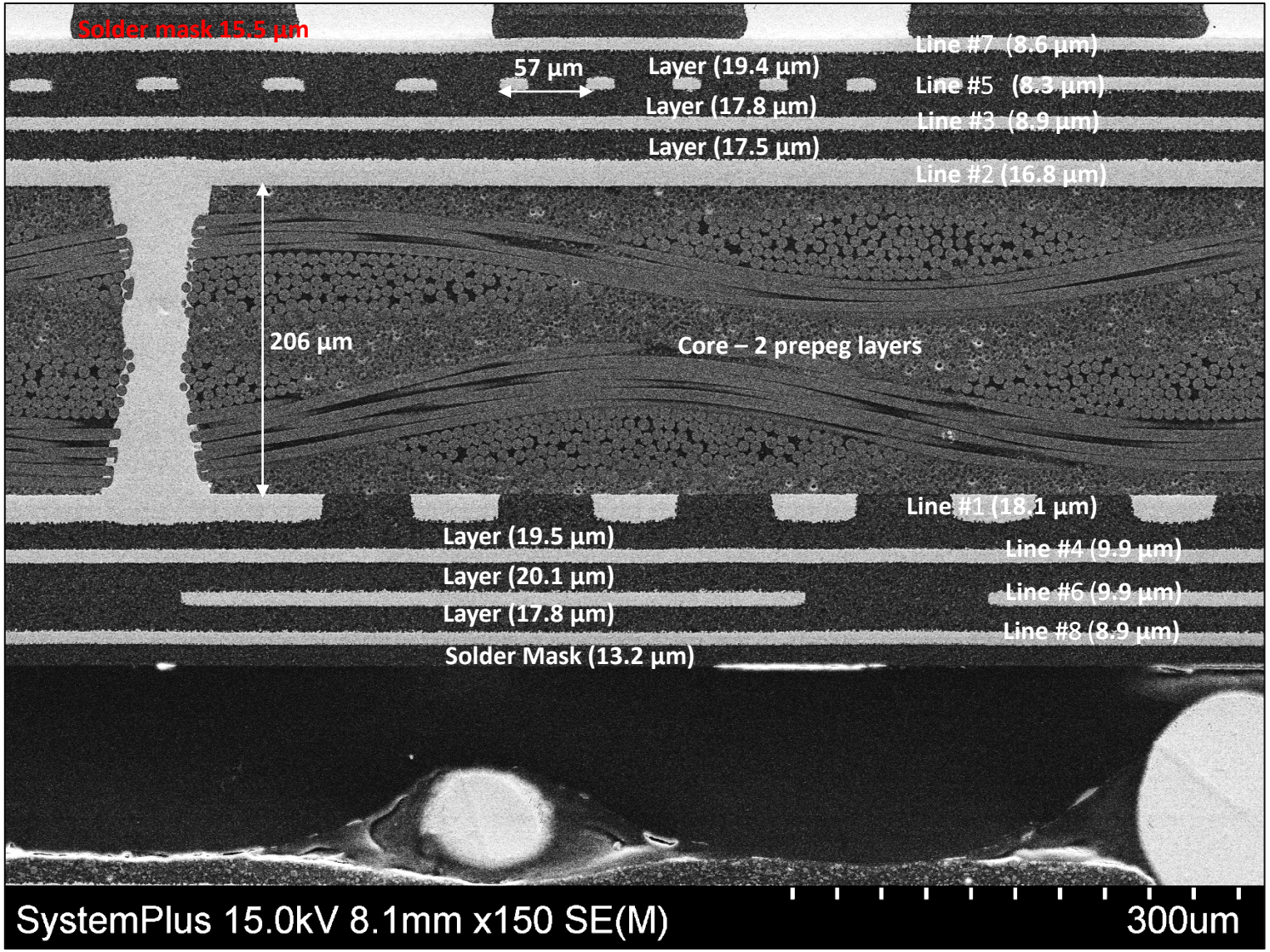
M1 Package Cross Section 2 – M1 Package PCB

- PCB Copper MicroVia Diameter: 40 µm
- Measured Line/Space Pitch : 57 µm
- Smallest Line 18 µm

The PCB Package is joined to the mother board using solder balls.

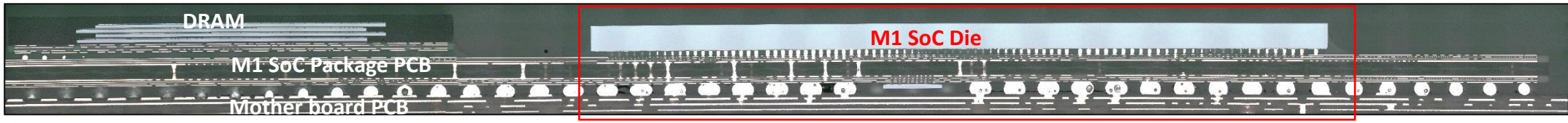


M1 SoC Package Cross Section- PCB



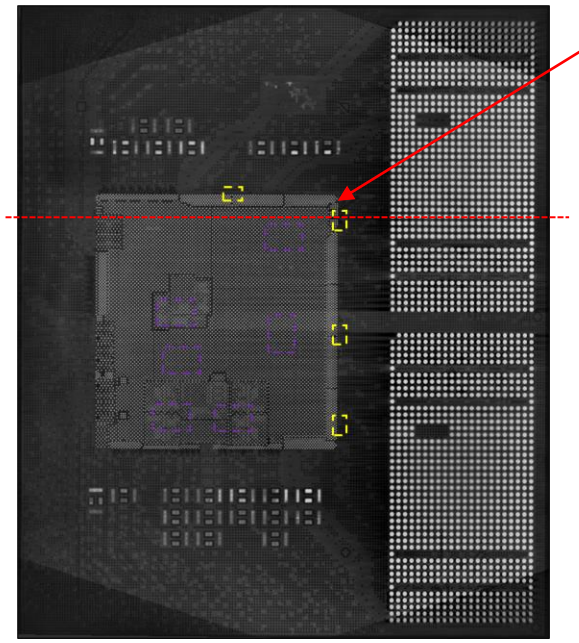
M1 SoC Package Cross Section- PCB

M1 Package Cross Section 2- M1 Package PCB

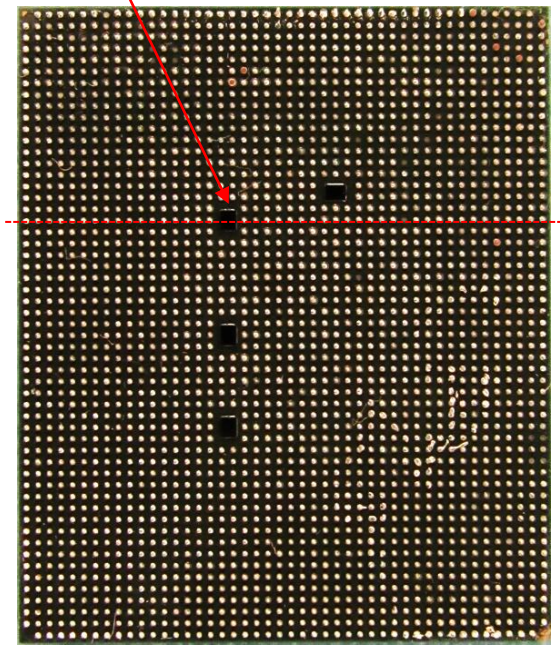


M1 SoC Package Cross Section

M1 SoC Package Cross Section



FLI & DRAM Interconnect Map – X-Ray View

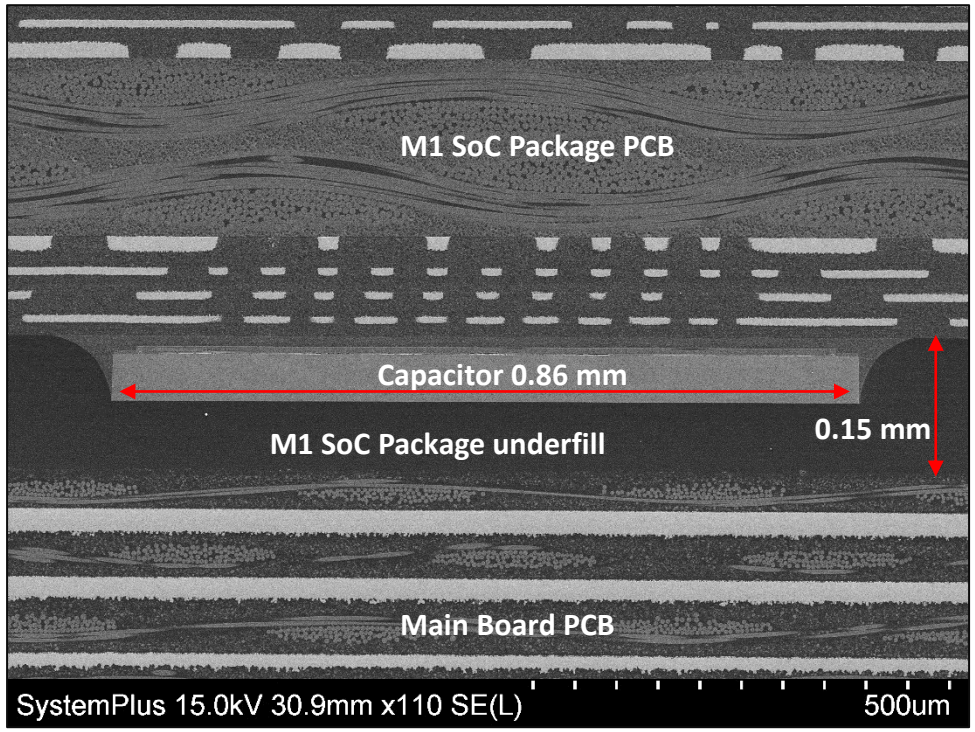


M1 SoC Package Backside

- Four Capacitors are integrated on the backside of the M1 SoC Package PCB.

M1 Package Cross Section 2- Package PCB

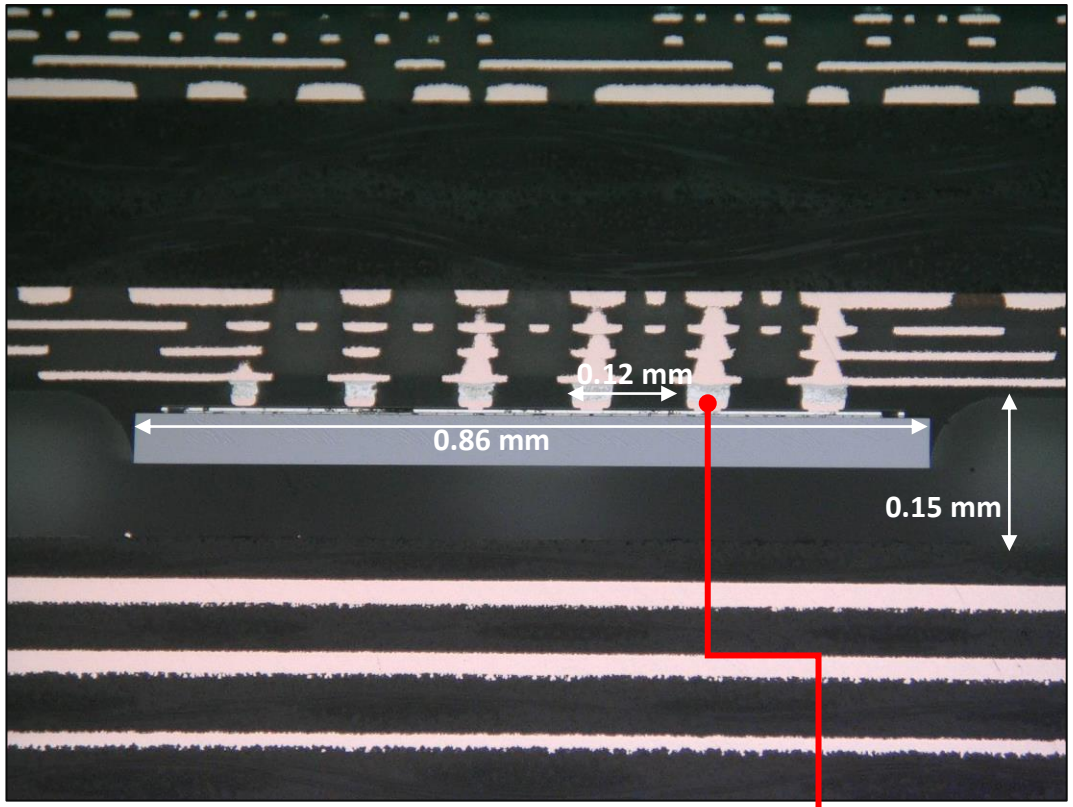
- The capacitors are joined to the M1 SoC Package PCB using microbumps.
- The capacitor is placed in flip chip position and joined to the PCB by a reflow process.



M1 SoC Package Cross Section- Capacitor

M1 SoC Package Cross Section- Capacitor

M1 Package Cross Section 2- Package PCB

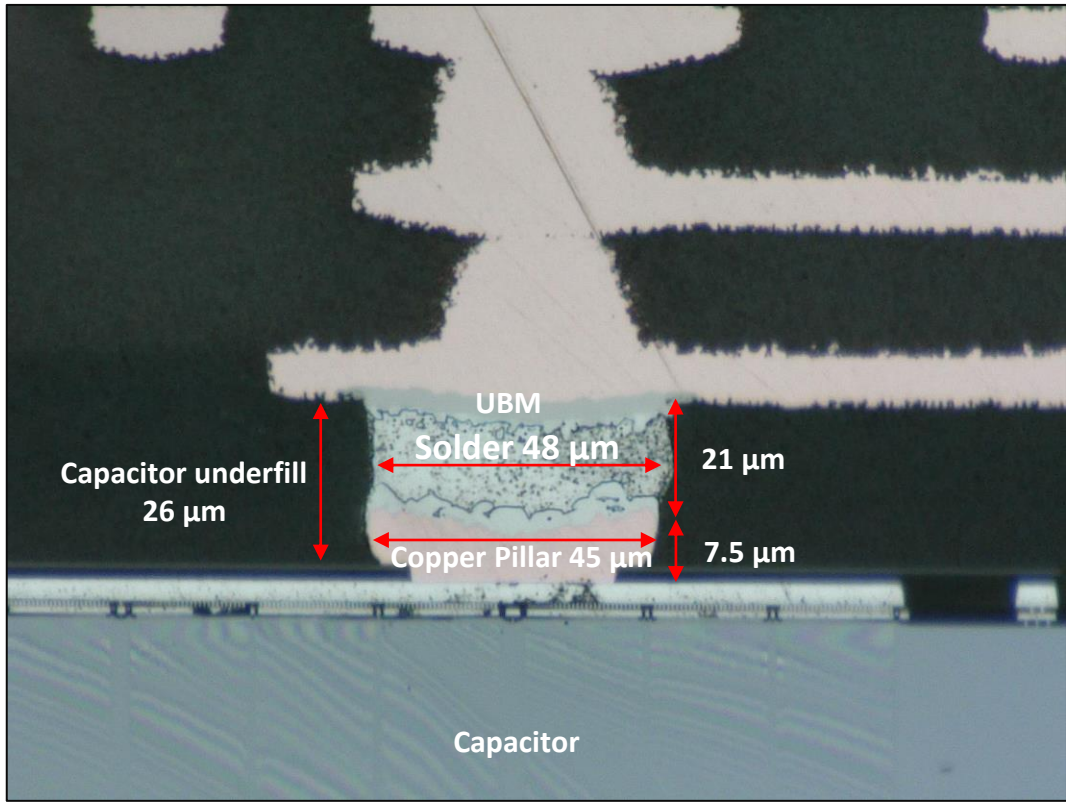


M1 SoC Package Cross Section- Capacitor

- *Capacitor microbump Pitch:123 µm*
- *Microbump Diameter: 48 µm*

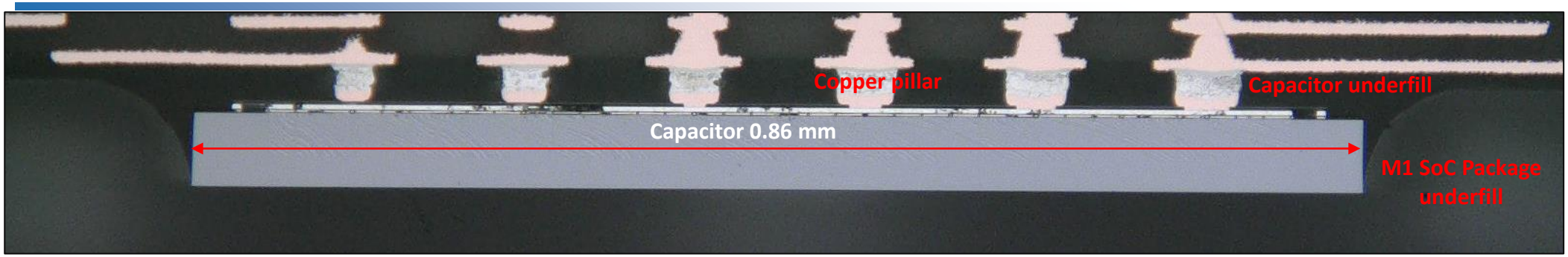
- The copper pillar is in direct contact with the capacitor top metal layer.

- Microbumps Pitch: 120 µm
- Copper pillar diameter: 45 µm
- Solder Ball diameter: 48 µm
- Capacitor Underfill thickness: 26 µm

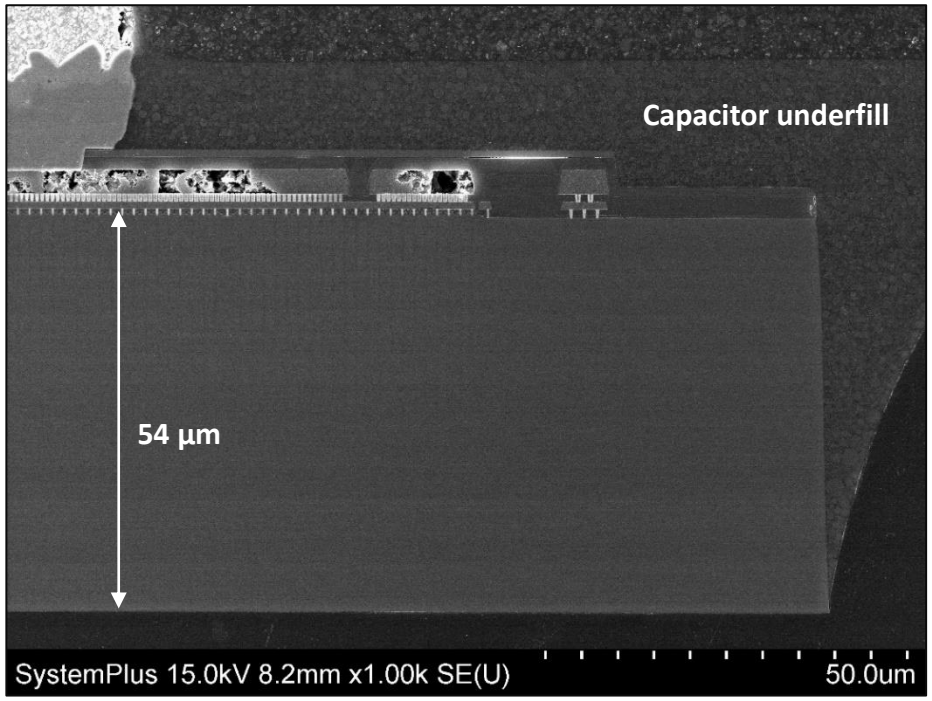


M1 SoC Package Cross Section- Capacitor

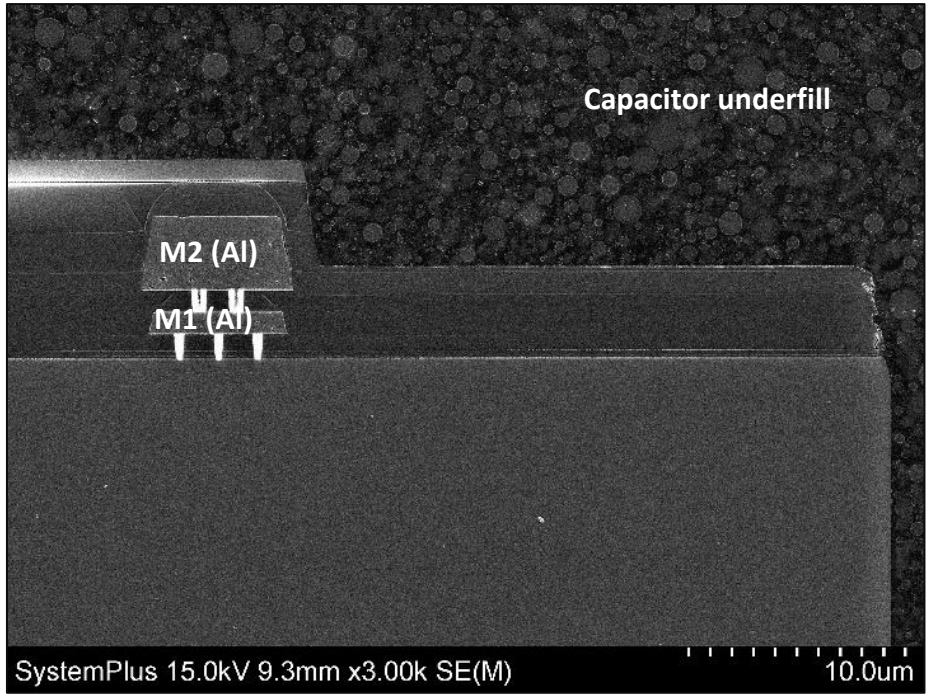
M1 Package Cross Section 2- Package PCB



M1 SoC Package Cross Section- Capacitor



M1 SoC Package Cross Section- Capacitor

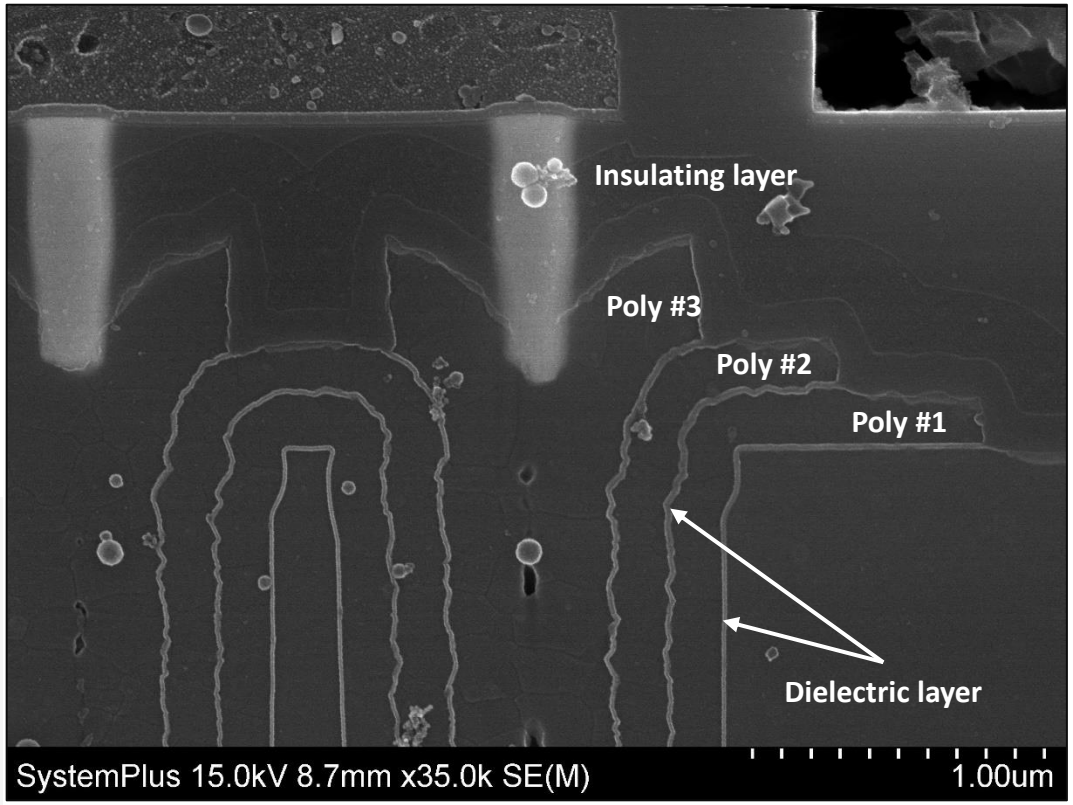


M1 SoC Package Cross Section- Capacitor

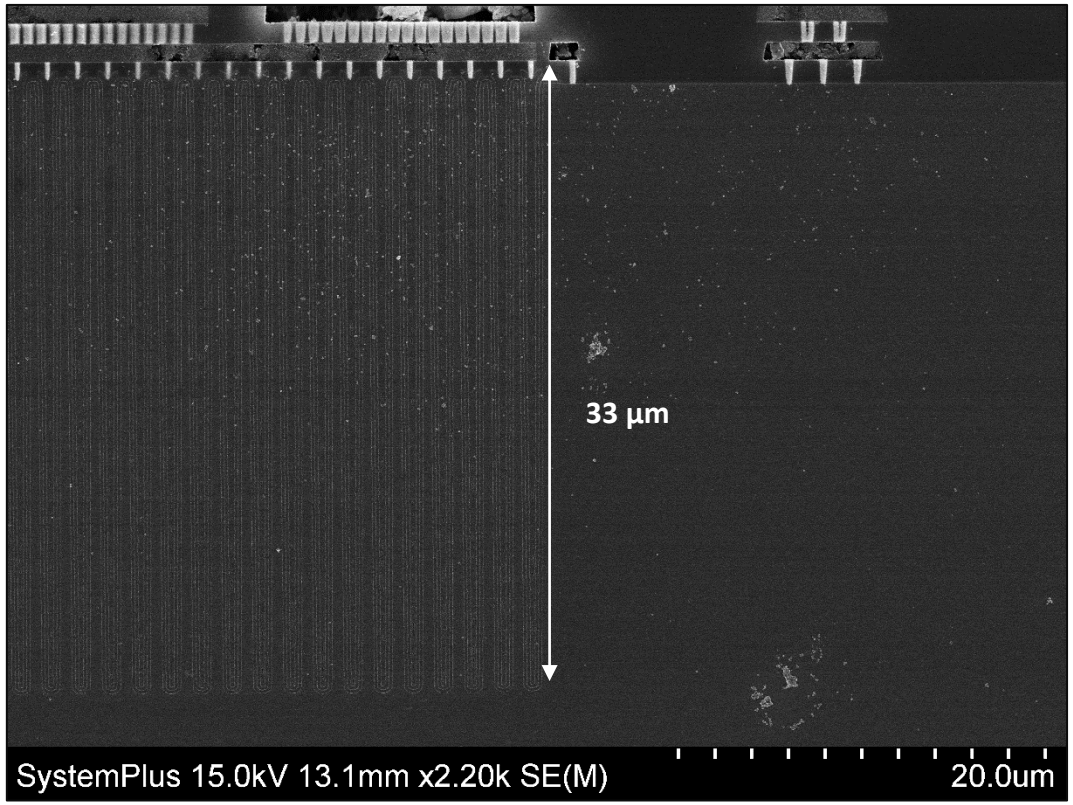
- The capacitors are placed on the M1 SoC Package PCB face down, the capacitors are connected to the PCB using micro bumps.
- Capacitor thickness: 54 µm
- The capacitor Die process uses 2 Aluminium metal layers.

M1 Package Cross Section 2- Package PCB

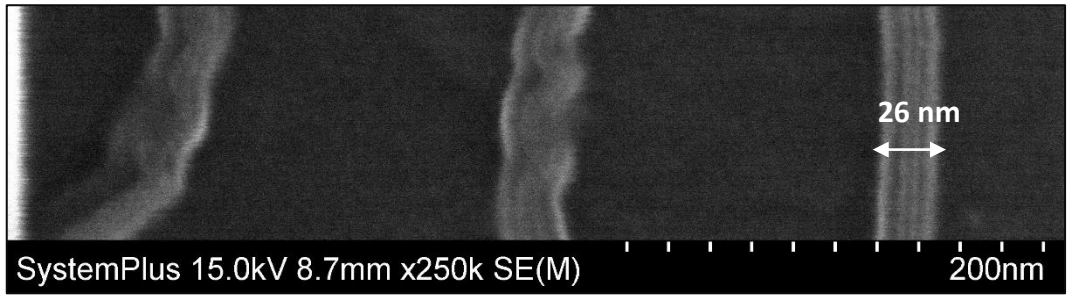
- Trench thickness: 33 µm
- Si is etched to form a deep trench. Polysilicon is deposited and a dielectric layer is deposited between two polysilicon materials.
- Dielectric layer : 26 nm
- The capacitor process uses 3 polysilicon layers.



M1 SoC Package Cross Section- Capacitor

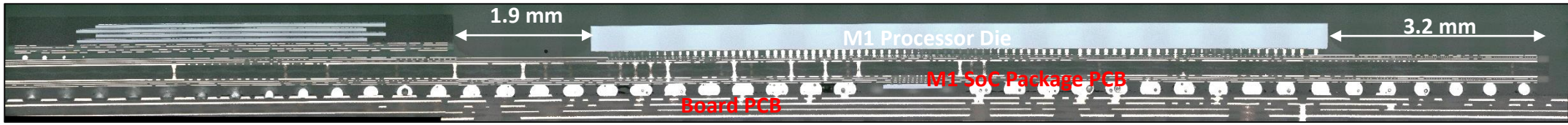


M1 SoC Package Cross Section- Capacitor

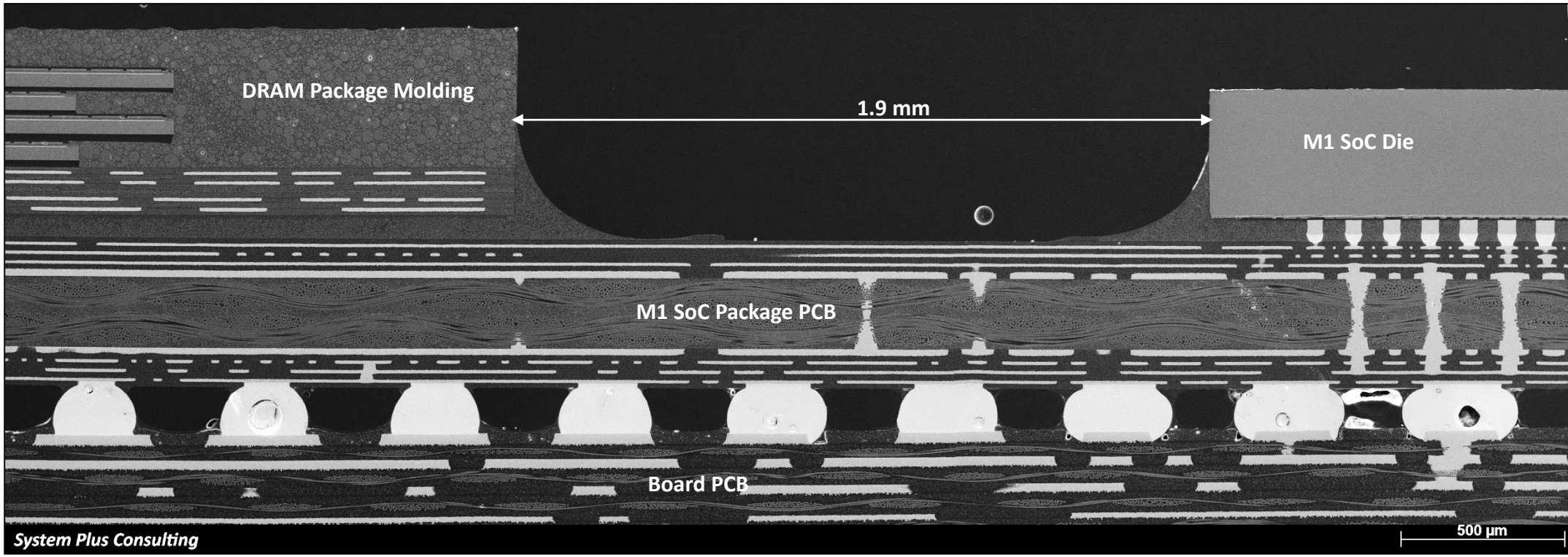


M1 SoC Package Cross Section- Capacitor

M1 Package Cross Section 2



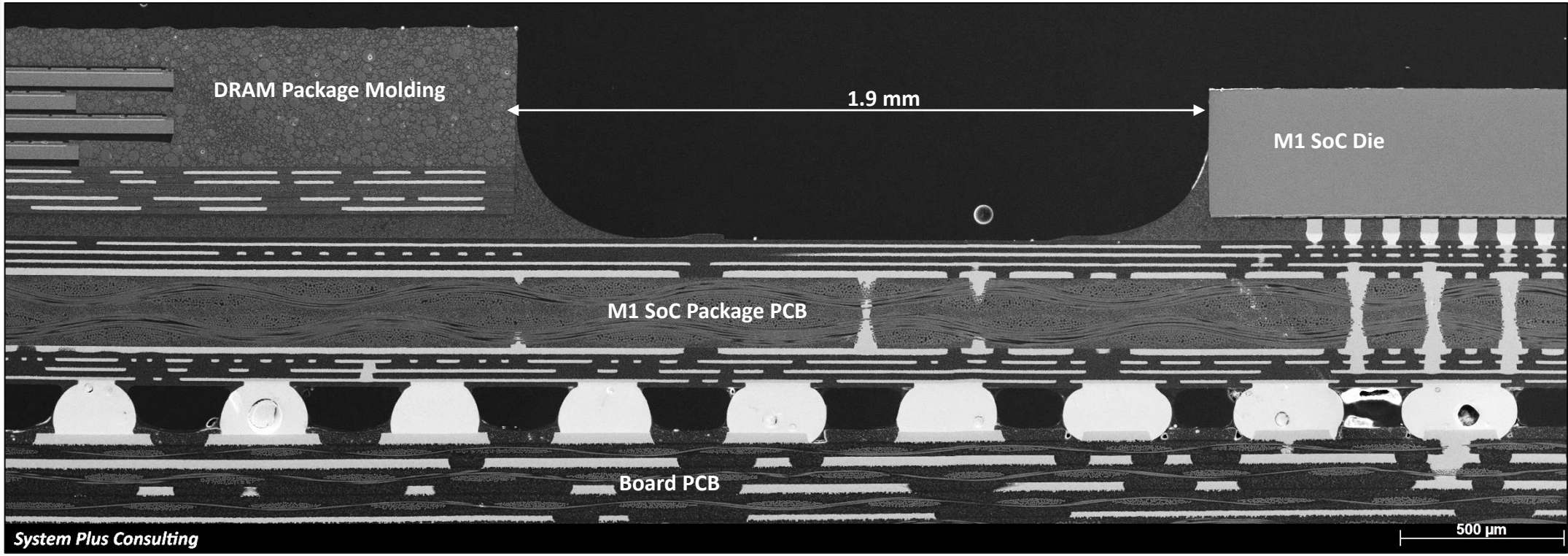
M1 SoC Package Cross Section



M1 SoC Package Cross Section

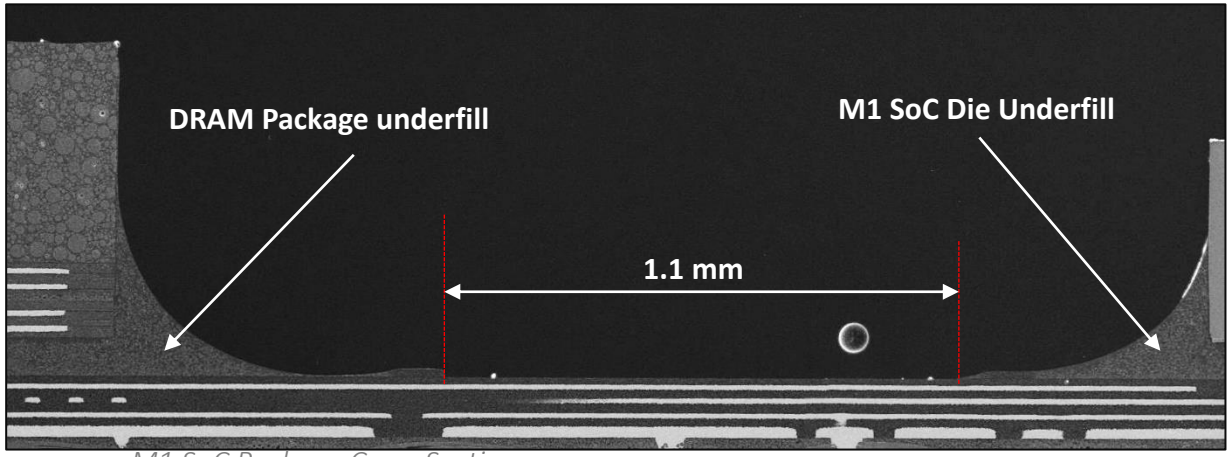
- Distance between DRAM Package and M1 Die : 1.9 mm
- M1 SoC Die distance to PCB edge: 3.2 mm

M1 Package Cross Section 2



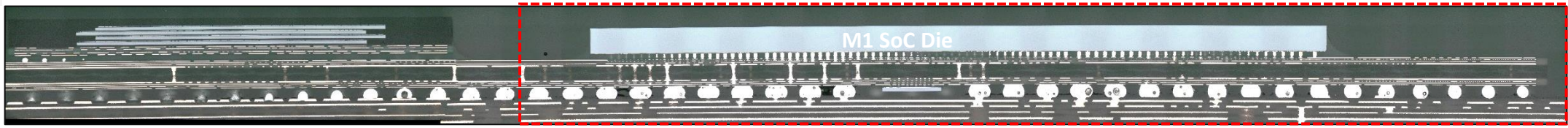
M1 SoC Package Cross Section

- Distance between DRAM Package and M1 Die : 1.9 mm
- Distance between DRAM underfill and M1 SoC Die underfill: 1.1 mm
- The M1 SoC die was attached to the package PCB prior to the DRAM Package. The gap between the M1 SoC and the DRAM is large enough to avoid the overlap of the CUFs.

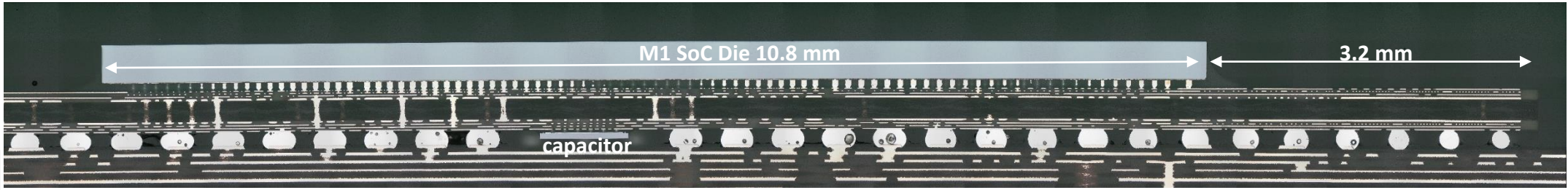


M1 SoC Package Cross Section

M1 Package Cross Section 2



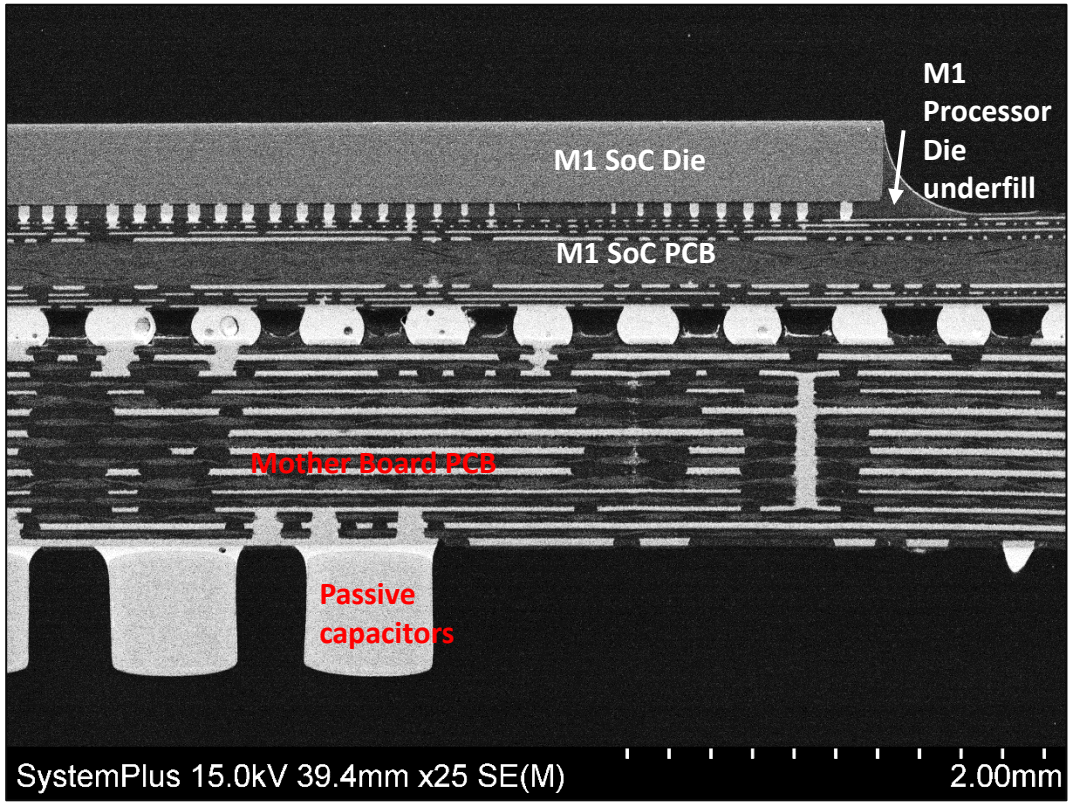
M1 SoC Package Cross Section



M1 SoC Package Cross Section

M1 Package Cross Section 2

M1 SoC Package Cross Section



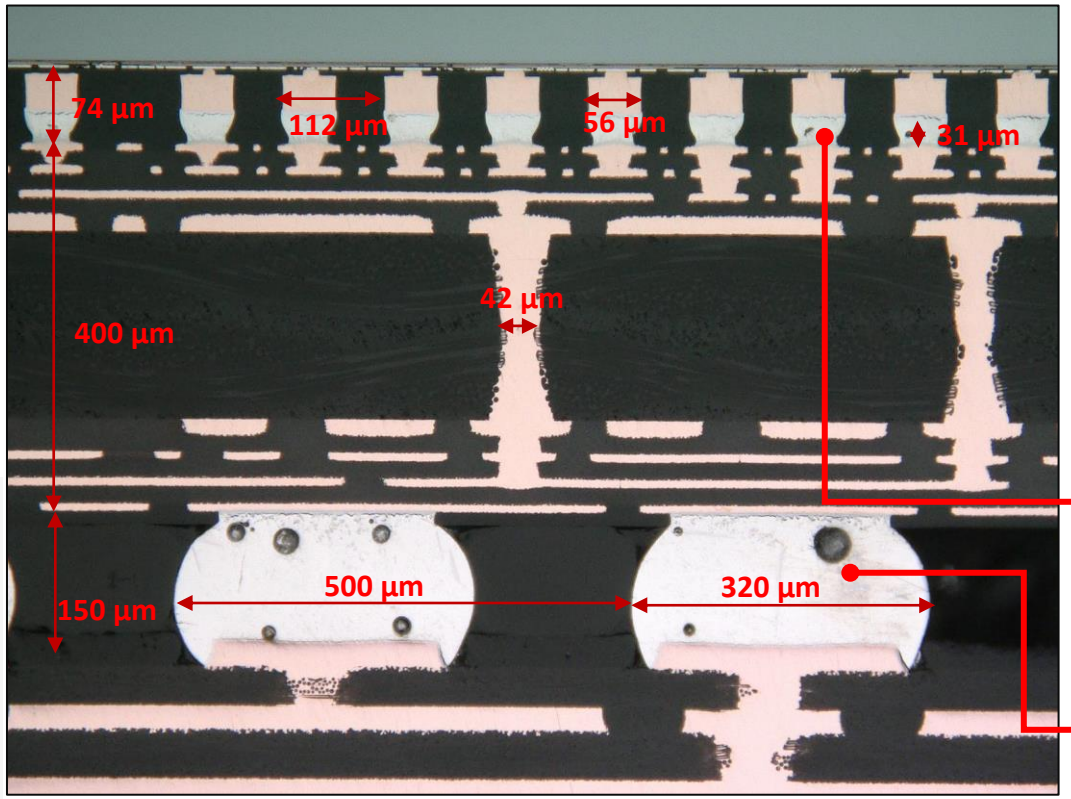
M1 SoC Package Cross Section

- The M1 SoC die is placed in face down on the PCB substrate.

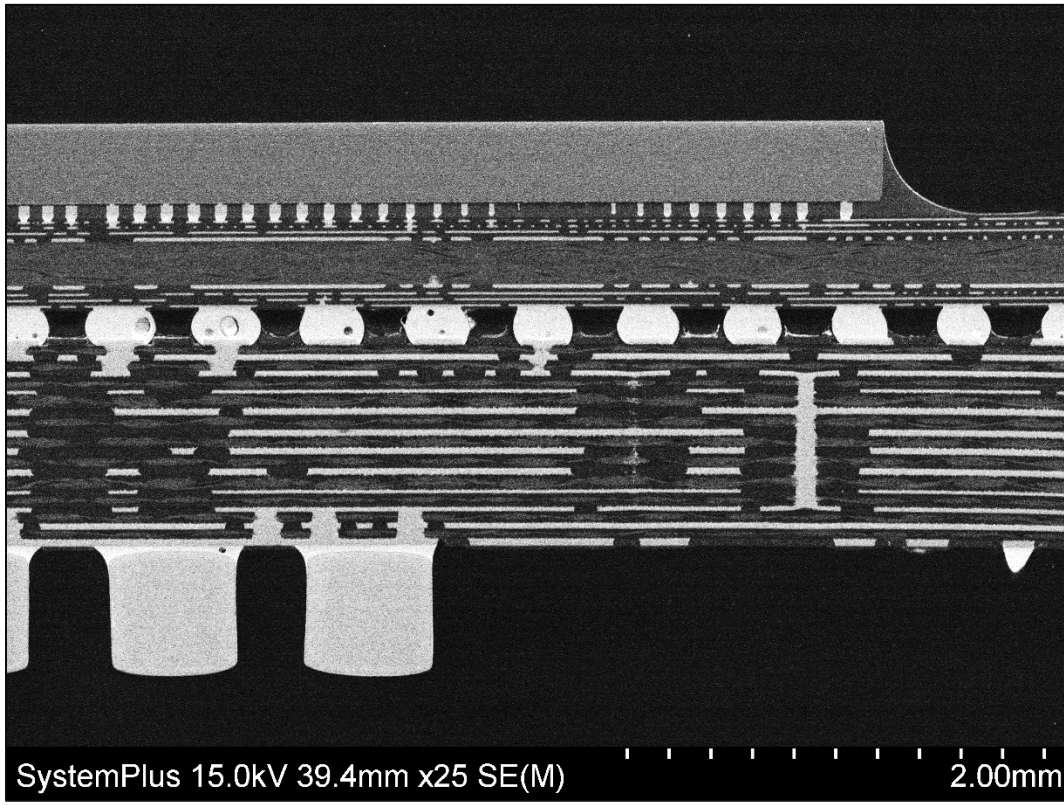
M1 Package Cross Section 2

- The M1 SoC die is placed in flip chip position on to the PCB substrate.
- Microbumps connect the M1 die to the M1 Package PCB.

- M1 die microbump pitch: 112 µm
- M1 Package PCB Ball pitch: 500 µm



M1 SoC Package Cross Section

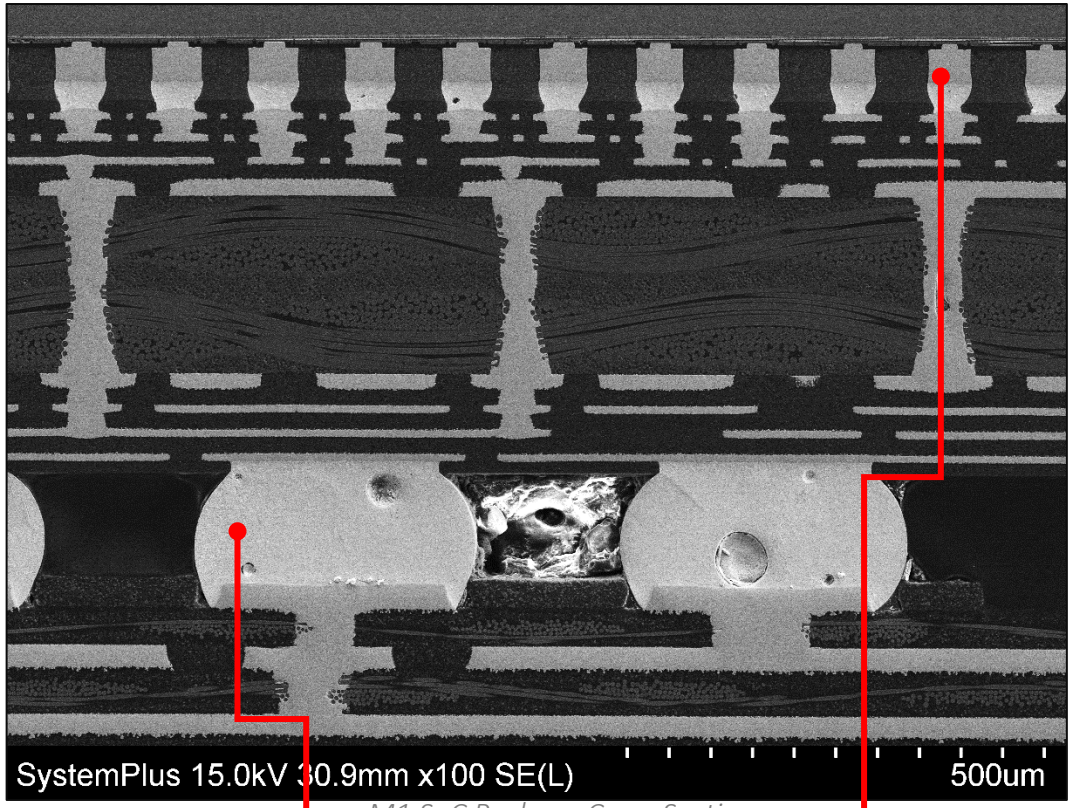


M1 SoC Package Cross Section

- *M1 Die microbump Pitch: 112 µm*
- *Microbump Diameter: 56 µm*

- *M1 Package PCB Ball pitch: 500 µm*
- *Ball Diameter: 320 µm*

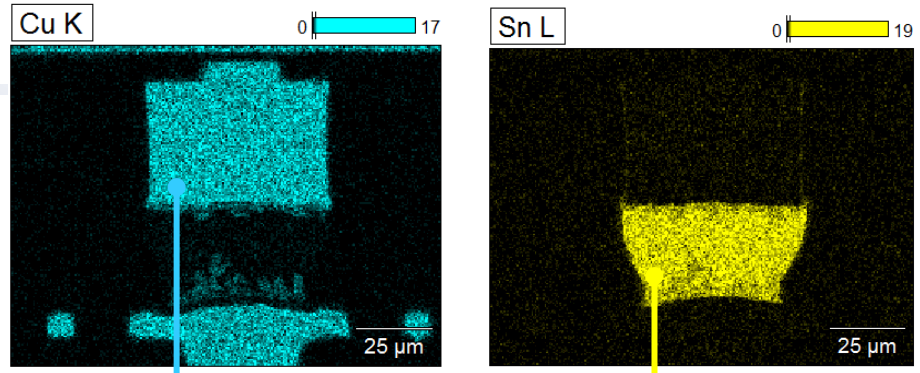
M1 Package Cross Section 2



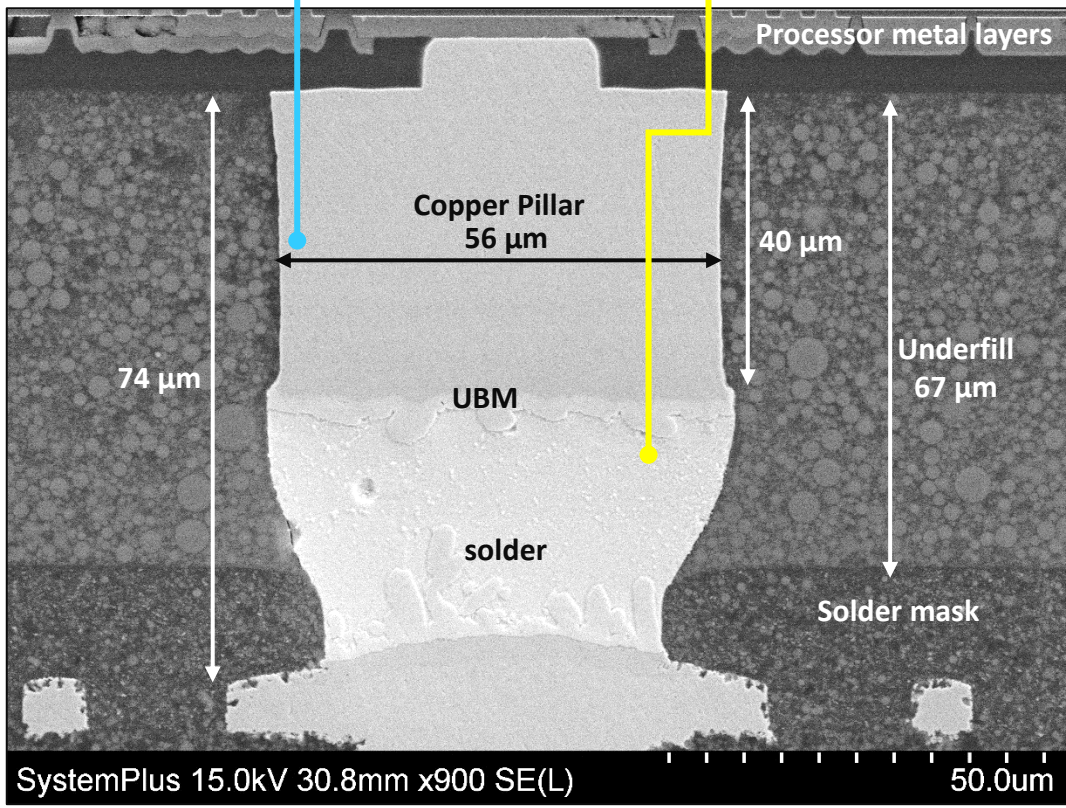
M1 SoC Package Cross Section

- *M1 Package PCB Ball pitch:* *500 µm*
- *Ball Diameter:* *320 µm*
- *M1 Die microbump Pitch:* *112 µm*
- *Microbump Diameter:* *56 µm*

- Copper pillar diameter: 56 µm
- Underfill thickness: 67 µm
- The microbump solder uses a Tin (Sn) compound solder paste.

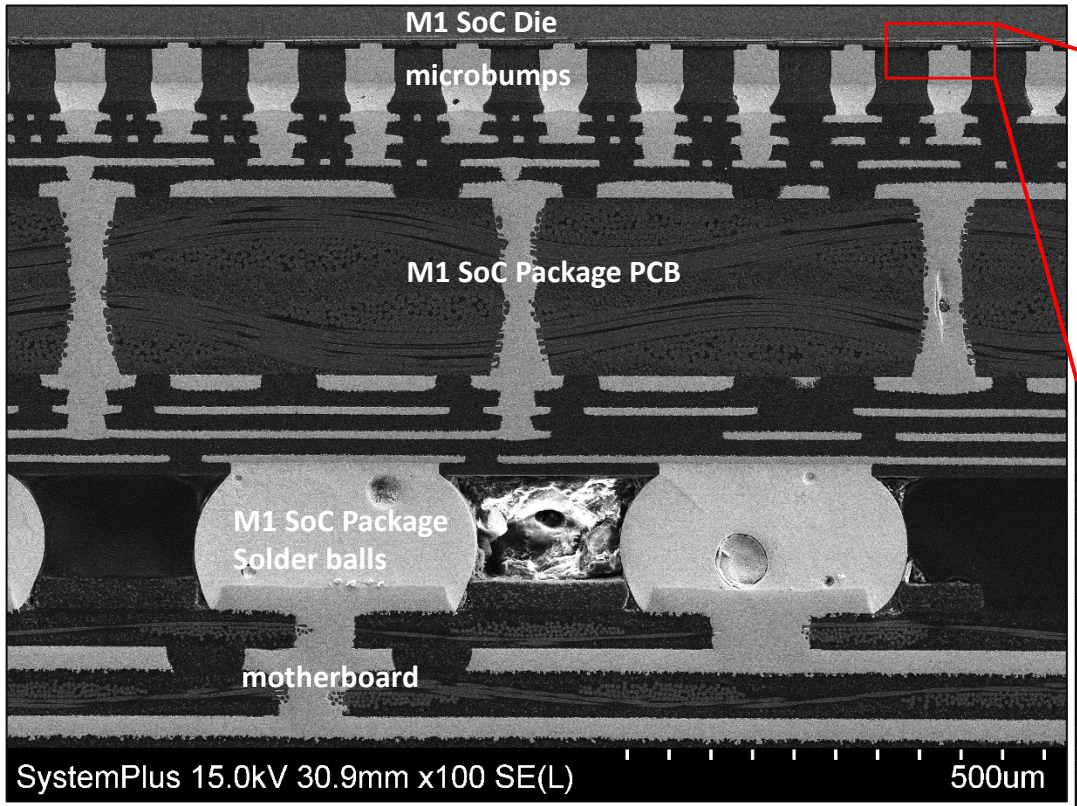


M1 SoC Package EDX Analysis

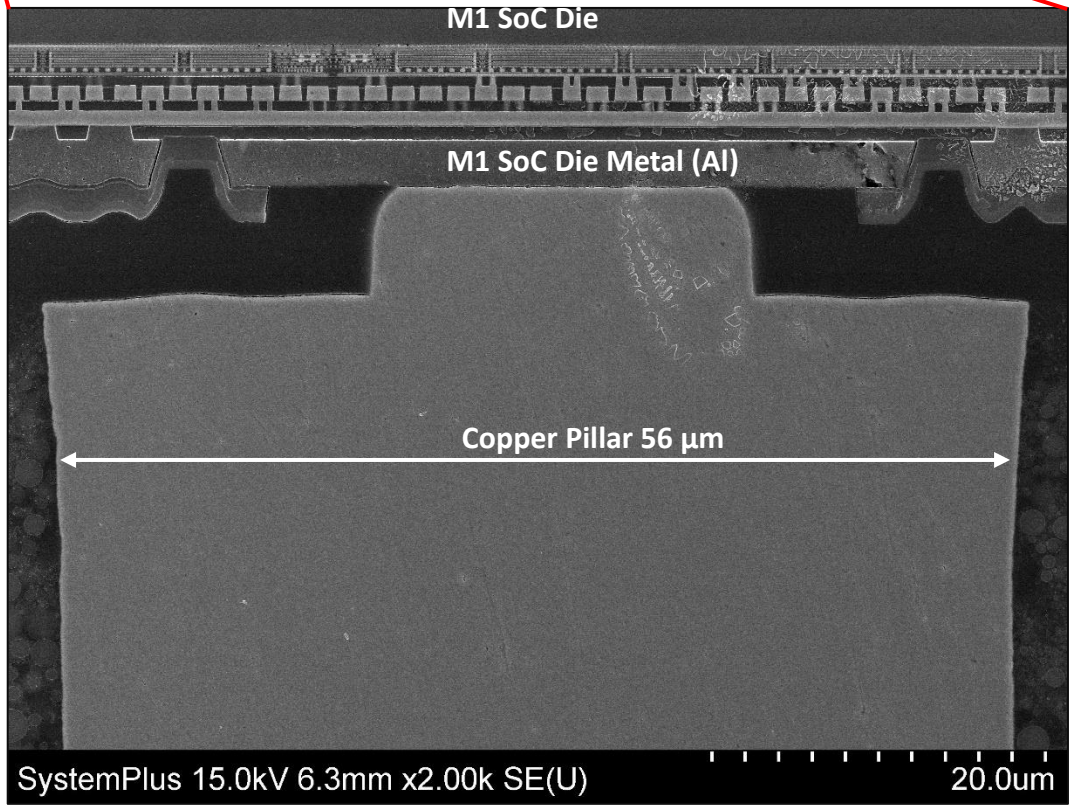


M1 SoC Package Cross Section

M1 Package Cross Section 2



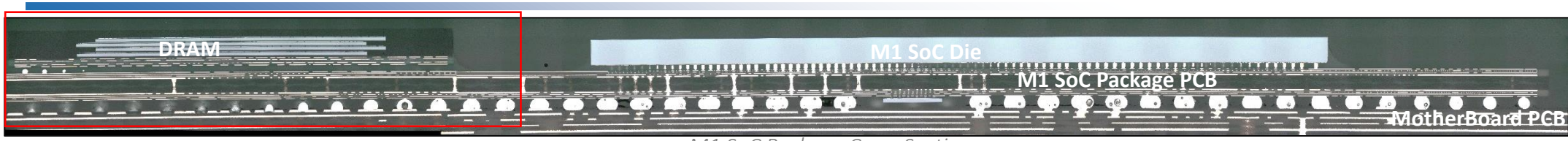
M1 SoC Package Cross Section



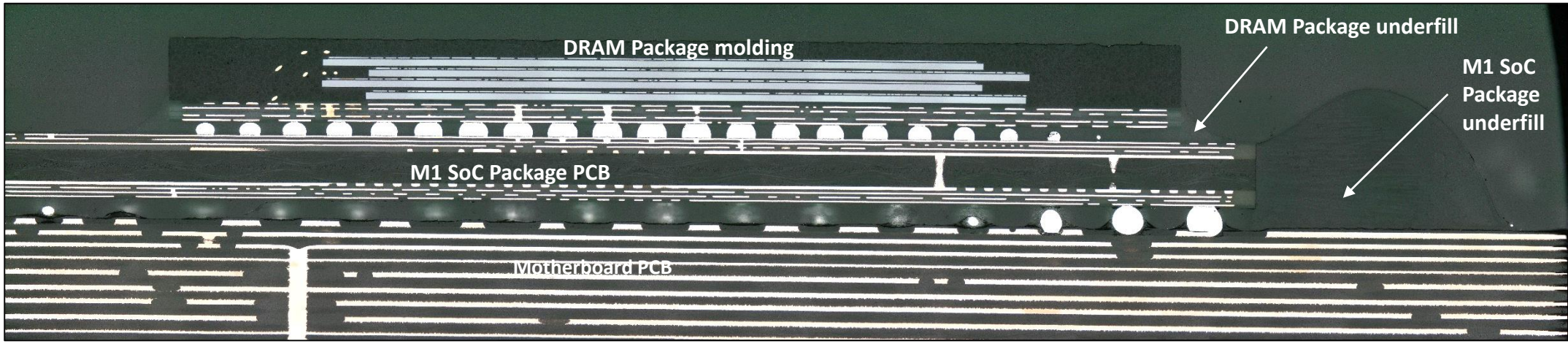
M1 SoC Package Cross Section

- The copper pillar is in direct contact with the M1 SoC Die top metal layer.

M1 Package Cross Section 2



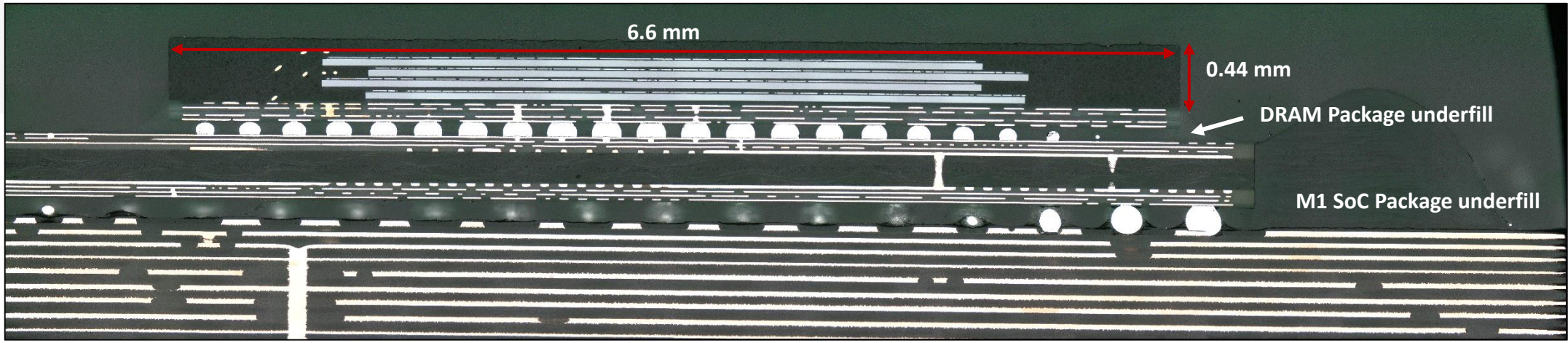
M1 SoC Package Cross Section



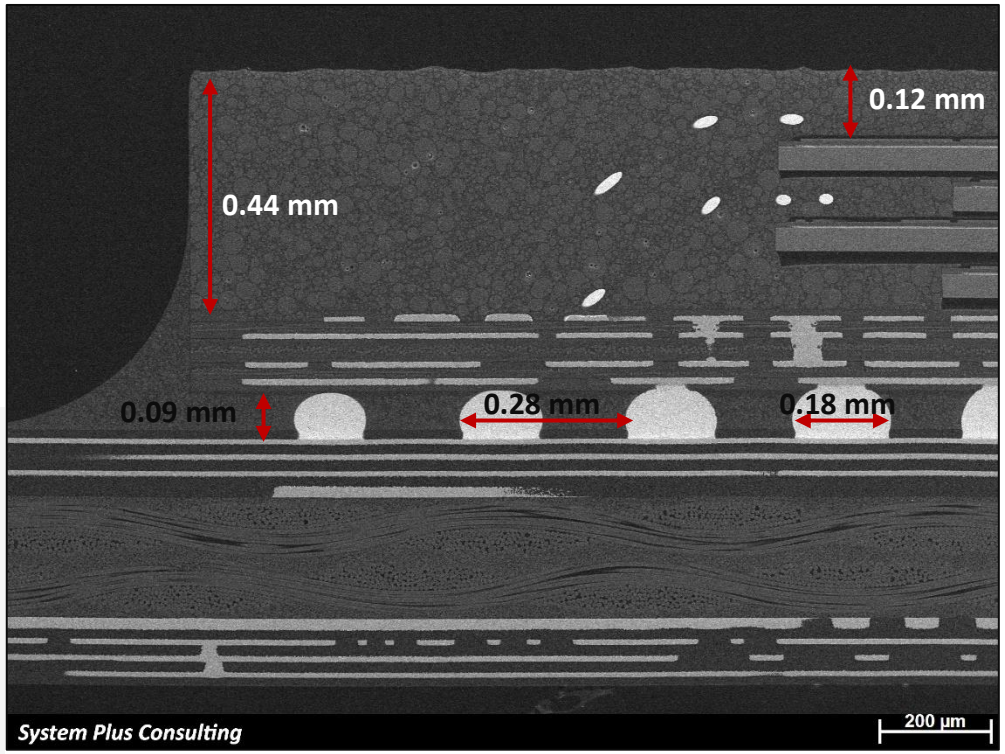
M1 SoC Package Cross Section

- DRAM Package is mounted on M1 SoC Package PCB.
- Two different types of underfill are used for the DRAM Package and for the M1 SoC Package PCB.

M1 Package Cross Section 2



DRAM Package Cross Section

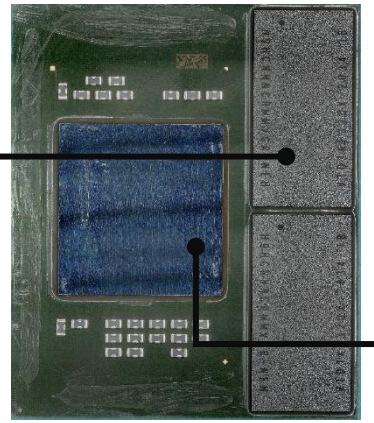


DRAM Package PCB

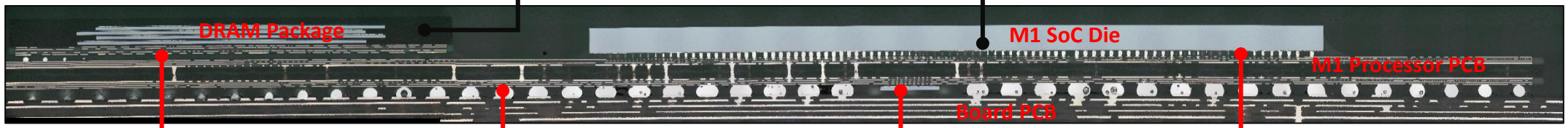
- DRAM dies are packaged in a BGA Package.
- DRAM Package molding thickness: 0.44 mm

- Solder balls connect the DRAM Memory to the M1 SoC PCB.
  - Ball Pitch: 0.28 mm
  - Ball Diameter: 0.18 mm
  - DRAM Package Underfill Thickness: 0.09 mm

Package Cross Section – Summary



M1 SoC Package – metal cover Removal



M1 SoC Package Cross Section

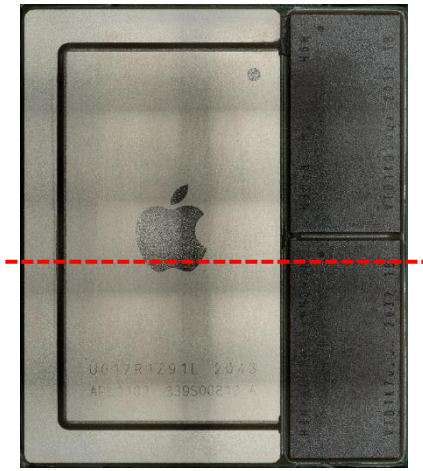
DRAM Package Balls
- *M1 Package PCB Ball pitch: 280 µm*
- *Ball Diameter: 180 µm*

M1 SoC Package Balls
- *M1 Package PCB Ball pitch: 500 µm*
- *Ball Diameter: 320 µm*

Capacitor
- *Capacitor microbump Pitch: 120 µm*
- *Microbump Diameter: 48 µm*

M1 SoC Die Microbumps
- *M1 Die microbump Pitch: 112 µm*
- *Microbump Diameter: 56 µm*

Package Cross Section – Summary



M1 SoC Package
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M1 SoC Package Cross Section
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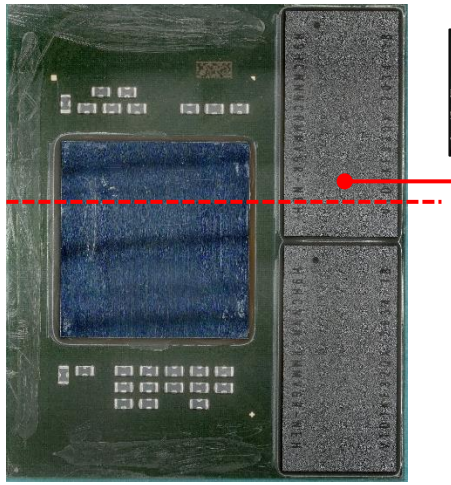
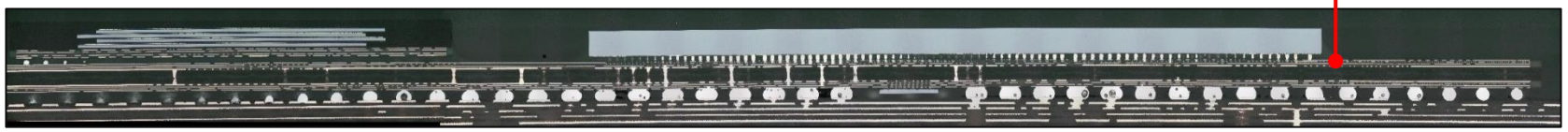
Package Cross Section Reveals
- *IHS Metal Cover*
- *DRAM Memory*
- *M1 SoC Die*
- *Package PCB*
- *Embedded Capacitor*

Package Cross Section Reveals
- *DRAM Memory*
- *M1 SoC Die*
- *Package PCB*
- *Capacitor on PCB Backside*



M1 SoC Package Opening
©2020 by System Plus Consulting

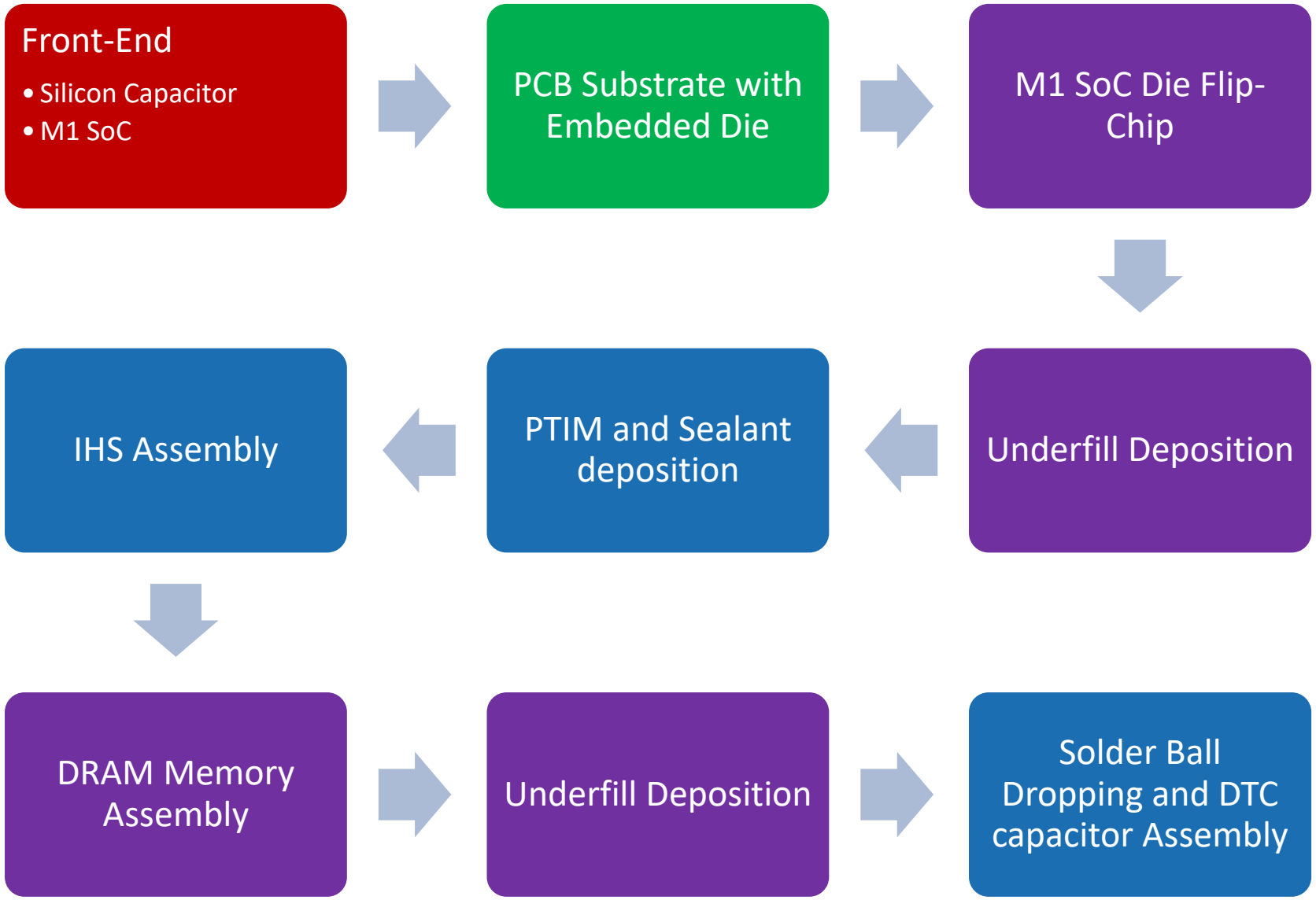


M1 SoC Package Cross Section
©2020 by System Plus Consulting

Package Opening Reveals
- *DRAM Memory*
- *M1 SoC Die*
- *Capacitor on PCB Backside*

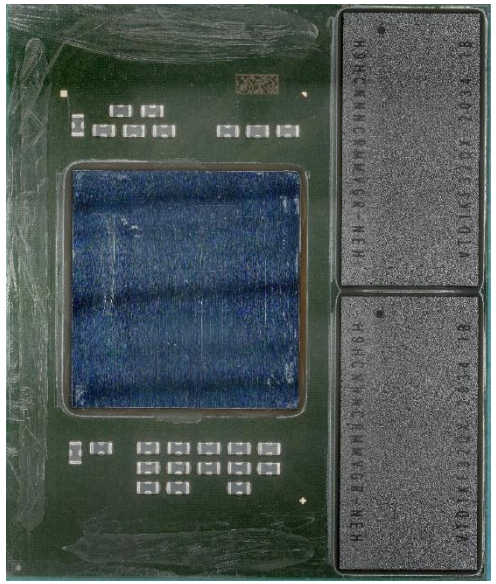
The M1 SoC Package integrates.
- **2** DRAM Packages (32Gb each)
- **1** M1 SoC Die
- **24** (0402) Passive capacitors
- **6** Embedded capacitors
- **4** Capacitors on PCB Backside

M1 Package Process Characteristic



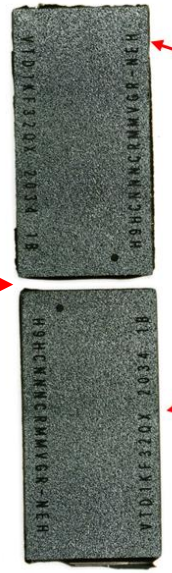
PHYSICAL ANALYSIS
D R A M

M1 Package Teardown



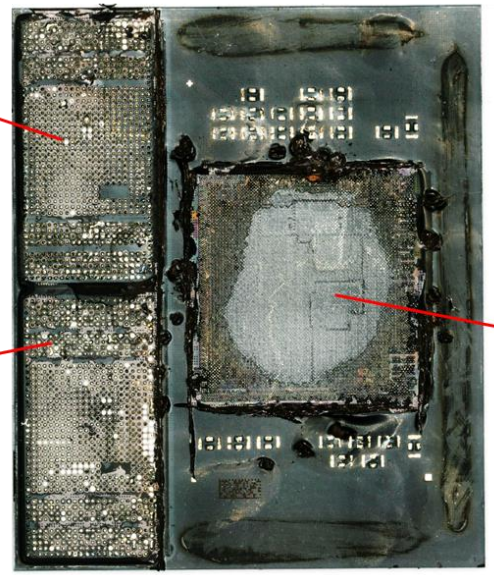
M1 Package Top view
©2020 by System Plus Consulting

TearDown



DRAM Memory Package
©2020 by System Plus Consulting

DRAM Package Removal



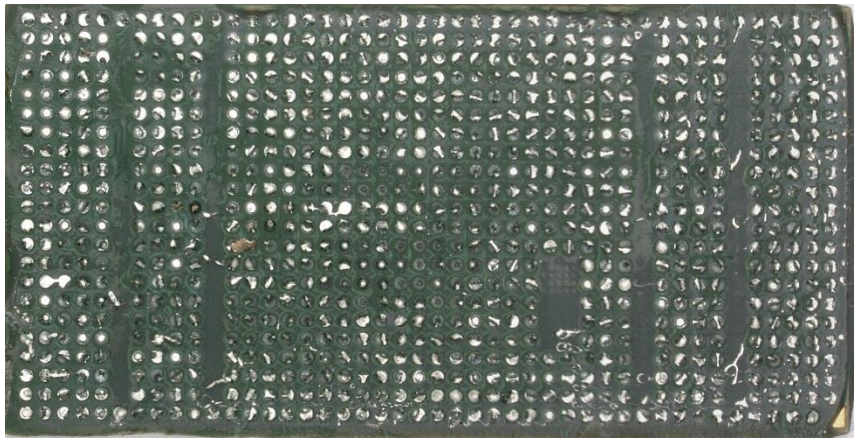
Package Cross-Section – Optical View
©2020 by System Plus Consulting

M1 SoC Die
©2020 by System Plus Consulting

DRAM Package Marking

- Package: BGA-877 pin
- Dimensions: 13.1 x 6.6 x 0.57 mm
- Surface: 86.4 mm²
- BGA Pitch : 0.28 mm

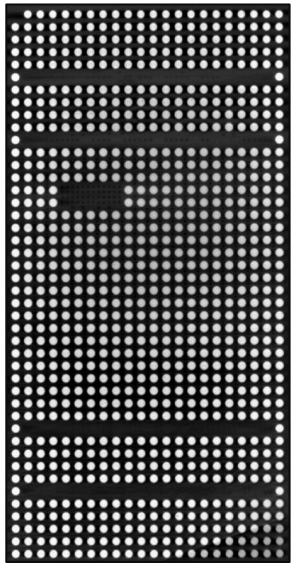
Memory Package Top view



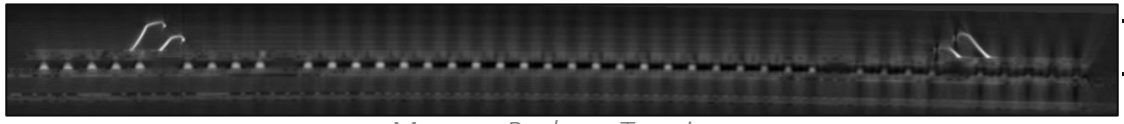
Memory Package Back view

DRAM Package Marking

Memory Package Top view
©2020 by System Plus Consulting



Memory Package Footprint
©2020 by System Plus Consulting



Memory Package Top view
©2020 by System Plus Consulting

Memory Package Top view
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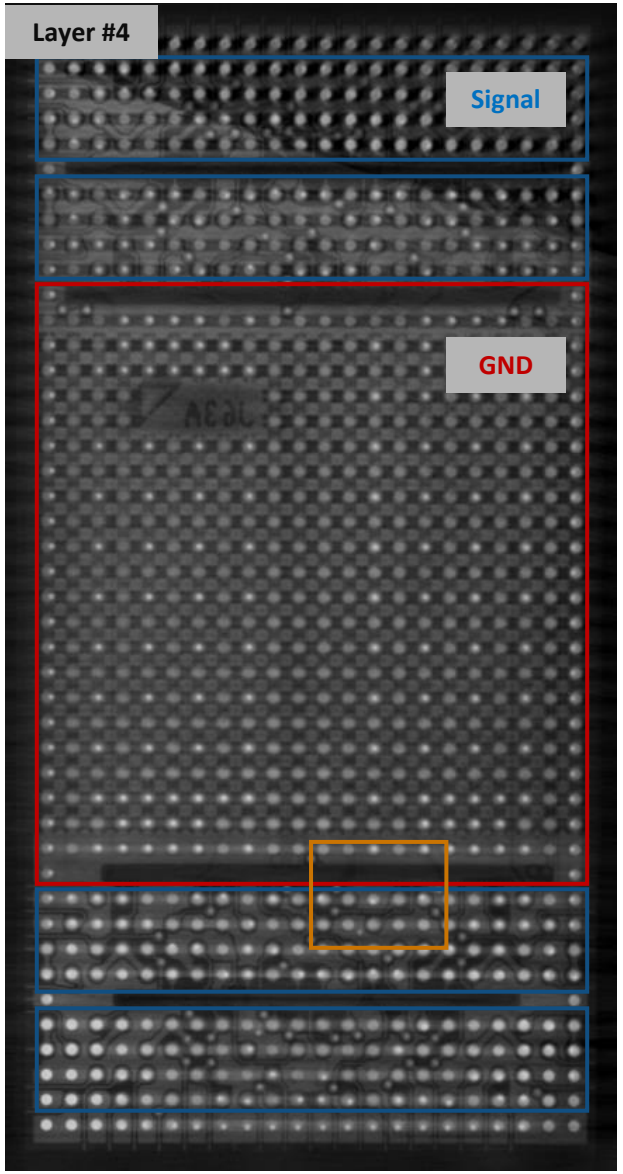
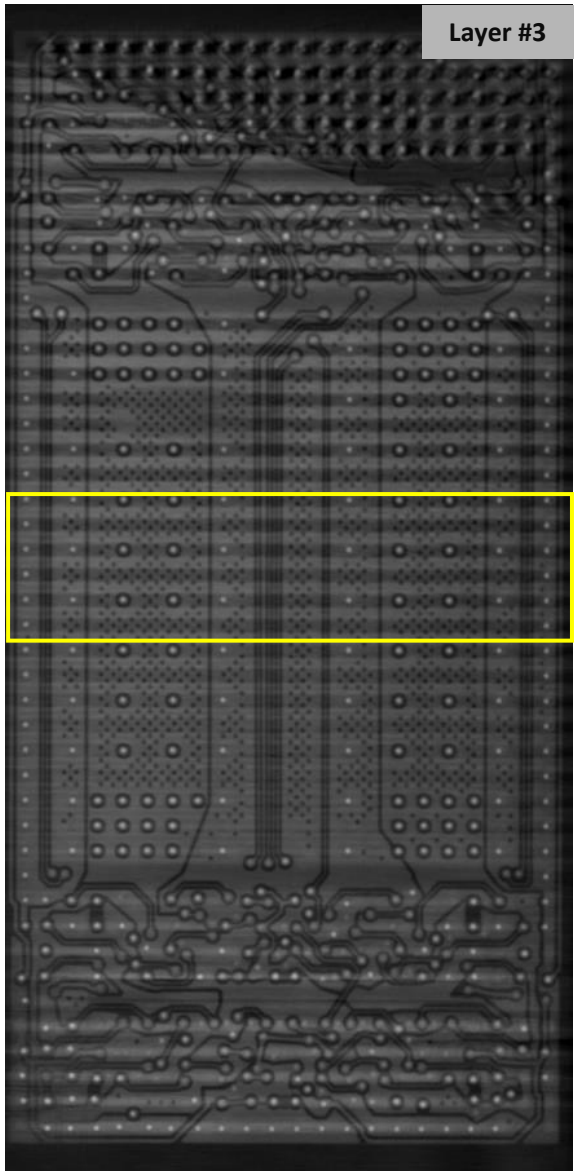
Attribute	Measurements
DRAM Form Factor	13.1 x 6.6 mm
BGA Count	877
BGA Pitch	0.28 mm
# of Die	4
Die Thickness, 1-4	38 µm
DAF Thickness	20 µm
Total DRAM Thickness	53 µm
DRAM package Thickness	0.57 mm
Total Mold Thickness	0.44 mm
Overmold Thickness on Die	0.12 mm
Die edge to Mold Edge	0.99 mm / 1.3 mm
Die Size	34.02 mm²
Ball Pitch	0.28 mm

P/N	H 9HC	NNN	CR	M	M	VG	R	-N	E	H
Decode	Hynix LPDDR 4	No NVM	32 Gb	1.1V/0.6V	1st Gen.	New PKG	Pb & Halogen Free	No NVM	4266 Mbps	Special Temp.

DRAM Package Substrate layer – X-Ray

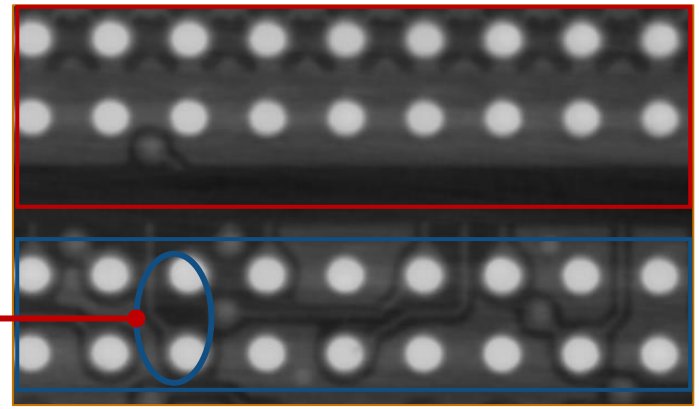


Memory Package Layer #4 – X-ray



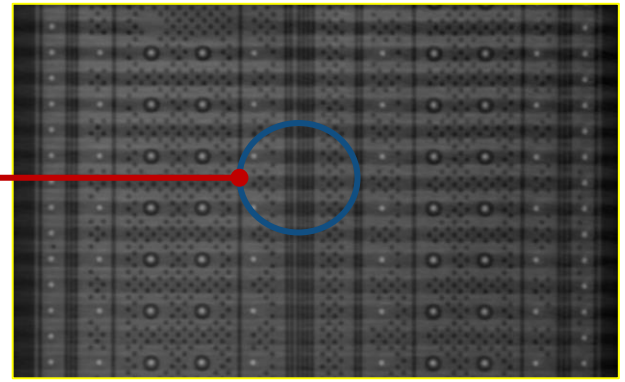
Memory Package Layer #3 – X-ray

- The signals pads are located in the first 10 rows of the north and the south side of the DRAM.



Memory Package Layer #4 – X-ray

BGA Pad: **181 µm**
Pitch: **281 µm**

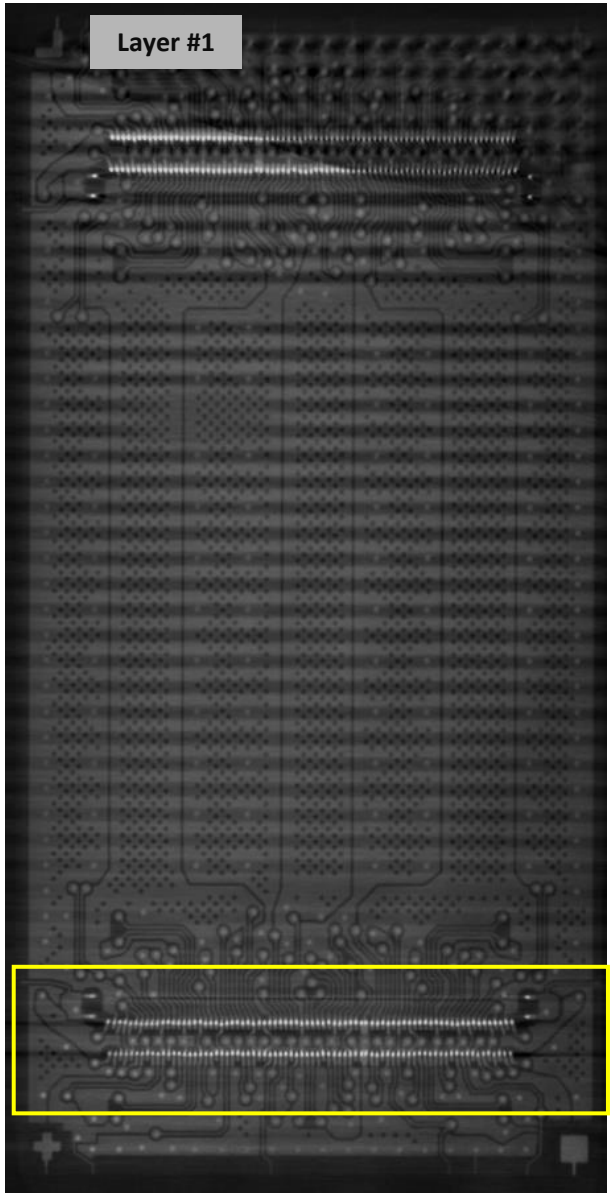


Memory Package Layer #3 – X-ray

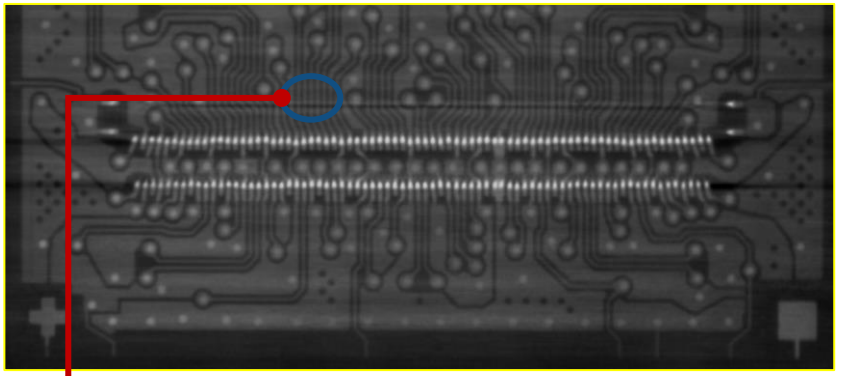
Line Space/Width: **24/20.9 µm**
Pitch: **45 µm**
Via pad: **105 µm**

DRAM Package Substrate layer – X-Ray

Memory Package Layer #2 – X-ray

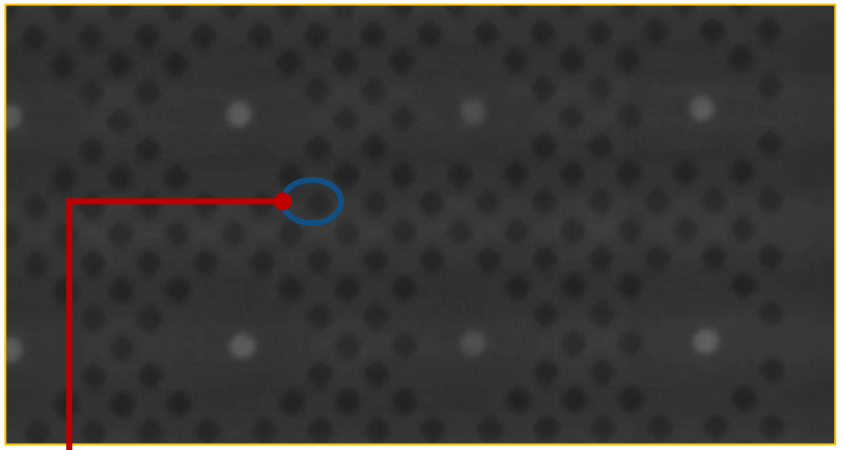


Memory Package Layer #1 – X-ray



Memory Package Layer #2 – X-ray

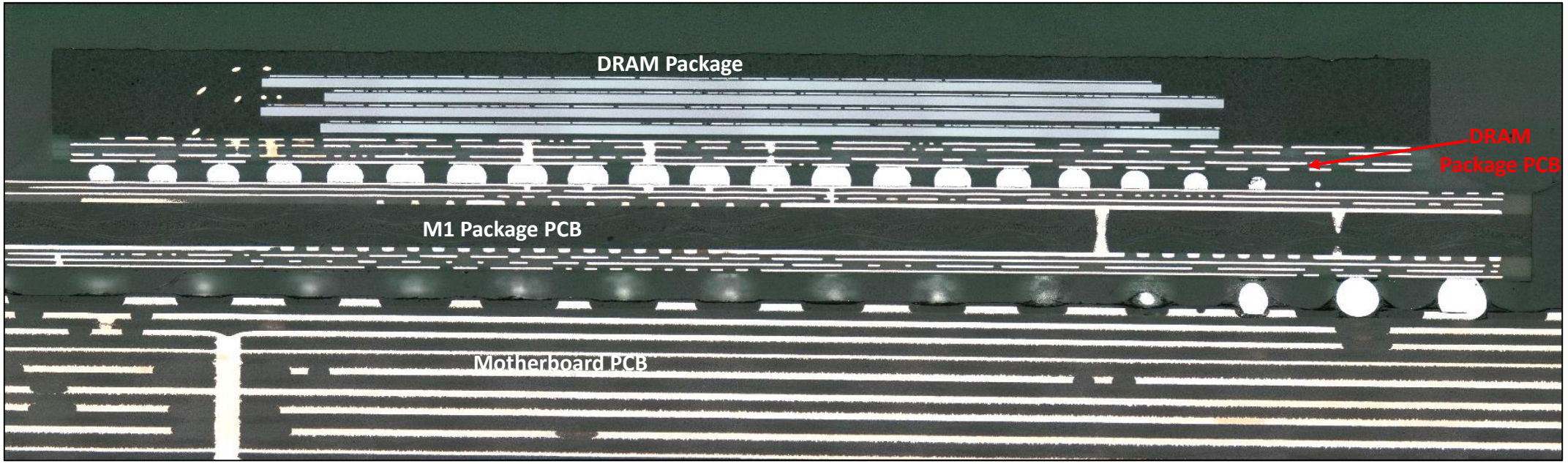
Line Space/Width:	**26.8/22 µm**
Pitch:	**48.8 µm**
Via pad:	**113 µm**



Memory Package Layer #1 – X-ray

Adhesion Square size:	**52 µm**
Adhesiion Square pitch:	**92 µm**

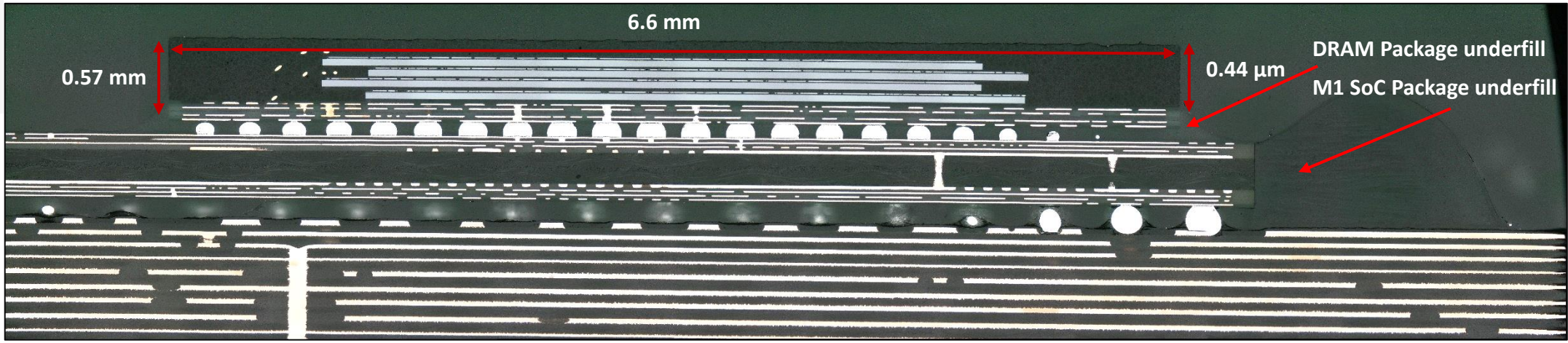
DRAM- Package Cross Section



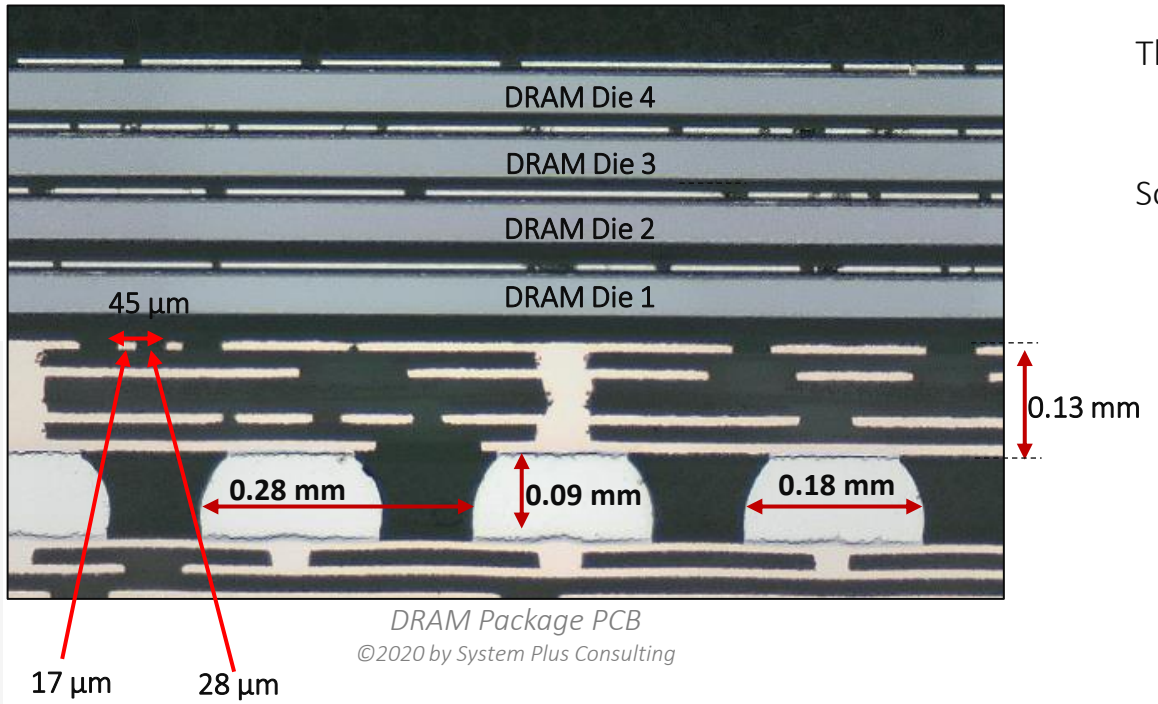
M1 SoC Package Cross Section

- Four DRAM Dies are integrated in one DRAM BGA Package.
- The DRAM Package is mounted on the M1 Package PCB.

DRAM- Package Cross Section Substrate



DRAM Package Cross Section



DRAM Package PCB

The DRAM package uses PCB substrate with 4 copper layers.

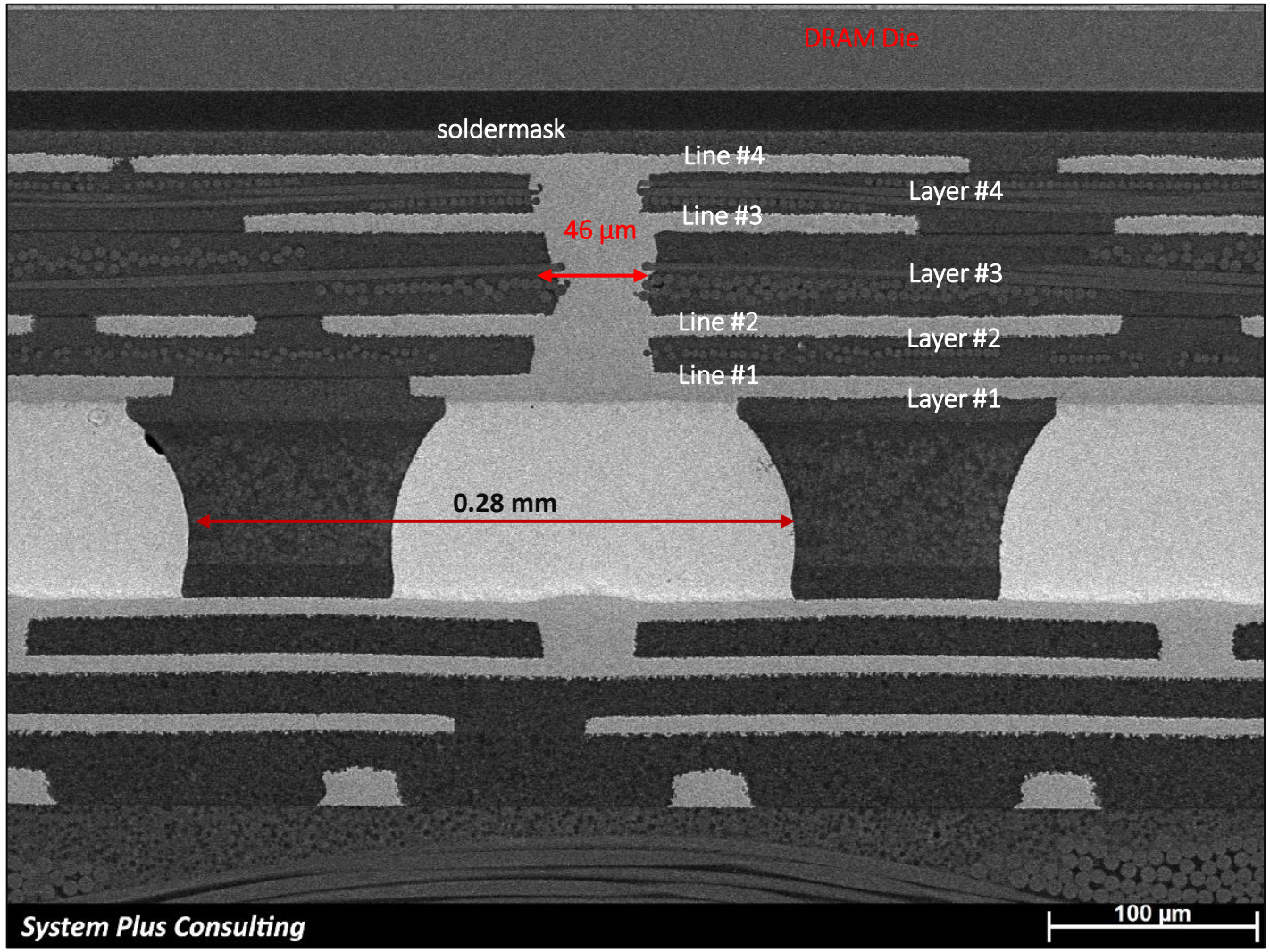
- PCB Thickness : 0.13 mm

Solder balls connect the DRAM Memory to the M1 SoC PCB.

- Ball Pitch: 0.28 mm
- Ball Diameter : 0.18 mm
- Separation between DRAM Package PCB and M1 SoC Package: 0.09 mm

- Measured Line/Space Pitch : 45 µm
- Smallest Line : 17 µm

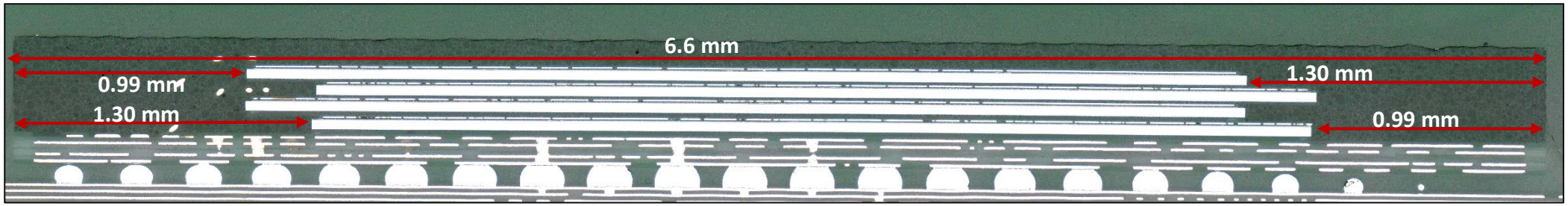
DRAM- Package Cross Section Substrate



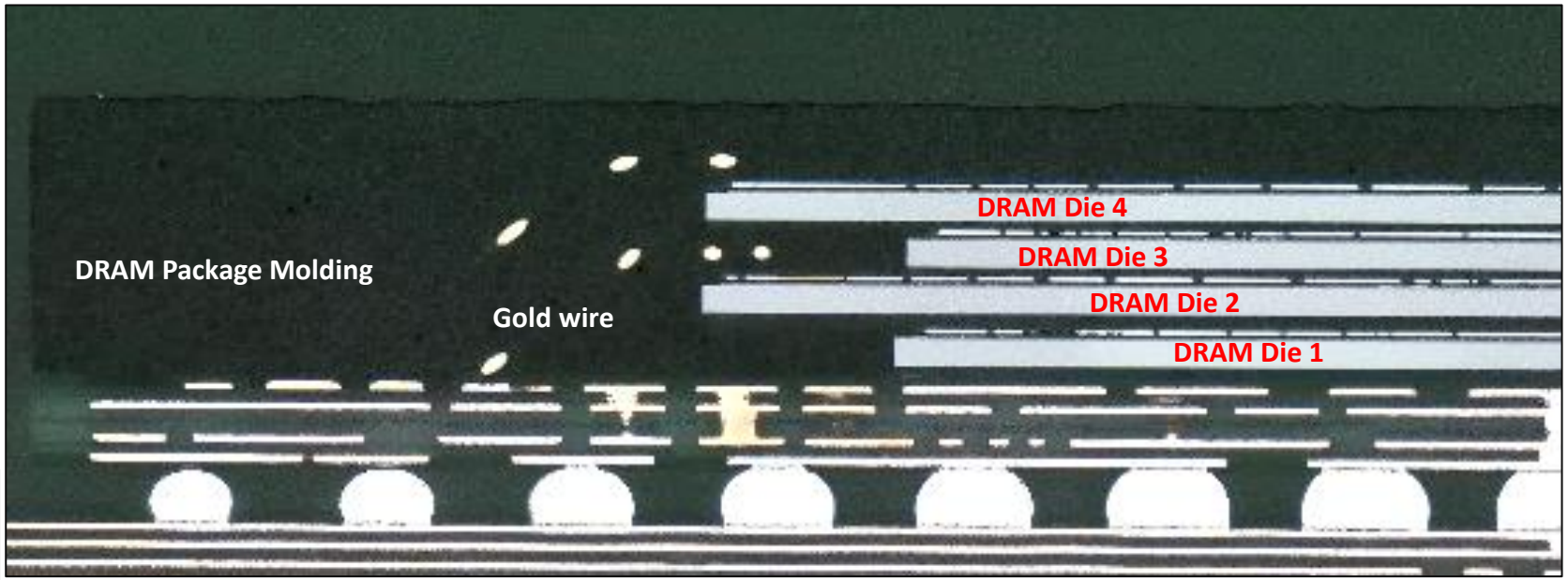
DRAM Package PCB

- PCB Copper MicroVia Diameter: 46 µm
- Copper line thickness:
  - Line #1: 9.1 µm
  - Line #2: 9.4 µm
  - Line #3: 8.5 µm
  - Line #4: 8.3 µm
- The PCB substrate is manufacturer using the conventional subtractive technology.
- Dielectric thickness:
  - Layer #1: 11.5 µm
  - Layer #2: 20.9 µm
  - Layer #3: 38.9 µm
  - Layer #4: 20.1 µm

DRAM- Package Cross Section



DRAM Package Cross Section



DRAM Package Cross Section

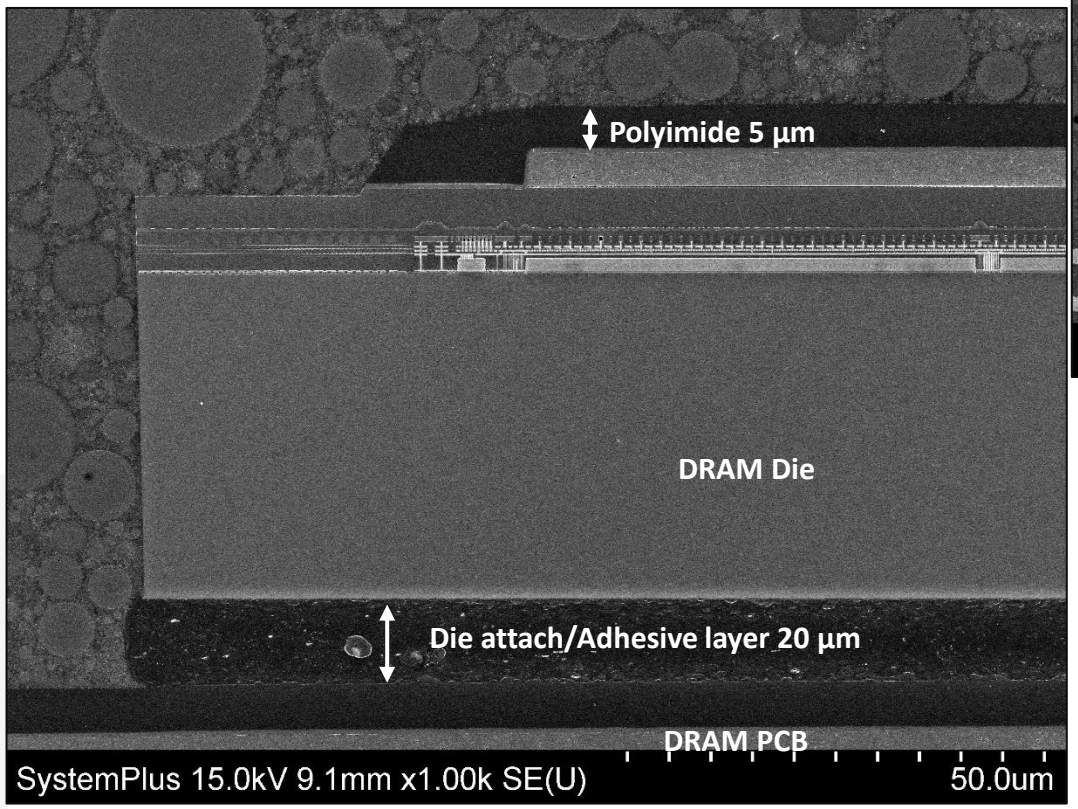
- 4 DRAM Dies are stacked in the package.
- DRAM dies are shifted to allow connection of the wire between the DRAM Die and the DRAM package PCB.
- The DRAM Package molding is symmetrical.
- Wire Material: Gold
- Wire Diameter: 17 µm

DRAM- Package Cross Section

- A thick adhesive layer (die attach) is deposited between each alternating die.

- Provide mechanical support and stability between the silicon die and the substrate and between silicon dies.
- Prevent bulking of dies due to stress or shock.

The die attach could also be critical for the electrical performance of the device.



DRAM Package Cross Section
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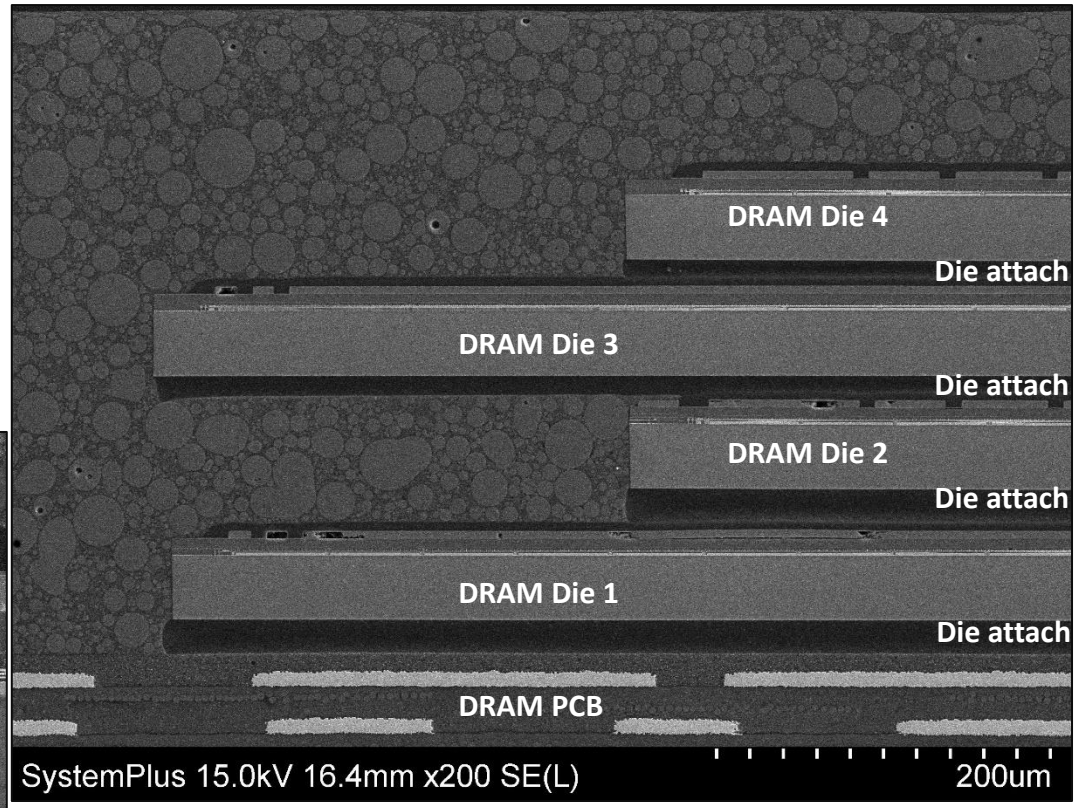

DRAM Package Cross Section
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- A polyimide layer is deposited to cover the metal layers on the DRAM dies, this protects the metal layers from degradation.

- Polyimide thickness: 5 µm
- Die attach layer: ~20 µm

DRAM Package Opening

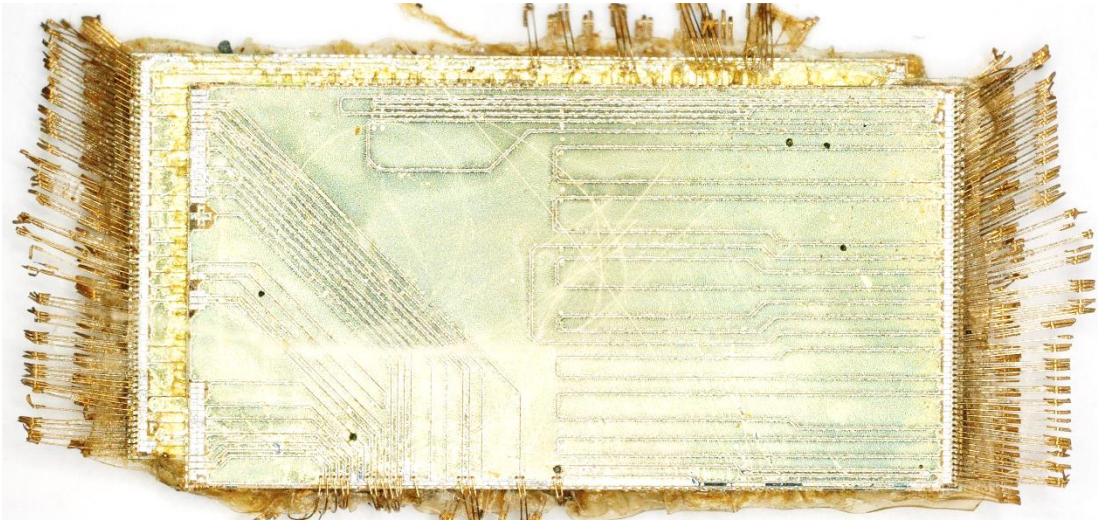
DRAM Package

Each DRAM Package has a capacity of 32Gb per package.

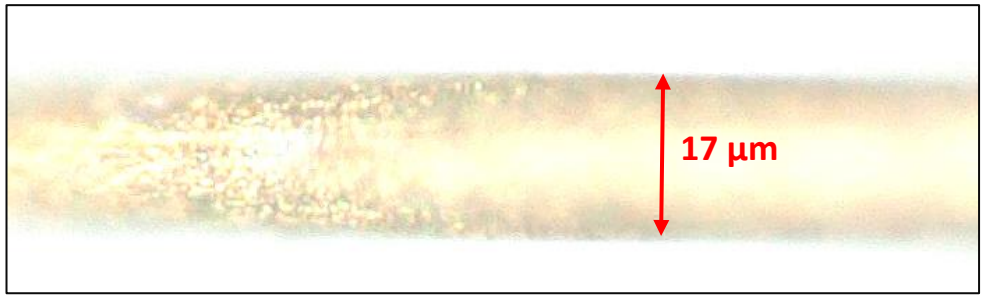
There are 4 dies in each DRAM Memory Package.

Therefore, each DRAM die capacity is 8Gb/1GB.

- Total Number of interconnect wires: 356 for 4 dies
- Inteconnect wires per die: 89
- Wire Diameter : ~ 17 µm
- Wire Material : Gold
- Wire average length: 1.1 mm

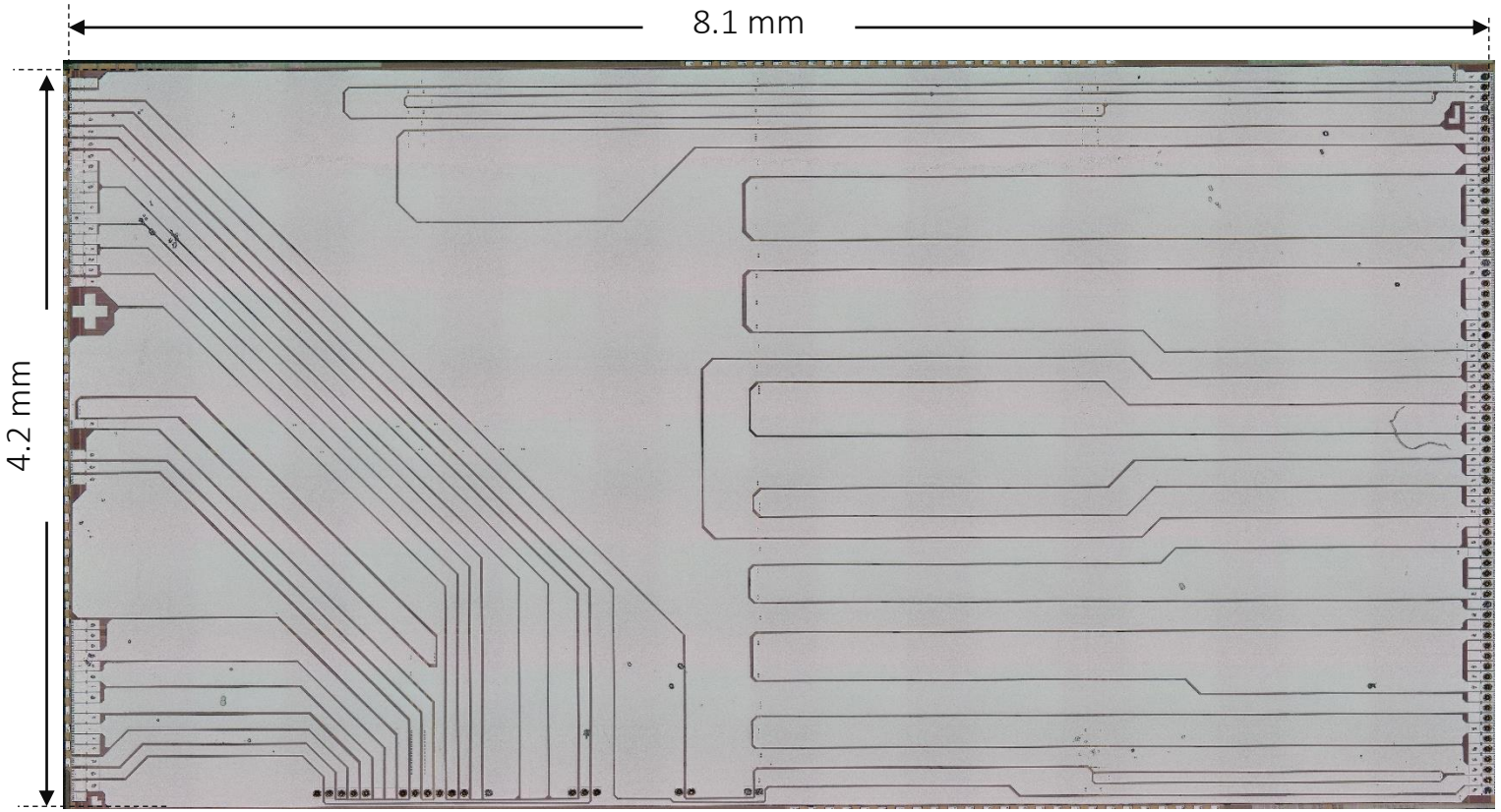


DRAM Package Opening



Wire

DRAM Die Dimensions& View



DRAM Die View

Die Area : 34.02 mm²

(8.1 mm x 4.2 mm)

Pads per memory die

Pad number : 133

Wires connected : 89

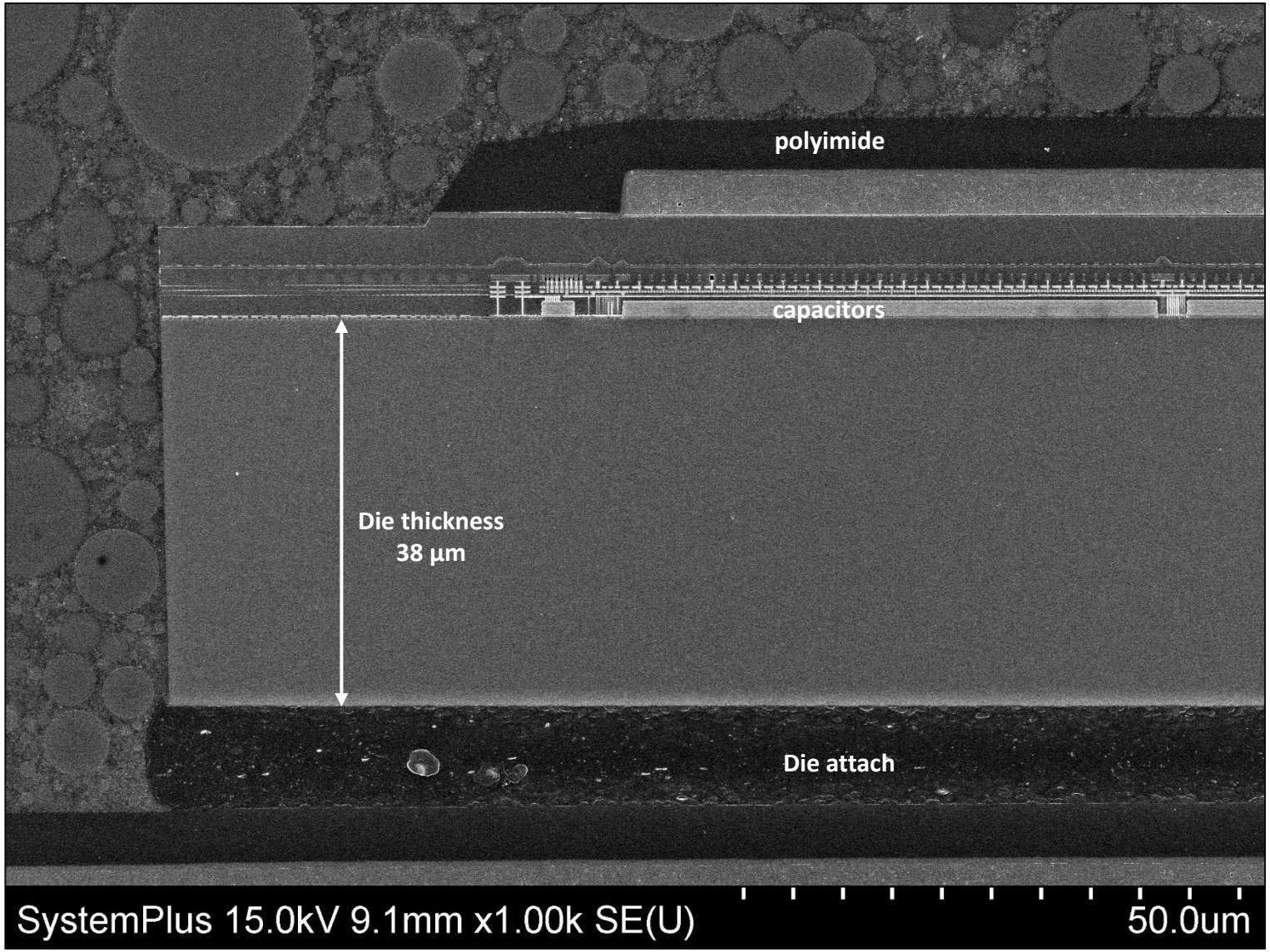
Test pads only: 32

Unused pads: 12

Die Density: 8Gb/34.02 mm²
0.24Gb /mm²

DRAM Die - Cross Section

- Memory die thickness: 38 µm

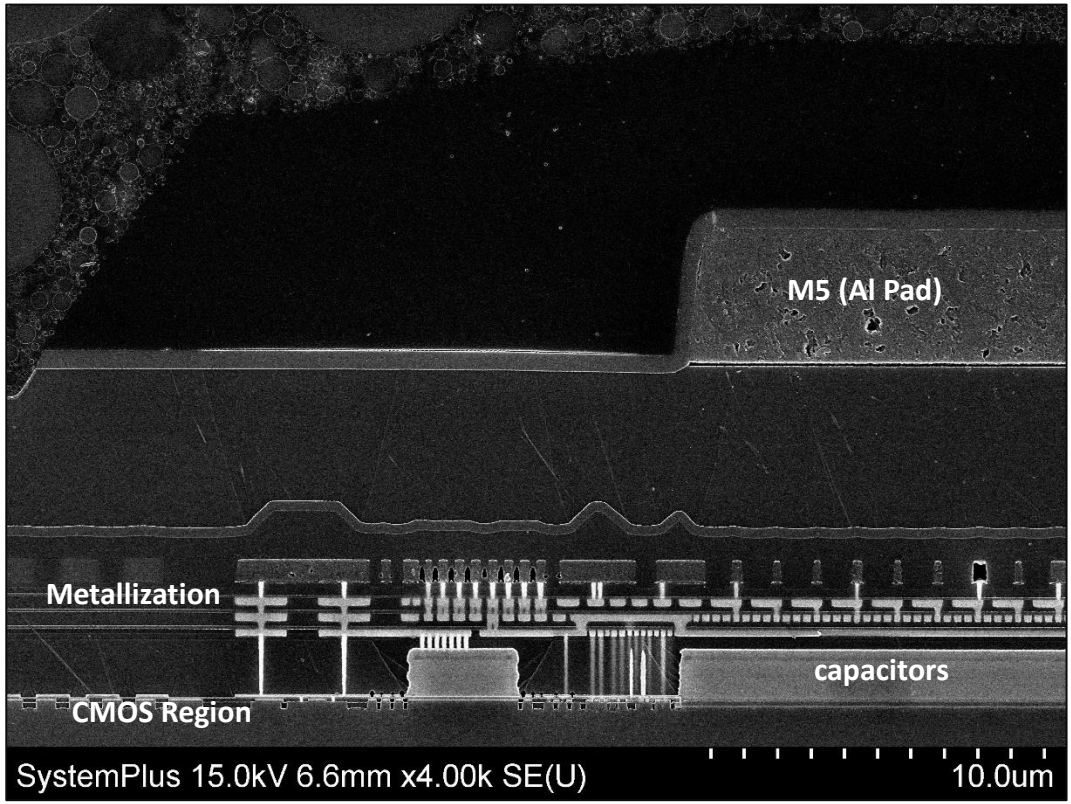


DRAM Die Cross Section

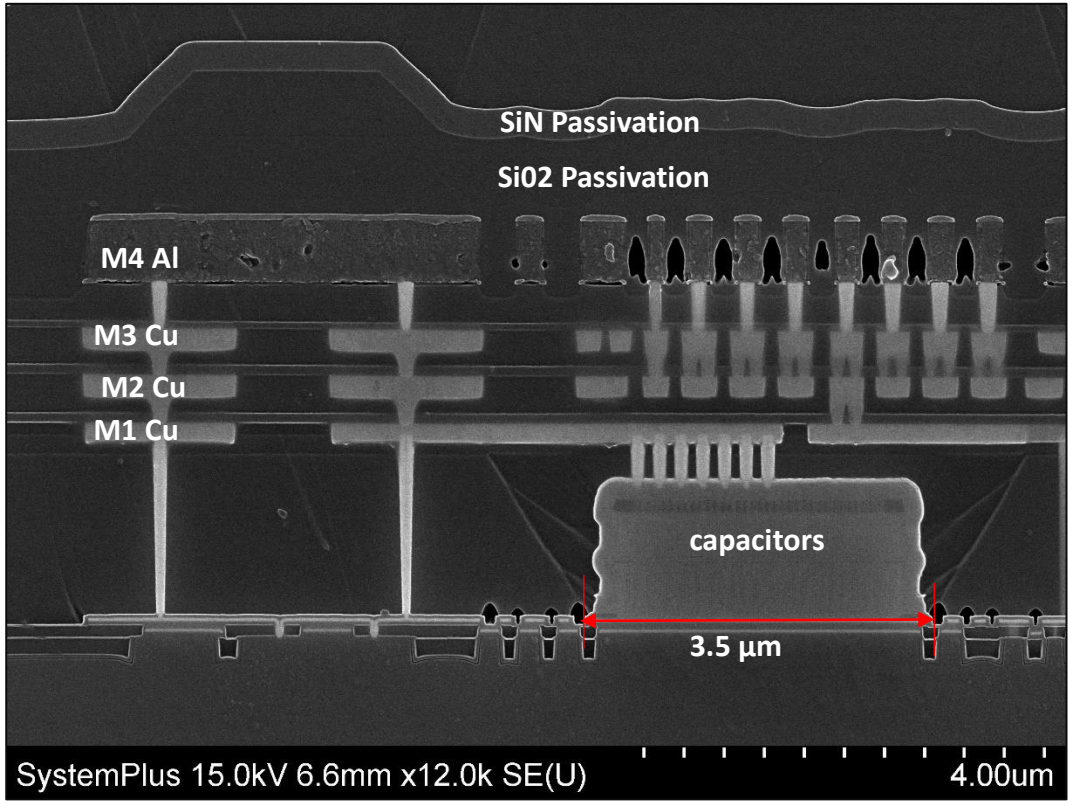
DRAM Die - Cross Section

DRAM memory cross-section reveals:

- Capacitors
- CMOS transistors
- Metal contacts and metal layers



DRAM Die Cross Section

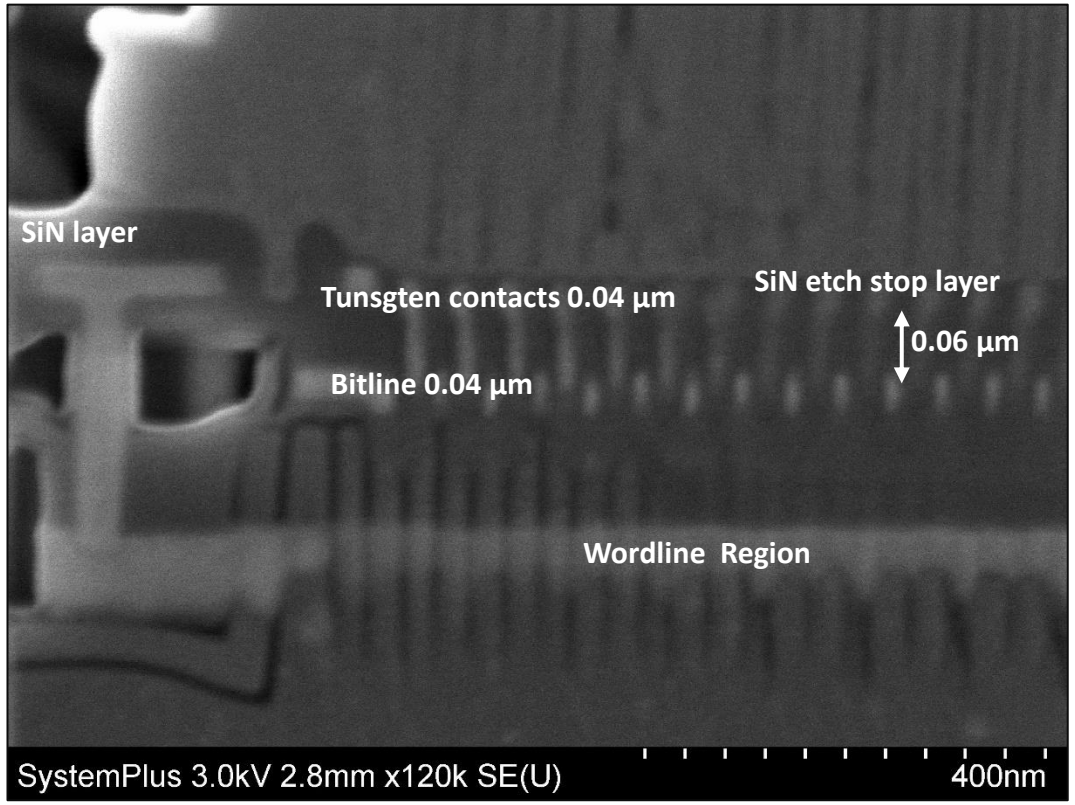


DRAM Die Cross Section

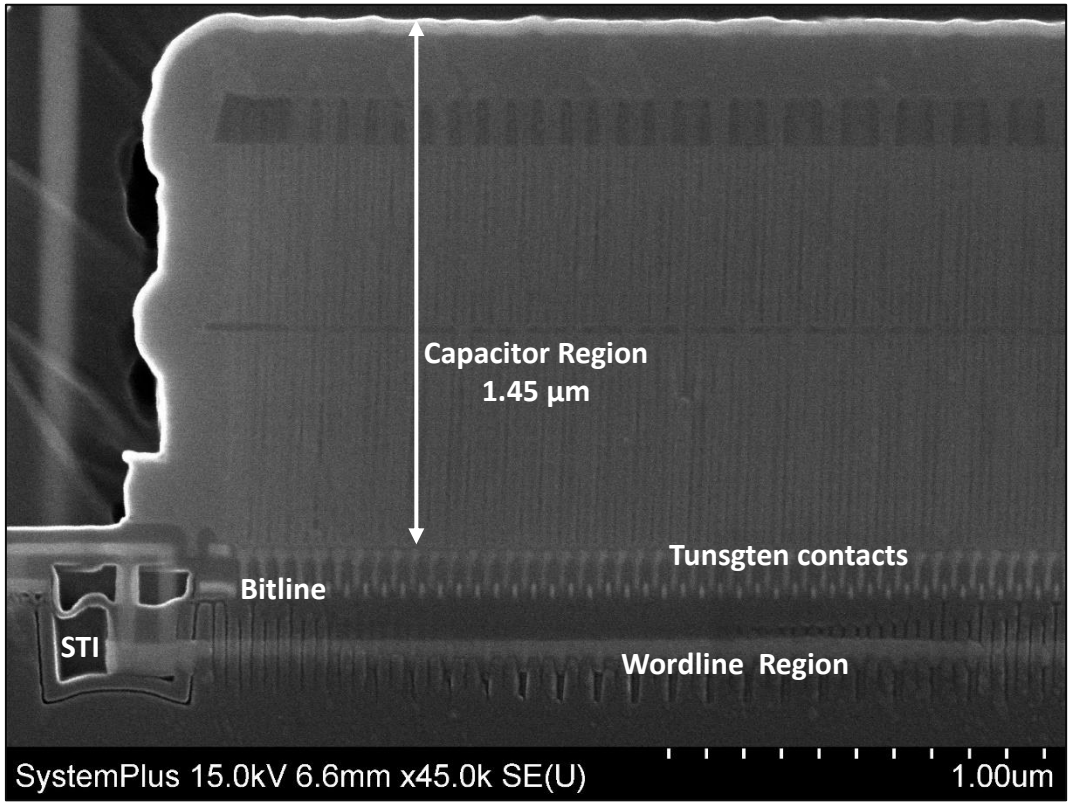
- The memory process uses Cu metal layers, Aluminium metal layer and a thick Aluminium metal pad.
- The memory process uses: 5 metal layers: 3 Cu + 2 Al

DRAM Die - Cross Section

- CMOS transistors and STI are formed at the base of the Silicon substrate.
- The STI isolate the CMOS transistors.
- Below the capacitors there is a wordline region, the wordlines are made of tungsten metal.
- A silicon oxide insulating trench isolates the wordlines.



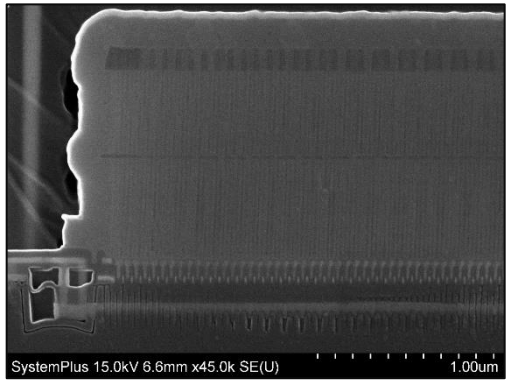
DRAM Die Cross Section



DRAM Die Cross Section

- After CMOS formation and wordline formation a layer of Silicon Nitride is deposited and patterned. This is followed by tungsten layer deposition to form bitline and tungsten contacts.
- The Silicon Nitride layer is deposited on top of the bitline contacts.

DRAM Die - Cross Section

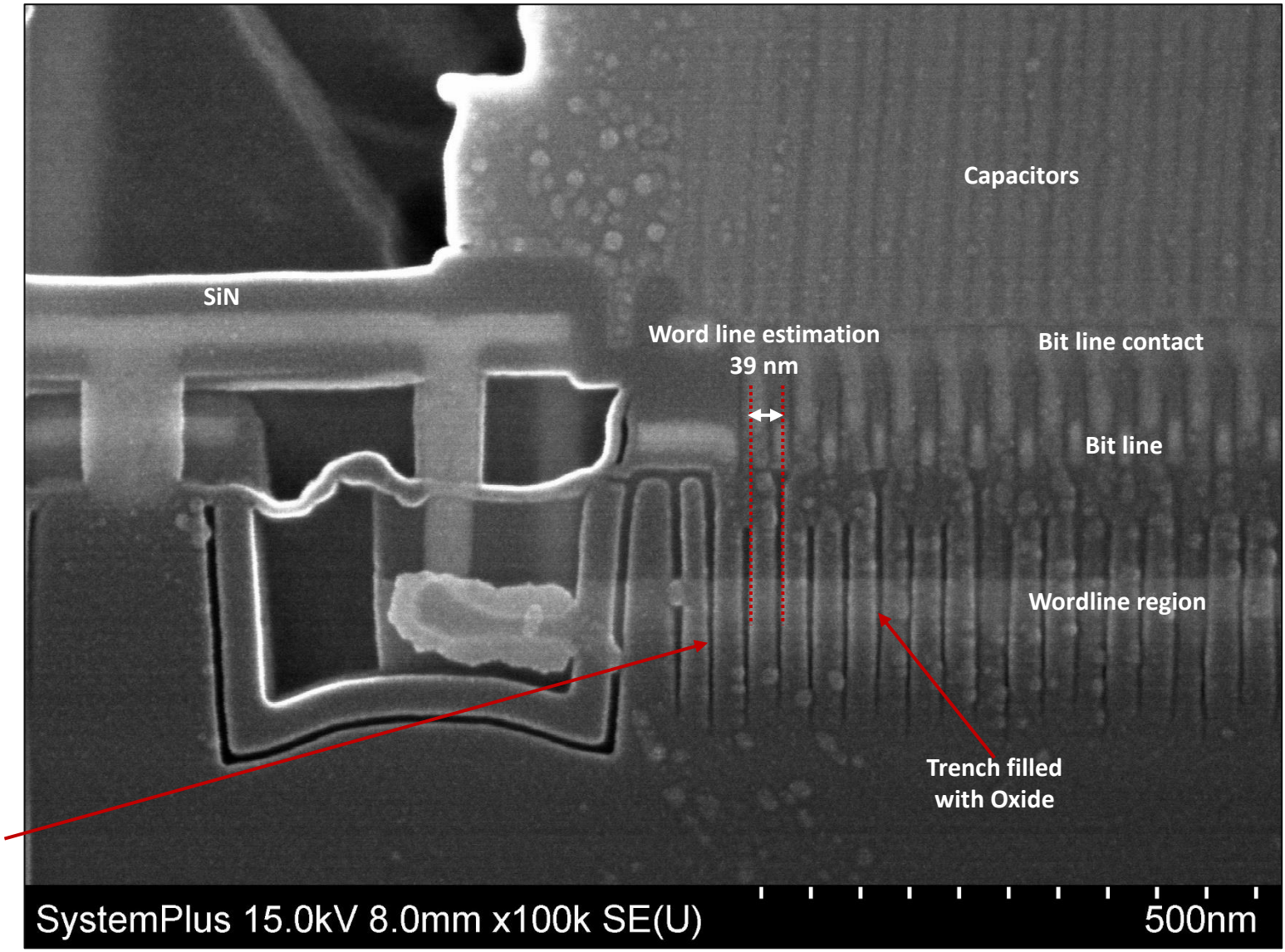


DRAM Die Cross Section

- A trench is formed by patterning the silicon and depositing silicon Oxide.
- The isolation layer in the trench defines the active patterns.

- Wordline Pitch Estimation:
  39 nm
- Estimated technology:
  19 nm

Trench- isolation region



DRAM Die Cross Section

DRAM Die - Cross Section

- The capacitors are built on the CMOS substrate.

Capacitor formation:

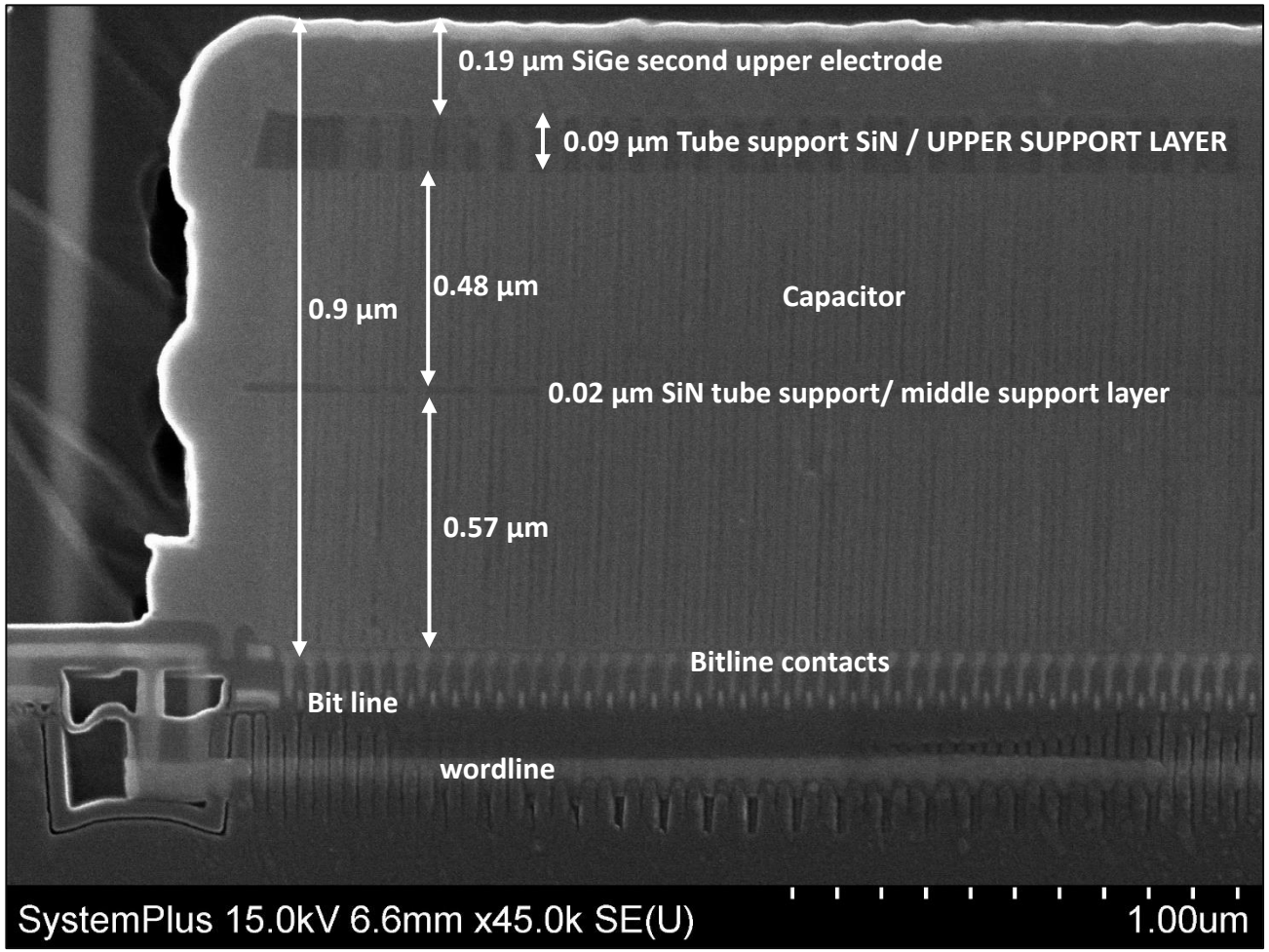
- A thin layer of silicon nitride is deposited followed by a thick sacrificial silicon oxide layer.
- A layer of SiN is then deposited that acts as the middle support layer.

- After the middle support layer of SiN, another thick layer of sacrificial silicon oxide is deposited.
- Finally, a layer of SiN layer is deposited for upper support layer/structure.

SiN etch stop layer:	0.01 µm
SiN middle support layer:	0.02 µm
SiN upper support layer:	0.09 µm

- The SiN top support, SiN middle support and the oxide layers are all etched at once to create the capacitor trench.
- One High Aspect Ratio etching step is performed during the manufacture of the capacitors.

- The middle and upper support structure provide lateral support to the capacitors.

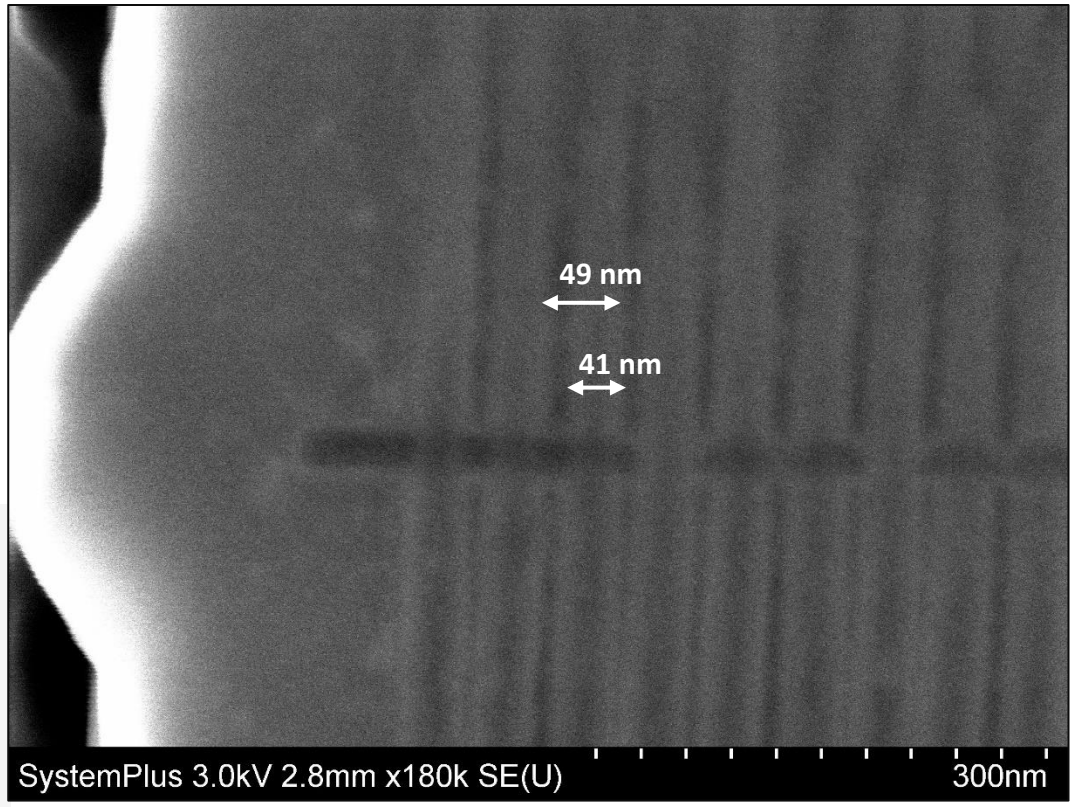


DRAM Die Cross Section

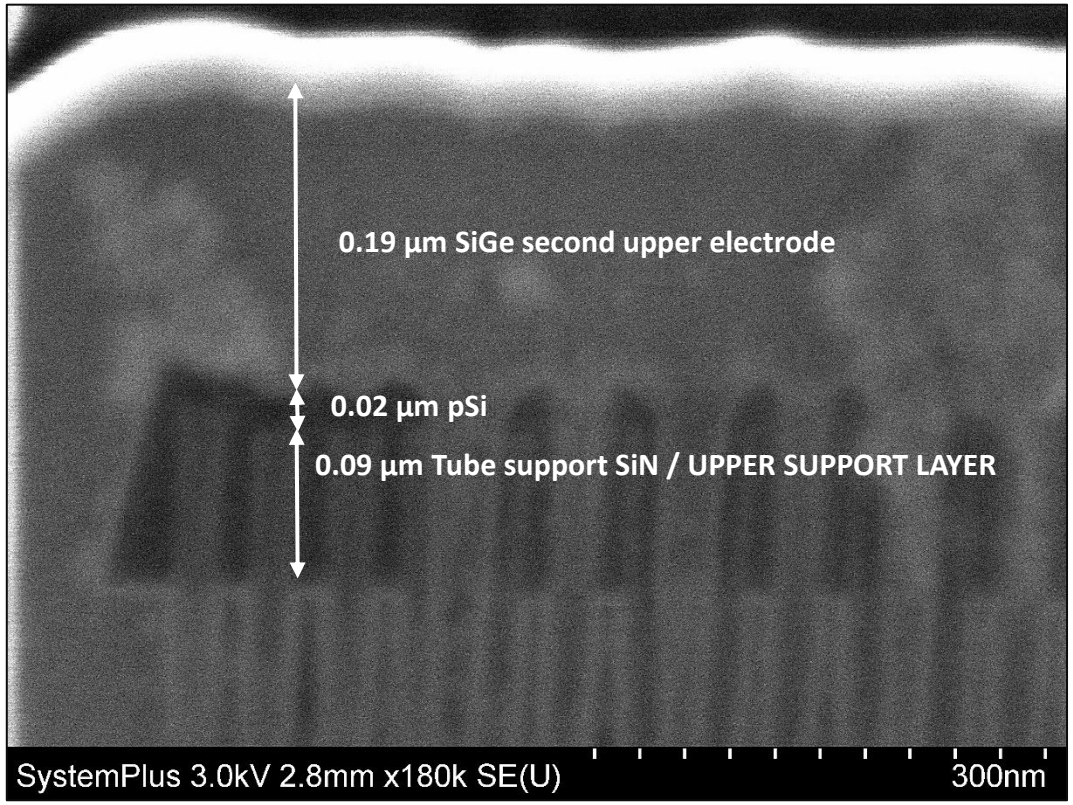
DRAM Die - Cross Section

The oxide between two capacitors prevents cell to cell charge interference.

- Capacitor width: 41 nm
- Capacitor pitch: 49 nm
- Oxide separating capacitors: 8 nm



DRAM Die Cross Section

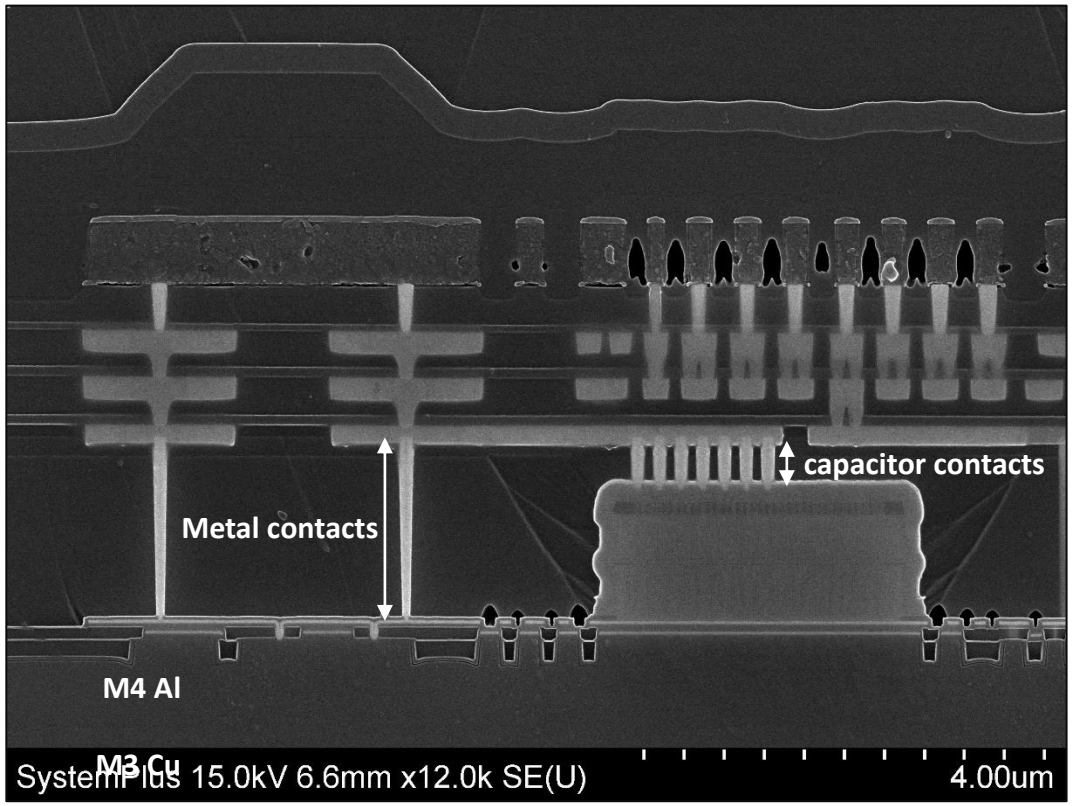


DRAM Die Cross Section

- The second conductive layer is formed by stacking SiGe on a polysislicon layer above the capacitors.
- A layer of tungsten metal envelopes the second SiGe electrode.

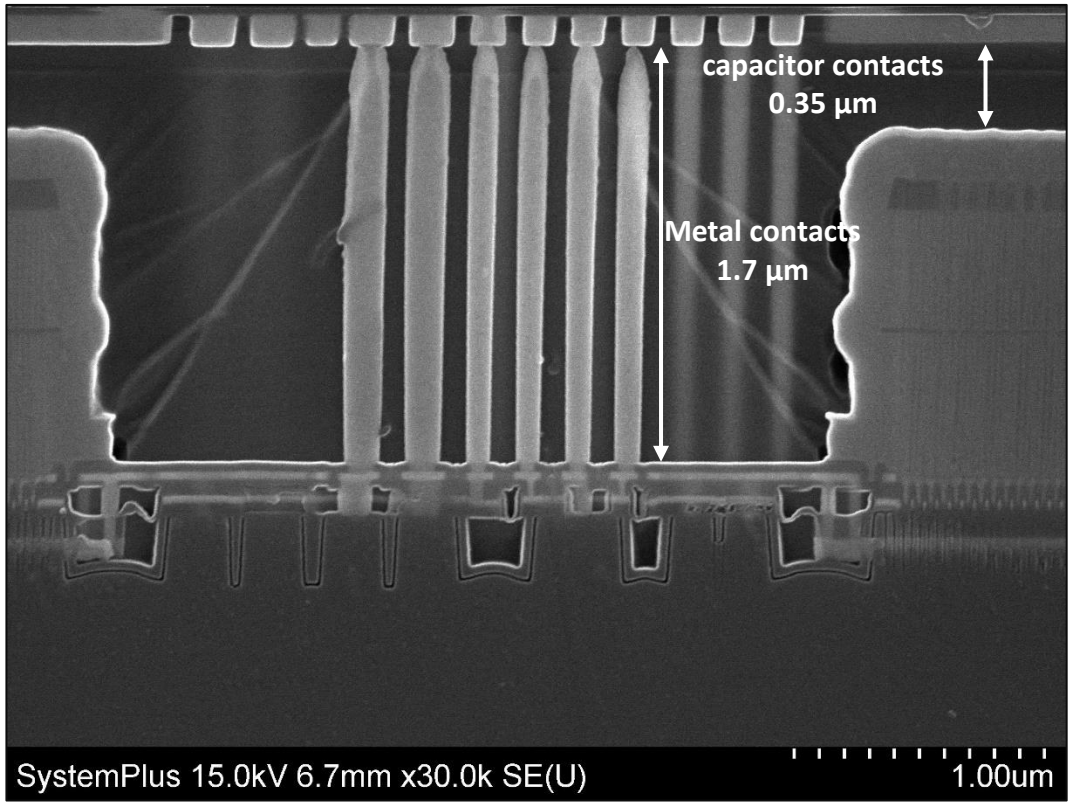
- Polysilicon layer: 0.02 µm
- Second electrode/ top electrode (SiGe): 0.19 µm

DRAM Die - Cross Section



DRAM Die Cross Section

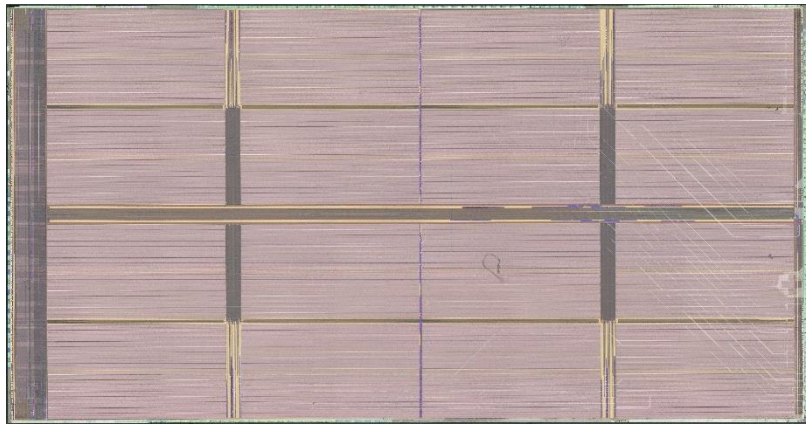
- Tungsten metal contacts connect the CMOS transistors and the bitline to the top metal layers.
- Silicon Oxide is patterned, and tungsten material is deposited. Tungsten contacts length: 1.7 µm
- Dual damascene technique is used to form the top copper metals.



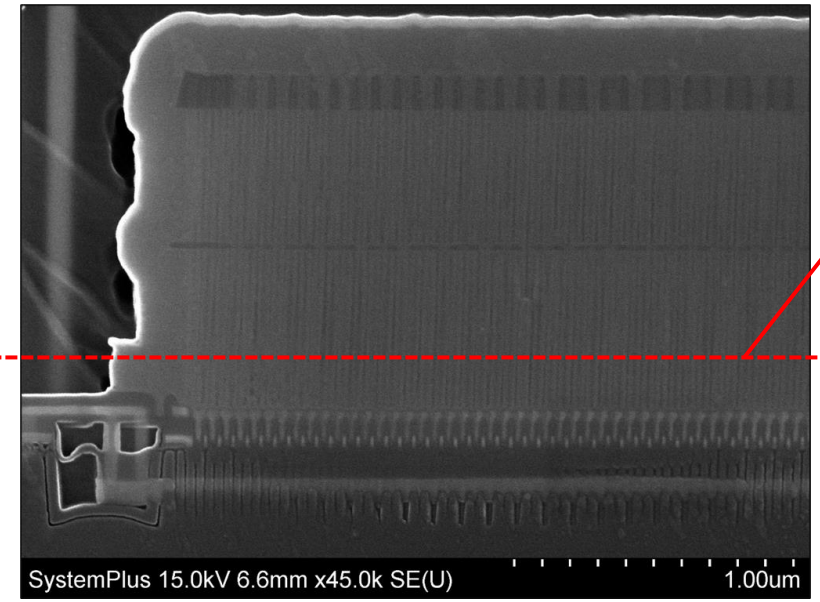
DRAM Die Cross Section

- Capacitor metal contacts connect capacitors to the top metal layers.
- Silicon Oxide is patterned, and Tungsten material is deposited.
- Capacitor contacts length: 0.35 µm

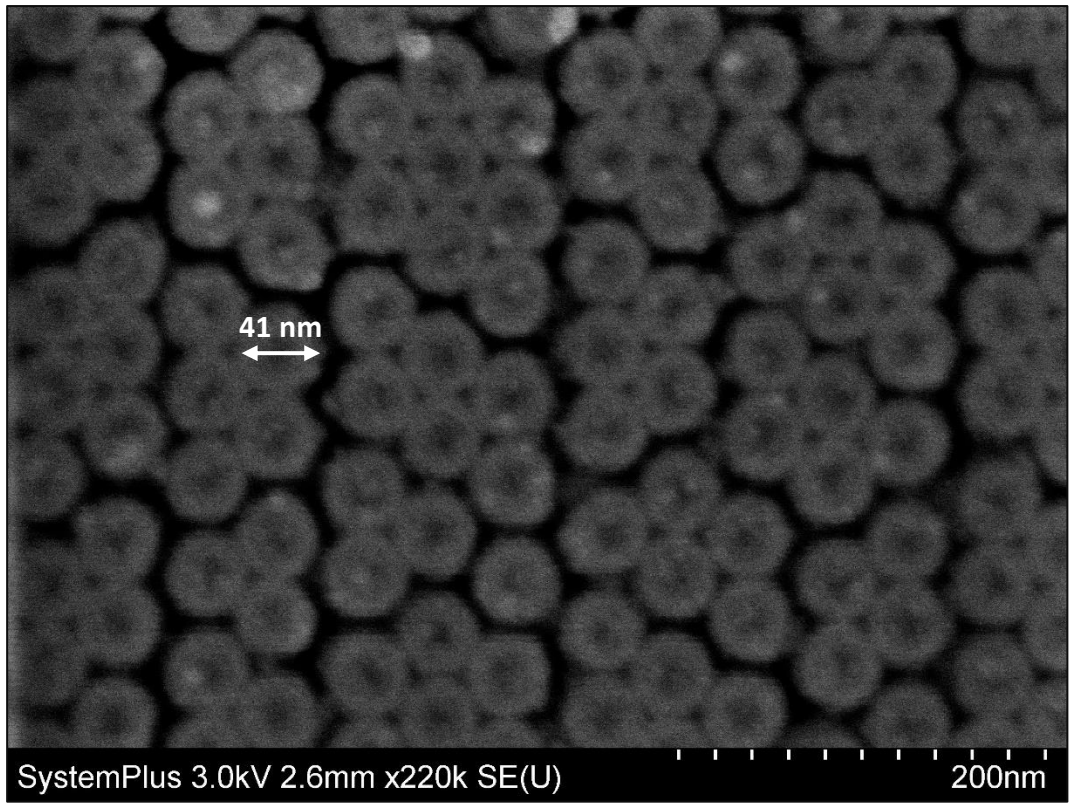
DRAM Die Delayering



Die Overview after removing of the metal Layers

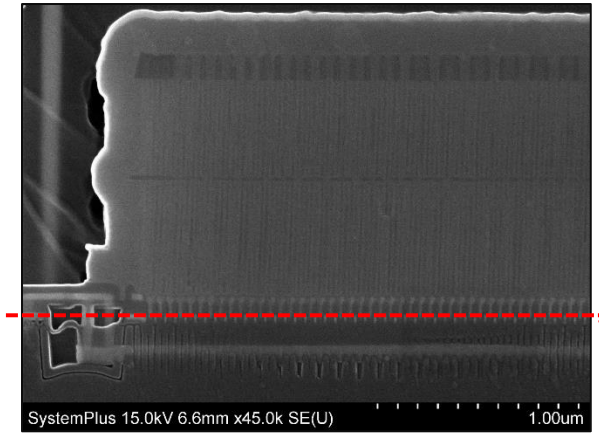


DRAM Die Cross Section



DRAM Die Delayering- Capacitors

DRAM Die Delayering



DRAM Die Cross Section
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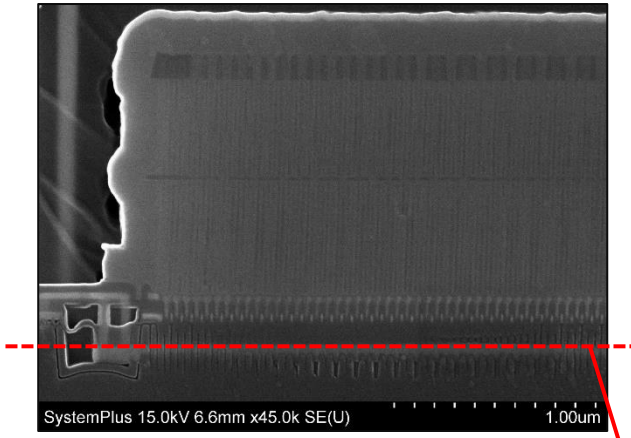

DRAM Die Cross Section
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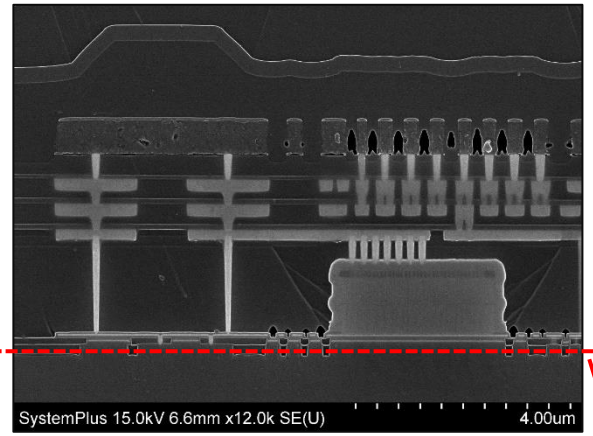

DRAM Die Cross Section
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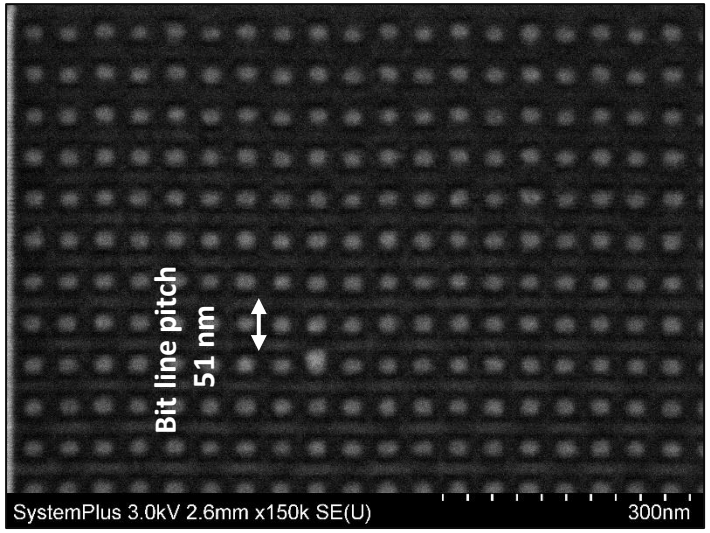

DRAM Die Delayering- Capacitors
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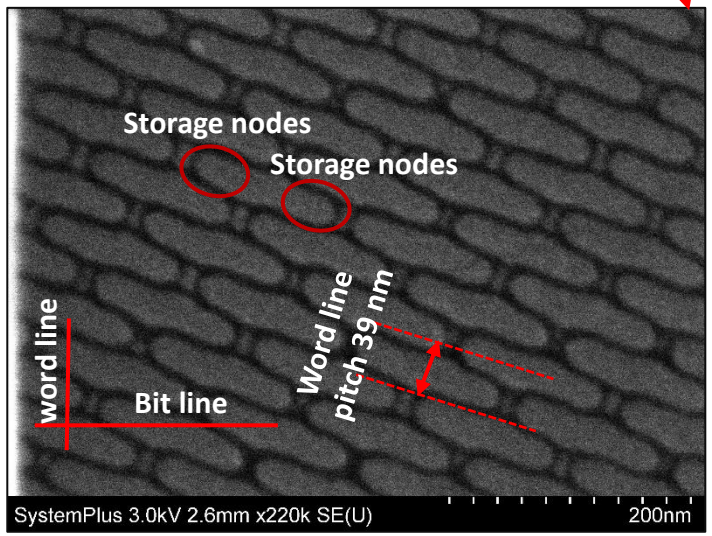

DRAM Die Delayering- Capacitors
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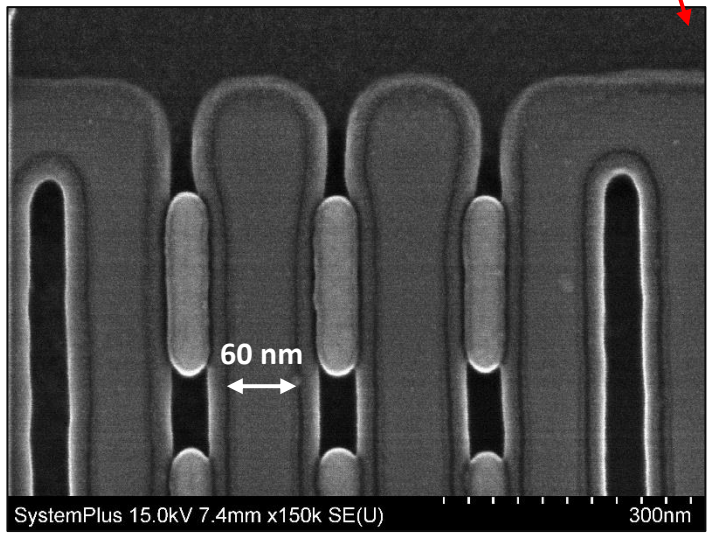

DRAM Die Delayering- Capacitors
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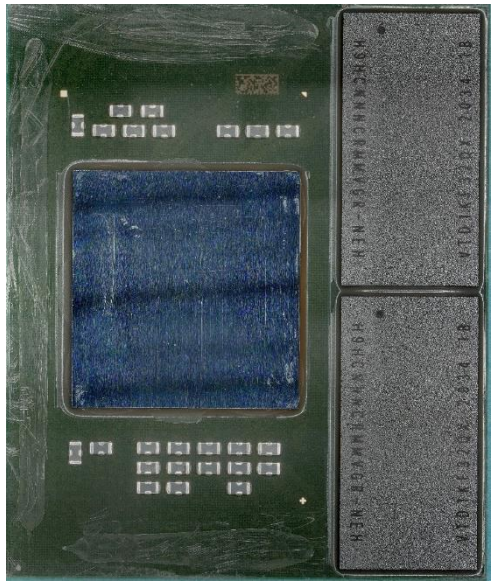
- Bitline pitch : 51 nm
- Word line pitch : 39 nm
- Estimated CMOS Transistor technology: 55 nm

PHYSICAL ANALYSIS
M1 SoC Die

M1 SoC Die Overview & Dimensions



M1 SoC Package Opening
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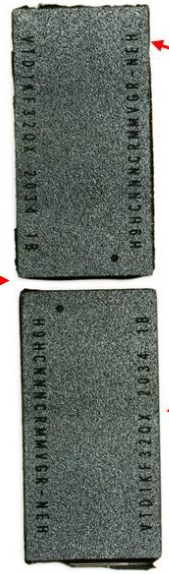
TearDown



DRAM Package
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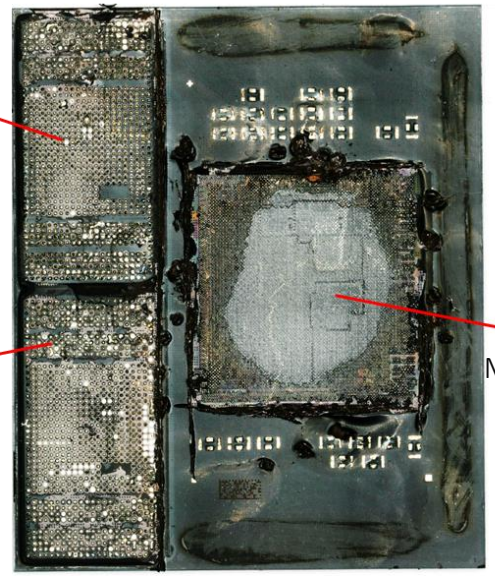
DRAM Package Removal



M1 SoC Package Opening
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M1 SoC Die

M1 SoC Die
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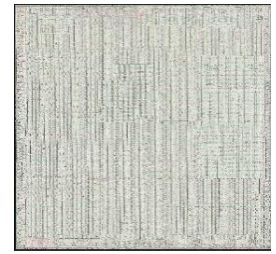

M1 SoC Die
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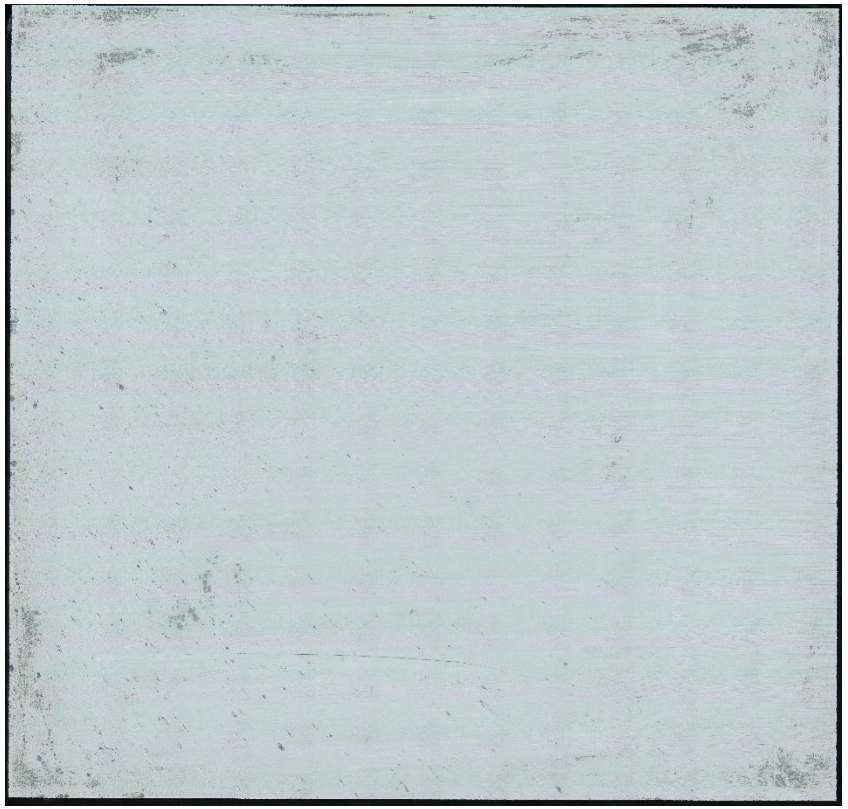
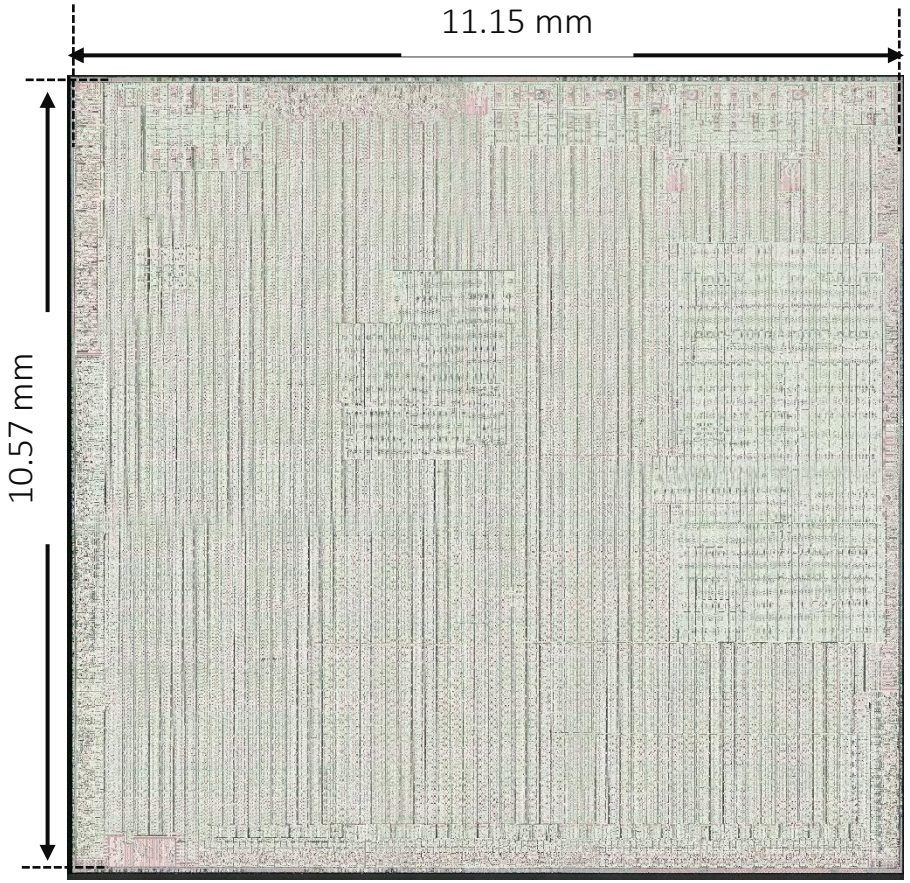
M1 SoC Die Overview & Dimensions

- Die dimension: (11.15 x 10.57 mm)

  117.8 mm²
- Pads: ~ 16, 500

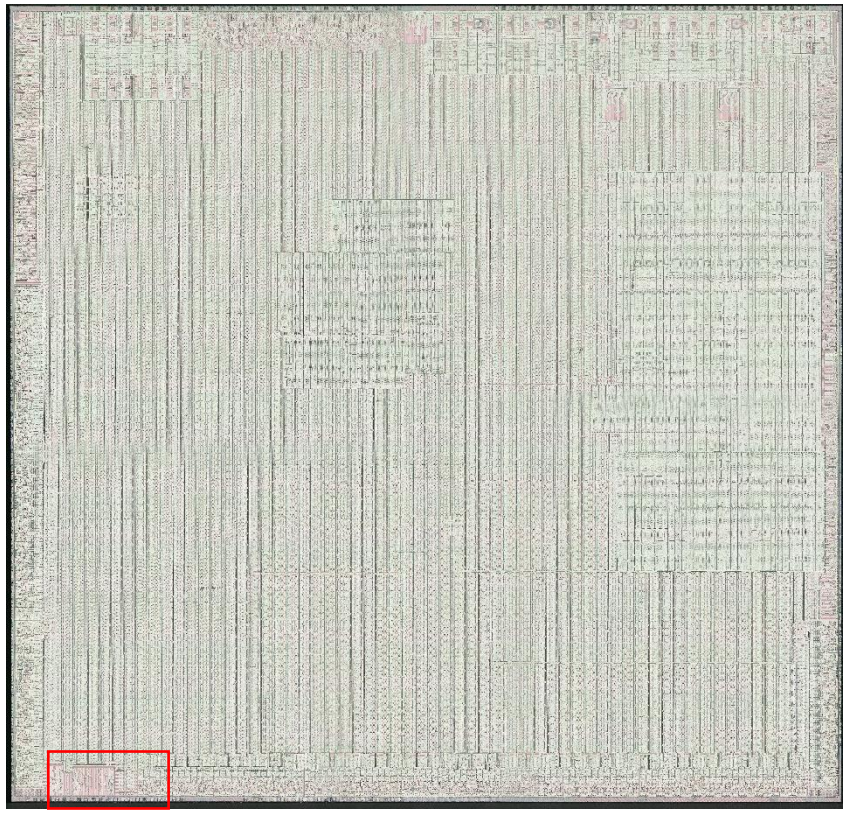


M1 SoC Die Backside

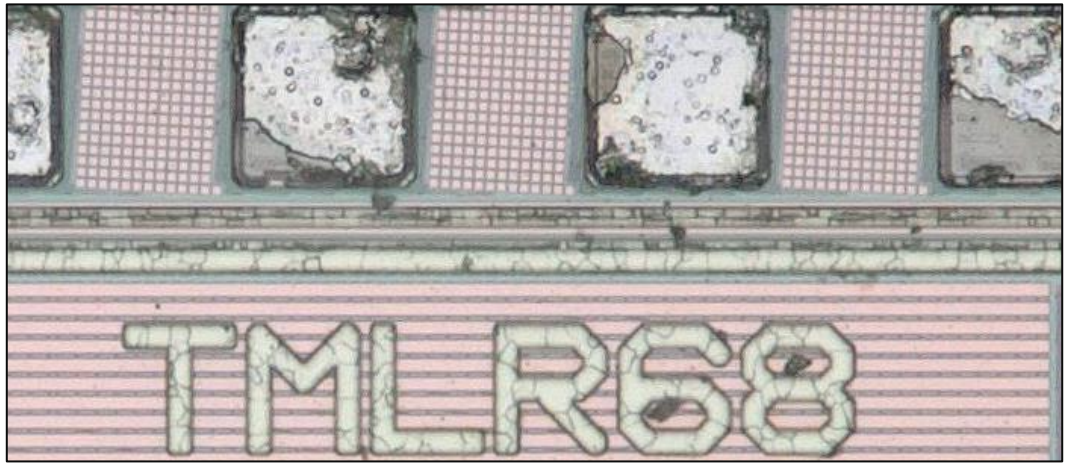


M1 SoC Die Frontside

M1 SoC Die Marking



M1 SoC Die View

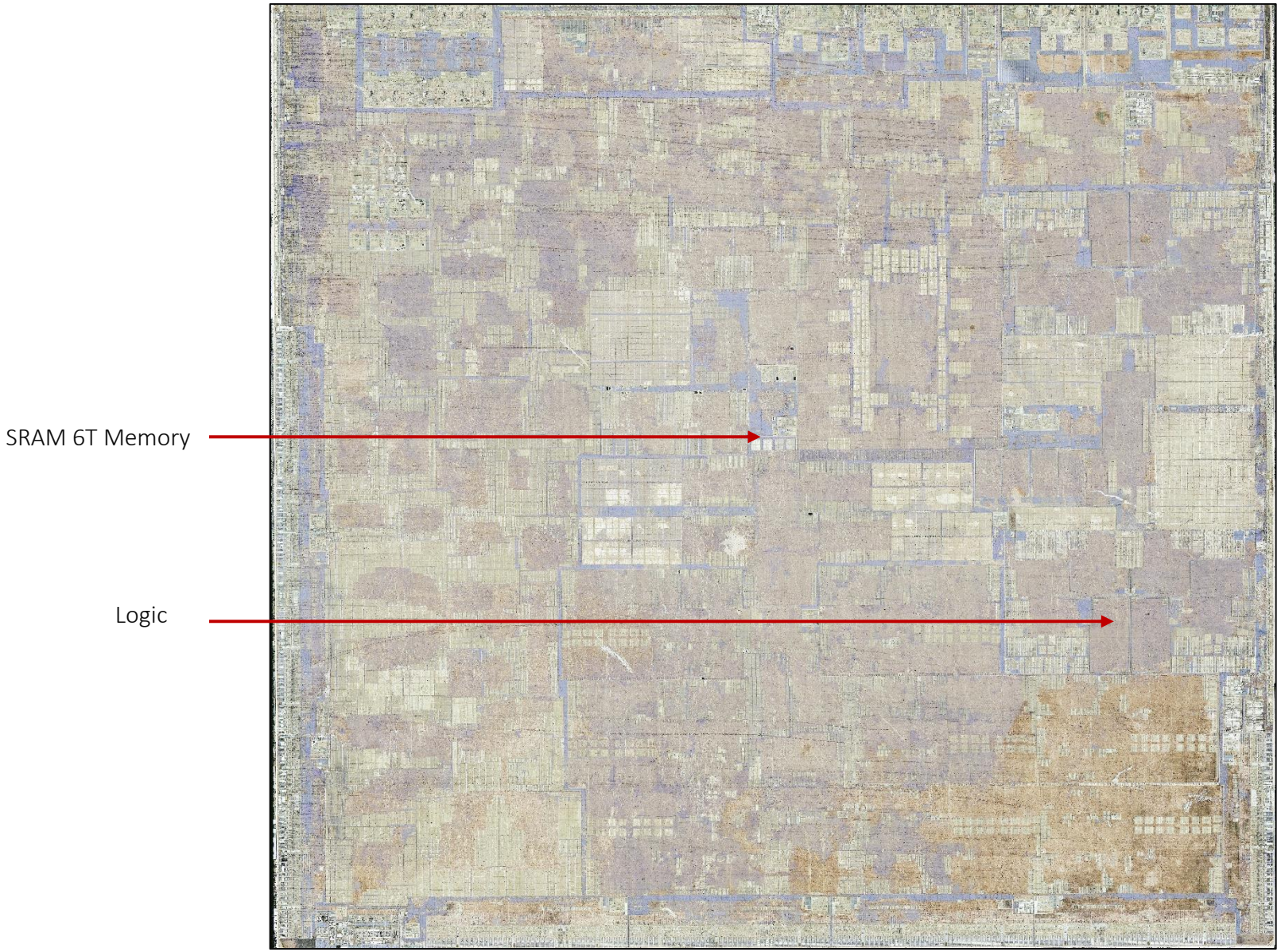


M1 SoC Die Marking

Die Marking

TMLR68 – Die Reference

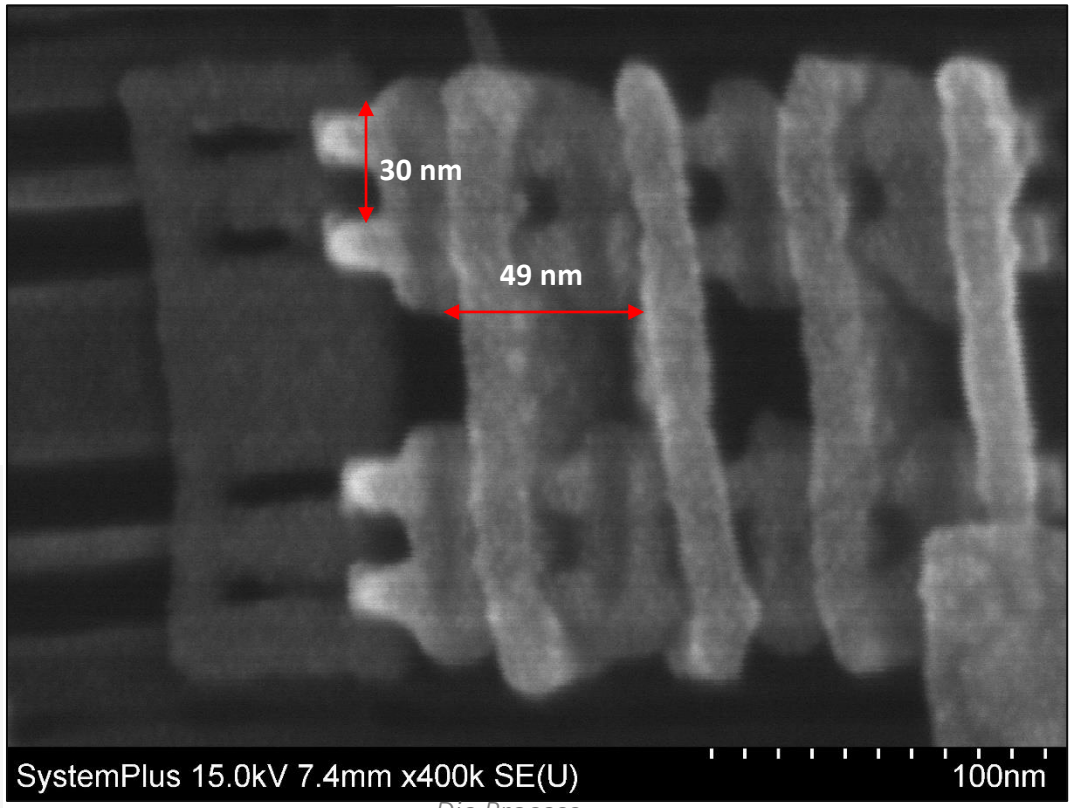
M1 SoC Die - Delayering



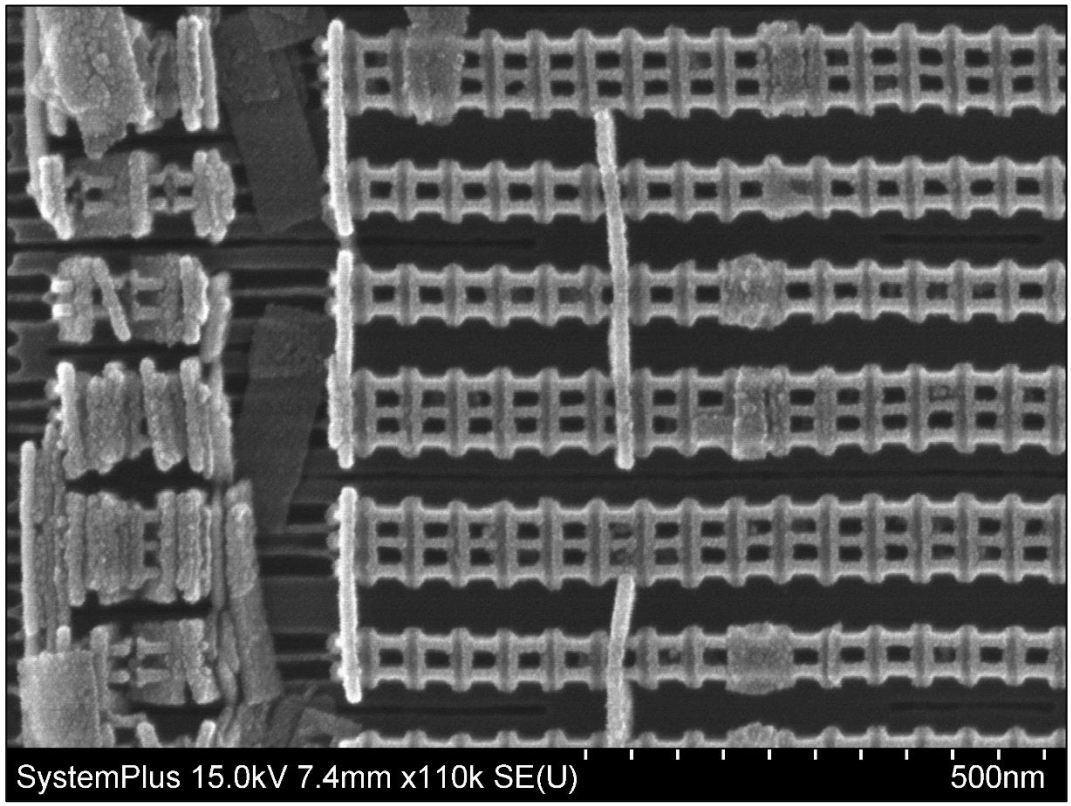
Die Overview after removing of the metal Layers

M1 SoC Die - Delayering

Die Delayering



Die Process



Die Process

The process uses FinFET transistors.

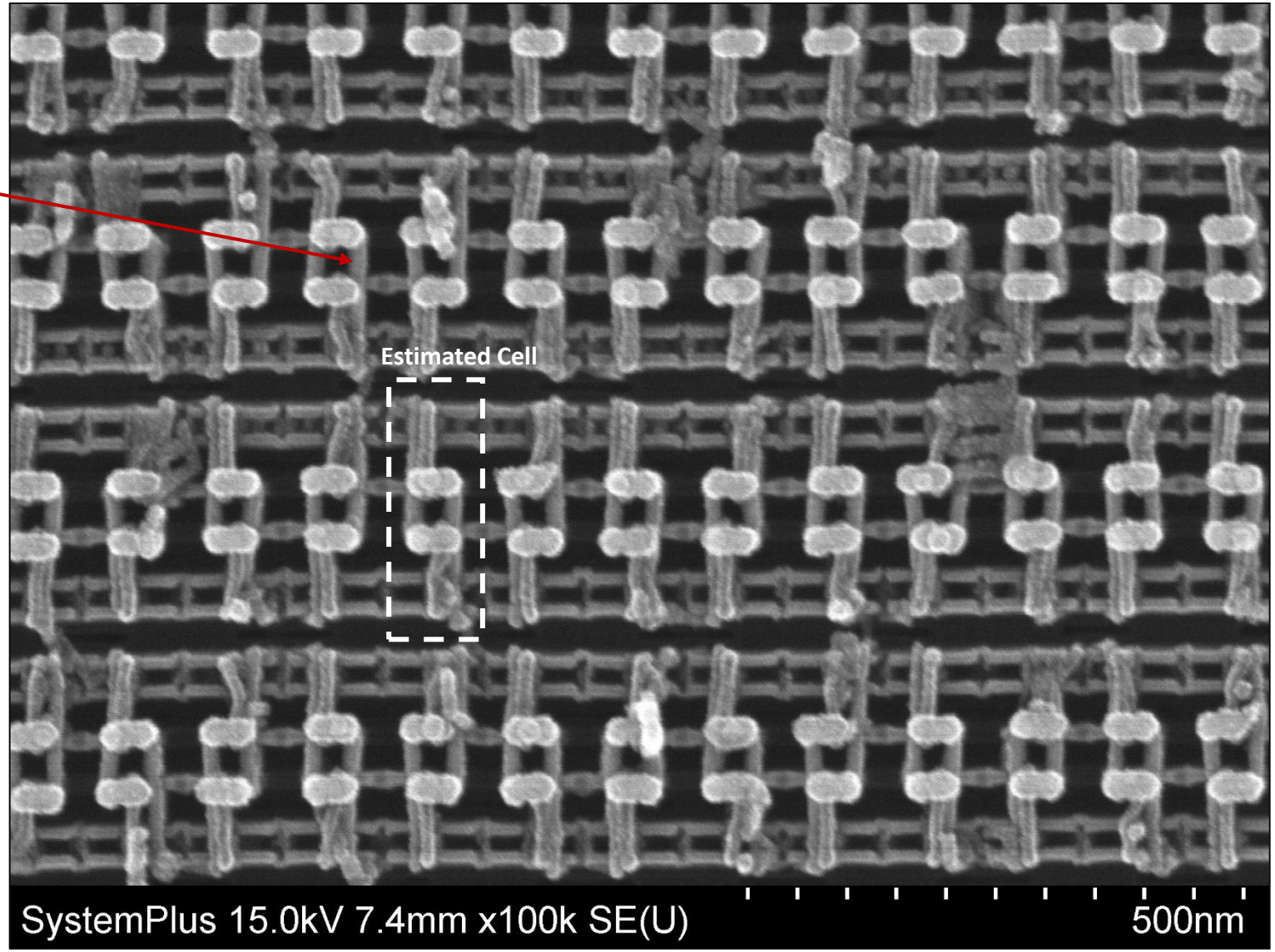
– FinFET Pitch : ~ 30 nm
– Gate Pitch : ~ 49 nm

• The gate pitch, FinFET pitch measurement, and the SRAM cell size let us think that the technology node is TSMC's 5 nm FinFET.

M1 SoC Die - Delayering

Die Delayering

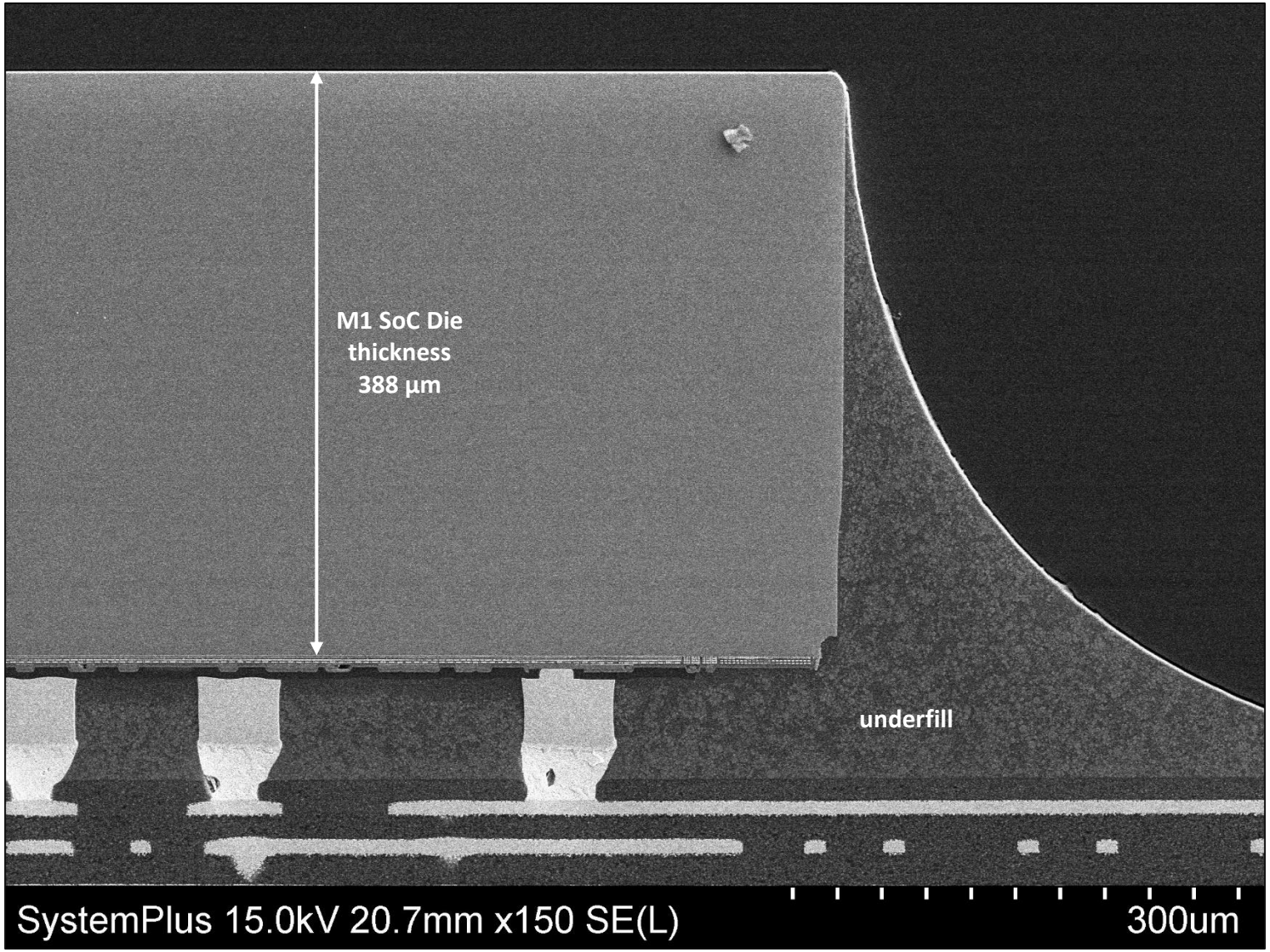
- Type: SRAM 6 transistors
- Cell size:
  - 0.019 µm²
    0.21 µm x 0.09 µm
  - This Corresponds to TSMC's 5 nm technology node.



Die Process – SRAM Memory

M1 SoC Die - Cross Section

- M1 Die thickness: 388 µm
- The M1 SoC Die is placed in flip chip position on the PCB substrate.

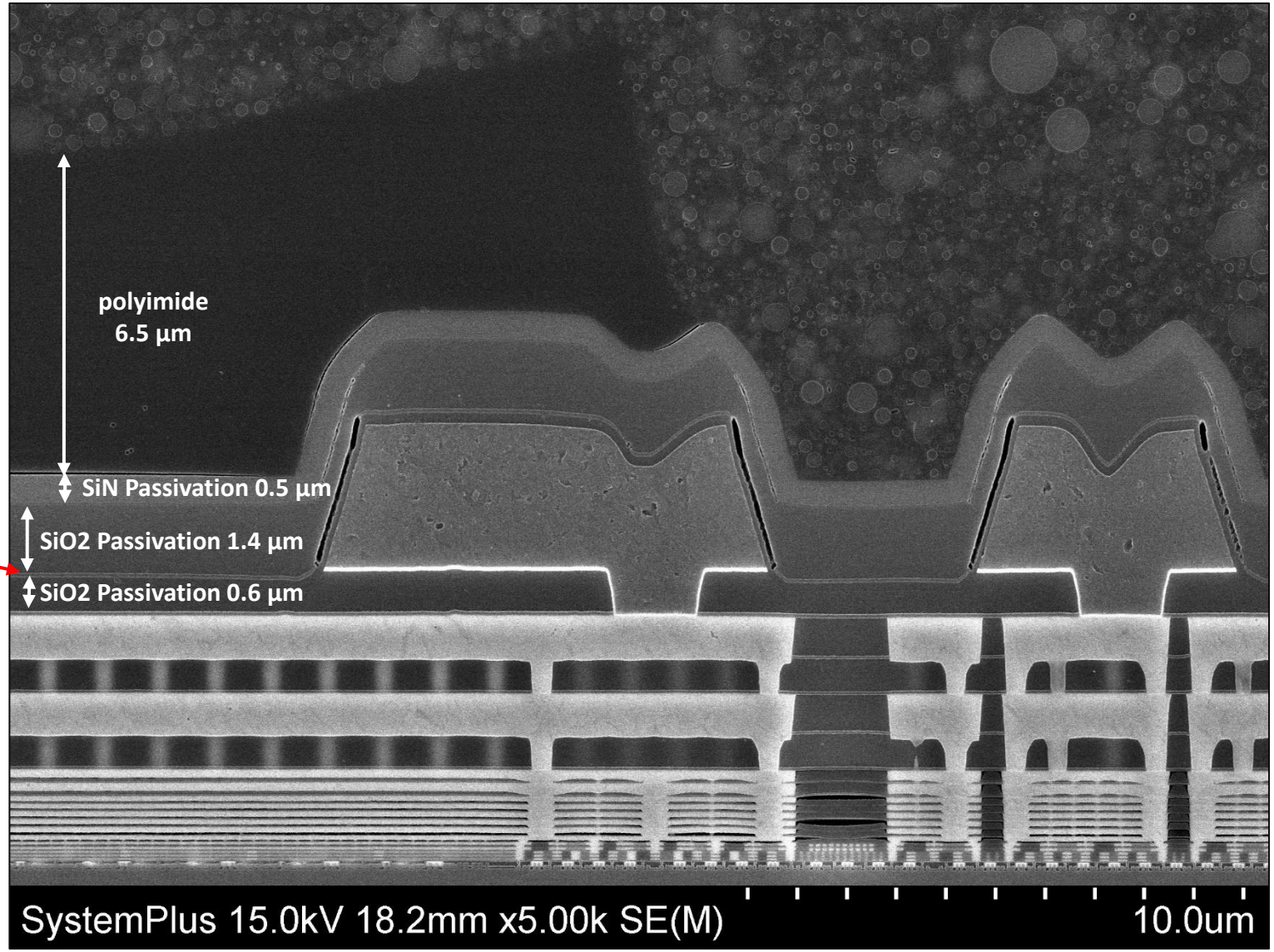


M1 SoC Die Cross Section

M1 SoC Die - Cross Section

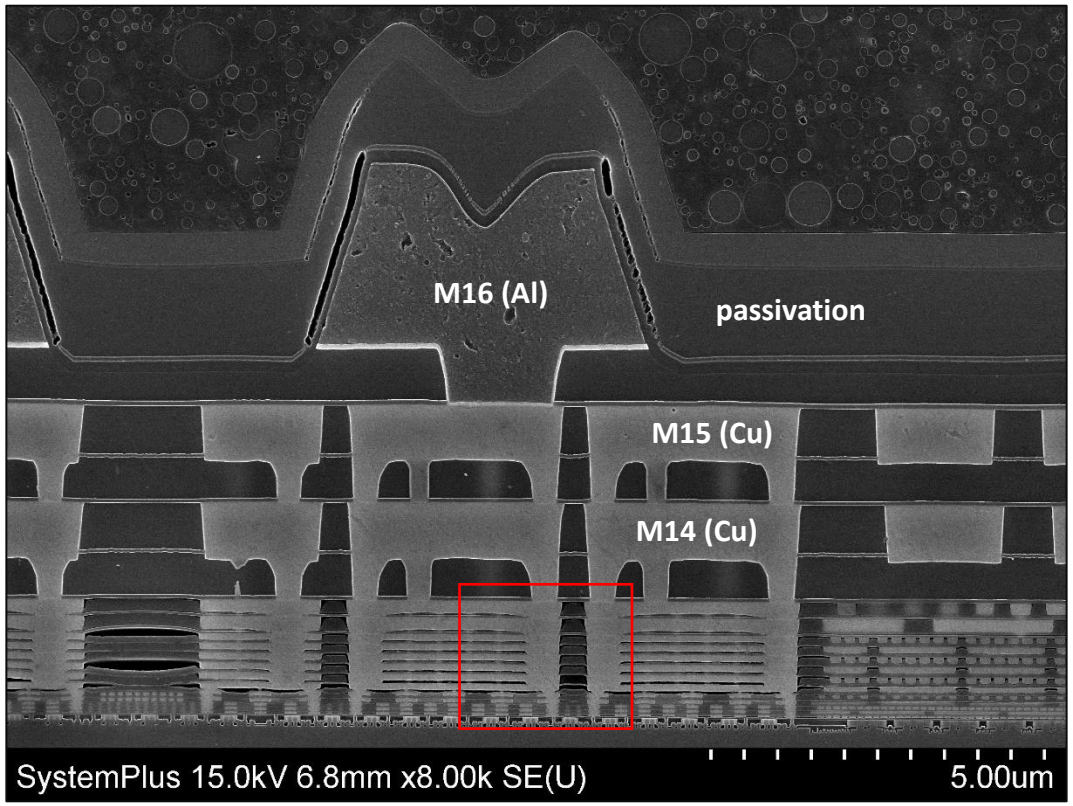
- A thin layer of SiN is deposited after the Al thick metal.
- The SiN layer could be deposited as an antireflective layer.
- A layer of polyimide is deposited on the M1 SoC Die.
- Polyimide thickness: 6.5 µm
- Thin layer of SiN thickness:

  70 nm



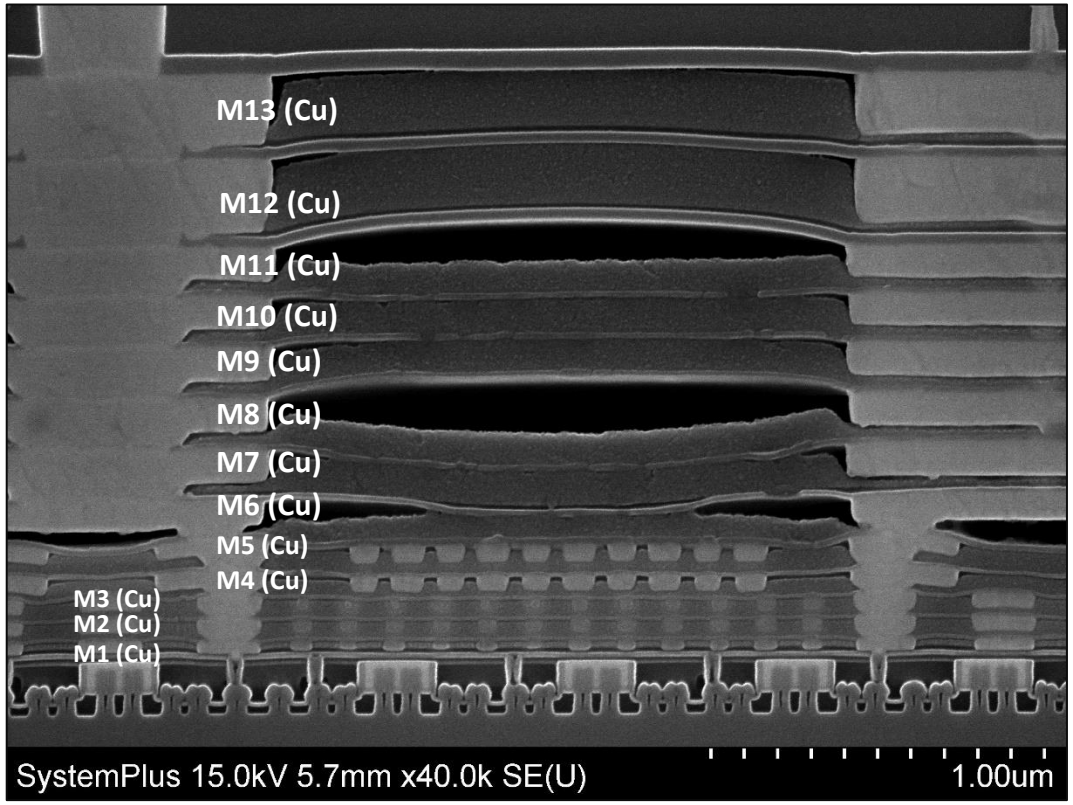
M1 SoC Die Cross Section

M1 SoC Die - Cross Section



M1 SoC Die Cross Section

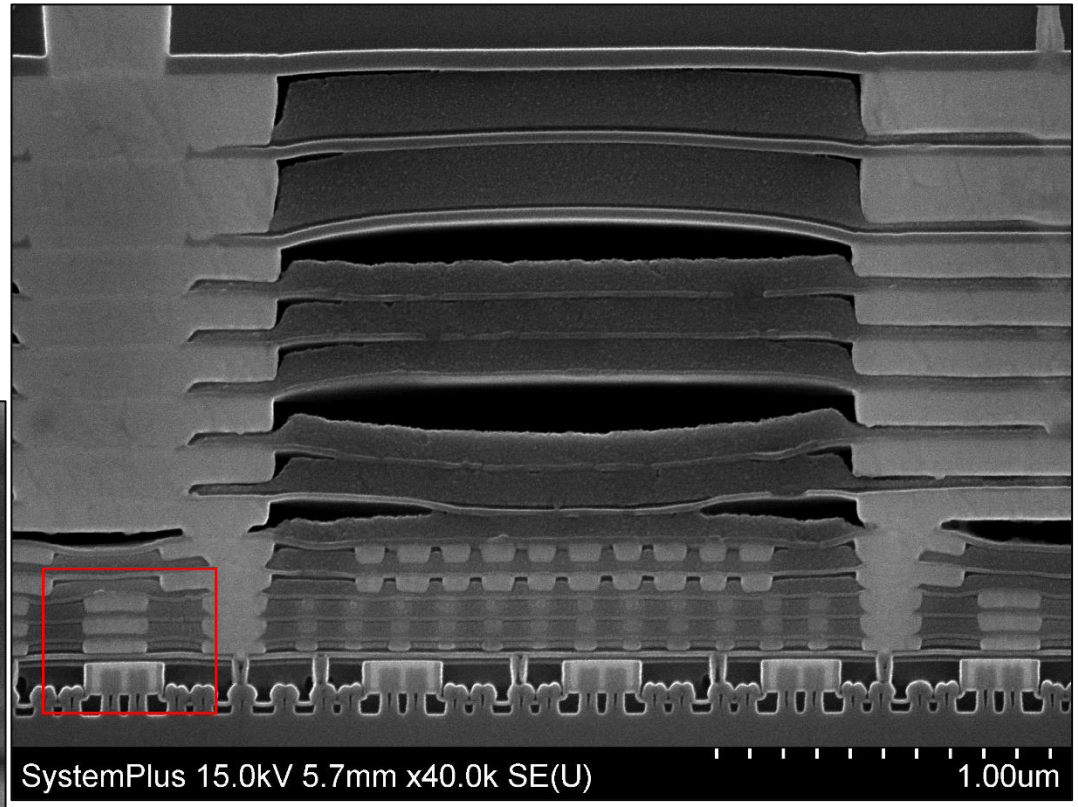
- The Processor Die uses 16 metal layers (15 Cu + 1 Al)



M1 SoC Die Cross Section

M1 SoC Die - Cross Section

- The die process uses FinFET Transistors.



M1 SoC Die Cross Section
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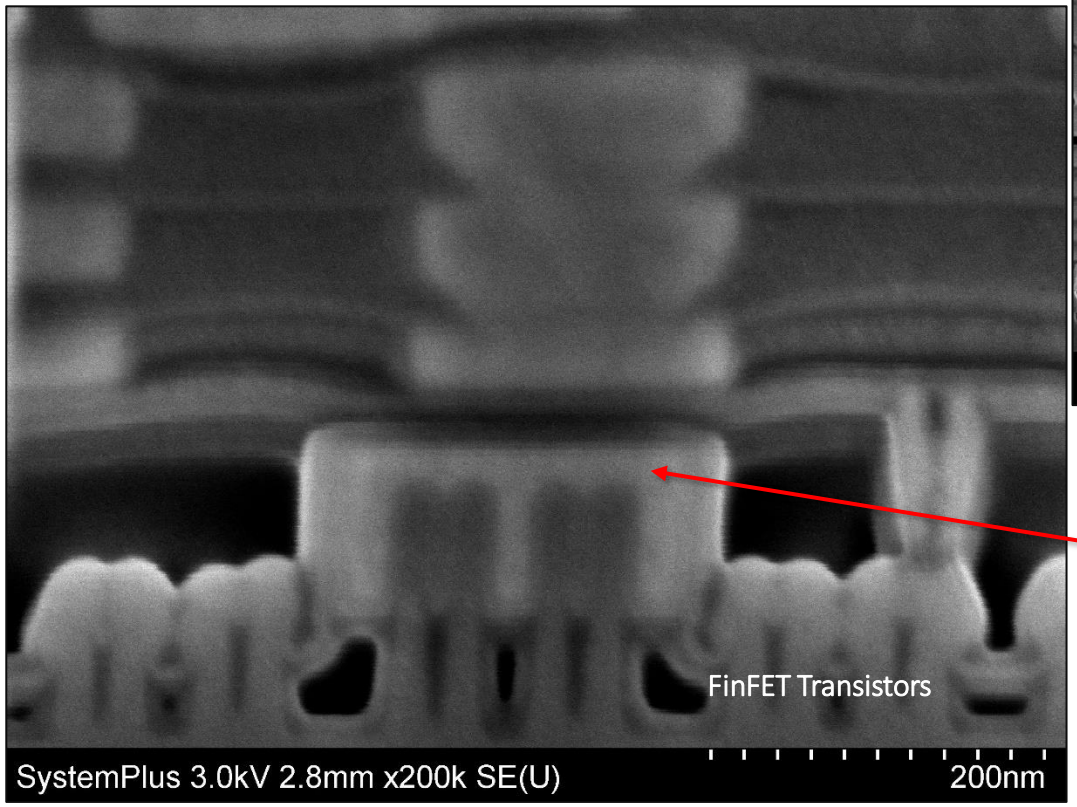
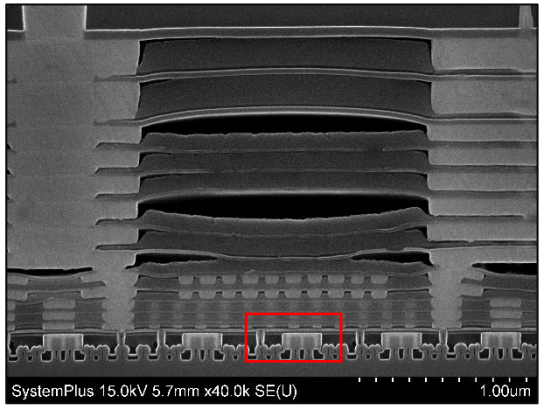


M1 SoC Die Cross Section- FinFET Transistors
©2020 by System Plus Consulting

TiN lined Co M0 local interconnect.
This is the SRAM cross-couple line.

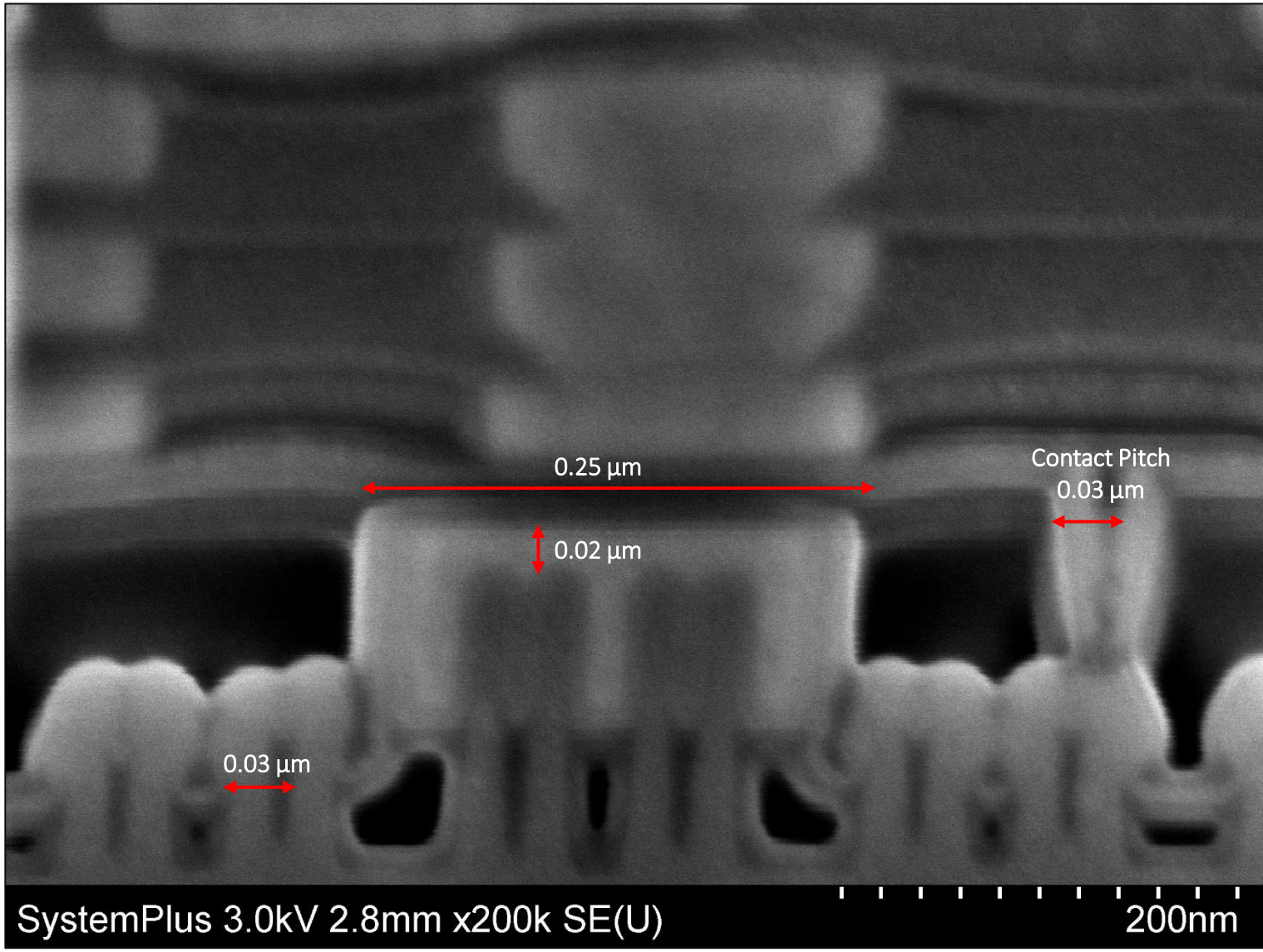
M1 SoC Die - Cross Section



M1 SoC Die Cross Section

- FinFET Pitch: 0.03 µm
- Contact Pitch: 0.03 µm

This corresponds to TSMC 5 nm FinFET Technology.



M1 SoC Die Cross Section- FinFET Transistors

F E O L
ANALYSIS

FEOL Analysis – Summary

The front end of line (FEOL) analysis of the Apple M1 is intended to provide insight into the high mobility channel (HMC) process employed by TSMC to manufacture the 5 nm generation products. The switch to HMC for PMOS devices is necessary to provide target performance for 5 nm which pure silicon is unable to provide.

The analysis provided herein is based on vertical cross-sections in a region of SRAM L2 cache memory (6T cell). Cross-sections both along and across the fins provided sufficient detail to understand the newest advanced logic semiconductor technology commercially available. The TSMC 5 nm process was first mass produced for the Apple A14 mobile application processor for iPhone a few weeks before the launch of the Apple M1 personal computer processor, the second mass produced 5 nm product.

After the formation of silicon fins, the NMOS area is protected while the PMOS fins are etched back. A selective epitaxy then grows SiGe onto the PMOS fins at a concentration of 30% Ge. This layer is maintained for approximately 17 nm after which the Ge content is reduced to 25%.

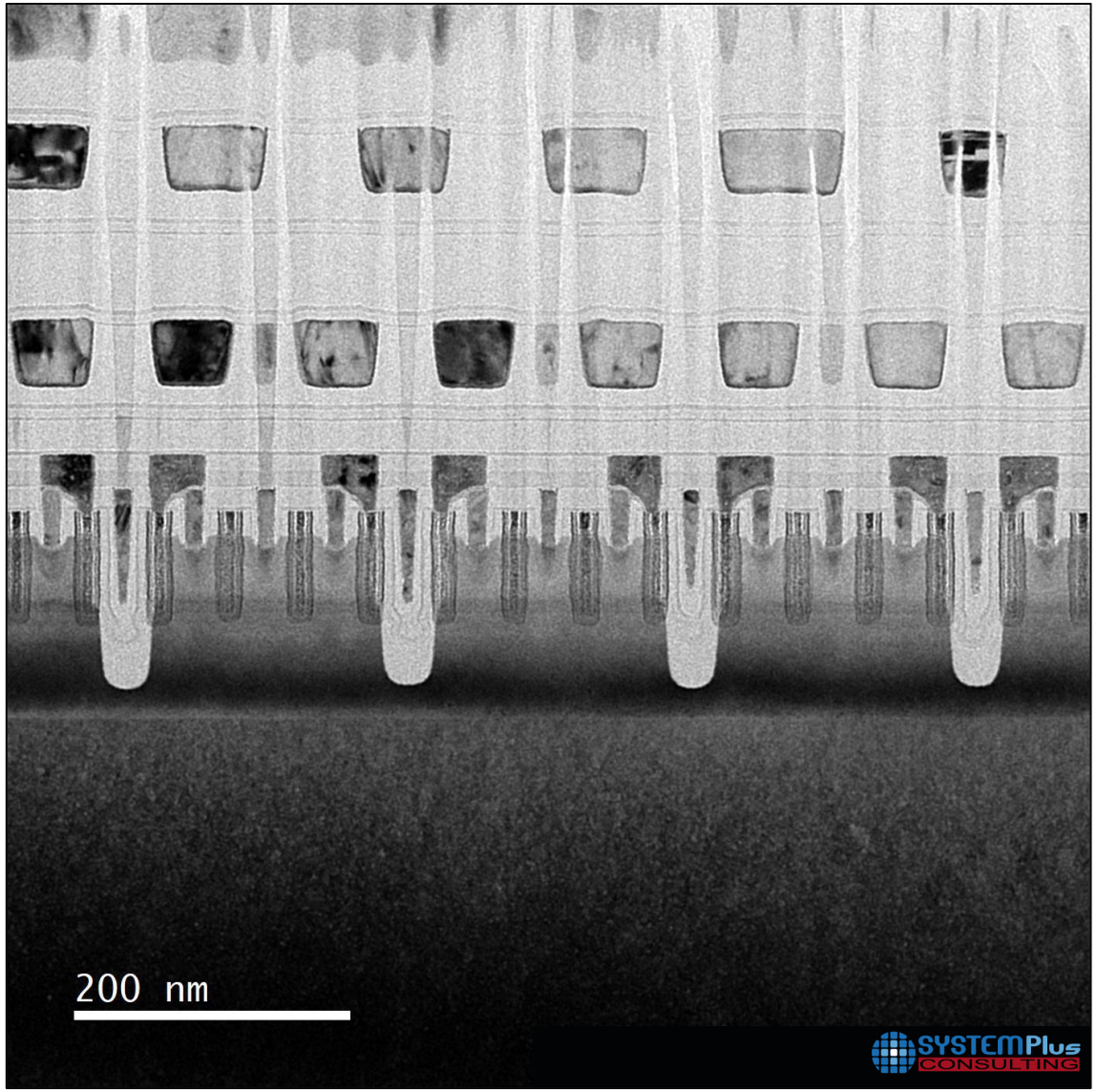
The source / drain regions of both NMOS and PMOS finFETS are engineered to provide the channel strain to increase hole or electron mobility as appropriate for each device polarity. In the case of the PMOS transistor, an additional e-SiGe with Ge 40% is formed to create the compressive channel strain to increase hole mobility and the interface for the metal contacts. In the NMOS source / drain, P is added since the atom is smaller than Si. This e-SiP S/D creates tensile strain in the NMOS channel thereby increasing electron mobility to enhance the NMOS finFET performance.

Other notable features in the front end are related to the contact materials. A similar TiN liner plus Co trench fill material stack is used both for the vertical contacts to S/D regions and the contacts to gates. This second level is also used for local interconnect such as the NMOS to PMOS cross-couple for the SRAM cell.

The following pages detail the methods used and the supporting TEM images and EDS data.

FEOL Analysis – TEM Along PMOS Fin

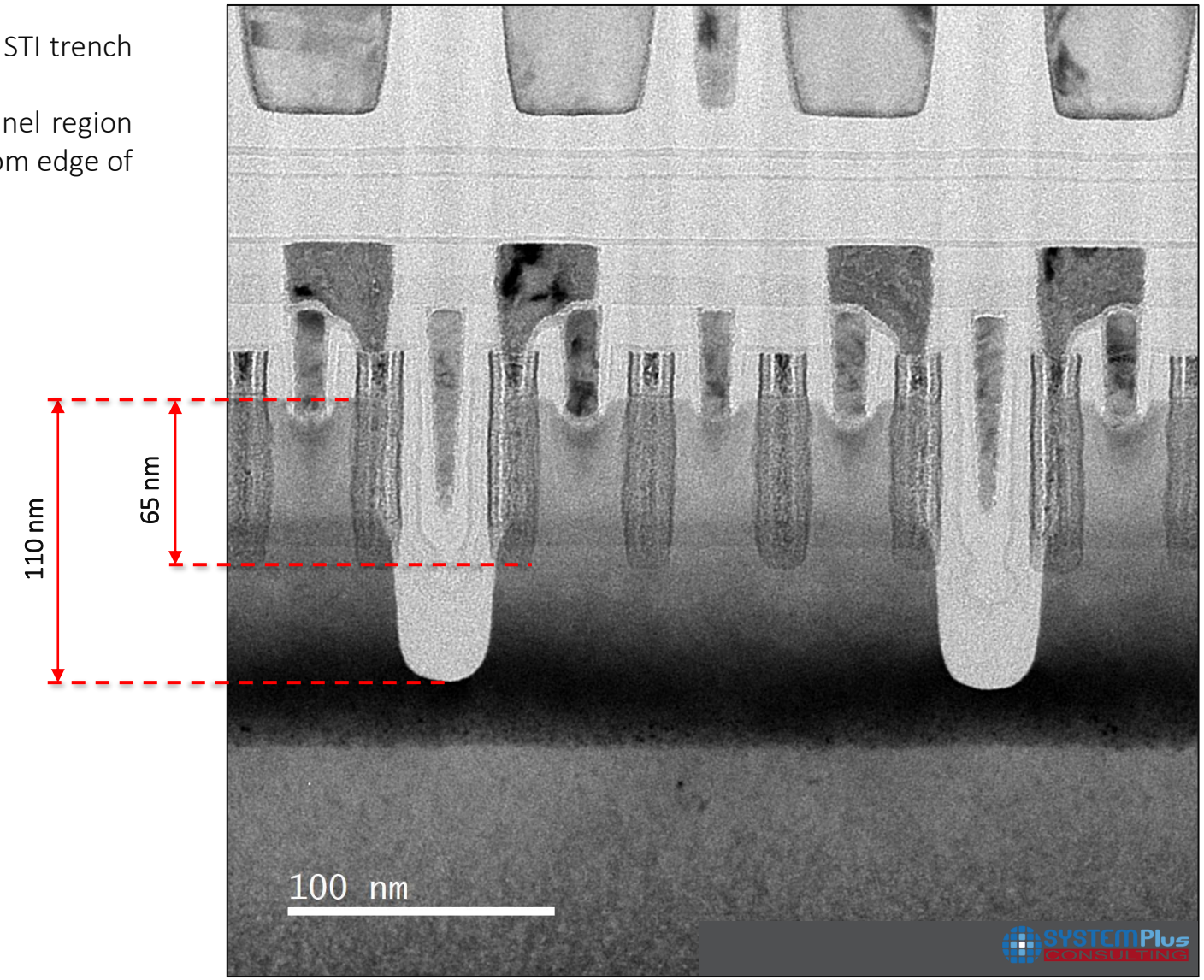
- The FEOL analysis focused on an L2 cache SRAM from the Apple M1 SoC.
- The main metallization is typical copper (Cu) damascene.
- Both vertical contact and local interconnect are comprised of a main cobalt (Co) fill with a titanium nitride (TiN) liner.



Cross-section Along PMOS FinFET in SRAM Cache (1) – Bright Field TEM Image

FEOL Analysis – TEM Along PMOS Fin

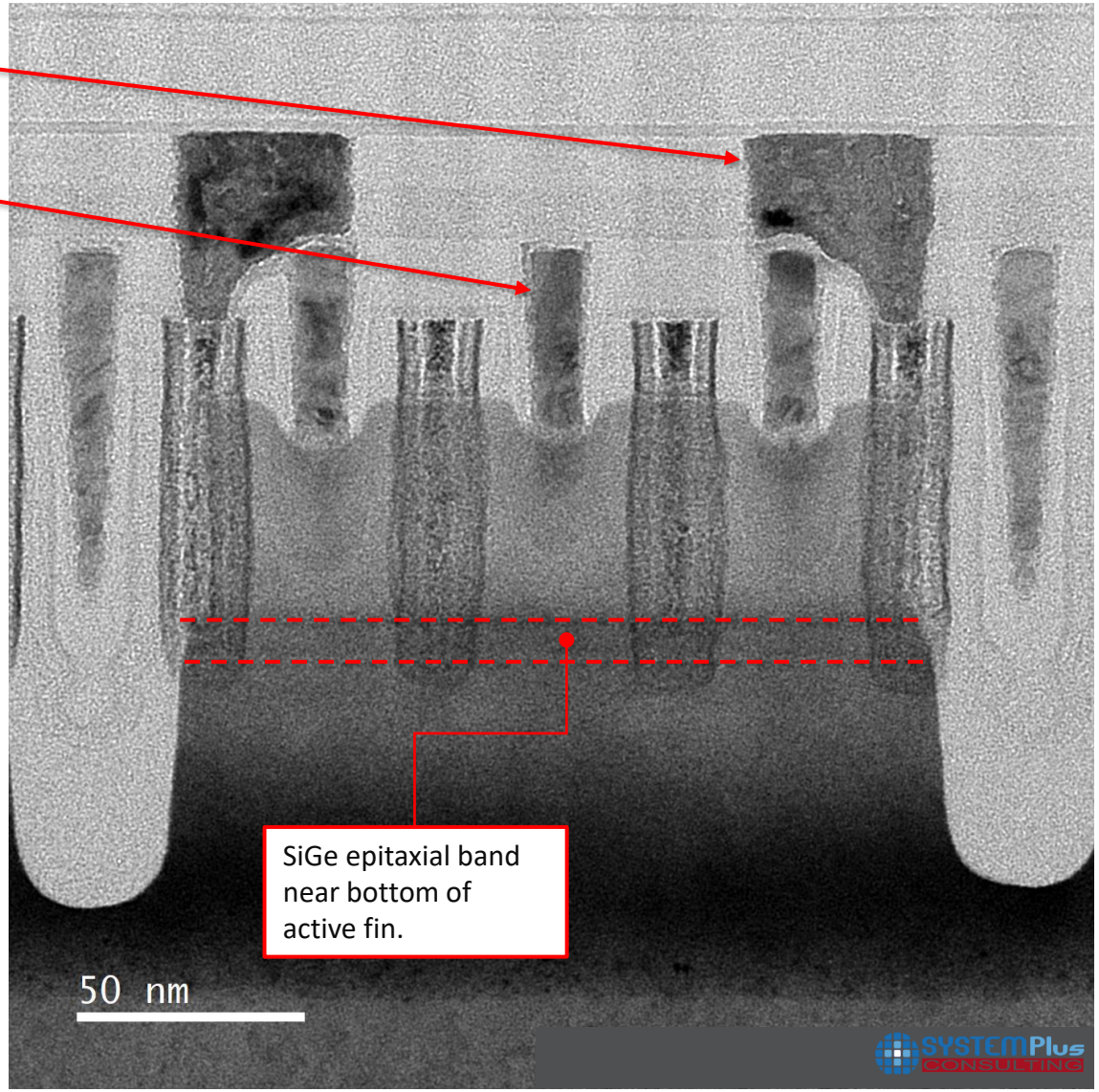
- PMOS fin height from the base of the STI trench is 110 nm in the SRAM.
- The vertical height of the active channel region of the PMOS finFET (top of fin to bottom edge of gate) is 65 nm.



*Cross-section Along PMOS FinFET in SRAM Cache (2) – **Bright Field** TEM Image*

FEOL Analysis – TEM Along PMOS Fin

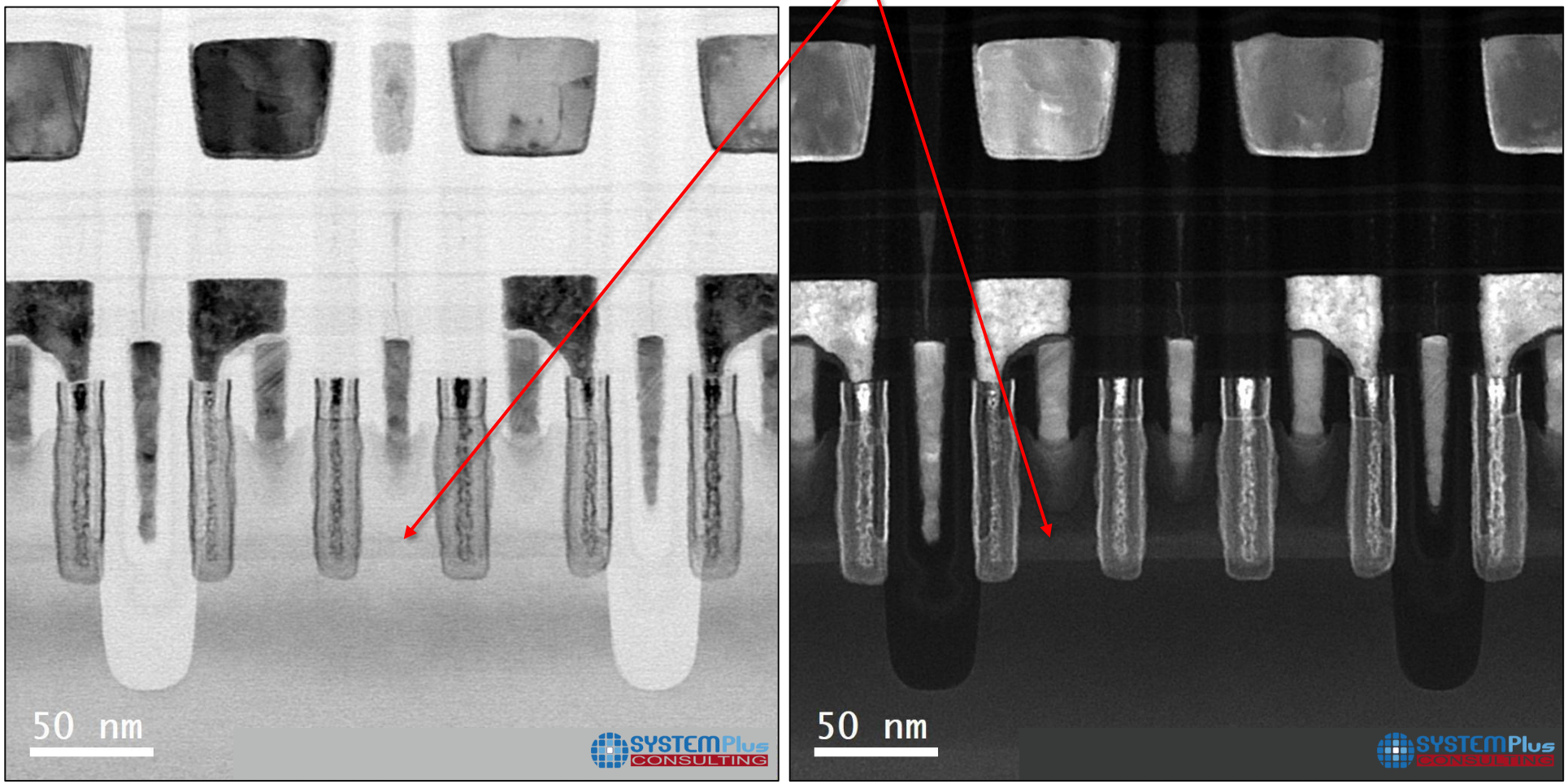
- The engineered high mobility channel (HMC) employed in the PMOS finFET of the TSMC 5 nm process is indicated by the darker band of contrast in the bright field (BF) TEM image at right.
- This darker band is a region of epitaxial silicon-germanium (SiGe) material.
- Its position on the fin is near the bottom of the active channel where the metal gates overlap it but do not extend much beyond it.
- The SiGe layer is approximately 17 nm thick and begins 46 nm below the top of the fin.



*Cross-section Along PMOS FinFET in SRAM Cache (3) – **Bright Field** TEM Image*

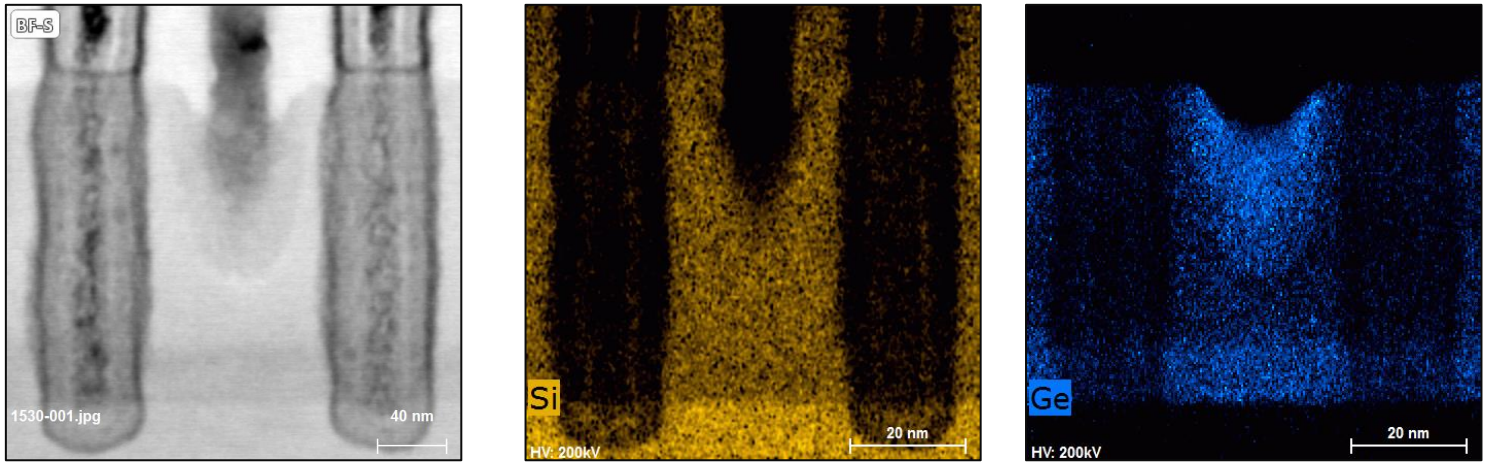
FEOL Analysis – TEM Along PMOS Fin

A higher concentration Ge portion of the SiGe high mobility channel fin is evident in the image contrast indicating a band of different material near the lower reaches of the finFET gate (darker band in BF, lighter band in ZC).

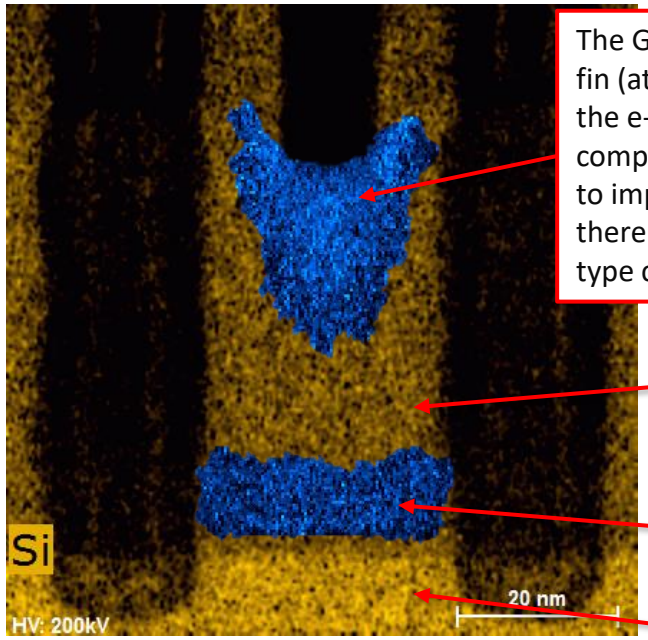


*Cross-section Along PMOS FinFET in SRAM Cache – TEM **Bright Field Image (left)** Zero Contrast (ZC) **Image (Right)***

FEOL Analysis – TEM Along PMOS Fin



Detail of PMOS FinFET with EDS Materials Analysis of the Fin Composition by 2D Mapping of the Characteristic X-rays



Composite 2D EDS Map Showing Ge Areas in Blue over Si in Orange

The Ge signal near the top of the fin (at base of metal contact) is the e-SiGe S/D creating compressive strain in the channel to improve hole mobility and thereby performance of the p-type channel.

Upper portions of the active fin channel appear to have lower concentration of Ge.

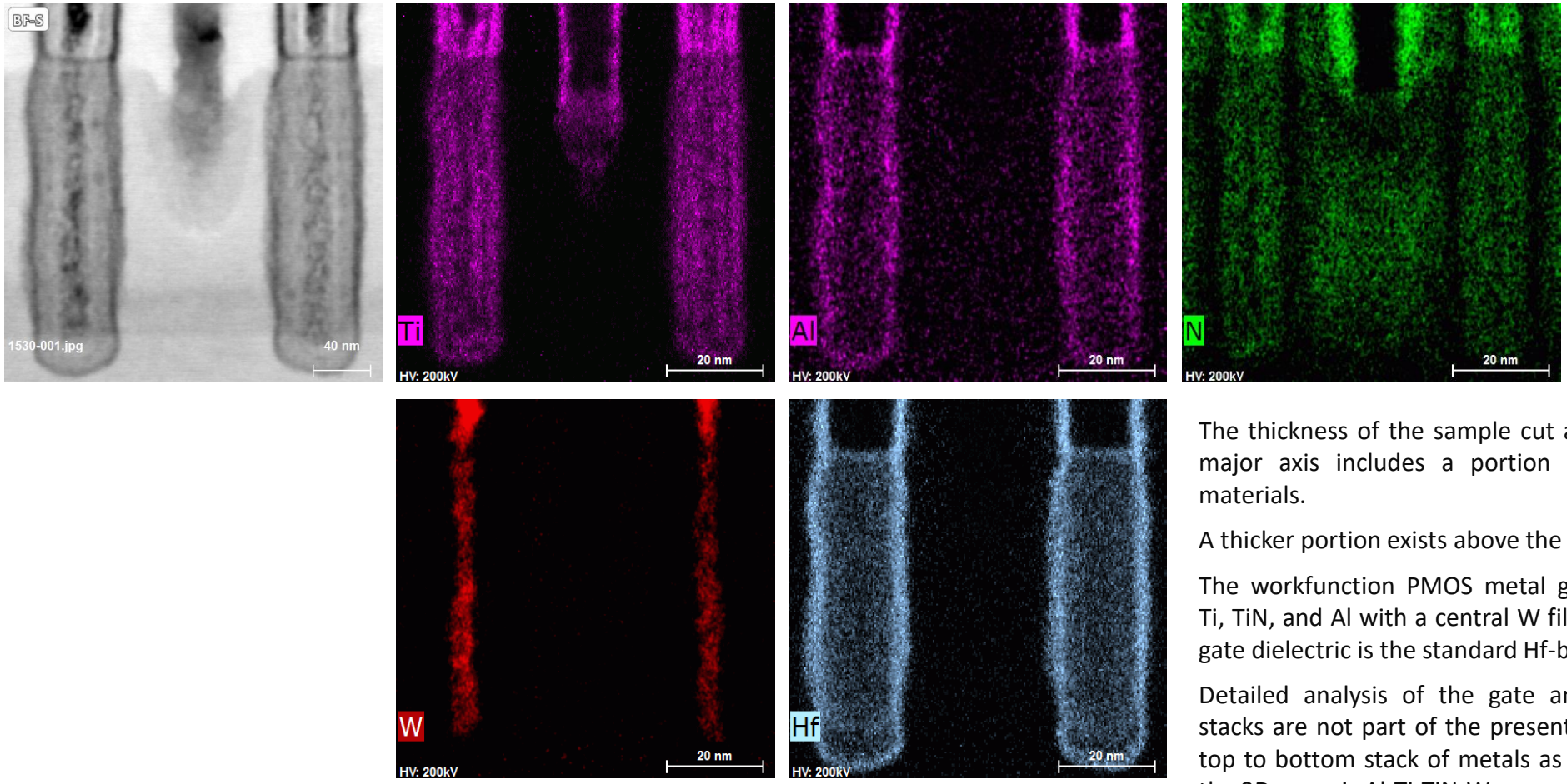
Epitaxial SiGe band in lower region of active fin channel

The base of the fin is silicon.

- An epitaxial SiGe portion of the high mobility channel (HMC) fin is clear in the 2D EDS mapping with a strong signal in the lower fin region.
- The Ge signal is reduced above this lower band suggesting that the high mobility channel engineering is targeted to the lower portion of the fin where the electrostatics of the gate are influencing the channel on only two sides as opposed to near the top of the fins where the gate wraps around and can invert the channel on three sides.

The presumed process is:
- Fin definition (global, N- and P-channels)
- Protect NMOS area, etch back PMOS fins
- Selective epitaxial growth of SiGe for HMC
- Continue epitaxy to complete fin (reduced Ge concentration)
- Embedded SiGe source / drain (S/D) formation for channel strain engineering

FEOL Analysis – TEM Along PMOS Fin



Detail of PMOS FinFET with EDS Materials Analysis of the Gate and Gate Dielectric Composition by 2D Mapping of the Characteristic X-rays

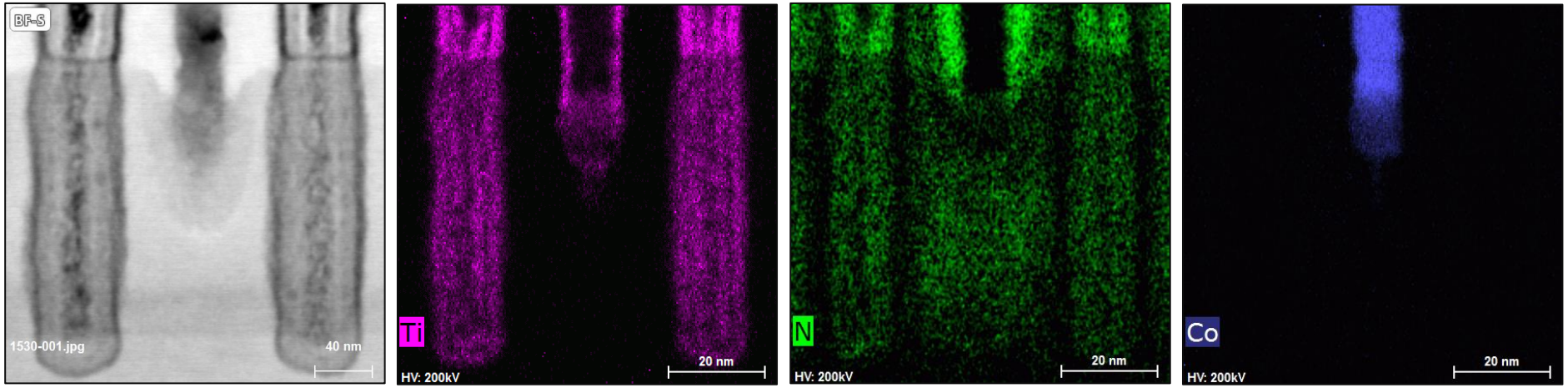
The thickness of the sample cut along the fin major axis includes a portion of the gate materials.

A thicker portion exists above the fin.

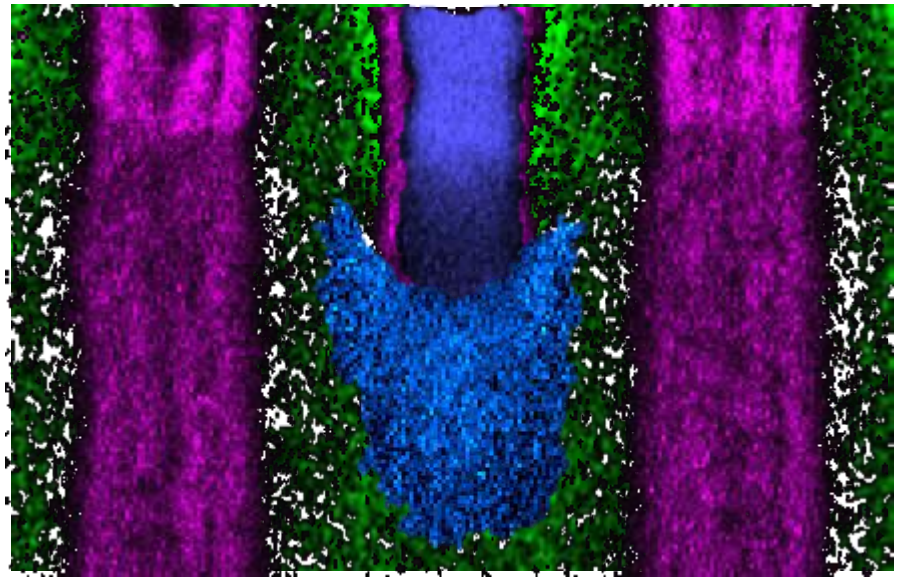
The workfunction PMOS metal gate includes Ti, TiN, and Al with a central W fill. The high-K gate dielectric is the standard Hf-based oxide.

Detailed analysis of the gate and dielectric stacks are not part of the present report. The top to bottom stack of metals as indicated by the 2D maps is Al-Ti-TiN-W.

FEOL Analysis – TEM Along PMOS Fin



Detail of PMOS FinFET with EDS Materials Analysis of the S/D Contact Metals by 2D Mapping of the Characteristic X-rays

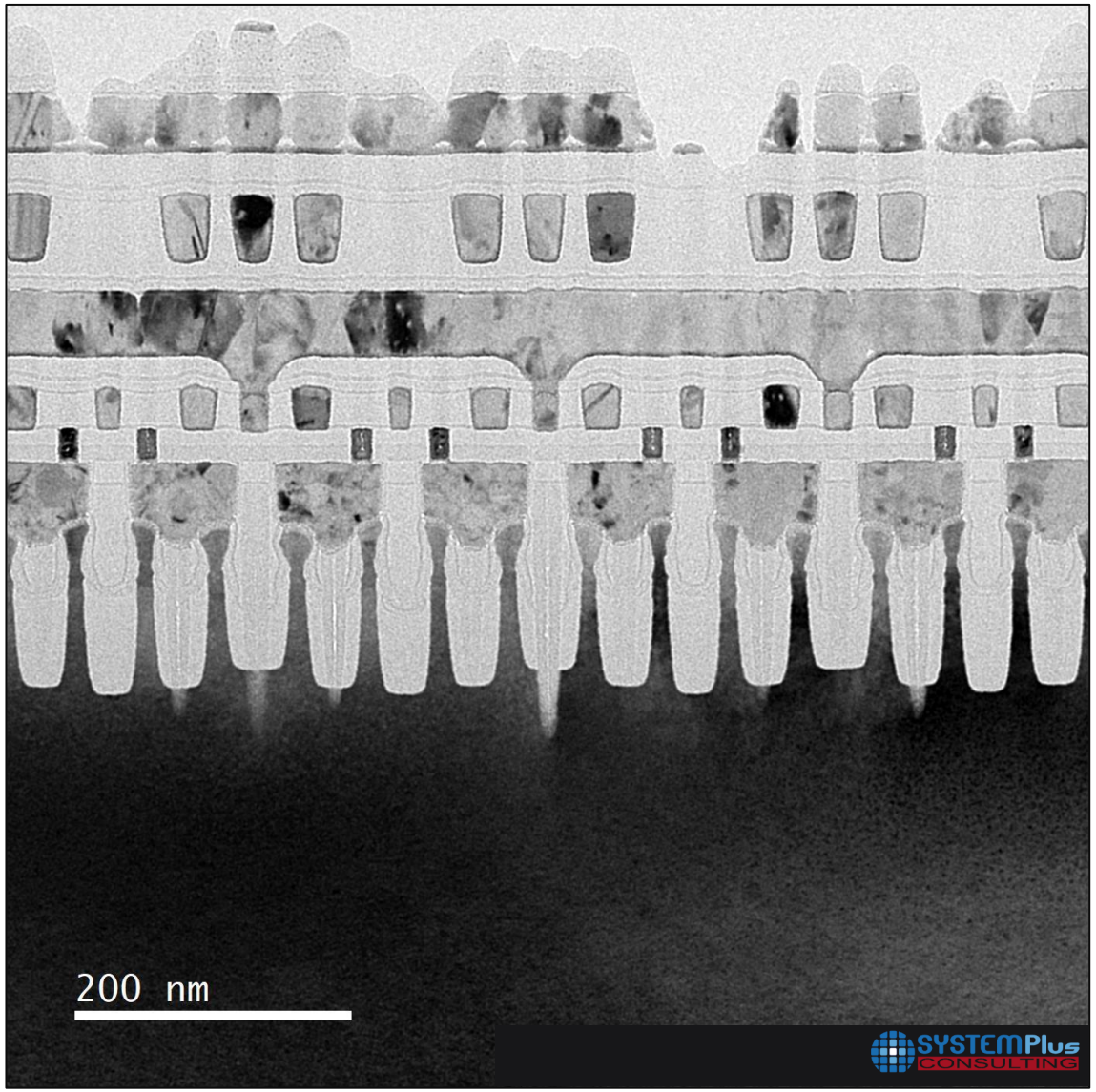


Composite 2D EDS Map Showing Contact to e-SiGe S/D

- Vertical contacts to S/D regions are formed in the contact holes with a TiN liner followed by a Co plug fill.

FEOL Analysis – TEM Across Fins

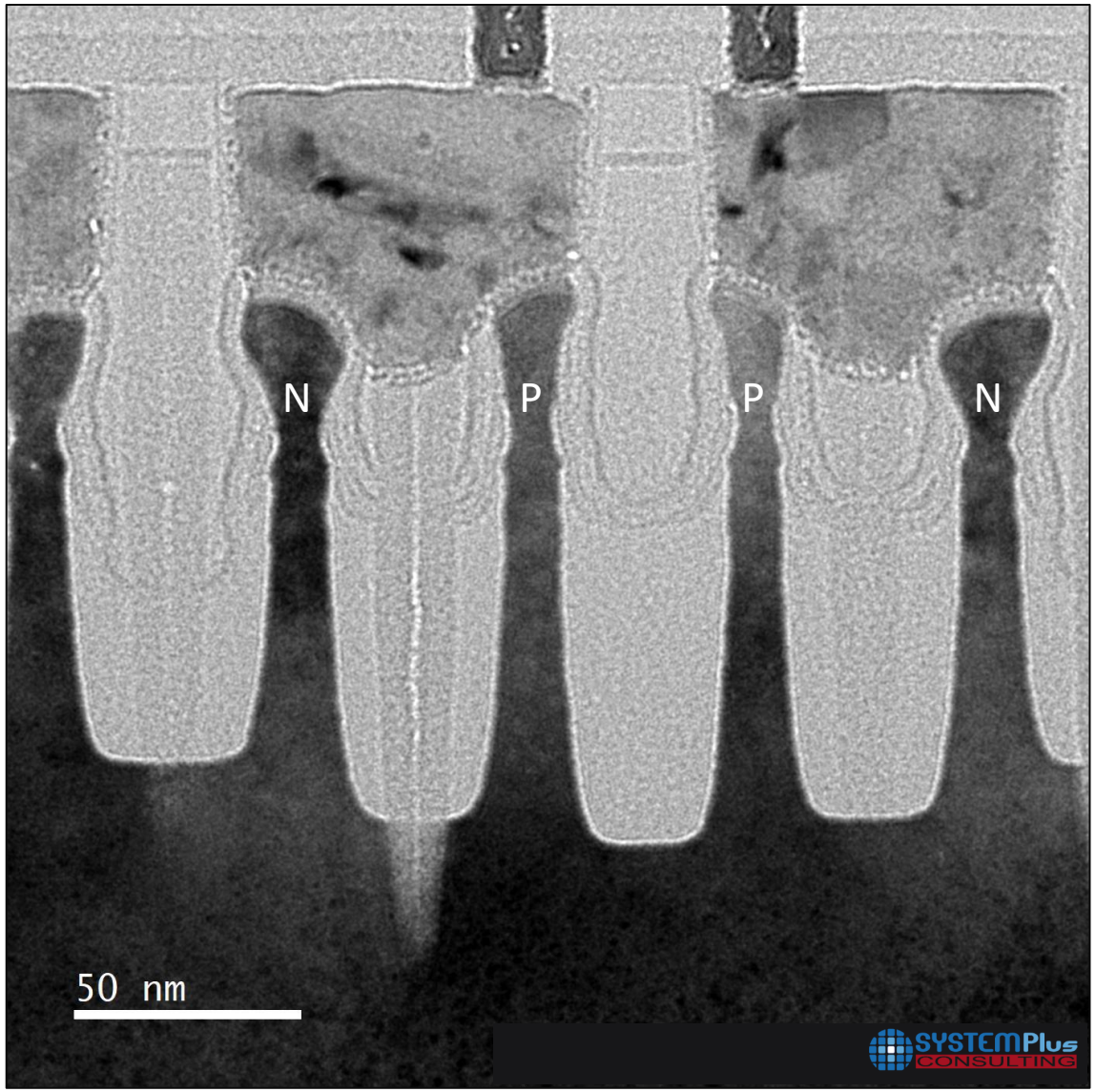
- The cross-section plane across fins in the SRAM reveals a series of NMOS and PMOS finFETs.



Cross-section Across Fins in SRAM Cache (1) – Bright Field TEM Image

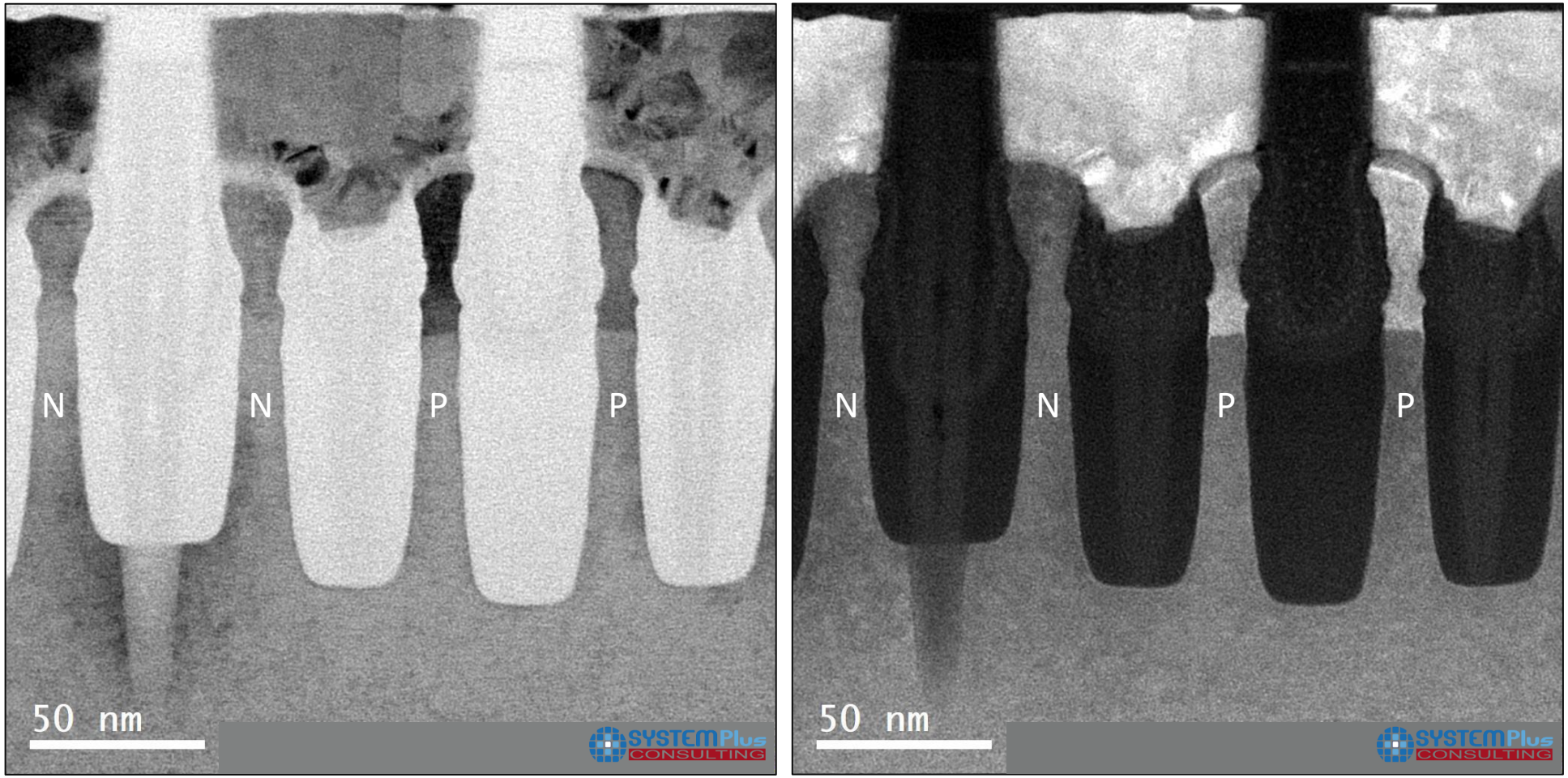
FEOL Analysis – TEM Across Fins

- The distinct shapes for each channel type are indicative of the embedded source / drain materials used to optimize channel strain for carrier mobility enhancement to improve transistor performance.



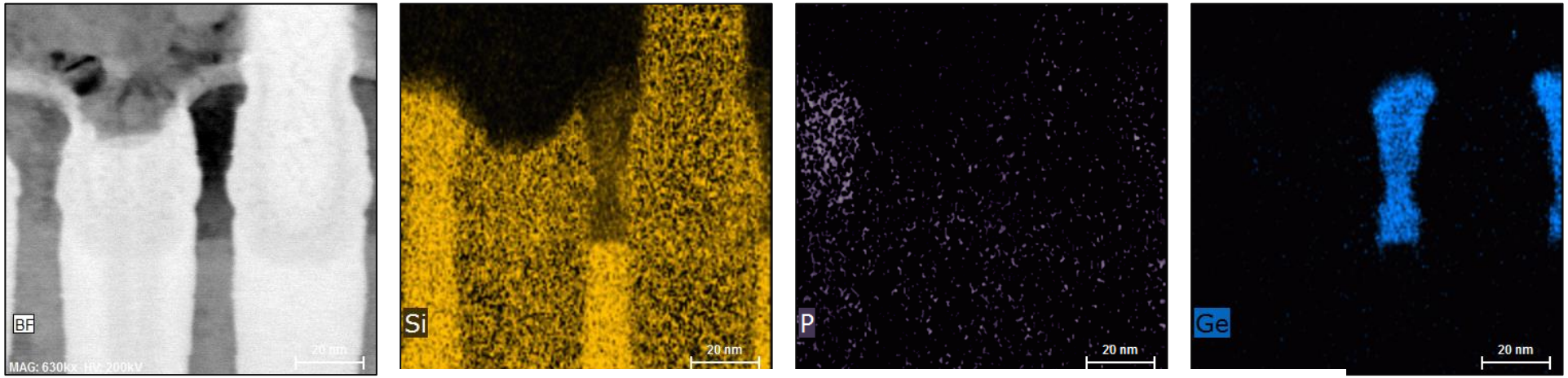
Cross-section Across Fins in SRAM Cache (2) – Bright Field TEM Image

FEOL Analysis – TEM Across Fins

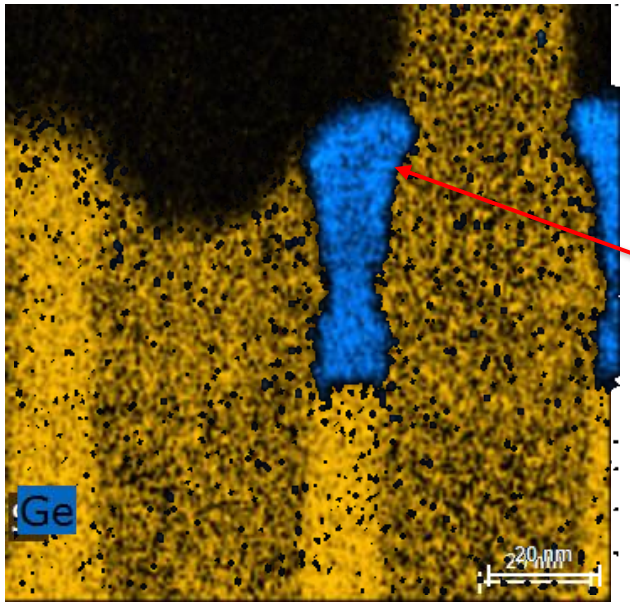


*Cross-section Across Fins in SRAM Cache – TEM **Bright Field Image (left) Zero Contrast (ZC) Image (Right)***

FEOL Analysis – TEM Across Fins



Detail of NMOS FinFET (left) and PMOS FinFET (right) with EDS Materials Analysis of the Fin Composition by 2D Mapping of the Characteristic X-rays



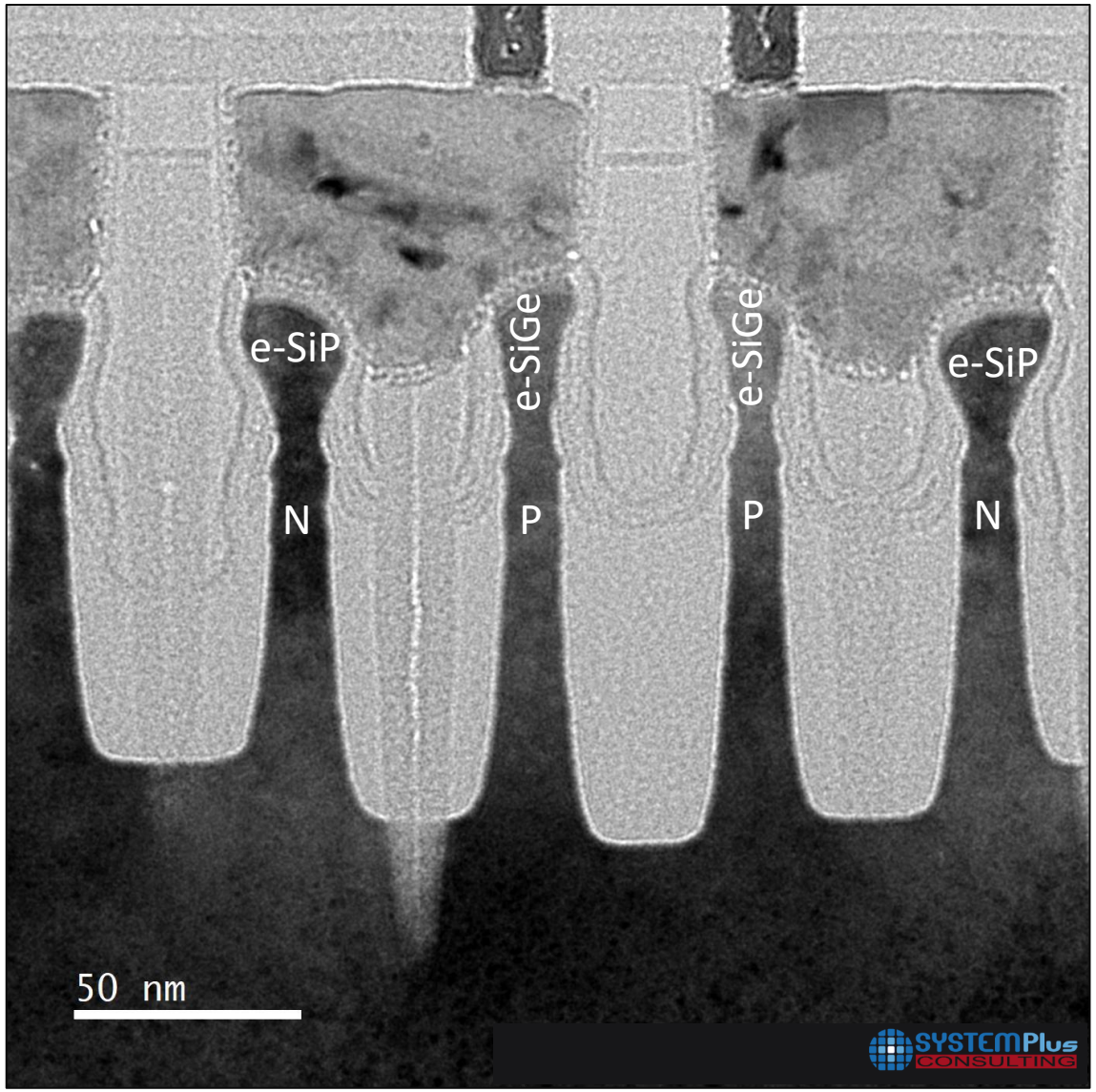
Composite 2D EDS Map Showing Ge Areas in Blue over Si in Orange

The Ge characteristic energy x-ray signal near the top of the fin (at base of metal contact) is the e-SiGe S/D creating compressive strain in the channel to improve hole mobility and thereby performance of the p-type channel. The lower portion represents the HMC.

- An epitaxial SiGe portion of the high mobility channel (HMC) fin is clear in the 2D EDS mapping with a strong signal in the fin region below the e-SiGe S/D.
- The phosphorous (P) signal near the top of the NMOS finFET indicates an e-SiP S/D for the n-channel devices.

FEOL Analysis – TEM Across Fins

- The smaller P atom in the e-SiP S/D creates tensile strain in NMOS finFET channels to improve electron mobility.
- The larger Ge atom in the e-SiGe S/D compresses the PMOS finFET channel to increase the hole mobility.
- This is a secondary effect for PMOS as the channel mobility is directly improved by the use of SiGe in the active channel portion of the fins.



Cross-section Across Fins in SRAM Cache (2) – Bright Field TEM Image

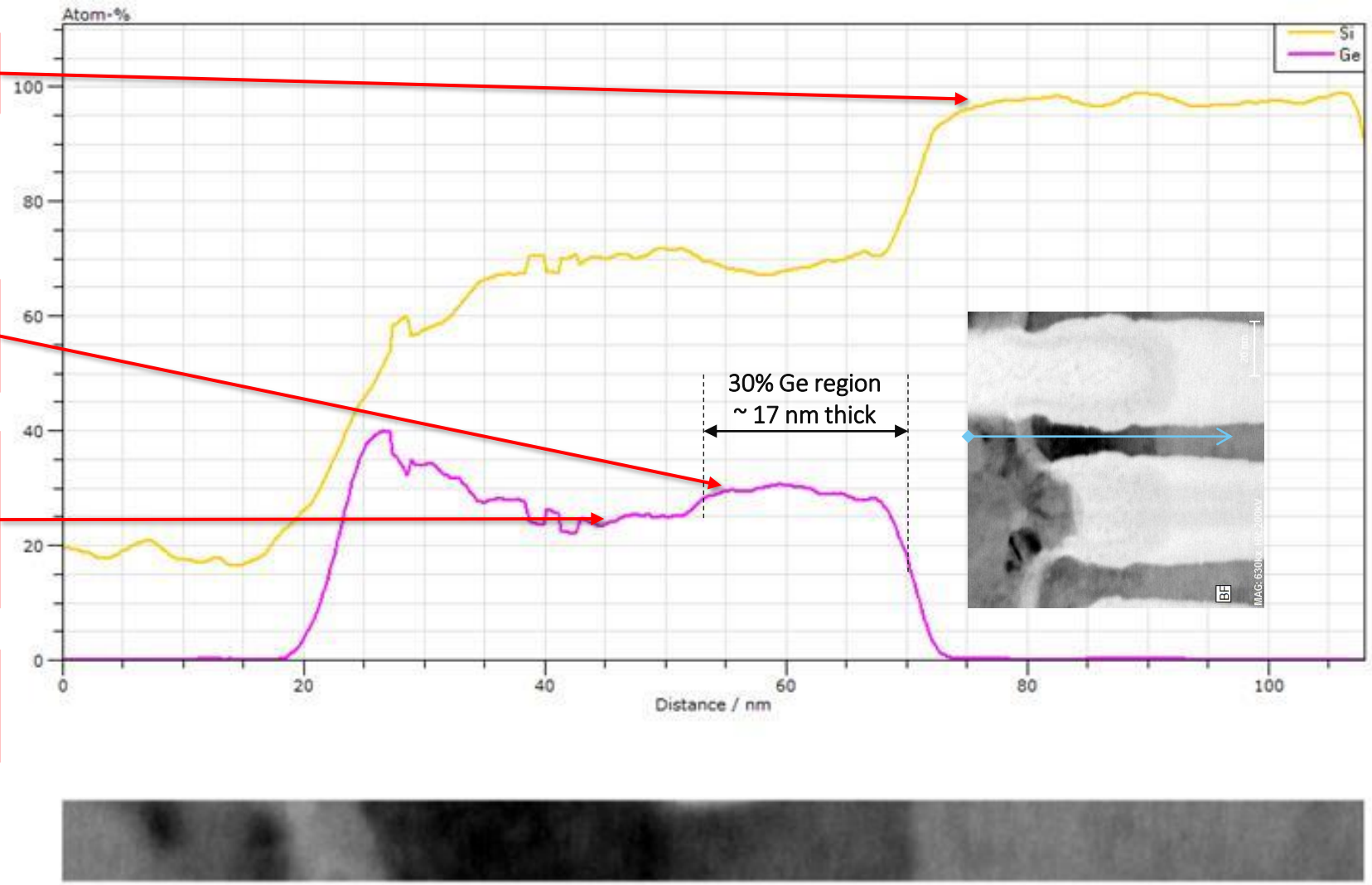
FEOL Analysis – TEM Across Fins

The lower fin is Si (below the etchback).

The first epitaxial SiGe region in the lower part of the PMOS fin is 30% Ge or $Si_{0.7}Ge_{0.3}$.

As epitaxy continues to grow the SiGe PMOS fin, the Ge concentration is reduced to approximately 25% or $Si_{0.75}Ge_{0.25}$.

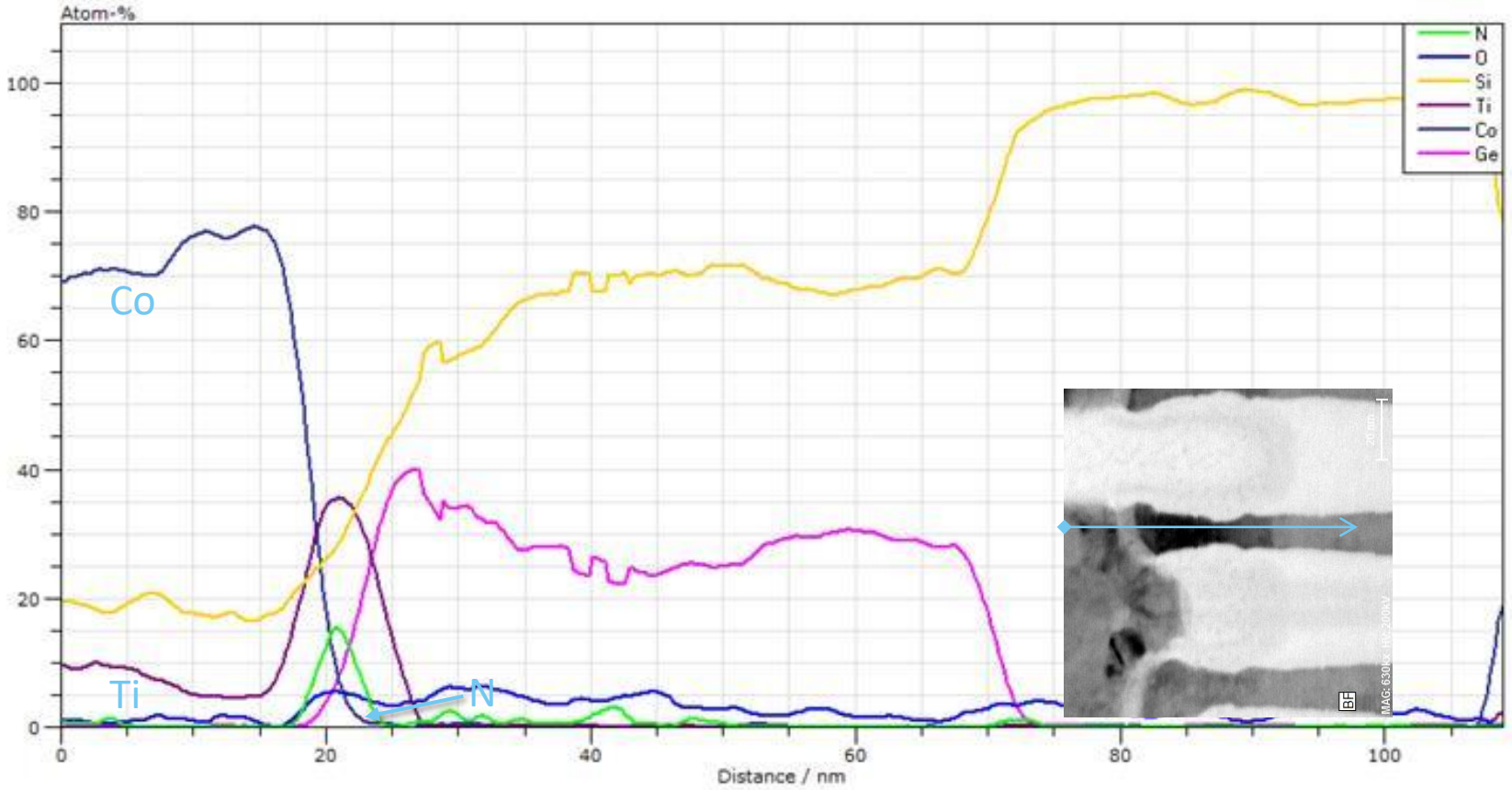
The compressive e-SiGe S/D boosts the Ge to 40% ($Si_{0.6}Ge_{0.4}$).



*Line Profile of Si and Ge in the PMOS Fin – TEM **EDS***

FEOL Analysis – TEM Across Fins

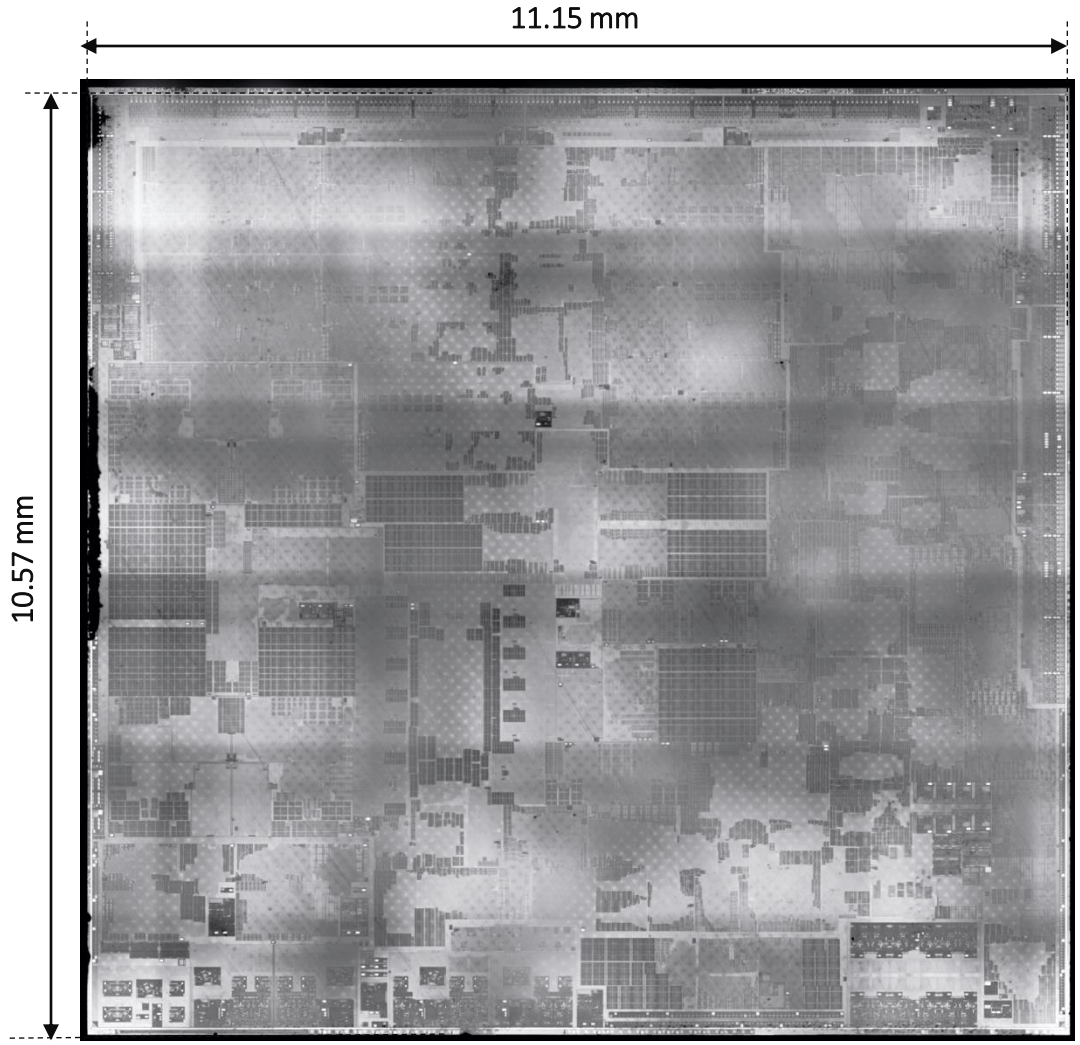
- The TiN lined Co filled contact materials are indicated by the Co, Ti, and N signals from 0 through ~ 25 nm in the graph to the right.



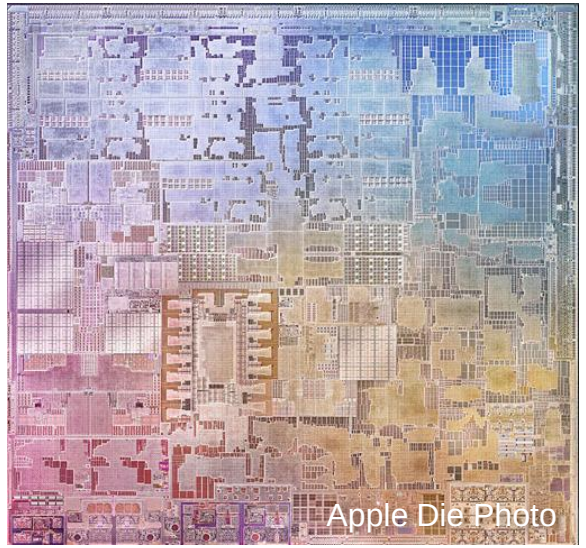
*Line Profile of Constituent Elements in the PMOS Fin and Contact – TEM **EDS***

FLOORPLAN
ANALYSIS

Die Overview & Dimensions



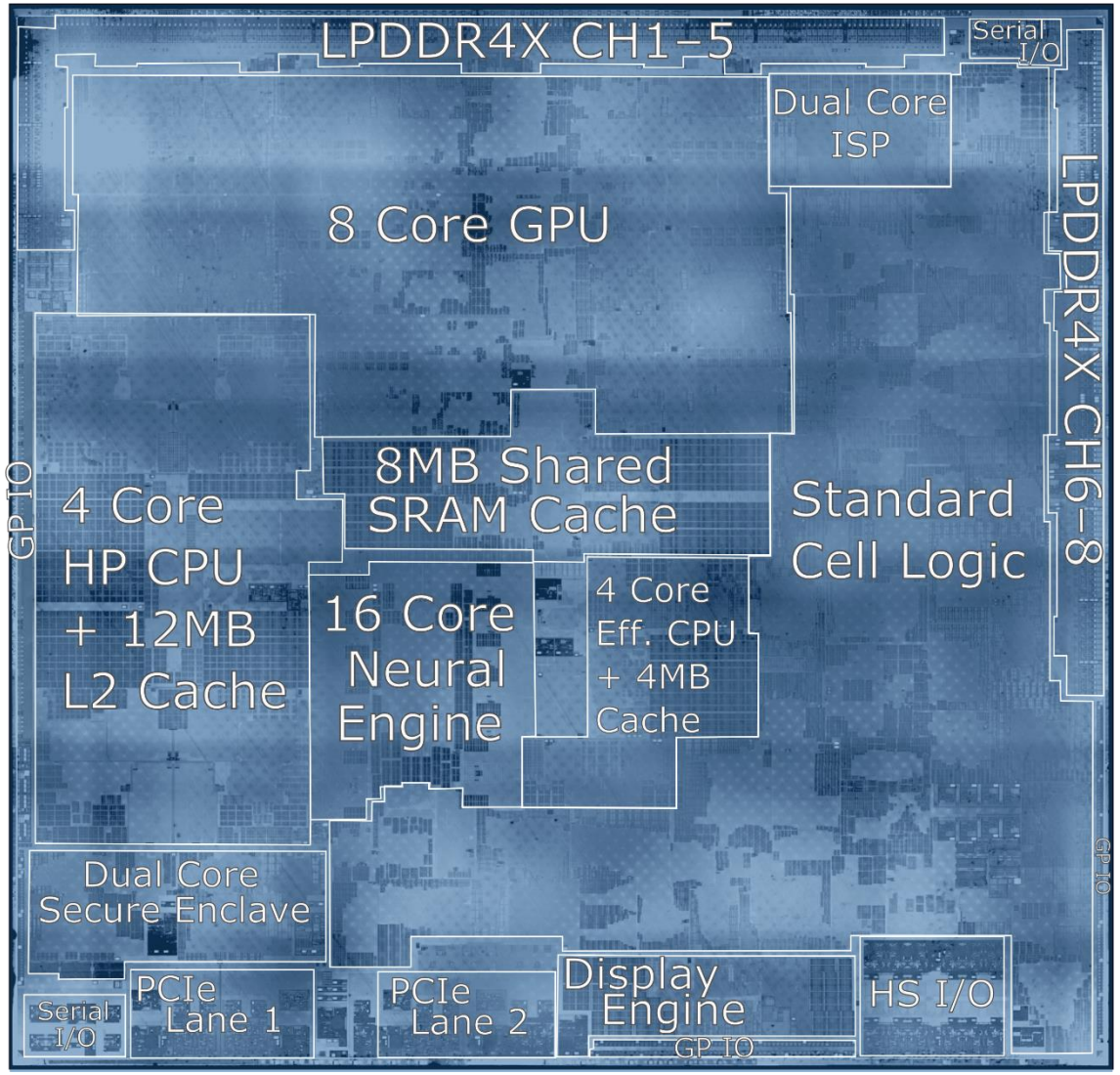
- Die Area: **117.8 mm²**
  (11.15 x 10.57 mm) (within scribe seal)



SoC Backside Die View adjusted to match orientation of Apple marketing Die Photo – Backside IROM

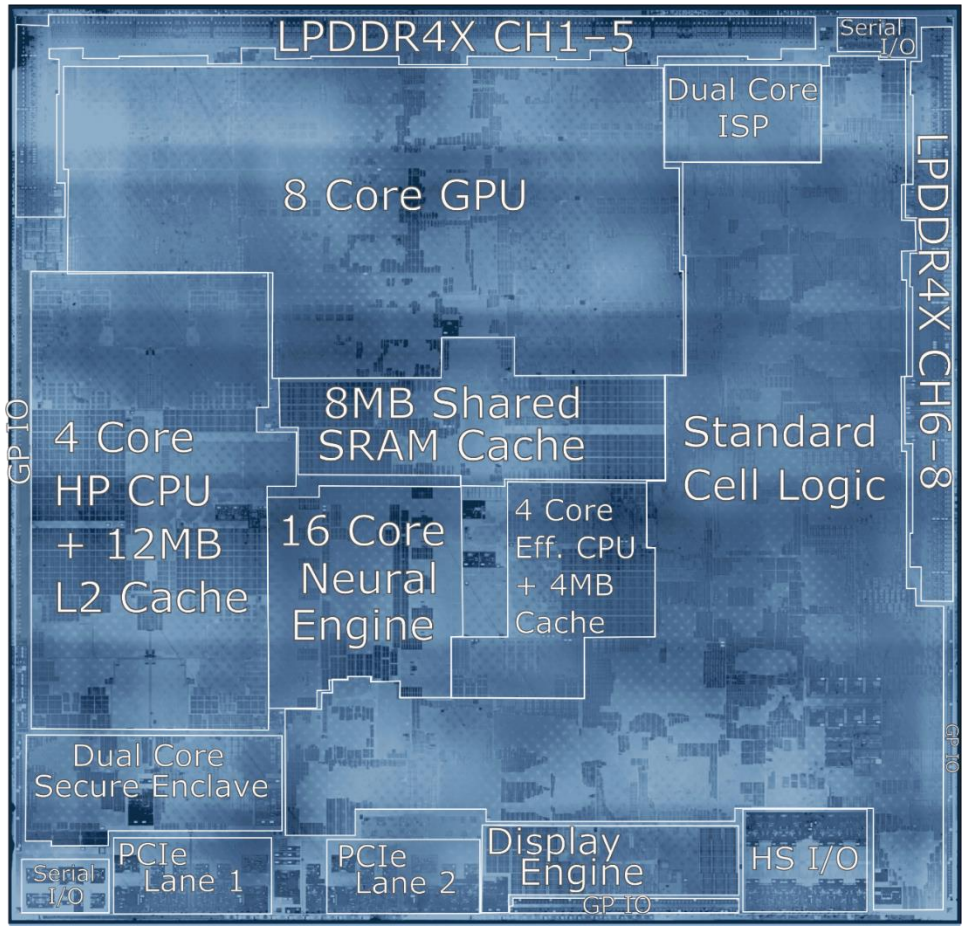
Die Floorplan – Major IP Blocks

- The three major contributors to die area are the eight core GPU, the standard cell logic area, and the HP computing complex comprising four Firestorm CPU cores and 12 MB of L2 SRAM cache memory.
- These three functional areas take up approximately 60% of the active area of the die (inside the scribe seal).



SoC Annotated with Major IP Blocks – Backside IROM View

Die Floorplan – Major IP Blocks



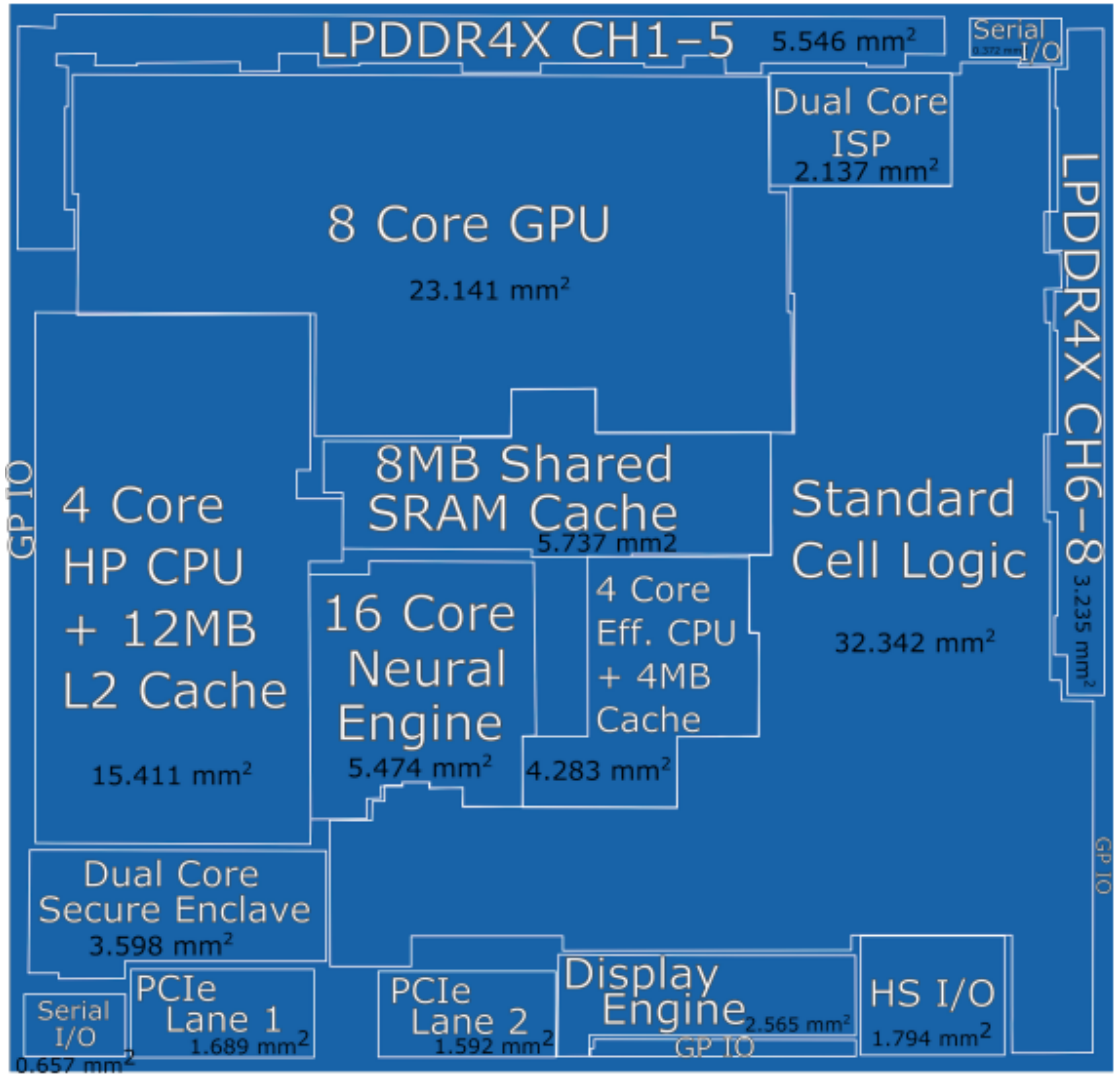
SoC Annotated with Major IP Blocks – Backside IROM View

Die Overview after removing of the metal Layers

Die Floorplan – Major IP Block Area Utilization

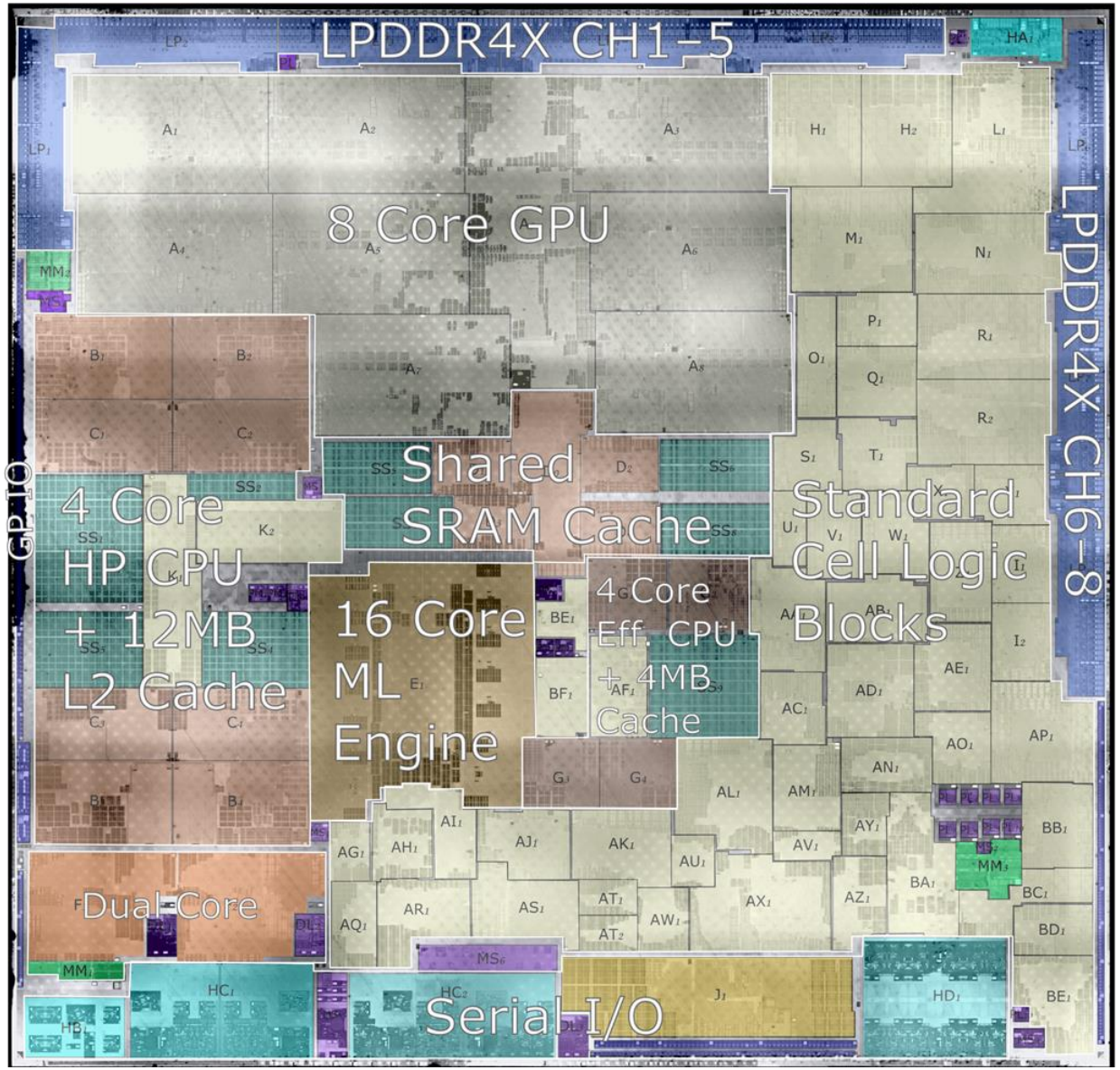
IP Block	Area (mm²)	% of Total
High Performance Compute Complex (4 Core HP CPU + 12MB L2 cache, *Firestorm*)	15.41	13.1%
Efficiency Compute Complex (4 Core Eff. CPU + 4MB L2 cache, *Icestorm*)	4.28	3.6%
8 Core GPU	23.14	19.6%
16 Core Neural Engine	5.47	4.6%
8 mB Shared SRAM Cache	5.74	4.5%
Dual Core Secure Enclave	3.60	3.1%
Standard Cell Logic	32.34	27.5%
LPDDR4X Interface Total (CH 1–8)	8.78	7.5%
Dual Core ISP	2.14	1.8%
Display Engine	2.57	2.2%
PCI Express (Lane 1 + Lane 2)	3.28	2.8%
HS I/O	1.79	1.5%
Other Serial I/O (2 Blocks)	1.03	0.9%

Major IP Block Area Summary with Percentage Die Contributions



Major IP Blocks and Area Utilization

Die Floorplan – Detail of Constituent Circuit Blocks

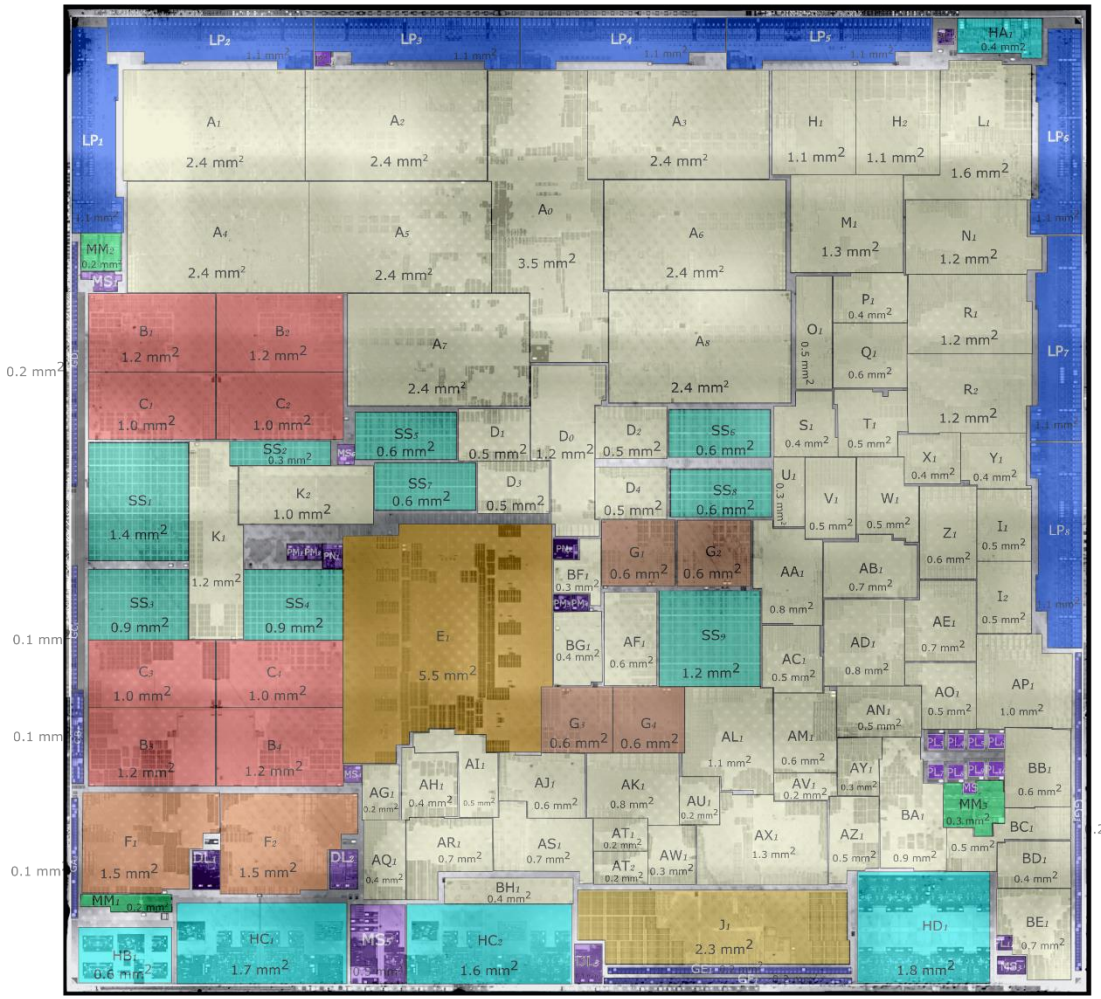


SoC Annotated with Major IP Blocks - IROM View

Die Floorplan – Detail of Constituent Circuit Blocks

Constituent Block (Not Comprehensive)	Area (mm^2)
HP CPU Core, *Firestorm (B1 + C1 block)*	2.24
Efficient CPU Core, *Icestorm* (D1 block)	0.45
GPU Core (A1 block)	2.44
Neural Engine Core	0.21
8 mB Shared SRAM Cache (blocks SS5–8)	2.32
Secure Enclave Core (F1 block)	1.46
LPDDR4X Interface (Block LP1)	1.09
HP CPU L2 SRAM Cache Array (block SS1)	1.42
HP CPU L2 SRAM Cache Array (block SS2)	0.30
HP CPU L2 SRAM Cache Array (block SS3)	0.85
HP CPU L2 SRAM Cache Array (block SS4)	0.85
Efficient CPU L2 SRAM Cache Array (block SS9)	1.17

Selected Constituent Block Area Summary



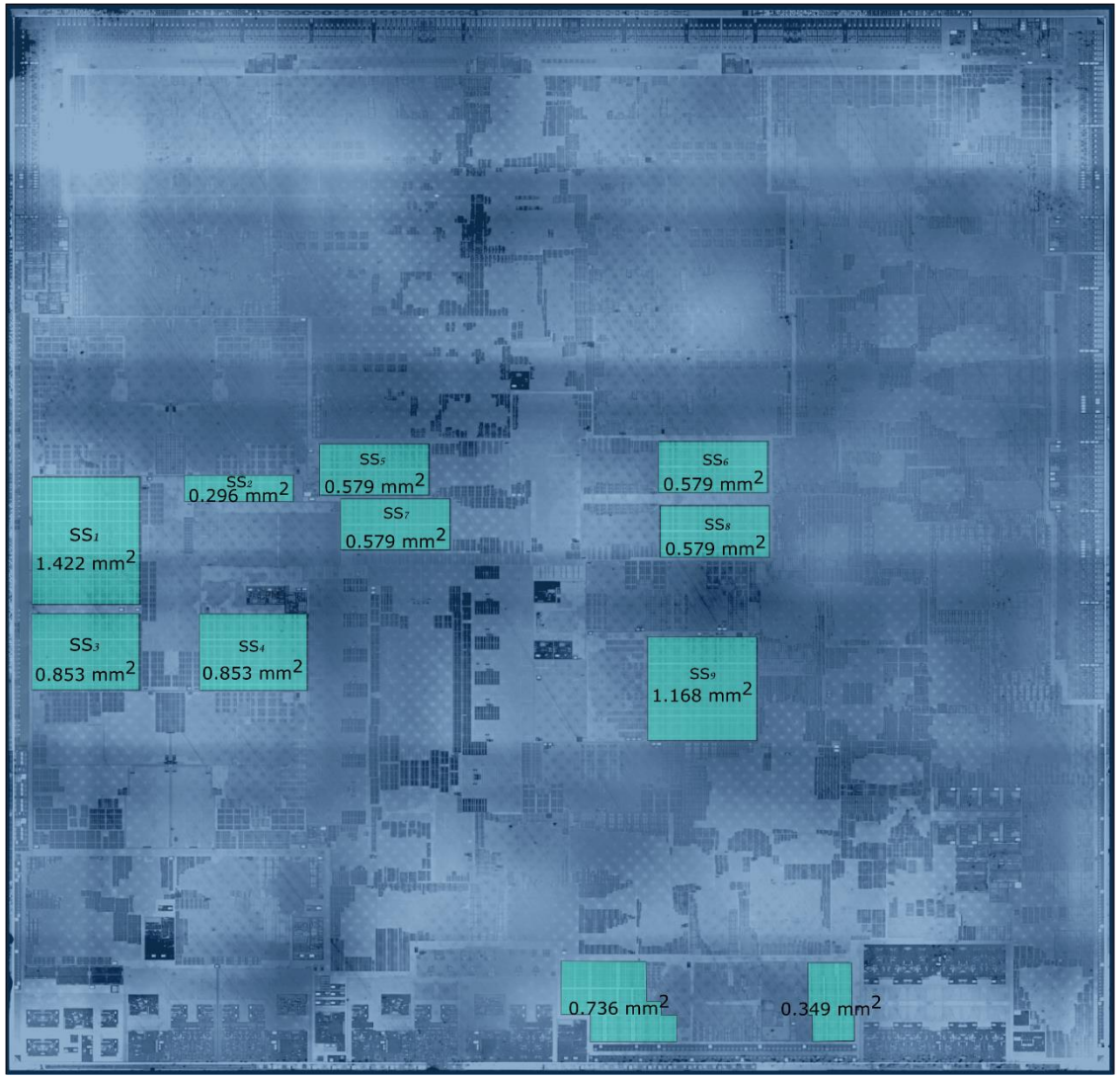
SoC Annotated with Major IP Blocks and Underlying Detailed Block Itemization – Backside IROM View

Note: Area annotations on image rounded to ± 0.1mm^2

Die Floorplan – SRAM

- Total SRAM cache arrays (not including L1 cache in cores) occupies 8.68 mm^2.
- The SRAM bit size estimate is 27.8 MB based on area calculation and Apple's disclosure of sizes for the CPU (Firestorm and Icestorm) L2 caches.
- Smaller SRAM areas distributed through the GPU connection logic (A0) and the standard cell logic are not allocated in this estimate.

Note: SRAM from Display Engine block (J1) allocated in that processing core area for die area totals.



SoC Annotated with L2 SRAM Cache Arrays – Backside IROM View

Die Floorplan – Memory Summary

- There are approximately 27.8 MB of L2 cache memory as well as distributed blocks of SRAM in various logic regions.
- The summary here includes only L2 cache types.
- In addition, three regions of assumed OTP memory were recognized.
- The total die are occupied by the SRAM is 8.68 mm^2.
- The OTP memory takes only 0.7 mm^2.

Memory Block	Description	Area (mm^2)
SS1	L2 SRAM	1.42
SS2	L2 SRAM	0.30
SS3	L2 SRAM	0.85
SS4	L2 SRAM	0.85
SS5	L2 SRAM	0.58
SS6	L2 SRAM	0.58
SS7	L2 SRAM	0.58
SS8	L2 SRAM	0.58
SS9	L2 SRAM	1.17
MM1	OTP / ROM Memory	0.17
MM2	OTP / ROM Memory	0.19
MM3	OTP / ROM Memory	0.33
No Label	Display Engine SRAM (die area sum included in IP block J1)	0.74
No Label	Display Engine SRAM (die area sum included in IP block J1)	0.35

Die Floorplan – Input / Output Summary

- The I/O functionality of the M1 includes eight 16b LPDDR4X channels, two lanes of PCI Express, three additional serial interfaces as well as seven regions of general purpose I/O.
- These functional blocks consume a total area of 15.8 mm² or 13.4% of the die.

I/O Block	Description	Area (mm²)
LP1	LPDDR4X Channel	1.09
LP2	LPDDR4X Channel	1.09
LP3	LPDDR4X Channel	1.09
LP4	LPDDR4X Channel	1.09
LP5	LPDDR4X Channel	1.09
LP6	LPDDR4X Channel	1.09
LP7	LPDDR4X Channel	1.09
LP8	LPDDR4X Channel	1.09
HA1	Serial I/O	0.37
HB1	Serial I/O	0.63
HC1	PCI Express (Lane 1)	1.66
HC2	PCI Express (Lane 2)	1.59
HD1	High speed serial interface	1.79
GA1	General purpose I/O	0.09
GB1	General purpose I/O	0.13
GC1	General purpose I/O	0.08
GD1	General purpose I/O	0.15
GE1	General purpose I/O	0.20
GF1	General purpose I/O	0.17
GG1	General purpose I/O	0.24

Die Floorplan – PLL and DLL Summary

- There appear to be several PLL types on the M1 die and an assumed DLL block.
- PL 1 through 11 are the same layout, PM 1 through 4 share another design while PN1 and PN2 are two other distinct layouts.

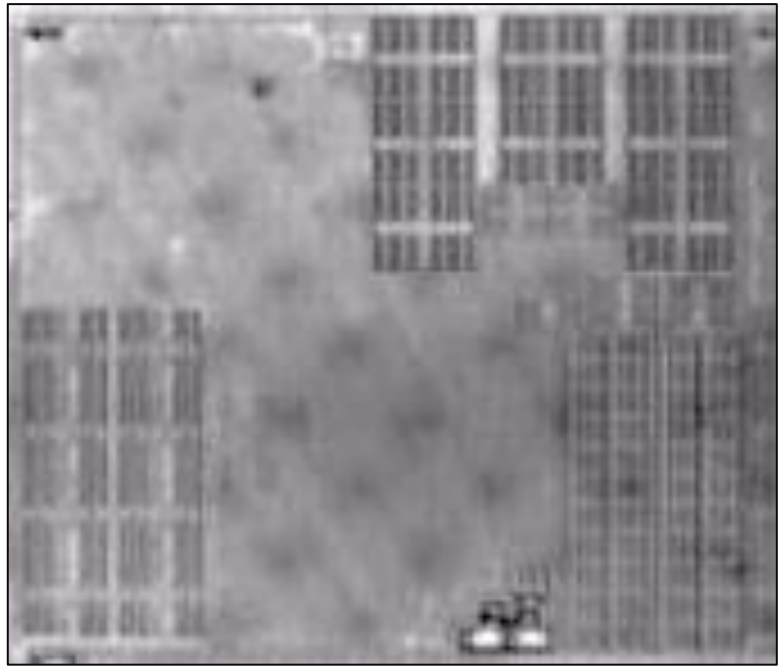
PLL / DLL Block	Description	Area (mm²)
PL1	PLL	0.027
PL2	PLL	0.027
PL3	PLL	0.027
PL4	PLL	0.027
PL5	PLL	0.027
PL6	PLL	0.027
PL7	PLL	0.027
PL8	PLL	0.027
PL9	PLL	0.027
PL10	PLL	0.027
PL11	PLL	0.027
PM1	PLL	0.035
PM2	PLL	0.035
PM3	PLL	0.035
PM4	PLL	0.035
PN1	PLL	0.058
PN2	PLL	0.063
DL1	DLL	0.131
DL2	DLL	0.131
DL3	DLL	0.131

Die Floorplan – Mixed Signal Summary

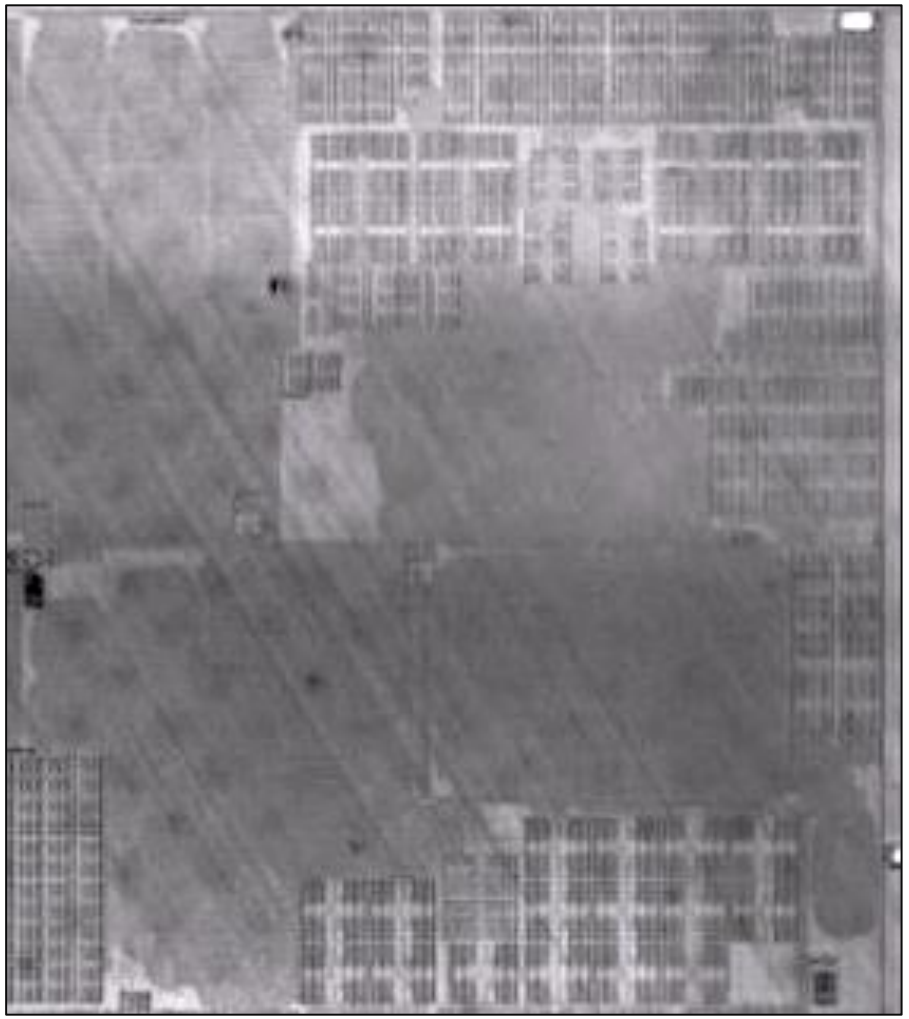
MS / Analog	Description	Area (mm^2)
MS1	Unspecified mixed signal block	0.072
MS2	Unspecified mixed signal block	0.015
MS3	Unspecified mixed signal block	0.060
MS4	Unspecified mixed signal block	0.035
MS5	Oscillator similar to those included in IO3 and IO4 (PCIe)	0.516
MS6	Unspecified mixed signal block	0.041

Die Floorplan – CPU Core Comparison

- The core layout images allow the complexity of the two CPU cores to be compared.
- A single HP core occupies 2.24 mm^2 of die area while each power efficient core takes up only 0.45 mm^2.



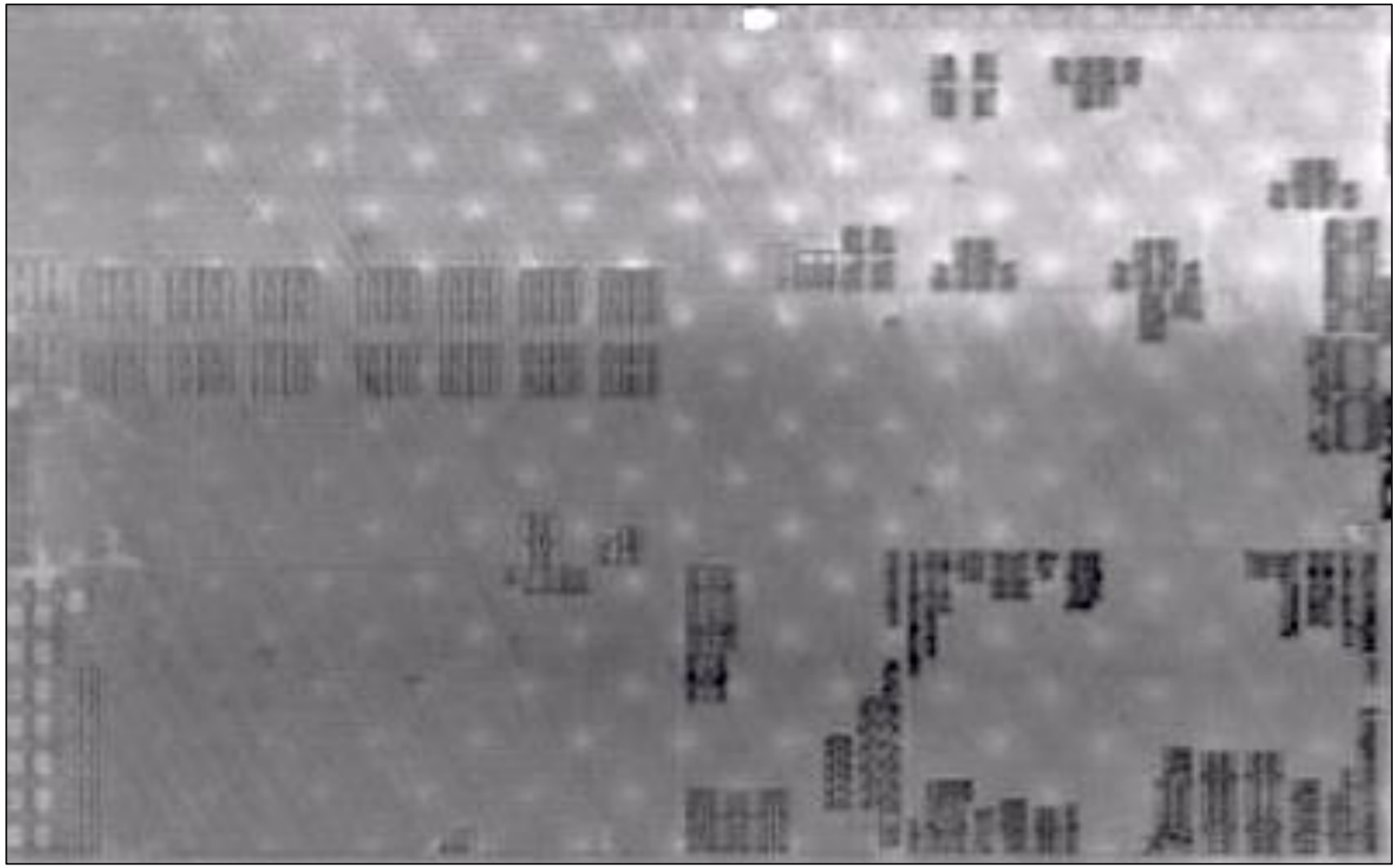
Efficient Icestorm CPU Core – Backside IROM Detail View



HP Firestorm CPU Core – Backside IROM Detail View

The images are not to scale.

Die Floorplan – GPU Core

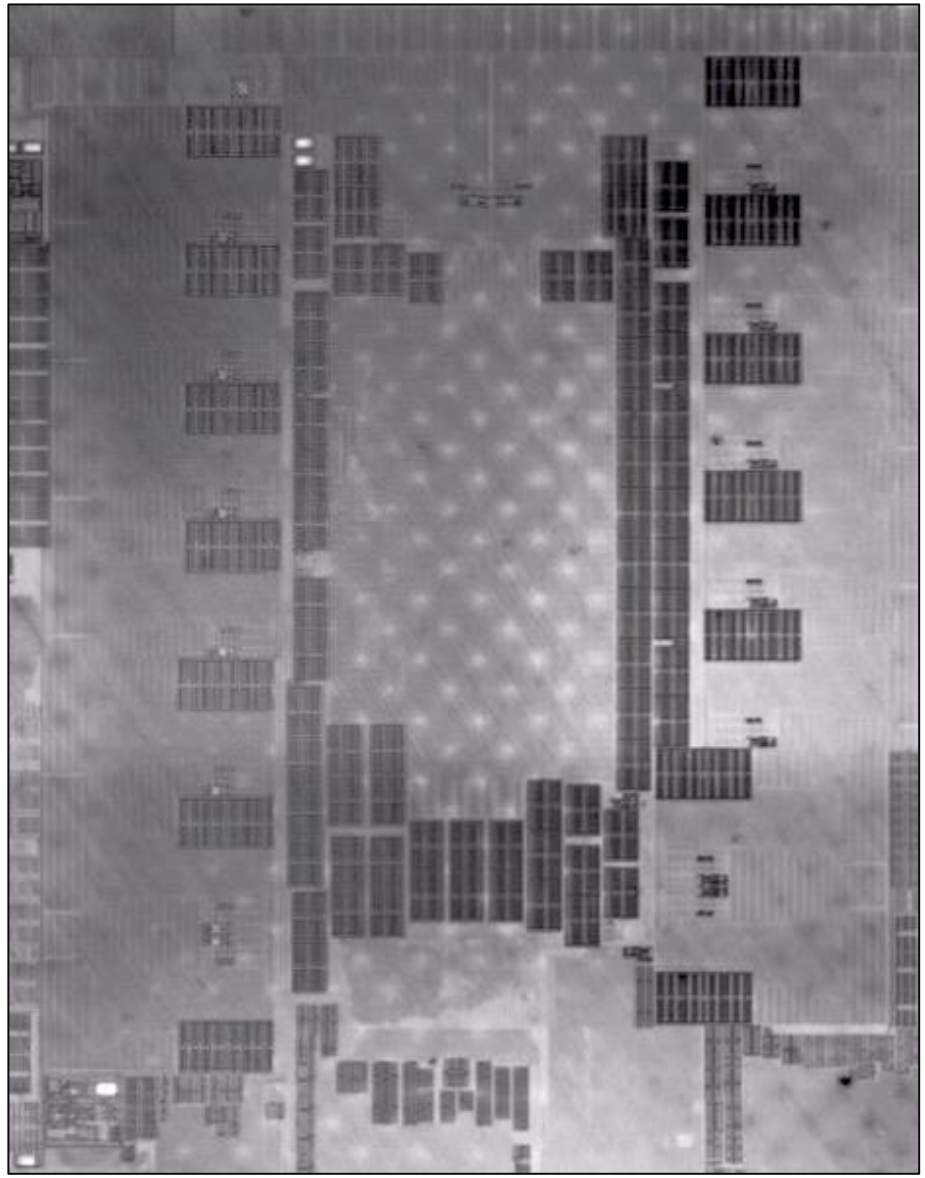


GPU Core – Backside IROM Detail View

- The M1 GPU complex includes eight of these cores as well as a logic area for control of data passing between them.

Die Floorplan – NPU Complex

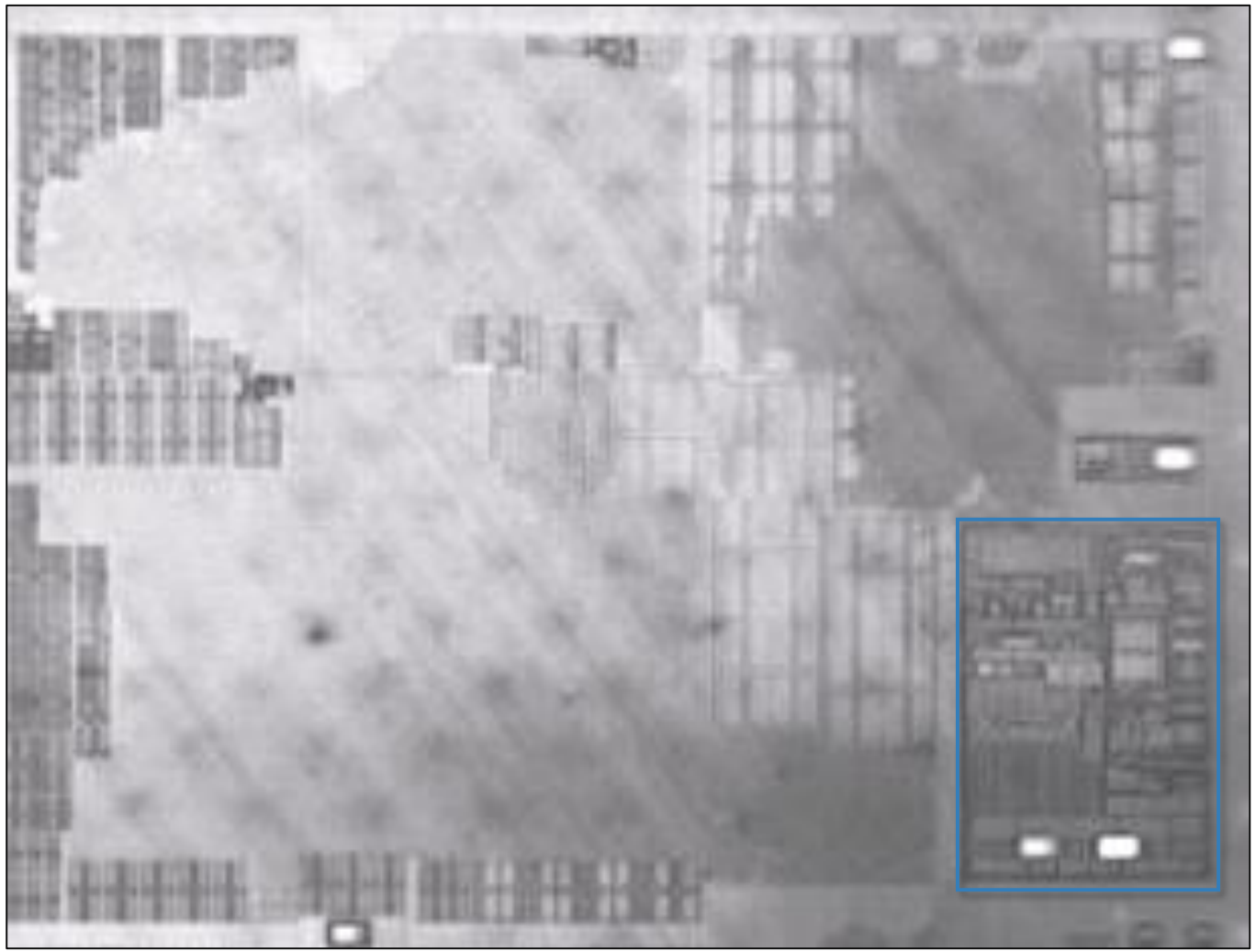
- The *Neural Engine* of the Apple M1 SoC is a complex of 16 small cores with a central area of control logic.



NPU Complex – Backside IROM Detail View

Die Floorplan – Secure Enclave Core

- This layout shows one of the two cores that comprise the dual core *Secure Enclave* of the M1.
- The boxed area shows the DLL layout appearing in the M1 design.



Secure Enclave Core – Backside IROM Detail View

MANUFACTURING
PROCESS FLOW

Global Overview – PCB Substrate

Die

CMOS Manufacturing
4P 2M (+1Cu pillar)
14 Lithography steps

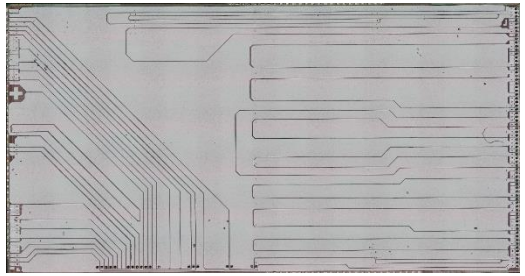
Embedded process

Embedded Die Substrate
Manufacturing
Intermediate Testing

Global Overview – DRAM Memory

Die

CMOS Transistors manufacturing
5M 1P
54 Lithography steps

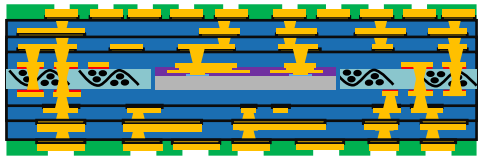


Packaging process

BGA Packaging
Final test
Dicing

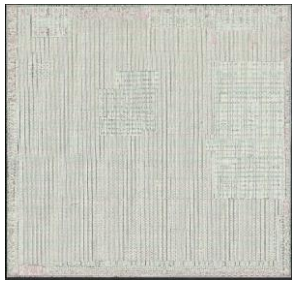
Global Overview – M1

PCB Substrate



Die

FinFET Transistors manufacturing
5 nm, 16M, HKMG
70 Lithography steps



Die

CMOS Manufacturing
3P 2M
12 Lithography steps

Packaging process

SiP Packaging
Final test
Dicing

DRAM Memory

Front-End Process Flow

M1 SoC Die

- Front-End Process:
  - Substrate: 300mm Si wafer
  - Process type: FinFET (Digital, SRAM)
  - Metal layers: 15 Cu + 1 Al layers
  - Technology node: 5 nm
  - Lithography steps: 70
  - Die area: 117.8 mm²

Die characteristics

Description		
Name		Marking
New Die		TMLR68
Type	Manufacturer	
ASIC	APPLE	

Die		
Width	Length	Area
10.570 mm	11.150 mm	117.856 mm2
Pad number	Stack option	Core area
16500		113.998 mm2

Front-End description

Technology		
Material	Min. dimension	Start production
Si	0.005 µm	15/07/2019
Functions		
Digital, SRAM		

Parameters		
Device	Gate oxide nb	Polysilicon nb
FinFET	2 ox	1 poly
Metal layers	Litho steps	
16 met	70 lithos	

Wafer Fabrication Unit

- The Apple M1 is the first ARM-based system on a chip (SoC) designed by Apple Inc.
- System Plus Consulting assumes that the manufacturing of the dies is made by TSMC on 300mm wafers.
- Wafer fab unit:
  - Name: TSMC Fab 18
  - Wafer diameter: 300 mm (12-inch)
  - Capacity: 60,000 wafers / month
  - Year of start: 2019
  - Most advanced process: FinFET 5nm
  - Products: advanced technology (FinFET)
  - Location: Tainan, Taiwan

Fab Unit Description			
Name			
TSMC - Fab 18			
Country		City	
Taiwan		Tainan	
Parameters			
Minimum dim.	Wafer size	Creation Date	Capacity
0.005 µm	**300 mm**	**01/01/2019**	60000 W/m
Type			
Automatized foundry			

- We assume that the complete construction of Phase 1 fab and equipment installation was completed in 2019
- We assume that mass production of the 5nm technology wafers started in the first half of 2020 .
  - System Plus Consulting assumes that clean room and equipment are new and not depreciated.

M1 SoC Die - Back-End 0: Probe test, Backgrinding,Bumping & Dicing

Probe test

- The wafers are tested one time after the end of the manufacturing process steps. The probe test consists of a test of all the electrical functions.
- System Plus Consulting estimates that the probe yield is 88% in medium yield.
- There are 524 potential good dies of 117.8 mm² per 300mm wafer.
- Equipment test is supposed to be a “High performance processor tester” ($1,836,000) with a parallelism of 1 die under test at one time.
- Estimated test time: 28.50 seconds per die.
- Probe test is supposed to be realized by TSMC in Taiwan.

Back-End 0 description

Probe test equipment			
High-performance processor (> 1.5GHz) high pin number			
Equipment Price	Paralelism	Test nb	Test duration
1,836,000 $	1 in //	1	28.50 sec
Other operations			
Bumping: Copper pillar			
Dicing: Mechanical sawing			

Backgrinding

- The wafer is thinned down to 388µm.
- We assume that backgrinding is done by TSMC in Taiwan.

Bumping and Dicing

- Bumping and dicing are assumed to be realized by TSMC in Taiwan.
- The bumping yield is estimated to 97%.
- The dicing yield is estimated to 99.14%.

M1 SoC Die Back-End: Final Test

- After the dicing, the component is tested during the final test.
  - System Plus Consulting estimates that the final tests are realized by TSMC in Taiwan.
  - Equipment test is supposed to be a “High performance processor tester” ($1,836,000) with a parallelism of 1 die under test at one time.
  - The test time is estimated to 28.50 seconds. 100% of the circuits are tested during the final test.
  - System Plus Consulting estimates that there is 1 component tested in parallel.
  - The final test yield is estimated to 99%.

Final test description			
Equipment			
High-performance processor (> 1.5GHz) high pin number			
Equipment Price	Paralelism	Test nb	Test duration
1,836,000 $	1 in //	1	28.50 sec

DRAM Memory Front End – Main Process Steps

Process flow methodology requires analysis of images and material used in order re-create the fabrication process of the memory.

- CMOS and metal layers front-end process:
  - Substrate: 300 mm Silicon wafer
  - Process type: CMOS (Digital, Analog)
  - Metal layers: 8 M total
    5 top metal (3 Cu + 1 Al + 1 Al pad)
    3 bottom metal layers (W –Word line, W Bit line, W metal 1)
  - Technology node: 55 nm
  - Lithography steps: 44

- DRAM capacitors process:
  - Main steps:
    - ✓ Bitline contacts
    - ✓ Stacking support material and sacrificial material
    - ✓ Etching support material and sacrificial material
    - ✓ Deposition of 1st electrode
    - ✓ Deposition of dielectric material
    - ✓ Deposition 2nd electrode
  - Technology node: 19 nm
  - Lithography steps: 10

DRAM Memory Front End – Main Process Steps

- We assume that the DRAM die is designed and manufactured by SK Hynix in China.
- Wafer fab line :
  - Name: Hynix C2
  - Wafer diameter: 300mm (12-inch)
  - Capacity: 121,000 wafers/month
  - Most advanced process: 18nm
  - Products: Memory
  - Location: Wuxi, China
- This manufacturing line was expanded/ updated in 2017 and completed in 2019.
- We estimate that a lot of equipment are new and not depreciated.

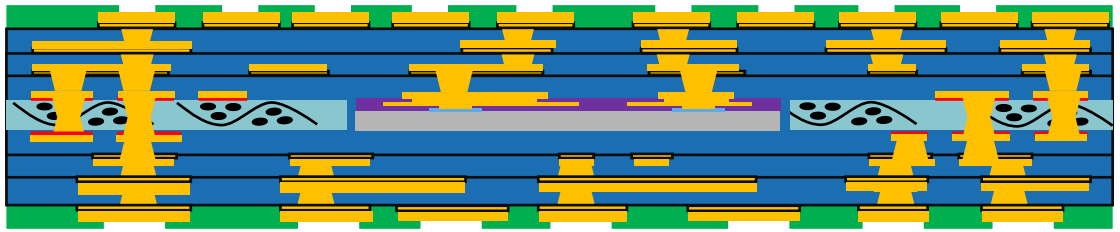
Fab Unit Description

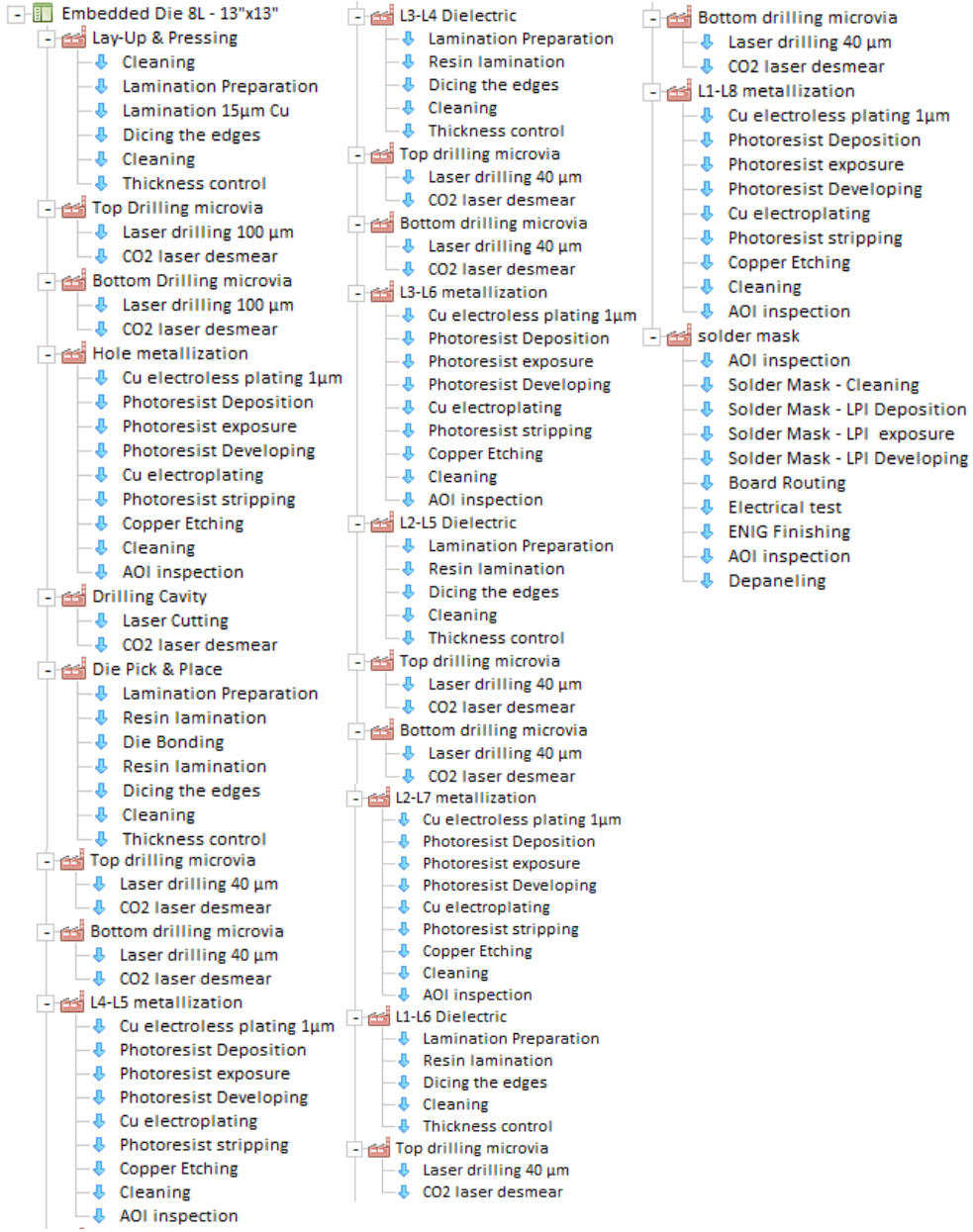
Name			
Hynix - C2			
Country		City	
China - (National)		Wuxi (Jiangsu)	
Parameters			
Minimum dim.	Wafer size	Creation Date	Capacity
0.018 µm	300 mm	01/04/2019	121000 W/m
Type			
Automatized foundry, up to 5 different technologies, memories, processor			

Embedded Die Process Flow

The embedded die is estimated to be manufactured by ASE in Taiwan.

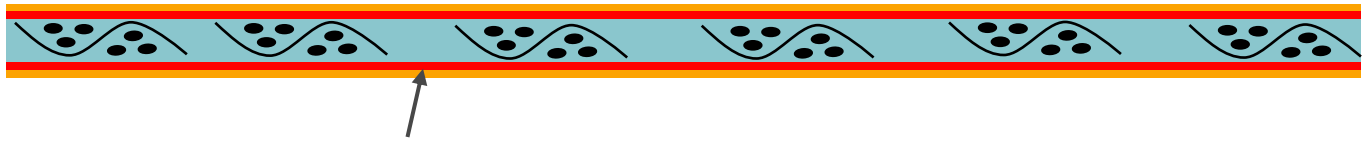
- Embedded Die Process:
  - ✓ Substrate Type: 8-Layer PCB substrate 335 x 340 mm panel
  - ✓ Process type : Embedded die Substrate using mSAP
  - ✓ Embedding technology: Chip First “Face-Up”
- Test:
  - ✓ Test type : Electrical & Thermal tests





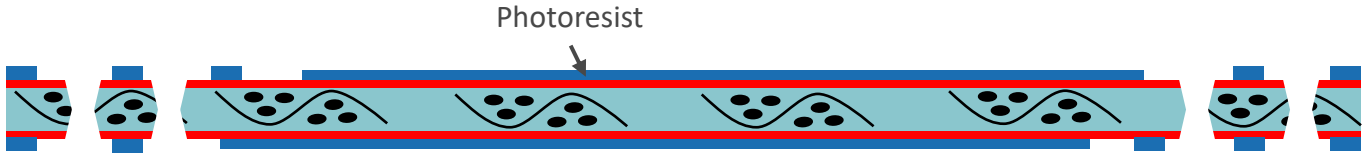
Packaging Process Flow (1/4)

PCB Substrate
- FR-4 Copper Clad

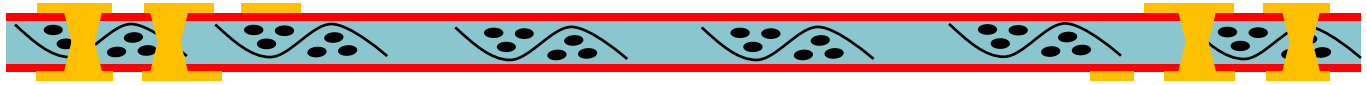


PCB Substrate
- Carrier peeling
- Laser drilling
- Electroless copper plating

PCB Substrate
- Imaging (photoresist lamination, exposure & developing) - LDI



PCB Substrate
- Copper Plating
- Via Filling



PCB Substrate
- Strip-Etch (Photoresist stripping, copper flash etching)
- Laser Drilling

Packaging Process Flow (2/4)

PCB Substrate
- Resin Lamination
- Hot Press

PCB Substrate
- Die Pick and Place
- Epoxy Resin Deposition

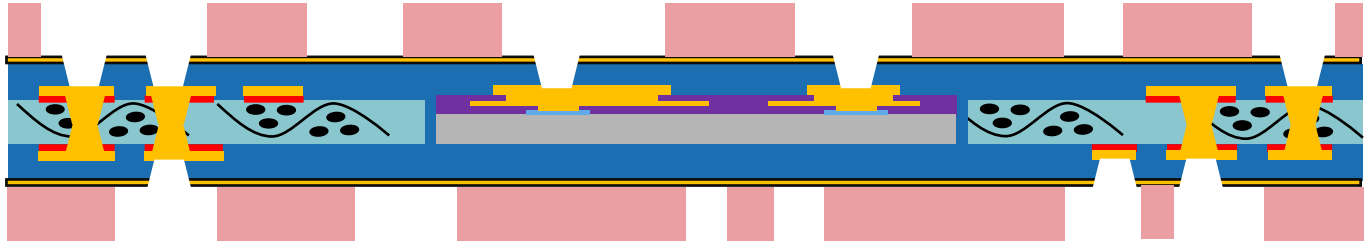
PCB Substrate
- Resin Lamination
- Hot Press

PCB Substrate
- Electroless copper plating

PCB Substrate
- Laser Drilling

Packaging Process Flow (3/4)

PCB Substrate
- Imaging (photoresist lamination, exposure & developing) - LDI



PCB Substrate
- Copper plating & Via Filling
- Strip-Etch (Photoresist stripping, copper flash etching)

PCB Substrate
- Resin Lamination
- Hot Press

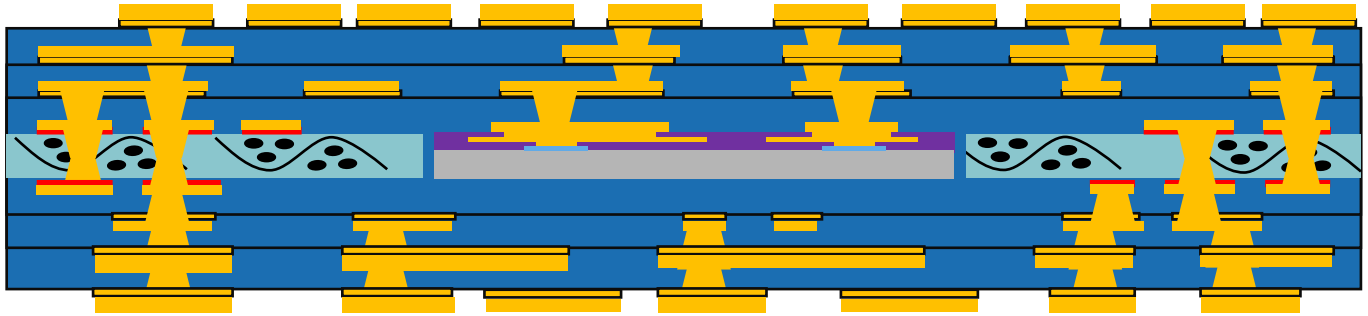
PCB Substrate
- Electroless copper plating

PCB Substrate
- Laser drilling

Packaging Process Flow (4/4)

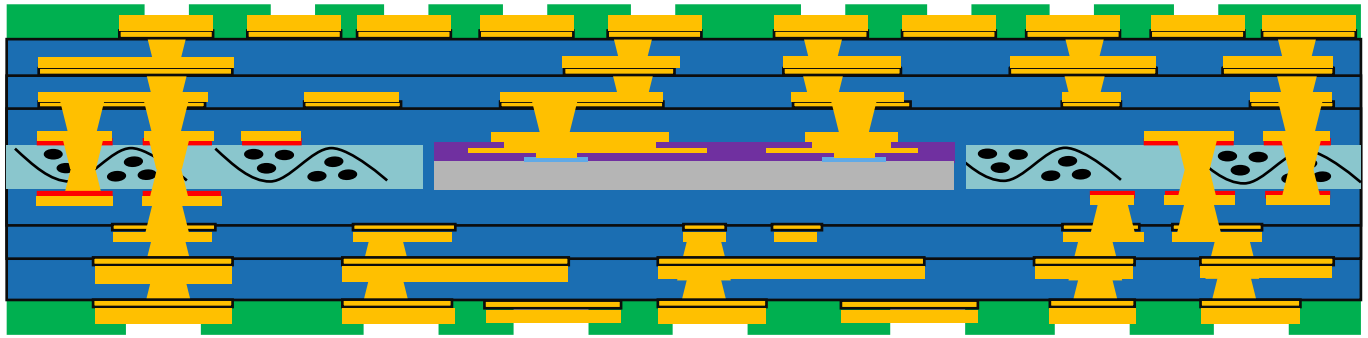
3 Times
PCB Substrate

- Imaging (photoresist lamination, exposure & developing) - LDI
- Copper plating & Via Filling
- Strip-Etch (Photoresist stripping, copper flash etching)
- Resin Lamination
- Hot Press
- Electroless copper plating
- Laser drilling



PCB Substrate

- Solder mask (LPI deposition, exposure & developing)
- Board routing
- Electrical test
- OSP Finishing
- AOI inspection



Component Final Assembly

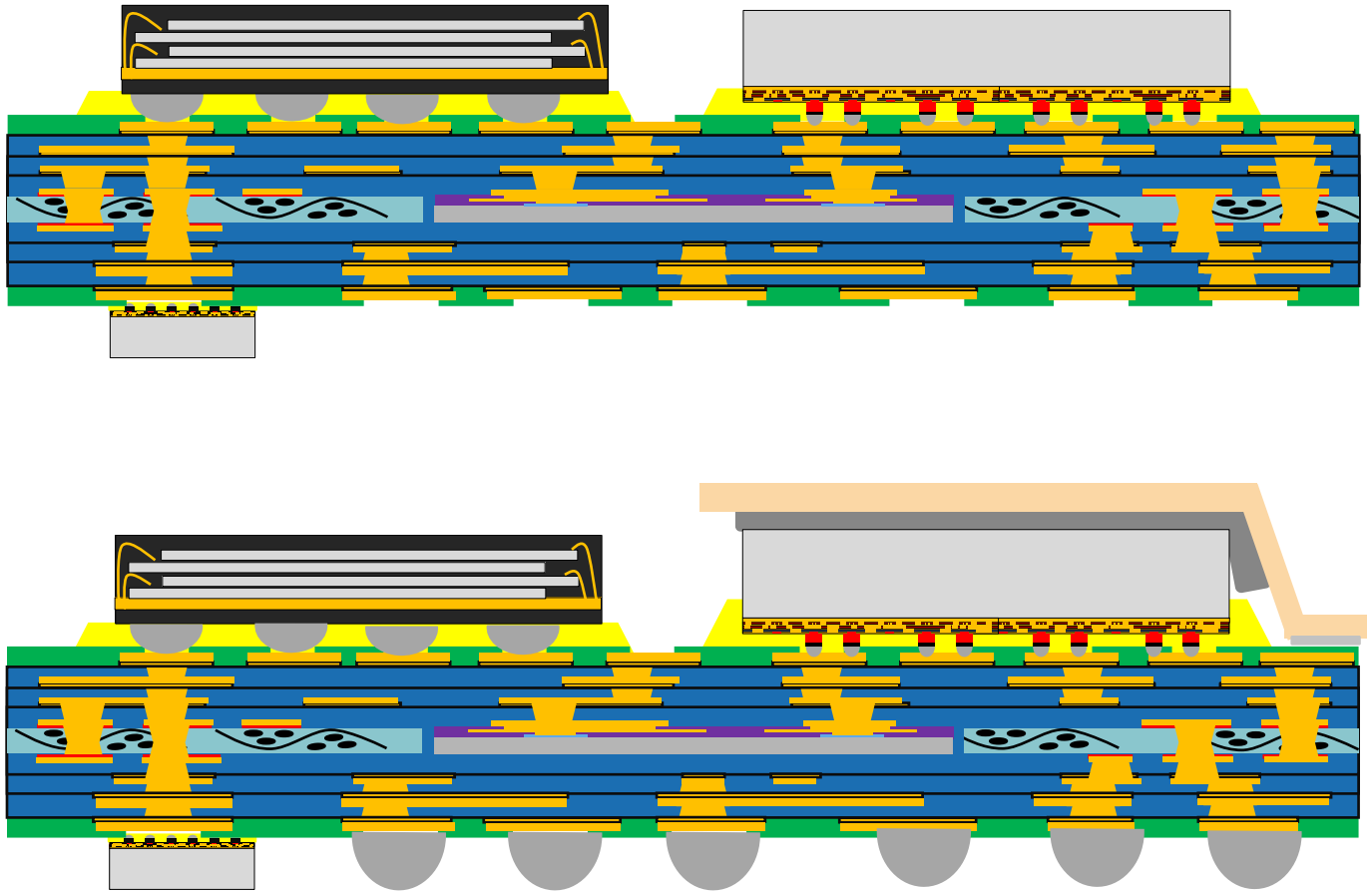
Package Assembly
- Pick and Place M1 SoC Die
- Underfill
- Cure

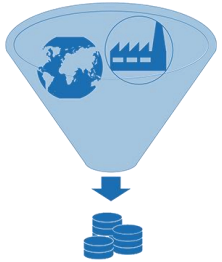
Package Assembly
- Pick and place DRAM PackageX2
- Underfill
- Cure

Package Assembly
- Pick and place SMD Components
- Underfill and Cure

Package Assembly
- Deposit TIM on M1 SoC chip
- Deposit IHS adhesive& Cure
- Pick and Place IHS metal cover

Package Assembly
- Solder ball drop
- Test





COST ANALYSIS

Synthesis of the Cost Analysis

The Apple M1 SoC Component is supplied by Apple.

The M1 SoC Apple die is designed by Apple and manufactured by TSMC in Taiwan.

The LPDDR4 DRAM memory dies are manufactured on 300mm (12-inch) wafers by SK Hynix.

Production of the Apple M1 SoC die is assumed to TSMC in Taiwan.

- The Wafer front-end Cost is estimated at $6,078 (in Medium Yield).
- The Wafer front-end Price is estimated at $12,156 (in Medium Yield).
- The die cost is estimated at $28.77 (in medium yield).
- The tested M1 SoC die cost is estimated at $29.80 (in Medium Yield).

Production of the DRAM die is assumed to SK Hynix.

- The CMOS and metal layers wafer front-end cost are estimated at $2,026 (in Medium yield).
- The DRAM cell structure front-end Cost is estimated at $612 (in Medium yield).
- The total front-end cost is estimated at $2,678 (in Medium yield).
- The die cost is estimated at $1.59 (in Medium yield).
- The 4GB/32Gb component price is estimated at $15.33 in Medium yield.

Assembly and test of the embedded die package is supposed to be ASE in Taiwan.

- The assembly and test price are estimated at $3.69 per module in Medium Yield.

Packaging Cost of the M1 SoC component cost is supposed to be $1.53 in Medium Yield.

- The packaging Price is estimated at $1.91 in Medium Yield.

The M1 SoC component cost is estimated at $67.97 in Medium Yield.

The M1 SoC component price is estimated at $97.10 in Medium Yield.

Main Steps of Economic Analysis – Supply Chain

M1 SoC Die
Front End Cost

M1 SoC Die
Probe Test & Dicing Cost

tsmc

SK Hynix DRAM
Front End Cost

SK Hynix DRAM
Probe Test & Dicing Cost

SK hynix

Embedded Die Packaging
Front End Cost

Embedded Die Packaging
Probe Test & Dicing Cost

ASE GROUP

Package Assembly Cost

Final Test Cost

OSAT
Taiwan

APPLE M1 SoC Component

Yield Explanation

The wafers and dies are tested during the process flow. There are 2 types of test :
- The tests on the physical characteristics of the wafer like the thickness of a deposited layer.
- The tests on the electrical functionalities of the die.

The difference is important because with the physical test, a poor result means a problem on one step and all the dies on the wafer are defective, so the wafer is scrapped. Usually, these yields are good for mature technologies.

The tests on the dies are different. Each die is tested, one by one or simultaneously using “parallel” tests, and only the defective dies are scraped. During the probe test which is realized on the wafer, the defective dies are marked and are not assembled in package.

In this reverse costing study, 5 yields are used :

Process	Yield	Apply on	Description
Front-End	Manufacturing Yield	IC	The defective wafers are scraped
Back-End 0	Probe yield	IC	The defective dies are scraped. The number of good dies is function of the probe yield. Only the good dies are assembled in the package.
Back-End 0	Thinning & Dicing Yields	IC	The defective dies are scraped
Back-End 1	Packaging yield	IC + Package	The defective components are scraped
Back-End 1	Final test yield	IC + Package	The defective components are scraped

Main Steps of Economic Analysis and Yield

	M1 SoC Die		
	Low Yield	Medium Yield	High Yield
FE : Manufacturing yield	79.9%	82.3%	84.2%
BE : Bumping yield	97.0%	97.0%	97.0%
BE : Probe yield	85.0%	88.0%	92.0%
BE : Dicing yield	99.1%	99.1%	99.1%

	DRAM Die		
	Low Yield	Medium Yield	High Yield
FE : Manufacturing yield	98.0%	98.5%	99.0%
BE : Backgrinding yield	99.3%	99.3%	99.3%
BE : Probe yield	95.0%	95.1%	95.2%
BE : Dicing yield	99.5%	99.5%	99.5%

	M1 SoC Die Final Test		
	Low Yield	Medium Yield	High Yield
BE : Final test yield	99.0%	99.0%	99.0%

	DRAM Component		
	Low Yield	Medium Yield	High Yield
BE : Packaging yield	99.7%	99.7%	99.7%
BE : Final test yield	98.8%	98.8%	98.8%

	Embedded Die Packaging		
	Low Yield	Medium Yield	High Yield
BE : Embedded Die Yield	98.0%	99.0%	99.9%
BE : Final Assembly Yield	99.0%	99.5%	99.9%

	M1 SoC Component		
	Low Yield	Medium Yield	High Yield
BE : Packaging yield	99.7%	99.8%	99.9%
BE : Final test yield	97.5%	98.0%	98.5%

- We perform the economic analysis of the M1 SoC die with the IC Price+ tool.
- We perform the economic analysis of the DRAM Memory CMOS Transistors, metal layers and package with the IC Price+ tool.
- We perform the economic analysis of the DRAM technology/capacitors with the IC CoSim+ tool.
- We perform the economic analysis of the embedded package/ PCB and final assembly with PackageCoSim+ tool.
- In our simulation, we assume a development and a production ramp up without important technical problem.

M1 SoC Wafer Front-End Cost

Front-End	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Raw wafer Cost (Si)	$90.00	1.4%	$90.00	1.5%	$90.00	1.5%
Clean Room Cost	$408.30	6.5%	$404.11	6.6%	$399.83	6.8%
Equipment Cost	$3,317.38	52.4%	$3,283.38	54.0%	$3,248.62	55.2%
Consumable Cost	$897.77	14.2%	$888.57	14.6%	$879.17	14.9%
Labor Cost	$342.70	5.4%	$339.19	5.6%	$335.60	5.7%
Yield losses Cost	$1,270.21	20.1%	$1,073.14	17.7%	$929.25	15.8%
M1 SoC Front-End Cost	**$6,326.36**	**100%**	**$6,078.39**	**100%**	**$5,882.47**	**100%**
Foundry Gross Profit	$6,326.36	+50.0%	$6,078.39	+50.0%	$5,882.47	+50.0%
M1 SoC Front-End Price	**$12,652.71**		**$12,156.78**		**$11,764.95**	

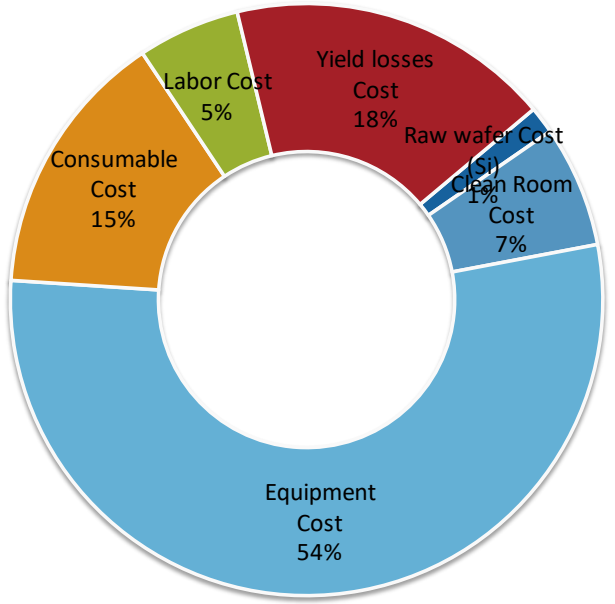
The M1 SoC Wafer front-end cost is estimated at $6,326 in low yield and $5,882 in high yield.

The largest portion of the manufacturing cost is due to the equipment at 54% in medium yield.

We assume that TSMC manufactures Apple's M1 SoC wafers.

We estimate TSMC's gross margin at 50%. The M1 SoC wafer cost with TSMC margin is estimated between $12,652 in low yield and $11,764 in high yield.

M1 SoC Front-End Cost Breakdown (Medium Yield)

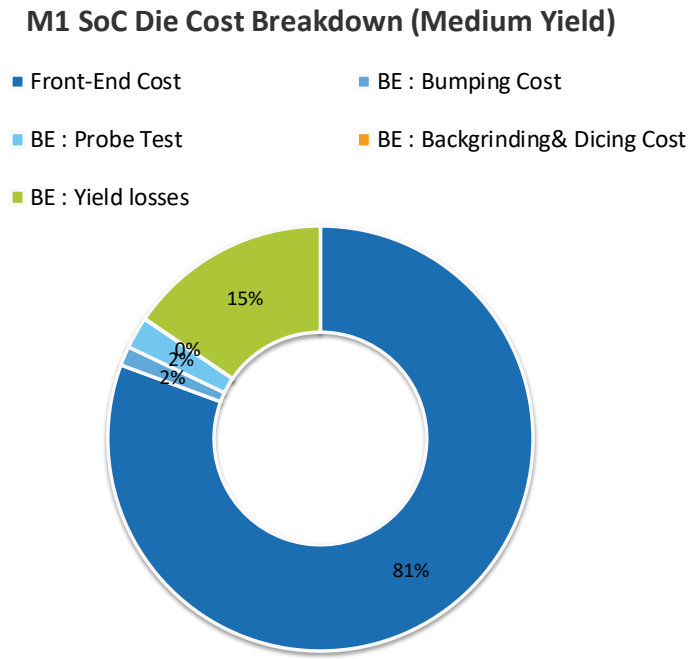


M1 SoC Wafer & Die Cost

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Front-End Cost	$12,652.71	95.6%	$12,156.78	95.4%	$11,764.95	95.1%
BE : Bumping Cost	$221.08	1.7%	$221.08	1.7%	$221.08	1.8%
BE : Probe Test Cost	$356.65	2.7%	$364.57	2.9%	$375.13	3.0%
BE : Backgrinding& Dicing Cost	$5.56	0.0%	$5.56	0.0%	$5.56	0.0%
Total Wafer Cost	**$13,236.01**	**100%**	**$12,747.99**	**100%**	**$12,366.72**	**100%**
Nb of potential dies per wafer	524		524		524	
Nb of good dies per wafer	428		443		463	
Front-End Cost	$24.146	78.1%	$23.200	80.6%	$22.452	84.1%
BE : Bumping Cost	$0.422	1.4%	$0.422	1.5%	$0.422	1.6%
BE : Probe Test	$0.681	2.2%	$0.696	2.4%	$0.716	2.7%
BE : Backgrinding& Dicing Cost	$0.011	0.0%	$0.011	0.0%	$0.011	0.0%
BE : Yield losses	$5.666	18.3%	$4.448	15.5%	$3.109	11.6%
Die Cost	**$30.925**	**100%**	**$28.777**	**100%**	**$26.710**	**100%**

By adding the bumping cost, probe test cost, the thinning and the dicing cost, the wafer cost is estimated at $12,085 in low yield and $11,297 in high yield.

The number of good dies per wafer is estimated at 428 in low yield and 463 in high yield, which results in a die ranging from $30.92 in low yield and $26.71 in high yield.

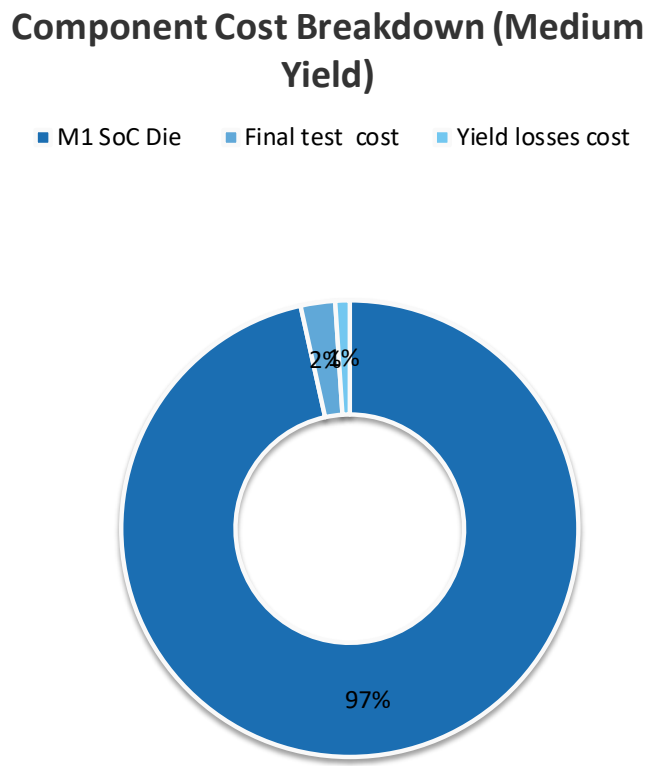


M1 SoC Tested Die Cost

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
M1 SoC Die	$30.925	96.7%	$28.777	96.5%	$26.710	96.4%
Final test cost	$0.727	2.3%	$0.727	2.4%	$0.727	2.6%
Yield losses cost	$0.327	1.0%	$0.305	1.0%	$0.283	1.0%
Final Die Cost	**$31.979**	**100%**	**$29.808**	**100%**	**$27.720**	**100%**

The tested M1 SoC Die cost ranges from $31.97 to $27.72 according to yield.

- The M1 SoC Die represents 97% of the component cost in medium yield.
- The final test represents 2% of the component cost in medium yield.
- Yield losses account for 1% of the component cost.



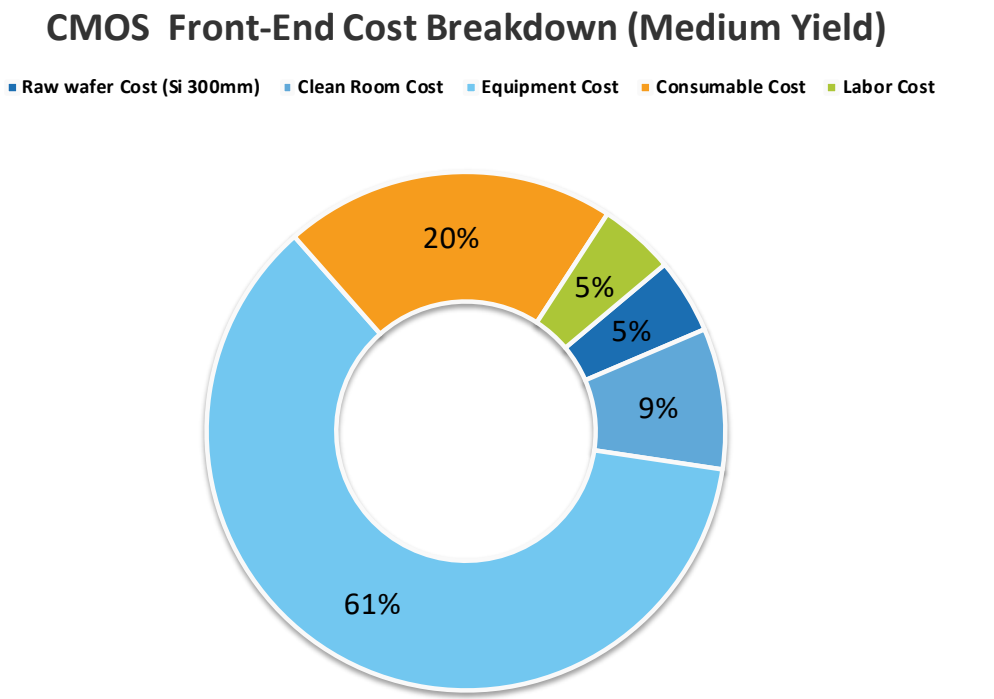
DRAM Memory - CMOS and Top Metal Layers Front-End Cost

CMOS transistor + 8 Metal layers (3 bottom+5top Metals)	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Raw wafer Cost (Si 300mm)	$95.00	4.7%	$95.00	4.7%	$95.00	4.7%
Clean Room Cost	$178.02	8.8%	$178.02	8.8%	$178.02	8.8%
Equipment Cost	$1,239.00	61.1%	$1,239.00	61.1%	$1,239.00	61.1%
Consumable Cost	$419.19	20.7%	$419.19	20.7%	$419.19	20.7%
Labor Cost	$95.31	4.7%	$95.31	4.7%	$95.31	4.7%
Memory Front-End Cost	**$2,026.52**	**100%**	**$2,026.52**	**100%**	**$2,026.52**	**100%**

This front-end cost includes STI insulation, 3 Bottom metal layers (word line in Tungsten, bit line in Tungsten, bit line contacts), CMOS transistors and 5 top metal layers.

The CMOS transistors, 3 bottom and 5 top metal layers front-end cost is $2,026 between high and medium yield.

The largest portion of the manufacturing cost is due to the equipment cost at 61%.



DRAM Memory - DRAM Structure and Total Front-End Cost

DRAM Cells Process	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Clean Room Cost	$53.93	8.8%	$53.93	8.8%	$53.93	8.8%
Equipment Cost	$295.66	48.3%	$295.66	48.3%	$295.66	48.3%
Consumable Cost	$249.83	40.8%	$249.83	40.8%	$249.83	40.8%
Labor Cost	$12.71	2.1%	$12.71	2.1%	$12.71	2.1%
Memory Front-End Cost	**$612.13**	**100%**	**$612.13**	**100%**	**$612.13**	**100%**
Yield losses Cost	$53.85		$40.18		$26.65	
Total Memory (CMOS, Metals, DRAM) Front-End Price	**$2,692.50**		**$2,678.83**		**$2,665.30**	

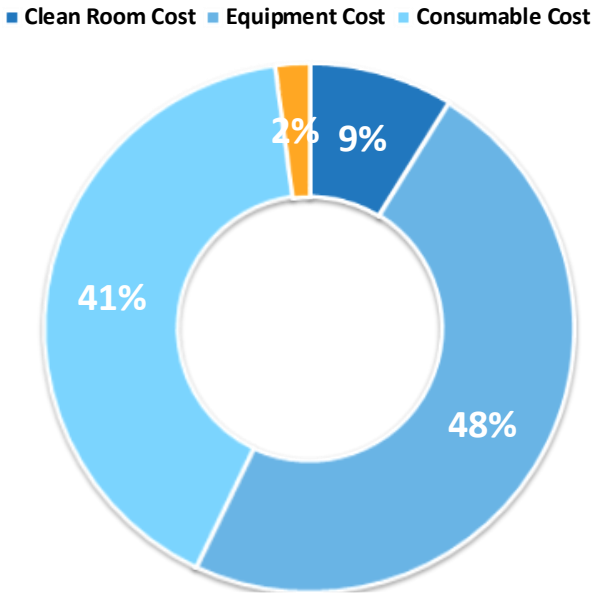
The DRAM capacitor structure front-end cost is estimated at $612.

The largest portion of the capacitor manufacturing cost is due to the high equipment cost at 48%.

Total memory front-end price includes the fabrication cost of CMOS transistor, the metal layers, the DRAM capacitors and yield loss cost.

Total memory front-end cost ranges from $2,692 to $2,665 depending on the different yield loss.

DRAM Cells Manufacturing Cost Breakdown (Medium Yield)

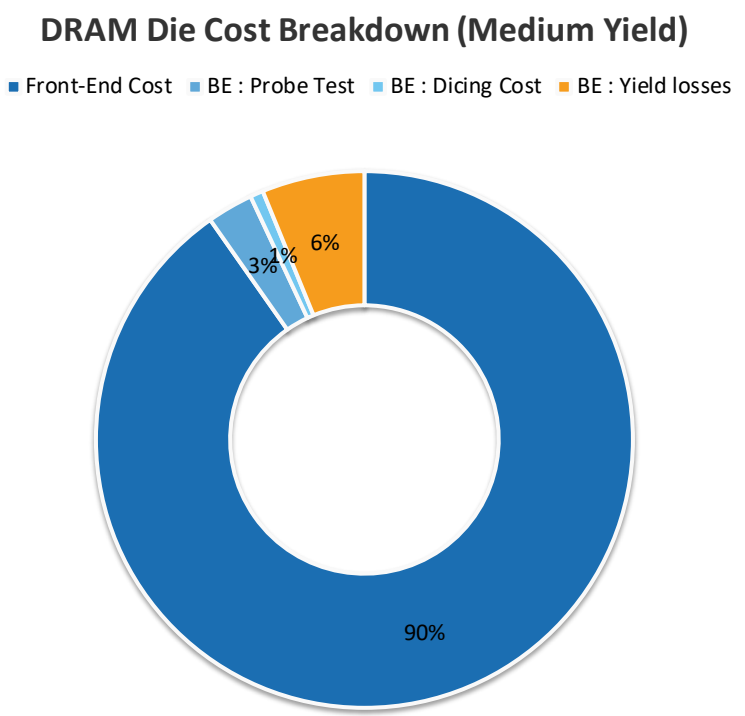


DRAM Memory Wafer & Die Cost

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Front-End Cost	$2,692.50	94.5%	$2,678.83	94.5%	$2,665.30	94.5%
BE : Backgrinding Cost	$50.81	1.8%	$50.81	1.8%	$50.81	1.8%
BE : Probe Test Cost	$82.07	2.9%	$82.12	2.9%	$82.16	2.9%
BE : Dicing Cost	$23.38	0.8%	$23.38	0.8%	$23.38	0.8%
Total Wafer Cost	**$2,848.76**	**100%**	**$2,835.14**	**100%**	**$2,821.65**	**100%**
Nb of potential dies per wafer	1,892		1,892		1,892	
Nb of good dies per wafer	1,776		1,777		1,779	
Front-End Cost	$1.423	88.7%	$1.416	88.7%	$1.409	88.8%
BE : Probe Test	$0.043	2.7%	$0.043	2.7%	$0.043	2.7%
BE : Dicing Cost	$0.012	0.8%	$0.012	0.8%	$0.012	0.8%
BE : Yield losses	$0.098	6.1%	$0.097	6.1%	$0.095	6.0%
Die Cost	**$1.604**	**98%**	**$1.595**	**98%**	**$1.586**	**98%**

By adding the backgrinding, probe test cost and the dicing, the wafer cost ranges from $2,848 to $2,821 according to yield variations.

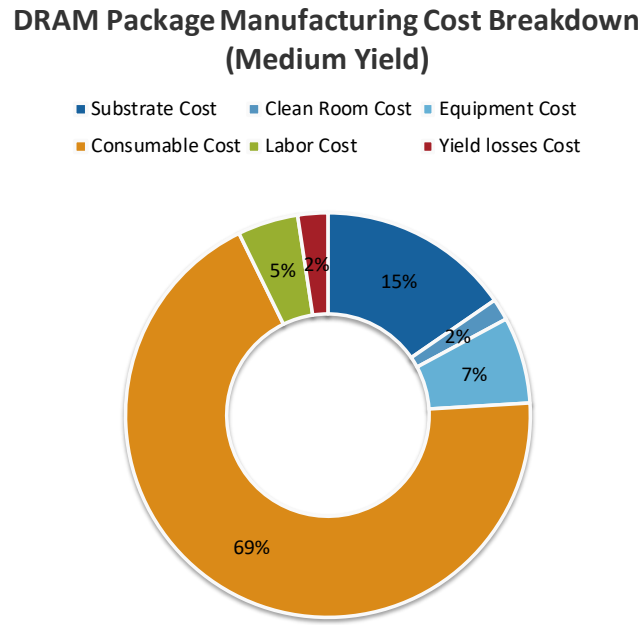
The number of good dies per wafer is estimated to ranges from 1,776 to 1,779 according to yield variations, which results in a die cost ranging from $1.60 to $1.58 between low and high yields.



DRAM Memory : Packaging Cost

	Q4 2020	Q1 2021	Q2 2021
(4) DRAM Dies Cost	$6.416	$6.382	$6.344

Package Manufacturing	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Substrate Cost	$0.1319	15.4%	$0.1319	15.4%	$0.1319	15.4%
Clean Room Cost	$0.0149	1.7%	$0.0149	1.7%	$0.0149	1.7%
Equipment Cost	$0.0593	6.9%	$0.0593	6.9%	$0.0593	6.9%
Consumable Cost	$0.5890	68.7%	$0.5890	68.7%	$0.5890	68.7%
Labor Cost	$0.0415	4.8%	$0.0415	4.8%	$0.0415	4.8%
Yield losses Cost	$0.0207	2.4%	$0.0206	2.4%	$0.0205	2.4%
Package Manufacturing Cost	**$0.857**	**100%**	**$0.857**	**100%**	**$0.857**	**100%**



Packaging includes the 4 DRAM memory dies of 8Gb each. The packaging cost is estimated to be $0.85 between low and high yield.

The package substrate accounts for 15% of the package total cost in medium yield.

Consumables account for 69% of total package cost in medium yield.

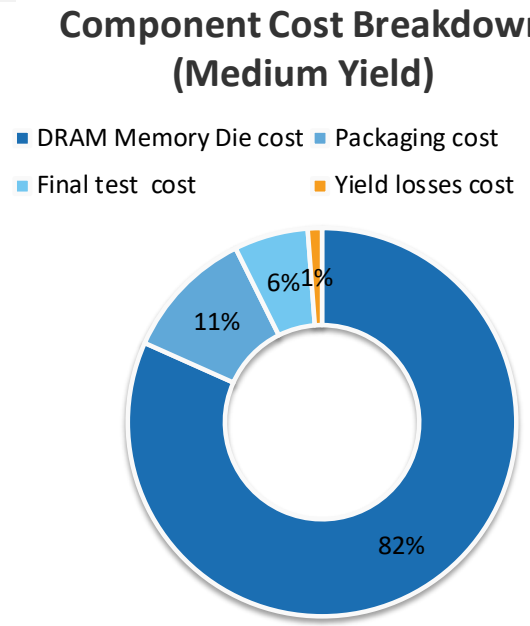
DRAM Memory Component Cost (4GB)

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
DRAM Memory Die cost	$6.416	81.8%	$6.382	81.7%	$6.344	81.6%
Packaging cost	$0.857	10.9%	$0.857	11.0%	$0.857	11.0%
Final test cost	$0.481	6.1%	$0.481	6.2%	$0.481	6.2%
Yield losses cost	$0.093	1.2%	$0.092	1.2%	$0.092	1.2%
Component Cost	**$7.847**	**100%**	**$7.812**	**100%**	**$7.774**	**100%**

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Component cost	**$7.85**		**$7.81**		**$7.77**	
SK Hynix Estimated Gross Profit	$8.10	+51%	$8.14	+51%	$8.18	+51%
	$15.95		**$15.95**		**$15.95**	

The DRAM 4GB/ 32Gb component cost ranges from $7.84 to $7.77 according to yield variations.

- The memory dies represent 82% of the component cost.
- The packaging represents 11% of the component cost.
- Final test and yield losses account for 7% of the component cost.
- (4GB/ 32Gb) LPDDR4 DRAM Memory market price is estimated to be between $15.95 in Q1 2021.



Embedded Die Packaging Cost

Module Parameters	
Module Length	27.50
Module Width	23.10

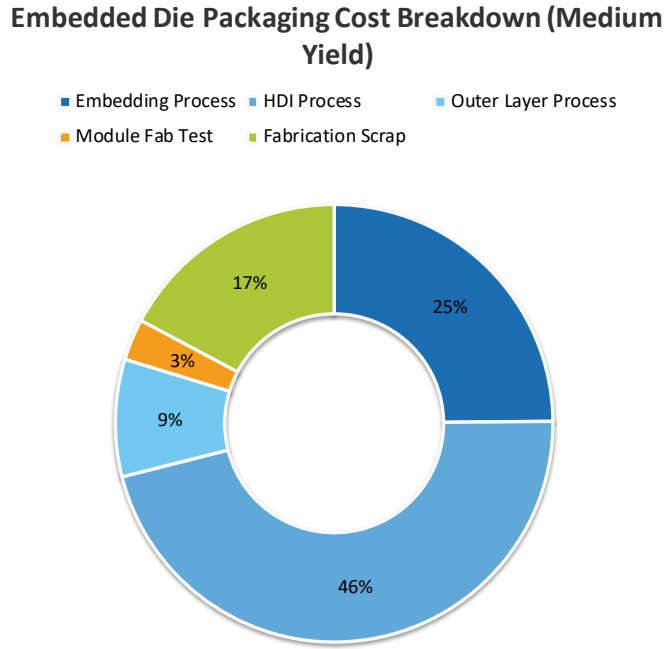
Panel Parameters (335mm x 340mm Panel)		
Panel Width	13.0 inch	330 mm
Panel Length	13.4 inch	340 mm

Silicon Capacitor Die Price (x6)	$47.376		$47.376		$47.376	

Embedded Die Package	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Embedding Process	$122.01	21.1%	$122.01	24.9%	$122.01	29.4%
HDI Process	$226.75	39.3%	$226.75	46.2%	$226.75	54.7%
Outer Layer Process	$42.53	7.4%	$42.53	8.7%	$42.53	10.3%
Module Fab Test	$15.00	2.6%	$15.00	3.1%	$15.00	3.6%
Fabrication Scrap	$170.72	29.6%	$84.50	17.2%	$8.37	2.0%
Embedded Die Process Cost per Panel	**$577.01**	**100%**	**$490.79**	**100%**	**$414.66**	**100%**
Nb Modules per Panel	168		168		168	
Embedded Die Process Cost per Module	**$3.435**		**$2.921**		**$2.468**	
OSAT Gross Profit	$0.859	+20.0%	$0.730	+20.0%	$0.617	+20.0%
Embedded Die Process Price per Module	**$4.293**		**$3.652**		**$3.085**	

The embedded die package cost per panel ranges from $577 to $414 between low and high yield. (panel size of *335mm x340mm)*.

- The number of modules per panel is estimated to be 168 between low and high yields.
- This results in embedded die process cost per module ranging from $3.43 and $2.46 between low and high yields.
- We estimate a 20% gross margin for the OSAT.
- The embedded die process price per module is estimated at $4.29 in low yields and $3.08 in high yields.



Embedded Die Packaging Steps Cost

Embedded Die Embedded Die Packaging		
Operation name	Step Cost (USD/Panel)	BreakDown
Embedding Process - Cleaning	$1.43	0.37%
Embedding Process - Lamination Preparation	$0.32	0.08%
Embedding Process - Lamination 15µm Cu	$4.96	1.27%
Embedding Process - Dicing the edges	$0.09	0.02%
Embedding Process - Cleaning	$1.43	0.37%
Embedding Process - Thickness control	$0.45	0.12%
Embedding Process - Laser drilling 40 µm	$0.98	0.25%
Embedding Process - CO2 laser desmear	$1.29	0.33%
Embedding Process - Laser drilling 40 µm	$0.98	0.25%
Embedding Process - CO2 laser desmear	$1.29	0.33%
Embedding Process - Cu electroless plating 1µm	$2.58	0.66%
Embedding Process - Photoresist Deposition	$0.17	0.04%
Embedding Process - Photoresist exposure	$0.60	0.15%
Embedding Process - Photoresist Developing	$2.23	0.57%
Embedding Process - Cu electroplating	$14.19	3.63%
Embedding Process - Photoresist stripping	$0.75	0.19%
Embedding Process - Copper Etching	$4.21	1.08%
Embedding Process - Cleaning	$1.36	0.35%
Embedding Process - AOI inspection	$4.32	1.10%
Embedding Process - Laser Cutting	$4.38	1.12%
Embedding Process - CO2 laser desmear	$1.29	0.33%
Embedding Process - Lamination Preparation	$0.32	0.08%
Embedding Process - Resin lamination	$22.03	5.63%
Embedding Process - Die Bonding	$26.34	6.73%
Embedding Process - Resin lamination	$22.05	5.64%
Embedding Process - Dicing the edges	$0.09	0.02%
Embedding Process - Cleaning	$1.43	0.37%
Embedding Process - Thickness control	$0.45	0.12%
HDI Process - Laser drilling 40 µm	$2.45	0.63%
HDI Process - CO2 laser desmear	$1.29	0.33%
HDI Process - Laser drilling 40 µm	$2.45	0.63%
HDI Process - CO2 laser desmear	$1.29	0.33%
HDI Process - Cu electroless plating 1µm	$2.58	0.66%
HDI Process - Photoresist Deposition	$2.06	0.53%
HDI Process - Photoresist exposure	$0.60	0.15%
HDI Process - Photoresist Developing	$2.23	0.57%
HDI Process - Cu electroplating	$14.19	3.63%
HDI Process - Photoresist stripping	$0.75	0.19%
HDI Process - Copper Etching	$4.21	1.08%
HDI Process - Cleaning	$1.36	0.35%
HDI Process - AOI inspection	$4.32	1.10%
HDI Process - Lamination Preparation	$0.32	0.08%
HDI Process - Resin lamination	$22.03	5.63%
HDI Process - Dicing the edges	$0.09	0.02%
HDI Process - Cleaning	$1.43	0.37%
HDI Process - Thickness control	$0.45	0.12%
HDI Process - Laser drilling 40 µm	$2.45	0.63%

Embedded Die Packaging Steps Cost

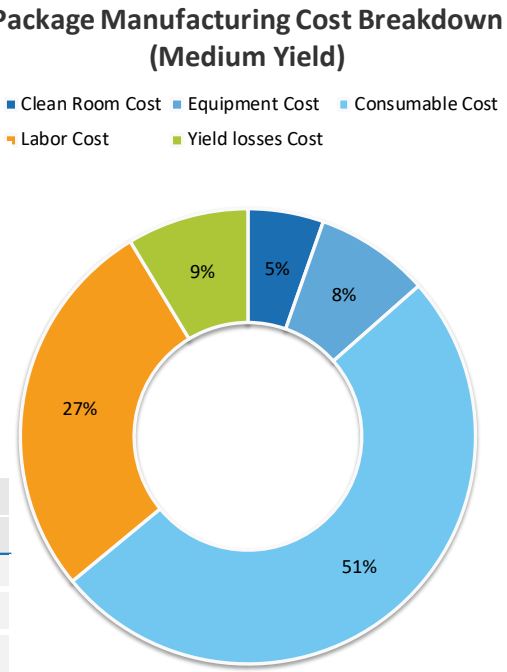
HDI Process - CO2 laser desmear	$1.29	0.33%
HDI Process - Laser drilling 40 µm	$2.45	0.63%
HDI Process - CO2 laser desmear	$1.29	0.33%
HDI Process - Cu electroless plating 1µm	$2.58	0.66%
HDI Process - Photoresist Deposition	$2.06	0.53%
HDI Process - Photoresist exposure	$0.60	0.15%
HDI Process - Photoresist Developing	$2.23	0.57%
HDI Process - Cu electroplating	$14.19	3.63%
HDI Process - Photoresist stripping	$0.75	0.19%
HDI Process - Copper Etching	$4.21	1.08%
HDI Process - Cleaning	$1.36	0.35%
HDI Process - AOI inspection	$4.32	1.10%
HDI Process - Lamination Preparation	$0.32	0.08%
HDI Process - Resin lamination	$22.03	5.63%
HDI Process - Dicing the edges	$0.09	0.02%
HDI Process - Cleaning	$1.43	0.37%
HDI Process - Thickness control	$0.45	0.12%
HDI Process - Laser drilling 40 µm	$2.45	0.63%
HDI Process - CO2 laser desmear	$1.29	0.33%
HDI Process - Laser drilling 40 µm	$2.45	0.63%
HDI Process - CO2 laser desmear	$1.29	0.33%
HDI Process - Cu electroless plating 1µm	$2.58	0.66%
HDI Process - Photoresist Deposition	$2.06	0.53%
HDI Process - Photoresist exposure	$0.60	0.15%
HDI Process - Photoresist Developing	$2.23	0.57%
HDI Process - Cu electroplating	$14.19	3.63%
HDI Process - Photoresist stripping	$0.75	0.19%
HDI Process - Copper Etching	$4.21	1.08%

HDI Process - Cleaning	$1.36	0.35%
HDI Process - AOI inspection	$4.32	1.10%
HDI Process - Lamination Preparation	$0.32	0.08%
HDI Process - Resin lamination	$22.03	5.63%
HDI Process - Dicing the edges	$0.09	0.02%
HDI Process - Cleaning	$1.43	0.37%
HDI Process - Thickness control	$0.45	0.12%
HDI Process - Laser drilling 40 µm	$2.45	0.63%
HDI Process - CO2 laser desmear	$1.29	0.33%
HDI Process - Laser drilling 40 µm	$2.45	0.63%
HDI Process - CO2 laser desmear	$1.29	0.33%
HDI Process - Cu electroless plating 1µm	$2.33	0.60%
HDI Process - Photoresist Deposition	$2.08	0.53%
HDI Process - Photoresist exposure	$0.35	0.09%
HDI Process - Photoresist Developing	$2.14	0.55%
HDI Process - Cu electroplating	$11.43	2.92%
HDI Process - Photoresist stripping	$0.65	0.17%
HDI Process - Copper Etching	$4.12	1.05%
HDI Process - Cleaning	$1.37	0.35%
HDI Process - AOI inspection	$2.50	0.64%
Outer Layer Process - Solder Mask - Cleaning	$1.44	0.37%
Outer Layer Process - Solder Mask - LPI Deposition	$1.36	0.35%
Outer Layer Process - Solder Mask - LPI exposure	$1.11	0.28%
Outer Layer Process - Solder Mask - LPI Developing	$0.60	0.15%
Outer Layer Process - Board Routing	$2.23	0.57%
Outer Layer Process - Electrical test	$0.71	0.18%
Outer Layer Process - ENIG Finishing	$0.54	0.14%
Outer Layer Process - AOI inspection	$33.15	8.47%
Outer Layer Process - Depaneling	$1.39	0.36%
Total	**$391.29**	**100%**

Packaging Cost

	Low Yield	Medium Yield	High Yield
Apple M1 Die Cost	$31.979	$29.808	$27.720
DRAM Component Price	$31.900	$30.660	$31.560
Embedded Die Packaging Price	$4.293	$3.652	$3.085
Embedded Capacitors (x6) Cost	$0.282	$0.282	$0.282
SMD Capacitor (x24)Cost	$0.112	$0.112	$0.112
Silicon Capacitor (x4) Cost	$0.124	$0.120	$0.116
IHS Cost	$0.045	$0.045	$0.045

Package Manufacturing	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Clean Room Cost	$0.0824	5.1%	$0.0824	5.4%	$0.0824	5.6%
Equipment Cost	$0.1245	7.7%	$0.1245	8.1%	$0.1245	8.5%
Consumable Cost	$0.7736	48.0%	$0.7736	50.5%	$0.7736	52.9%
Labor Cost	$0.4186	26.0%	$0.4186	27.3%	$0.4186	28.6%
Yield losses Cost	$0.2110	13.1%	$0.1324	8.6%	$0.0644	4.4%
Package Manufacturing Cost	**$1.610**	**100%**	**$1.531**	**100%**	**$1.463**	**100%**
OSAT Gross Profit	$0.4025	+20.0%	$0.3828	+20.0%	$0.3658	+20.0%
Package Manufacturing Price	**$2.013**		**$1.914**		**$1.829**	



The Packaging cost for the M1 SoC Package includes the assembly of Apple M1 SoC Die, 2 DRAM Memory Packages, 4 Silicon Capacitors ,24 SMD Capacitors and 6 silicon capacitors embedded in the Package PCB.

The Package Manufacturing cost ranges from $1.61 in low yield and $1.46 in high yields.

- Consumables accounts for 51% of total package cost in medium yield.
- Labor accounts for 27% of total package cost in medium yield.
- Equipment account for 8% of total package cost in medium yield

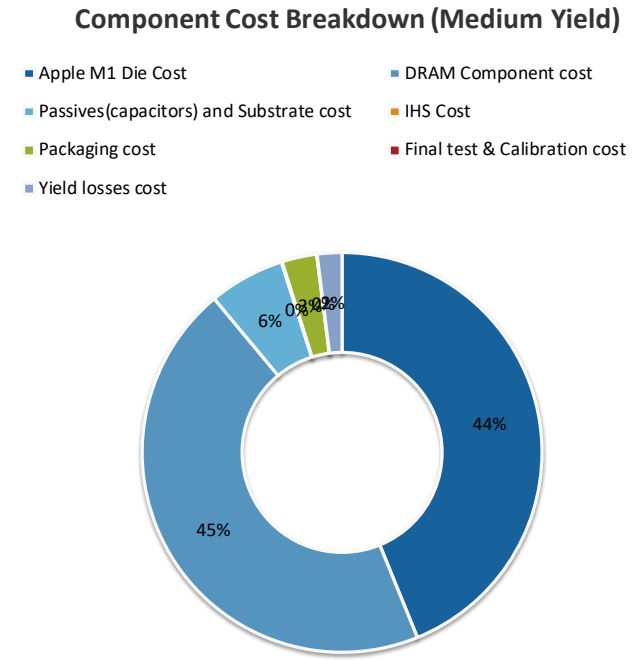
We estimate 20% for the OSAT Gross profit which results in the packaging price ranging from $2.01 to $1.83 between low and high yield.

M1 SoC Component Cost

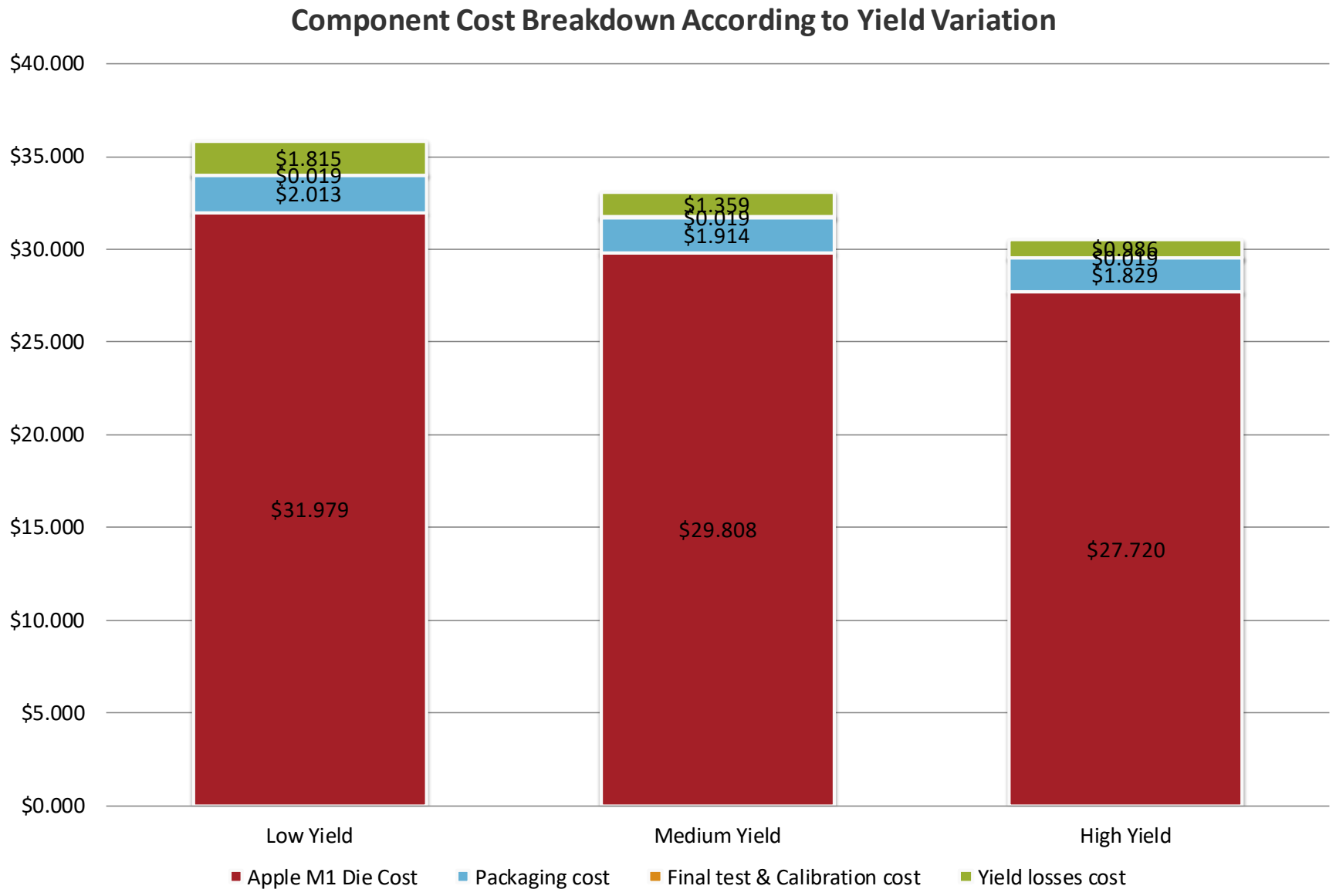
	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Apple M1 Die Cost	$31.979	44.1%	$29.808	43.9%	$27.720	42.2%
DRAM Component cost	$31.900	44.0%	$30.660	45.1%	$31.560	48.0%
Passives(capacitors) and Substrate cost	$4.811	6.6%	$4.166	6.1%	$3.595	5.5%
IHS Cost	$0.045	0.1%	$0.045	0.1%	$0.045	0.1%
Packaging cost	$2.013	2.8%	$1.914	2.8%	$1.829	2.8%
Final test & Calibration cost	$0.019	0.0%	$0.019	0.0%	$0.019	0.0%
Yield losses cost	$1.815	2.5%	$1.359	2.0%	$0.986	1.5%
Component Cost	**$72.581**	**100%**	**$67.971**	**100%**	**$65.755**	**100%**

The M1 SoC Component cost ranges between $72.58 in low yield to $65.75 in high yield.

- The Apple M1 SoC die represent 44% of the component cost.
- The DRAM Memory Component represents 45% of the component cost.
- Passive components and substrate cost account for 6% of the component cost.
- Final Test, calibration and yield cost account for 5% of the component cost.



M1 SoC Component Cost



SELLING PRICE

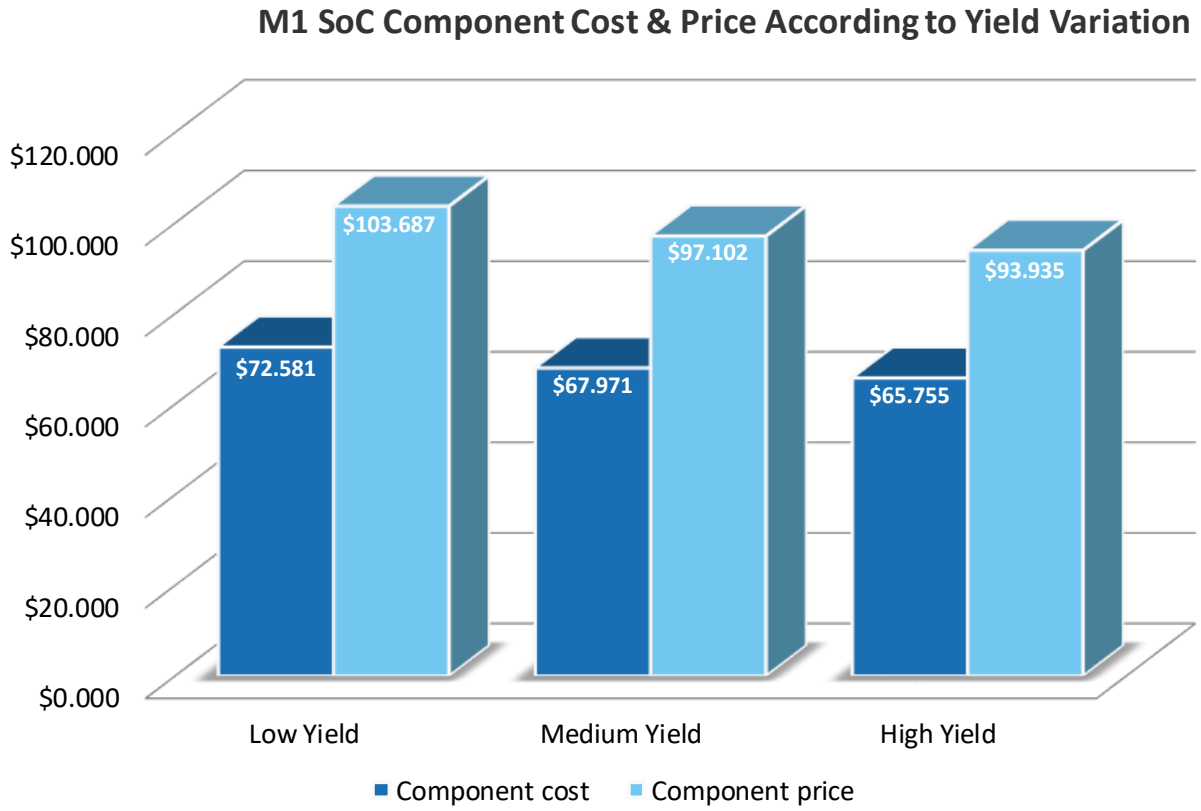
M1 SoC Component Price

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Component cost	**$72.581**		**$67.971**		**$65.755**	
Apple Gross Profit	$31.106	+30%	$29.131	+30%	$28.181	+30%
Component price	**$103.687**		**$97.102**		**$93.935**	

Apple Semiconductor	
Gross Margin	30.0%

We assume that Apple Semiconductor sells the M1 SoC Component to Apple Computers division.

We estimate an average gross margin of 30% for Apple Semiconductor, which results in the component price ranging from $103.68 to $93.93.



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Feedbacks

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Please note that without any feedback from you, we consider that the report satisfied you.

We appreciate to work with you and want to make sure we meet your expectations.

Sincerely,
System Plus Consulting

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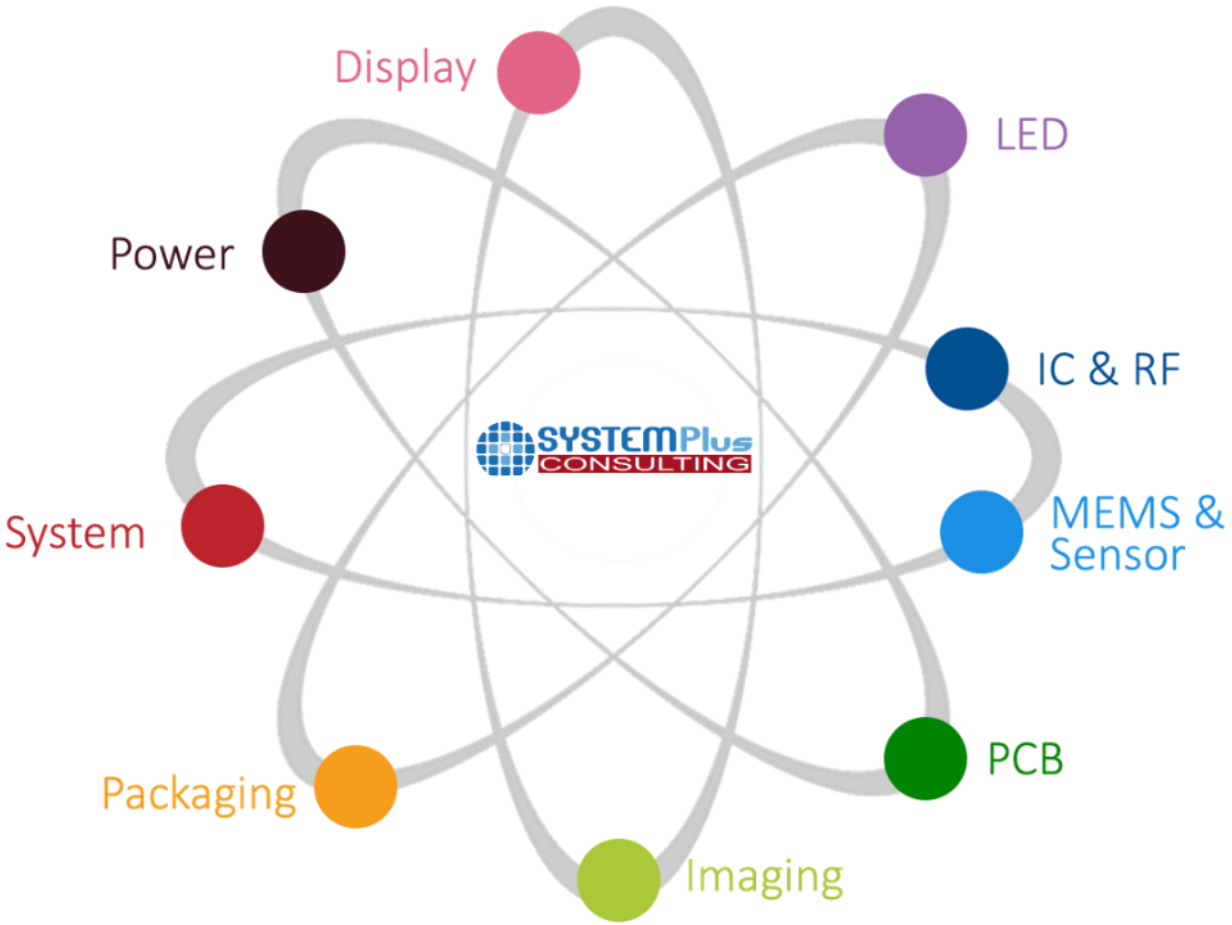

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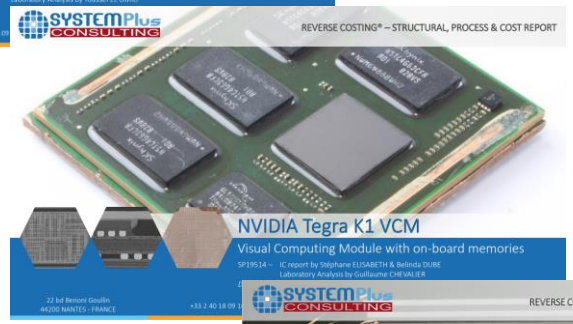

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