ATTD
Competitive
Analysis

Apple MacBook Pro Systems with M1 Pro and M1 Max SoC Analysis

WW10, 2022 Report

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intel®

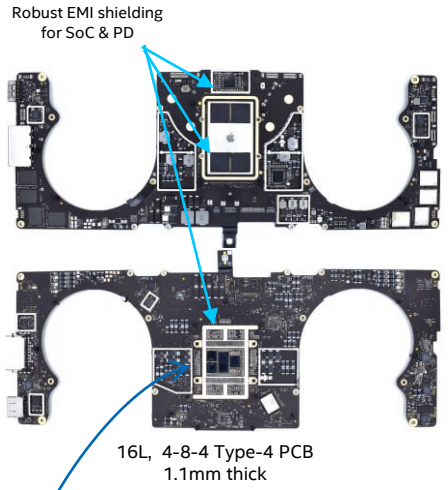
Apple M1 Pro/Max Package Analysis

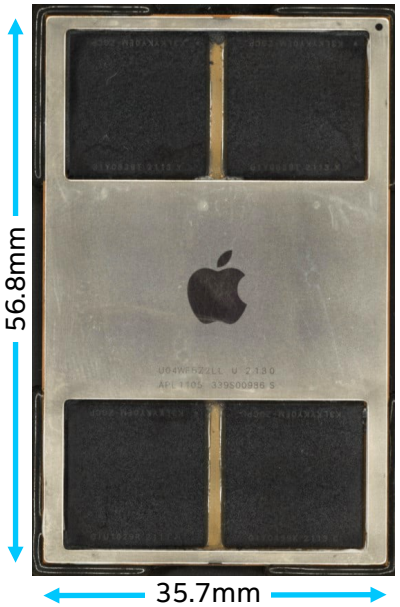
Since the M1 Pro die is a simple chop of the M1 Max and they share packaging materials, etc. Data duplication has been minimized.

- **The M1-Max SoC is comprised of a 19.04 x 22.02mm (419mm²)die on 35.7 x 56.8mm 310um thick 11-layer coreless ETS substrate**. M1 Pro: 19.04x13.3 die/ 24.7x56.8mm substrate.
  - 11-layer coreless ETS substrate, e-less NiPdAu cap on surface layers (pads, dams 2DID mark). No solder resist on FLI side. Assembly may have been done in strip format.
  - Unique girdle shaped Cu pillar bumps at 85 min pitch with Sn (so SnCu) FLI solder, landing on e-less NiPdAu substrate pads .
  - Cu layer thickness ranges from 8-15um. Dielectric layer thickness ranges from 10-18um except ~25um thick due to glass cloth in 2 layers closest to board.
  - Min Line/Space observed is 15/12um single ended routing, 20/35um for differential pairs. 100um round adhesion holes versus the square grid hole pattern used on the M1 and A12X.
  - Substrate and board 3D X-Ray imagery is included. Contact ATTD C/A for access to the full high-resolution images.
- The MacBook Pro 14" M1-Pro and –Max are built on a 1.1mm thick, 16-layer Type 4 PCB. With exception of more robust RF shielding, construction is typical of MacBook Pros..
- The **M1 Max SoC die is ready for ~770 IO/mm die-to-die interconnect using 25um minimum pitch InFO-L** (silicon bridge embedded in fan out RDL interposer) or similar advanced package technology. A high-density differential IO circuit block along one edge of the SoC was not shown in Apple's press releases. This block is currently populated only with power/ground bumps (at 140um bp) but can provide 756 bytes of die-to-die data transfer (770 IO/mm escape density, not including P/G reference etc.) when connected on a fan out embedded bridge interposer at 25x35um micro-bump pitch, consistent with TSMC's disclosures on InFO-L design rules.
- Similar to M1 MacBook, thermals are managed with a dual-fan cooled heat pipe which penetrates the heat sink to directly contact gray TIM2 (triauryl phosphate with 9um Al and ZnO filler) above the Ni-plated Cu IHS. A black grease-like TIM2 (PDMS with 60um AlOx particles) fills the gap between DRAM packages and the heat sink.. The same grease-like TIM fills the gap between the bottom-side VR components and the EMI shielding. TIM1 is PDMS based, with Al, Si and traces of Zn in filler. PDMS based sealant with Al/Si filler holds it together.
- As mounted on the PCB, the IHS has 72um convex warpage (frowny face) and BGA heights range from 190um to 390um indicating the substrate, stiffener, and IHS combination was marginal and would not meet industry's JEDEC expectations. DFM and reliability was obviously considered when planning the ball map.
  - Warpage is managed with a ~1.3/2mm wide 0.4mm thick nickel-plated stainless steel (Fe/Cr/Mn) stiffener ring around the substrate perimeter with a ~flat plate IHS adhered to the ring. The IHS has cutouts for the LPDDR packages; both 8GB and 16GB DRAMs extend up into the hole, but not above the IHS. DRAMs were attached before stiffener ring covered key fiducials. Assembly was possibly done in strips to support tight stiffener-edge tolerance and manage the in-process warpage. Fiducials near the substrate corners were not noted for stiffener attach.
- 14x14mm (2406 BGAs at 0.27mm) **LPDDR5** packages (Max- 4 pcs, Pro – 2 pcs) are SMT'd to the top of the substrate and underfilled before stiffener ring attach. Our teardown samples had either Samsung 8GB (1Gb 1-y die, 0.65mm Z) or SKHynix 16GB (1-y die, 0.85mm Z). Both suppliers used a 4-layer (coreless/prepreg dielectric) FBGA package.
- M1-Max Power delivery is managed with 3-5 **CMOS voltage regulators with integrated magnetic inductor** power delivery ICs attached to the other side of the main board directly beneath the SOC chip. 34 DTCs and 17 IDCs on 5 CMOS voltage regulator with integrated magnetic inductor IC's are mounted to the board directly beneath the SOC. 10 0.5um thick Cobalt-rich (CZT?) sheets above and below 18um thick copper traces form 28 integrated inductor pairs on the 4.6x5.9mm die. They are attached as 6.8x7.4mm 4-layer coreless exposed die CSP packages with ~0.5mm BGA pitch/BLUF. (3 components on M1-Pro skus). Across the Mi-Pro and M1-Mac there appear to be 5 variants of voltage regulator packages. Each component can support 2 power rails. 34 ~1.7 x 2.3 mm 100um thick / 9um Deep Trench Capacitors are SMT'd on the substrate land side (140um bump pitch). These may be a new design; DTCs used as LSCs on the M1 package had 30um trench depth, embedded caps had 6.8um depth. Additionally, 17 0603 3T Die Side Capacitors are used.

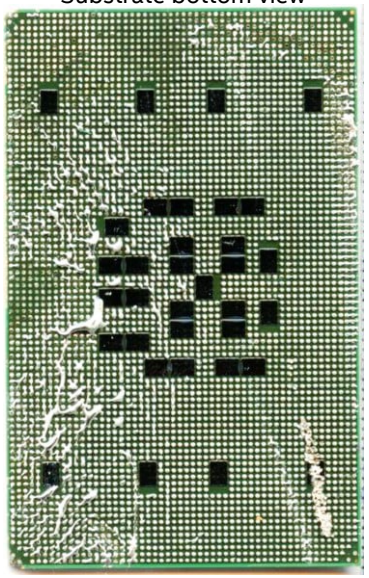
MacBook Pro 16” with Apple M1 Max SoC

Some images courtesy of TMG Si C/A

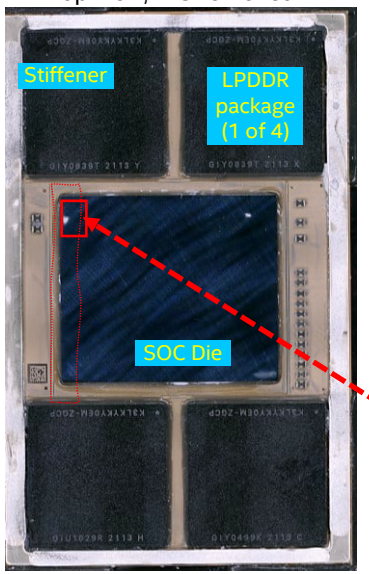


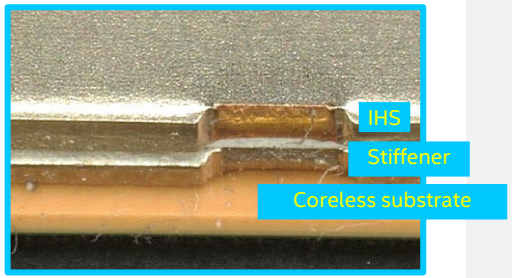


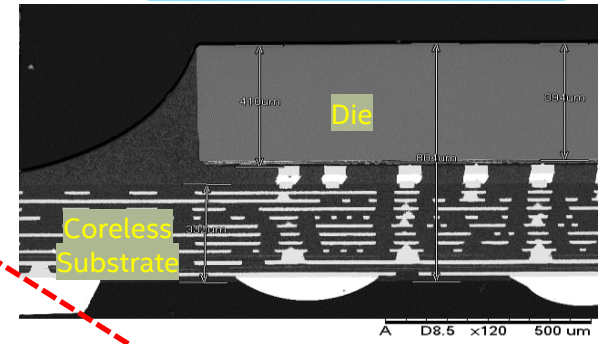
Substrate bottom view



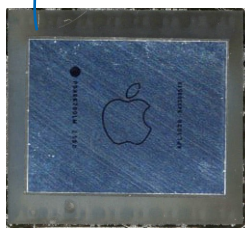
Top view, IHS removed



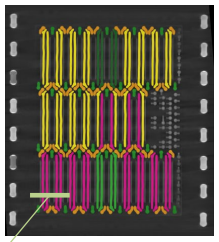




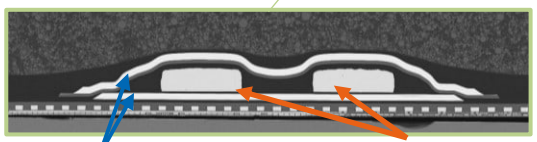
5 Power Delivery ICs
HF VRs w/Mag Inductors



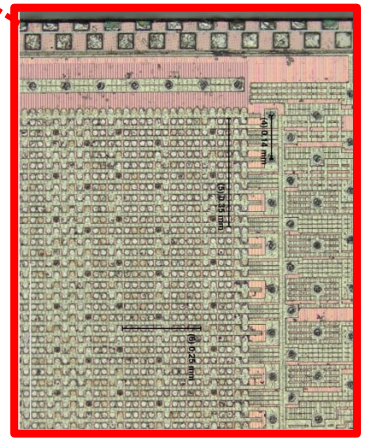
VR Package (3 on M1-Pro)



VR Die Top Metal Layer



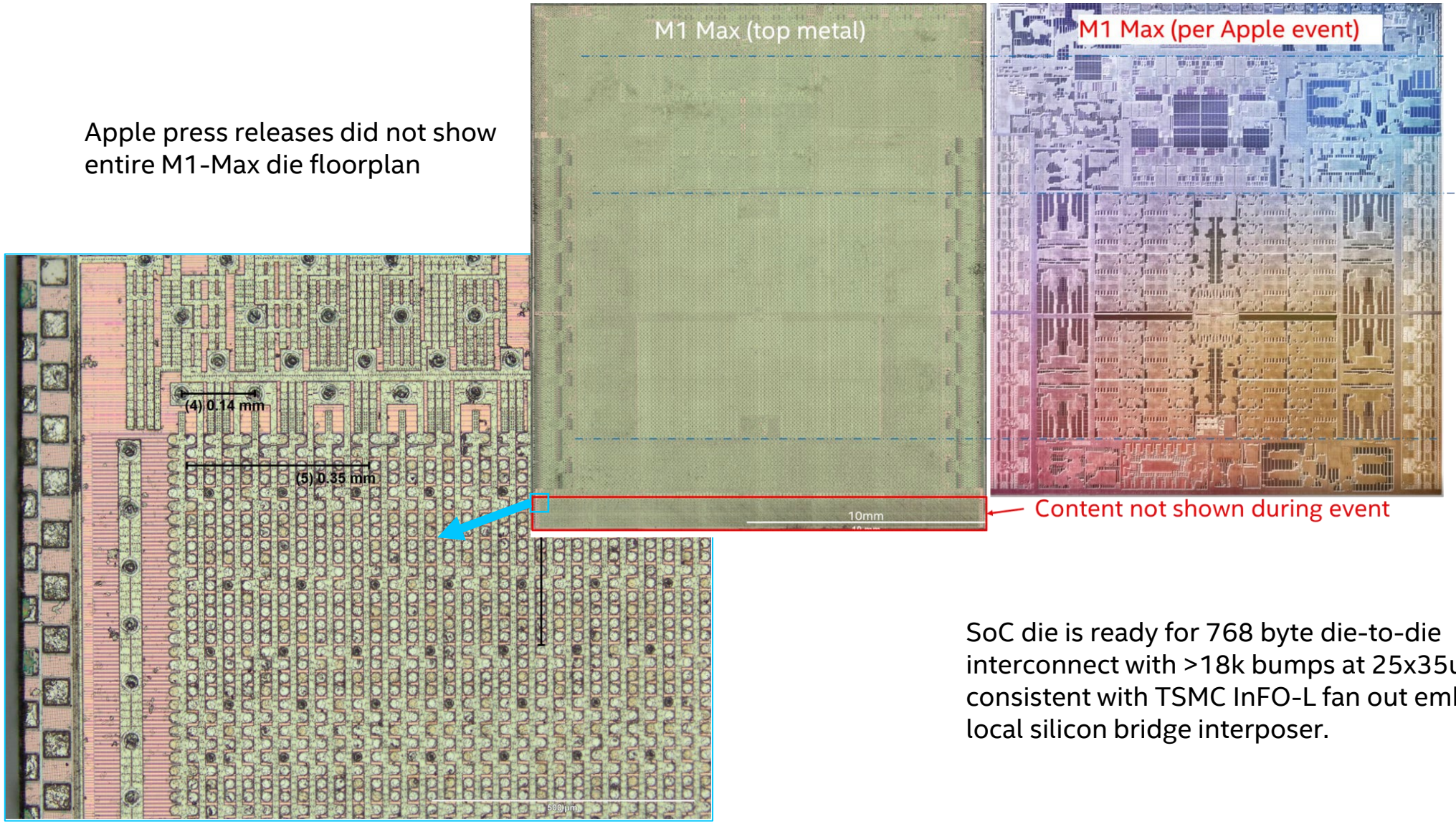
- **56.8 x 35.7mm, 11-layer 300um coreless ETS substrate**
  - Ni-Pd-Au surface Cu (pads, dams, 2DID).
  - 15/12um min L/S, ABF(?) dielectric, 2 bottom layers w/glass cloth.
  - Suspected supplier: UMTC, and possibly AT&S
  - SLI: 0.63mm BGA pitch SAC solder.
- 34-1.7x2.3x0.1mm DTC LSC, 140um bp. 17-0603 3T DSC
- 19x22mm SoC, 85um min bp; 58um Cu pillar/Sn or SnCu FLI solder.
- **4- 14x14mm 8/16GBx128b Samsung/SKHynix 1y LPDDR5 BGAs (0.27mm bp/CUF)**
- Stiffener frame with IHS, IHS cutouts for LPDDR5 packages



Future D2D IO region @ 25um bp (~770 IO/mm)
Forecast: InFO_LSI MCP/ MacPro duo

M1 Max SoC die is prepped for High Density D2D connections

Apple press releases did not show entire M1-Max die floorplan



SoC die is ready for 768 byte die-to-die interconnect with >18k bumps at 25x35um pitch, consistent with TSMC InFO-L fan out embedded local silicon bridge interposer.

Images courtesy of TMG Si C/A team

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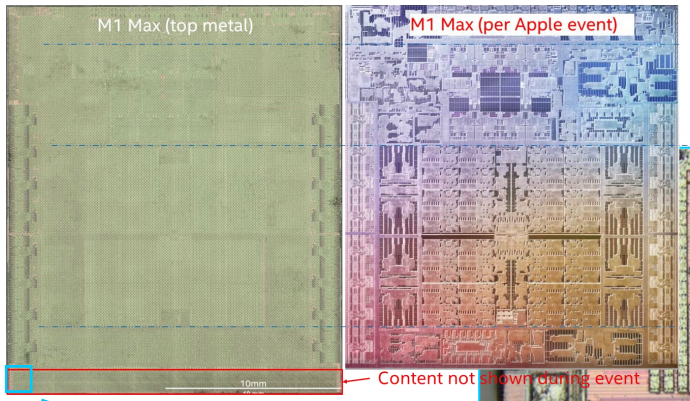

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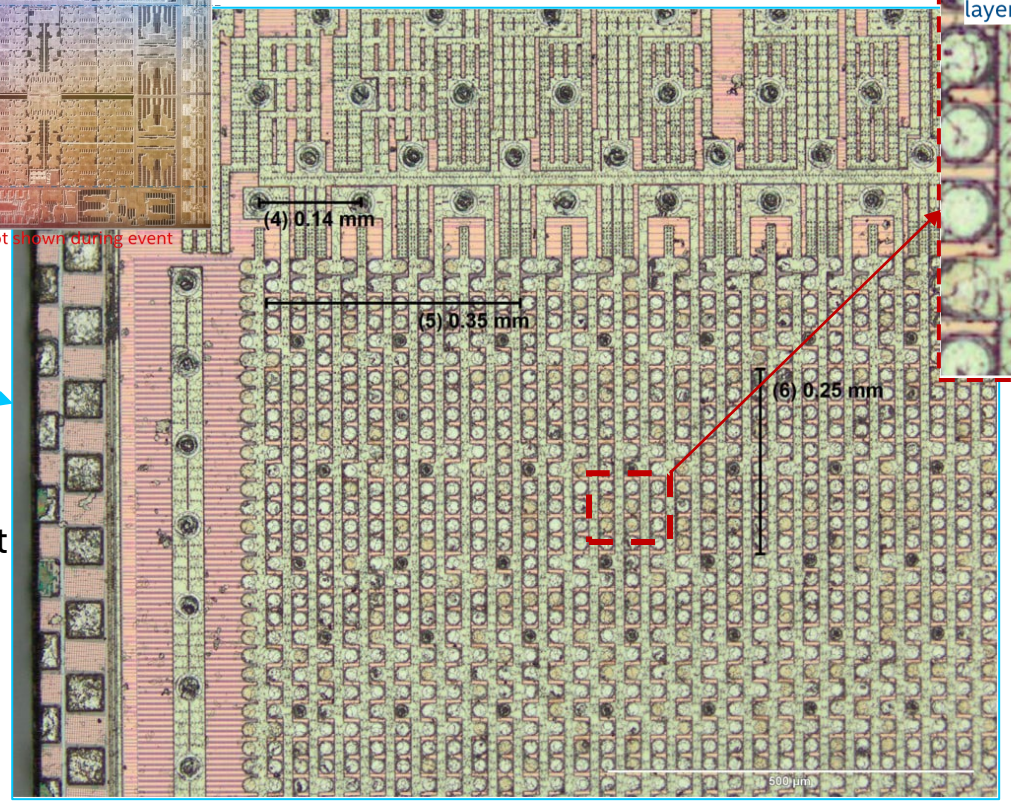
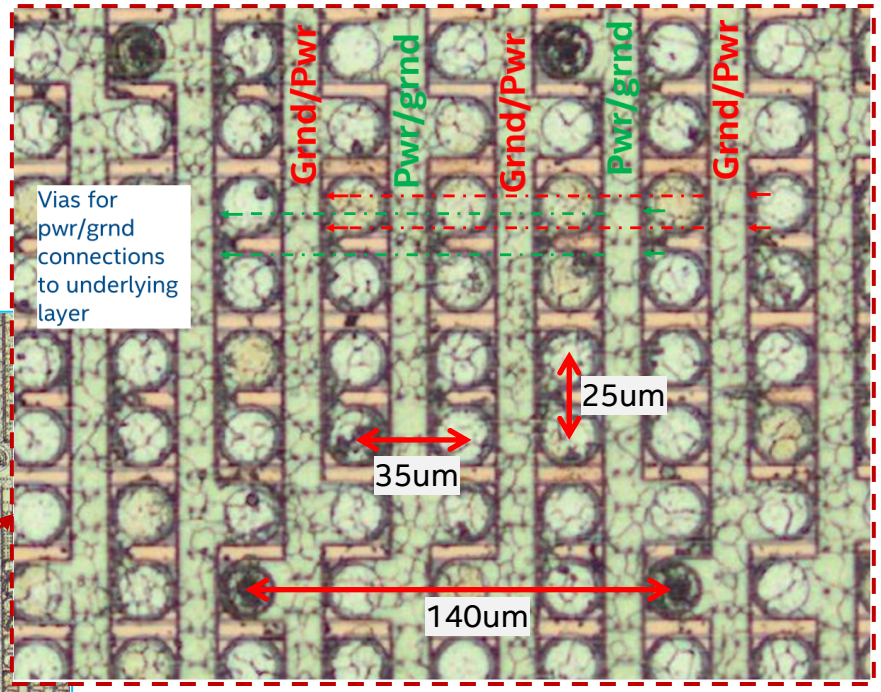


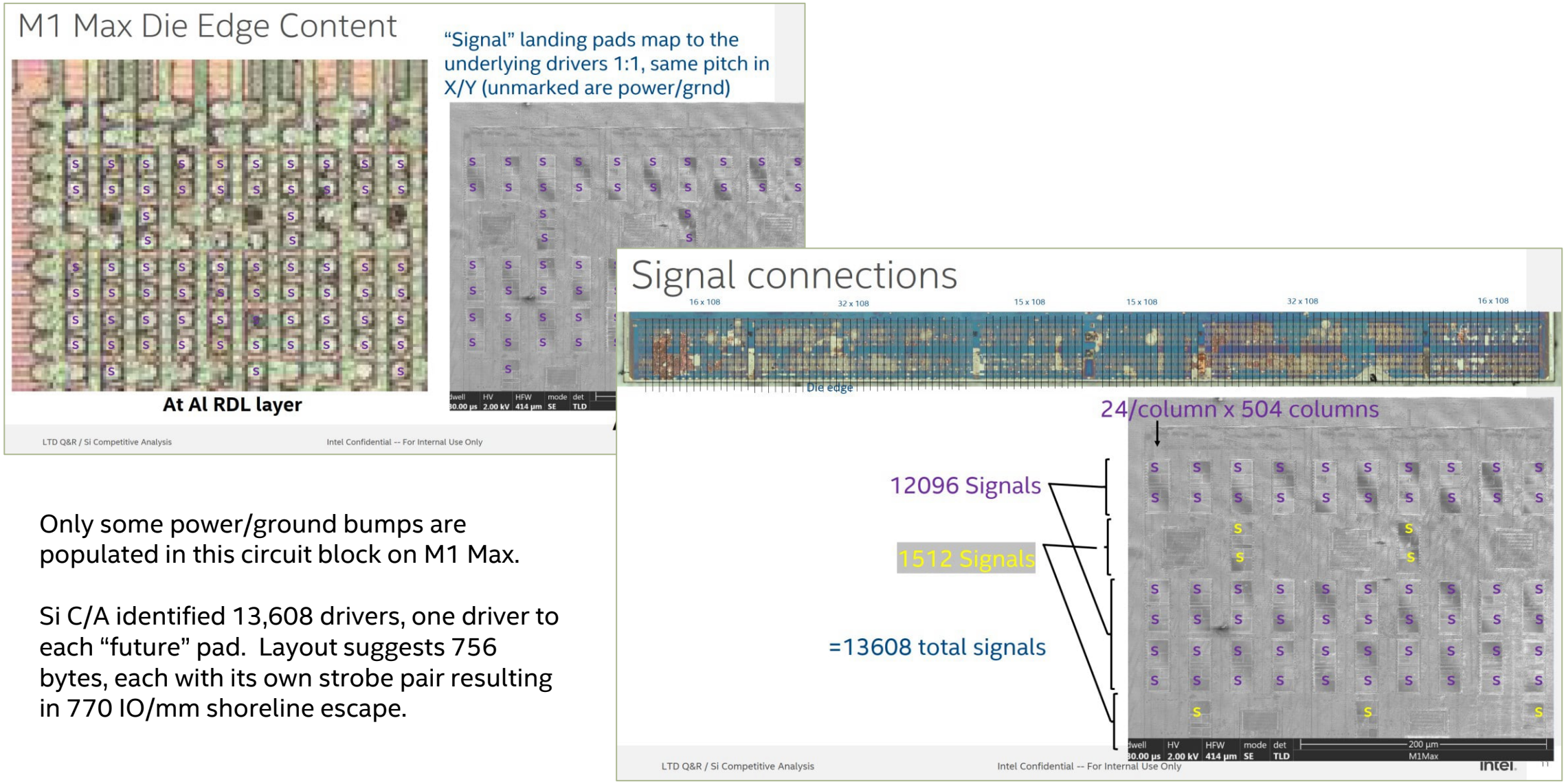


Si C/A identified 13,608 drivers, one driver to most “future” pads. Layout suggests 756 bytes, each with its own strobe pair resulting in 770 IO/mm shoreline escape.

Only some power/ground bumps are populated today in this circuit block on M1 Max; vias connected to bumps are darkened due to exposure to copper bump etchants. Pads for future micro-bump bridge connect are a lighter color.

Images courtesy of TMG Si C/A team

Apple M1 Max Future Die to Die Circuitry



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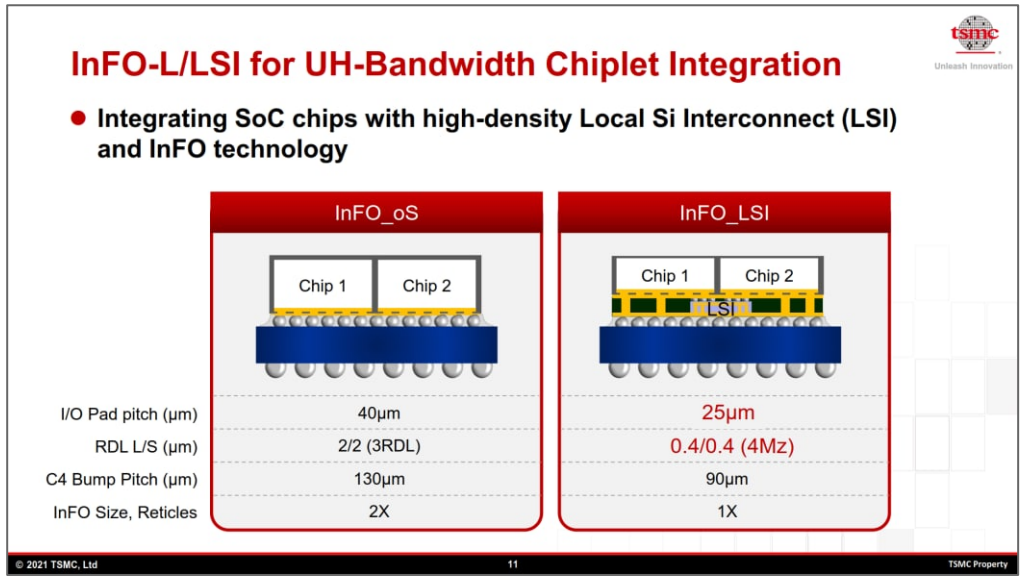
Speculation on M1 Max "Duo" MCP

TSMC's InFO_LSI

- Local Silicon Bridge embedded in chip-first fan out RDL interposer
- Ready 'now' (TSMC 2020 AIP Day: "Qual to complete Q1'21")



57x72mm package

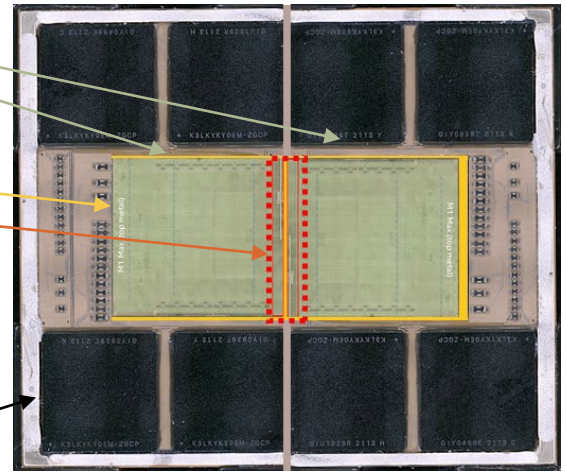
2 M1-Max SOCs
>13k connections on interposer

19x44mm InFO-L (1X R)
18x3mm LSI bridge
~65 gross Interposers/Wafer

Interposer+WLA est price $20-30/ 2-die MCP assuming InFO-L price is $2,000/w

+ 8 LPDDR pkgs
connected thru package

Hypothetical M1 Max "Duo" MCP

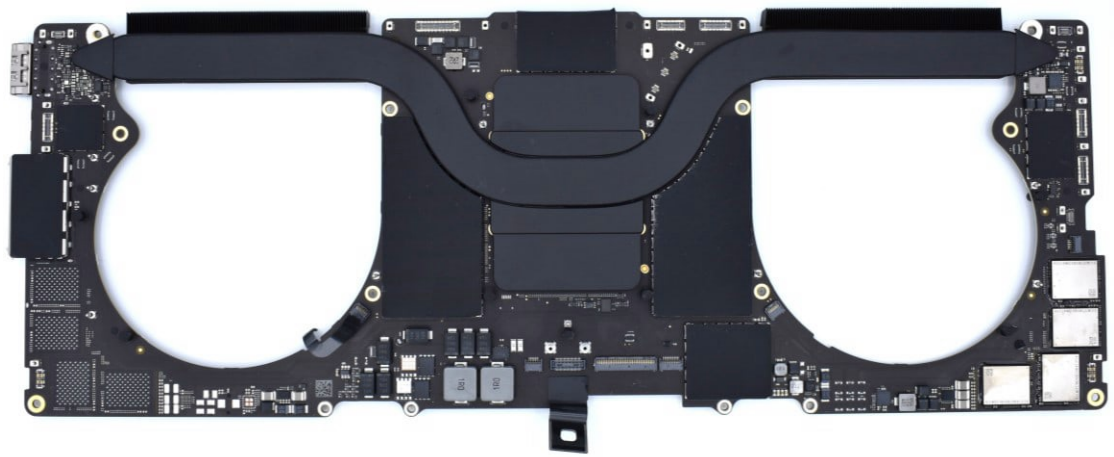


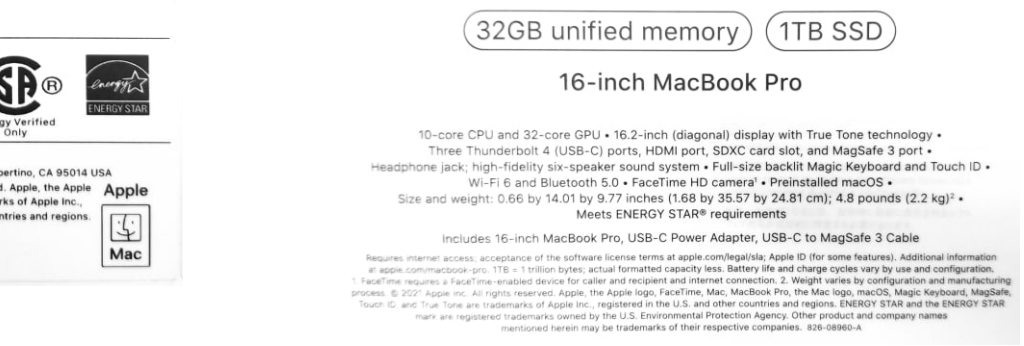
Hypothetical image shown is photo editing, abutting two M1 Max packages together. Substrate warpage would likely make such a construction non-manufacturable. Apple might need to pursue 8-2-8 or PoINT type architecture.

Cost SWAG, not ratified

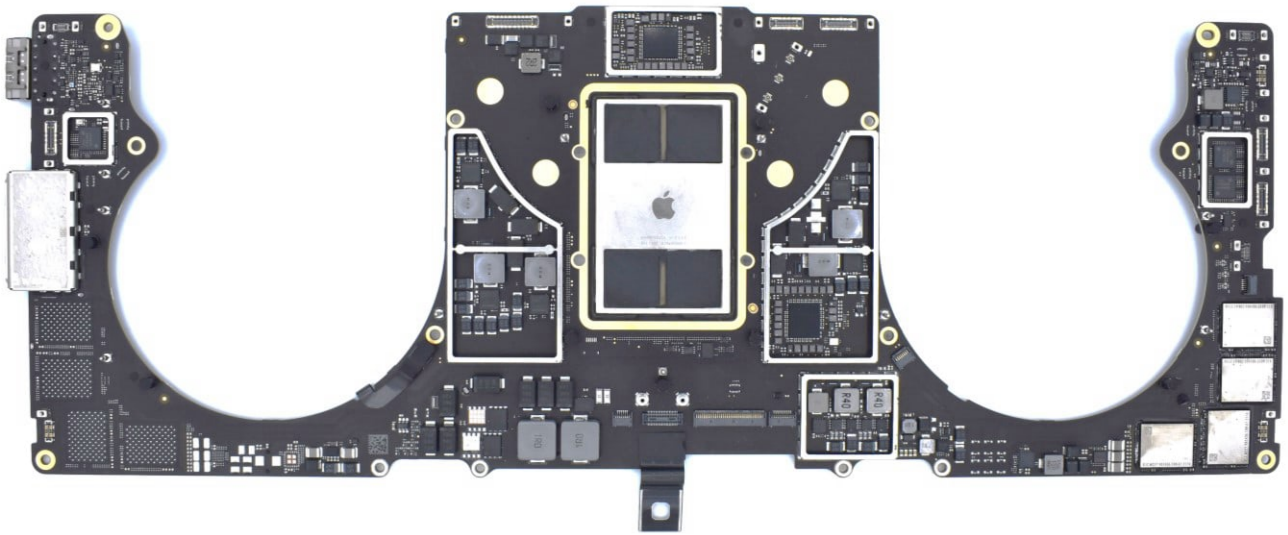
M1 Max die x2	$200
InFO-L	$ 30
Substrate(s)	$ 40+
OSAT	$ 8
LPDDR5 x8	$320
Total	$600+

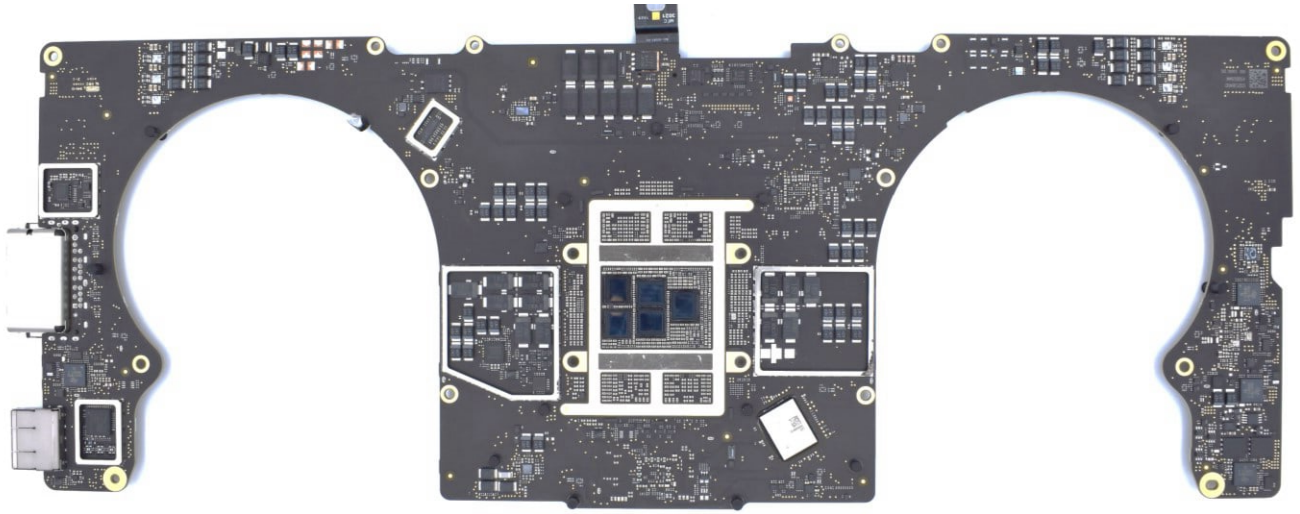
MacBook Pro 16” with Apple M1 Max SoC



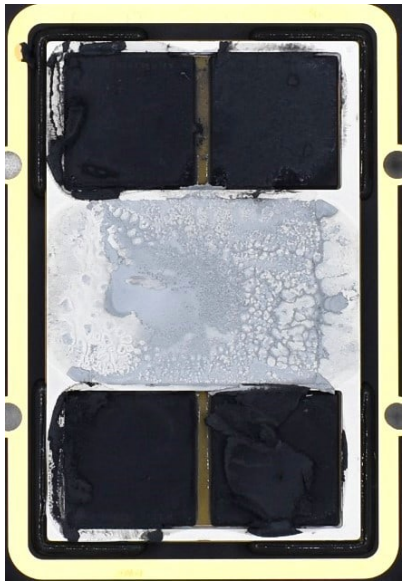


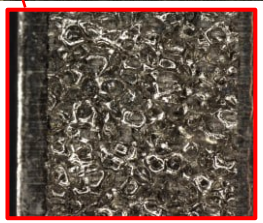
MacBook Pro 16” with Apple M1 Max SoC



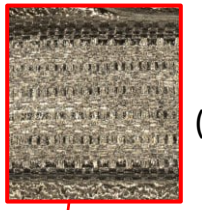


2 types of Thermal Interface Material





Wire mesh
(EMI Shield)



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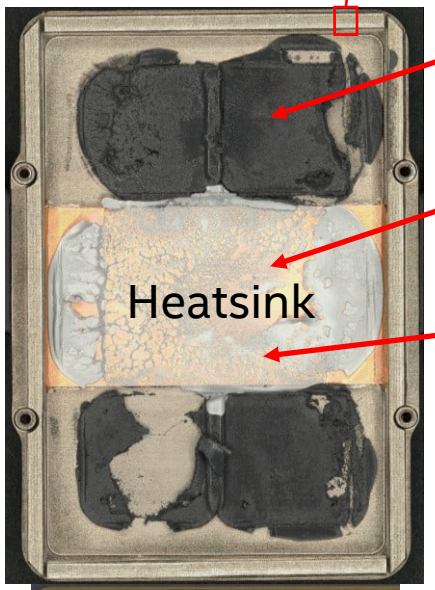
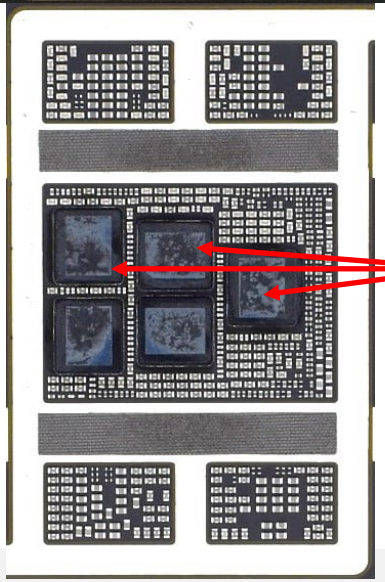


TIM2 above
LPDDRs

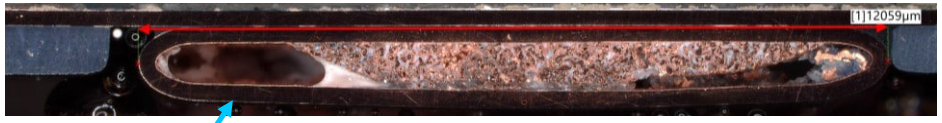
TIM2 above
SoC

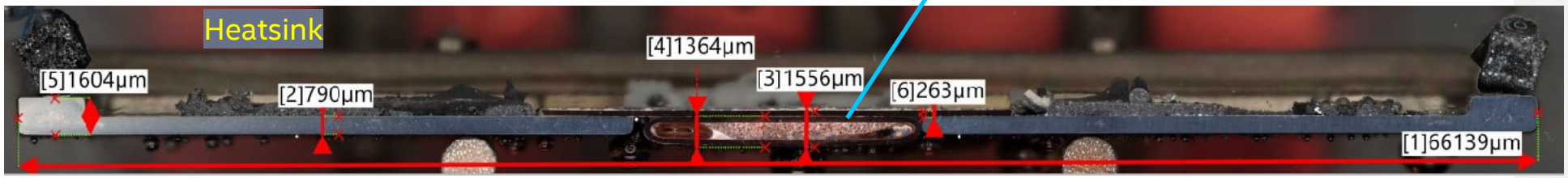
Penetrating
Heat pipe
eliminates
one interface
between IHS
(similar to M1
MacBook Pro)



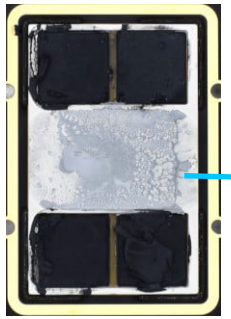
Thermal
Interface Material
to cool 5
Package Voltage
Regulators (PVR)

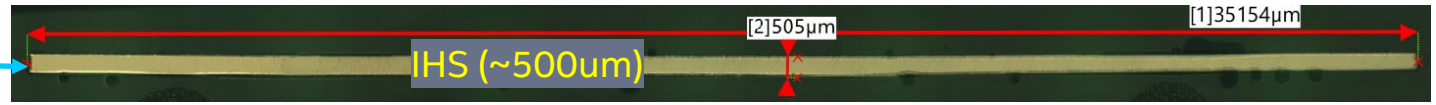
Apple M1 Max X-Sections – Heat Sink/IHS/Stiffener/PVR IHS

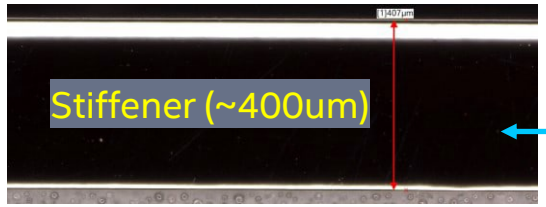


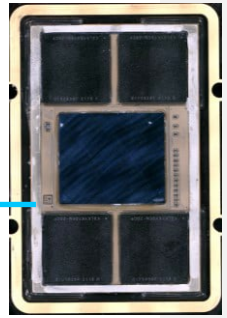


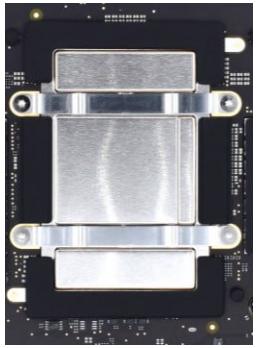
Materials: Heat sink: aluminum body, sintered Cu heat pipe
IHS: Copper
Stiffener Ring: Stainless Steel

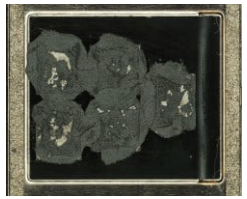


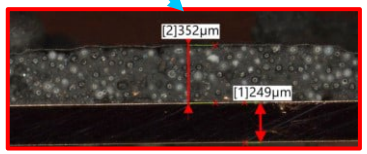


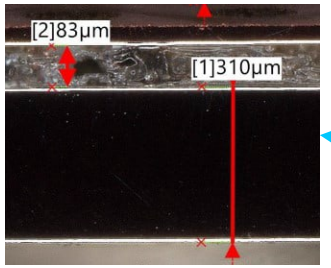


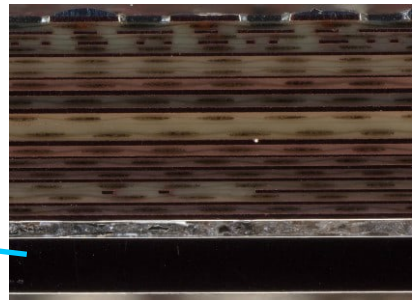


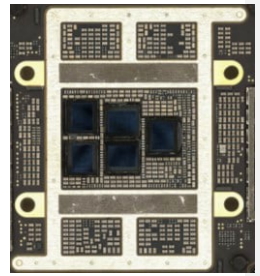








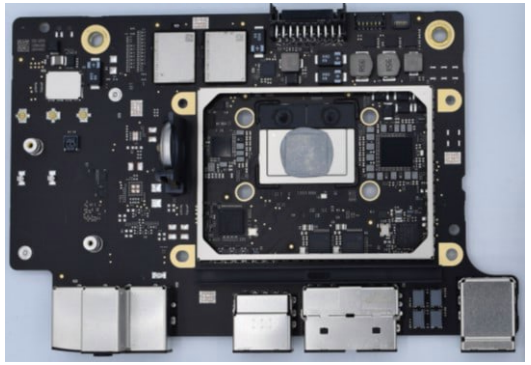




Metal frame
soldered to the board (~310um)

EMI Shielding More Robust vs M1 Mac Mini / MacBook

M1 Mac Mini

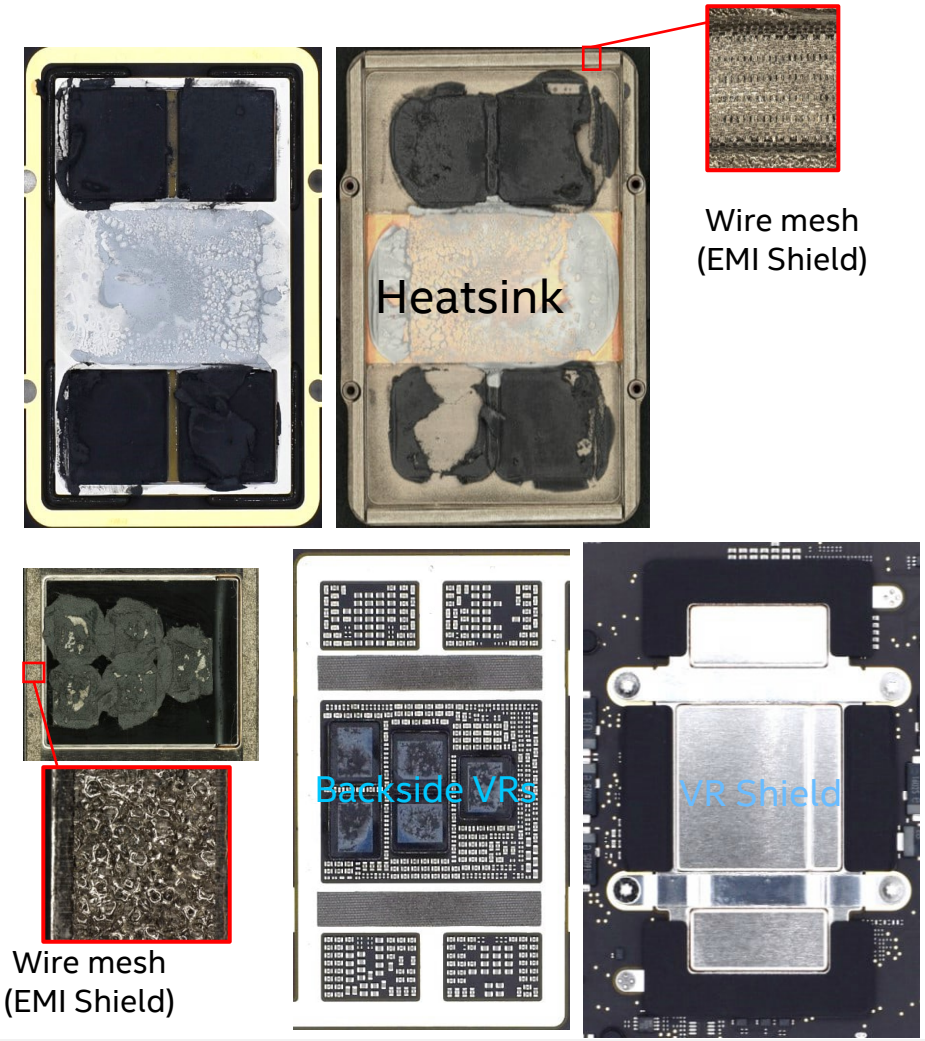


Foam between heat sink edge and board
No shield on board backside

M1 MacBook Pro

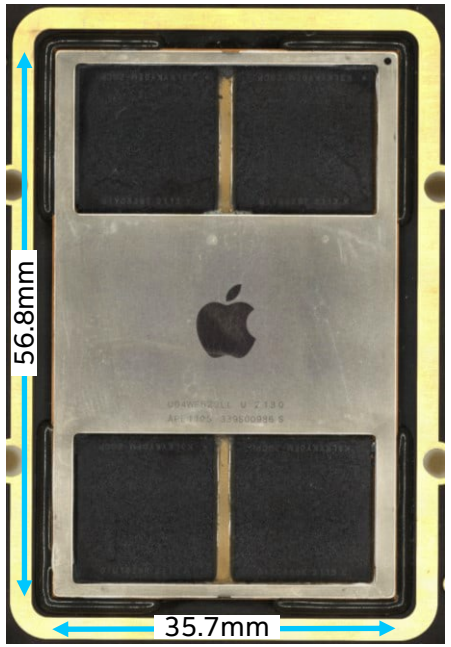
Foam between heat sink edge and board
Mesh between heat sink and IHS foot
No mesh surrounding DRAMs
No shielding on board backside

M1-Max MacBook Pro

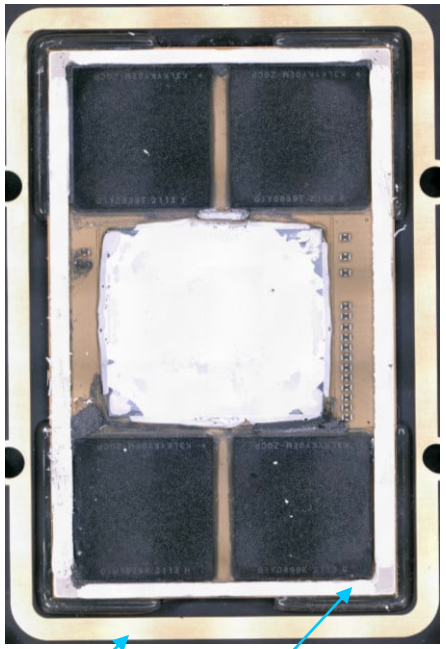


Apple M1 Max SoC

M1 Max
Package Top



M1 Max
Lid Removed



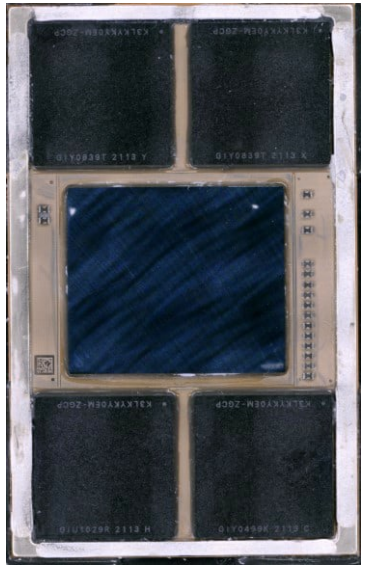
Heat sink/EMI shield contact surface on main board

Stiffener frame
1.3/2.0mm wide
400um thick
Stiffener frame is grounded to substrate

M1 Max
Lid Bottom side

IHS lid is a flat plate with cutouts for LPDDR5 DRAM packages

M1 Max
PTIM cleaned



SoC: 19.04 x 22.02mm die
LPDDR: 14x14mm
17 0603 3T DSCs

M1 Max
Package Bottom

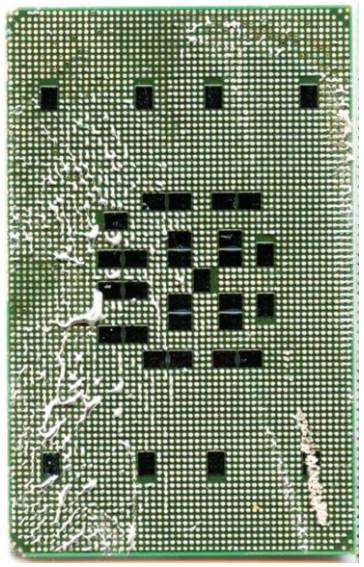
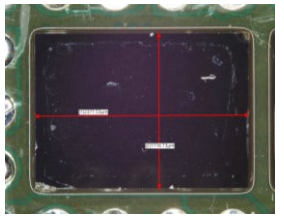


*Image horizontally flipped

- 0.6mm bp BGA qty:
- 34 DTC's, Size = 1.7x2.3x0.1mm



M1 Max
PCB Bottom

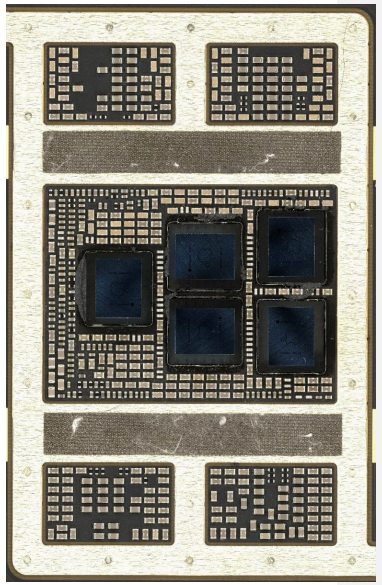
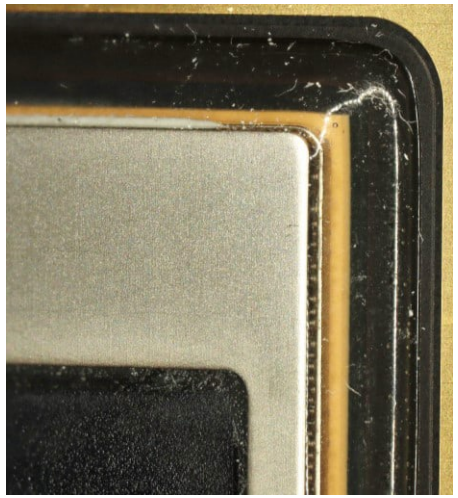
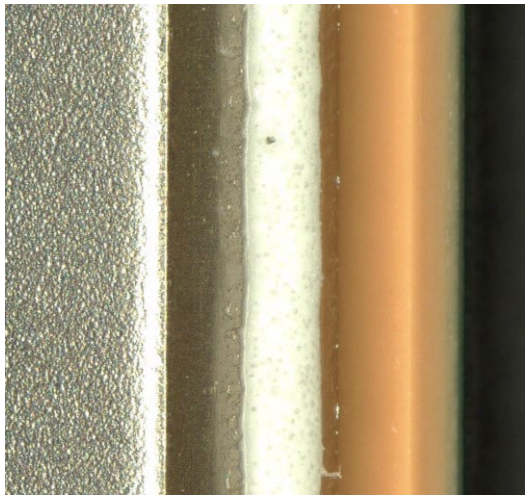


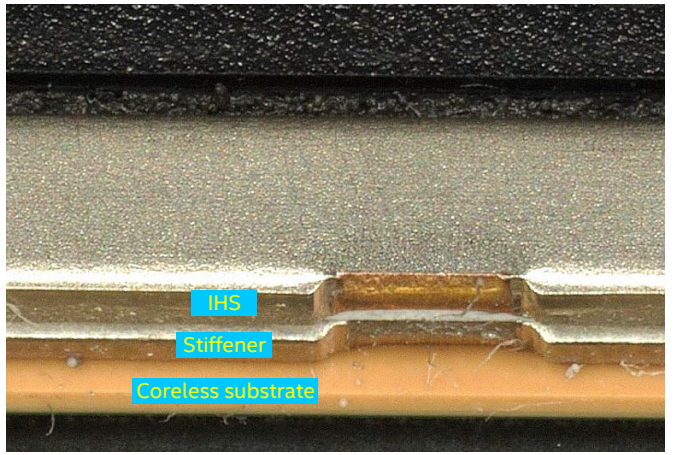
*Image horizontally flipped

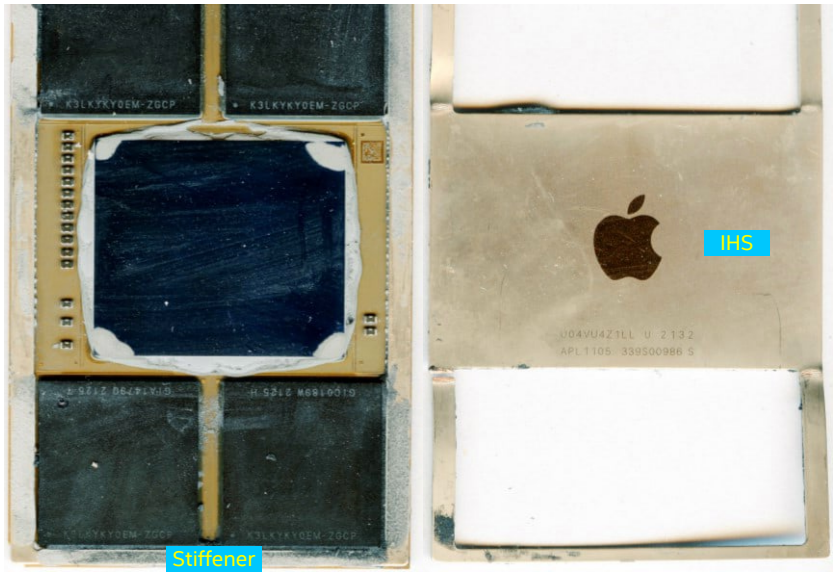
*Some images courtesy of TMG Si C/A team

Apple M1 Pro/M1 Max Package details





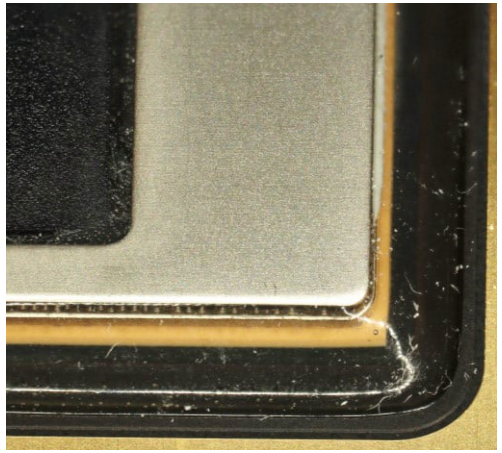




- Corner glue covers significant perimeter of the package.
- Coreless substrate with no Solder Resist on top layer, typical of ETS substrates.
- A combination of stiffener around package + footless IHS covering only the die area are attached to each other with sealant.
- Holes in the copper IHS accommodate different height (different capacity) BGA packages and reduce thermal cross talk between LPDDR packages and the SOC.

*Some images courtesy of TMG Si C/A team

Apple M1 Pro/M1 Max – Corner Glue material analysis



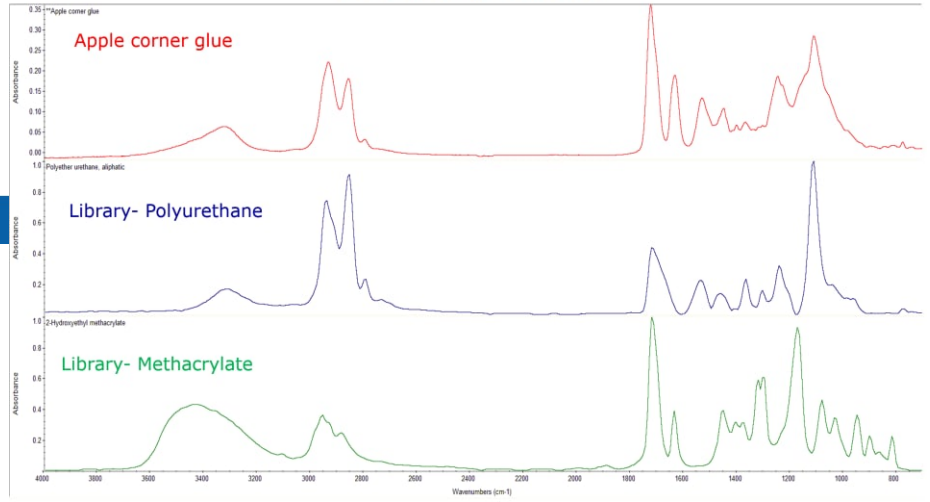
1

FTIR Analysis Report

- **FAMIS #L2146074**
- **Purpose**
  - FTIR competitive analysis of Apple SoC corner glue
- **Analyst**
  - Derek Hetherington
- **Equipment**
  - Thermo iS50 FTIR with Ge ATR
- **Summary**
  - The corner glue is a good match for a mixture of Polyurethane and a Methacrylate

2

FTIR Spectra



- The corner glue is a good match for a mixture of Polyurethane and a Methacrylate

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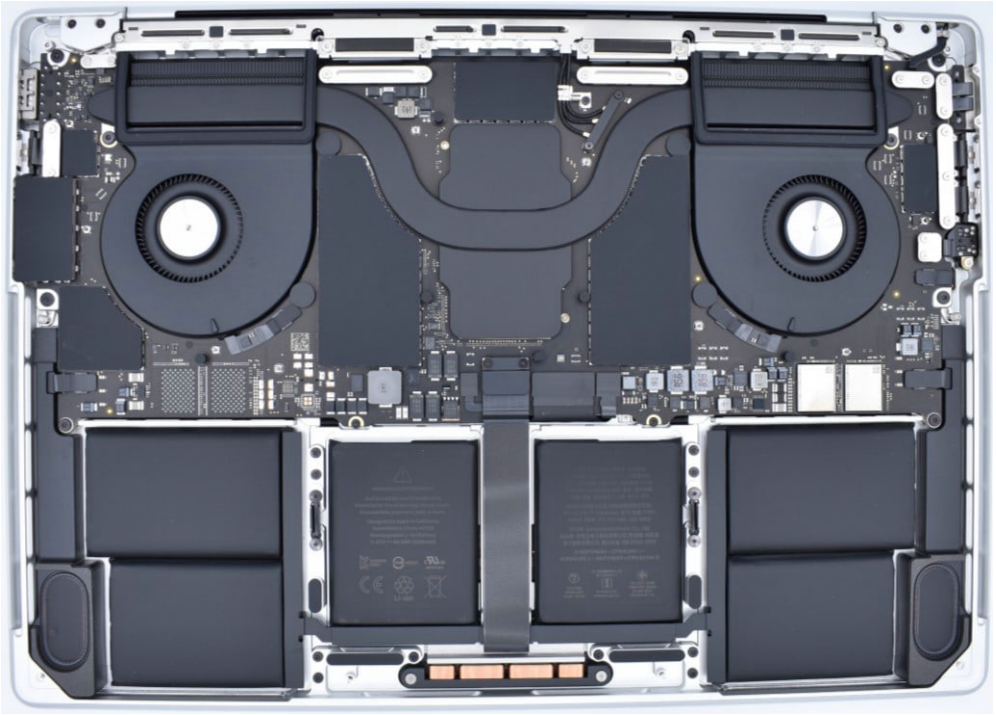
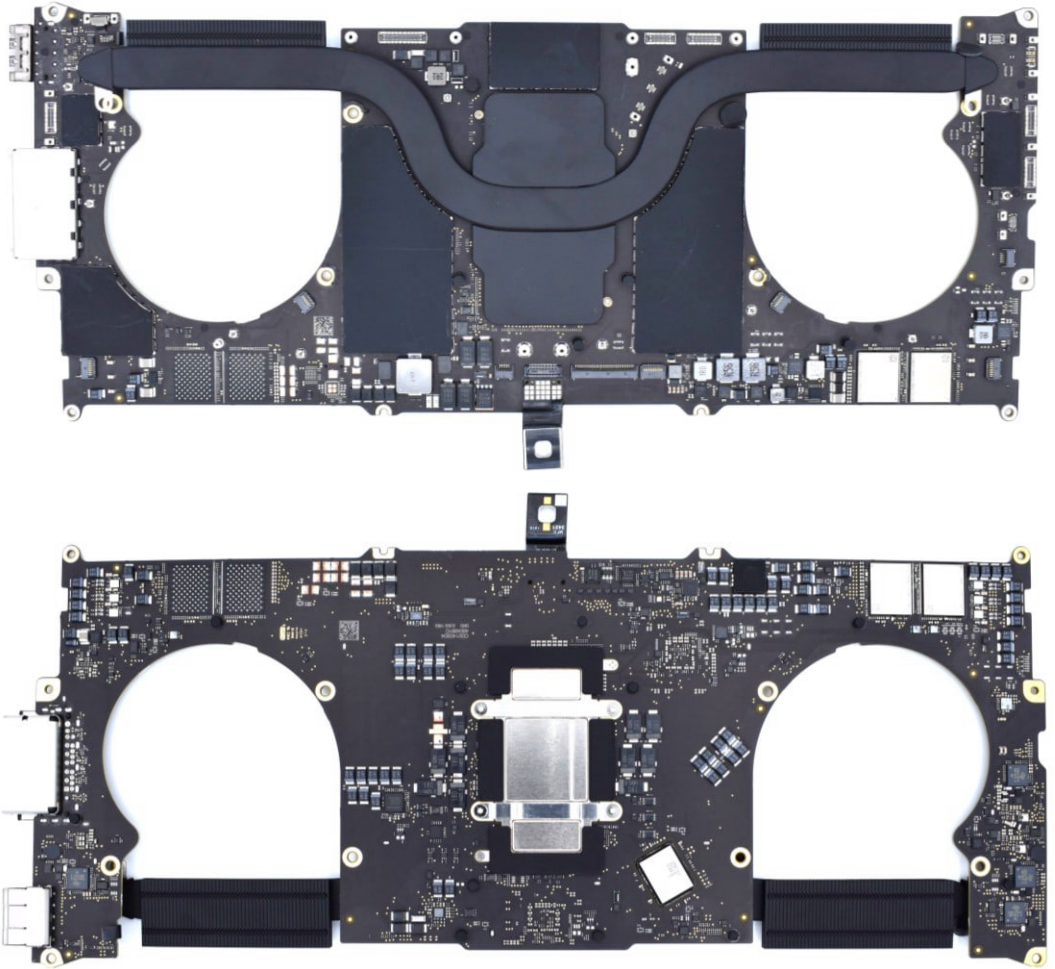
MacBook Pro 14” with Apple M1 Pro SoC





16GB unified memory | 1TB SSD

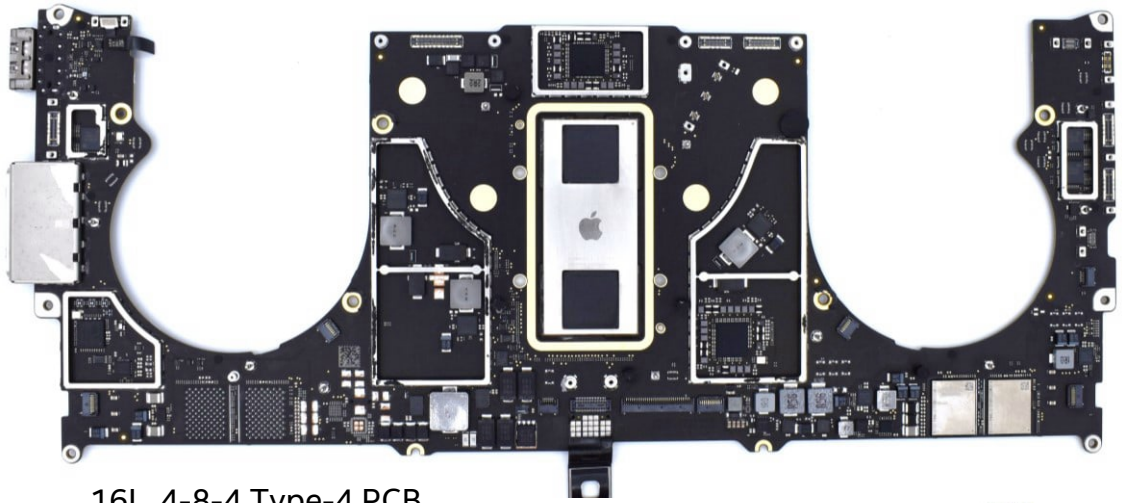
14-inch MacBook Pro

10-core CPU and 16-core GPU • 14.2-inch (diagonal) display with True Tone technology • Three Thunderbolt 4 (USB-C) ports, HDMI port, SDXC card slot, and MagSafe 3 port • Headphone jack; high-fidelity six-speaker sound system • Full-size backlit Magic Keyboard and Touch ID • Wi-Fi 6 and Bluetooth 5.0 • FaceTime HD camera[1] • Preinstalled macOS • Size and weight: 0.61 by 12.3 by 8.71 inches (1.55 by 31.26 by 22.12 cm); 3.5 pounds (1.6 kg)[2] • Meets ENERGY STAR® requirements

Includes 14-inch MacBook Pro, USB-C Power Adapter, USB-C to MagSafe 3 Cable

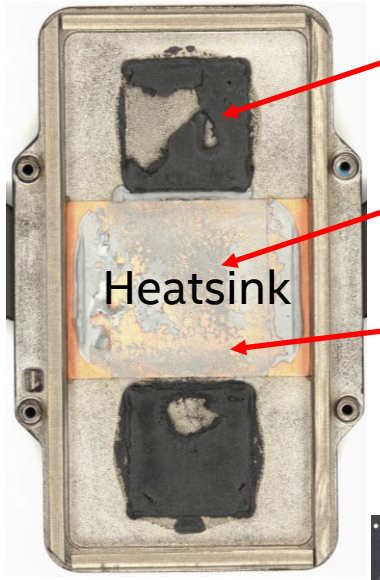
Requires internet access; acceptance of the software license terms at apple.com/legal/sla; Apple ID (for some features). Additional information at apple.com/macbook-pro. 1TB = 1 trillion bytes; actual formatted capacity less. Battery life and charge cycles vary by use and configuration. 1. FaceTime requires a FaceTime-enabled device for caller and recipient and internet connection. 2. Weight varies by configuration and manufacturing process. 826-08974-A

MacBook Pro 14” with Apple M1 Pro SoC



16L, 4-8-4 Type-4 PCB
1.1mm thick

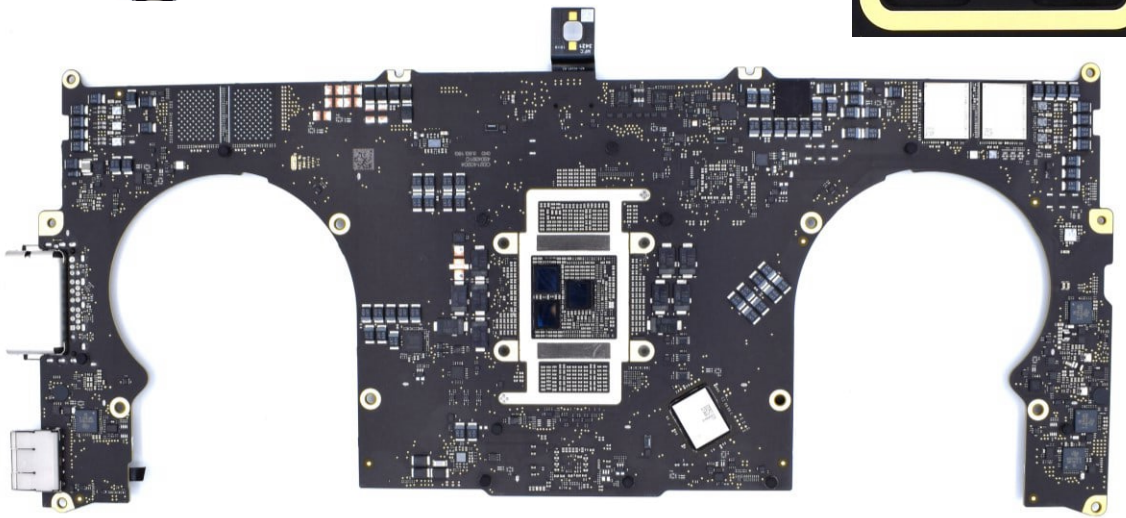
2 types of Thermal Interface Material



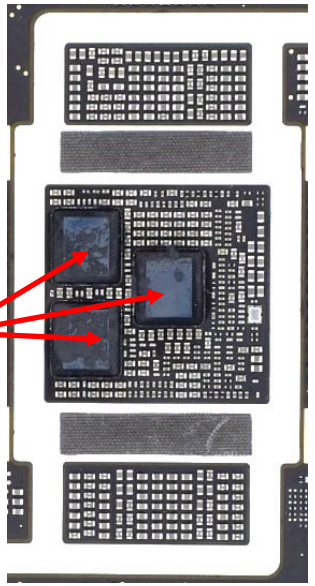
TIM2 above LPDDRs

TIM2 above SoC

Penetrating Heat pipe eliminates one interface between IHS (similar to M1 MacBook Pro)



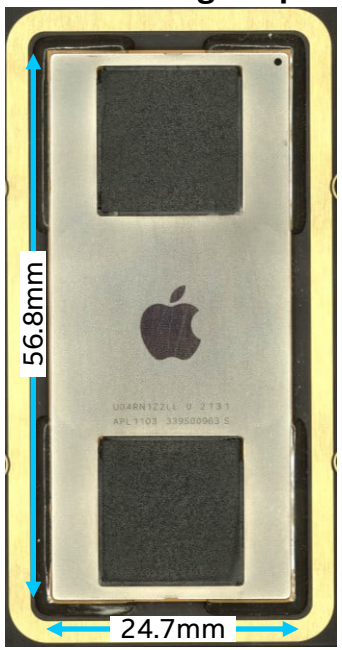
Thermal Interface Material to cool 3 power delivery ICs



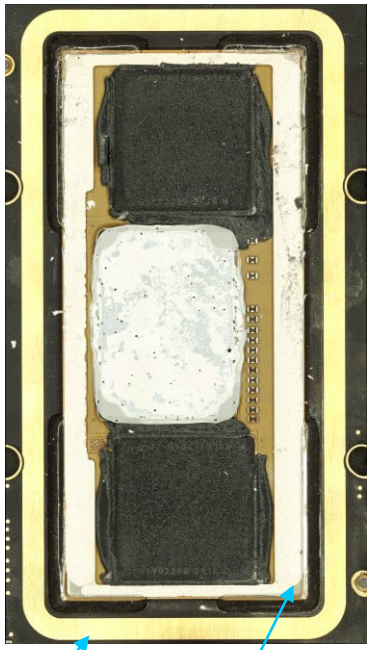
*Same wire mesh/EMI shields and thermal materials as highlighted on MacBook Pro16’ system.

Apple M1 Pro SoC

M1 Pro
Package Top



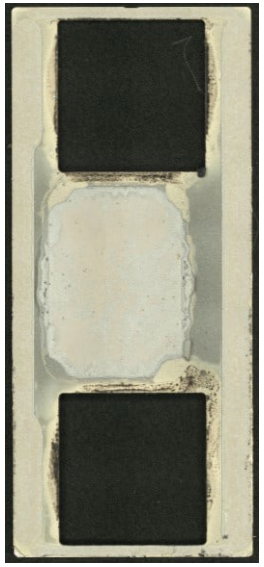
M1 Pro
Lid Removed



Heat sink/EMI shield contact surface

Stiffener frame

M1 Pro
Lid Bottom side



IHS lid is a flat plate with cutouts for LPDDR5 DRAM packages

M1 Pro
PTIM cleaned

SoC: 19.04 x 13.3mm die
LPDDR: 14x14mm
15 0603 3T DSCs

M1 Pro
Package Bottom

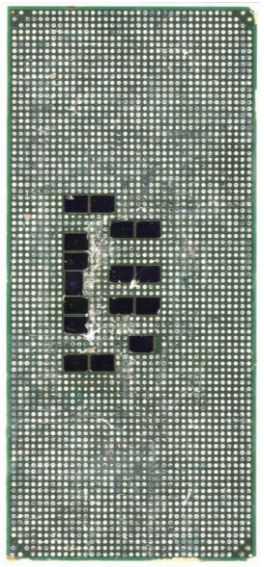
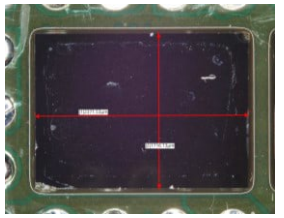


*Image horizontally flipped

- Pitch: 0.6mm
- BGA qty: TBD
- 16 DTC's, size: 1.7x2.3mm



M1 Pro
PCB Bottom

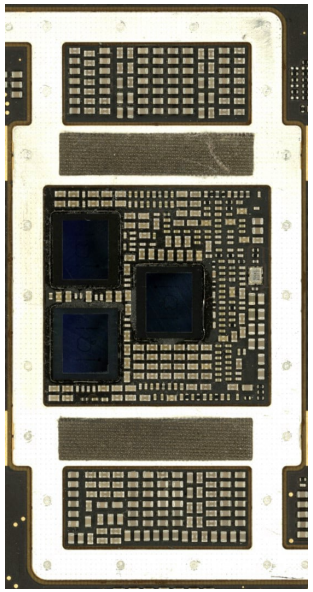
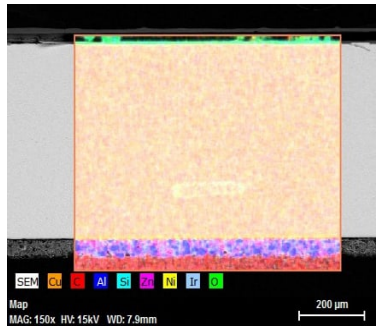
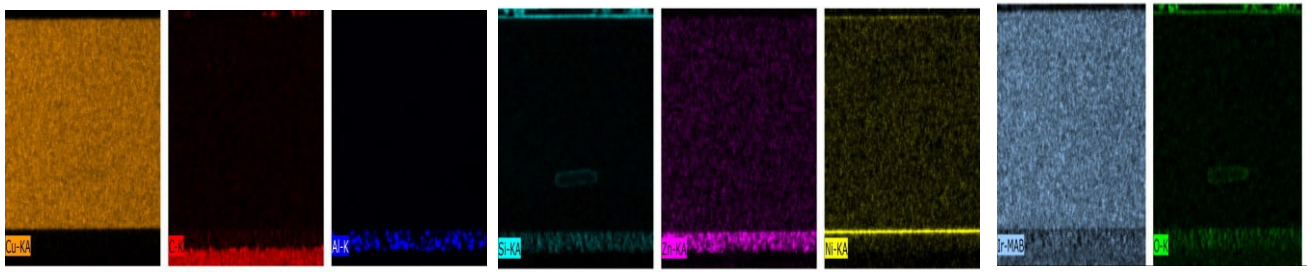


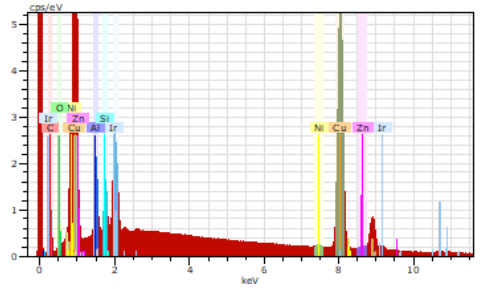
*Image horizontally flipped

Apple M1-Max IHS and Stiffener EDX

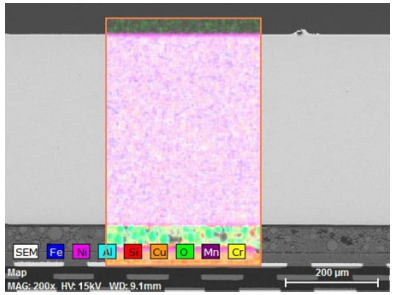
Integrated Heat Spreader X-Section

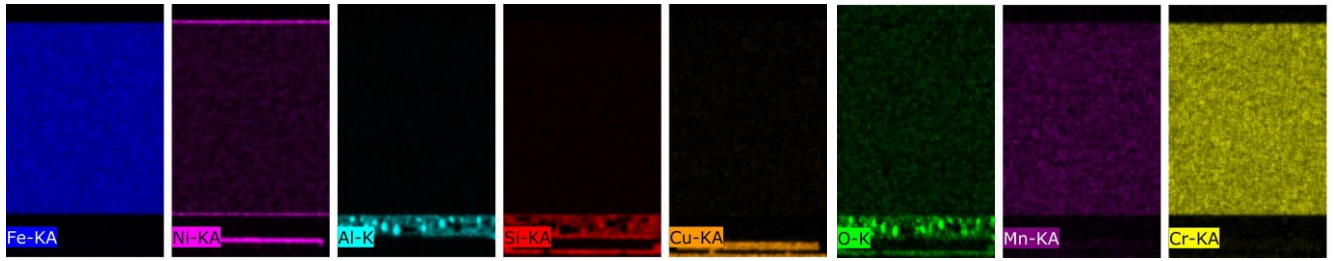


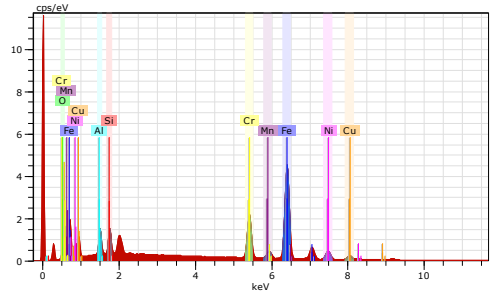




Stiffener & Fiducial X-Section

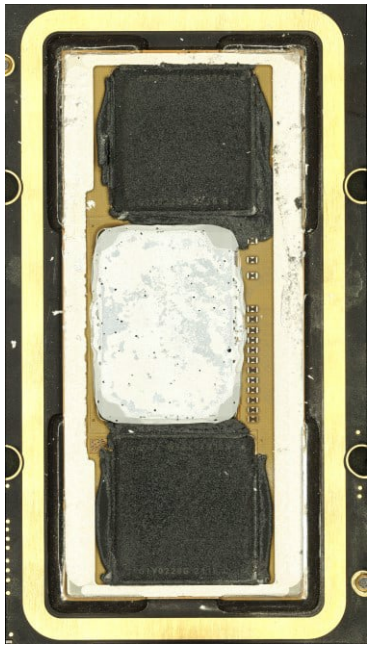






- The IHS is Ni plated Cu
- TIM1 filler contains Al, Si and Zn
- The stiffener is Ni plated stainless steel (Fe/Cr/Mn).
- Al/Si filler is in stiffener/substrate adhesive sealant.

Apple M1 Pro/M1 Max - TIM material analysis



1

FTIR Analysis Report

Luminis #L2208021

Purpose

- FTIR competitive analysis of Feb 22 Apple Macbook IHS PTIM

Analyst

- Derek Hetherington

Method

- Thermo Continuum FTIR w/ Ge ATR

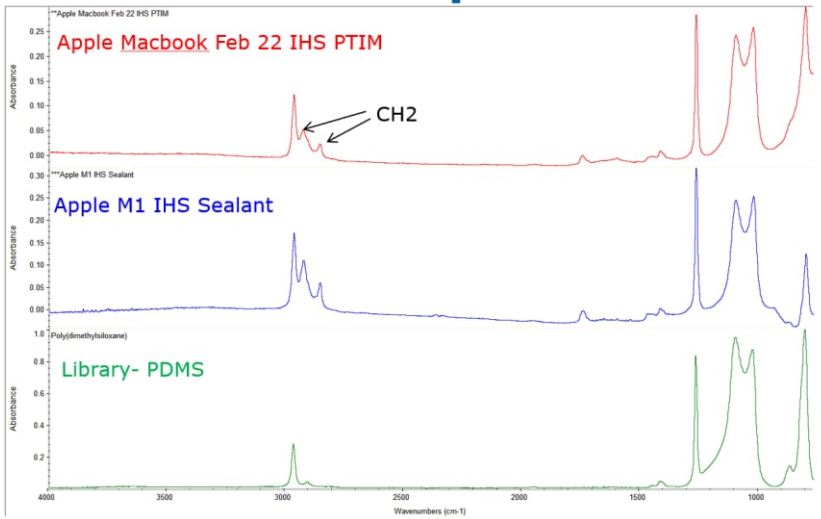
Summary

- The PTIM is a very good match for prior Apple M1 PTIM
- It is PDMS based with a longer chain hydrocarbon or another siloxane with CH2

ATTD CORE COMPETENCY Intel Confidential

2

FTIR Spectra



- The PTIM is a very good match for prior Apple M1 IHS sealant
- It is PDMS based with a longer chain hydrocarbon or another siloxane with CH2

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Apple M1 Pro/M1 Max - TIM material analysis

FTIR Analysis Report

- **FAMIS #L2145087**
- **Purpose**
  - FTIR competitive analysis of Apple TIM materials
- **Analyst**
  - Derek Hetherington
- **Equipment**
  - Thermo iS50 FTIR with Ge ATR
- **Summary**
  - See slides

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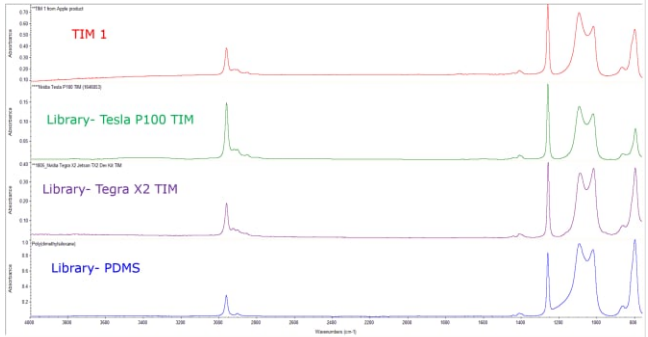
TIM 1 FTIR Spectra

2



- TIM 1 is PDMS based and is very similar to Nividia TIM from the Tesla P100 and Tegra X2

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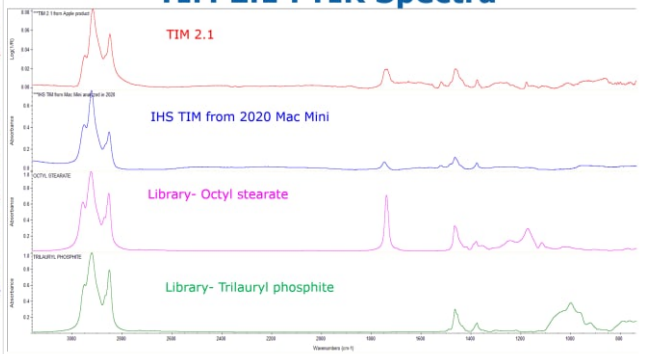
TIM 2.1 FTIR Spectra

3



- TIM 2.1 is very similar to the 2020 Mac Mini IHS TIM. It was a good match for trilauryl phosphite and a stearate

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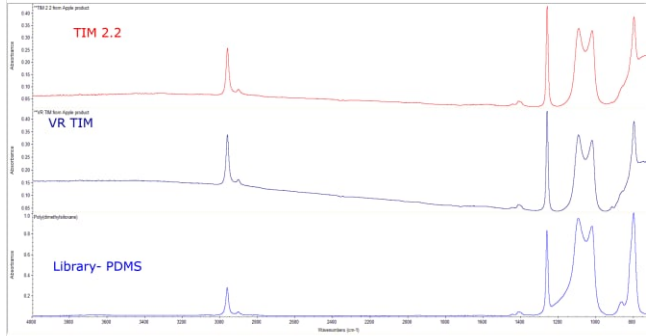
TIM 2.2 and VR TIM FTIR Spectra

4



- TIM 2.2 and VR TIM are very good matches for PDMS

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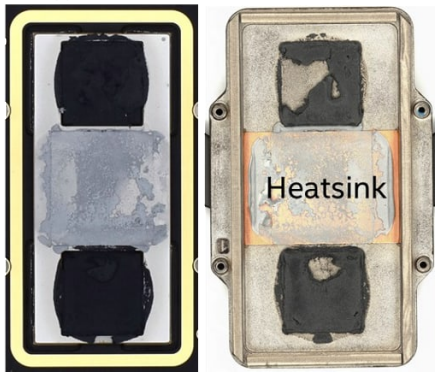
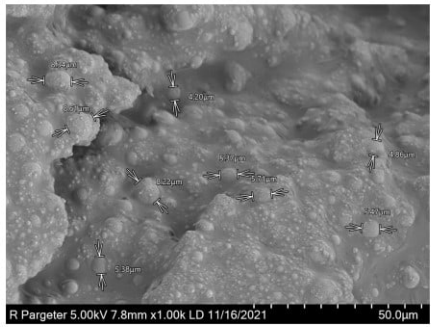
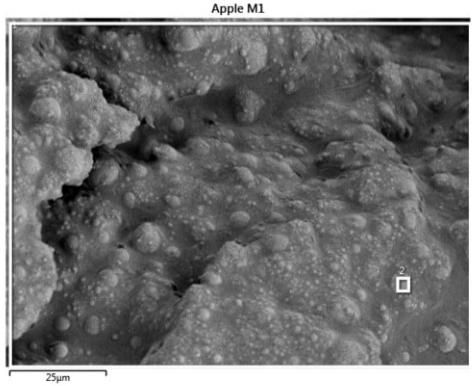
2 types of Thermal Interface Material



Apple TIM2 Grey



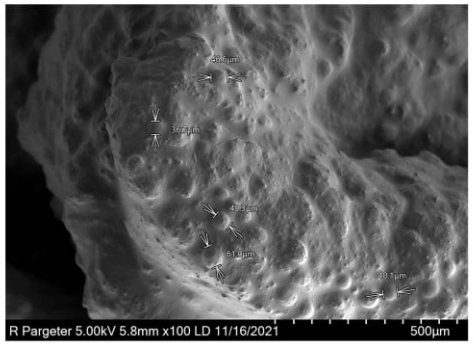


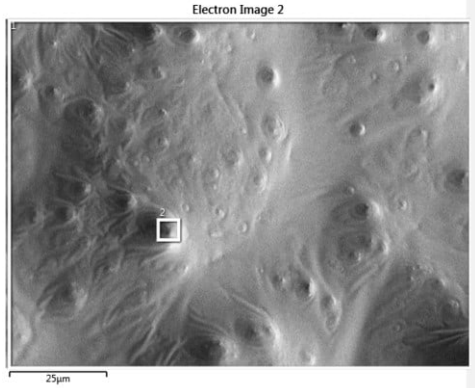
Max Particle Size: ~9 um
Al and ZnO particles

Spectrum Label	C	O	Al	Si	Zn	Total
1	53.34	15	17.35	8.9	5.41	100
2	27.46	8.42	61.8		2.32	100

Materials Technology Development | Intel Top Secret | intel | 1

Apple TIM2 Black



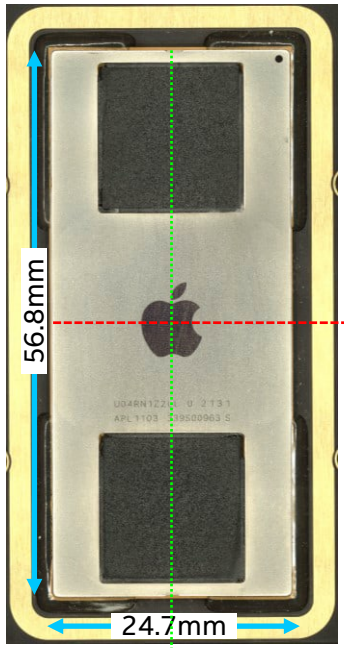


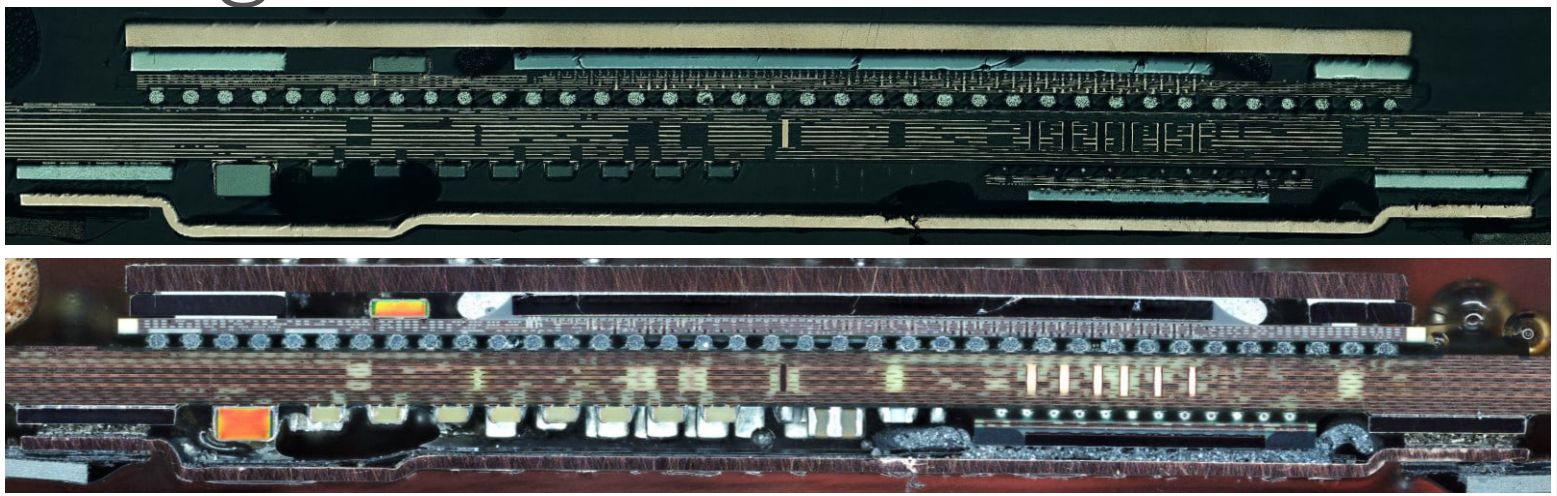
Max Particle Size: ~61 um (measured)
Al particles only

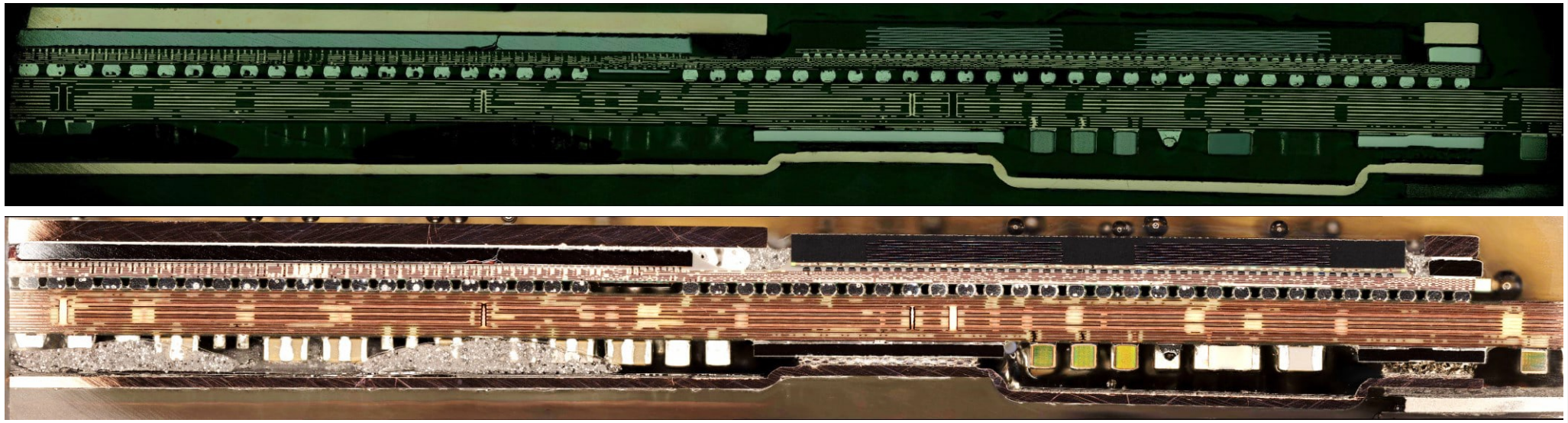
Spectrum Label	C	O	Al	Si	P	Total
1	43.13	32.77	3.44	20.34	0.32	100
2	25.3	42.38	19.82	12.49		100

Materials Technology Development | Intel Top Secret | intel | 2

Apple M1 – Pro Package X-Section

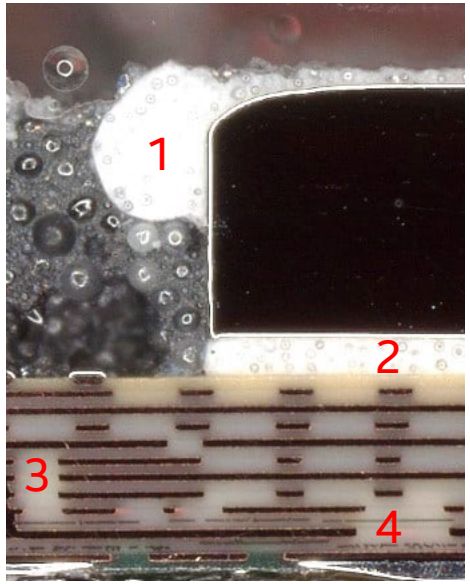


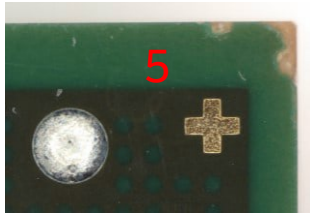




- 11-layer coreless ETS substrate, Ni/Pd/Au cap on surface layers (pads, dams, 2DID mark).
- Cu layer thickness ranges from 8-15um. Dielectric layer thickness ranges from 10-18um except ~25um thick due to glass cloth in 2 layers closest to board.
- The LPDDR Memory is a molded package with 4-layer coreless substrate, dielectric with glass cloth and 4 stacked dice.
- 100 um thick DTCs with 9um depth trenches.

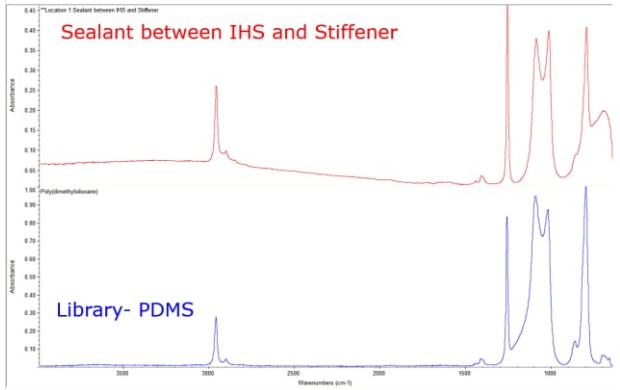
Apple M1 Pro/M1 Max – Substrate Materials Analysis





Sealant between IHS and Stiffener FM Spectra

2

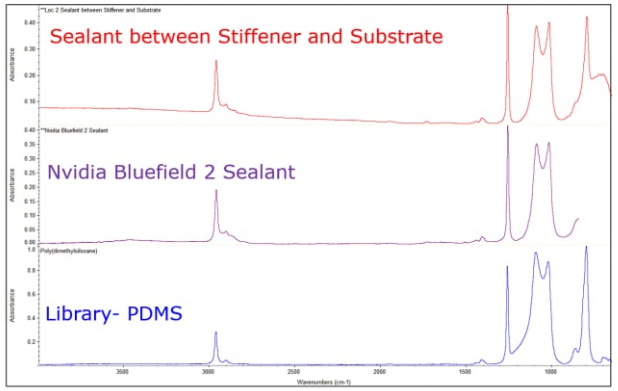


1

- The Sealant between IHS and stiffener is a very good match for PDMS

Sealant between Stiffener and Substrate FM Spectra

2

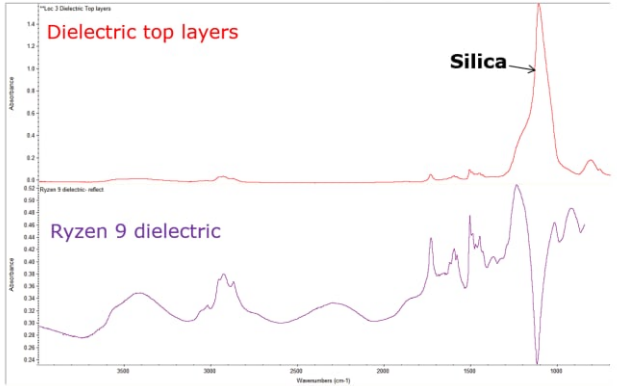


2

- The Sealant between Stiffener and Substrate is a very good match for PDMS and matches other PDMS based materials like Nvidia Bluefield 2 Sealant etc

Dielectric Top layers FM Spectra

3

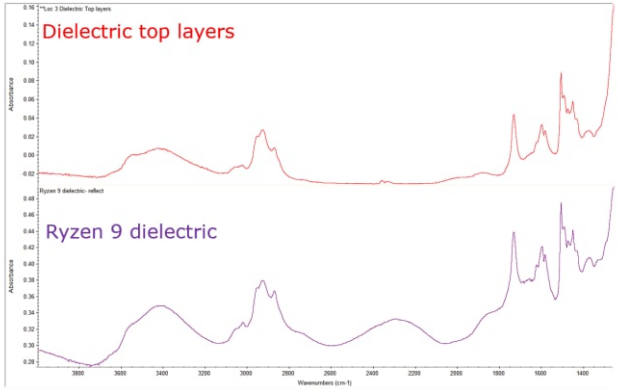


3

- The Dielectric top layers are a very good match for a silica filled epoxy. The epoxy portion is a very good match for the Ryzen 9 dielectric

Dielectric Top layers FM Spectra

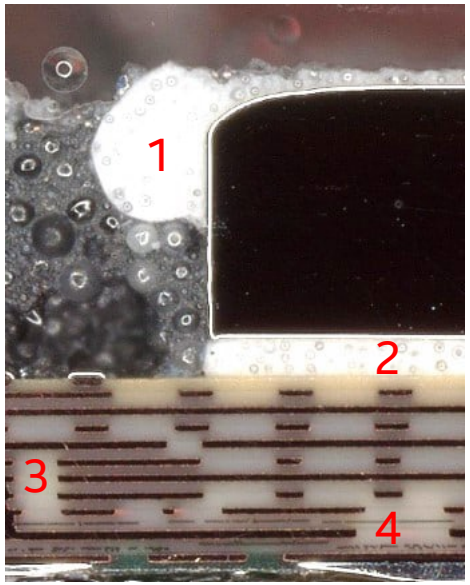
4

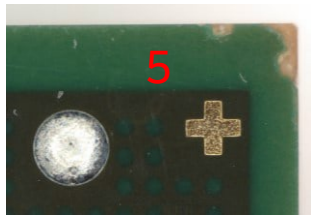


3

- The Dielectric top layers are a very good match for a silica filled epoxy. The epoxy portion is a very good match for the Ryzen 9 dielectric

Apple M1 Pro/M1 Max – Substrate Materials Analysis





1

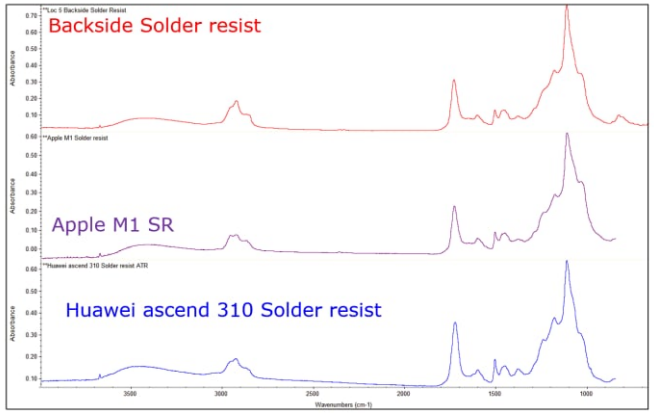
FTIR Analysis Report

- **Luminis #L2147064**
- **Purpose**
  - FTIR Competitive analysis of Apple materials
- **Analyst**
  - Derek Hetherington
- **Method**
  - Thermo IS-50 FT-IR Spectrometer w/ Ge ATR
- **Summary**
  - See Slides

Intel Confidential

7

Backside Solder resist FM Spectra



5

- The Backside Solder resist is a very good match for many Solder resist materials in the library.

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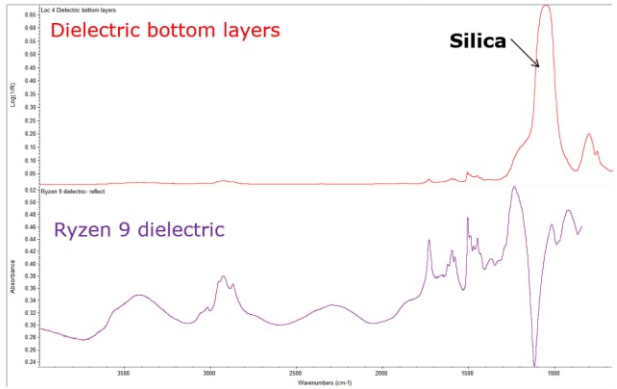
5

Dielectric Bottom layers FM Spectra



4

- The Dielectric bottom layers are a very good match for a silica filled epoxy. The epoxy portion is a very good match for the Ryzen 9 dielectric

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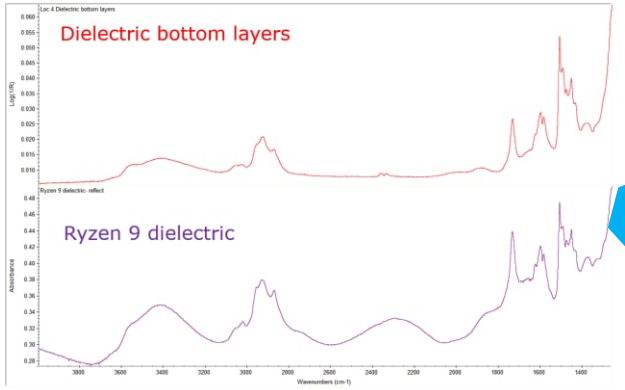
6

Dielectric Bottom layers FM Spectra



4

- The Dielectric bottom layers are a very good match for a silica filled epoxy. The epoxy portion is a very good match for the Ryzen 9 dielectric

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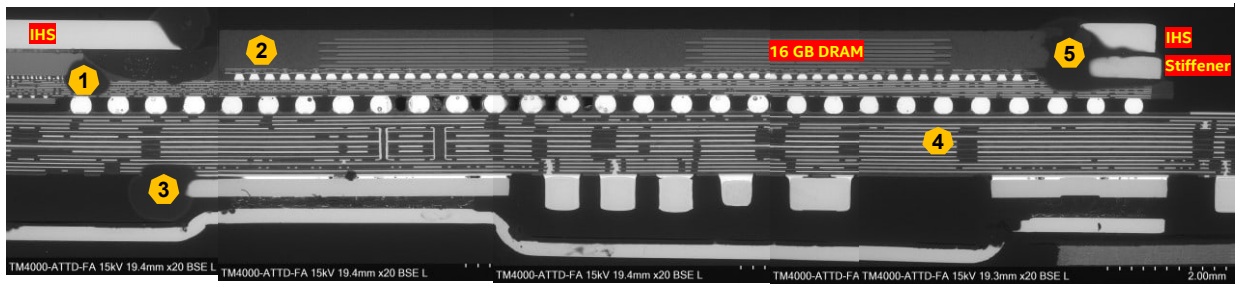
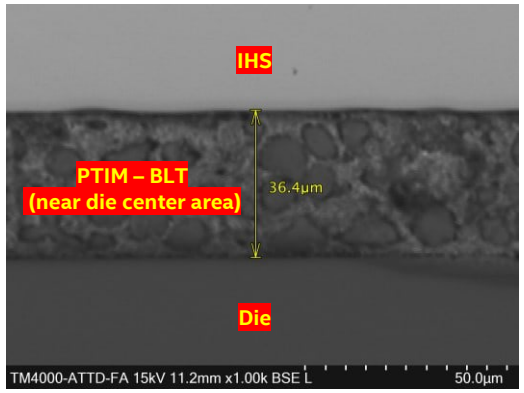
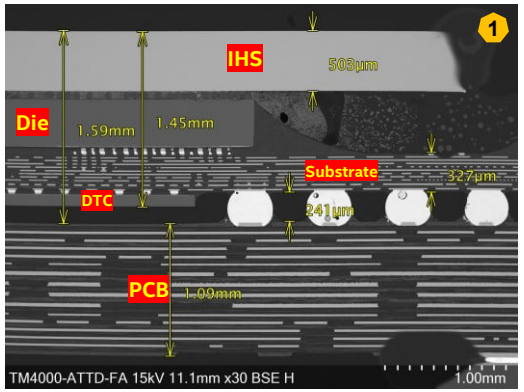
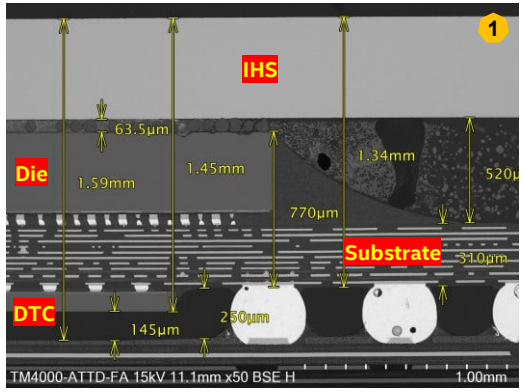
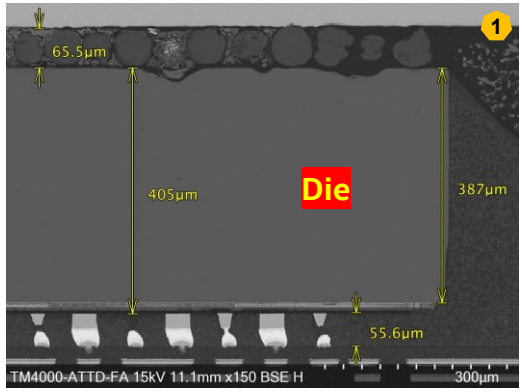
Apple M1 – Pro (16GB DRAM) X-Section

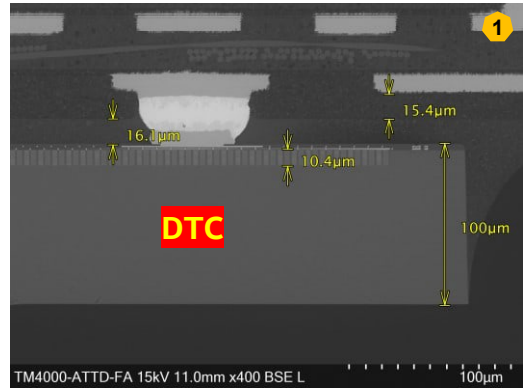


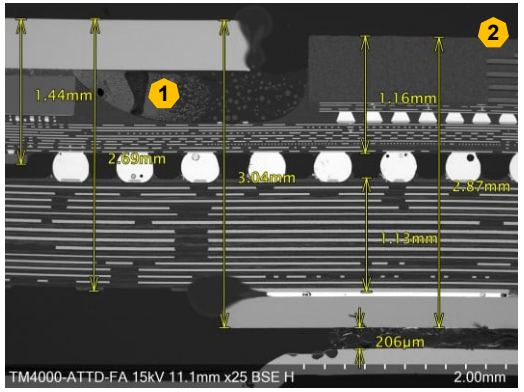


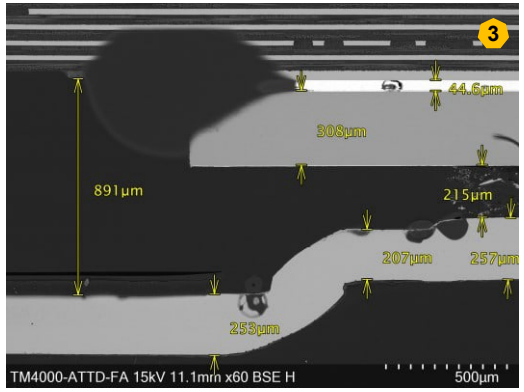


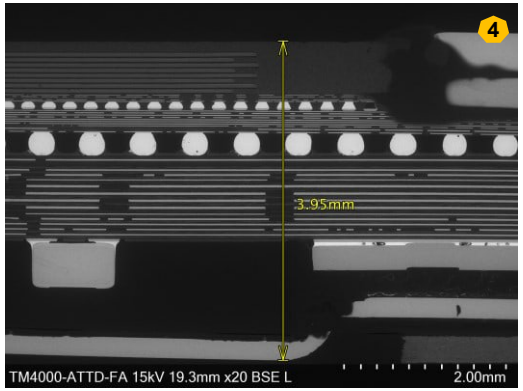


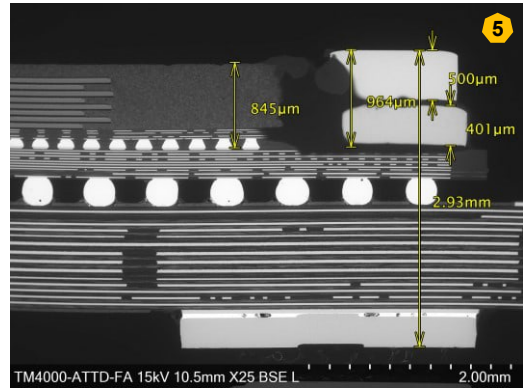




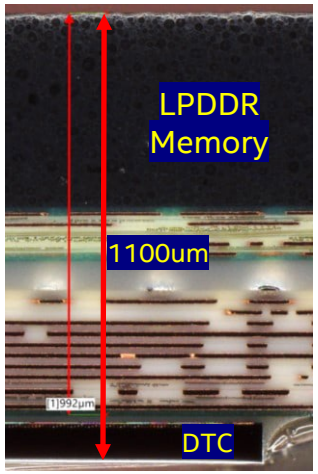


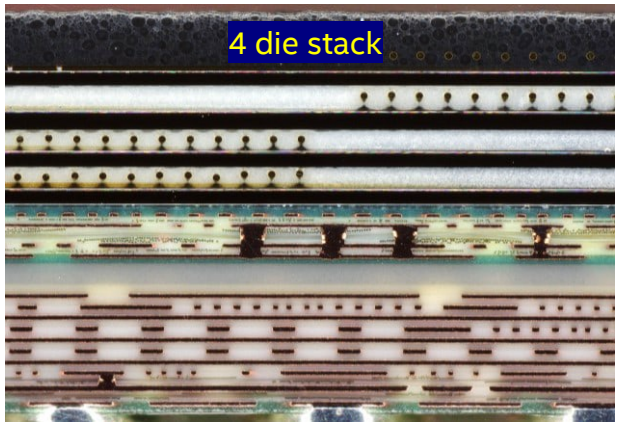


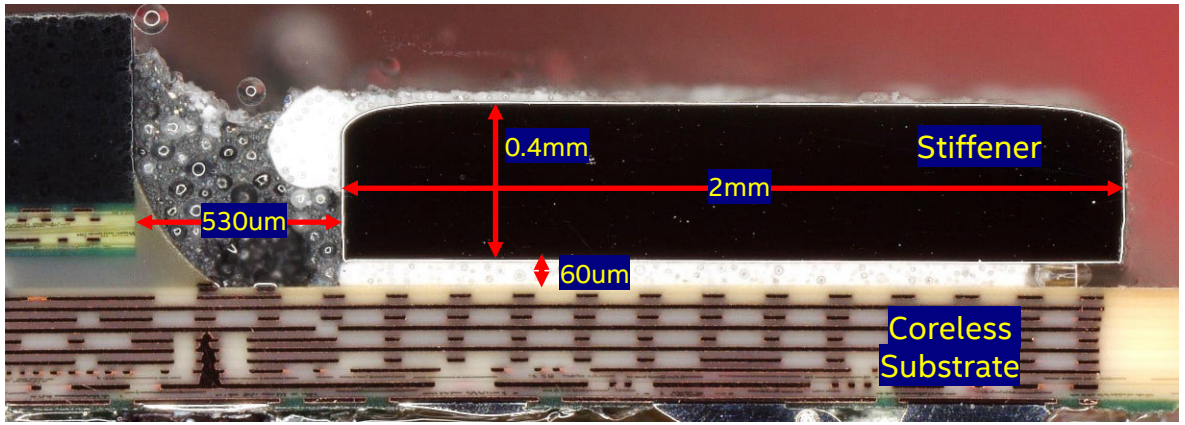


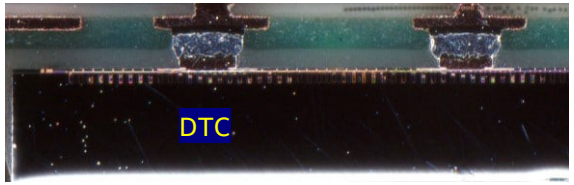


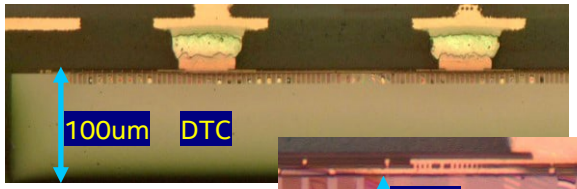
Apple M1 – Max Package X-Section

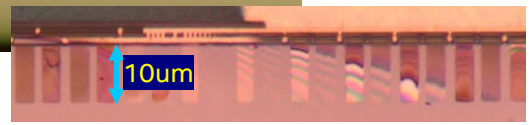


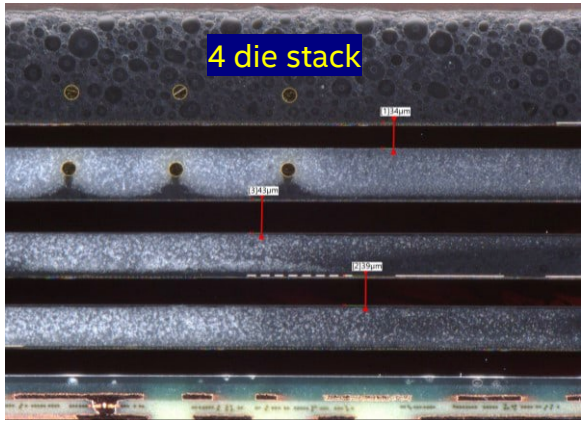


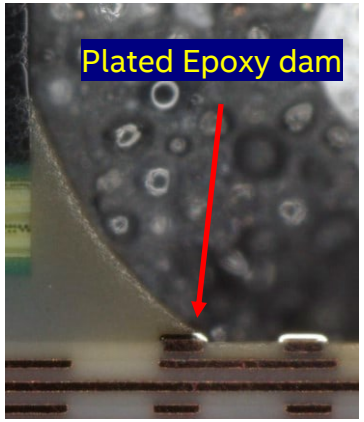










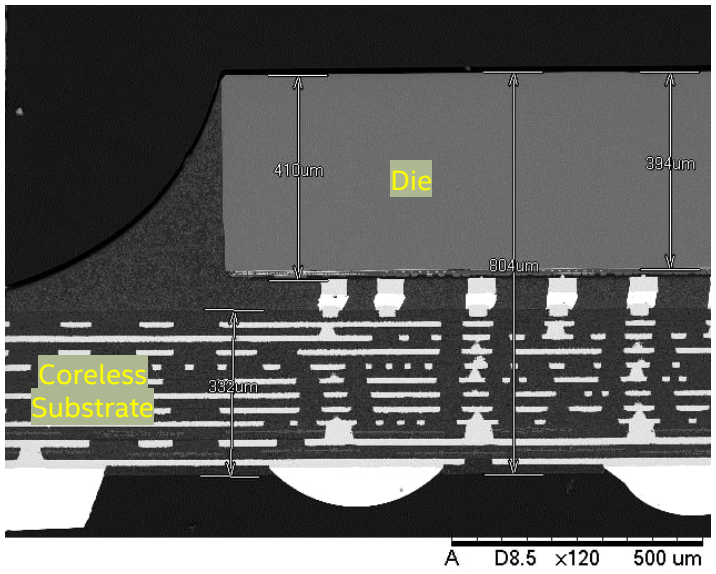


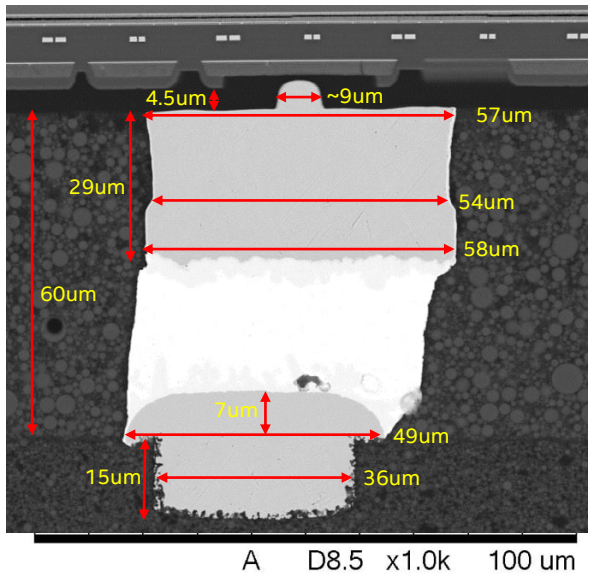
M1-Max Layer	Thickness (um)
FSR	N/A
1	15
Dielectric	10
2	8
Dielectric	18
3	10.8
Dielectric	16.5
4	9
Dielectric	17
5	11
Dielectric	15
6	10
Dielectric	18
7	12
Dielectric	15
8	10
Dielectric	18
9	10
Dielectric (Glass cloth)	26
10	13
Dielectric (Glass cloth)	23
11	12
BSR	18

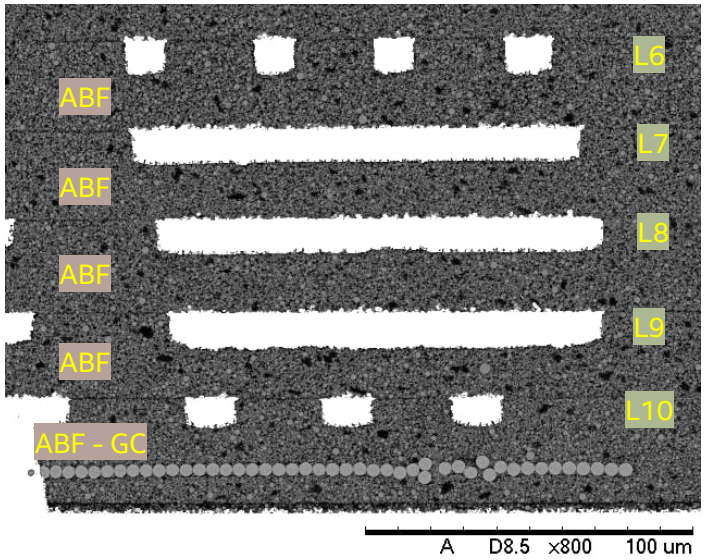
DDR Memory Layer	Thickness (um)
FSR	15
1	7
Dielectric (Glass cloth)	19
2	9
Dielectric (Glass cloth)	42
3	11
Dielectric (Glass cloth)	18
4	9
BSR	15

- 11-layer coreless ETS substrate, Ni/Pd/Au cap on surface layers (pads, dams, 2DID mark).
- Cu layer thickness ranges from 8-15um. Dielectric layer thickness ranges from 10-18um except ~25um thick due to glass cloth in 2 layers closest to board.
- The LPDDR Memory is a molded package with 4 layer coreless substrate, dielectric with glass cloth and 4 stacked dice. Both 8GB and 16GB packages extend into the IHS opening.
- 100 um thick DTCs with 9um depth trenches.

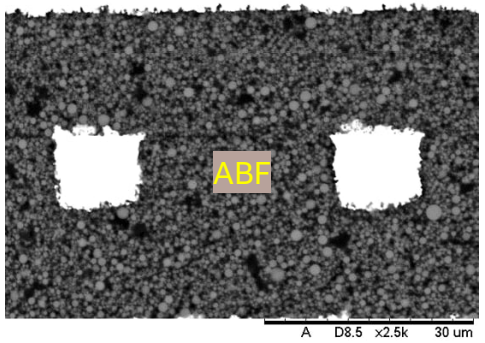
Apple M1 – Max Package X-Section

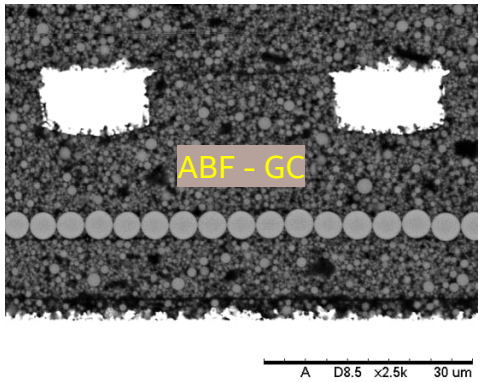






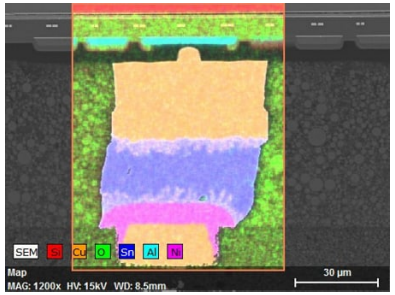
- Total package height is 800um (from BSR to top of die), die height is 410um and the coreless substrate is 330um (without BGA height).
- Cu roughness and particle filler content looks very similar between ABF and ABF with glass cloth layers.
- 58um diameter cu pillar die bump has a unique girdled shape with necking and bulge

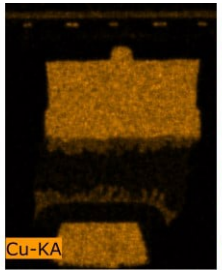


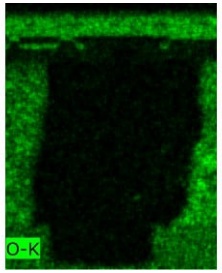


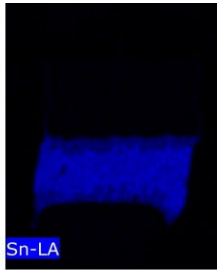
Apple M1 – Max Package - EDX Analysis

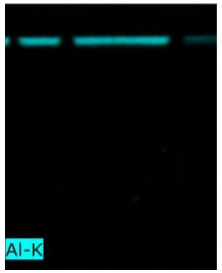
FLI Bumps

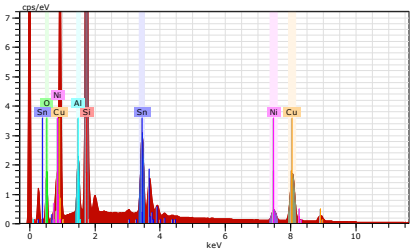




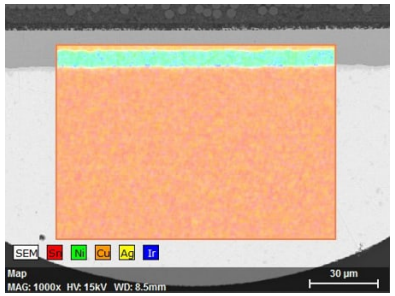


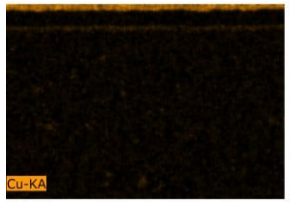


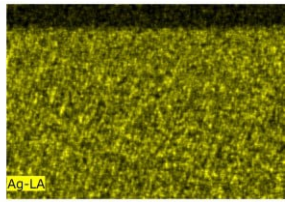


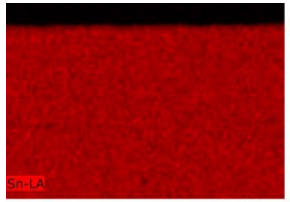


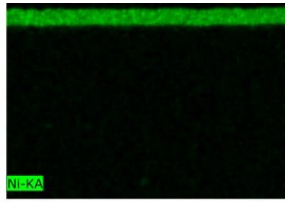
SLI BGA

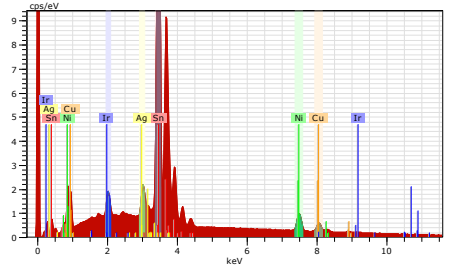




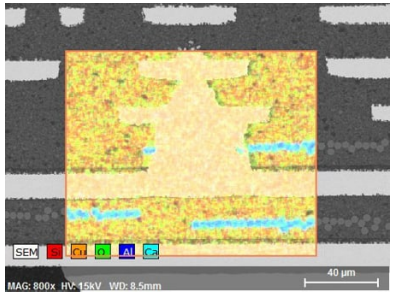


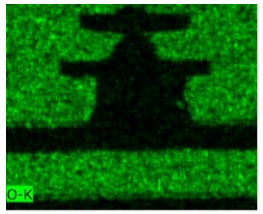


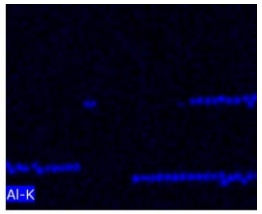


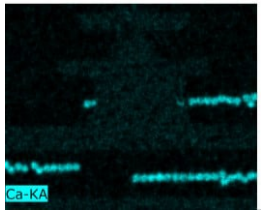


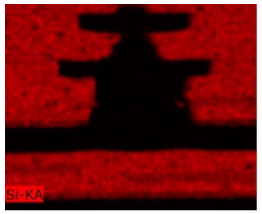
Substrate

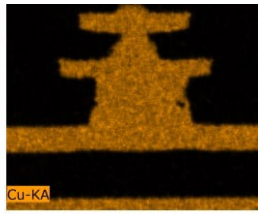


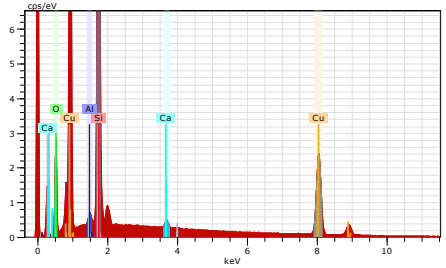






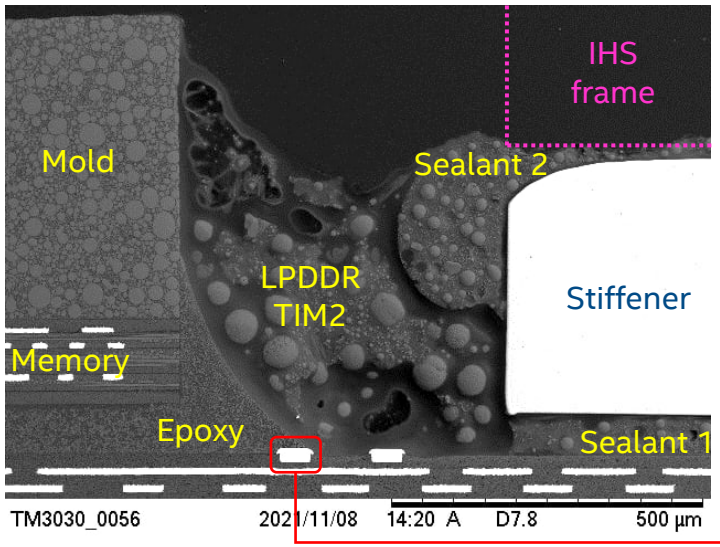


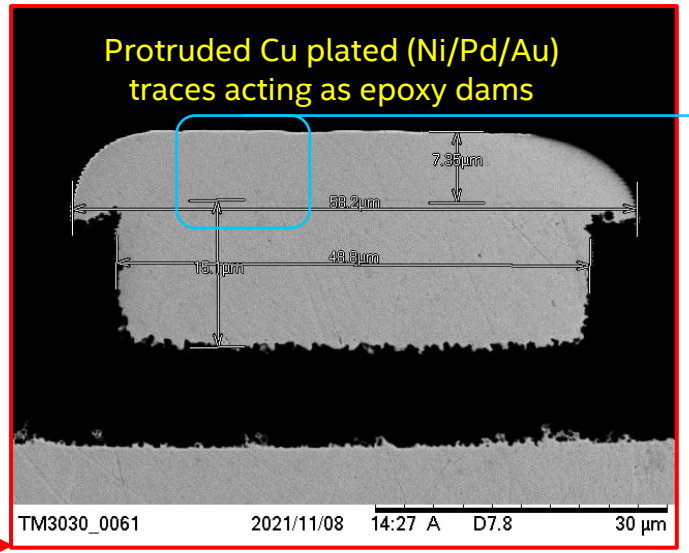


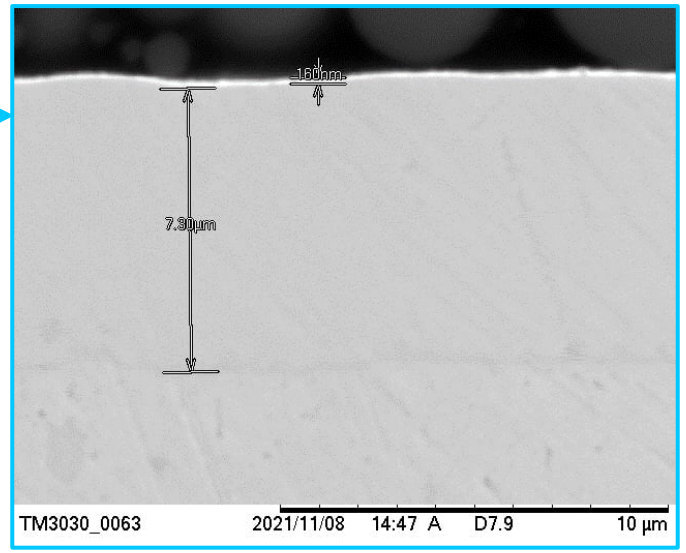


- The substrate bump metallurgy is Ni (likely NiPdAu plating) on top of embedded Cu pads. Die bump is copper pillar. FLI solder is likely Sn.
- The BGA metallurgy is undetermined SAC solder alloy.
- Substrate bottom layers show Si/Al/Ca elements on glass cloth.

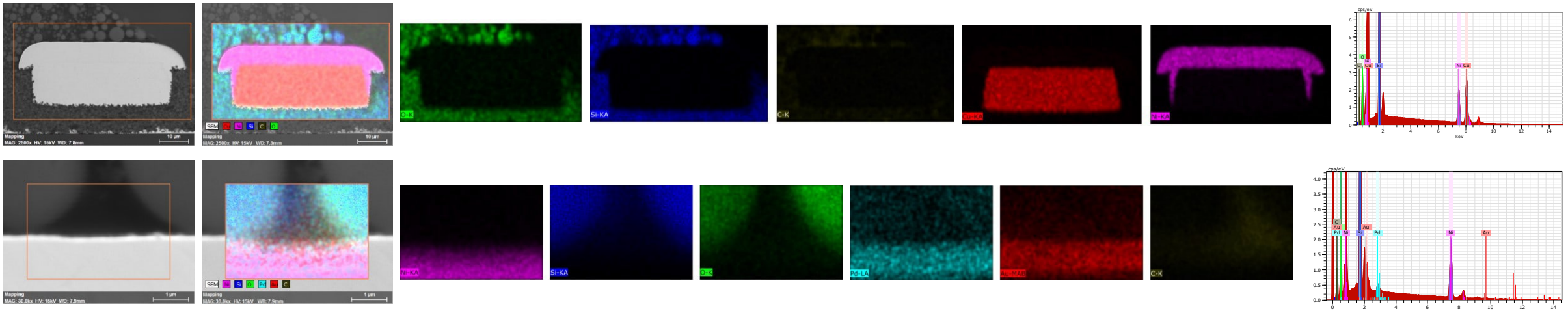
Apple M1 – Max Package X-Section





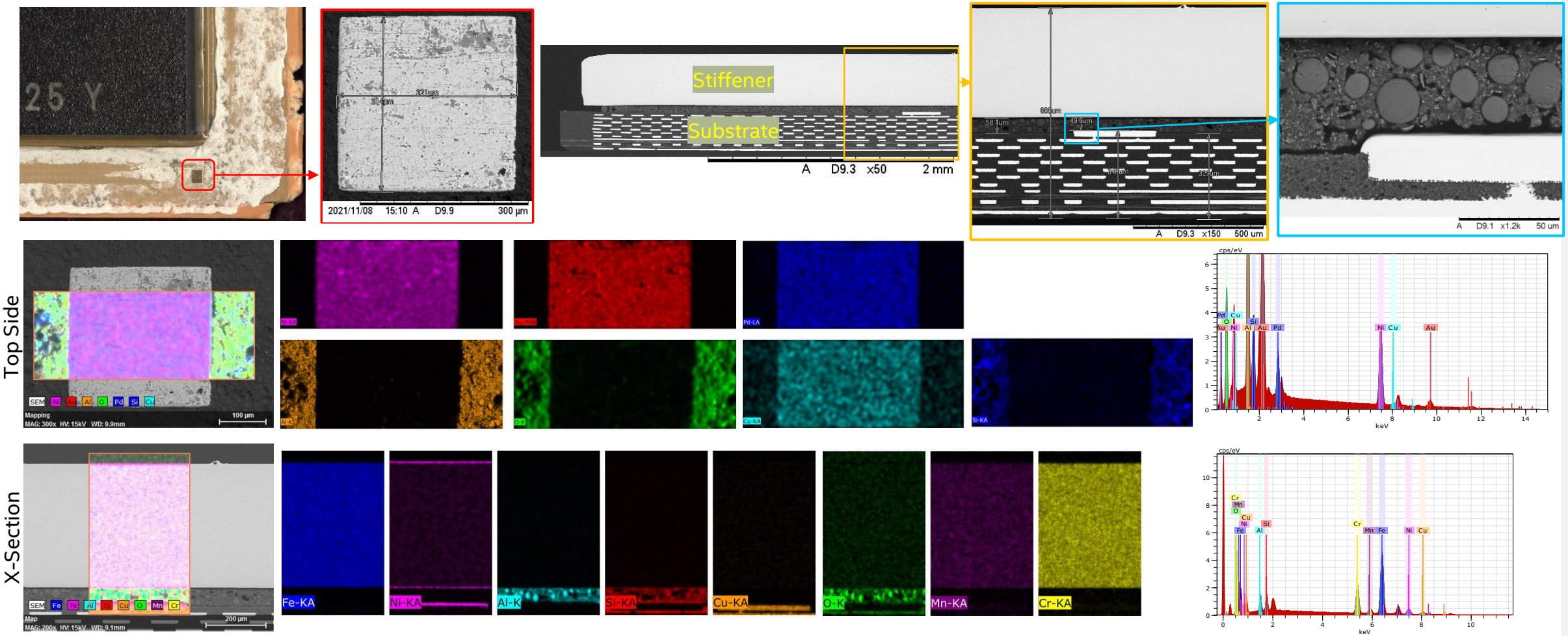


Epoxy Dam:
X-Y dimensions: ~60 x 22um
Cu Thickness: 15um
Ni thickness: 7um
Pd/Au Thickness: 160nm



Protruded traces (Cu traces plated with Ni/Pd/Au) act as CUF containment.

Apple M1 – Max Package



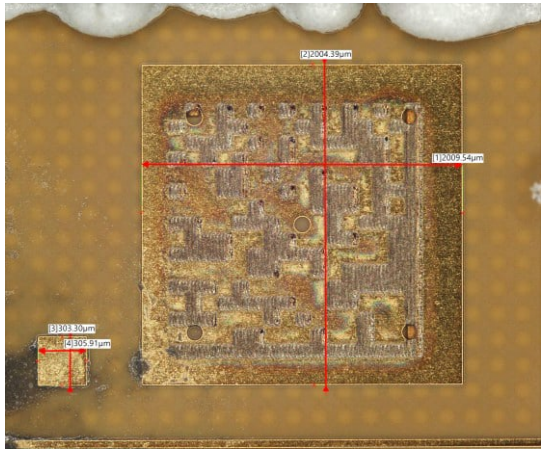
- ~300 um square pads located underneath stiffener, presumably fiducials.
- EDX analysis confirms same metallurgy as found on epoxy dams suggest all top layer was plated uniformly.
- The stiffener is Ni plated stainless steel (Fe/Cr/Mn).
- Al/Si in stiffener/substrate adhesive sealant.

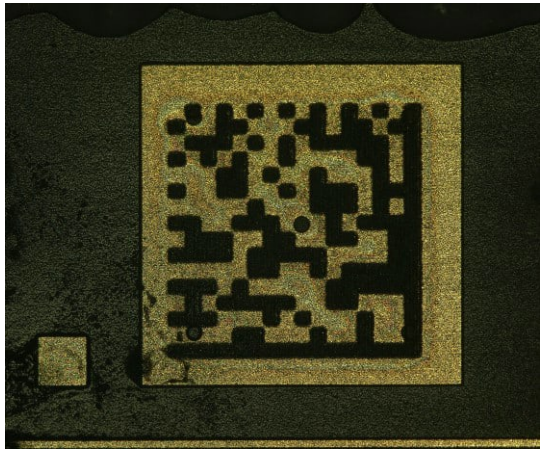
Apple M1 Pro/Max – Other package details

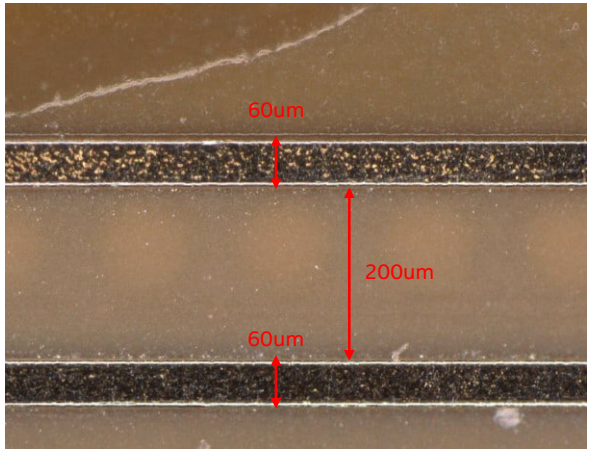
2D-ID (Laser Mark)

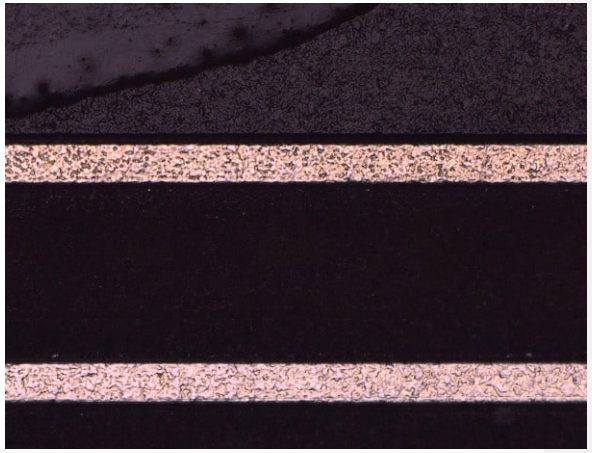
Epoxy Dam

Top Side

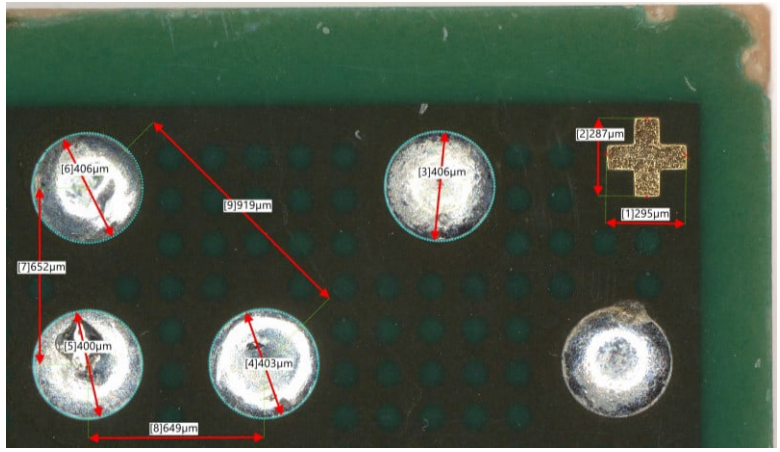


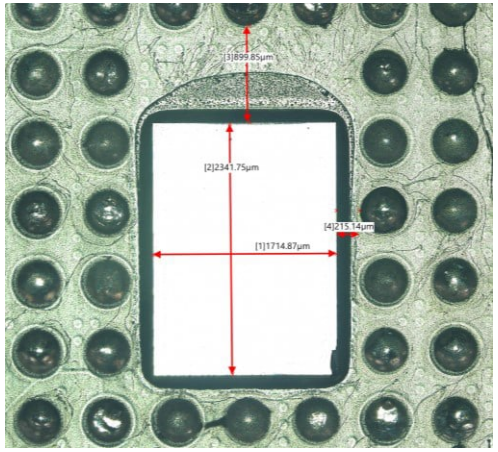


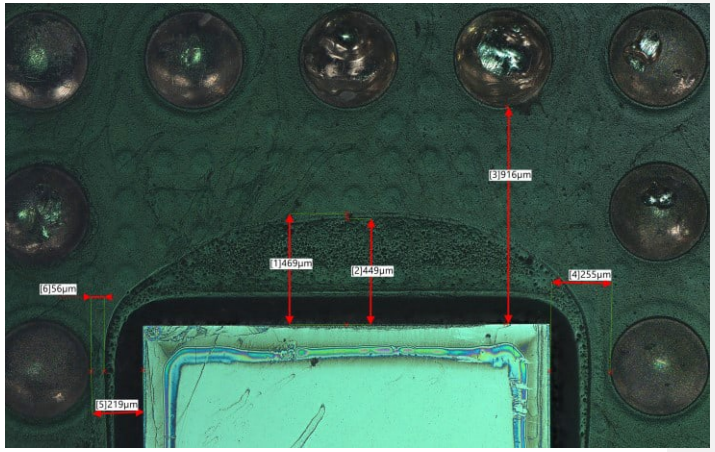




Bottom Side



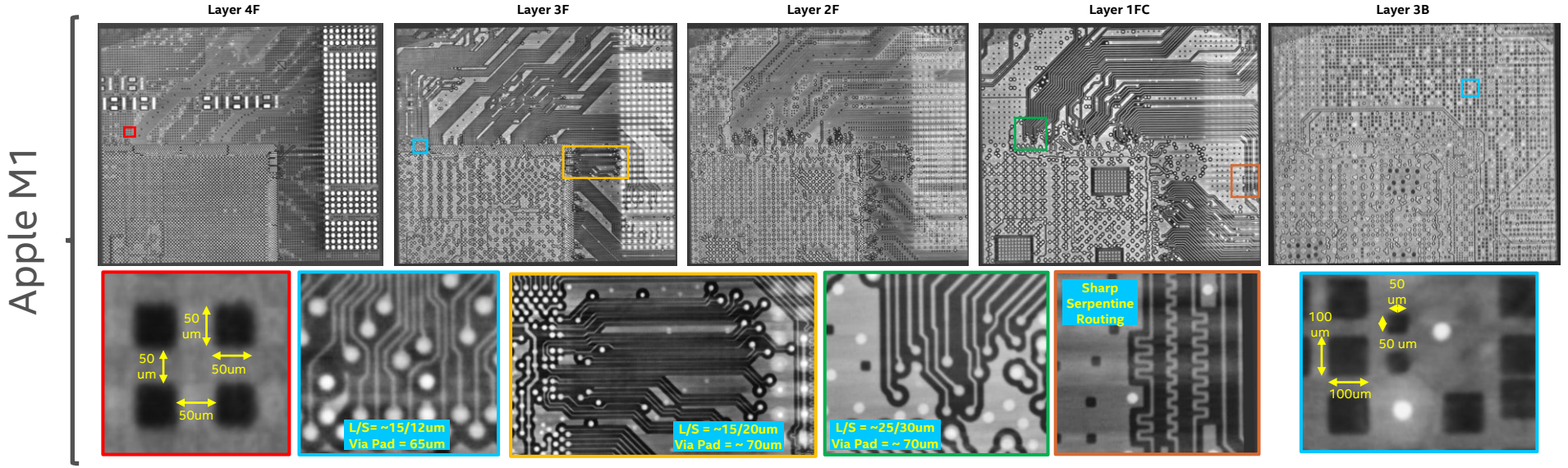


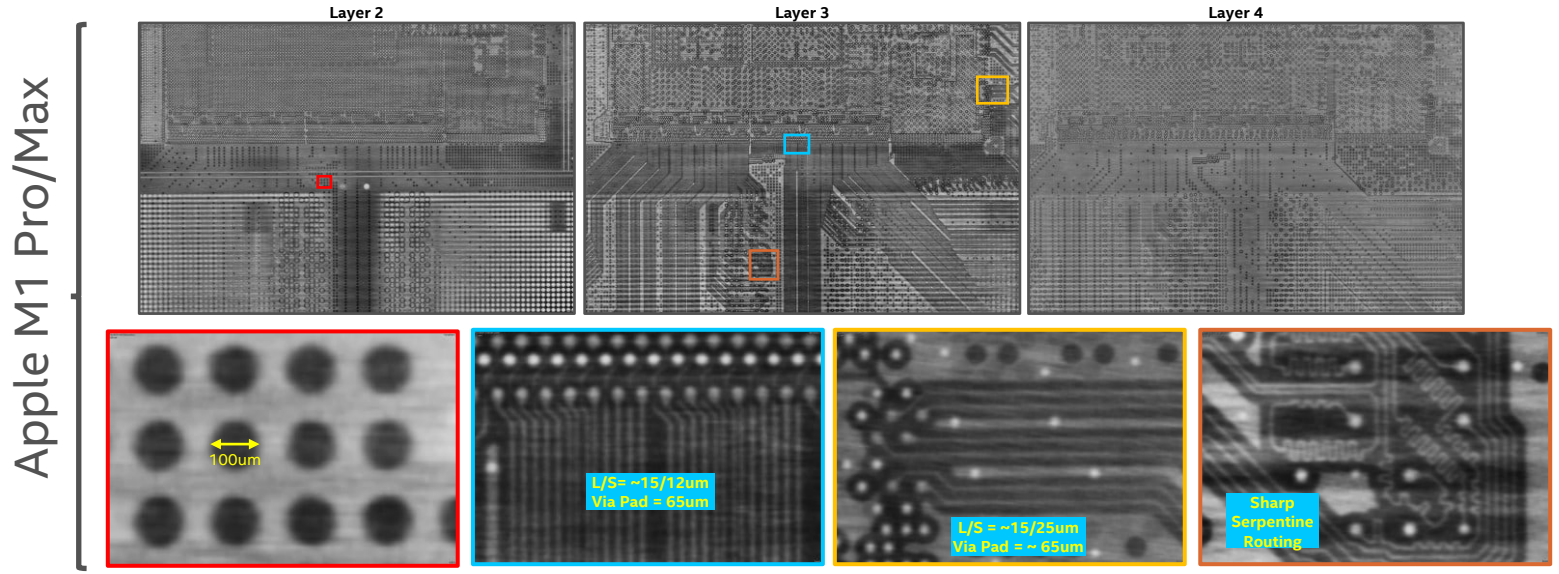


BGA details

DTC details

Apple M1 vs M1 Pro/Max Substrate Design Similarities





- Dual referencing used for high-speed signals.
- Same L/S used for single ended and differential pair signals.
- Sharp serpentine routing is used.

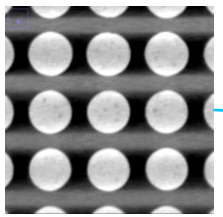
- The main difference is the use of 100um round adhesion holes vs 50x50um or 100x100um square holes.

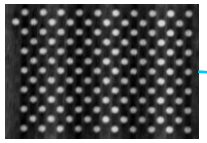
Solder joint pitch

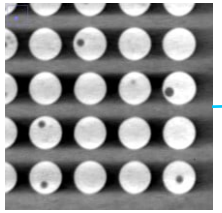
14” M1-Max

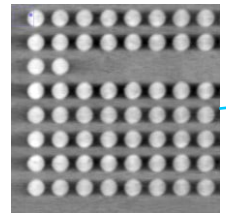
- Substrate SLI : 0.63 mm
- Deep Trench Caps: 0.14mm (0.2mm FCS) diagonal
- PCB Voltage Regulators: 0.485mm
- LPDDR: 0.27mm

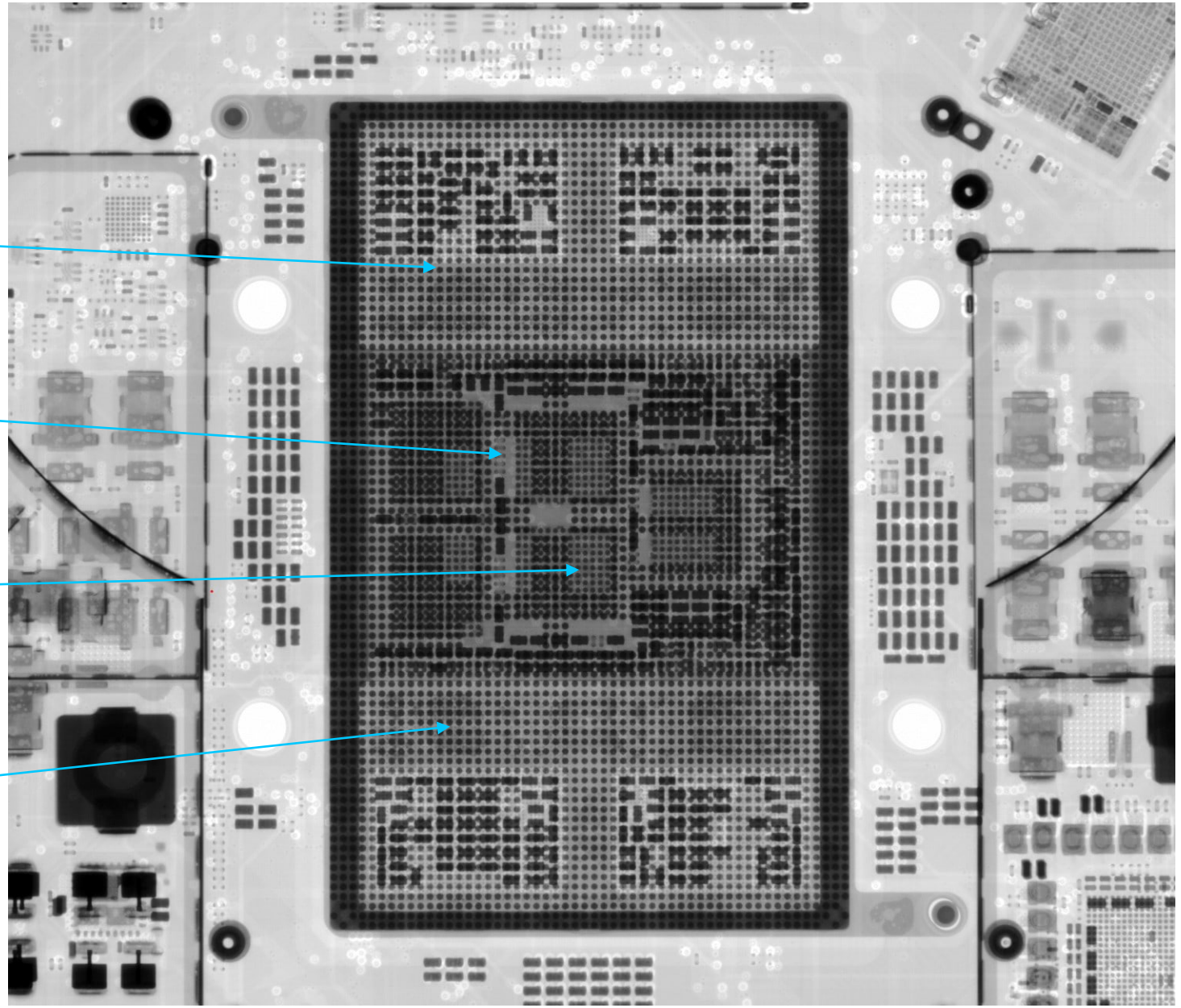
SoC FLI: 85x85um minimum (excluding ‘future’ D2D IO block)





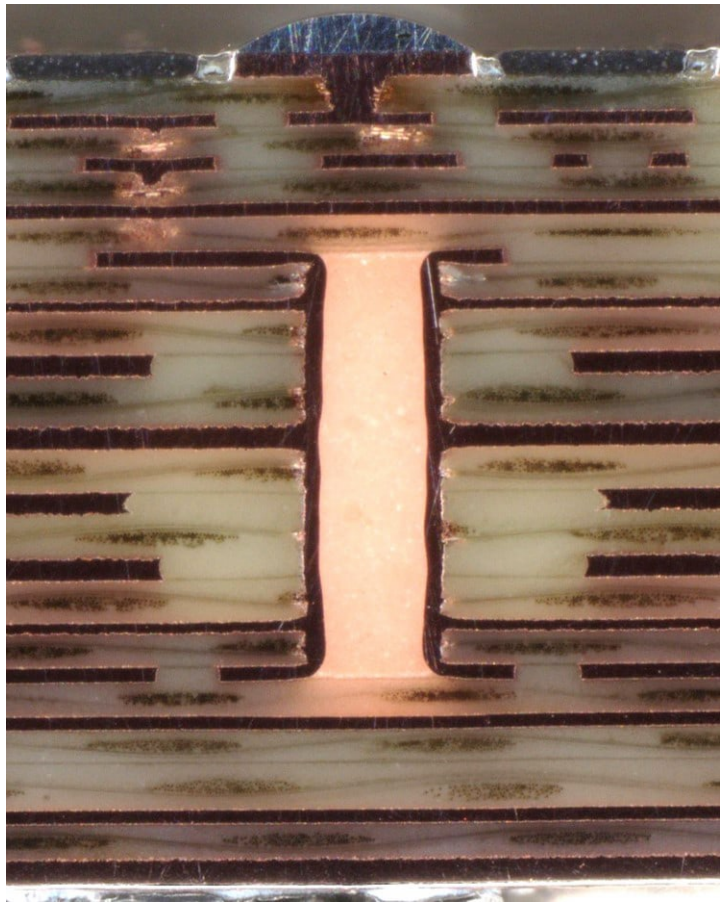


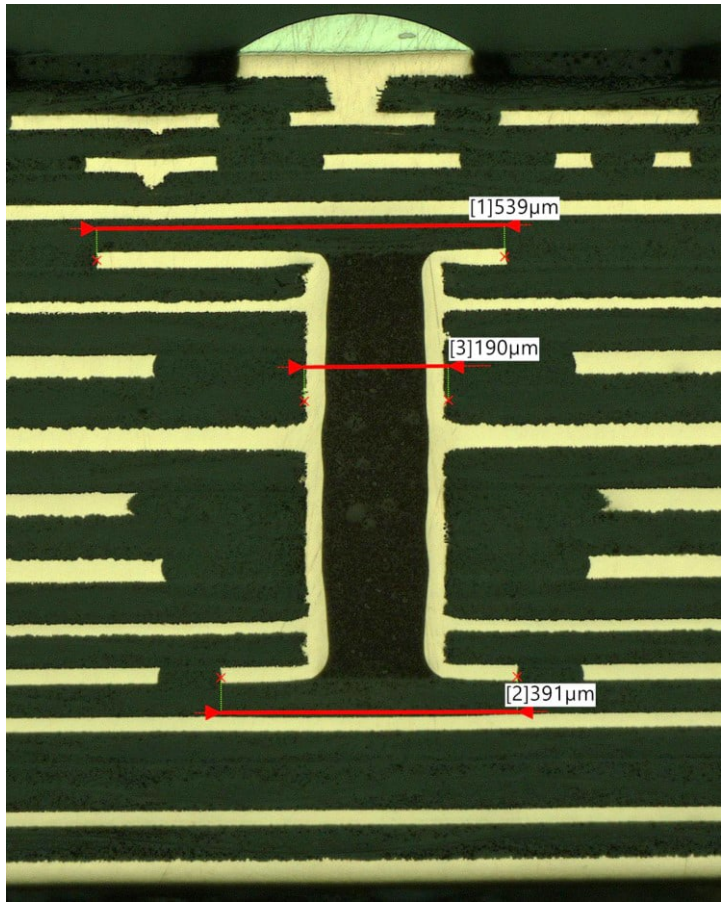


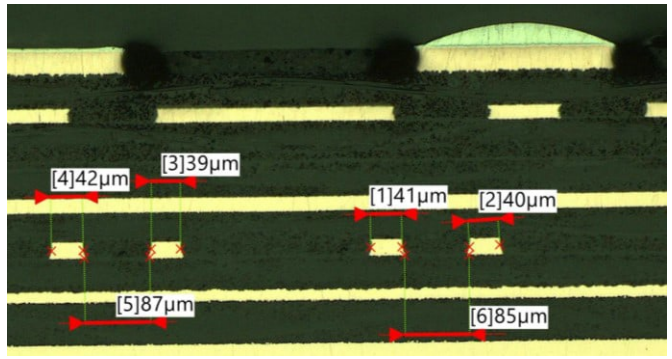


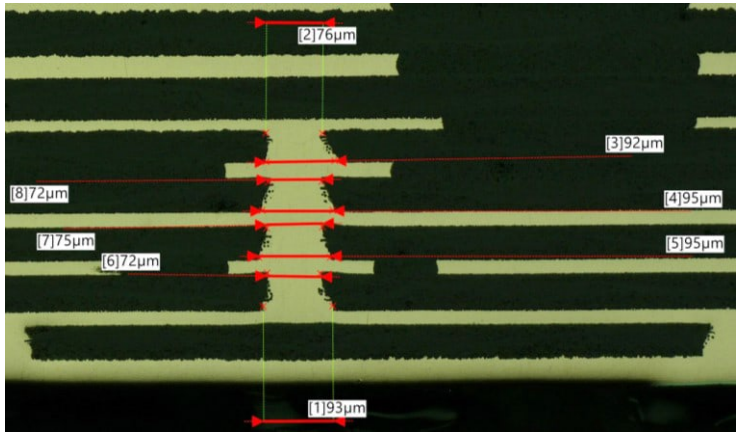
2D X-ray

Apple M1 – Max Board X-Section







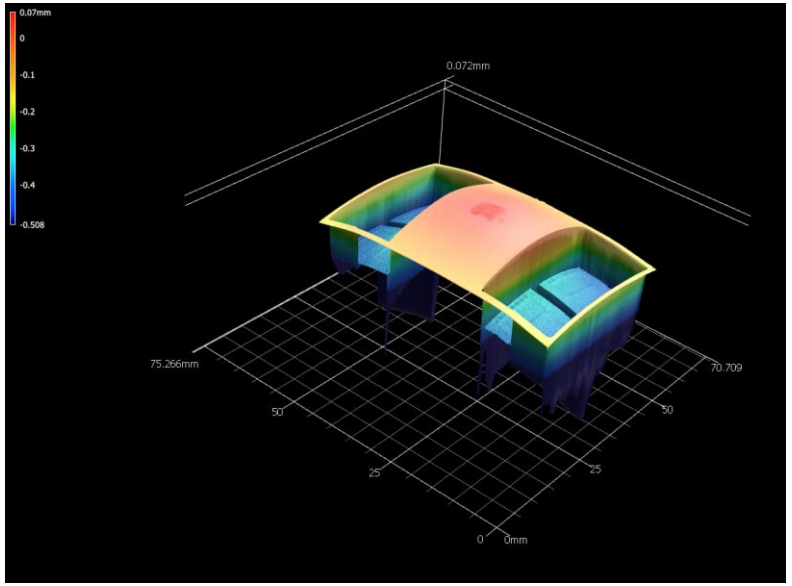


M1-Max Board Layer	Thickness (µm)
FSR	20
1	36
Dielectric	47
2	16
Dielectric	40
3	19
Dielectric	44
4	21
Dielectric	41
5	24
Dielectric	45
6	14
Dielectric	56
7	29
Dielectric	63
8	30
Dielectric	56
9	32
Dielectric	58
10	28
Dielectric	55
11	13
Dielectric	48
12	18
Dielectric	41
13	20
Dielectric	43
14	19
Dielectric	47
15	19
Dielectric	48
16	30
BSR	20

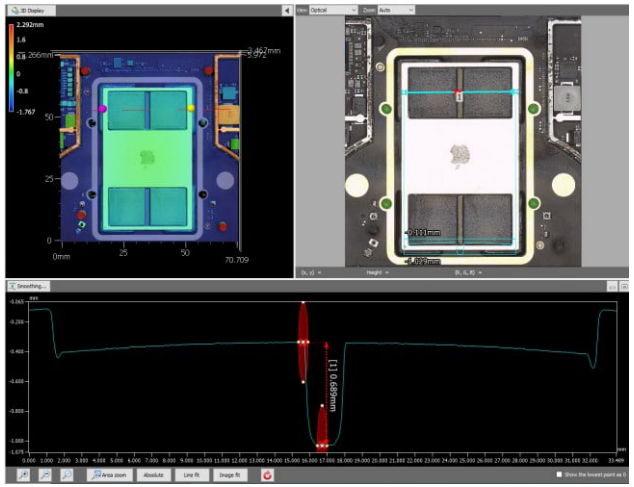
16 layers board, min L/S is 40/85 um, via top/bottom diameter is ~95/70um.

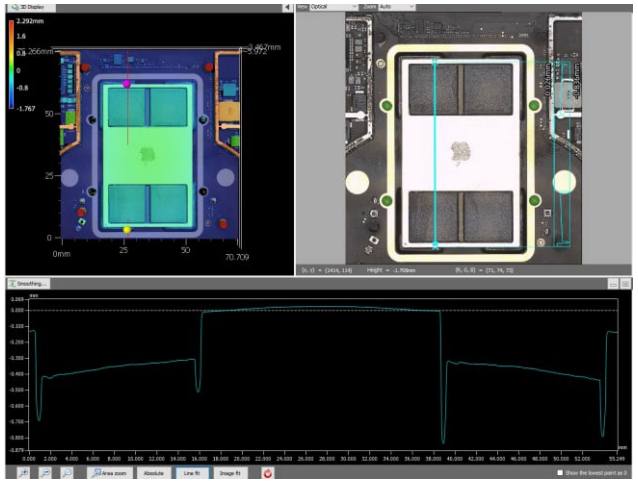
Warpage Profile

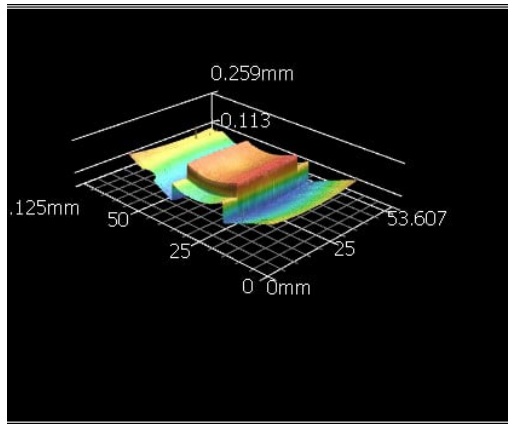
MacBook Pro 16” - M1 Max SoC – Board Top Side: preliminary data



The IHS top surface has 72um convex curvature, package still mounted to the board.



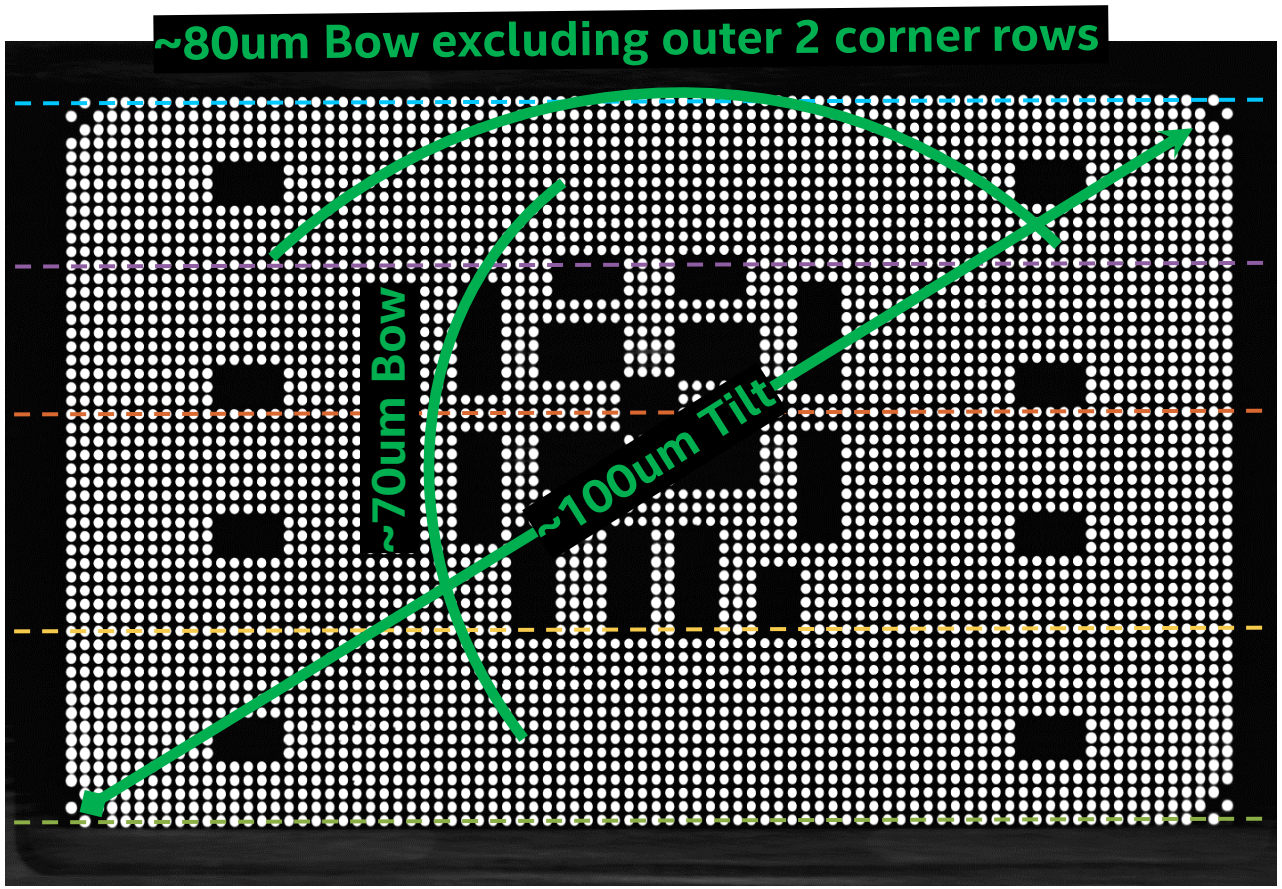


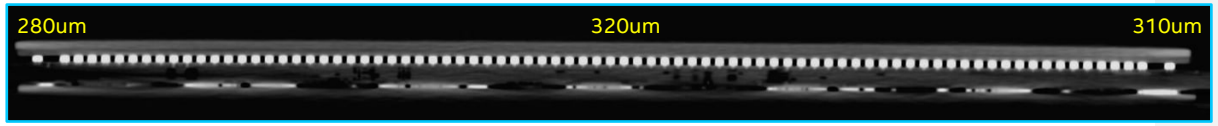


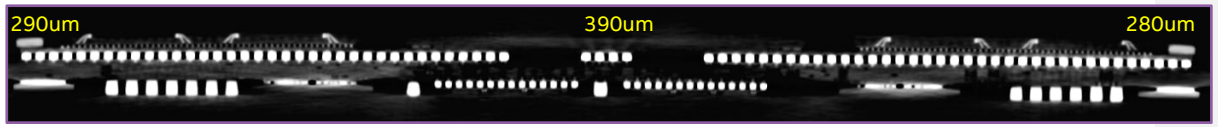
Heat sink flatness and additional measurements are pending.

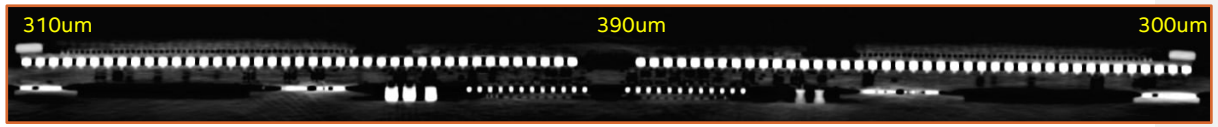
Ack: K.C. Liu

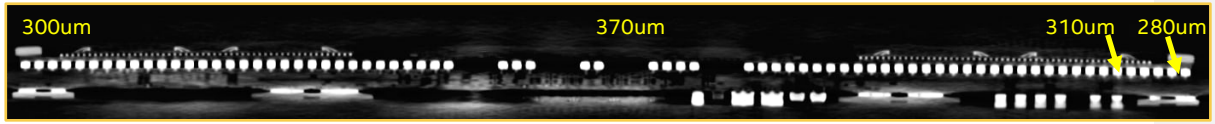
Apple M1 – Max BGA height

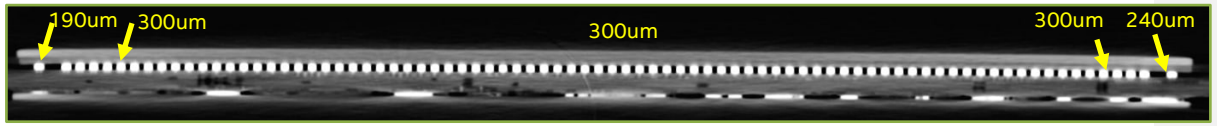










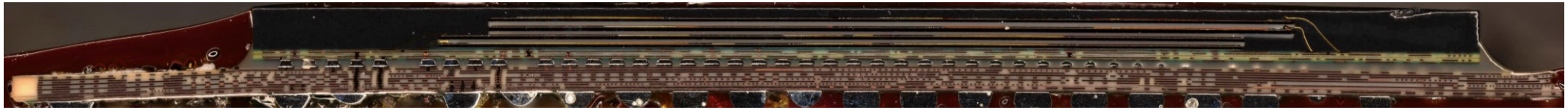


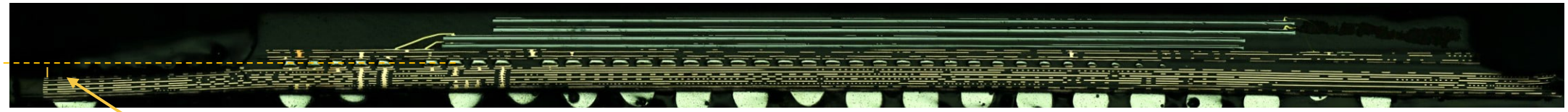
BGA height ranges from 190um to 390um BGA depop, NCTF accommodates severe extreme-corner bending

*Measurements taken using 3D X-Ray scan of the package mounted to the board; the heatsink, package lid and metal frames underneath the board were removed, only the stiffener was still attached.

Apple M1 Pro Package Warpage

Samsung 8GB SKU

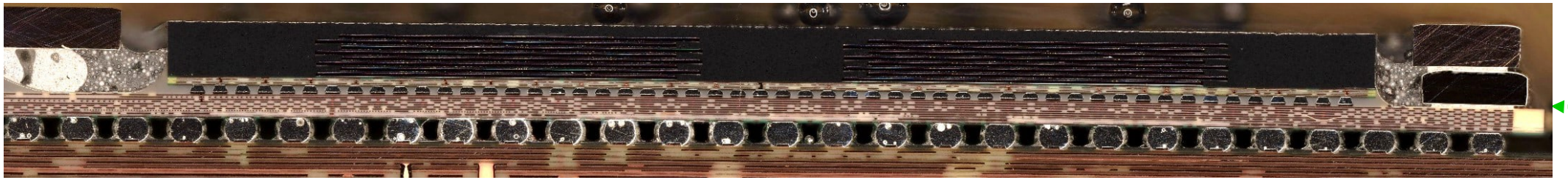




Free standing (No IHS, Stiffener or board)

~130um warpage in outer 3mm edge of freestanding substrate

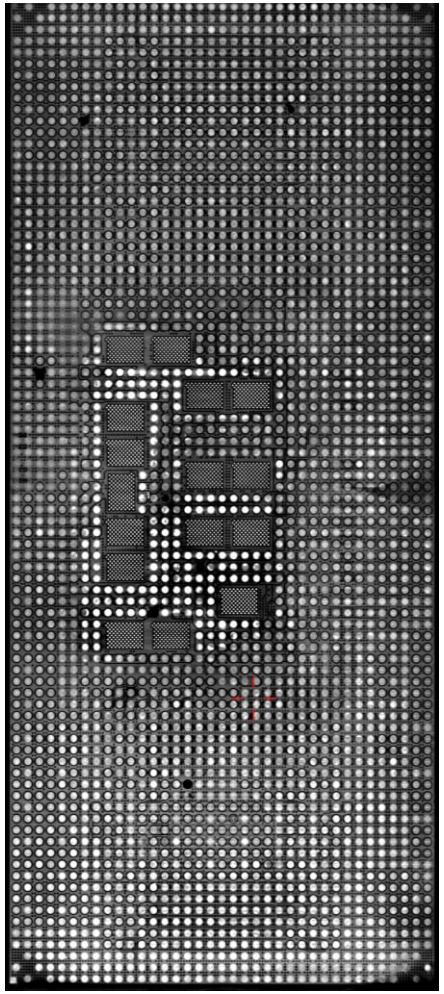
SKHynix 16GB SKU

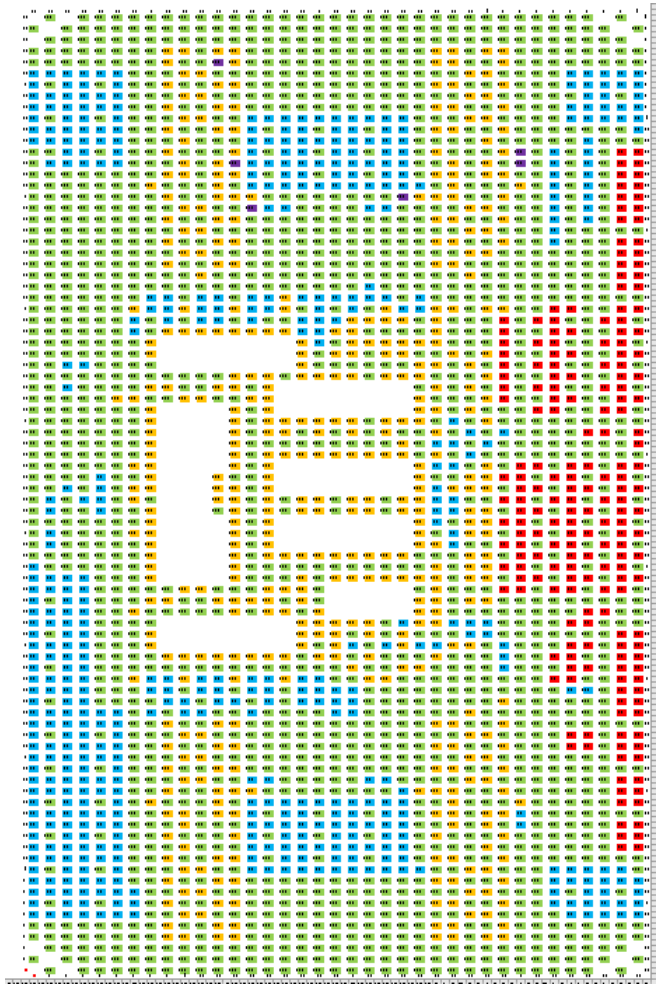


Fully enabled (IHS, Stiffener and board intact)

Stiffener and IHS significantly improve package flatness, although not enough to meet JEDEC standards

Apple M1 Pro Package – Pin Map





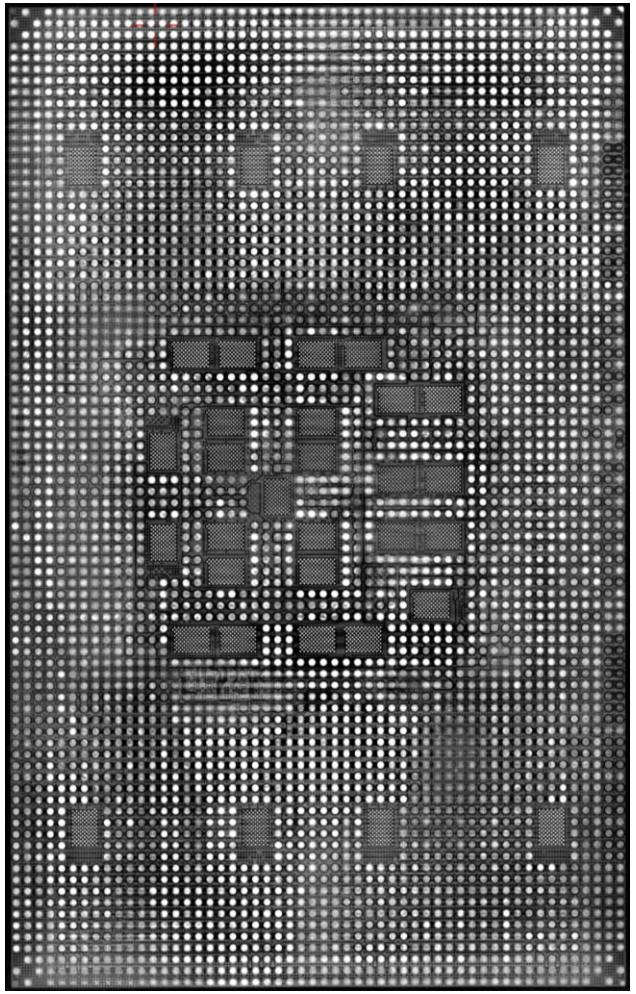
Balls connect to DDR Package Pins	DDR	6
Total Differential pair Signals	DP	198
Total Single Ended	SE	511
No broken out on board SE	NBS	0
No broken out on board DP	NBD	0
Sense Pins or Debug	SOD	0
Power Pin	PWR	476
Ground Pin	VSS	1779
TOTAL # of Pin		2970

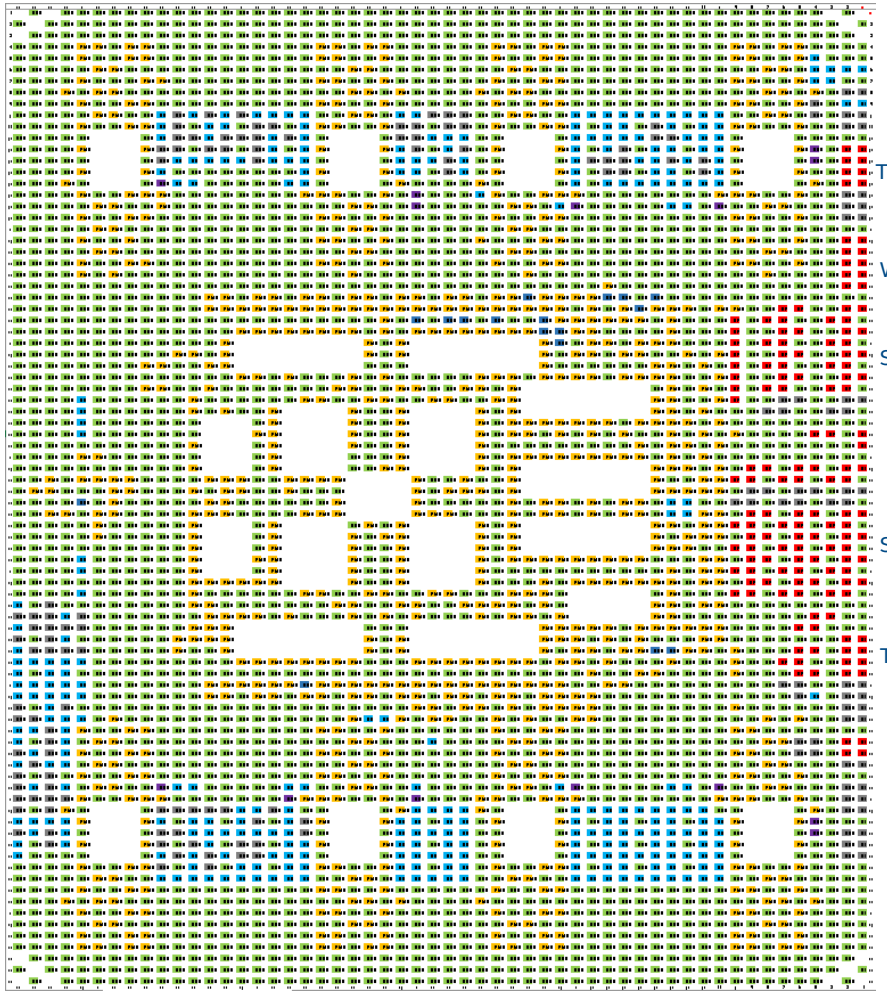
- Total of 2970 pins
- 99 pairs DP signals (198 signals) detected
- 511 single ended signals detected but without board x-ray verification, some error in classify those SE signals may occur
- Not able to identify NBS/NBD and SOD without board x-ray info
- No DTC cavity below DRAM chip on M1 Pro

Ball map was optimized for SMT yield and reliability with ~ 5 rows NCTF

Ack: CSA System - Will, Zaki, Ming Hui, Stephanie

Apple M1 Max Package – Pin Map





Balls connect to DDR Package Pins	DDR	14
Total Differential pair Signals	DP	144
Total Single Ended	SE	307
No broken out on board SE	NBS	111
No broken out on board DP	NBD	54
Sense Pins or Debug	SOD	17
Power Pin	PWR	908
Ground Pin	VSS	2628
TOTAL # of Pin		4183

- Total of 4183 pins
- Total of 99 pairs DP signals (198 signals) and 72 pairs DP signals routed on board
- Total of 418 single ended signals detected and 304 signals routed on board
- Note presence of DCs beneath DRAMs

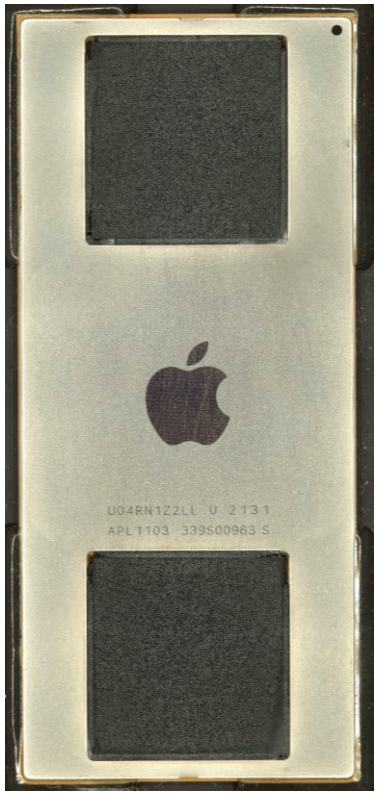
Excel pinmap file: M1_Max_Pinmap

Ball map was optimized for SMT yield and reliability with 3-4 rows NCTF

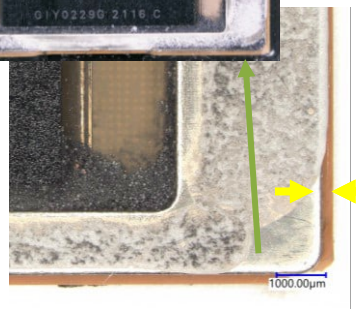
Ack: CSA System - Will, Zaki, Ming Hui, Stephanie

Apple M1 Pro MoP Assembly Flow

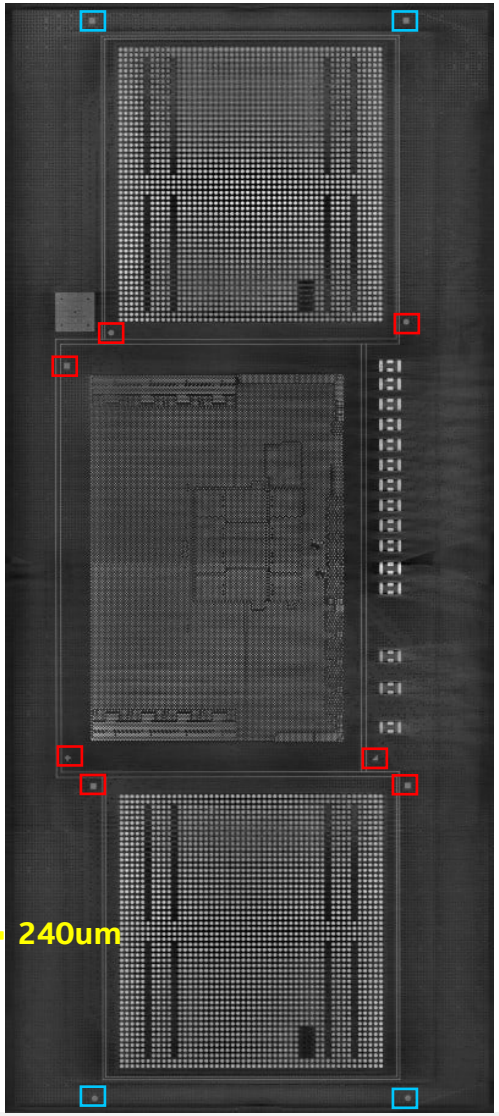
Fully Assembled M1 Pro Package



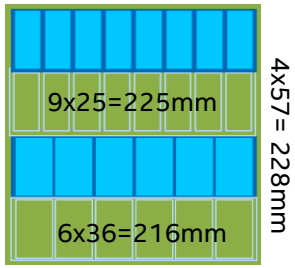
IHS removed



3D Xray- Top Substrate Layer



4 strips of 1x9-Pro or 1x6-Max substrates could fit in standard ¼ panel with equivalent to singulated panel utilization



~240x245mm ¼ panel useable area

*7 fiducials underneath IHS

*4 fiducials underneath the IHS and stiffener

- DRAMs were attached before stiffener ring covered key fiducials.
- Assembly may have been done in strips to support tight stiffener-edge tolerance.

Package Assembly Flow :

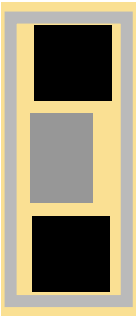
1. Pick & place SoC die- Underfill & cure

2. Pick & place DRAM package (x2)- Underfill & cure

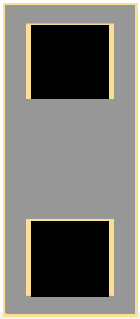
3. Pick & place SMD Components- Underfill & cure

Bottom side of substrate

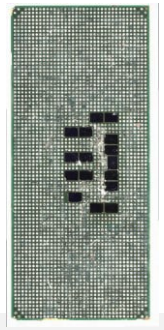
4. Apply stiffener adhesive- pick & place stiffener



5. Apply TIM1 & IHS adhesive- pick & place IHS

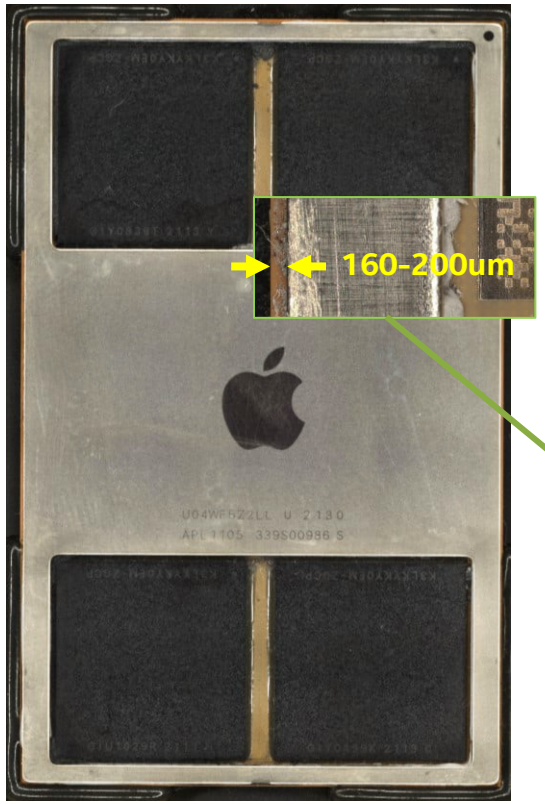


6. BGA solder drop & Test



Apple M1 Max MoP Assembly Flow

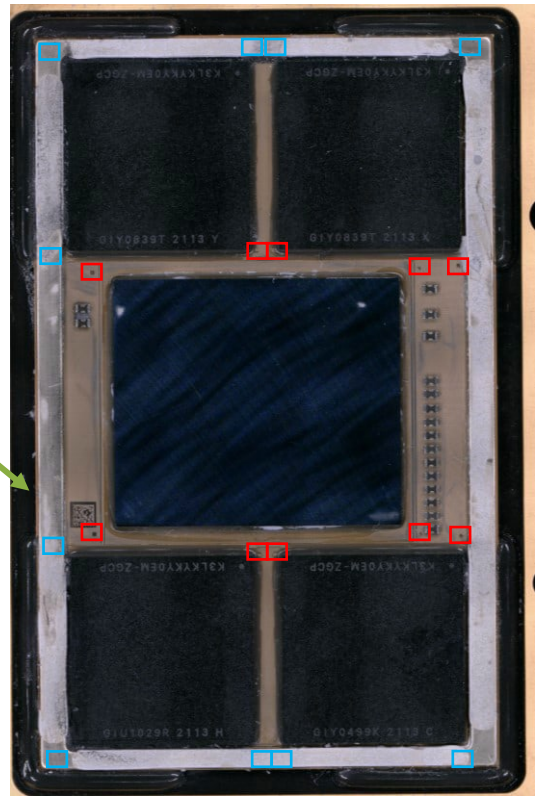
Fully Assembled M1 Max Package



195um

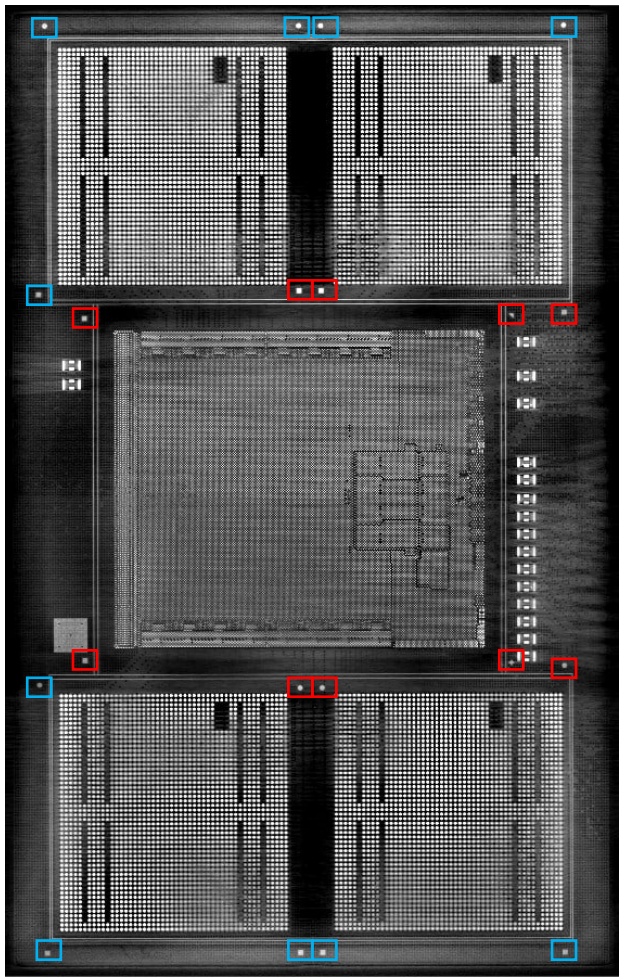
IHS removed

135um



- DRAMs were attached before stiffener ring covered key fiducials.
- Assembly may have been done in strips to support tight stiffener-edge tolerance.

3D Xray- Top Substrate Layer

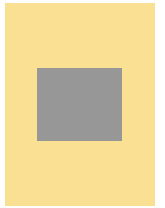


*10 fiducials underneath IHS

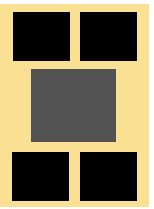
*10 fiducials underneath IHS & stiffener

Package Assembly Flow :

1. Pick & place SoC die- Underfill & cure

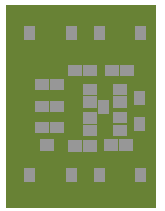


2. Pick & place DRAM package (x4)- Underfill & cure

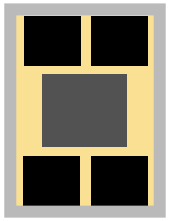


3. Pick & place SMD Components- Underfill & cure

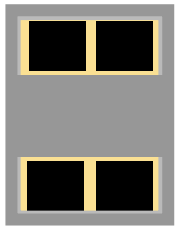
Bottom side of substrate



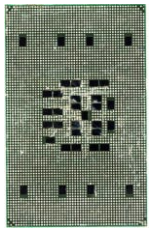
4. Apply stiffener adhesive- pick & place stiffener



5. Apply TIM1 & IHS adhesive- pick & place IHS



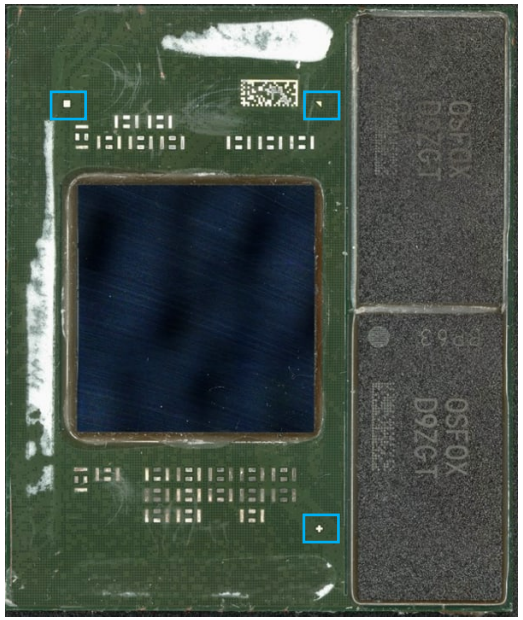
6. BGA solder drop, singulation & Test



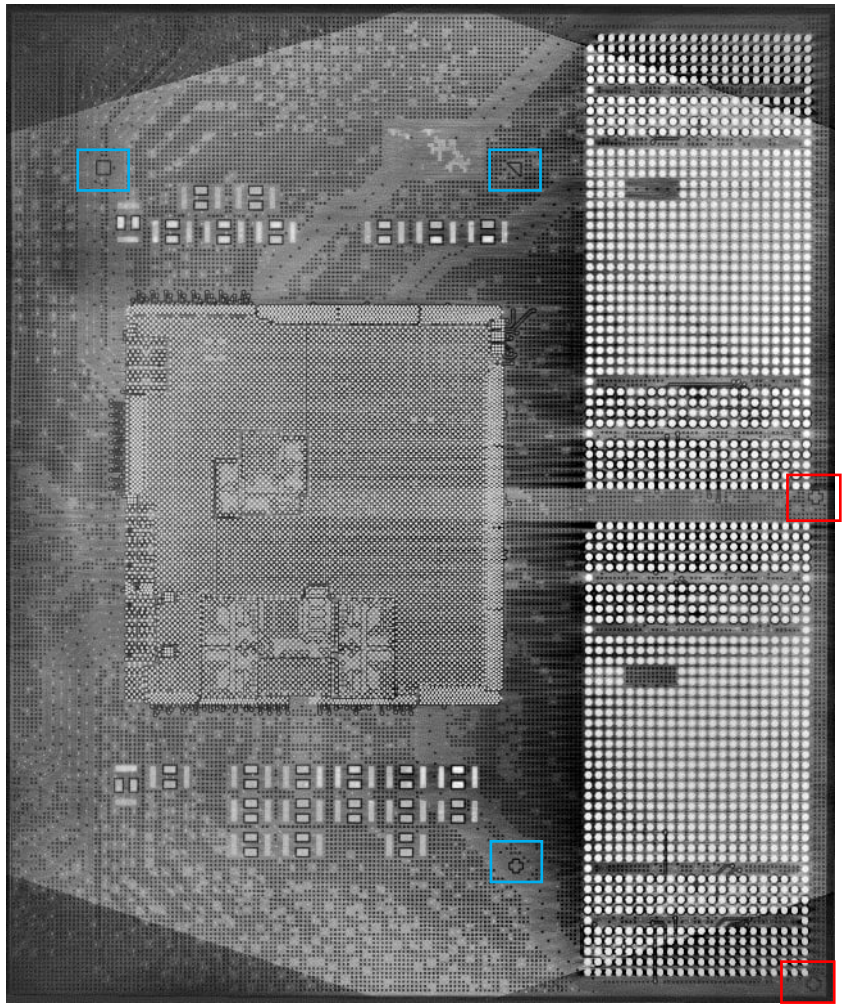
Apple M1 MoP Assembly Flow

Fully Assembled M1 Package

Half IHS removed



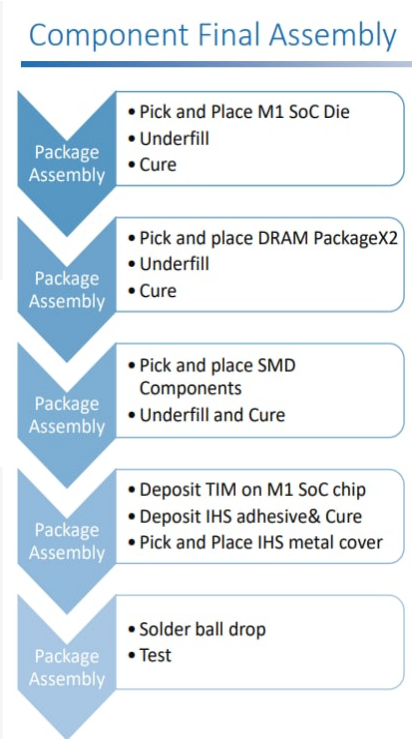
3D Xray- Top Substrate Layer



Due to location of fiducials underneath the IHS, we can deduce DRAMs are attached after SoC die and before IHS assembly.

Cored BGA substrate has adequate rigidity to tolerate 250um IHS to substrate edge tolerances in singulated assembly flow.

Package Assembly Flow:



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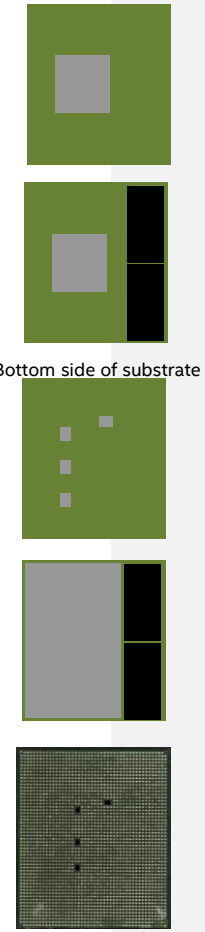


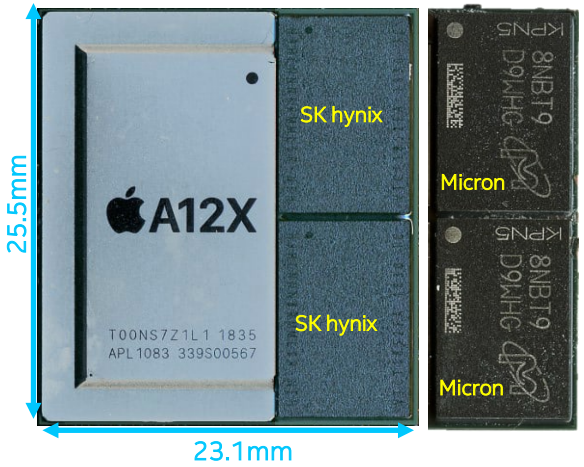
Bottom side of substrate

*1 fiducial at the corner of each DRAM package

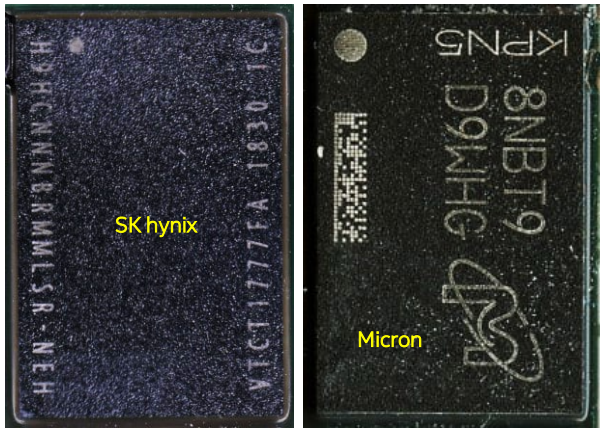
*3 fiducials underneath the IHS

Apple A12X -M1- M1 Pro/Max - LPDDR Memory Packages

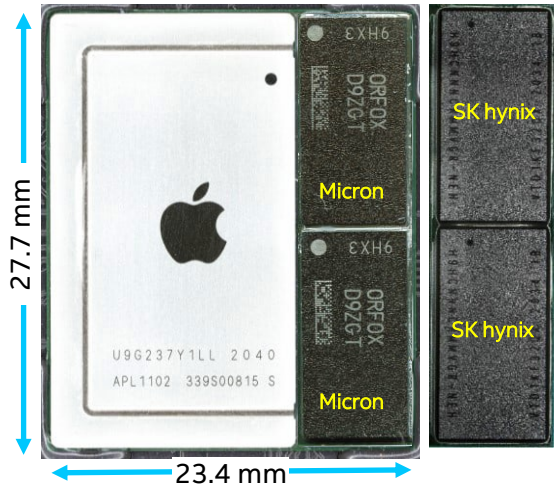
A12X



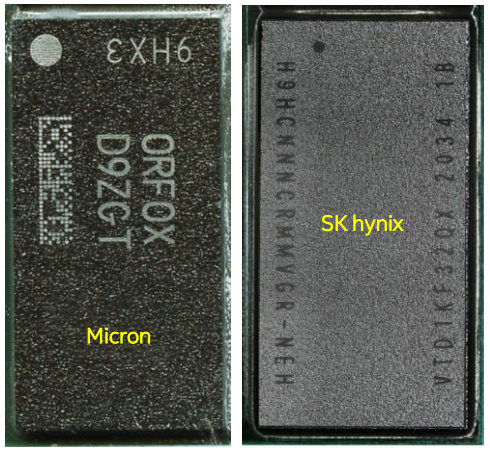
- Package Size=23.1x25.5mm
- Die Size = 10.2x12.6 mm
- Memory Size= 8x12mm
- 19 0402 3 terminal DSC's



M1



- Package Size=23.4x27.7mm
- Die Size = ~10.9x11.4mm
- Memory Size= ~6.6x13.2mm
- 24 0402 3 terminal DSC's



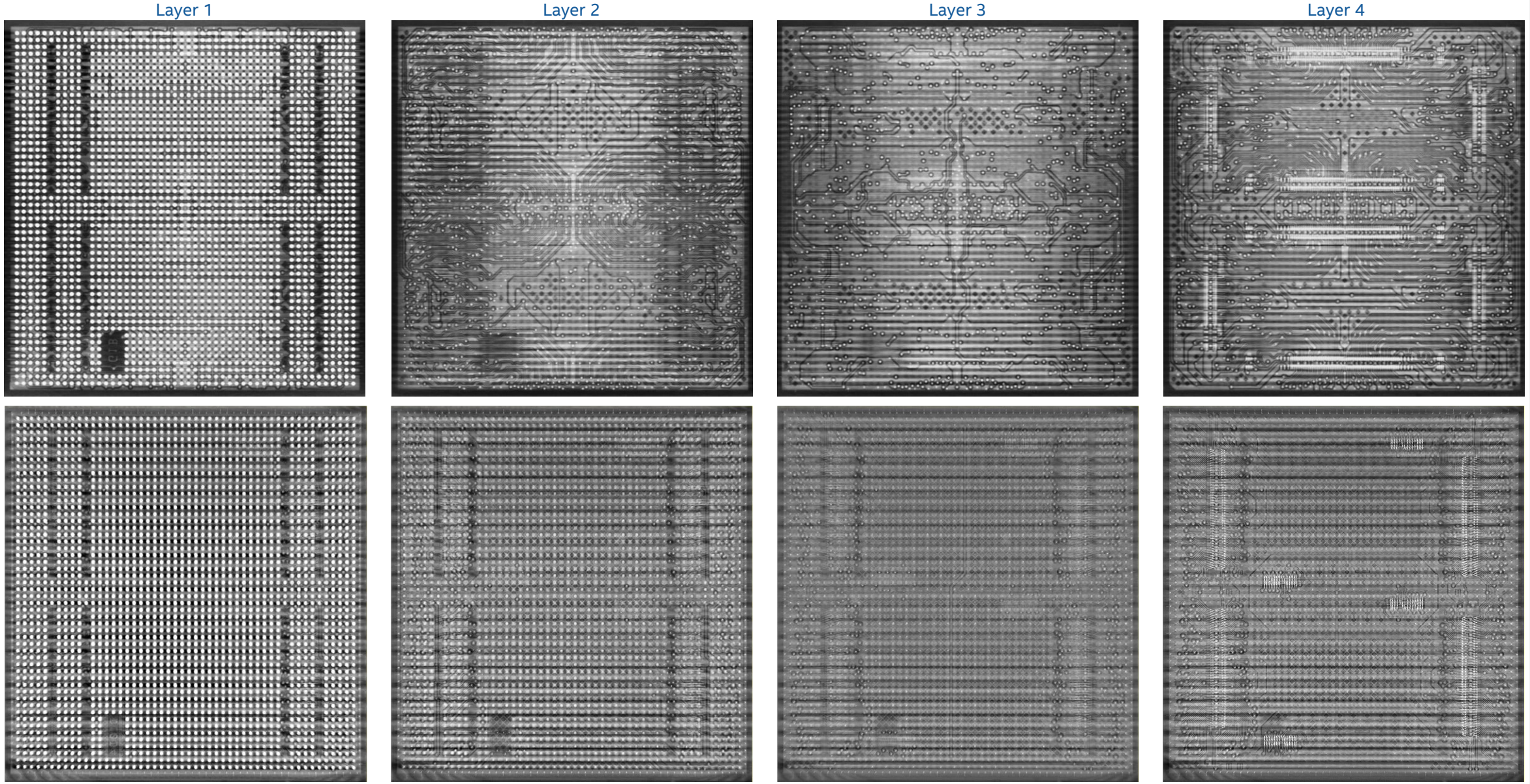
M1 Max

*Complete DRAM Package image not captured.

- Package Size=56.8x35.7mm
- Die Size = 19x22mm
- Memory Size= 14.4x13.9
- 17 0603 3T DSC's

We cannot rule out the use of Micron DRAMs on M1 Pro/Max

Apple M1 Pro/Max LPDDR5 *8GB vs 16GB DRAM* Package Differences

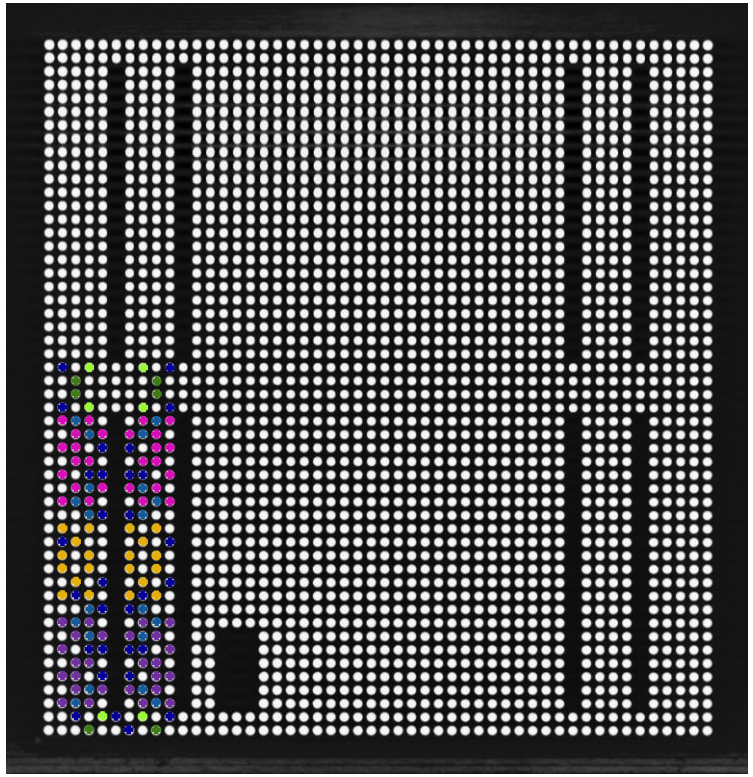


Different DRAM supplier using same ball array/qty and substrate layer count but different substrate design and die features (wire bonding locations/pinout, die qty, die stack arrange, total height, etc.).

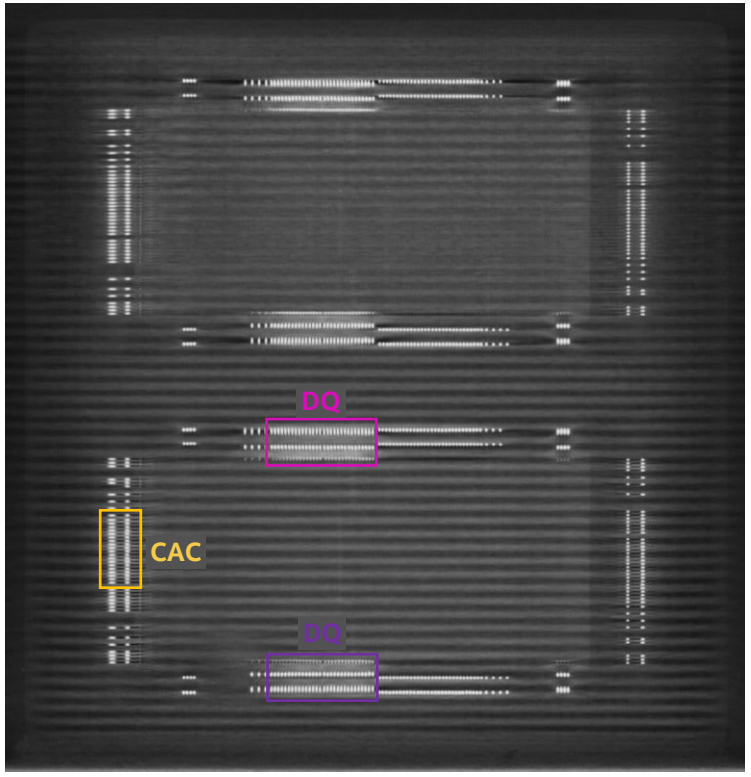
Contact ATTD C/A for access to the full high-resolution images.

Apple M1 Pro/Max LPDDR5 Wire Bonding Differences

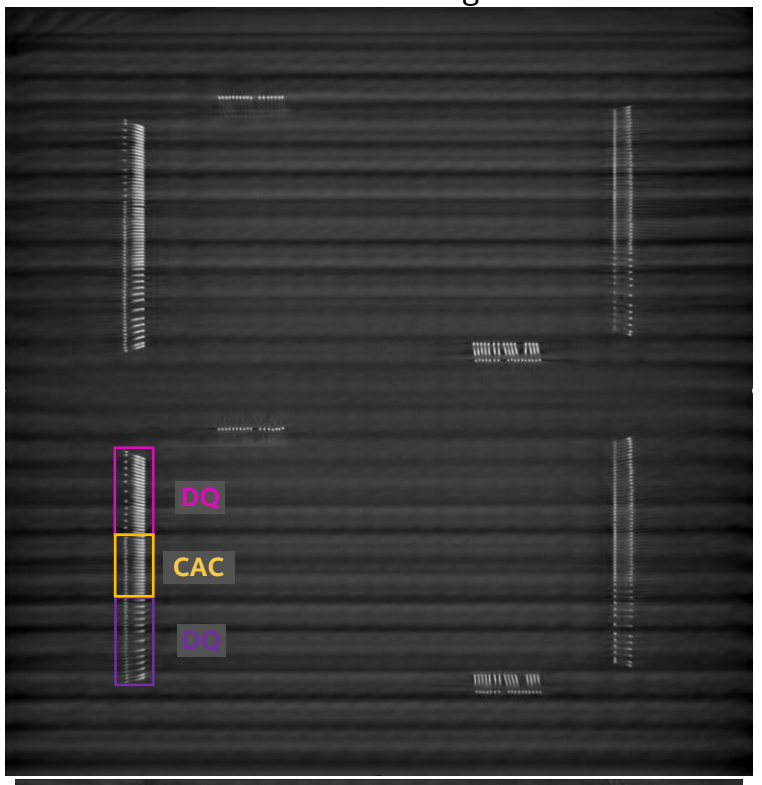
BGA qty = 2406



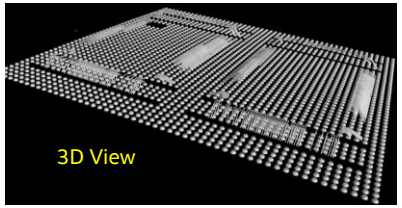
8GB DRAM Package
Wire Bonding



16GB DRAM Package
Wire Bonding



- **M1 Pro:** 16GB capacity system
  2 Samsung 8GB-DRAM packages- 8 die each/16 total
- **M1 Pro:** 32GB capacity system
  2 SK Hynix 16GB-DRAM package – 16 die each/32 total
- **M1 Max:** 32GB capacity system
  4 Samsung 8GB-DRAM packages – 8 die each/32 total

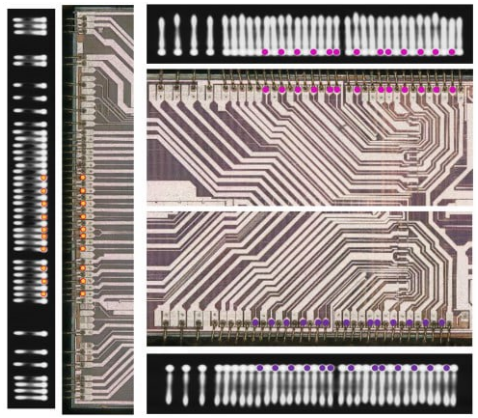


Different DRAM suppliers using same ball map, but different die and different wire bonding techniques including FoW, staggered, etc.

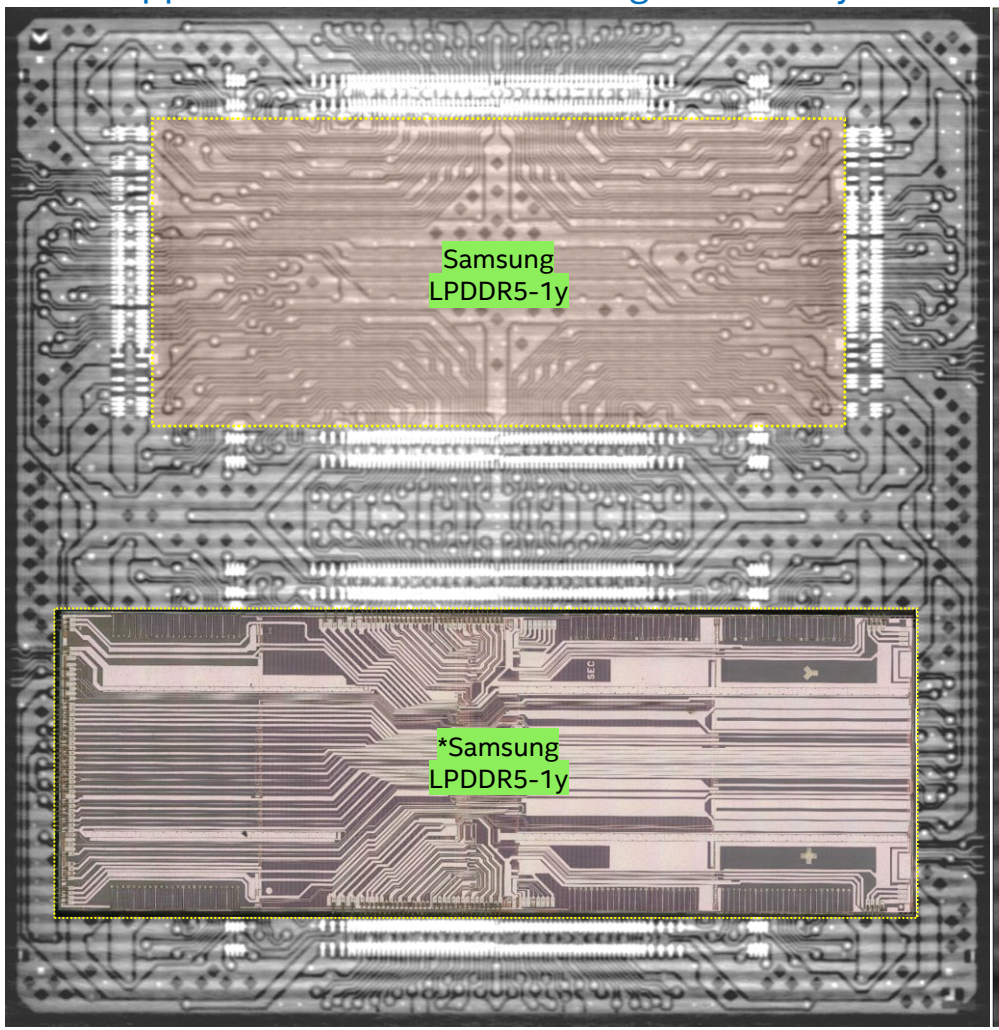
- Each DQ group has13 signals
- Each CAC group has 10 signals

Apple M1 Pro/Max LPDDR5 Die Differences

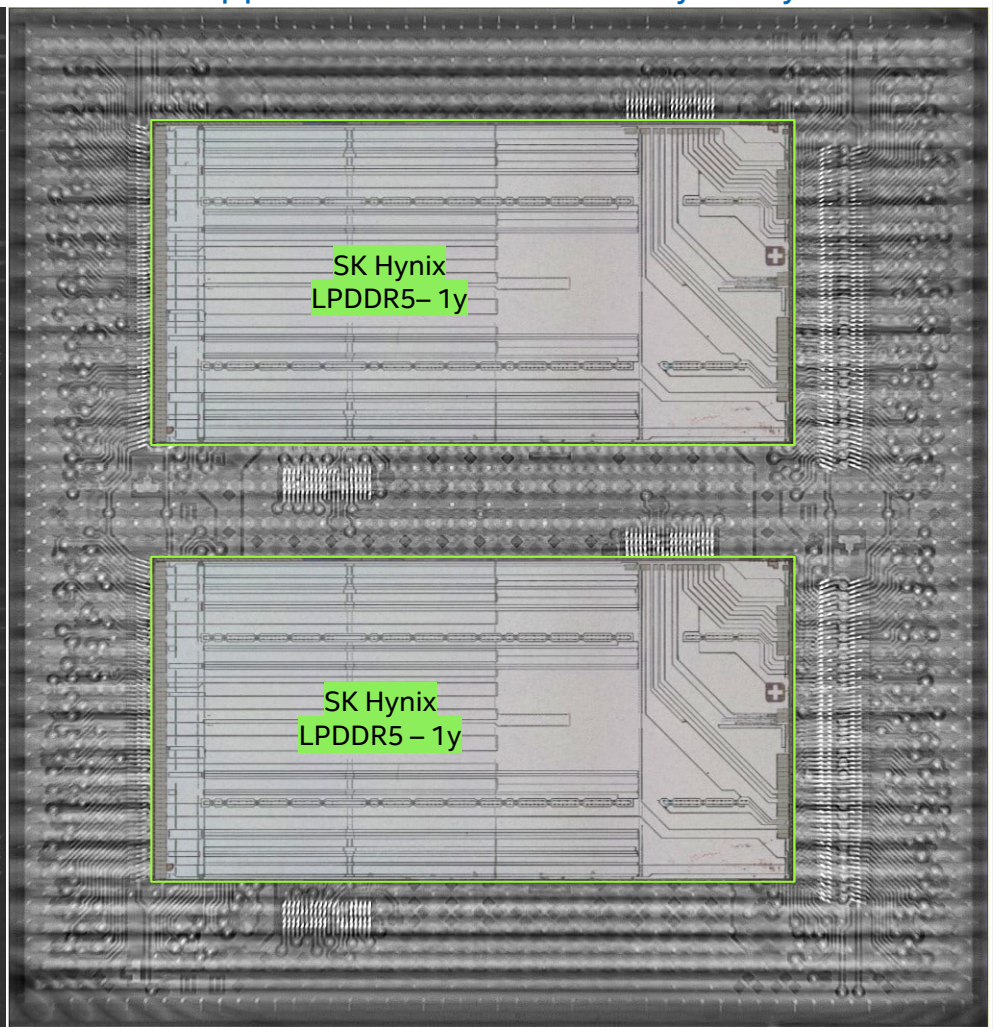
*8GB die wire bonding pinout matches with the 12GB die.



Apple – 8GB DRAM → Samsung LPDDR5-1y

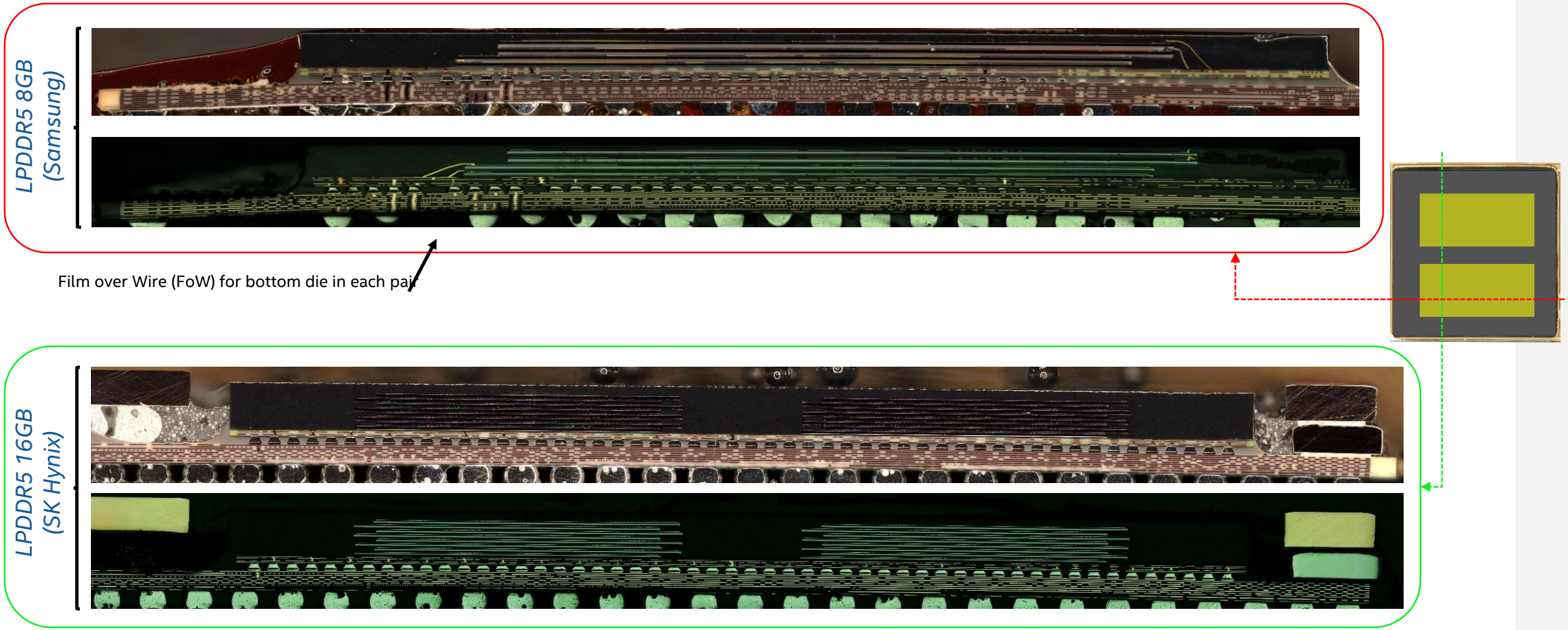


Apple – 16GB DRAM → SK Hynix-1y



- The 8GB DRAM package have 8 dice total, the wire bonding location and pinout qty is similar to the Samsung LPDDR5-1y die (*the die image corresponds to a 12GB die version).
- The 16GB DRAM package have 16 dice total, the wire bonding location, pinout and die size is the same to the SK Hynix LPDDDR5-1y die.

Apple M1 Pro/Max LPDDR5 *8GB vs 16GB DRAM* Package Differences

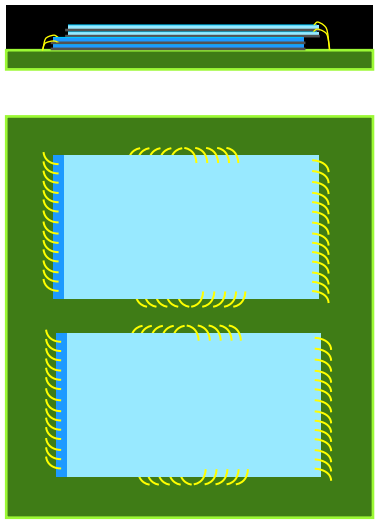


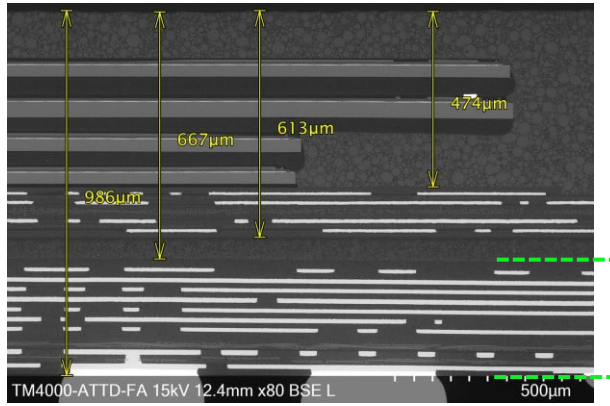
Different DRAM suppliers use different die stack arrange, *details on next slide*.

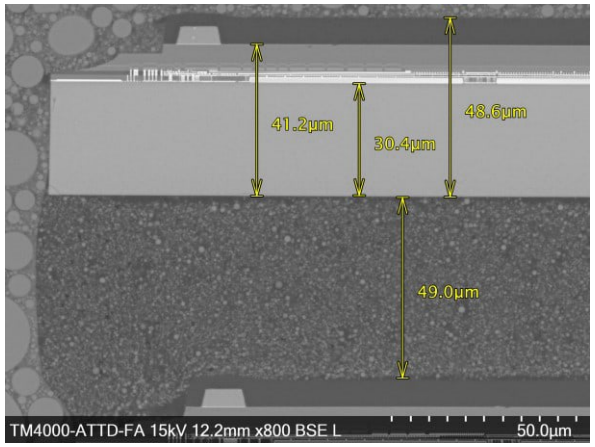
- The Samsung 8GB package have 4 dice stack (8 dice total) as for the SK Hynix 16GB package, it have 8 dice stack (16 dice total).

Apple M1 Pro/Max LPDDR5 *8GB vs 16GB DRAM* Package Differences

LPDDR5 8GB (Samsung)

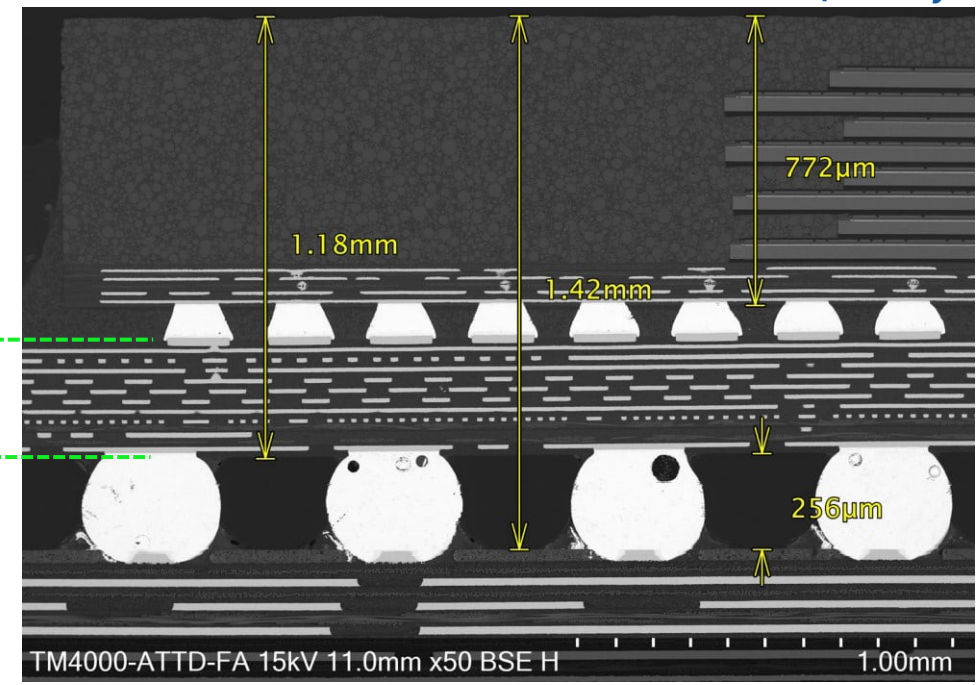


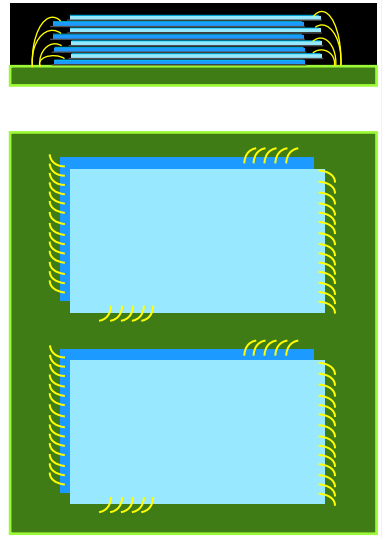




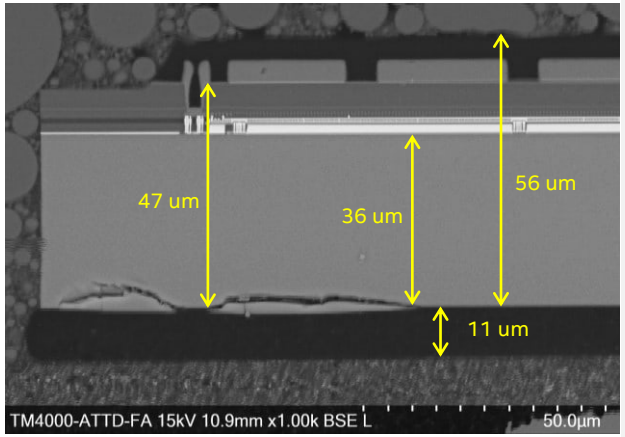
- 4 die stack up – 8 die total → Package height 613um.
- 1 pair of dice aligned per side and then another pair shifted on X axis only.
- Die thickness ~49um, bulk silicon thick ~30um and attach film thick ~ 50um.

LPDDR5 16GB (SK Hynix)

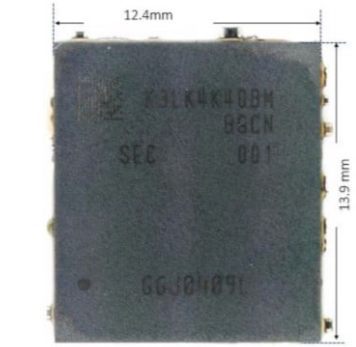




- 8 die stack up – 16 die total → Package height 772um.
- Each die is shifted at both axis
- Die thickness ~56um, bulk silicon thick ~36um and attach film thick ~11um.



LPDDR5 Package/Die Comparison



Samsung 12GB 1y LPDDR5
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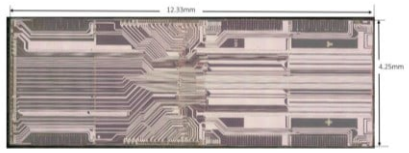

Samsung 12G 1y LPDDR5
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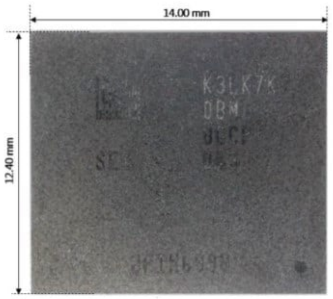

Samsung 8GB 1z LPDDR5
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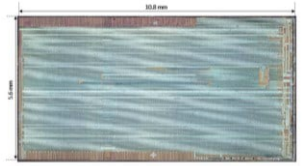

Samsung 16Gb 1z LPDDR5
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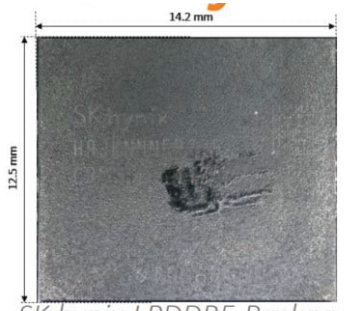
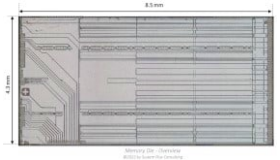
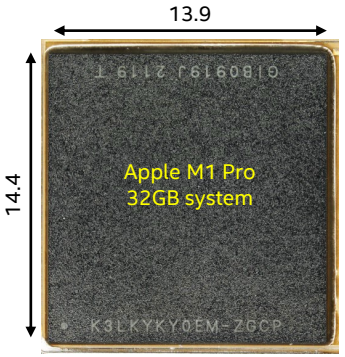


SK hynix LPDDR5 Package
©2022 by System Plus Consulting

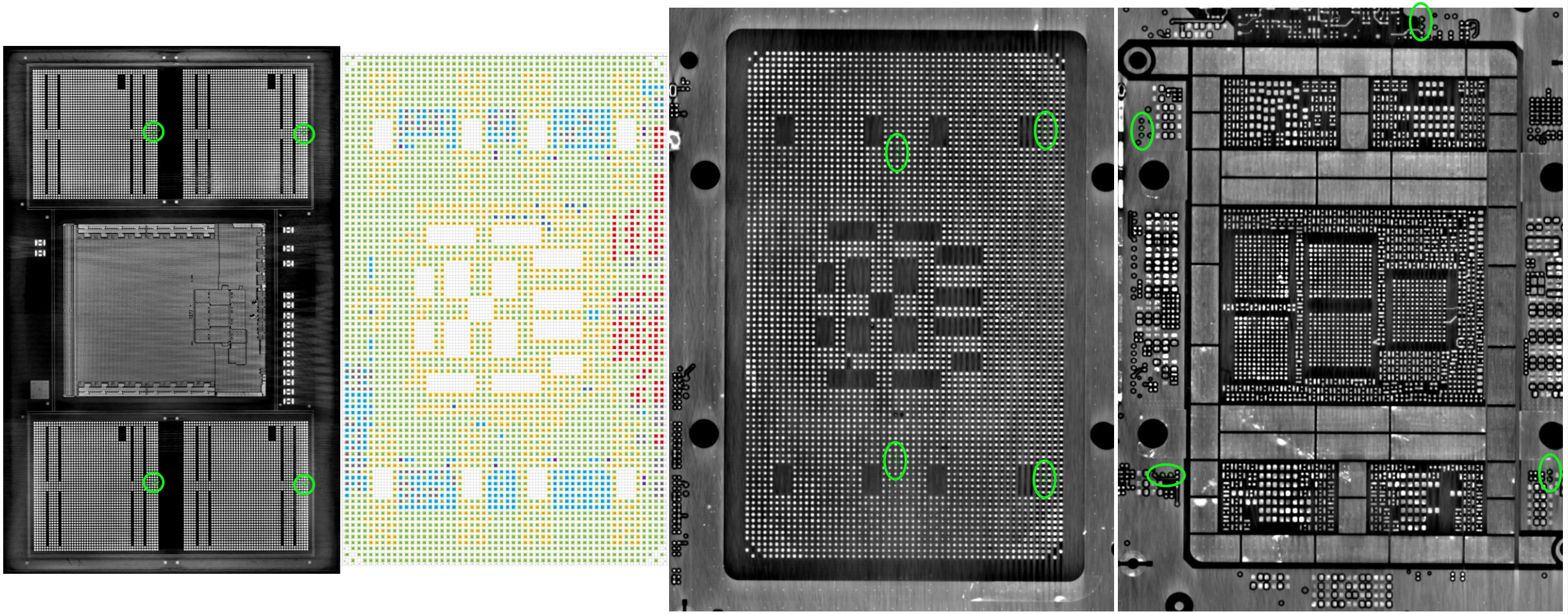




	Samsung LPDDR5 1y	Samsung LPDDR5 1z	SK Hynix LPDDR5 1y	(Apple M1 Pro/Max – 8GB) Samsung - LPDDR5-1y	(Apple M1 Pro/Max – 16GB) SK Hynix - LPDDR5-1y
Package Capacity	12 GB	8GB	8GB	8GB	16GB
Package Type	BGA 496 balls	BGA 496 balls	BGA 496 balls	BGA 2406 balls	BGA 2406 balls
Dimensions	13.9x12.4 mm	14x12.4 mm	14.2x12.5	14.4x13.9 mm	14.4x13.9 mm
Package Thickness	0.6 mm	0.38 mm	0.5	**0.63 mm**	**0.77 mm**
Package surface area	172.36 mm2	173.6 mm2	177.5 mm2	200.2 mm2	200.2 mm2
Dies in package	8	4	**8**	**8**	**16**
Die capacity	12Gb/1.5GB	16Gb/2GB	8Gb		
Die dimensions	12.33x4.25 mm	10.8x5.6 mm	8.5x4.3 mm	9x4.25 mm	8.5x4.3 mm
Die area	52.4 mm2	60.5 mm2	36.55 mm2	38.3 mm2	36.3 mm2
Die density	0.23 Gb/mm2	0.264 Gb/mm2	0.22 Gb/mm2		0.22 Gb/mm2
Potential dies per wafer	1204	1048	1760		1760
Potential capacity per wafer	14448 Gb/300mm wafer	16768 Gb/300mm wafer	14080 Gb/300mm wafer		14080 Gb/300 mm wafer

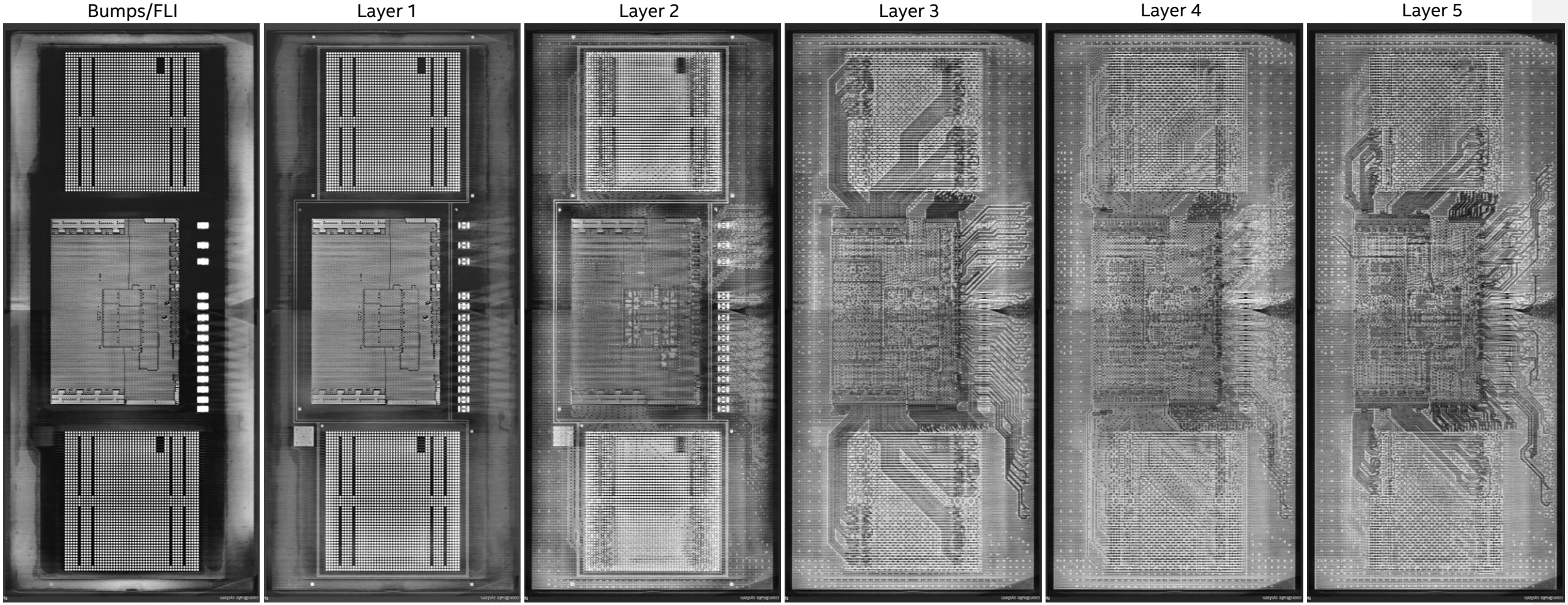
- The custom Apple LPDDR5 package is different in size and BGA qty to other Samsung LPDDR5 packages commercially available.
- Apple is using two different DRAM suppliers, Samsung and SK Hynix; both using an organic substrate with 4 layers, but different layer design and pinout/die wire-bonding locations.
- The 8GB DRAM package have 8 total die, the wire bonding location and pinout qty is similar to the Samsung LPDDR5-1y die.
- The 16GB DRAM package have 16 total die, the wire bonding location and pinout qty is similar to the SK Hynix LPDDR5-1y die.

Apple M1 Max SoC Substrate – DRAM Test Point



Some DRAM pads are connected thru the substrate to PCB board bottom side test pads, those may be used for electrical test.

Apple M1 Pro SoC Substrate - 3D X-Ray

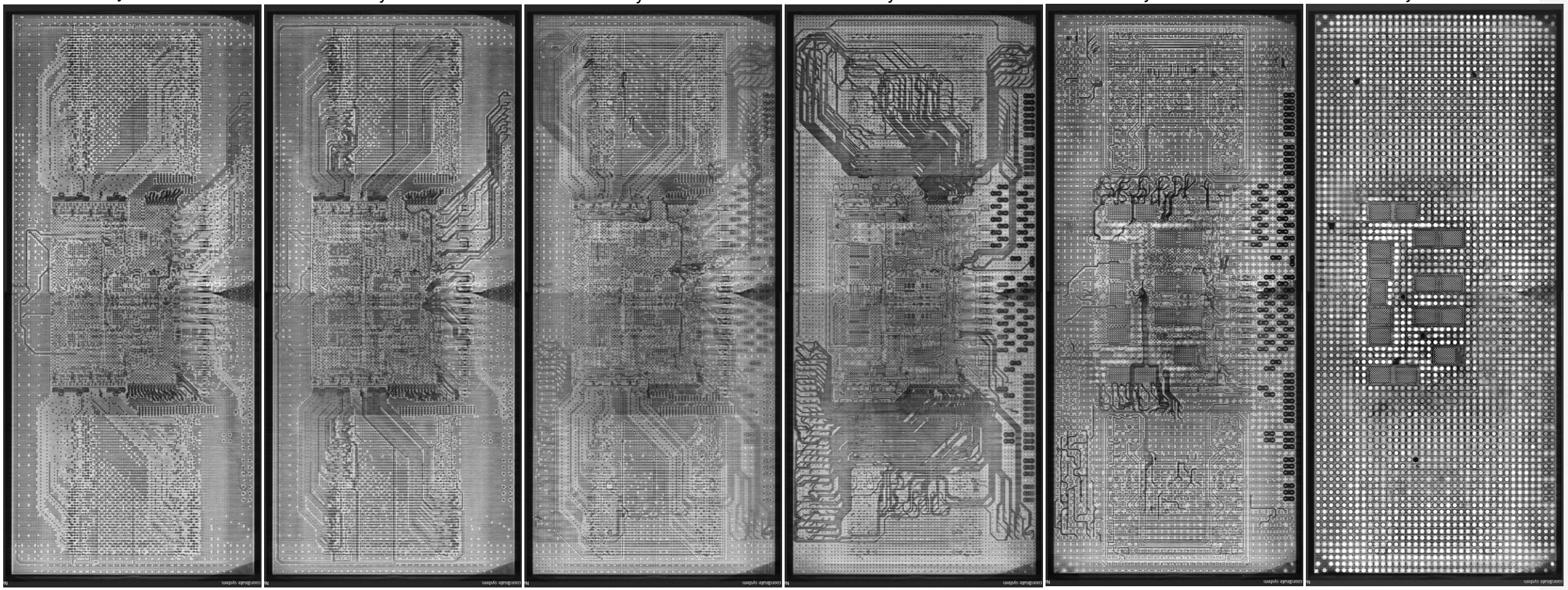


- 11-layers Coreless substrate.
- Layer 1 is used only for bump pads, fiducials, epoxy dams and 2D ID laser mark pad.
- DDR and high speed I/O routing on layers 3, 5 and 7; layer 9 have the rest of the routing signals.
- 21 power rails from 2 PMICs are distributed in the substrate.

Contact ATTD C/A for access to the full high-resolution images.

Apple M1 Pro SoC Substrate - 3D X-Ray

Layer 6 | Layer 7 | Layer 8 | Layer 9 | Layer 10 | Layer 11



- 11-layers Coreless substrate.
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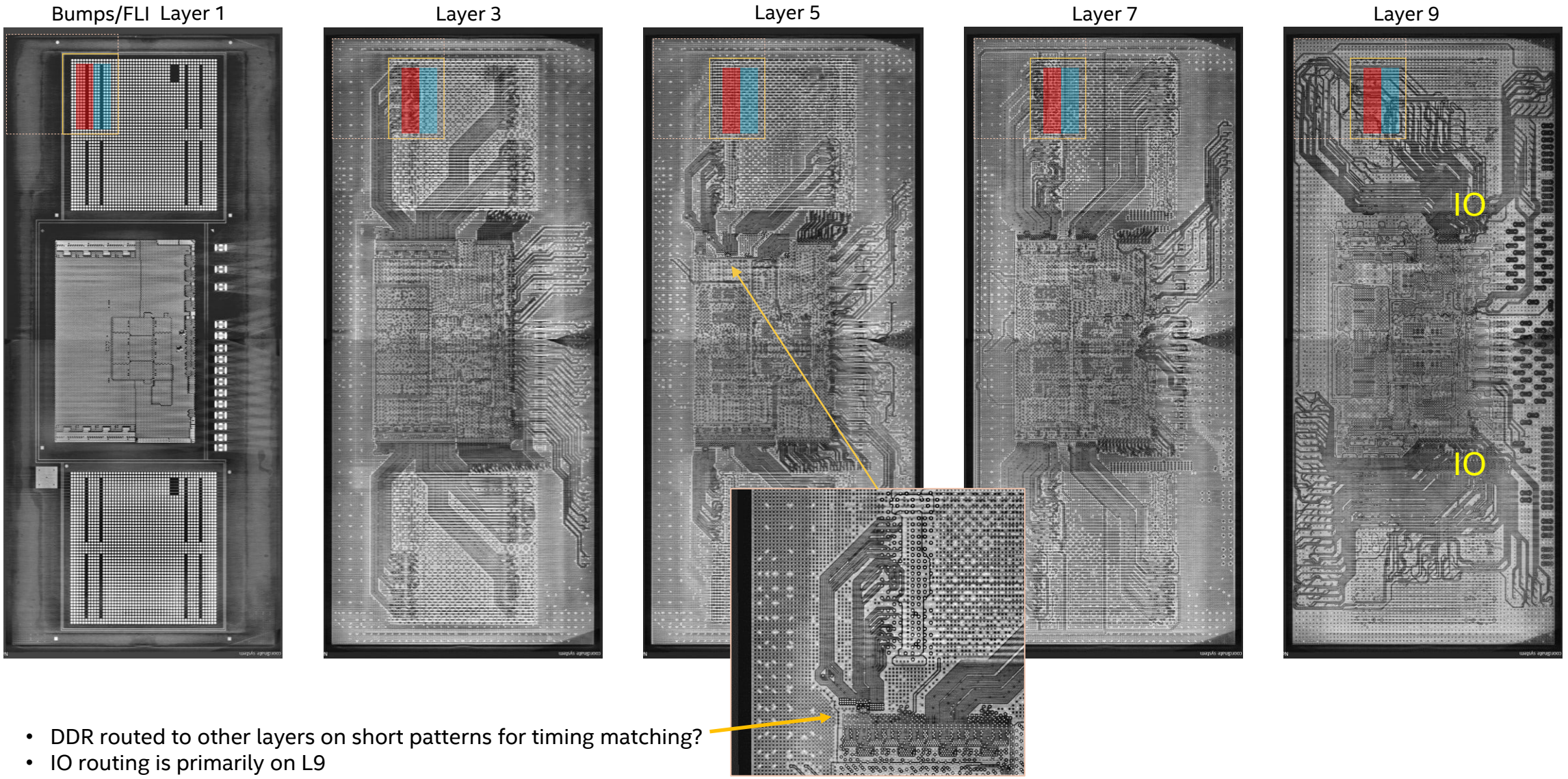
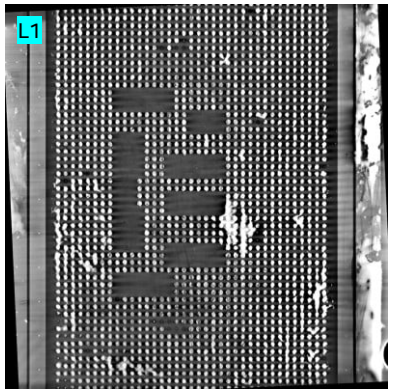
Contact ATTD C/A for access to the full high-resolution images.

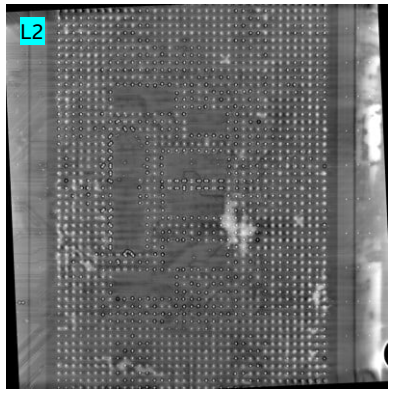
Apple M1 Pro SoC Substrate - 3D X-Ray: DDR/IO Focus

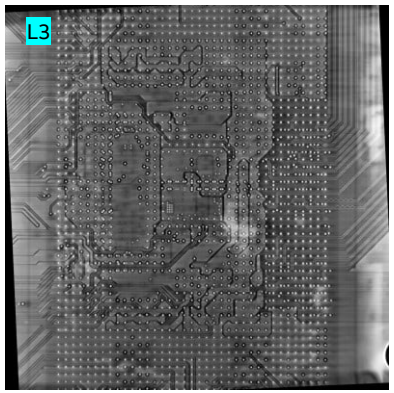


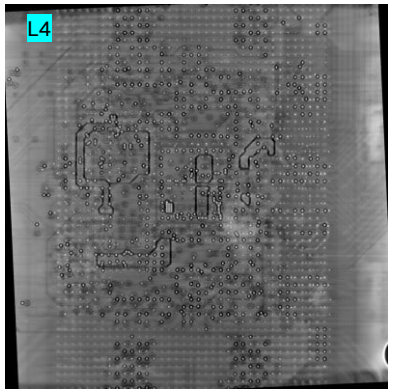
- DDR routed to other layers on short patterns for timing matching?
- IO routing is primarily on L9

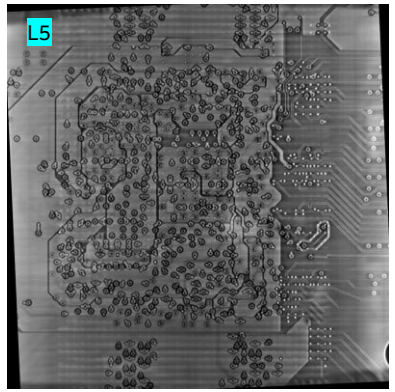
Apple MacBook 14” – M1 Pro Board - 3D X-Ray

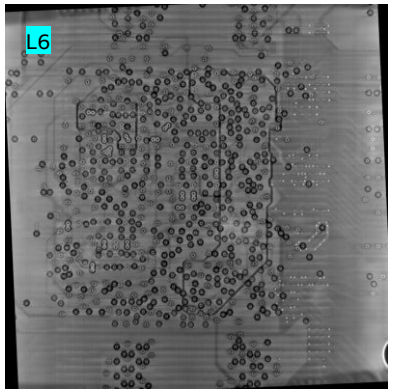


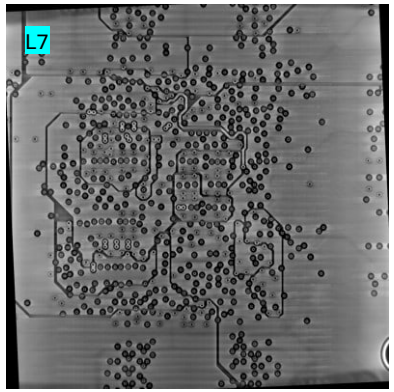


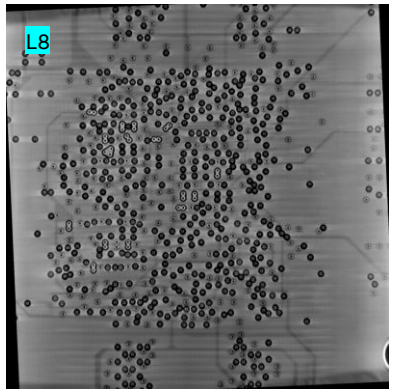


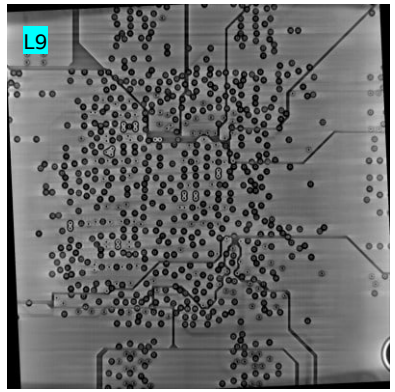


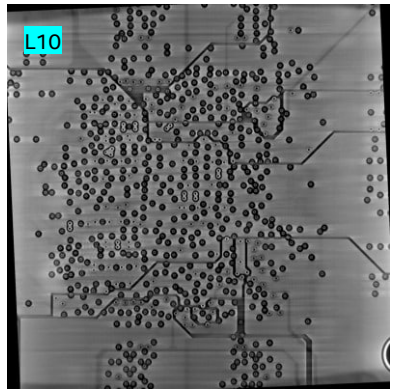


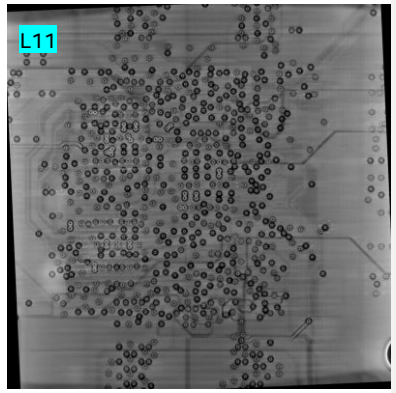


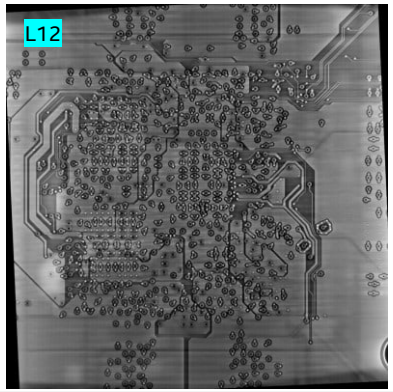


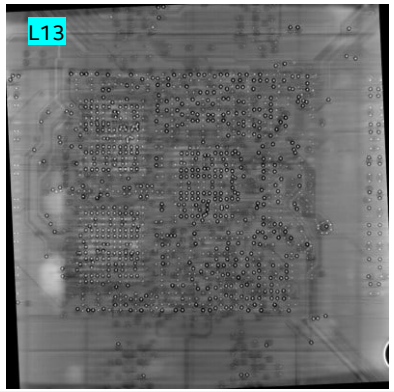


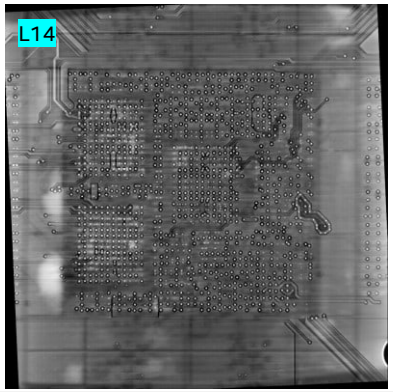


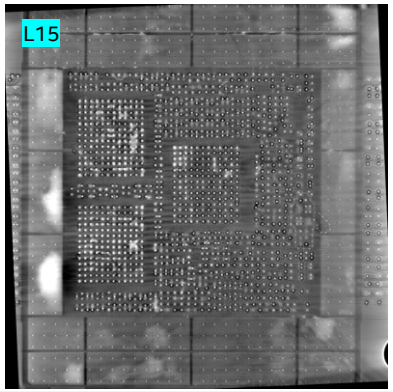


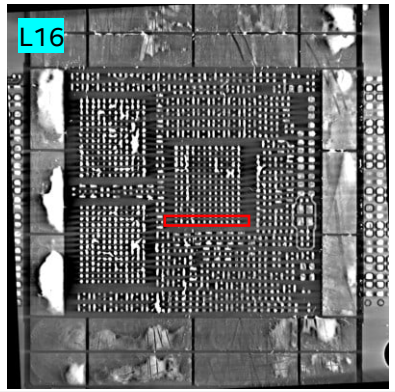








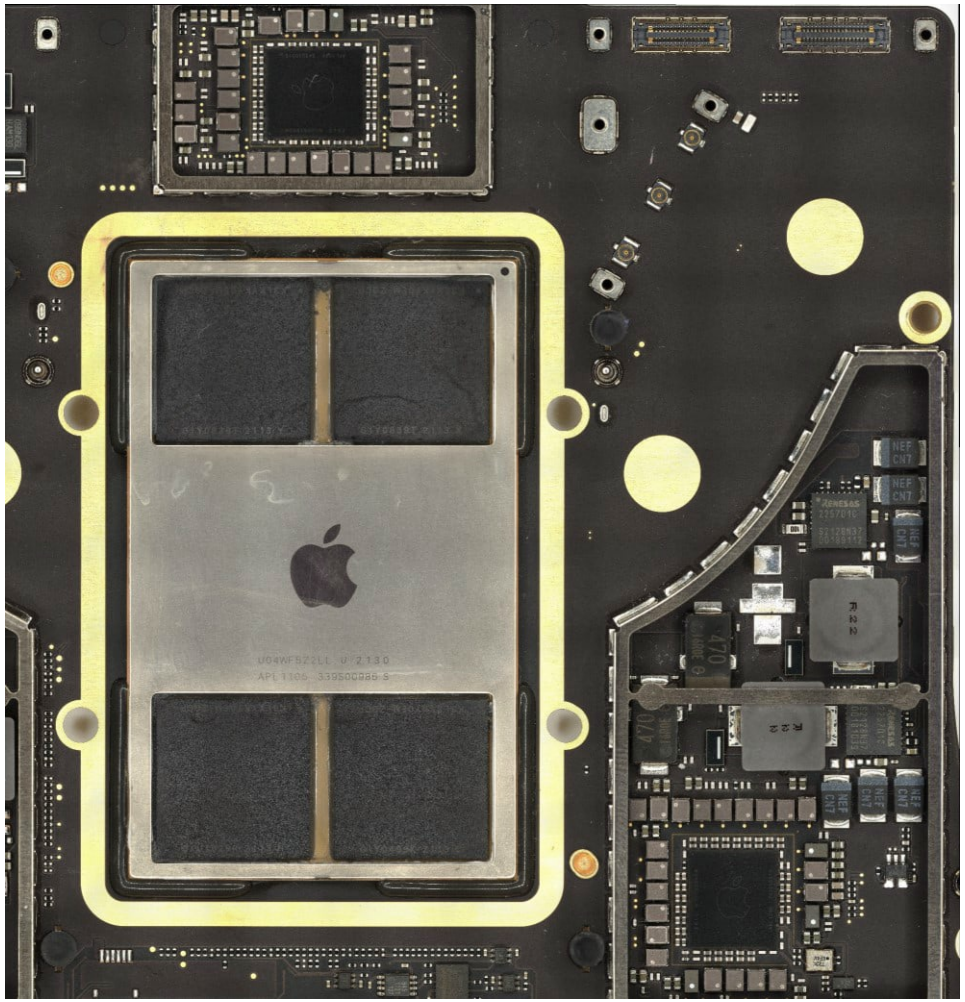




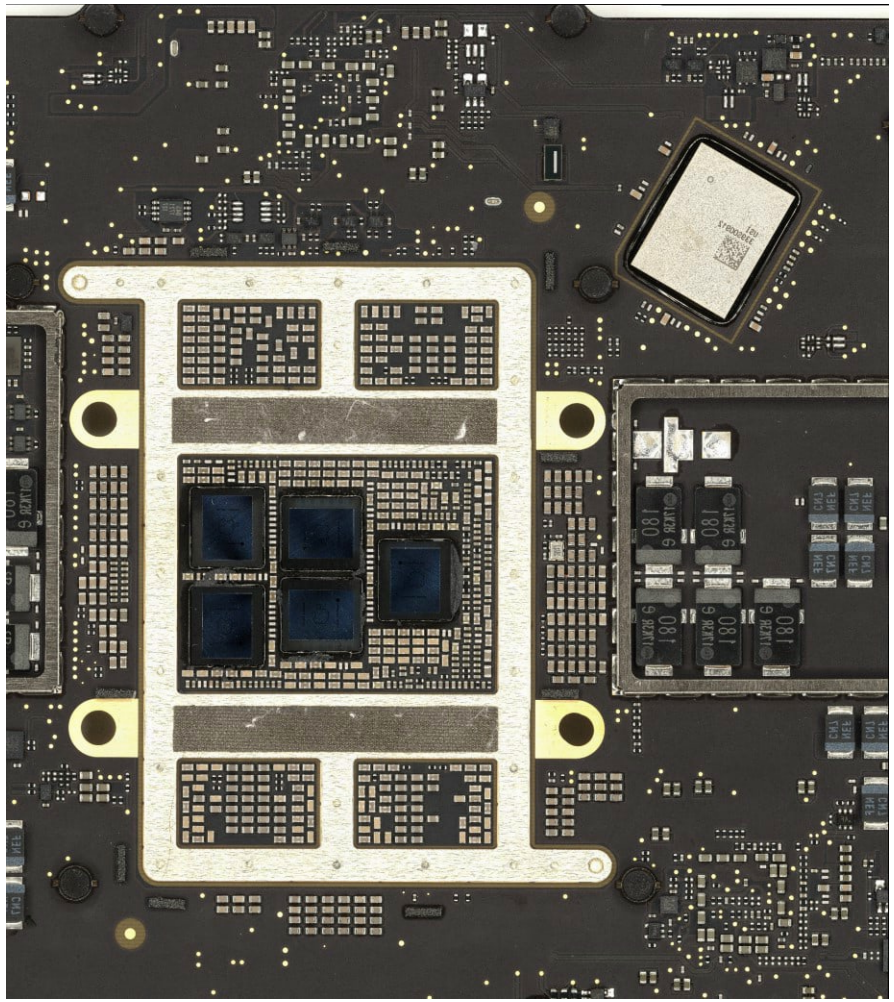
Contact ATTD C/A for access to the full high-resolution images.

Apple MacBook 16” – M1 Max Board

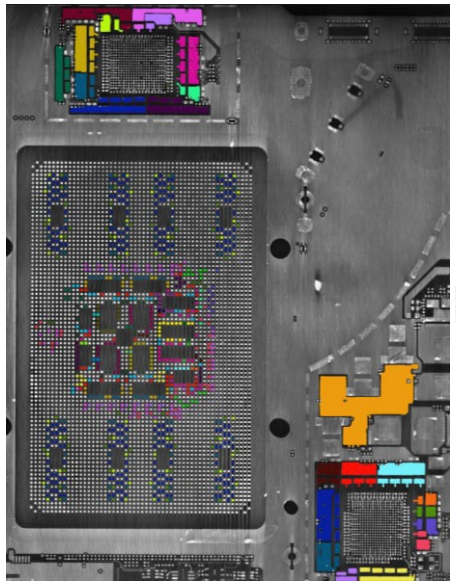
Top



Bottom

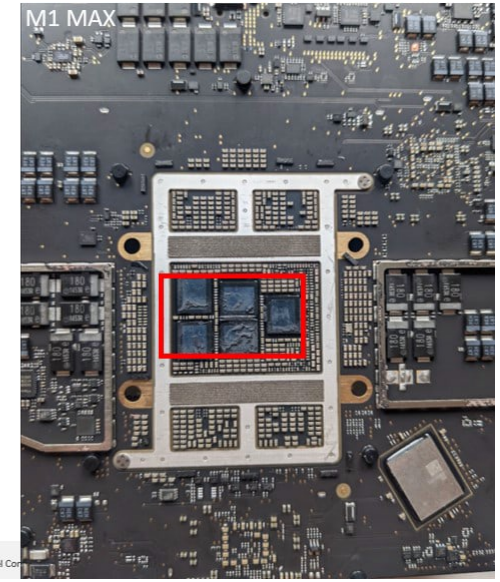


Power Delivery Analysis



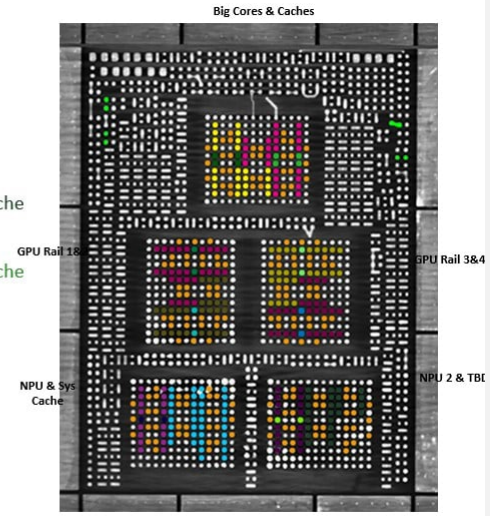
Back side
M1 Max

- New on the M1 Pro and Max are APL 1020 Integrated VRs on the backside.
- These are power from the 1.8V power stage on the top side.
- They used to power compute rails (Big Core, GPU, L1 L2 Cache)
- Maximum input power observed on the Max is 102W for a CPU+GPU workload combo



Backside VRs Power Rails
M1 Max

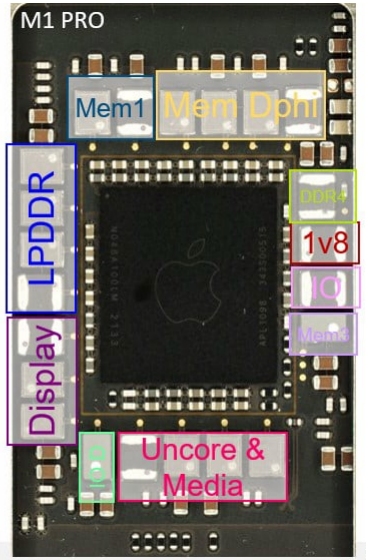
- GPU Rail 1
  - GPU 1 Secondary
- GPU Rail 2
  - GPU 2 Secondary
- GPU Rail 3
  - GPU 3 Secondary
- GPU Rail 4
  - GPU 4 Secondary
- TBD???
- Big Core Cluster 1
  - Big Core Cluster 1 Cache
- Big Core Cluster 2
  - Big Core Cluster 2 Cache
- NPU 1
  - NPU 1 Registers
- NPU 2
  - NPU 2 Registers
- System Cache



North PMIC Rails
M1 Pro

- 3.8V input power
- 10 rails with 22 Inductors
- All multiple phase rails are asymmetrical and have 2 modes single phase or full phase

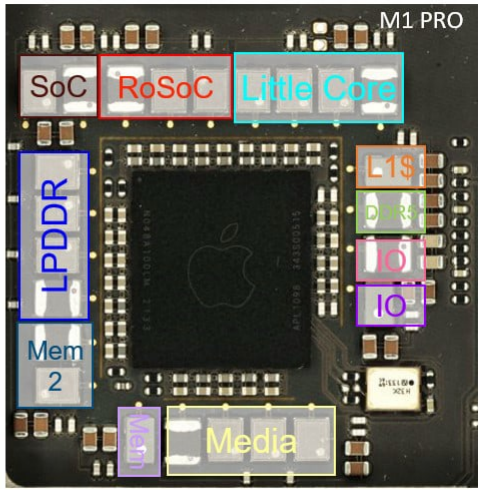
	Rail	Phases	Idle Voltage	Max Voltage	Typical Power [W]
SoC	Memory_d.Phy	4	0.64	0.88	1.6
SOC+LPDDR	LPDDR_IO_0.58V_Right	2	0.58	0.58	0.12
SoC	Display_2_Max_Only				
LPDDR	LPDDR_VDD2_1.05V_Right	4	1.05	1.05	0.85
SoC	Display_1	3	0.67	0.7	0.13
SoC	IO_TBT_xxxx	1	0.86	0.86	0.1
SoC	Uncore_Media_Tbt_Ctrl	4	0.64	0.7	0.15
SoC	Memory_A.Phy_R_VDDQ.TX	1	1.12	1.13	0.23
SoC	IO_PCIE_LPDDR_MC_xxx	1	1.2	1.2	0.2
Platform	Platform_HDMI_Bridge	1	1.8	1.8	0.8
LPDDR	LPDDR_d.IO_0.9V_R	1	0.9	0.9	0.01



South Pmic Rails
M1 Pro

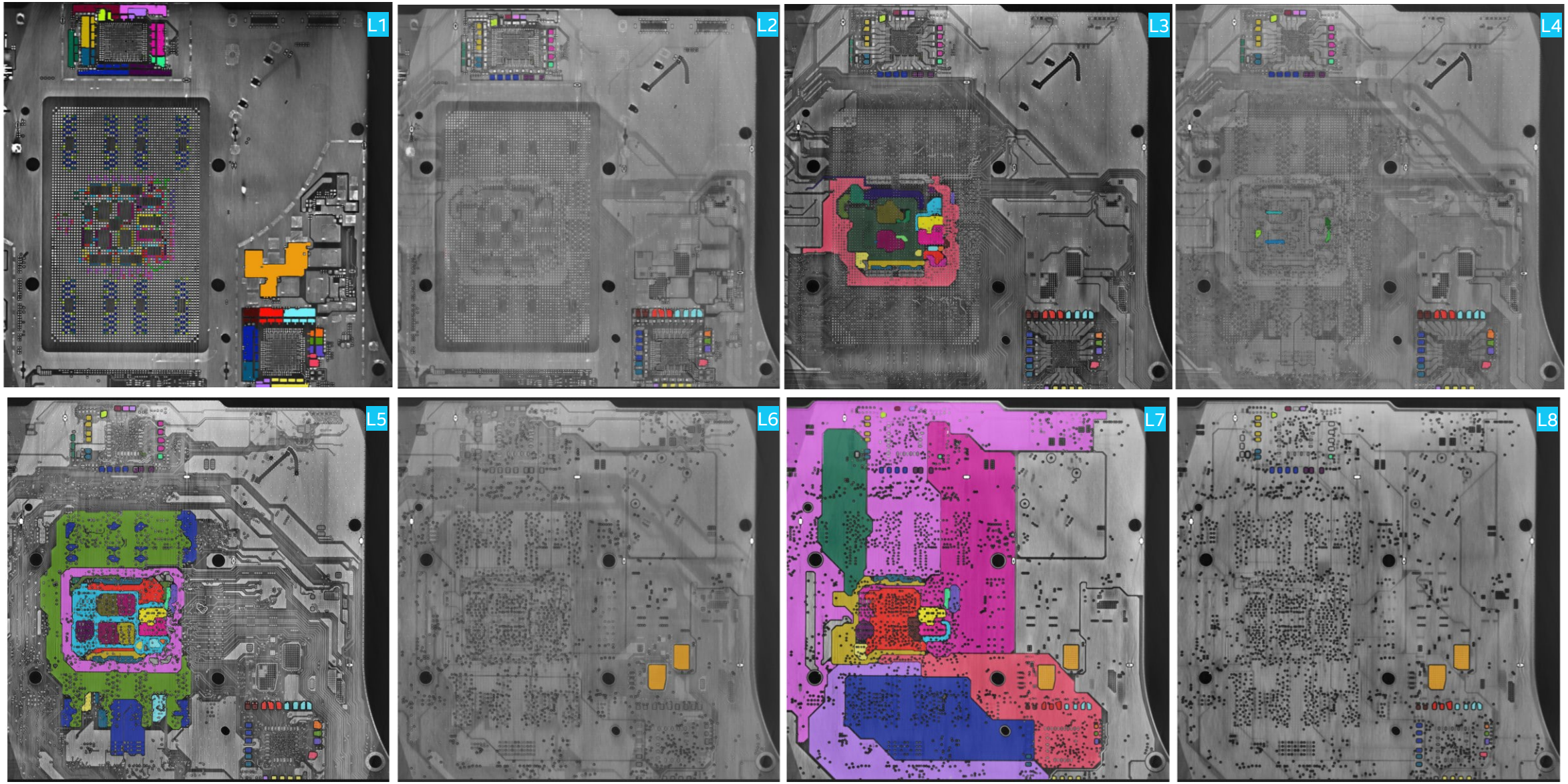
- 3.8V input power
- 11 rails with 23 Inductors
- All multiple phase rails are asymmetrical and have 2 modes single phase or full phase

	Rail	Phases	Idle Voltage	Max Voltage	Typical Power [W]
SoC	Little Core	4	0.58	0.83	0.58
SoC	RoSoC_IP_0.82V	2	0.82	0.82	0.16
SoC	RoSoC_Unknown	3	0.8	0.92	0.06
LPDDR	LPDDR_VDD2_1.05V_Left	4	1.05	1.05	0.87
SOC+LPDDR	LPDDR_IO_0.58V_Left	1	0.58	0.58	0.13
SoC	Memory_A.Phy_Left	4	1.12	1.13	0.23
SoC	Media Video Encoder	1	0	0.58	0.04
SoC	IO_PCIE_EDP_DP_Fuse_Ctrl	1	0.81	0.81	0.1
SoC+Platform	IO_TBT_xxx	1	1.2	1.2	0.2
LPDDR	LPDDR_VDD1_1.8V	1	1.8	1.81	0.46
SoC	Little_Cache	1	0.77	0.93	0.08



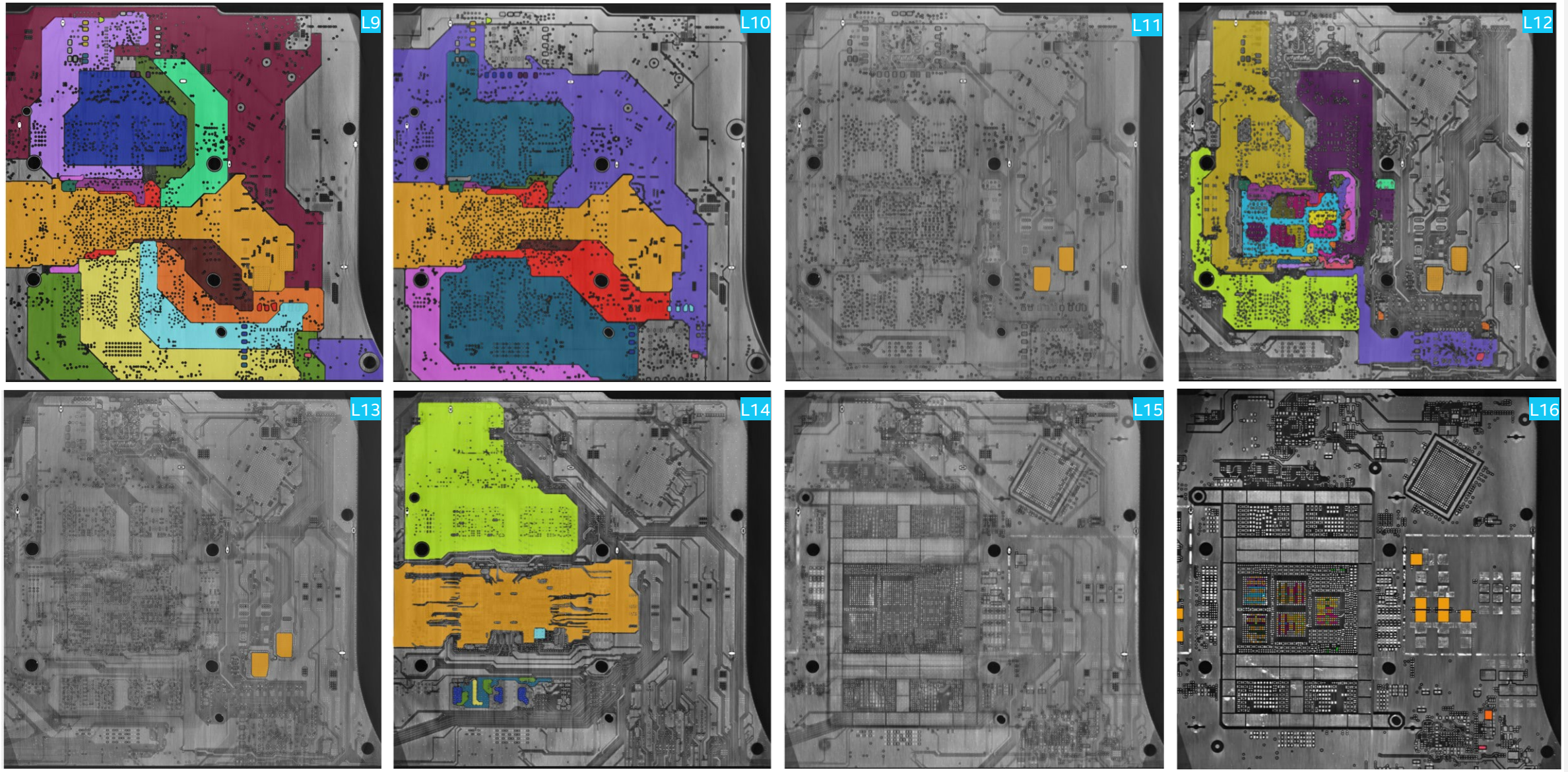
Ack: Vlad Nica, Suzanne Huang, John Powell, Le Nhung, Mike Duong, Will Berger, Mike Goldsmith

Apple MacBook 16” – M1 Max Board - 3D X-Ray



Contact ATTD C/A for access to the full high-resolution images.

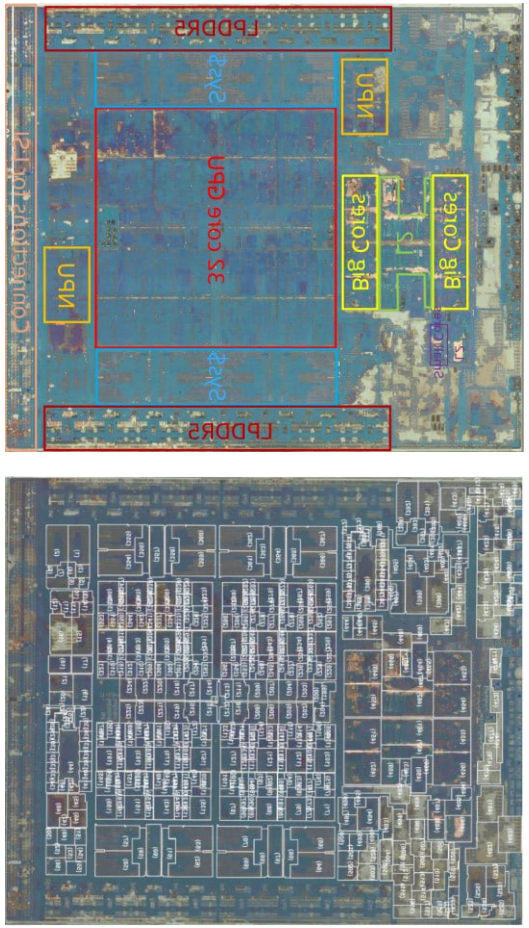
Apple MacBook 16” – M1 Max Board - 3D X-Ray



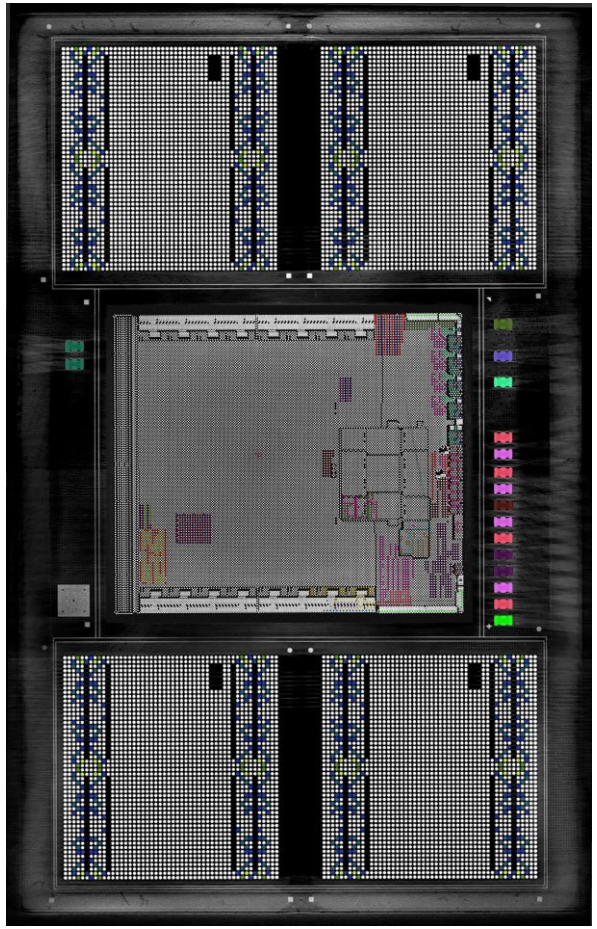
Apple M1 Max SoC Substrate - 3D X-Ray

Ack: Silicon CA team

Die Floor Plan



Layer 1



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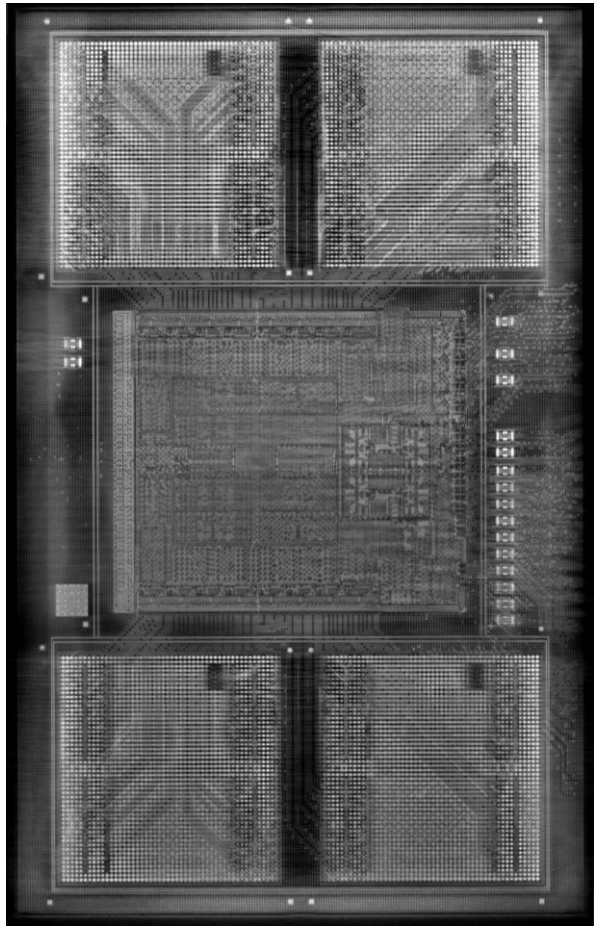
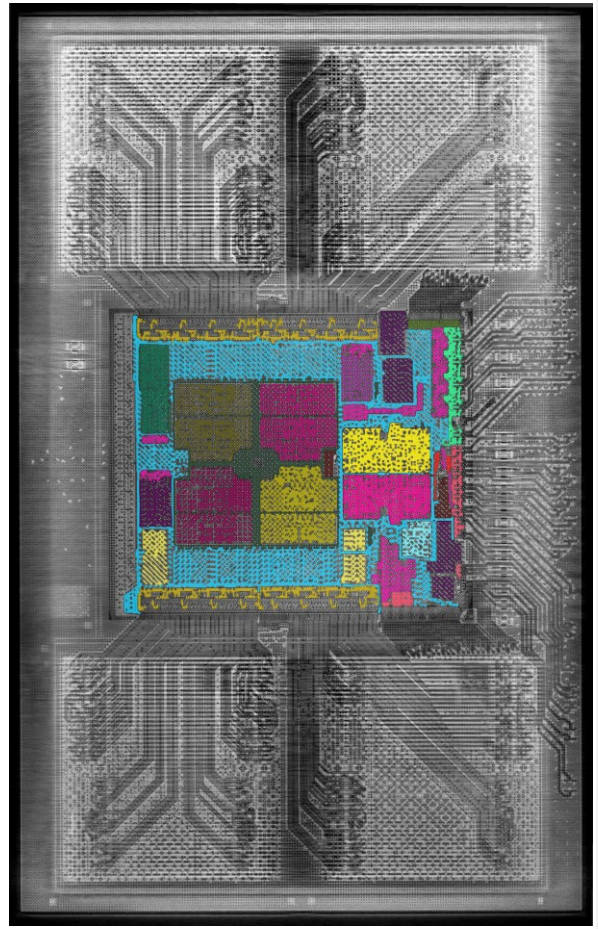


Layer 3

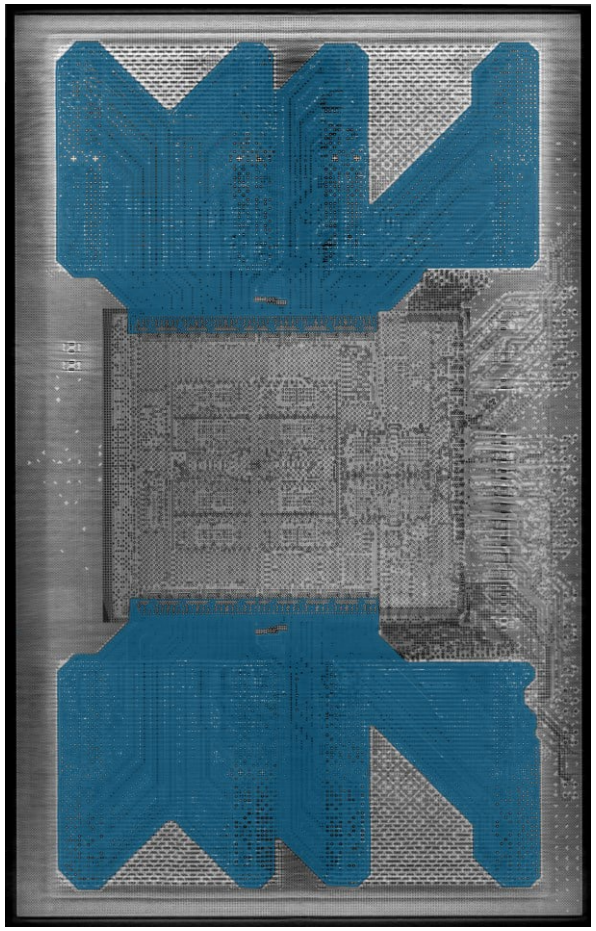


- 11-layers Coreless substrate.
- Layer 1 is used only for bump pads, fiducials, epoxy dams and 2D ID laser mark pad.
- DDR and high speed I/O routing on layers 3, 5 and 7; layer 9 carries the rest of the routing signals.

Contact ATTD C/A for access to the full high-resolution images.

Apple M1 Max SoC Substrate - 3D X-Ray

Layer 4



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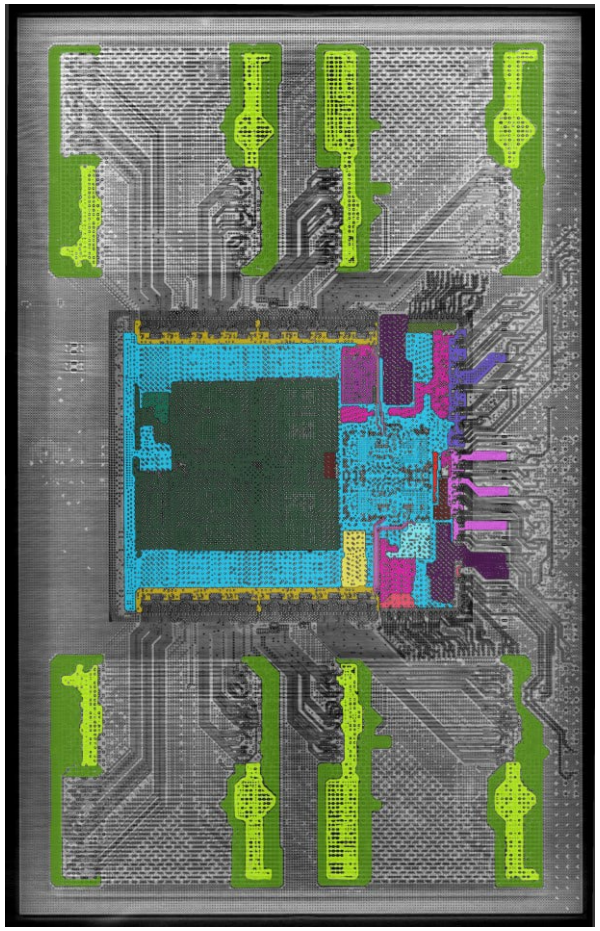

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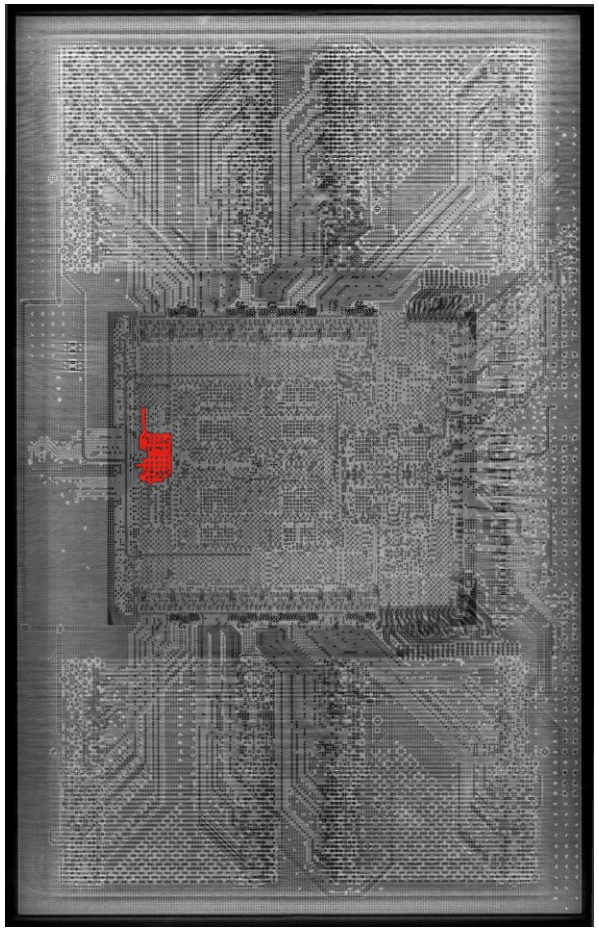
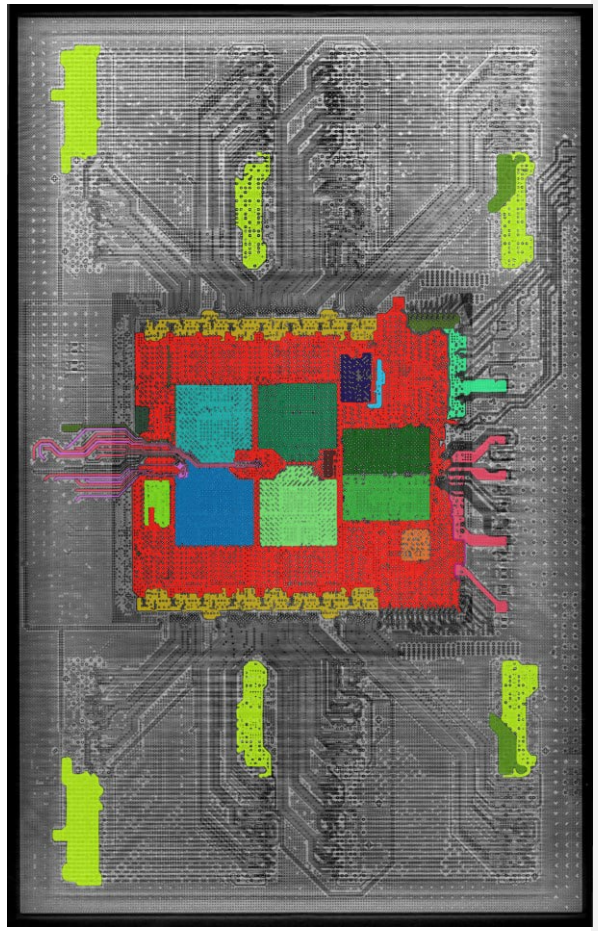


Layer 7



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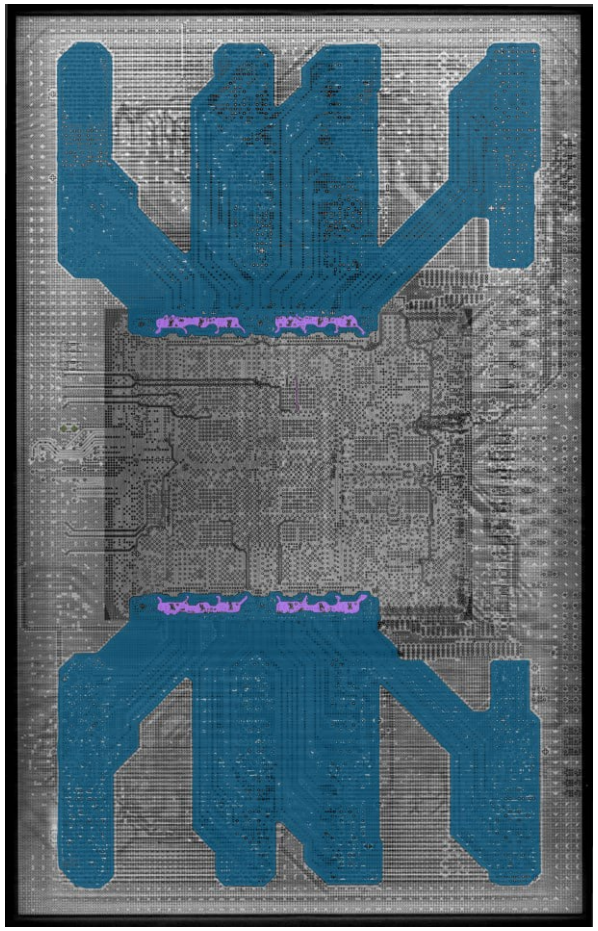
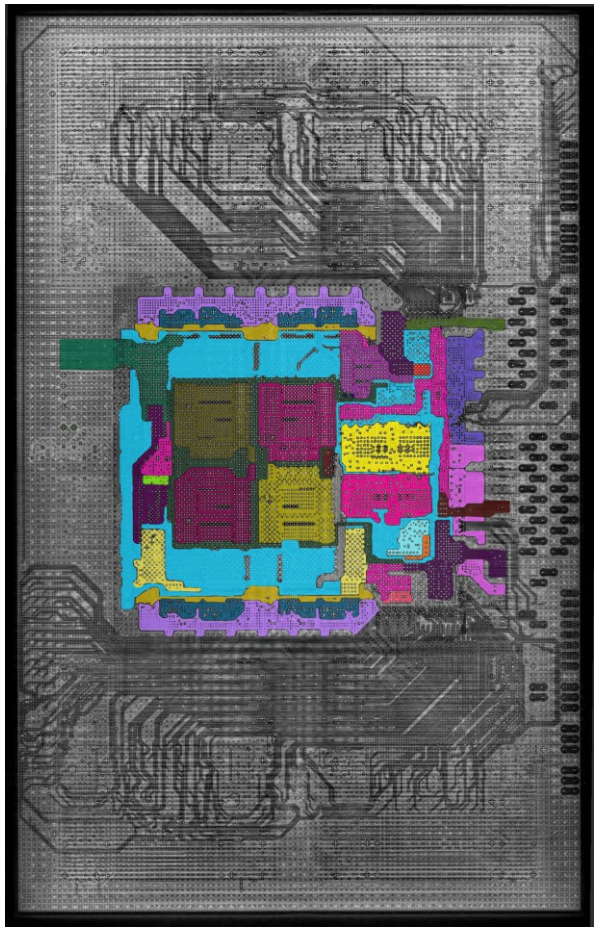
Apple M1 Max SoC Substrate - 3D X-Ray

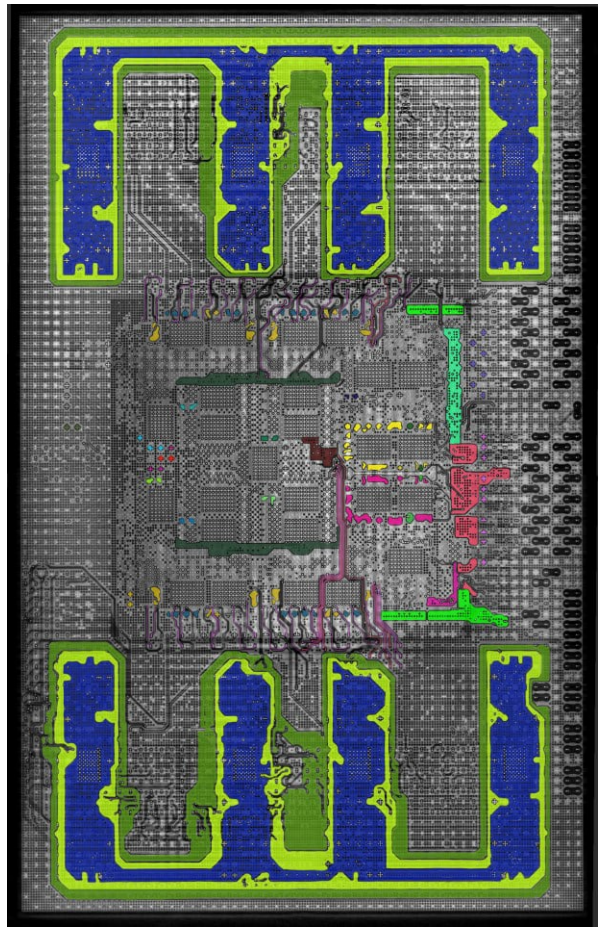
Layer 8



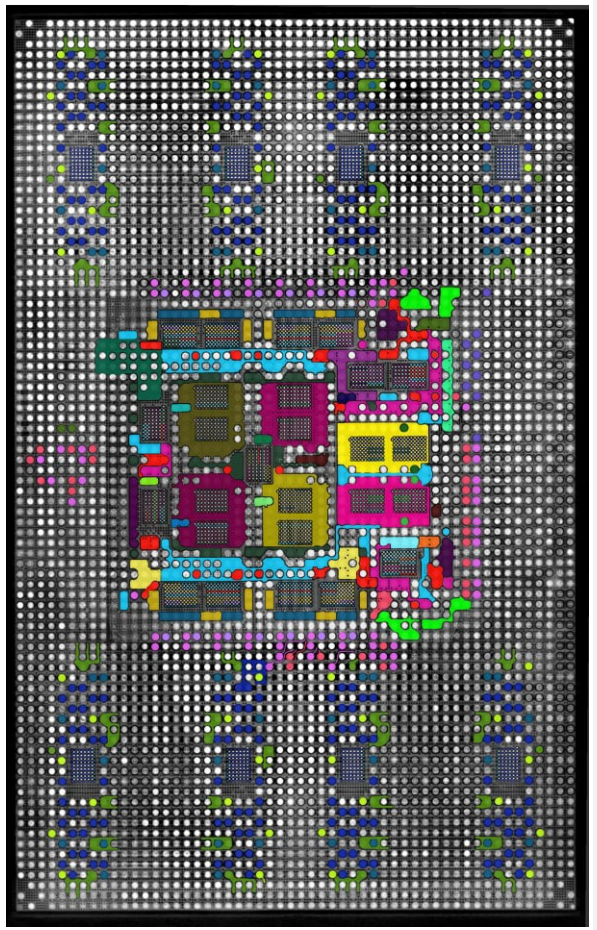
Layer 9



Layer 10

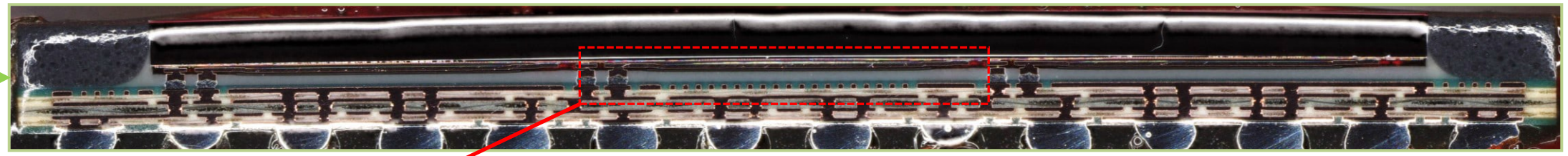


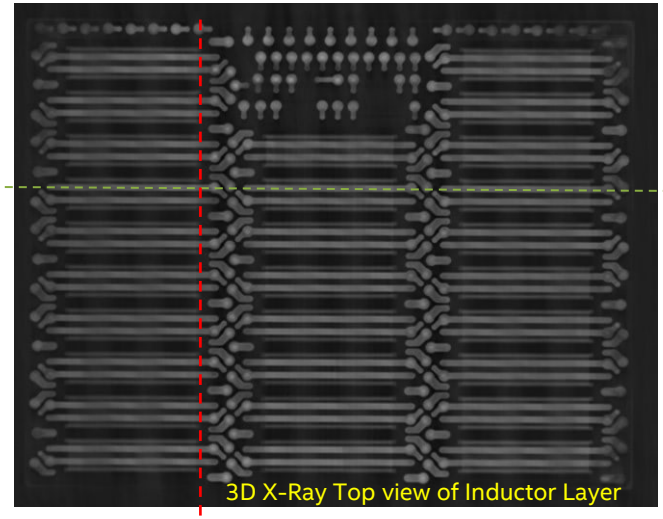
Layer 11

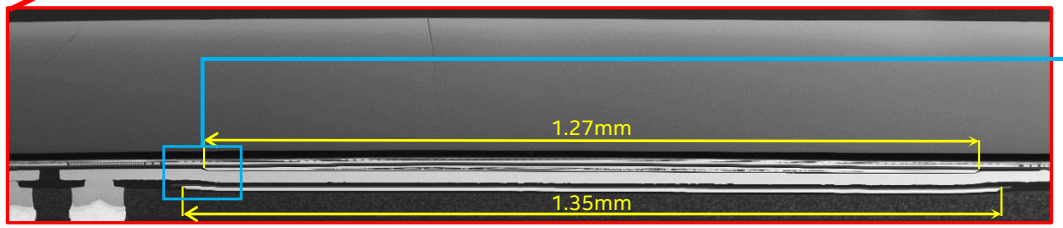


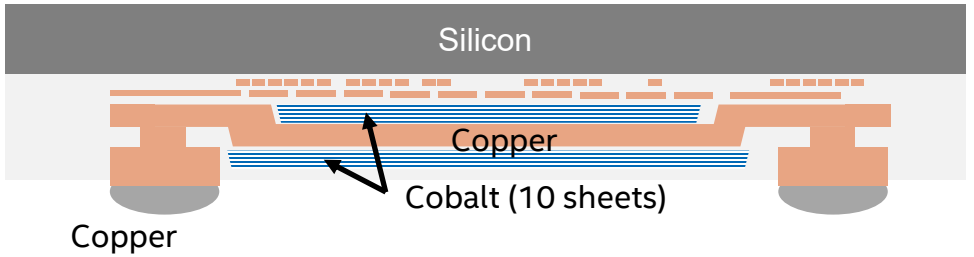
- 11-layers Coreless substrate.
- Layer 1 is used only for bump pads, fiducials, epoxy dams and 2D ID laser mark pad.
- DDR and high speed I/O routing on layers 3, 5 and 7; layer 9 have the rest of the routing signals.

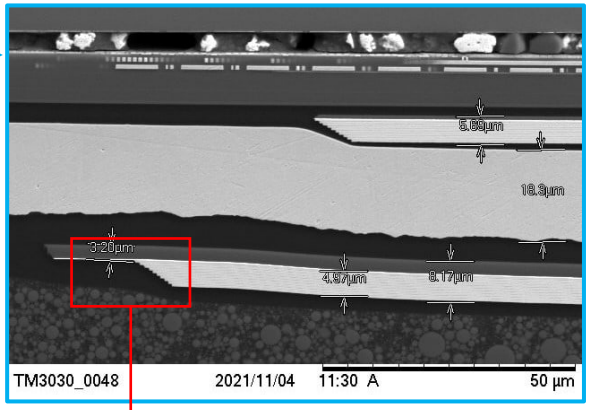
CMOS Voltage Regulators with Integrated Inductor

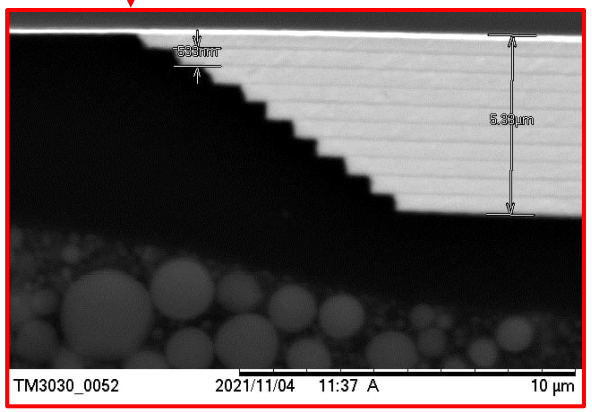


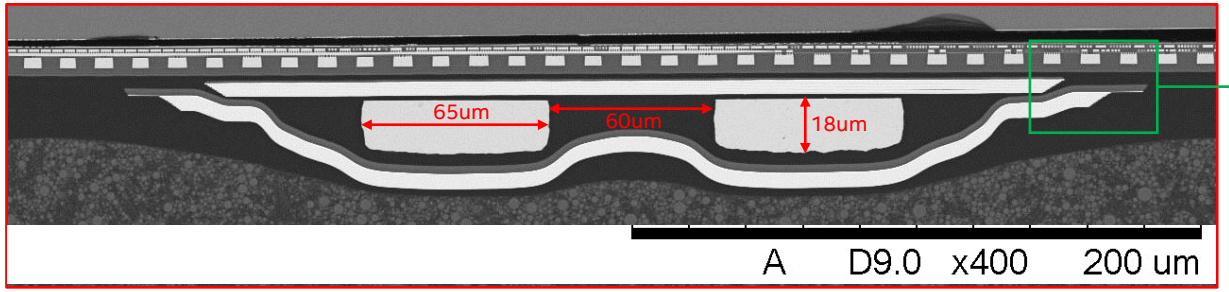


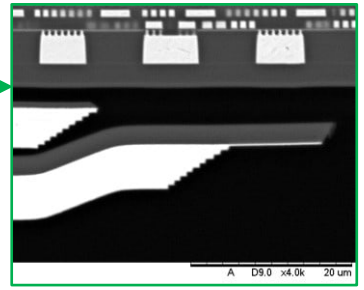






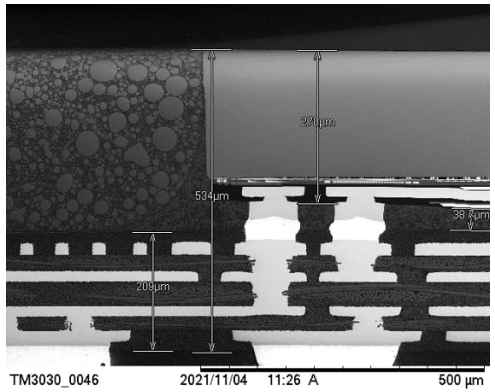


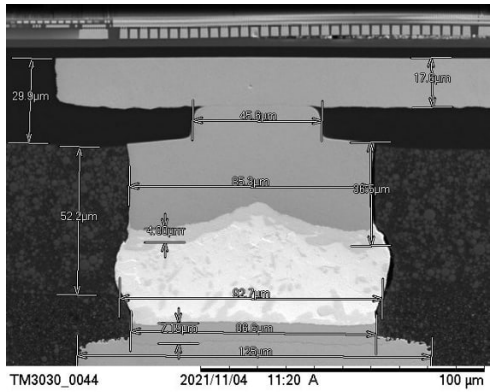


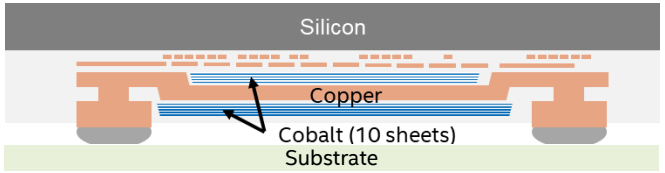


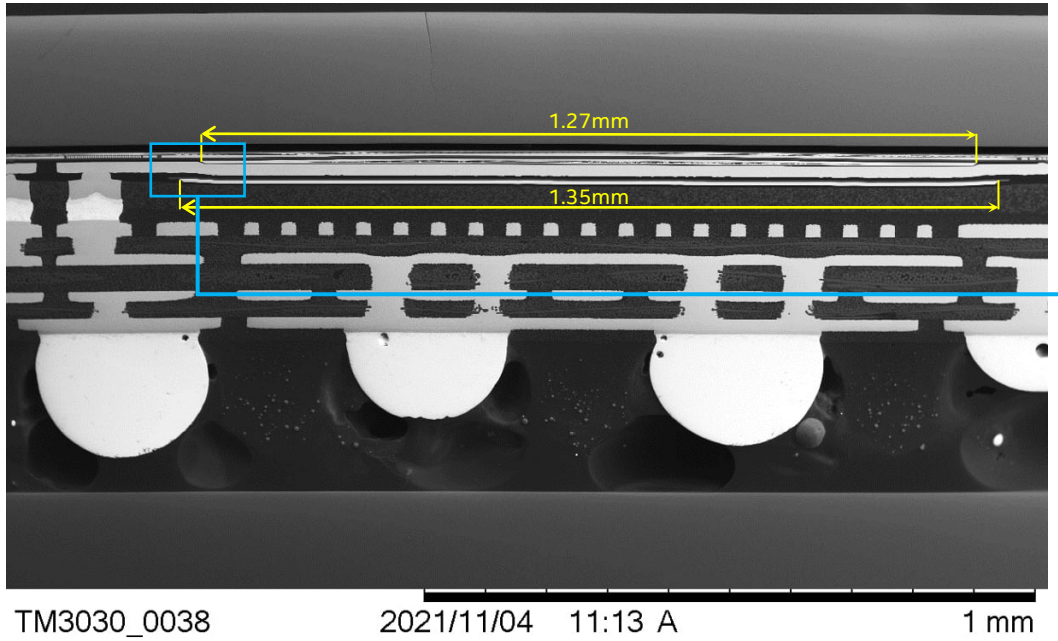
Voltage regulators incorporate a series of 28 inductor pairs formed by sputtering 10 0.5um thick Cobalt-rich (likely CZT) layers separated by 30nm dielectric layers. The stair-step edge is likely a result of wet etch. A dielectric of undetermined composition effectively provides an air gap.

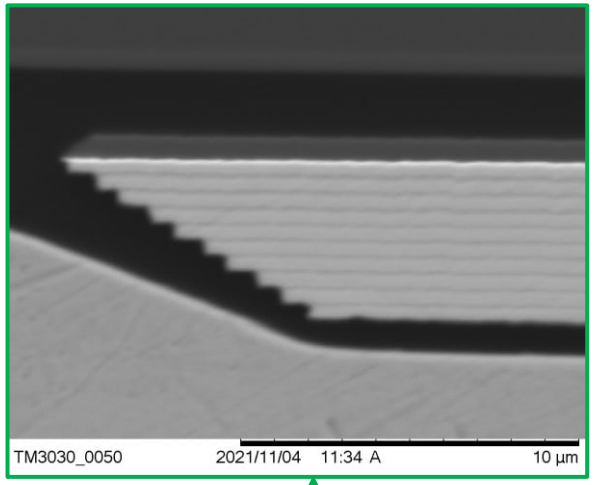
Voltage Regulator Package – X-Section

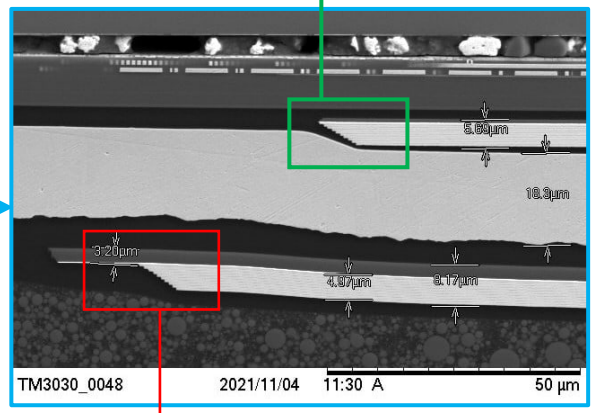


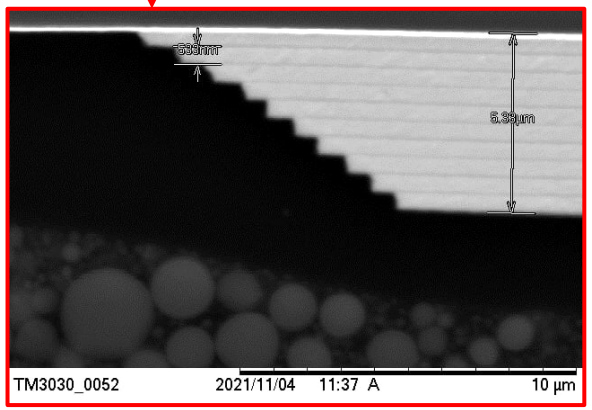








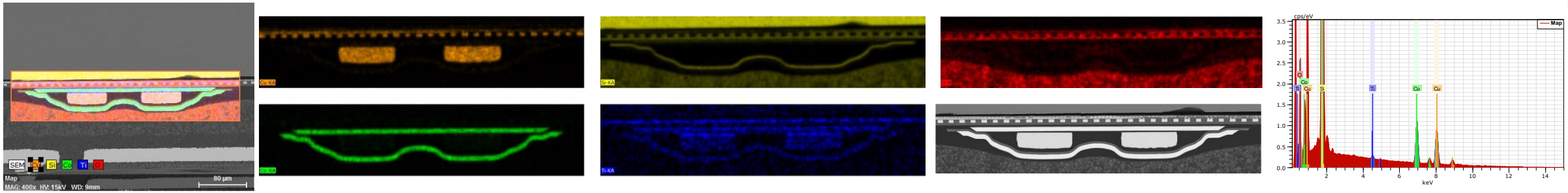




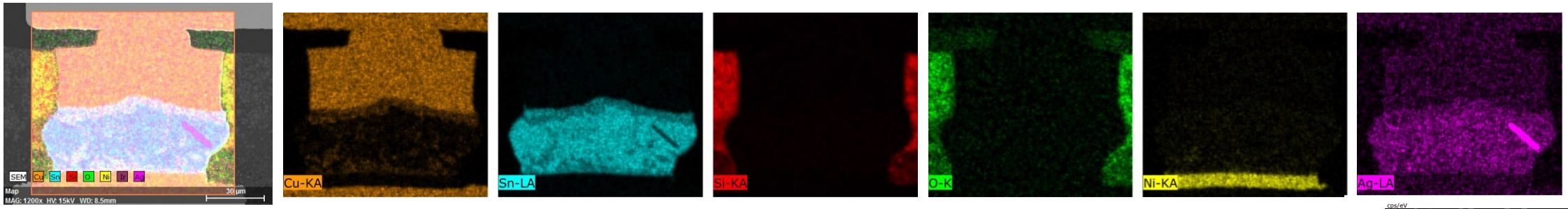
- Total package height is ~ 534um (without BGA's), coreless substrate height ~210um.
- Die thickness is ~ 270um, bulk silicon = ~220um.
- FLI: 140um min bump pitch. SLI: 0.485mm BGA pitch
- The right images show the details of the ferromagnetic material (primarily composed of Cobalt, we suspect it is CZT) surrounding the Cu strips *(EDX analysis on next slide).*
- The ferromagnetic material is built with a stack of 10 layers of ~ 500nm thick Co-rich material seperated by 30nm dielectric layers.

Voltage Regulator Package – EDX analysis

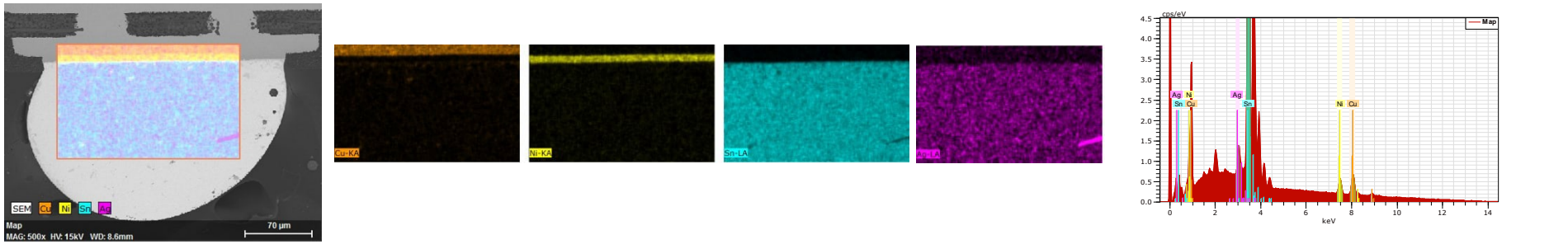
Inductor



FLI/Bump



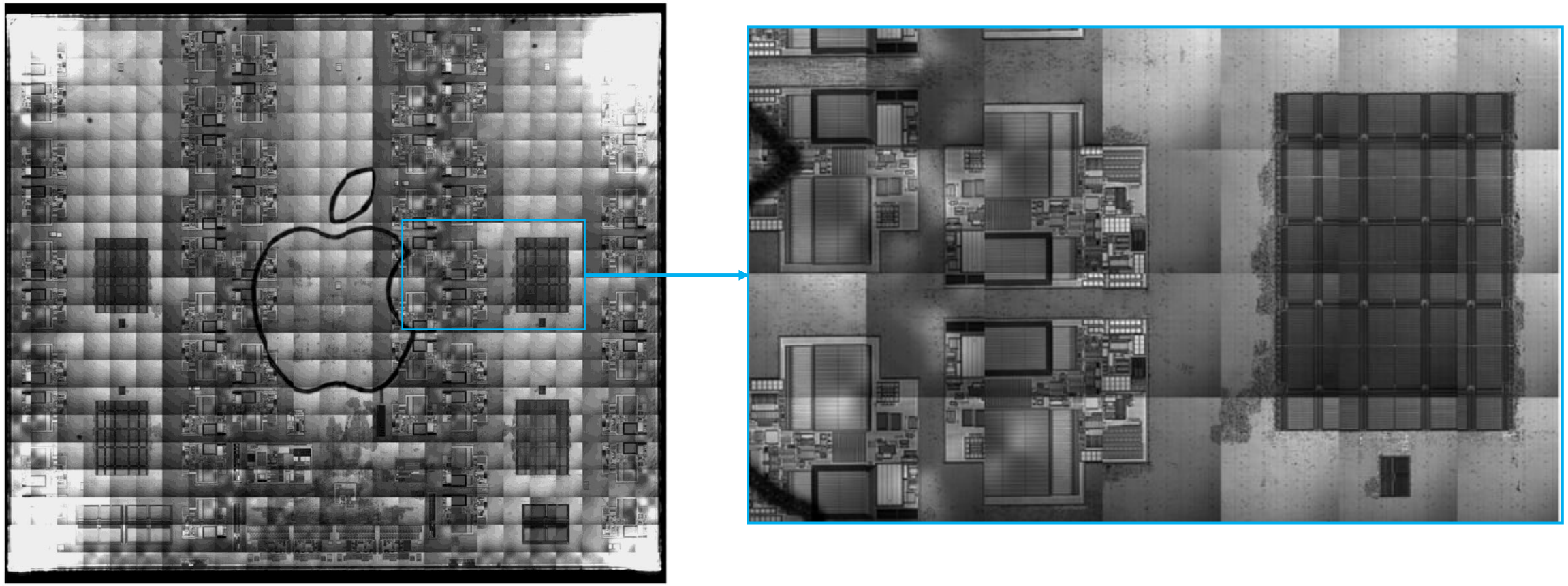
SLI/Ball



- The top die layers is a group of Cu strips surrounded by ferromagnetic material (primarily Co). Ti layer purpose is still TDB.
- Die bumps are made of Cu.
- Substrate bumps and BGA balls are SAC solder. Substrate FLI and SLI pads are nickel plated copper.

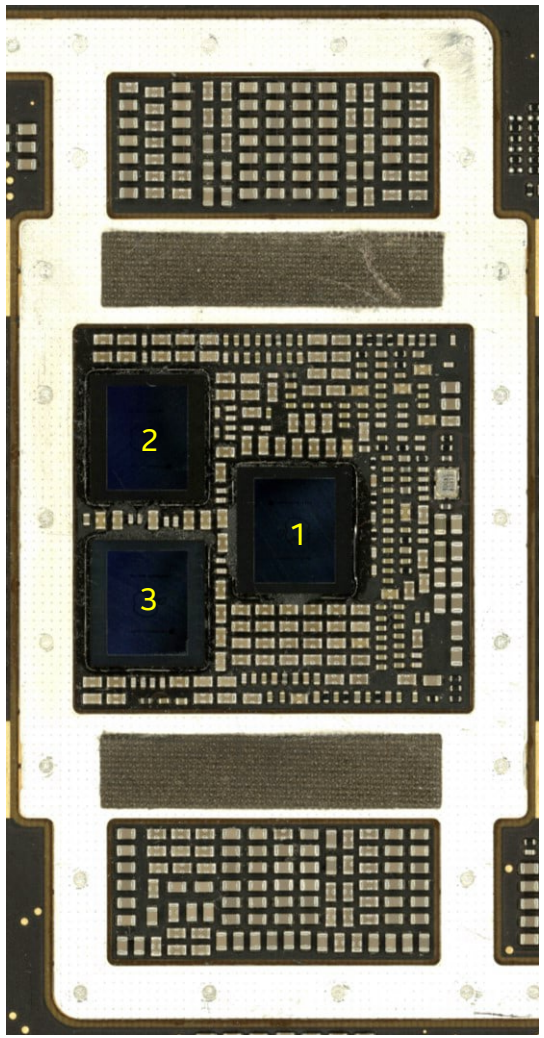
VR Die IRLC Image (343S00510)

Stitched IRLC images taken at 20x (FOV size = 250um)

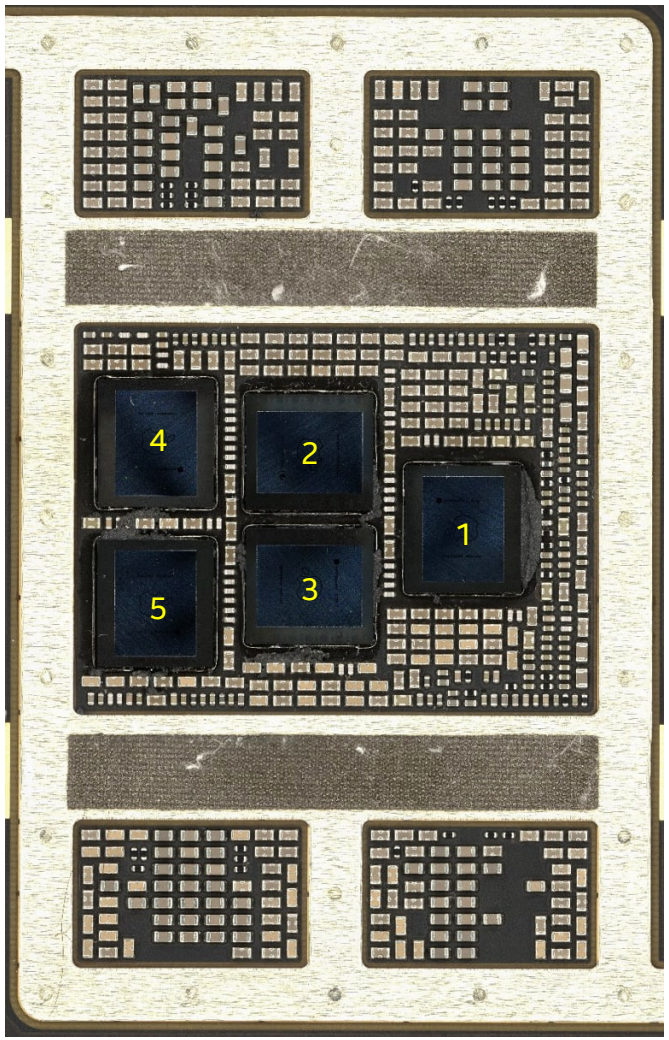


Ack: Jacob Woolsey, FA R&D Engineer – CH6

Package Voltage Regulator Laser Marks



System/SoC	System	Laser Marks				
Apple 14' MacBook Pro M1 Pro	System 1	1	APL1028	343S00**510**	P0AKK700LM	2130
		2	APL1028	343S00**506**	P0AKK2L2LL	2131
		3	APL1028	343S00**508**	P0AKK6LC11	2131
	System 2	1	APL1028	343S00**510**	P0AKH8L4LN	2129
		2	APL1028	343S00**506**	P0A2K1L011	2131
		3	APL1028	343S00**508**	POAKK2L2LL	2131
Apple 16' MacBook Pro M1 Max	System 1	1	APL1028	343S00**510**	P0AHR4L811	2132
		2	APL1028	343S00**506**	P0AKH7Y411	2129
		3	APL1028	343S00**506**	P0AKH7Y411	2129
		4	APL1028	343S00**509**	P0AHS4Y111	2132
		5	APL1028	343S00**507**	P0AKM3LHLL	2134
	System 2	1	APL1028	343S00**510**	POAHR4Y211	2131
		2	APL1028	343S00**506**	POAKR70011	2134
		3	APL1028	343S00**506**	POAKR70011	2134
		4	APL1028	343S00**509**	POAKK1L3LL	2132
		5	APL1028	343S00**507**	POAHS40011	2132
	System 3	1	APL1028	343S00**510**	POAHR4Y211	2131
		2	APL1028	343S00**506**	POAKR70011	2134
		3	APL1028	343S00**506**	POAKR70011	2134
		4	APL1028	343S00**509**	POAKK1L3LL	2132
		5	APL1028	343S00**507**	POAHS40011	2132

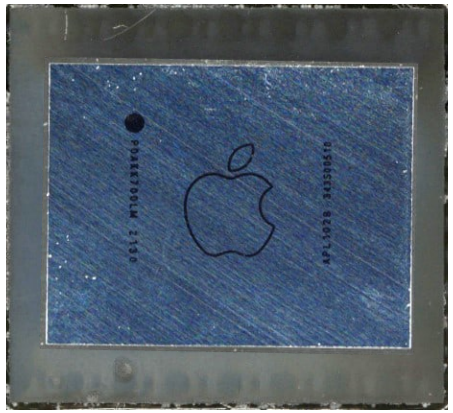


**Ack: TMG Si C/A team*

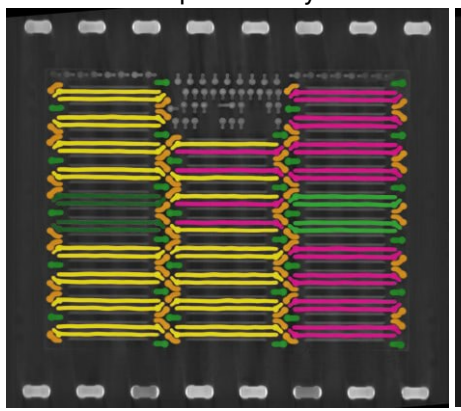
Different laser mark numbers per location suggest that there are 5 different types of PVR.

Voltage Regulators (343S00510) - *PCB Bottom Side Components*

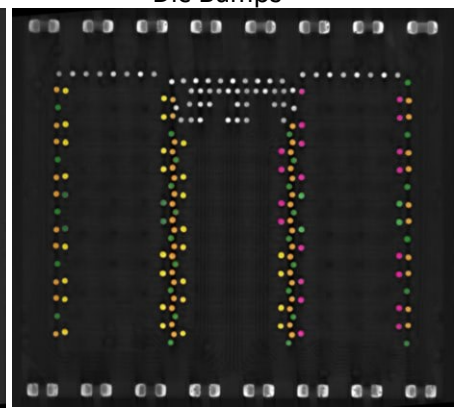
Top View



Die Top Metal Layer



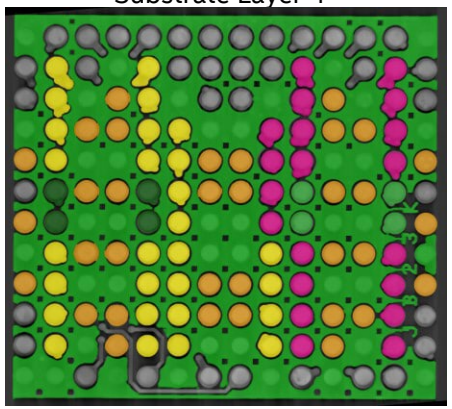
Die Bumps



Component size: 6.8x7.4mm.
Die size: 4.6x5.9mm.
BGA Qty: 168 balls at 0.485mm bp
Components Qty: Pro-3, Max-5

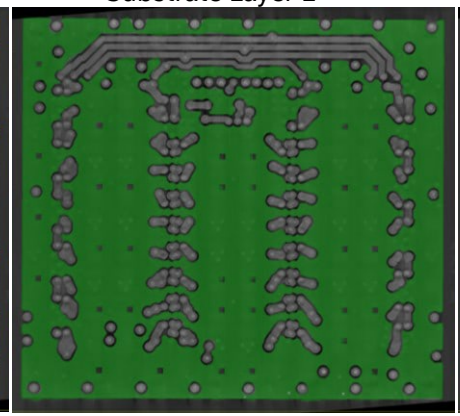
- Current flows in opposite direction in each inductor pair to cancel the magnetic flux.
- Orange= input
- Yellow/pink are 2 output supply domains.
- Five versions exist based on part numbers.

Substrate Layer 4

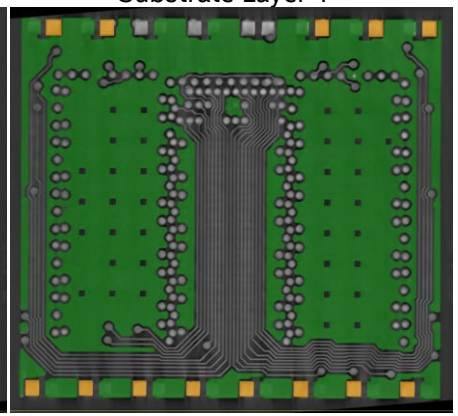


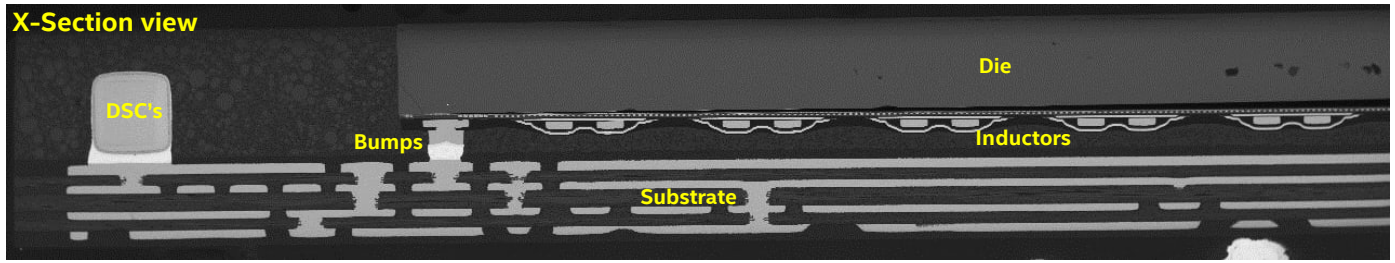
Substrate Layer 3

Substrate Layer 2



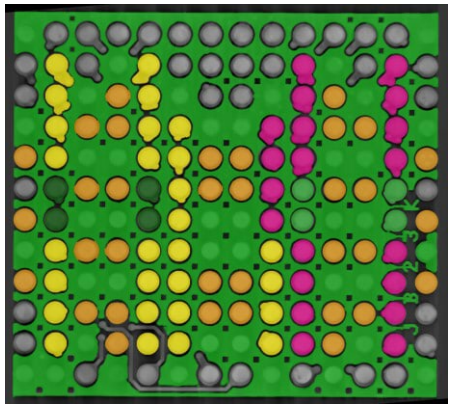
Substrate Layer 1



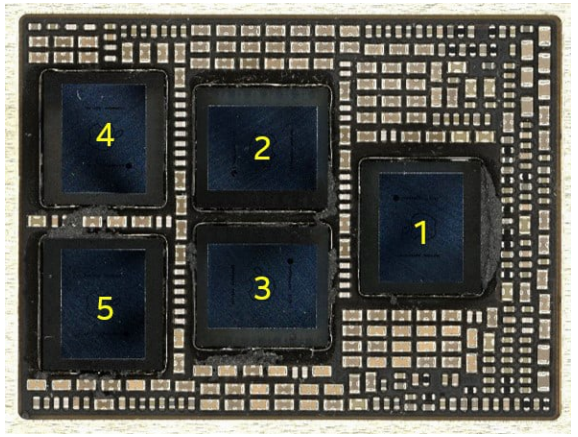


Voltage Regulators - *PCB Bottom Side Components*

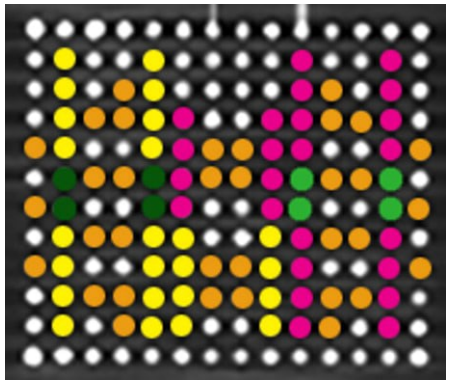
Package Level



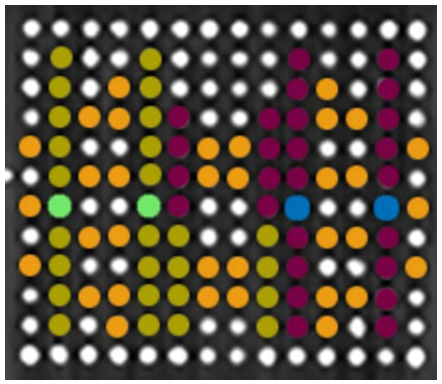
System/SoC	System	Laser Marks				
Apple 16' MacBook Pro M1 Max	System 1	1	APL1028	343S00**510**	P0AHR4L811	2132
		2	APL1028	343S00**506**	P0AKH7Y411	2129
		3	APL1028	343S00**506**	P0AKH7Y411	2129
		4	APL1028	343S00**509**	P0AHS4Y111	2132
		5	APL1028	343S00**507**	P0AKM3LHLL	2134



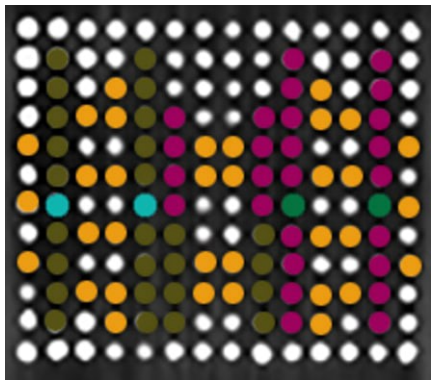
Board Level



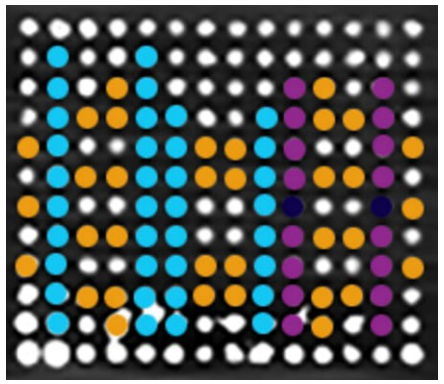
343S00**510**
Input pins: 34
Output pins: 56 total
24–24-4-4



343S00**506**
Input pins: 34
Output pins: 56 total
26–26-2-2



343S00**506**
Input pins: 34
Output pins: 56 total
26–26-2-2



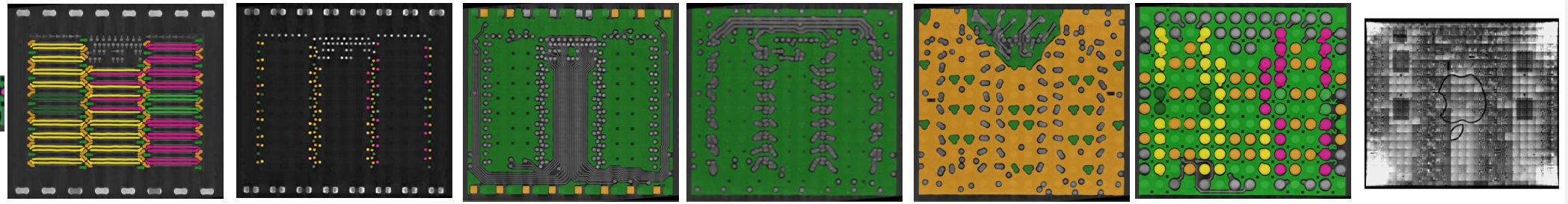
343S00**509**
Input pins: 34
Output pins: 54 total
36–16-2

343S00**507**
Input pins: 34
Output pins: 42 total
24–16-2

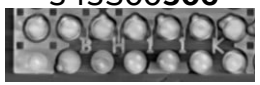
- The orange pins corresponds to power input, the other colored pins correspond to output domains, which are different for each component type, however no noticeable differences were found at VR package/die level (detailed images on next slide).

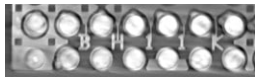
Voltage Regulators Comparison

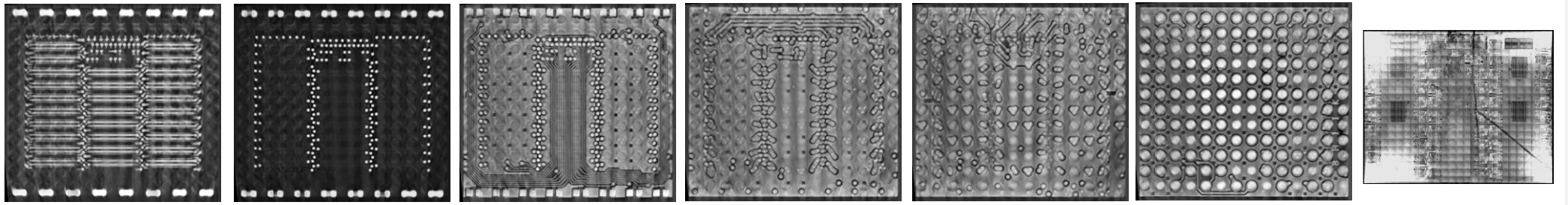
343S00**510**



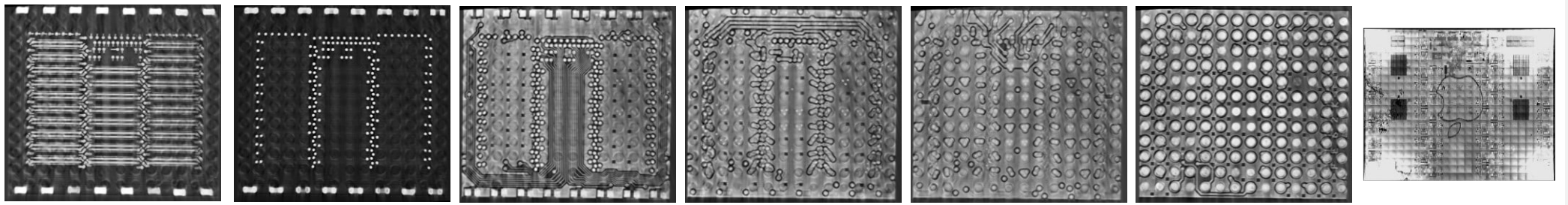
343S00**506**



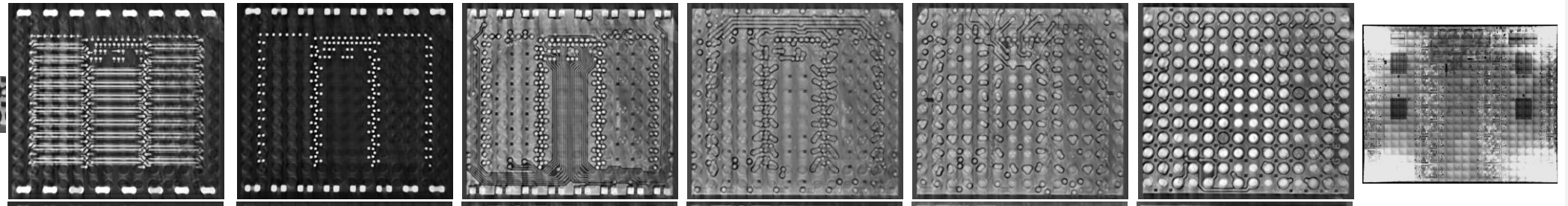




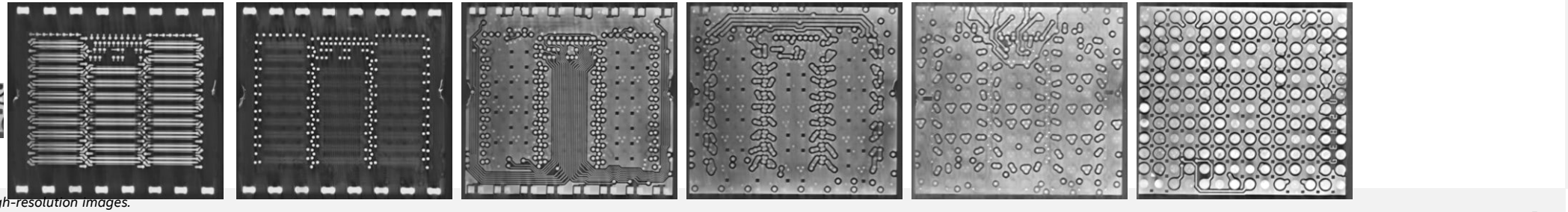
343S00**507**



343S00**509**



343S00**508**



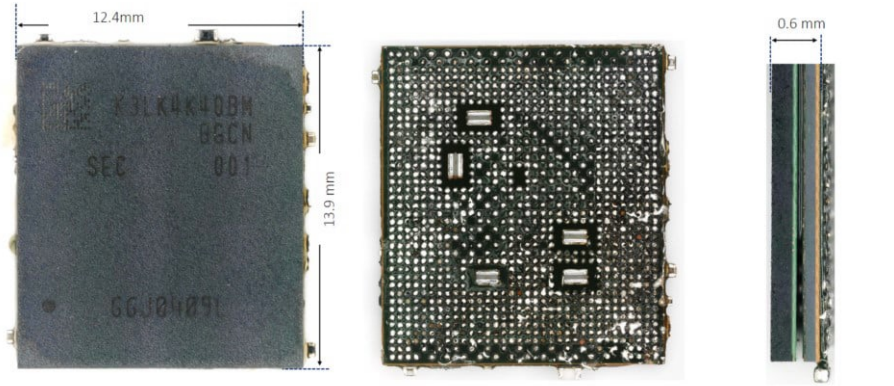
Contact ATTD C/A for access to the full high-resolution images.

Back-up

Samsung LPDDR5 1y Memory

Samsung LPDDR5 Package

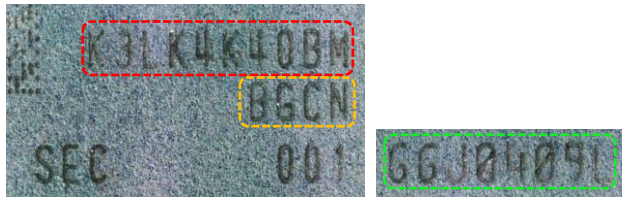
Package:	BGA- 496
Dimensions:	13.9 x 12.4 x 0.6 mm
Surface:	172mm²
Pitch :	0.4mm



Package Top View
©2020 by System Plus Consulting

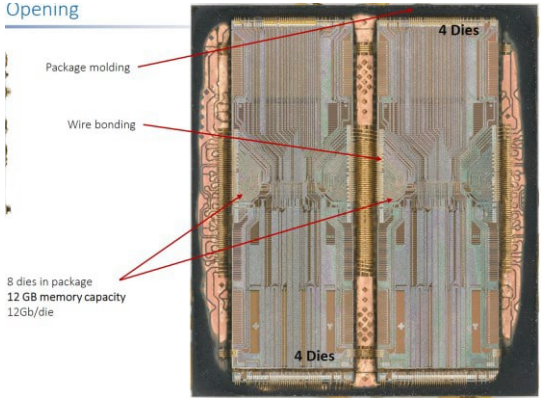
Package Bottom View
©2020 by System Plus Consulting

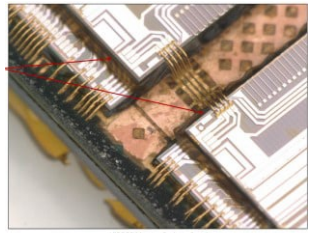
Package Side View
©2020 by System Plus Consulting



K3LK4K40BM – Component reference
BGCN
SEC - Component manufacturer (Samsung Electronics Corporation)
001
GGJ0409L - Package trace code

Opening

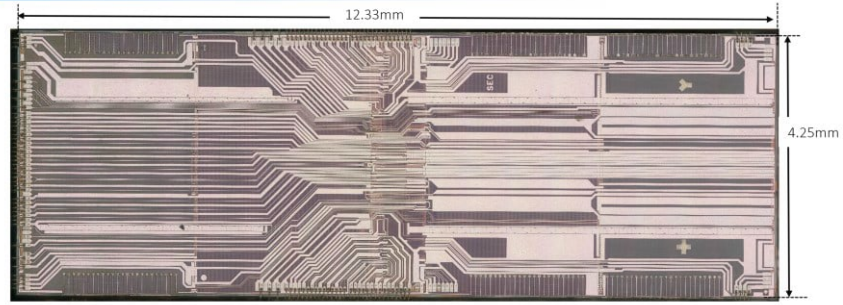




LPDDR5 Memory Package Opening
©2020 by System Plus Consulting

Analysis	Characteristics/Observations
Package thickness	0.6mm
Number of dies in package	8
Die area	52.1mm²
Die thickness	36µm
Density per die	12Gb/ Die
Die density/mm²	0.23Gb/mm²
DRAM capacitor height	0.9µm
Word line pitch	36nm
Process technology	10nm class
Capacitance aspect ratio	18:1
Metal layers	8M (1 W wordline + 1 W bite line + 1 W above bitline+ 3Cu+ 1Al+ 1Al pad)
CMOS transistor technology	45nm

Samsung LPDDR5 - Memory Die



Samsung LPDDR5 Memory Die
©2020 by System Plus Consulting

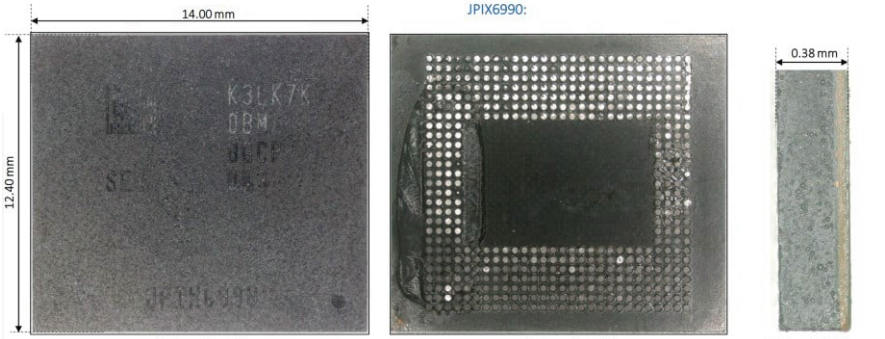
- Die Area: 52.1mm² (12.32 x 4.23mm)
- Nb of PGDW per 12-inch wafer: 1,204
- Pad number: ~ 159
  - Connected : 118
  - Test Pads : 20
  - Unused pads : 21

Source:
System Plus Consulting
Samsung 12GB Mobile LPDDR5 Memory
Samsung Galaxy S20 Ultra 5G

Samsung LPDDR5 1z Memory

Package Views & Dimensions

- Package: BGA 496 balls
- Dimensions: 14.00 x 12.40 x 0.38 mm
- Ball pitch: 0.4 mm
- Marking:
  - SEC: Samsung Semiconductor component manufacturer
  - K3LK7K70BM: Component Reference
  - BGCP:
  - 043:
  - JPIX6990:

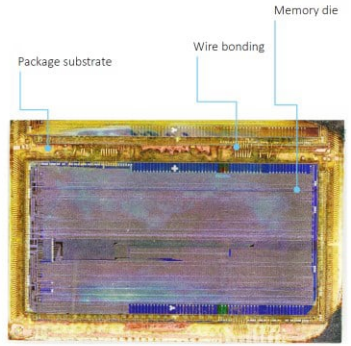


Package Front View
Package Back View
Package Side View
©2021 by System Plus Consulting

Summary of the Physical Analysis

Memory Package:
- Electronic components assembly
- DRAM memory capacity : 8GB
- Memory dies in package: 4 dies
- Electrical connections and support: balls on smartphone PCB

Memory Die:
- Die Area:
  - ✓ 60.48mm²
- Process:
  - ✓ CMOS 45nm 1P
  - ✓ Metal layers: 8 (4M (top) & 3M bottom)
- Die capacity:
  - ✓ 2GB/ 16 Gb
- Placement: wire bonding to substrate

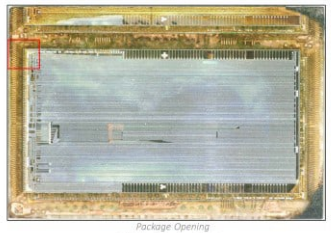


Memory Package Opening
©2021 by System Plus Consulting

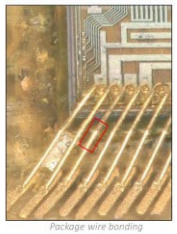
Memory Process Characteristics

- CMOS and metal layers front-end process:
  - Substrate: 300mm Silicon wafer
  - Process type: CMOS (Digital, Analog)
  - Metal layers: 8 total
  - Technology node: 45nm for the CMOS transistors
  - Technology node: 16nm for the bitline and wordline
  - Lithography steps: 46
- DRAM cell process:
  - Technology node: 10nm class/ 1z nm
  - Lithography steps: 9
- Total lithography steps: 55

Package Opening

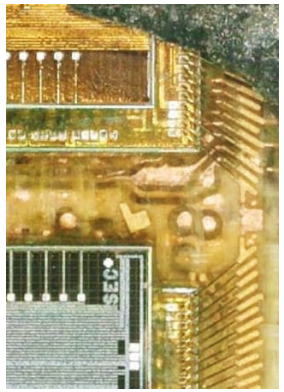


Package Opening
©2021 by System Plus Consulting



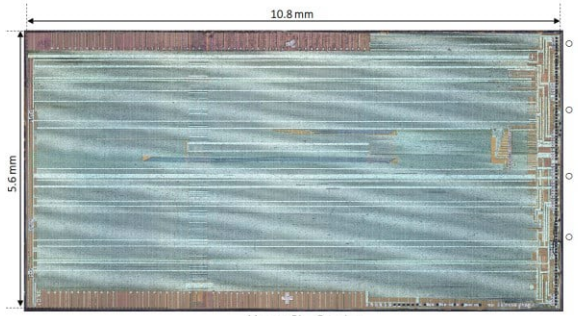
Package wire bonding
©2021 by System Plus Consulting

Package wire bonding
©2021 by System Plus Consulting



- Package opening reveals 4 DRAM dies.
- Package capacity: 8GB/64Gb per package
- Die capacity: 16Gb per die
- Wire bonding
  - Material: Gold wire
  - Wire number total: 472
  - Wire number per die: 118
  - Wire diameter: 19 µm
  - Wire average length: 0.4 mm

Die Overview & Dimensions



Memory Die - Overview
©2021 by System Plus Consulting

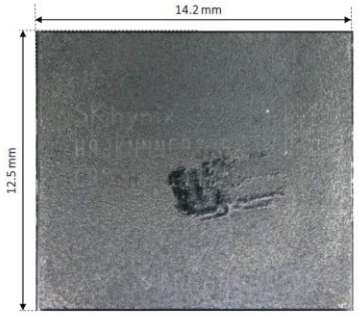
- Die area: 60.48 mm² (10.8 x 5.6 mm)
- Nb of PGDW per 12-inch wafer: 1,048
- Pad number: 234
  - Connected: 118
- Memory density: 16Gb/60.48 mm² 0.264 Gb/mm²

Source:
System Plus Consulting
Samsung 16Gb LPDDR5 1z DRAM Memory
Low Power DRAM Memory 1z Generation

SK Hynix LPDDR5 1y Memory

SK hynix Package Views & Dimensions

- Package: 496 balls
- Dimensions: 14.2 x 12.5 x 0.5mm
- Ball pitch: 0.4 mm
- Marking:
  - SK hynix – memory Manufacturer
  - H9JKNNNFB3AECR-N6H – component part number
  - TD8HF318Q2 – package reference

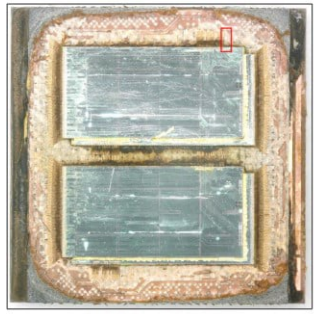


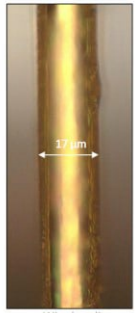
Package Front View

Package Side View

- Marking:
  - SK hynix – memory Manufacturer
  - H9JKNNNFB3AECR-N6H – component part number
  - TD8HF318Q2 – package reference

SK hynix Package Opening


Memory Package Opening



Wire bonding

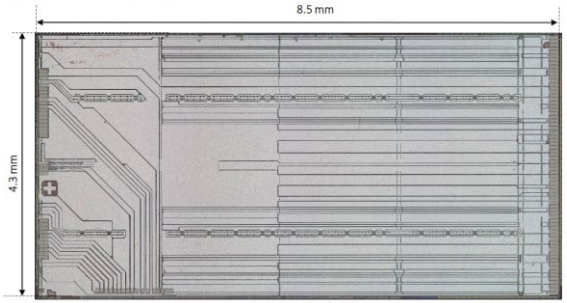
Memory Package Opening (after metal wire removal)

- Package opening reveals 8 DRAM dies.
- Package capacity: 8GB/64Gb per package
- Die capacity: 1GB/8Gb per die
- Wire bonding
  - Material: Gold wire
  - Wire number total: 680
  - Wire number per die: 85
  - Wire diameter: 17 µm
  - Wire average length: 0.75 mm

SK hynix - Memory Process Characteristics

- CMOS and metal layers front-end process:
  - Substrate: 300mm Silicon wafer
  - Process type: CMOS (Digital, Analog)
  - Metal layers: 8 total
  - CMOS technology node: 65nm for the CMOS transistors
  - Lithography steps: 43
- DRAM cell process:
  - Technology node: 1y nm (~18nm)
  - Lithography steps: 11
- Total lithography steps: 54

SK hynix Die Overview & Dimensions



Memory Die - Overview

- Die area: 36.55 mm² (8.5 x 4.3 mm)
- Nb of PGDW per 12-inch wafer: 1,760
- Pad number: 121
  - Connected: 85
- Memory density: 8Gb/36.55 mm² 0.22 Gb/mm²

Source:
System Plus Consulting
DRAM LPDDR5 Mobile Memories
Comparison of Samsung, SK Hynix and Micro Low Power DRAM Memory

Low Power Double Data Rate 5 (LPDDR5) - (JESD209-5B)

16 Die configuration, Package ballout & Pin Definition

16.1 Package Configuration

16.1.1 Package Considerations for Byte-Mode Devices

Two Byte-Mode LPDDR5 SDRAMs can be logically combined into a Standard LPDDR5 SDRAM. Byte mode devices use the same bank architecture with one row address added and the page size reduced by half compared to a standard device of the same density. Two byte-mode die of the same density can be combined to make an equivalent x16 device of twice the given density. The inputs are ganged and the DQ busses from the two devices are assigned individually to the 16-bit channels.

Packages for Standard and Byte-Mode devices share the same ballmaps. This section describes internal wiring changes and system considerations when using packages containing Byte-Mode devices.

Three different die combinations are supported:

1) Standard - Packages configured with only Standard LPDDR5 die.
2) Byte-Mode - Packages configured with only Byte-Mode LPDDR5 die.
3) Mixed - Packages configured with both Standard and Byte-Mode LPDDR5 die. In this mixed configuration, some ranks contain only Standard die and other ranks contain only Byte-Mode die.

For mixed packages, standard devices shall be assigned to the lower numbered ranks and byte-mode devices shall be assigned to the higher numbered ranks.

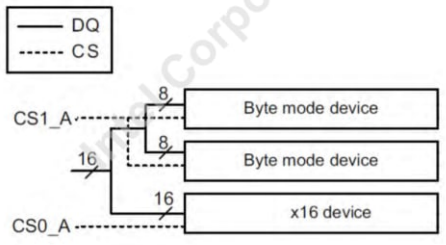


Figure 318 — Example of rank assignment for a single-channel dual-rank package

16.4 Package Die Layout

Ballmaps for LPDDR5 dual-channel packages shall follow the pad order based on the second die placement (Channel B) being rotated with respect to the first die (Channel A) placement.

Ballmaps for LPDDR5 quad-channel packages shall follow the pad order based on:

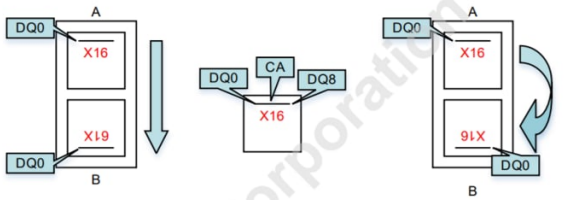
1. The Channel B die placement being rotated with respect to the Channel A die placement.
2. The Channel D die placement being rotated with respect to the Channel C die placement.

TABLE 462 IS FOR REFERENCE ONLY:

LPDDR5 is based on a single channel (x16) die concept. In contrast, LPDDR4 is based on a dual channel die concept with the pad order of the second channel being mirrored with respect to the first channel.

Examples of dual channel mirror die (LPDDR4) and single channel die (LPDDR5) package layout are shown below. LPDDR5 pad ordering has not been balloted and is shown for illustrative purposes only.

Table 462 — Package configuration example



LPDDR4 Dual Channel Mirror Die	LPDDR5 single Channel die	Example of placing 1 Ch. die in 2 Ch. configuration
• Ch. B is folded down from Ch. A.	• Pad order approach likely similar to LPDDR4	• Ch. B is rotated from Ch. A

16.5 Package Configuration

Two Byte-Mode LPDDR5 SDRAMs can be logically combined into a x16 LPDDR5 SDRAM. Byte mode devices use the same bank architecture with one row address added and the page size reduced by half compared to a x16 device of the same density. Two byte-mode die of the same density can be combined to make an equivalent x16 device of twice the given density. The inputs are ganged and the DQ busses from the two devices are assigned individually to the 16-bit channels.

Packages for x16 and Byte-Mode devices share the same ballmaps. This section describes internal wiring changes and system considerations when using packages containing Byte-Mode devices.

Three different die combinations are supported:
1) Standard - Packages configured with only x16 LPDDR5 die.
2) Byte-Mode - Packages configured with only Byte-Mode LPDDR5 die.
3) Mixed - Packages configured with both x16 and Byte-Mode LPDDR5 die. In this mixed configuration, some ranks contain only x16 die and other ranks contain only Byte-Mode die.

For mixed packages, x16 devices shall be assigned to the lower numbered ranks and byte-mode devices shall be assigned to the higher numbered ranks.

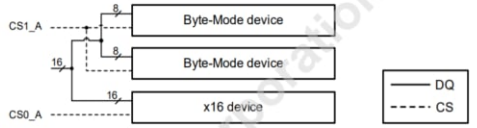


Figure 319 — Example of rank assignment for a single-channel dual-rank package

Packaged devices support only one set of latency parameters depending on the die combination:

1) Standard packages - configured with only x16 LPDDR5 dies – support x16 LPDDR5 latency parameters.
2) Byte-Mode packages - configured with only Byte-Mode LPDDR5 dies – support byte-mode latency parameters.
3) Mixed packages - configured with both x16 and Byte-Mode LPDDR5 dies – support byte-mode latency parameters

MR0 OP[1] for each die indicates the appropriate timing support.

16.6 ZQ Wiring

LPDDR5 devices are designed to allow up to NZQ die within a single package to connect to a common ZQ resource. When multiple die share a ZQ resource, one die is designated as the Initiator die. ZQ Calibration Command to Latch Time (tZQCAL4, tZQCAL8 and tZQCAL16) varies depending on the number of die sharing a ZQ resource. (See 4.2.1 for more information.)

Single and dual-channel packages shall support a single ZQ ball which is wired to all die.

Quad-channel packages support 2 ZQ balls where all die from two channels are wired to each ZQ ball. Wiring details are specified in the package ballmap.

Logical mapping – channel, rank and byte (for byte mode) - for all Initiator die is specified in the package ballmap.

Low Power Double Data Rate 5 (LPDDR5) (JESD209-5B)

JEDEC Standard No. 209-5B
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16.2 Pad Order

Table 461 — LPDDR5 Pad order

TOP					
Pad number	Pad Name	Pad number	Pad Name	Pad number	Pad Name
1	VDD2H	36	VDD2H	60	VSS
2	VSS	37	RESET_n	61	DQ7
3	VDD1	38	VDD2L	62	VDDQ
4	VDD2H	39	VSS	63	DQ6
5	VDD2L	40	CA6	64	VSS
6	VSS	41	CA5	65	DQ5
7	VDD2H	42	VDD2H	66	VDDQ
8	VSS	43	CA4	67	DQ4
9	DQ8	44	CA3	68	VSS
10	VDDQ	45	VSS	69	DMI0
11	DQ9	46	CK_c	70	VDDQ
12	VSS	47	CK_t	71	VDD2L
13	DQ10	48	VDD2H	72	VSS
14	VDDQ	49	CS	73	WCK0_t
15	DQ11	50	CA2	74	WCK0_c
16	VSS	51	VSS	75	VDD2H
17	RDQS1_t	52	CA1	76	VDDQ
18	RDQS1_c	53	CA0	77	RDQS0_c
19	VDDQ	54	VDD2H	78	RDQS0_t
20	VDD2H	55	VDD2L	79	VSS
21	WCK1_c	56	VSS	80	DQ3
22	WCK1_t	57	ZQ	81	VDDQ
23	VSS	58	VDDQ	82	DQ2
24	VDD2L	59	VDD2H	83	VSS
25	VDDQ			84	DQ1
26	DMI1			85	VDDQ
27	VSS			86	DQ0
28	DQ12			87	VSS
29	VDDQ			88	VDD2H
30	DQ13			89	VSS
31	VSS			90	VDD2L
32	DQ14			91	VDD2H
33	VDDQ			92	VDD1
34	DQ15			93	VSS
35	VSS			94	VDD2H
				Bottom	

NOTE 1 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.
NOTE 2 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

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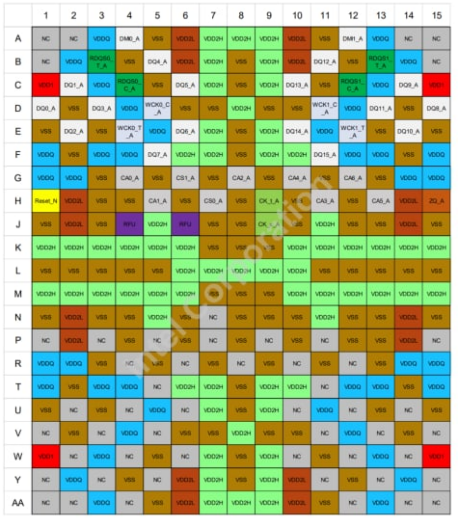
16.3 Package Ballout

16.3.1 315-ball 1CHx16 Discrete Package, 0.80mm x 0.70mm using MO-338A



NOTE 1 0.8mm pitch (X-axis) 15 columns, 0.7mm pitch (Y-axis), 21 rows.
NOTE 2 Top View, A1 in top left corner.
NOTE 3 ZQ_A ball supports Channel A.
NOTE 4 ZQ Initiator Die for ZQ_A shall be assigned to Rank 0 of Channel A die. If this rank is composed of byte-mode dice, the lower die shall be the initiator die.

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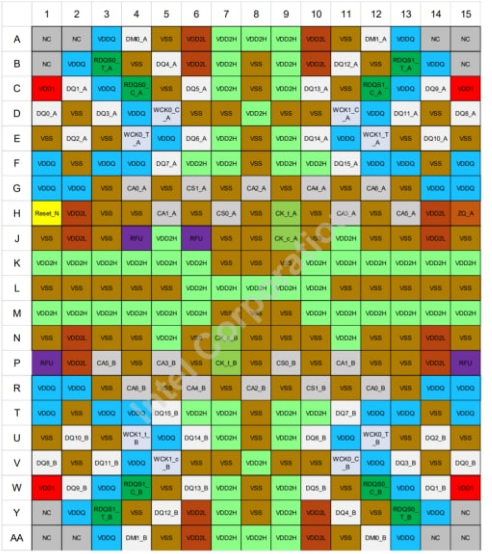
16.3.2 315-ball 2CHx32 Discrete Package, 0.80mm x 0.70mm using MO- 338A



NOTE 1 0.8mm pitch (X-axis) 15 columns, 0.7mm pitch (Y-axis), 21 rows.
NOTE 2 Top View, A1 in top left corner.

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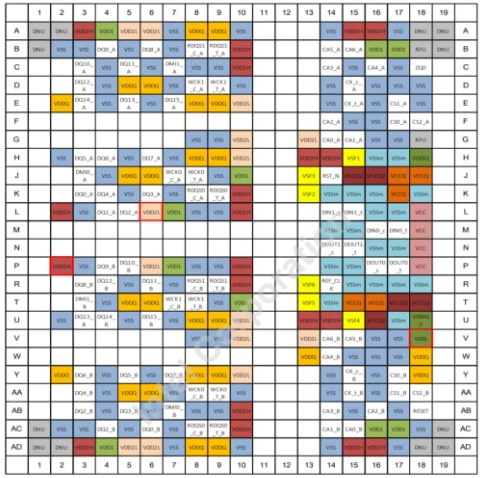
16.3.3 297 ball UFS MCP Two-Channel FBGA (top view) using MO-276



NOTE 1 0.5mm pitch, 24 rows x 19 columns.
NOTE 2 11.5 mm x 13 mm and 13 mm x 14 mm body size.
NOTE 3 Top View, A1 in top left corner.
NOTE 4 CS2_A and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.
NOTE 5 ZQ Initiator Die for ZQ0 ball shall be assigned to Rank 0 of Channel A die. If this rank is composed of byte-mode die, the lower byte die shall be the Initiator die.
NOTE 6 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

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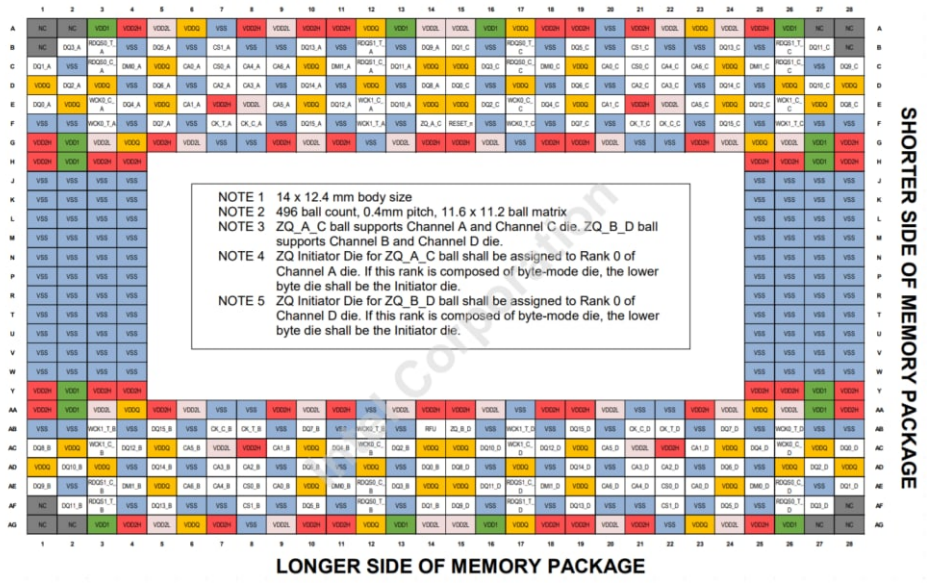
16.3.4 LPDDR5 496 ball PoP Quad x16 Channel FBGA using MO-344



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16.3.5 LPDDR5 441ball x64 discrete package, 0.65 mm x 0.65 mm using MO-342

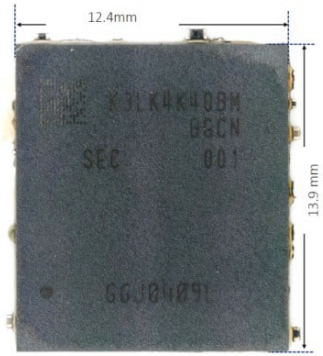
NOTE 1 14 mm x 14 mm body size
NOTE 2 441 ball count, 0.65 mm pitch, 21 x 21 ball matrix
NOTE 3 Top view, A1 is in top left corner.
NOTE 4 ZQ_A_C ball supports Channel A and Channel C die. ZQ_B_D ball supports Channel B and Channel D die.
NOTE 5 ZQ Initiator Die for ZQ_A_C ball shall be assigned to Rank 0 of Channel A die. If this rank is composed of byte-mode die, the lower byte die shall be the Initiator die.
NOTE 6 ZQ Initiator Die for ZQ_B_D ball shall be assigned to Rank 0 of Channel D die. If this rank is composed of byte-mode die, the lower byte die shall be the Initiator die.
NOTE 7 This package shall not be used double-sided unless solder joint reliability satisfies application requirements.

Apple DRAM Supplier Identification → Samsung (SEC)

Samsung LPDDR5 1y

Samsung LPDDR5 Package

Package:	BGA- 496
Dimensions:	13.9 x 12.4 x 0.6 mm
Surface:	172mm²
Pitch :	0.4mm



Package Top View
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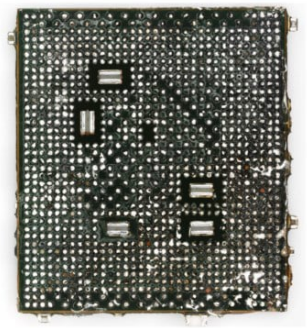

Package Bottom View
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Package Side View
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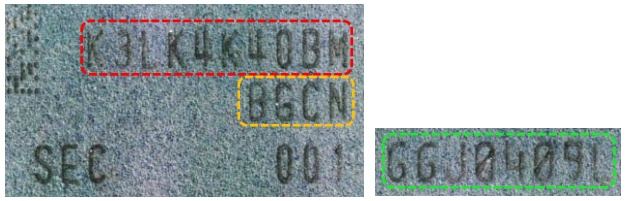
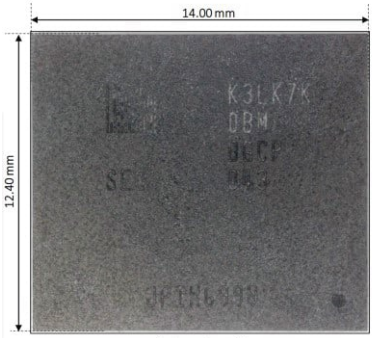


K3LK4K40BM – Component reference
BGCN
SEC - Component manufacturer (Samsung Electronics Corporation)
001
GGJ0409L - Package trace code

Samsung LPDDR5 1z

Package Views & Dimensions

- Package: BGA 496 balls
- Dimensions: 14.00 x 12.40 x 0.38 mm
- Ball pitch: 0.4 mm
- Marking:
  - SEC: Samsung Semiconductor component manufacturer
  - K3LK7K70BM: Component Reference
  - BGCP:
  - 043:
  - JPIX6990:



Package Front View
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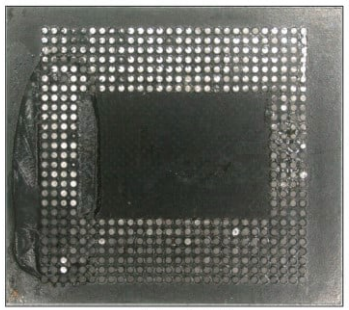

Package Back View
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Package Side View
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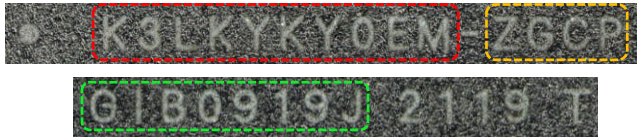
SEC: Samsung Semiconductor component manufacturer
K3LK7K70BM: Component Reference
BGCP:
043:
JPIX6990:

Apple LPDDR5 M1 Pro/Max



The Apple M1 Pro/Max LPDDR5 memory packages are from Samsung Electronic Corporation as laser mark part number code suggests.

Samsung LPDDR4X Memory

IC

Manufacturer	SAMSUNG
Manufacturer Country (HQ)	Korea, Republic of
IC Name	K3UHAHA0AMAGCL
IC Type	MEMORY DDR RAM
Part Description	12GB LPDDR4X SDRAM
Datasheet link	https://www.samsung.com/semiconductor/dram/lpddr4x/K3UHAHA0AM-AGCL/

Packaging

L	12.42 mm
W	12.42 mm
Area	154.3 mm2
H	0.84 mm
balls/pins	556
Pitch	0.4 mm
Type	POP TOP
Substrate material	FR4 3Layers 0.12mm H
Markings	SEC 919 K3UHAHA 0AMAGCL GHA9369T 1929 B NH4BR MP8

Die Info

# Die	12
All Die Area	412.8 mm2
all die area/pkg	2.68

Die 1 Info

L	8 mm
W	4.3 mm
Manufacturer	SAMSUNG
Process (nm)	14
Description	SAMSUNG, SEC Y 3, 8Gb LPDDR4 SDRAM
Quantity	12

Manf. $

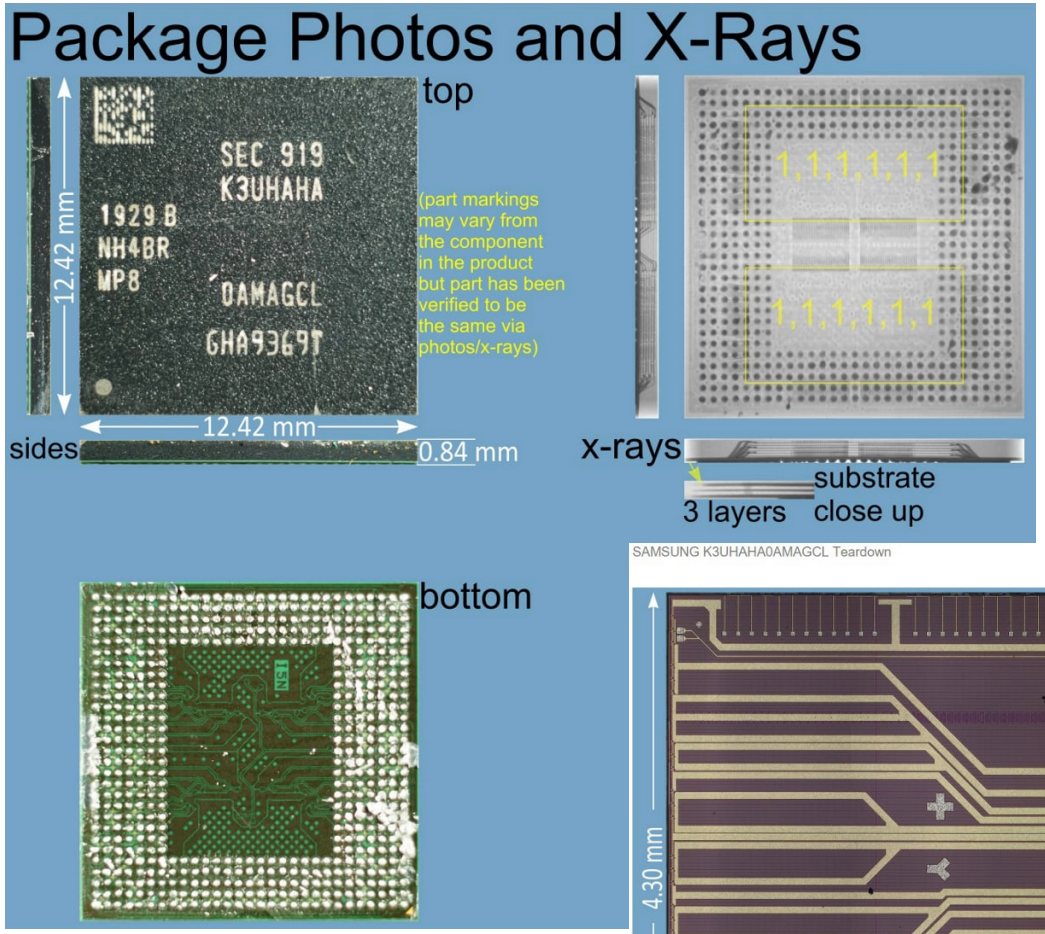
Est. ASP $	39.7651
GM%	35.0%
Est. cost $	0

Est. ASP$ as of 1Q 2022

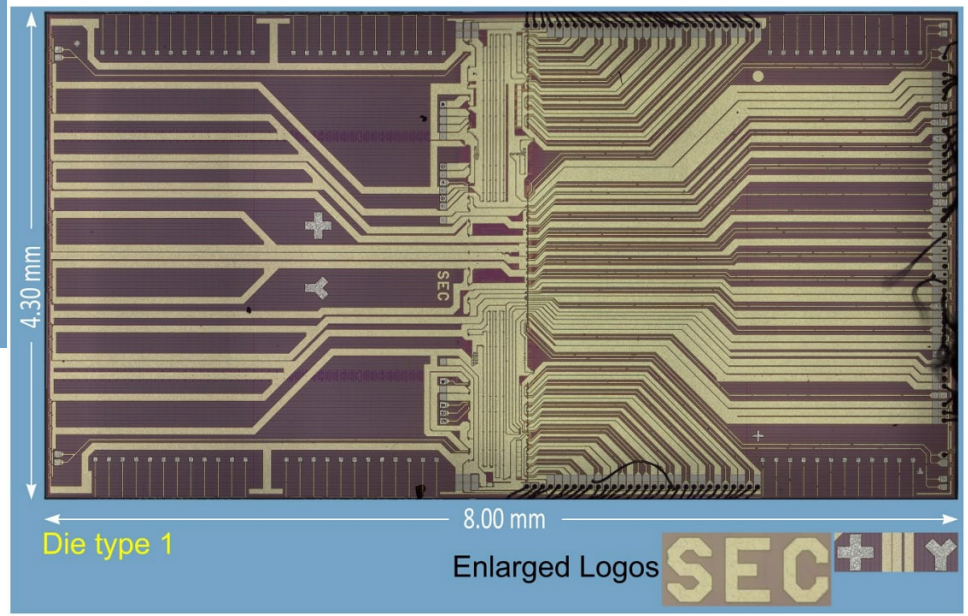
US$	39.7651

Included In

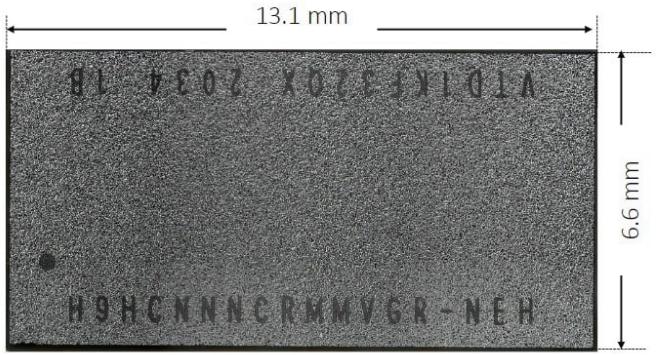
VIVO X60 Pro 5G (China)
OPPO Reno5 Pro 5G
SAMSUNG Galaxy Note10+ 256GB
Realme GT Neo 5G
OPPO Reno3 5G 12GB RAM
SAMSUNG Galaxy Fold



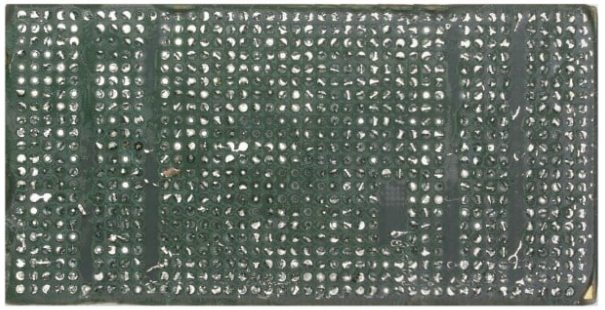
SAMSUNG K3UHAHA0AMAGCL Teardown



Apple M1 **SK Hynix** LPDDR4 Memory



Memory Package Top view
©2020 by System Plus Consulting



Attribute	Measurements
DRAM Form Factor	13.1 x 6.6 mm
BGA Count	877
BGA Pitch	0.28 mm
# of Die	4
Die Thickness, 1-4	38 µm
DAF Thickness	20 µm
Total DRAM Thickness	53 µm
DRAM package Thickness	0.57 mm
Total Mold Thickness	0.44 mm
Overmold Thickness on Die	0.12 mm
Die edge to Mold Edge	0.99 mm / 1.3 mm
Die Size	34.02 mm²
Ball Pitch	0.28 mm

DRAM Package Opening

DRAM Package
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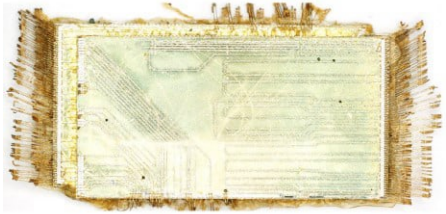
Each DRAM Package has a capacity of 32Gb per package.
There are 4 dies in each DRAM Memory Package.
Therefore each DRAM die capacity is 8Gb/1GB.

- Total Number of interconnect wires: 356 for 4 dies
- Inteconnect wires per die: 89
- Wire Diameter : ~ 17 µm
- Wire Material : Gold
- Wire average length: 1.1 mm



DRAM Package Opening
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Wire
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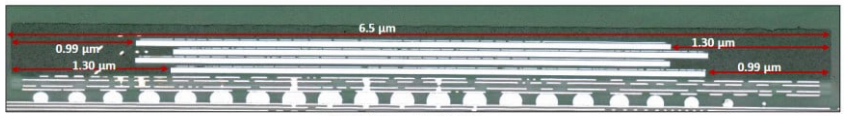
DRAM- Package Cross Section



DRAM Package Cross Section
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Memory Package Top view
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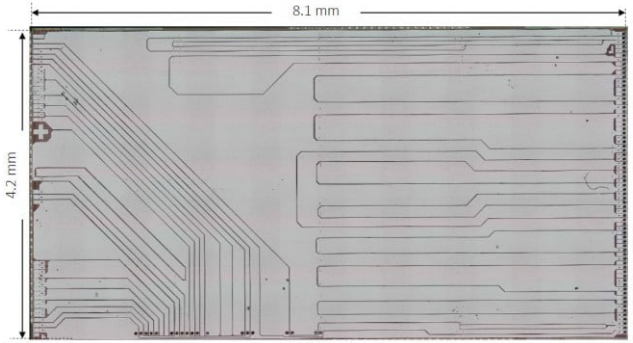
DRAM Die Dimensions& View



DRAM Die View
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Die Area : 34.02 mm²
(8.1 mm x 4.2 mm)

Pads per memory die
Pad number : 133
Wires connected : 89
Test pads only: 32
Unused pads: 12

Die Density: 8Gb/34.02 mm²
0.24Gb /mm²

P/N	H 9HC	NNN	CR	M	M	VG	R	-N	E	H
Decode	Hynix LPDDR 4	No NVM	32 Gb	1.1V/0.6V	1st Gen.	New PKG	Pb & Halogen Free	No NVM	4266 Mbps	Special Temp.

Apple M1 Max SoC (Die Area) - 3D X-Ray