

Design Techniques for High-Speed Low-Power Wireline Receivers

by

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Abstract

High-speed data transmission through wireline links, either copper or optical based, has become the backbone for modern communication infrastructure. Since at multi-Gb/s data rates the transmitted signal is attenuated and distorted by the channel, sophisticated analog front-end and/or digital signal processing are required at the receiver (RX) to recover data and clock from the received signal.

In this thesis, both analog- and digital-based receivers are investigated, and power-reduction techniques are exploited at both system- and circuit-levels. A speculative successive-approximation register (speculative/SAR) digitization algorithm is proposed for use at the receiver front-end of digital receivers that combines equalization and data recovery with the digitization step at the front-end analog-to-digital converter (ADC). Furthermore, an architecture for quadrature clock generation is proposed which is of use in both analog and digital receivers. Then, an analog clock and data recovery (CDR) architecture suitable for high data rates (e.g., beyond 10 Gb/s) is proposed that utilizes a wideband data phase generation technique to facilitate mixer-based phase detection. The CDR architecture is implemented and experimentally validated for a 12.5 Gb/s system. Finally, a mixed-mode hardware-efficient CDR architecture is proposed that exploits both analog

Abstract

and digital design techniques to reach a robust operation suited for long-haul optical link communications. Proof-of-concept prototypes of the proposed RX architectures are designed and implemented in 65 nm and 90 nm CMOS processes. The prototypes are successfully tested. Note that although individual performance merits of the each prototype may not necessarily outperform that of the state-of-the-art, however, the prototypes confirm the feasibility of the proposed structure. Furthermore, the proposed architectures can be used at higher data rates particularly if more advanced technologies with higher device transit frequency, (f_T), is used.

Preface

I, Arash Zargaran-Yazd, am the principle contributor of all chapters. Professor Shahriar Mirabbasi who supervised the research has provided technical consultation and editing assistance on the manuscript. Hooman Rashtian and Kamyar Keikhosravy have respectively contributed to the design of VCO and comparator of the prototype chip presented in Chapter 6. As described below, some of the chapters in this thesis have been written based on the following published work.

Conference papers:

A. Zargaran-Yazd, S. Mirabbasi, and R. Saleh, “A 10 Gb/s low-power SerDes receiver based on a hybrid speculative/SAR digitization technique,” in *ISCAS*, may 2011, pp. 446–449 →Chapter 3

A. Zargaran-Yazd and S. Mirabbasi, “A 25 Gb/s full-rate CDR circuit based on quadrature phase generation in data path,” in *ISCAS*, May 2012, pp. 317–320 →Chapters 4, and 5

Journal papers:

A. Zargaran-Yazd and S. Mirabbasi, “Low-power design technique for decision-feedback equalisation in serial links,” *Electronics Letters*,

vol. 48, no. 17, pp. 1042–1044, 2012 →Chapter 2

A. Zargaran-Yazd, K. Keikhosravy, H. Rashtian, and S. Mirabbasi, “Hardware-efficient phase-detection technique for digital clock and data recovery,” *Electronics Letters*, vol. 49, no. 1, pp. 20–22, 3 2013 →Chapter 6

A. Zargaran-Yazd and S. Mirabbasi, “12.5-Gb/s full-rate CDR with wideband quadrature phase shifting in data path,” *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 60, no. 6, pp. 297–301, 2013 →Chapter 5

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List of acronyms

ADC	analog to digital converter
ADFE	analog decision feedback equalizer
ASDFE	adaptive slicer decision feedback equalizer
BER	bit error rate
CDR	clock and data recovery
CPW	coplanar wave guide
CTLE	continuous time linear equalizer
DAC	digital to analog converter
DFE	decision feedback equalizer
DLL	delay locked loop
DR	data rate
DSP	digital signal processing
FD	frequency detector
FFE	feed forward equalizer
FIR	finite impulse response
IC	integrated circuit
IP	internet protocol
ISI	inter symbol interference

LUDFE	loop unrolled decision feedback equalizer
MUX	multiplexer
NRZ	non return to zero
PCB	printed circuit board
PD	phase detector
PDC	phase detector characteristic
PI	phase interpolator
PLL	phase locked loop
PSD	power spectral density
QCG	quadrature clock generator
QPC	quadrature phase corrector
QPS	quadrature phase splitter
RX	receiver
SAR	successive approximation register
SASDFE	speculative adaptive slicer decision feedback equalizer
SERDES	serializer deserializer
TRX	transceiver
TX	transmitter
UI	unit interval
VCO	voltage controlled oscillator
XO	crystal oscillator

List of symbol definitions

A	signal amplitude
c_{dd}	total drain capacitance
c_{gd}	gate drain capacitance
c_{gg}	total gate capacitance
c_{gs}	gate source capacitance
c_{lat}	lateral capacitance
c_{sub}	capacitance to substrate
C_L	load capacitance
$CLKH$	full-rate clock
$CLKL$	sub-rate clock
CLK_{rec}	recovered clock
D_{eq}	equalized data
D_{rec}	recovered data
D_{rx}	received data
D_x	XORed data
f_0	nominal frequency
f_{bw}	3-dB bandwidth frequency
f_T	unity gain frequency of transistor
g_m	transistor transconductance

List of symbol definitions

\mathbf{I}_{cpl}	coupling current
\mathbf{I}_{d}	drain current
\mathbf{I}_{ss}	tail current
\mathbf{L}	inductance
\mathbf{Q}	quality factor
\mathbf{r}_{o}	output resistance of transistor
\mathbf{R}_{T}	termination resistance
\mathbf{t}_{p}	propagation time
$\mathbf{v}_{\text{cursor}}$	absolute cursor voltage
\mathbf{v}_{gs}	transistor gate source voltage
\mathbf{V}_{o}	output voltage
\mathbf{v}_{od}	transistor overdrive voltage
\mathbf{v}_{sw}	peak voltage swing
\mathbf{v}_{th}	transistor threshold voltage
λ	channel length modulation factor
θ	phase error
ϕ_{I}	in-phase signal component
ϕ_{Ib}	in-phase inverted signal component
ϕ_{q}	quadrature-phase signal component
ϕ_{qb}	quadrature-phase inverted signal component
\mathcal{L}	phase noise
ω	angular frequency
ω_{n}	natural angular frequency
τ	time constant

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Dedication

To my parents

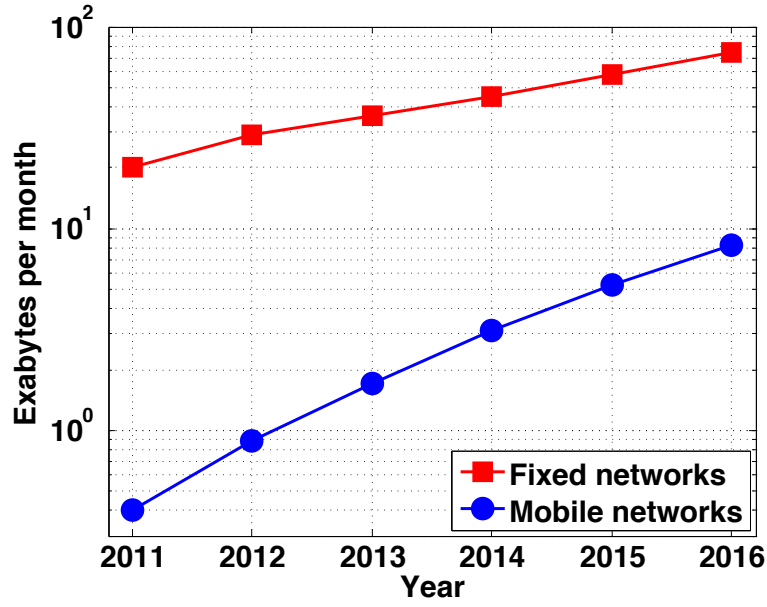
Chapter 1

Introduction

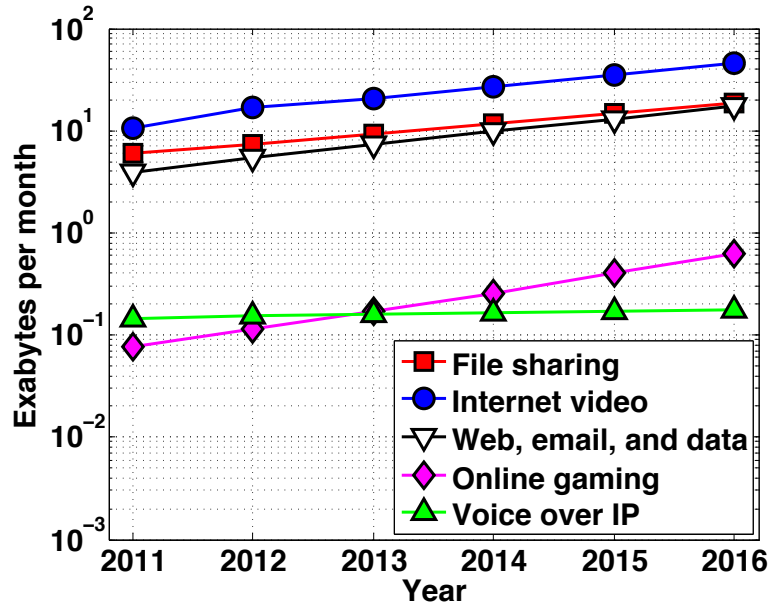
1.1 Motivation

Fueled in part by the growing trend of cloud-based computation and storage, and high-speed wireless data access, the global demand for communication bandwidth has continued to unprecedentedly increase. It is expected that by 2016, the global annual data traffic will reach 1.3 zettabytes per year (10^{21} bytes per year) or 110.3 exabytes per month (10^{18} bytes per month). Such data traffic would be equivalent to transferring all movies ever made in history every 3 minutes [1]. Figure 1.1a shows the speculated trend in global internet protocol (IP) traffic growth for fixed and mobile networks. Figure 1.1b categorizes the total IP traffic based on the type of usage. It can be observed that the data traffic is expected to increase by roughly two orders of magnitude by 2016, over a decade period. Figure 1.2 shows the historical trend of data rates in both optical links and Ethernet standards. Note that the data rates in these standards are mostly set based on the trend of the bandwidth demand as illustrated in Fig. 1.1a, rather than by the speed limits of the available monolithic integrated circuit (IC) technologies. According to Fig. 1.2, to address the trend in global bandwidth demand, the most recent standards call for data rates up to 100 Gb/s in the

1.1. Motivation



(a)



(b)

Figure 1.1: Trend of global IP traffic based on type of network (a), and the traffic trend based on type of usage (b). Plotted based on data provided in [1].

backbone wireline channels. While the higher cost of optical modules and challenges in integration with a monolithic transmitter (TX) and receiver (RX) increases the overall cost of optical data transmission as compared to electrical transmission, optical mediums have been historically preferred in high-speed standards. This is primarily due to the lower high-frequency loss of an optical medium compared to a metal-based medium (e.g., copper cables). However, as illustrated in Fig. 1.2, the data-rate gap between optical and electrical (Ethernet) links has been continuously reduced in the recent years. One major motivation for such trend is the vital role that the cost factor plays in commercial applications. However, technically this can be explained by the advancements in the wireline transmitter and receiver designs which enable high-speed data transmission over lossy and low-cost electrical channels. Among the TX and RX, the design of a wireline RX can be more challenging due to the distortion of data in the channel. Addressing some of the most important trade-offs and challenges specific to the RX is the goal of this research.

1.2 Serial-link data transmission and reception

The infrastructure of modern wireless and wireline communication systems is composed of multiple backplanes, each of which having several chips on them. The connection between different boards and chips is realized through a series of package I/Os, as well as vias, stubs, connectors and copper traces drawn on printed circuit boards (PCBs). The ever increasing Ethernet traffic and prevalence of multicore CPU architectures calls for a substantial increase

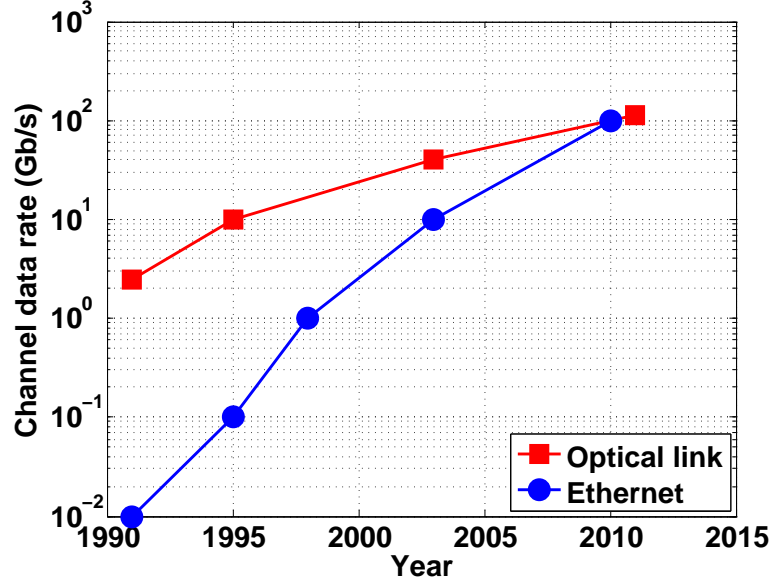


Figure 1.2: Historical trend of channel data rates in optical link and Ethernet standards.

in the speed of board-to-board and chip-to-chip data transfer. Although the data is usually transmitted in parallel format within ICs, serial links have become the optimum design choice for connection between chips and boards at multi-Gb/s data rates. The stringent requirements of allowable skew between different channels of parallel data bus and the small tolerable clock jitter limit the application of parallel data transmission to lower speed links.

There are two aspects of a serial link that differentiate it from a parallel link (also known as a “bus”). First, as annotated in Fig. 1.3, a serial link is a single transmission channel with a line data rate, DR_s , that is multiple of the individual line data rate DR_p in a parallel link, and can be written as

$$DR_s = \widehat{DR_p} = n_p \times DR_p \quad (1.1)$$

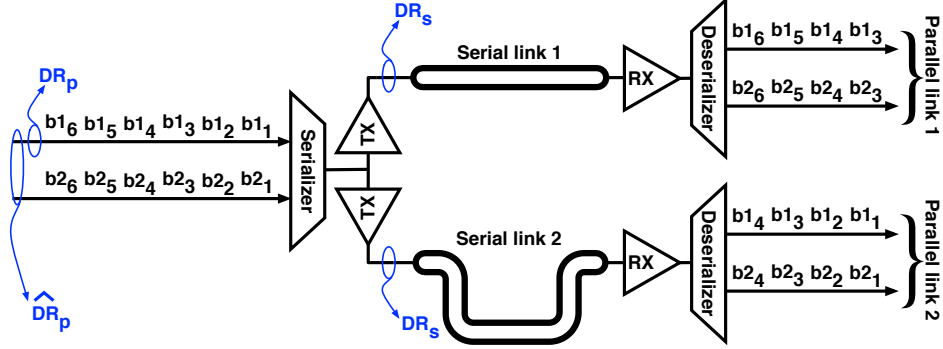


Figure 1.3: Visual comparison of the zero skew allowance in parallel links versus arbitrary skew allowance in serial links.

where $\widehat{DR_p}$ and n_p are the total data rate of a parallel link, and the number of transmission channels (lines) in the parallel link, respectively. The conversion from multiple channels to a single channel running at a faster data rate is performed using a serializer. The data on a serial link can be converted to a parallel format through a deserializer.

Second, a group of data lines in a parallel link are logically differentiated from a group of serial links through the difference in skew tolerance among the channels in each of the groups. As shown in Fig. 1.3, by definition, there is typically a very small (i.e., a fraction of unit interval) tolerance for skew among the channels in the former group. However, in serial links, there can be an arbitrary skew among the channels. The freedom in skew, and a smaller physical footprint of a serial link as compared to a parallel link have proved advantageous in high-speed data transmission from both cost and design standpoints.

Figures 1.4a and 1.4b show two common forms of serial data transmission. In Fig. 1.4a, the transmitter and receiver pairs are typically located in the

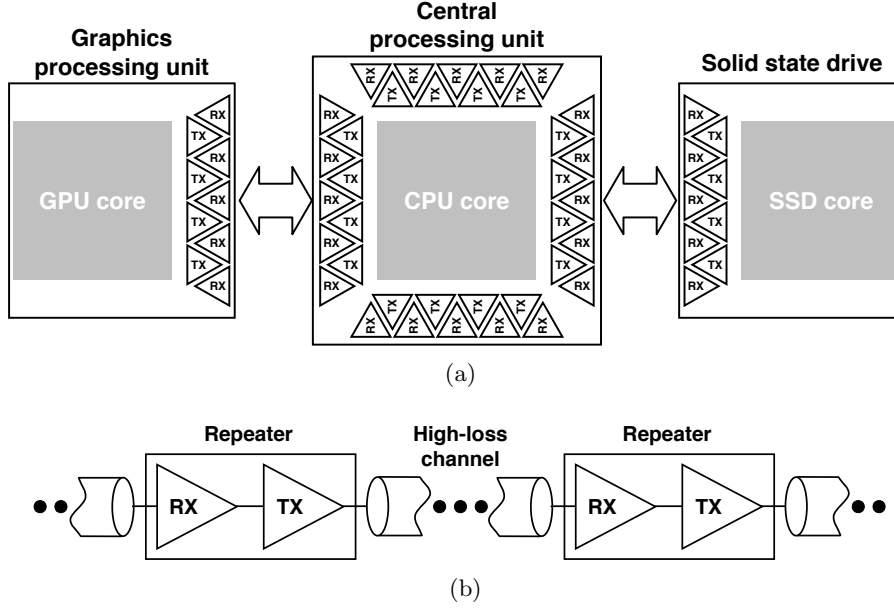


Figure 1.4: Typical usage of TX-RX pairs in backplanes and motherboards (a), and usage of TX-RX pairs as repeaters in long-haul optical communication (b).

boundaries of chips which need to talk to other chips located on the motherboards and backplanes. Figure 1.4b shows another form of usage in which each TX-RX pair form a repeater chip. Such repeaters are placed in certain locations along a high loss channel, as in long-haul links. An example of such use of TX-RX pairs is in submarine communication cables.

1.3 Clocking schemes in serial links

While data transmission and reception in serial links can be categorized based on many aspects, characterization based on the clocking scheme is especially useful for system-level design. Figure 1.5 classifies the clocking

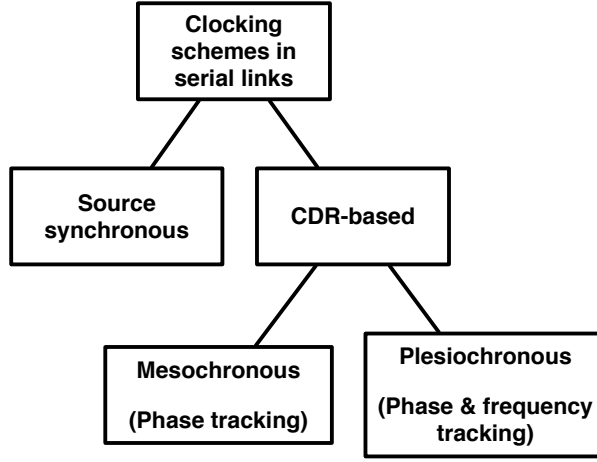


Figure 1.5: Classification of clocking schemes in serial links.

schemes in serial links. In the source synchronous scheme (Fig. 1.6a), the clock is forwarded along with data from TX to RX. The clock path and data paths are designed to have equal propagation delays. This insures that the relative phase offset between data and clock remains constant as they travel through the matched channels. An active or passive delay element producing the delay value clk_{del} is used at RX to align the sampling edge of the clock to the middle of the data eye. There are two drawbacks associated with this clocking scheme: First, it is challenging to maintain a constant clk_{del} among process, voltage, and temperature (PVT) corners. Second, it might be challenging or unfeasible to maintain the delay match between the data and clock channels due to the area constraints imposed by other blocks and transceivers. Also, the channel incurs different propagation delays for the data which has broadband frequency characteristic, and the relatively narrowband clock.

1.3. Clocking schemes in serial links

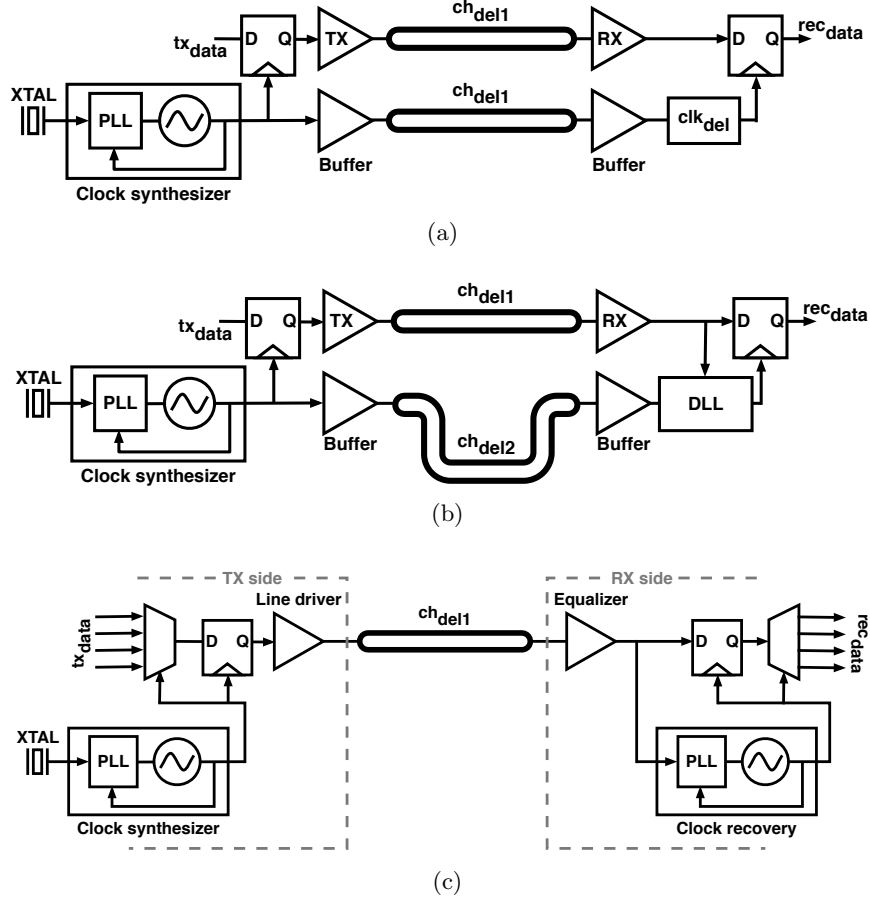


Figure 1.6: Source synchronous (a), Mesochronous (b), and Plesiochronous (c) clocking schemes in serial links.

A clock and data recovery (CDR) based clocking schemes can be either Mesochronous, or Plesiochronous. In the Mesochronous scheme (Fig. 1.6b), clock is still forwarded to RX; however, there is no matching constraint for the delay of data channel, ch_{del1} , relative to the delay of the clock channel, ch_{del2} . Therefore, while the clock frequency at RX and TX match, RX needs a mechanism to recover the correct phase of the sampling clock based on the received data. Such task is usually performed through a delay-locked loop

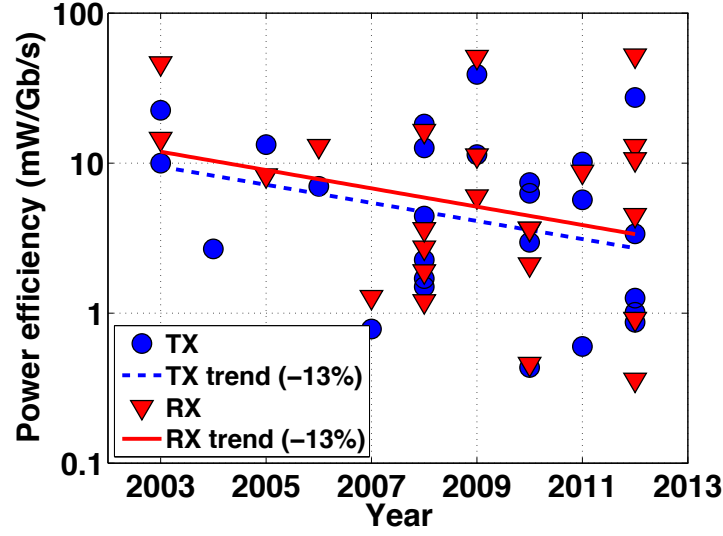
(DLL).

In the Plesiochronous scheme (Fig. 1.6c), only data is sent to RX. Hence, both TX and RX have their own local clocks. The TX and RX clocks are both synthesized locally using a phase-locked loop (PLL). However, TX PLL utilizes a local crystal oscillator (XO) as the reference, while RX uses the received data as the reference for the clock synthesis PLL. This allows for arbitrary, yet limited, phase and frequency offset between RX and TX clocks. Therefore, a Plesiochronous TX-RX pair is more flexible to be used in applications that do not allow for a separate clock route, or wherever a perfect match between ch_{del1} and ch_{del2} is not possible. While such clocking scheme doesn't have the disadvantages mentioned for the source synchronous method, it comes at the price of complexity and area/power overhead that CDR imposes on RX. Designing power efficient CDRs at multi Gb/s speeds is an active area of research.

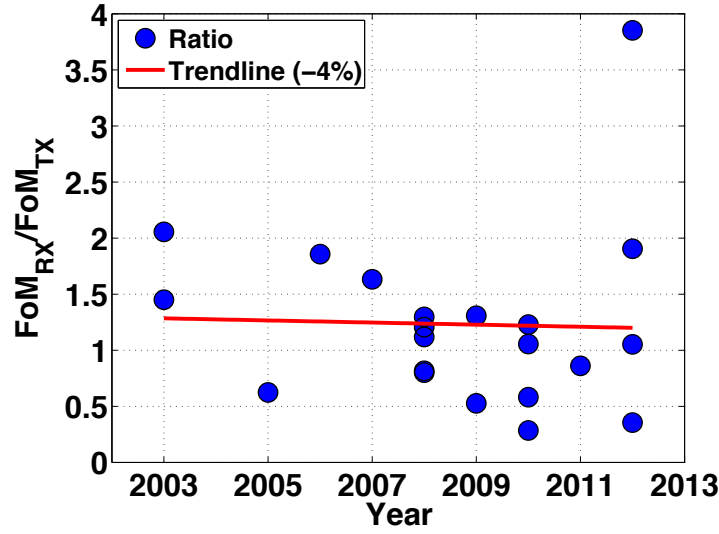
1.4 Power efficiency of wireline TX and RX

To motivate this work and investigate techniques for enhancing the overall power efficiency of a serial link, it is helpful to compare the power consumption of TX versus that of RX. A commonly used figure-of-merit (FoM) for wireline systems is the power efficiency of the link¹ which is measured in mW/(Gb/s) and provides a mean to compare the efficiency of TX, RX, or the overall transceiver (TRX). The associated FoMs are denoted as FoM_{TX} , FoM_{RX} , or FoM_{TRX} , respectively. Figure 1.7a compares the power effi-

¹Or similarly, power efficiency of a stand-alone TX or RX.



(a)



(b)

Figure 1.7: Trend in power efficiency FoM for TX (FoM_{TX}) and RX (FoM_{RX}) (a), and the trend of $\frac{FoM_{RX}}{FoM_{TX}}$ (b). For more information regarding the data plotted in Figs. 1.7a and 1.7b please refer to [2–24], and [2–17], respectively. Note that some of the references either report more than one TX-RX, or report power consumptions for several data rates.

1.5. Summary of objectives and contributions

ciency of TX and RX architectures which have been published in the past decade. The trendline of both FoM_{TX} and FoM_{RX} demonstrate a reduction of -13% per year. Also, the average power consumption for the RX block is approximately 15% more than that of the TX block. Note that Fig. 1.7a illustrates results from literature that report either individual TX or RX, or a TRX. Figure 1.7b shows the ratio $\frac{FoM_{RX}}{FoM_{TX}}$ for the published work that present a TRX where the power for RX and TX blocks are individually reported. As the trendline in this figure demonstrates, power consumption of RXs are on average 25% more than that of the TX. This trend is almost flat over time which indicates that the RX is typically expected to consume a larger portion of the overall link power budget. Additionally, given that a large portion of TX power consumption is due to the requirement of driving a $25\ \Omega$ impedance ($50\ \Omega$ channel $\parallel 50\ \Omega$ termination) with a certain voltage swing dictated by the standard, the power budget of the TX is more constrained. Therefore, in this research we focus on the RX.

1.5 Summary of objectives and contributions

The main research objectives of this work are as follows:

- Designing a digitization algorithm to address the specific requirements of low-power multi-Gb/s wireline RX. Currently, the major obstacle in designing digital high-speed serial link receivers is the power consumption of the front-end baud-rate ADC. The power consumption and area of a generic full-flash ADC makes its integration into the receiver a challenging task. To address this issue, we have developed

a speculative/SAR ADC which can operate at speeds comparable to a full-flash ADC, while consuming less power.

- Designing and analyzing the performance and power consumption of an injection-locked quadrature clock generator. Such block is an integral part of CDRs that require a quadrature-phase clock in addition to the in-phase clock component. Optimizing the power dissipation of this block is discussed from both circuit-level and system-level perspectives.
- Proposing and developing an analog receiver architecture that utilizes a mixer-based phase detection mechanism to achieve relatively low power consumption at data rates beyond 10 Gb/s. The CDR comprises the proposed quadrature clock generator.
- Design of a hardware-efficient mixed-mode eye monitoring technique for clock and data recovery. The design addresses the power consumption issue from system-level.

1.6 Organization of thesis

Figure 1.8 demonstrates the receiver blocks that are addressed in chapters of this thesis. Below is the description and breakdown:

Chapter 2 focuses on equalization in both analog and digital RX.

Chapter 3 discusses a digitization algorithm for ADC-based RX.

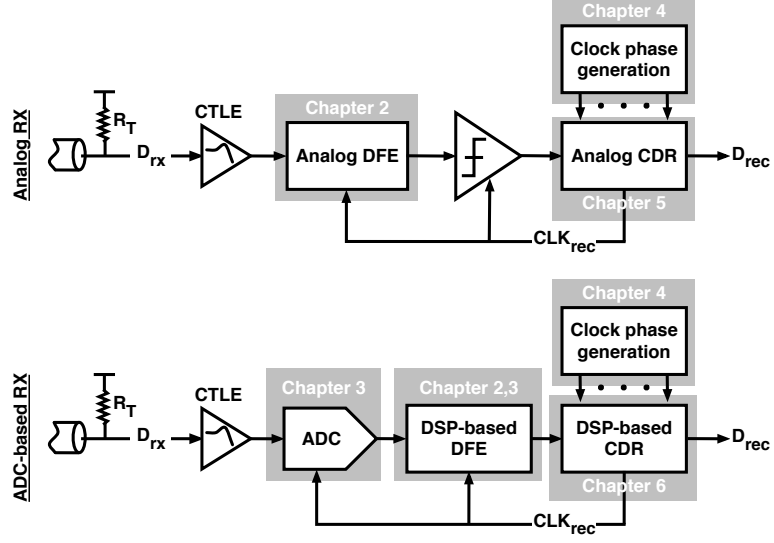


Figure 1.8: Block diagram showing the outline and breakdown of the thesis.

Chapter 4 presents an architecture for quadrature clock generation, and the associated power consumption optimization.

Chapter 5 presents an analog architecture for clock and data recovery, employing the proposed clock generation technique.

Chapter 6 presents a mixed-mode CDR architecture that partitions the RX blocks into analog and digital domains.

Chapter 7 concludes this thesis and discusses the potential future work.

Chapter 2

Low-power equalization

The continues scaling of integrated circuits has increased the speed of the on-chip signal processing. However, the data transmission channels (i.e. copper wires in printed circuit boards) have roughly stayed the same. Long gone are the days where the transmission channels were considered ideal over the bandwidth of signal. In this chapter, first the mechanism of data distortion due to a lossy channel is described. Then, various methods of data equalization are introduced. Finally, this Chapter focuses on addressing the power consumption aspect of decision feedback equalization in high-speed serial links.

2.1 Channel as a low-pass filter

Due to dielectric loss, skin effects, and parasitic crosstalk with adjacent channels, the signal observes the channel as a low pass filter, which attenuates the high-frequency components of the transmitted signal, and also adds deterministic and random noises to it.

Figure 2.1 shows the top and side views of a simple one layer printed circuit board (PCB). The bottom layer is a grounded conductor (typically copper) to serve as a global ground, and provide noise isolation. Each layer

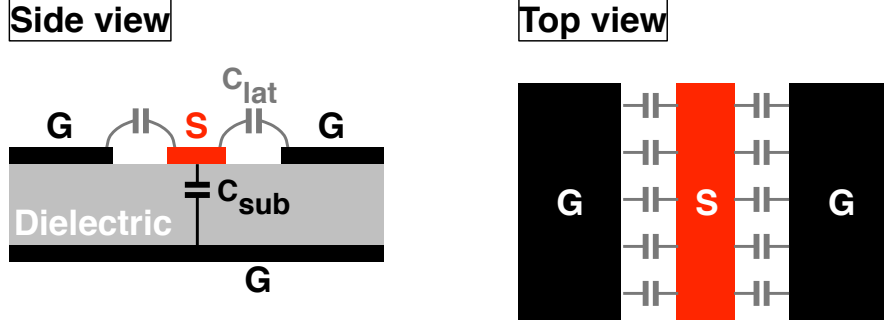


Figure 2.1: Side and top views of a CPW PCB trace.

of conductor is isolated from the next conductor layer through a dielectric. As Fig. 2.1 illustrates, the signal trace (S) is shielded from both sides using ground (G) traces. Such structure forms a coplanar wave guide (CPW) channel and is useful to reduce crosstalk among different signal traces. However, such isolation comes at the price of lateral parasitic capacitance, c_{lat} , on the signal line, which degrades the frequency response of the channel. Also, the parasitic capacitance to the grounded substrate, c_{sub} , results in additional signal loss. For the value of C_{sub} per unit area, c_{sub} we can write

$$c_{sub} \propto \frac{\epsilon}{d} \quad (2.1)$$

where ϵ and d are the dielectric constant and thickness of dielectric, respectively. Therefore, based on 2.1, to reduce c_{sub} , we should either decrease ϵ or increase d . Increasing d is not optimal as results in a thicker PCB, and decreasing ϵ requires materials that considerably increase the cost of PCB.

2.2 Inter-symbol interference

The Nyquist criterion states that if the relation given by

$$T \geq \frac{1}{2 \times W} \quad (2.2)$$

holds, a Nyquist pulse² can be transmitted through the channel without being distorted. Here, T is symbol (bit) duration and W is the channel bandwidth. However, while serial link data rates have considerably increased in the last decade (Fig. 1.2), the bandwidths of the links have not increased at the same rate and typically we have $T \ll 1/(2W)$. As the symbol duration is reduced below the limit defined by the Nyquist criterion, distortion-free data transmission becomes impossible. To explain the mechanism of data distortion, we briefly discuss the frequency response of channel.

Figure 2.2 shows the frequency and phase responses of a 10" CPW FR4 channel. The magnitude response of channel resembles that of a low-pass filter. As a result, the sharp edges in the transmitted waveform would be observed as rounded curves at the receive side [25].

The phase response indicates that depending on frequency, the various harmonics of broadband received data experience unequal propagation delays through the channel. This separates the frequency components of the data in time domain; hence, partially merging a bit to its pre-cursor and post-cursor bits. This issue, being described as Inter-symbol interference (ISI), degrades the quality of the data at the receive side of the channel. Higher data rates (i.e. shorter T), or lower channel bandwidth aggravate this prob-

²As an example, a pulse that has a raised-cosine spectra.

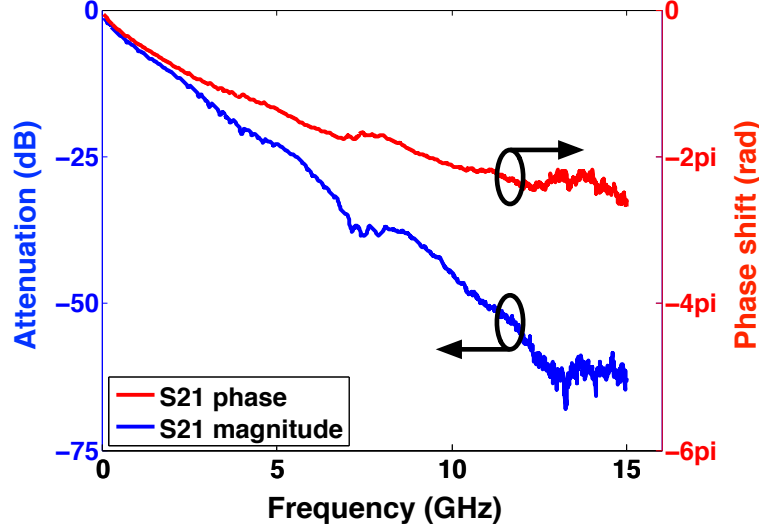


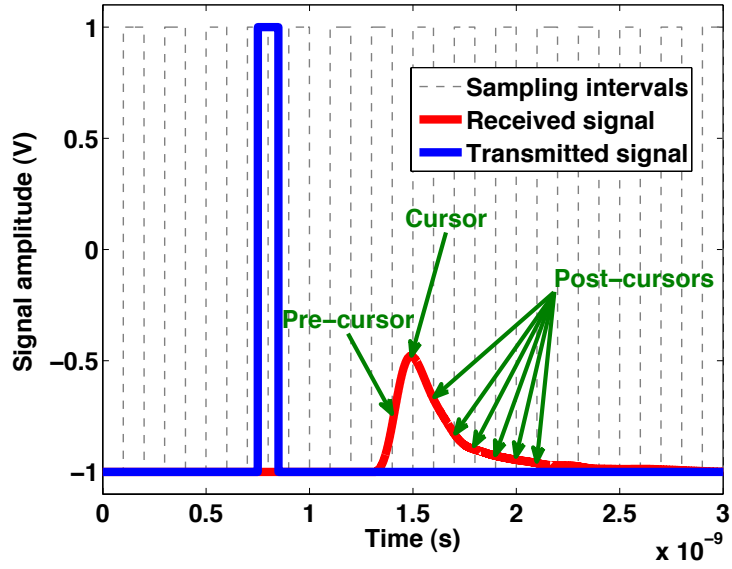
Figure 2.2: Frequency response of a 10 inch CPW FR4 channel.

lem.

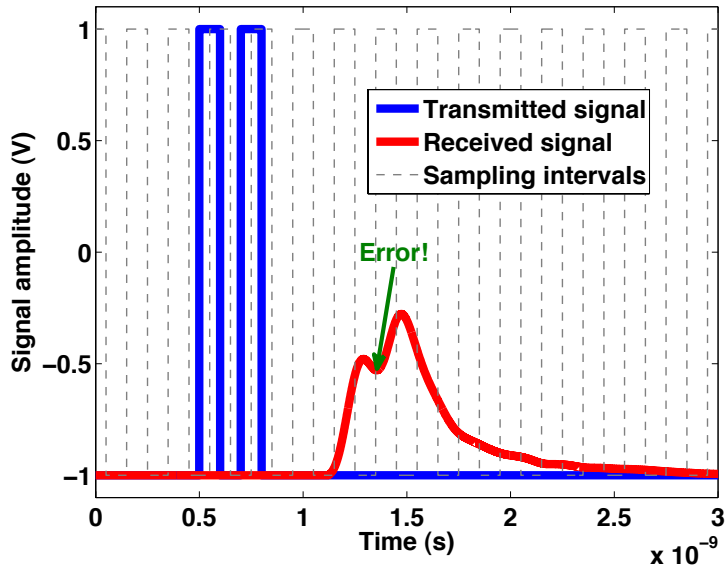
The channel's impulse response provides an intuitive perspective of how data gets distorted by the low-frequency characteristic of channel. To generate such impulse response, we can transmit an isolated '1' which is preceded and succeeded by a group of '0's and observe the output of channel. Figure 2.3a illustrates this concept. If we sample the impulse response of channel at each bit interval, the sample with largest amplitude is called *cursor*, and the samples with non-zero values before and after the cursor are called *pre-cursor* and *post-cursor*, respectively [26]. Figure 2.3b shows how ISI shifts the amplitude of the cursor below the decision threshold, and thus bit error results.

The time-domain responses of the channel in Fig. 2.2 to 2Gb/s, and 4Gb/s NRZ data are shown in Fig.2.4. As shown in Fig.2.4b, and Fig.2.4d, the

2.2. Inter-symbol interference



(a)



(b)

Figure 2.3: Simulated impulse response of a band limited FR4 channel using a 0.1ns wide pulse (a), and distortion of the received signal beyond the detectable limits due to ISI (b)

2.2. Inter-symbol interference

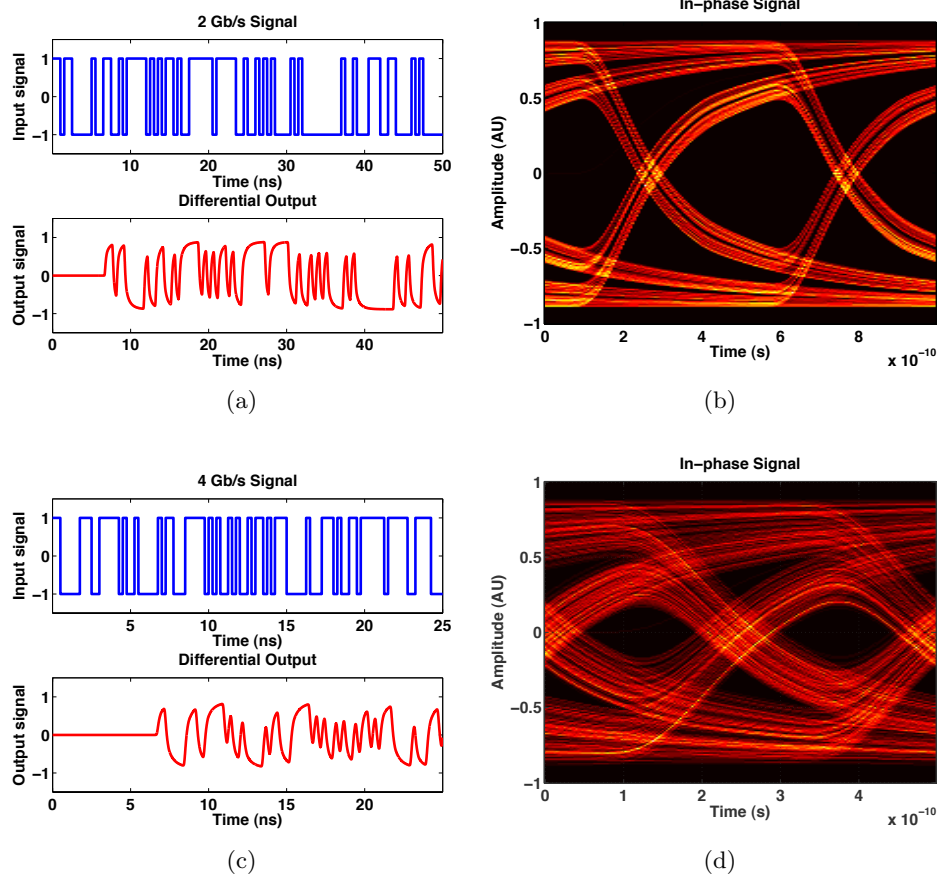


Figure 2.4: Simulated response of the band-limited channel of Fig.2.2 along with the corresponding eye diagrams using 2Gb/s (a-b), and 4Gb/s (c-d) random data patterns.

channel non-idealities result in small vertical eye opening at the receiver side and this problem gets aggravated as data rate increases. This makes the data recovery task more complicated and increases the bit error rate (BER) of the receiver. Low-pass property of channel does not allow the channel's output to properly follow the abrupt changes of transmitted signal waveform. For a lossy channel without reflections, the smallest vertical

eye opening typically occurs when an isolated ‘0’ or an isolated ‘1’ is transmitted (i.e., ...00001000... or ...11110111...). Such cases determine the worst case voltage margin at RX sampler(s), which affects the bit error rate of the link. If the ISI is large enough, it can completely close the data eye and make the detection of the transmitted symbols without equalization impossible. As a result, Different types of equalization are used at both TX and RX to partially cancel ISI.

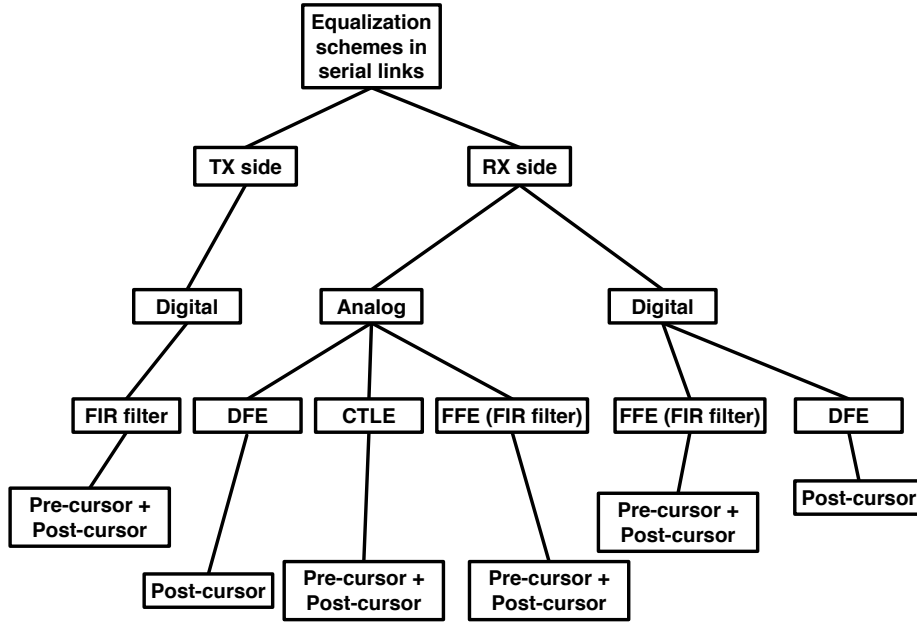


Figure 2.5: Classification of equalizers used in high speed links.

2.3 Channel equalization

As signal distortion due to ISI is inevitable in high speed links, the data should be equalized either at TX, RX, or both TX and RX sides. This

2.3. Channel equalization

provides the subsequent blocks (e.g., clock recovery and data recovery) with an apprehensible signal. Figure 2.5, classifies the equalizers based on domain (analog versus digital), and side (TX versus RX) of implementation.

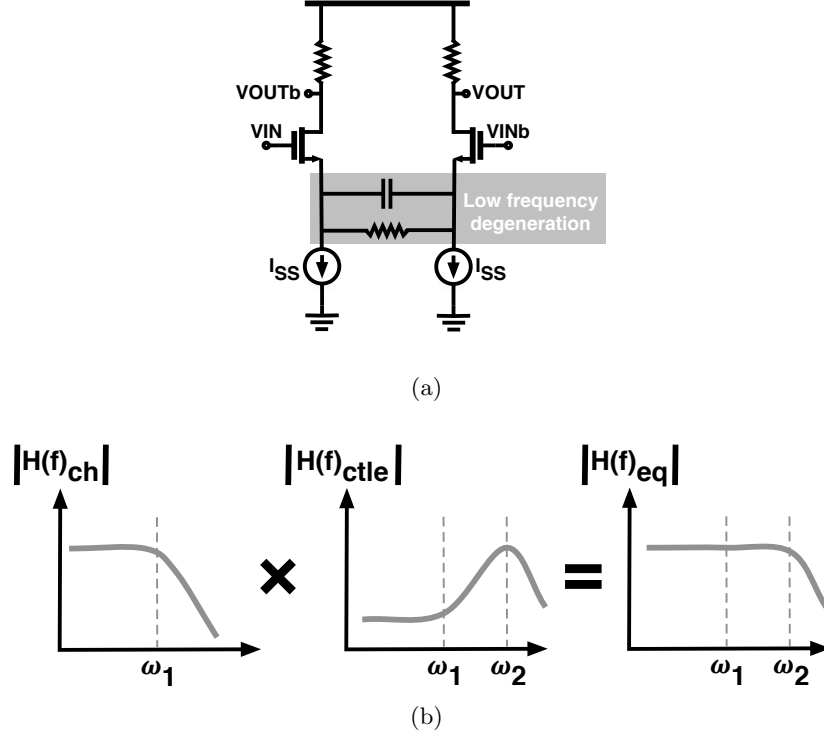


Figure 2.6: Schematic of typical implementation of continues-time linear equalizer (CTLE) (a), and compensation for low-pass characteristic of channel through low-frequency source degeneration (b).

2.3.1 Continues-time linear equalizer

Figure 2.6a shows the schematic of a continuous-time linear equalizer (CTLE) which is commonly used at the front-end of RX to emphasize the high frequency components in the received data, D_{rx} , or equivalently de-emphasize the low frequency components in D_{rx} . In the CTLE of Fig. 2.6a which

2.3. Channel equalization

utilizes resistive loads, low-frequency components in D_{rx} are attenuated through reducing the DC gain of the differential stage using source degeneration. Considering the simple channel in Fig. 2.6b with low pass frequency response and 3-dB bandwidth of ω_1 , the zero in the CTLE frequency response, $|H(f)_{ctle}|$, should be ideally located at ω_1 to flatten the overall equalized frequency response, $|H(f)_{eq}|$. Note that as $|H(f)_{ctle}|$ can not sustain an increasing gain till infinite frequency, inevitably the magnitude response will fall at ω_2 , where $|H(f)_{ctle}|$ has two poles. To provide a satisfactory equalization at a reasonable power consumption, ω_2 should be set such that

$$\frac{1}{2} \times DR < \omega_2 < \frac{2}{3} \times DR \quad (2.3)$$

where DR is the data rate in Gb/s [24].

2.3.2 FIR filter

Figure 2.7a shows the block diagram of a finite impulse response (FIR) filter as used in TX to pre-emphasis the high frequency contents of transmitted data, D_{tx} . Flip flops (FFs) are used to delay the signal for one clock cycle or equivalently 1 unit interval (UI). Based on channel impulse response, a weight, W_i is applied to the digital data through an operational transconductance amplifier (OTA) stage. The overall combination of the FF and OTA form a filter tap. The taps which precede and succeed the main tap are called anti-causal taps and causal taps, respectively. Anti-causal taps (i.e. W_{-1}) are used to cancel pre-cursor components in channel impulse re-

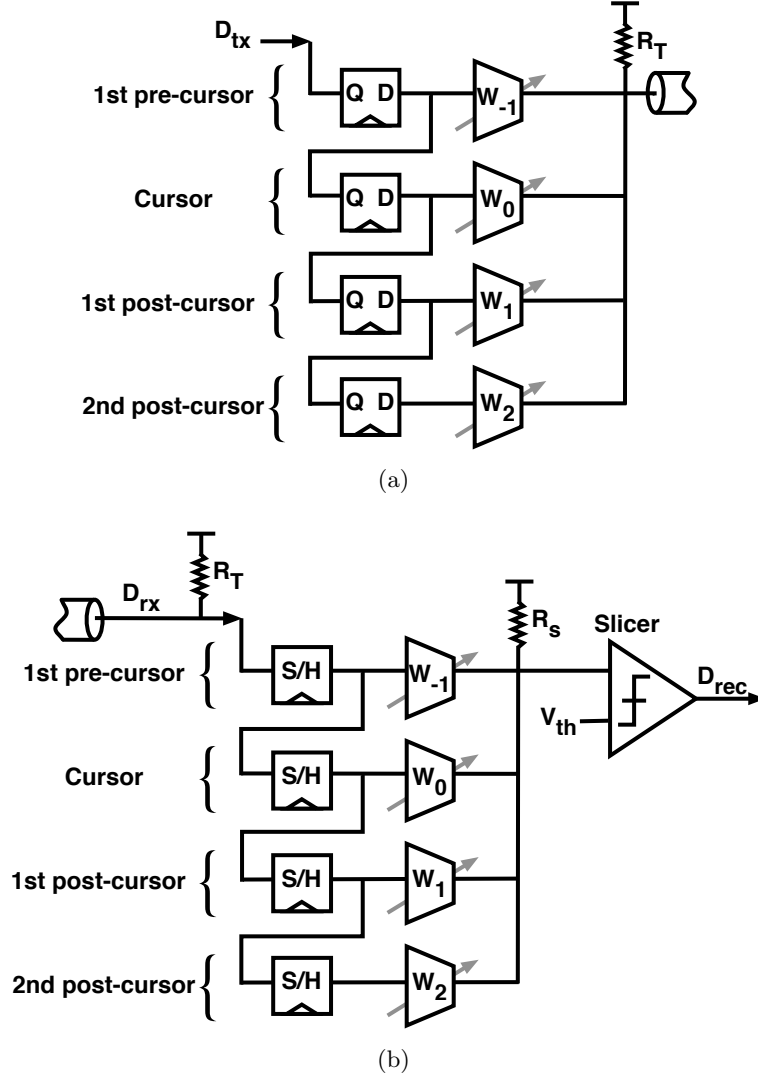


Figure 2.7: Block diagram of FIR filter as used in TX (a), and schematic of FIR filter as used in RX (b).

sponse; likewise, causal taps are used to cancel the post-cursor components. Although such filters are simple and inherently fast, their major drawback is degradation of signal-to-noise ratio (SNR) at the TX node due to the

limited swing of output stage. In other words, as in CTLE, high frequency components are emphasized at the price of de-emphasizing low-frequency components, which translates to a lower SNR.

Figure 2.7b shows the potential implementation of an FIR filter in analog domain at RX. Although feasible, FIR filters are rarely implemented in analog domain. One significant challenge in such implementation is noise enhancement in the sample and hold (S/H) chain. However, in DSP-based RX, where equalization is performed on the digitized data, FIR filters are commonly used before a decision feedback equalizer (DFE) to cancel pre-cursor taps of channel. Such FIR filters are commonly referred to as a feed-forward equalizer (FFE) [27].

2.4 Decision feedback equalization

Decision feedback equalizers (DFEs) use the knowledge of previously recovered bits to estimate their effect on the current bit, and subtract the estimated distortion value from the received signal. DFE is a key component of high speed³ wireline receivers, and plays a vital role in the emerging 40 to 100 Gb/s links [28]. In channels with a long impulse response tail, canceling the post-cursor inter-symbol interference using a DFE is a preferred choice over a feed-forward equalizer. Such design choice is based on the fact that unlike FFEs, DFEs do not enhance the noise, or deliberately attenuate high-frequency components of the received signal [29]. However, DFEs suffer from stringent requirement for timing closure in the feedback loop within 1

³In this manuscript we refer to data rates > 10 Gb/s as “high speed”.

unit interval. Depending on the speed and the amount of necessary post-cursor ISI cancellation, the power consumption of the DFE block may not fit within the receiver's power budget [30]. Furthermore, given a certain technology, the implementation of DFE may not be feasible due to capacitive self-loading of devices. In this chapter, we propose a DFE implementation technique which relaxes the trade-off between the power consumption, the speed, and the amount of post-cursor ISI needed to be canceled.

2.4.1 Conventional analog DFEs

To make a decision, conventional analog DFEs (ADFEs) utilize a static slicing threshold equal to the voltage at the mid-point of the equalized data eye. Figure 2.8a shows a 3-tap ADFE where using DAC1, the ISI is subtracted from the distorted received signal at the summing node. The result is compared with the static slicing threshold voltage V_s to recover the data. Lets consider the channel of Fig. 2.9, whose transfer function is

$$H_{ch}(z) = h_0 + h_1z^{-1} + h_2z^{-2} + h_3z^{-3} \quad (2.4)$$

In addition to the cursor h_0 , the channel impulse response has three post-cursor components, i.e., h_1 to h_3 . Thus, the total amount of post-cursor ISI with respect to cursor can be written as

$$W_{DFE} = \frac{|h_1| + |h_2| + |h_3|}{|h_0|} \quad (2.5)$$

To force all post-cursor components to zero, the transconductance of the

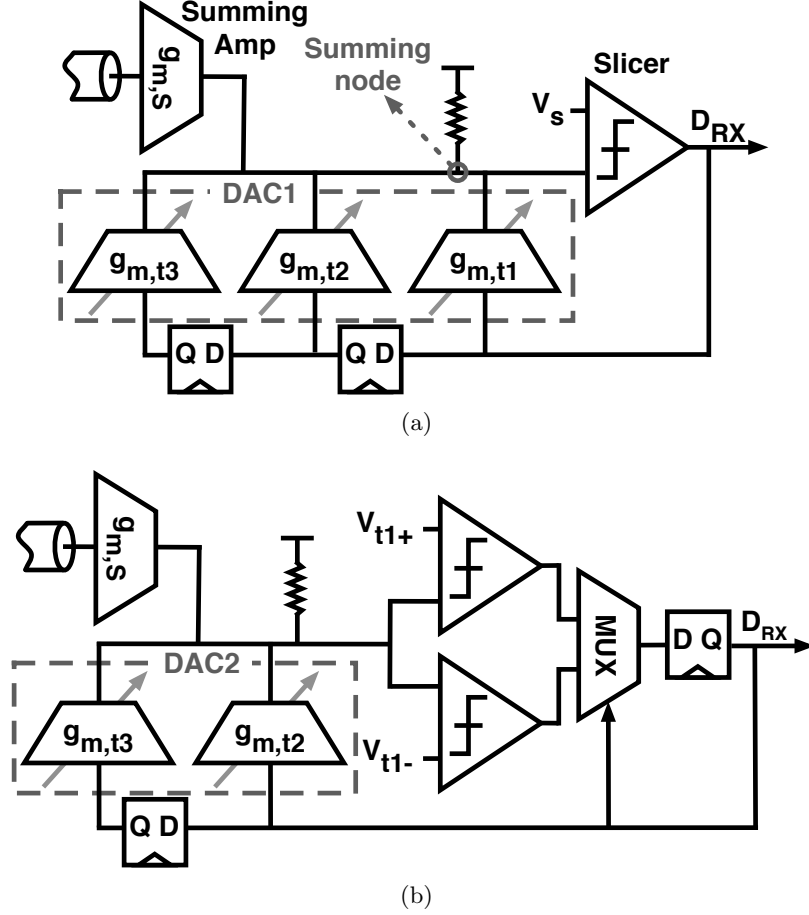


Figure 2.8: A 3-tap ADFE (a), and a (1+2)-tap LUDFE, i.e., the first tap is unrolled (b). Although the signals and circuit blocks are fully differential, for simplicity, they are shown as single ended.

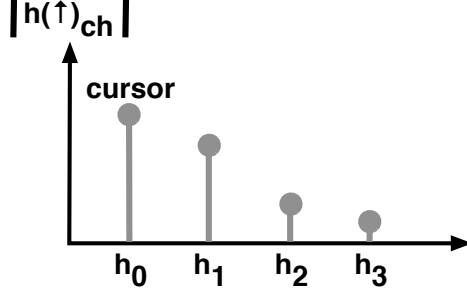


Figure 2.9: Illustration of the impulse response of a $h_0 + h_1z^{-1} + h_2z^{-2} + h_3z^{-3}$ channel.

summing amplifier, $g_{m,S}$, and total transconductance of the taps in DAC1, $g_{m,DAC1}$, have to be chosen such that:

$$g_{m,S} = \frac{A_1\omega_{bw1}C_L}{1 - \underbrace{\left(\frac{A_1\omega_{bw1}}{\omega_T/\gamma}\right)}_{\text{term } \alpha} \underbrace{\left(1 + \frac{2W_{DFE}V_{cursor}}{v_{od,t}}\right)}_{\text{term } \beta}} \quad (2.6)$$

$$g_{m,DAC1} = \frac{2g_{m,S}W_{DFE}V_{cursor}}{v_{od,t}} \quad (2.7)$$

where $A_1\omega_{bw1}$, C_L , ω_T , γ , $v_{od,t}$, and V_{cursor} are the gain-bandwidth required to meet the timing closure at the summing node, input capacitance of the slicer, the unity-gain frequency of the input devices in the summing amplifier, c_{dd}/c_{gg} (i.e., C_{drain}/C_{gate}) of input devices, overdrive voltage of the tap devices, and the amplitude of the cursor, respectively. Allocating $m\tau$ (m times the time constant of the summing node) for settling, the required bandwidth is $\omega_{bw1} = m/(1UI - t_{del1})$, where t_{del1} is the worst-case data

2.5. Proposed adaptive slicing technique

propagation delay among taps (usually is the highest for the first tap). In Eq. 2.6, *term* α is due to the self loading of the summing amplifier and *term* β introduces the effect of W_{DFE} on self loading of the summing amplifier. The total transconductance required for timing closure $g_{m,total}$ is equal to $g_{m,DAC1} + g_{m,S}$.

2.4.2 Loop-unrolled DFE

Compared to the shift-register flip-flops in Fig. 2.8a, the comparator has a higher propagation delay as it should resolve a small signal difference to the full swing. Thus, the overall timing margin for the entire loop is limited by the small timing margin of the first tap. One well-known remedy is the loop-unrolled DFE (LUDFE) architecture shown in Fig. 2.8b, in which the first tap is taken out of the critical path by having two comparators in parallel. However, this is achieved at the price of the added multiplexer (MUX) delay and the doubled C_L , which in turn may increase the overall required $A_1\omega_{bw1}$ at the summing node [31]. Hence, considering channels with different first post-cursor h_1 (or equivalently the weight of first DFE tap, t_1), this approach does not necessarily decrease DFE's power penalty or enhance the timing margin. For the LUDFE shown in Fig. 2.8b, the term W_{DFE} in Eqs. 2.6 and 2.7 shall be replaced by $W_{DFE} - (|h_1/h_0|)$.

2.5 Proposed adaptive slicing technique

The proposed adaptive slicer DFE (ASDFE) technique is based on [32] and is shown in Fig. 2.10a. Here, instead of subtracting the post-cursor ISI from

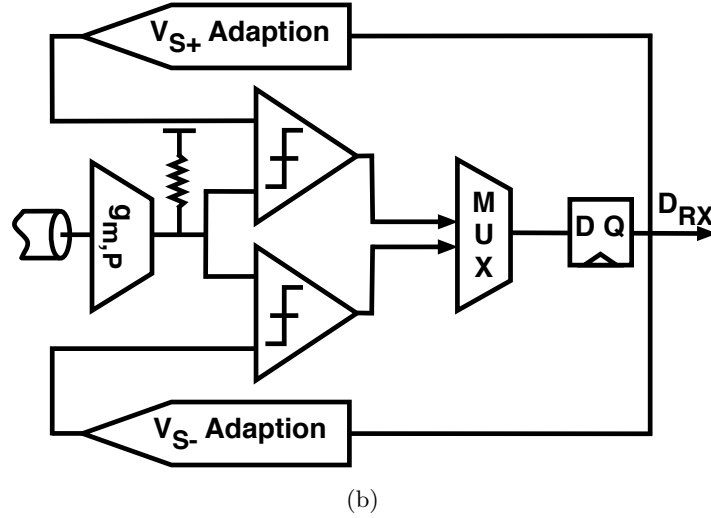
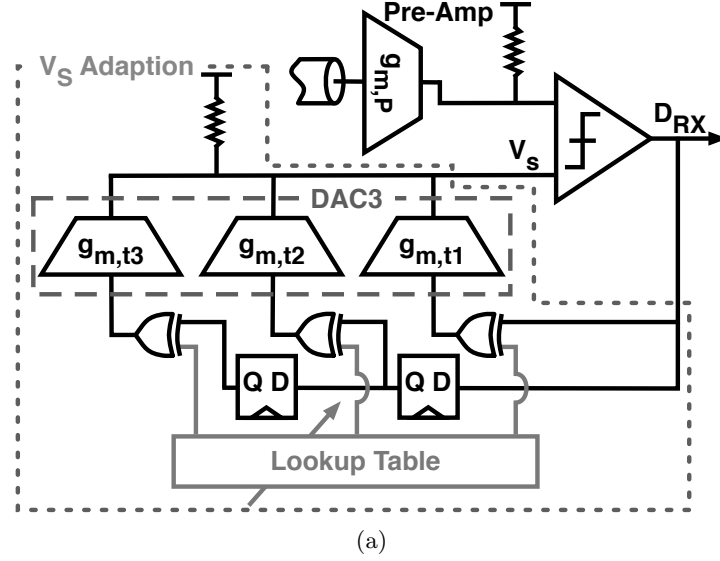


Figure 2.10: ASDFE technique (a). The gray lines indicate low-speed signals. SASDFE architecture (b).

the signal itself and performing a bit decision using a static threshold, the slicer (comparator) threshold V_s is adaptively adjusted in each UI and the distorted signal coming from the channel is left unaltered. Based on the

2.5. Proposed adaptive slicing technique

knowledge of channel's impulse response and the previously recovered bits, the appropriate threshold is achieved through deviating V_s from the average of the worst-case '1' and the worst-case '0' voltages. Unlike ADFE and LUDFE that most of the capacitive loading is on the timing-critical summing node, the proposed approach allows for distributing the capacitance between the inputs of the slicer. In this technique, the need for a fast-settling summing amplifier is obviated as signal summation is replaced by threshold adaption. In ASDFE, a pre-amplifier having transconductance of $g_{m,P}$ is used to drive the input capacitance of the slicer C_L . For $g_{m,P}$, and total transconductance of taps in DAC3, $g_{m,DAC3}$, we can write

$$g_{m,P} = \frac{A_1(m/1UI)C_L}{1 - \left(\frac{A_1(m/1UI)}{\omega_T/\gamma}\right)} \quad (2.8)$$

$$g_{m,DAC3} = \frac{W_{DFE}A_1\omega_{bw3}C_L}{1 - \left(\frac{W_{DFE}A_1\omega_{bw3}}{\omega_T/\gamma}\right)} \quad (2.9)$$

where terms with subscripts '1' and '3' refer to ADFE and ASDFE architectures, respectively. In Eq. 2.9 the required bandwidth to meet the timing closure, ω_{bw3} , is slightly more than ω_{bw1} due to additional delay of an XOR gate, i.e., $t_{del3} > t_{del1}$ (Fig. 2.10a).

Figure 2.10b shows the proposed speculative adaptive slicer DFE (SAS-DFE) architecture which is based on the two-way parallel implementation of the ASDFE technique. Here, in addition to adapting the comparator threshold based on the previously recovered bits as in ASDFE, the threshold of each of the two comparators is affected by the speculation based on

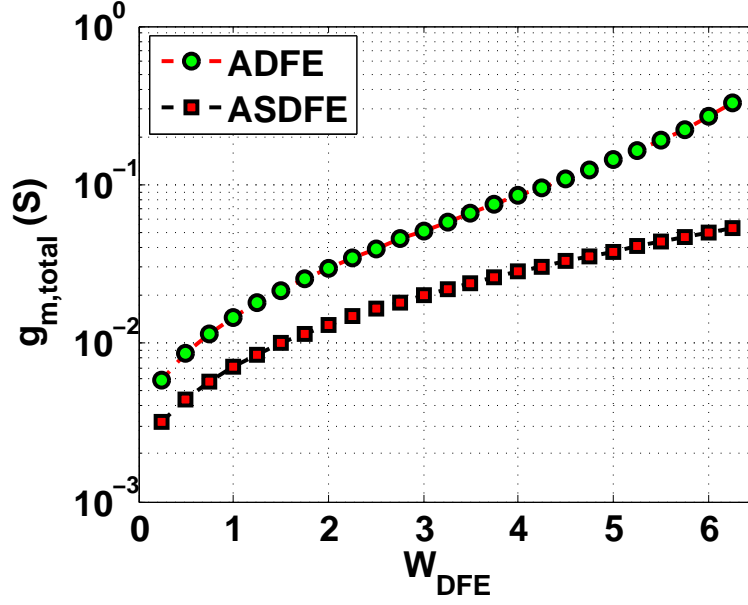
2.6. Comparison of power-equalization efficiency

the two possible bit outcomes ‘0’ or ‘1’. The threshold V_{s+} is based on a speculated value of ‘1’ for the cursor. In the same manner, threshold V_{s-} is adjusted based on a speculated cursor value of ‘0’. The main motivation for having two ASDFE loops in parallel is to enable signal digitization, which is required by clock recovery (CR) algorithms such as Mueller-Muller [33]. For digitization, V_{s+} and V_{s-} are set below and above the corresponding speculated cursor voltage levels, respectively. While holding the sampled signal, the two thresholds are swept in opposite directions in consecutive search cycles similar to successive approximation ADC (SAR) [32]. However, unlike the SAR method, the proposed digitization method has a much smaller search domain and hence a significant speed advantage. Considering k number of search cycles, Eq. 2.8 can be modified for SASDFE architecture by using $(k \times m)/1UI$, as the pre-amplifier should settle before the first digitization cycle. Additionally, the capacitive load C_L is doubled. Finally, in Eq. 2.9 we have $\omega_{bw4} = (k \times m)/(1UI - t_{del4})$, where the term with subscript ‘4’ refers to SASDFE. Note that the parallelism in SASDFE of Fig. 2.10b is equivalent to 1-tap loop unrolling; therefore, we typically have $t_{del4} < t_{del3}$.

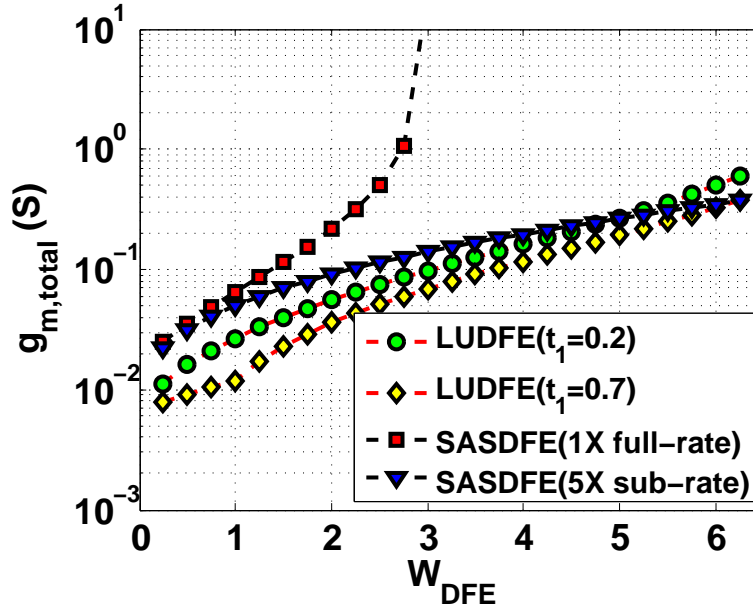
2.6 Comparison of power-equalization efficiency

Figure 2.11a compares the $g_{m,total}/W_{DFE}$ trade-off between ADFE and ASDFE. If we denote v^* as

$$v^* = \frac{2I_d}{g_m}, \quad (2.10)$$



(a)



(b)

Figure 2.11: Comparison of $g_{m,total}/W_{DFE}$ trade-off between ADFE and ASDFE (a), and between LUDFE and SASDFE (b).

2.6. Comparison of power-equalization efficiency

then, considering that during the design process v^* is typically chosen to be a fixed value ⁴, we would have

$$P_{total} \propto g_{m,total} \quad (2.11)$$

where P_{total} is the total power consumption. Therefore, while the vertical axis is in units of Siemens, it is also generally proportional to the overall power consumption.

In ADFE, the power penalty due to W_{DFE} increases considerably if the amount of post-cursor ISI that needs to be canceled is more than the V_{cursor} . Such power penalty can quickly dominate the RX power consumption. On the other hand, the ASDFE approach shows a more relaxed trade-off. Figure 2.11b shows the same comparison between LUDFE and SASDFE, both utilizing two slicers in parallel. The LUDFE graph is plotted for the two cases that the unrolled tap t_1 (or equivalently the first post-cursor component h_1) has values equal to 0.2 and 0.7 with respect to the cursor. Such $|h_1/h_0|$ ratios are the prevalent extremes among serial links [35]. The SASDFE graphs are plotted for full-rate, and 5-way time-interleaved sub-rate architectures, where in both cases we have $k = 5$. As W_{DFE} increases, achieving timing closure in full-rate SASDFE quickly becomes power-inefficient and ultimately infeasible. However, the sub-rate SASDFE provides simultaneous equalization, data recovery and digitization of sampled signal with a power dissipation comparable to that of LUDFE at relatively high values of W_{DFE} .

⁴In high-speed analog circuits typically we choose $v^* \approx 0.2 V$ [34].

2.7 Chapter summary

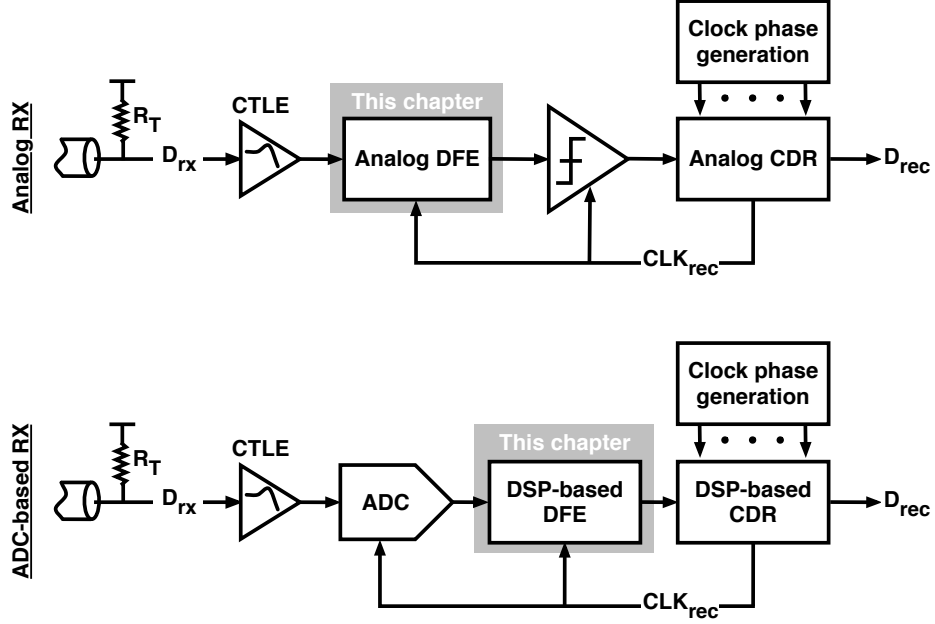


Figure 2.12: Graphical illustration of the digital and analog DFE blocks addressed in this chapter, and their interaction with other RX blocks.

With the emerging high-speed wireline data rates, canceling higher amounts of post-cursor ISI would be a necessity. As noted on Fig. 2.12, this chapter investigates the power penalty of canceling a certain amount of post-cursor ISI taps (W_{DFE}) using DFE. From Fig. 2.12 it can be seen that the equalized signal is used for recovering the data and aligning the sampling edge of clock to the middle of data eye. While the analog and digital CDR architectures proposed in Chapters 5 and 6 do not include a DFE⁵, it should be noted that an under-equalized data eye can severely degrade the perfor-

⁵For the purpose of measurements, high-frequency cables and probes are used to provide interface to the chip

mance of the CDR; this is further discussed in Chapter 7. In this Chapter, the sub-rate SASDFE architecture was proposed, which facilitates canceling significant amount of post-cursor ISI and simultaneous digitization of sampled data, while avoiding unreasonable power dissipation at RX front-end. In particular, in high-loss channels that ADFE or LUDFE based RXs may be impracticable due to excessive power consumption, ASDFE and sub-rate SASDFE designs provide a relaxed power-equalization trade-off. In Chapter 3, we propose a digital RX architecture which builds on the SASDFE.

Chapter 3

Low-power DSP-based RX

While CMOS scaling has been promising to enhance the performance of digital circuits, from an analog perspective, the performance of N-channel and P-channel devices has deteriorated in scaled CMOS technologies [34]. Hence, the trend of moving as much as signal processing tasks as possible from analog domain to digital domain is becoming more and more popular. Following this trend, advanced high-speed serializer/deserializer (SerDes) circuits are becoming more DSP-based to take advantage of improved functionality and flexibility of the digital clock and data recovery (CDR) and equalization [25, 27, 36, 37]. Figure 3.1 shows the simplified block-diagram of a DSP-based (ADC-based) wireline RX. Usually, a gain block precedes the ADC to adjust the swing of received signal based on the input range of ADC. Additionally, as explained in Chapter 2, the gain stage may act as CTLE to provide high-frequency peaking to partially compensate for ISI. The digitized signal provided by ADC is processed by succeeding DSP-based equalization and clock recovery blocks.

As wireline data rates increase in the multi-Gb/s range in the emerging standards, e.g., IEEE 802.3ba Ethernet standard, sophisticated feed-forward equalization and decision feedback equalization are needed to compensate

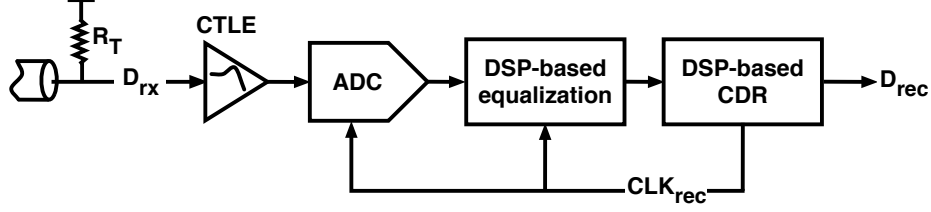


Figure 3.1: Simplified block diagram of an ADC-based RX.

for ISI. Such elaborate equalization translates into tens of FFE and DFE taps, that if implemented in analog domain, result in a large silicon area and a high power consumption beyond what can be afforded in a practical RX. Therefore, the evolution towards a digital architecture seems vital to enhance the power/area scalability, achieve bit error rates (BERs) equal to or better than 10^{-12} under high channel loss [38], and simplify the migration of circuits to more advanced process technologies.

3.1 Quantifying power efficiency in RX

Although promising, the performance merits of DSP-based receivers is confined by metrics such as power consumption, speed, digitization resolution, and the impairments of the front-end ADC [25, 37]. Among these issues, the high power consumption of an ADC operating beyond 10 GS/s is a prohibiting factor to integrate one within an RX. Figure 3.2 shows⁶ the trade-off between power consumption and sampling frequency, F_s , of different ADC architectures, which have been published in literature from 1997 to 2012. To provide a fair comparison, an FoM is defined for power consumption per

⁶Plotted based on data from [39].

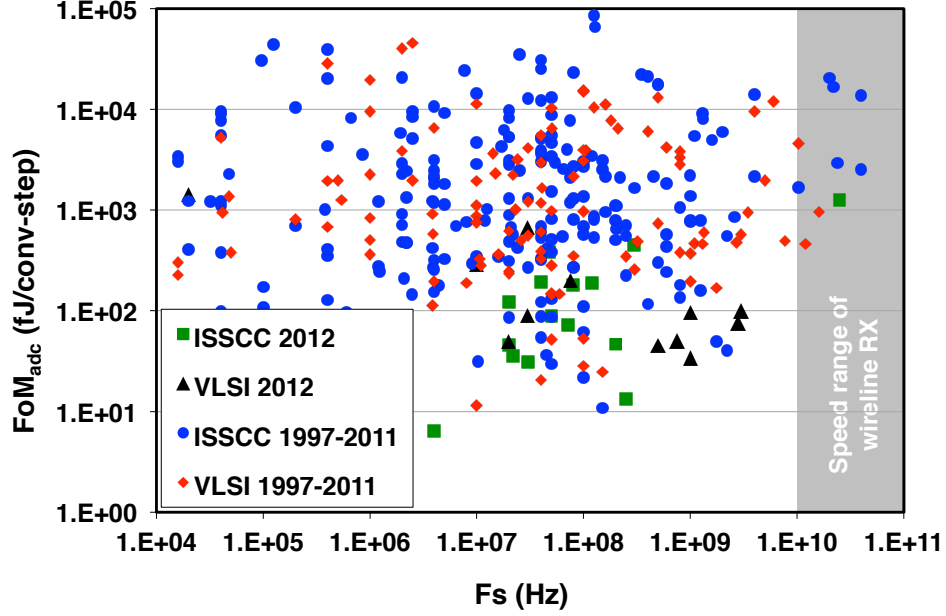


Figure 3.2: Power consumption versus sampling frequency for ADC's published in literature from 1997 to 2012.

conversion step and is defined as follows

$$FoM_{adc} = \frac{P_{adc}}{2^n \times F_s} \quad (\text{fJ/conversion step}) \quad (3.1)$$

where n is the digitization resolution. Based on Fig. 3.2, the total power consumption, P_{adc} , of a 5-bit 10 GS/s ADC which samples the 10 Gb/s received data, D_{rx} , once every UI (i.e., baud-rate sampling), is given by

$$P_{adc} > 2^5 \times 10 \text{ (GHz)} \times 500 \text{ (fJ/conversion step)} = 160 \text{ (mW)} \quad (3.2)$$

3.2. ADC performance requirements

To realize the feasibility of using such ADC in the RX, we use a commonly used FoM for power efficiency of RX, which is given by

$$FoM_{RX} = \frac{P_{RX}}{DR} = \frac{P_{ctle} + P_{adc} + P_{eq} + P_{cdr}}{DR} \quad (\text{mW/Gb/s}) \quad (3.3)$$

where DR is the data rate, and P_{RX} , P_{ctle} , P_{eq} , P_{cdr} are the power consumptions of RX, CTLE, FFE/DFE, and CDR. Therefore, the P_{adc} of 160 mW given in Eq. 3.2, results in $FoM_{RX} > 16$ mW/Gb/s. While such power consumption can be tolerated in high-speed optical TX-RX pairs (Fig. 1.4b), it is not a viable option for chip-to chip communication where an array of TX-RX pairs is used (Fig. 1.4a).

Recently published work [40, 41] use interpolating-flash and pipeline ADC topologies for the front-end ADC to decrease the number of comparators from the 2^n regime in full-flash n -bit ADCs [27, 42] to 17 [40] and 6 [41] comparators per sub-ADC for 5 bits of resolution, respectively. This is achieved at the price of limiting the speed of each sub-ADC to 2.5 GS/s [40] and 1.2 GS/s [41]. In this Chapter, we propose a hardware efficient low-power RX architecture which utilizes the SASDFE introduced in Chapter 2.

3.2 ADC performance requirements

The ADC topology and its digitization resolution depend on the speed, power, and BER requirements of RX. For multi-Gb/s receivers, usually flash topology is the feasible choice [27, 37, 42]. However, high power consump-

3.2. ADC performance requirements

tion and capacitive loading of a flash ADC make its use in high-speed digital RX, and the move from conventional binary RX to ADC-based RX, debatable [36]. Recently, using SAR topology, promising performance has been achieved at speeds up to 24 GS/s [43] and 40 GS/s [44]. Nevertheless, such ADCs do not necessarily consume less power than a full-flash ADC [45]. As the maximum conversion rate of a single SAR ADC is still less than 100 MS/s [46], it should be highly interleaved (i.e., $160\times$ in [43]) to reach sampling rates beyond 10 GS/s. Such immense level of interleaving results in high area overhead due to peripheral circuitry, and an elaborate calibration mechanism is needed to cancel the sub-ADC non-idealities to avoid pattern-noise in ADC array [47]. In our design, by using the proposed speculative digitization technique in the SAR ADC, we have limited the interleaving factor of the ADC to 5 for a 10 GS/s speed, in 65 nm CMOS. To determine the sampling frequency of the ADC, a trade-off should be made between P_{adc} and the amount of information provided to the clock recovery algorithm (i.e., more information is extracted from D_{rx} in an over-sampling clock recovery scheme) [40]. In this work, as in [27], the overall ADC sampling and digitization rate is equal to the baud-rate to achieve a data recovery rate equal to the highest clock rate in the system. Hence, Mueller-Muller [33] algorithm would be a candidate for the clock recovery scheme.

There are several factors such as channel characteristics, and the signaling scheme that determine the resolution of ADC. In presence of higher amounts of ISI, the ADC resolution needs to be higher to allow for optimum equalization and clock recovery with the aid of the DSP core. Also, In multi-level

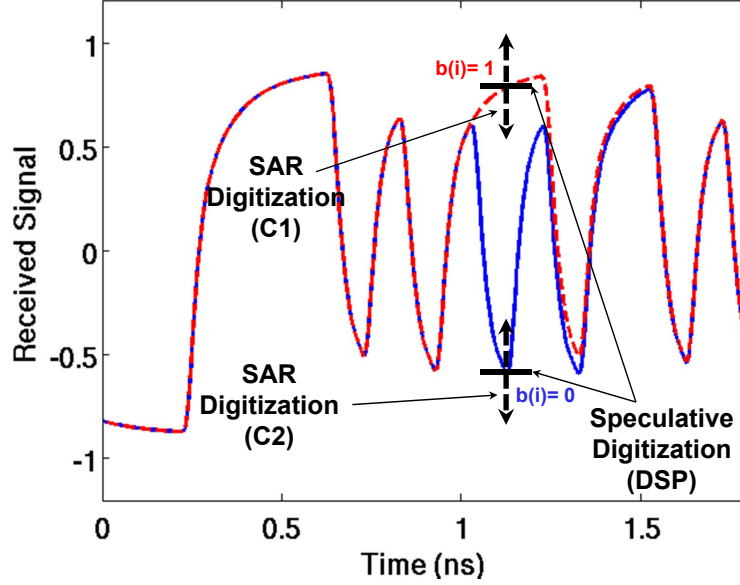


Figure 3.3: Illustration of speculative (solid lines) and SAR digitization steps (dashed lines) for two different data patterns. The two patterns differ in the received bit at time=1.1ns.

signaling schemes, the maximum number of signal levels that can be transmitted is confined by the receiver's ADC resolution [25].

3.3 Speculative/SAR digitization algorithm

Figure 3.3 shows two distorted 10 Gb/s patterns at the RX end of the channel, which only differ in the bit received at time=1.1 ns. Due to the lowpass nature of the channel, the received data can no longer maintain the original voltage levels which are represented by a '0' or a '1'. The high-frequency signal components are filtered out and hence, if a consecutive '0' and '1' pattern is transmitted, the difference in the values of $ab(i)$ (i.e., analog value

3.3. Speculative/SAR digitization algorithm

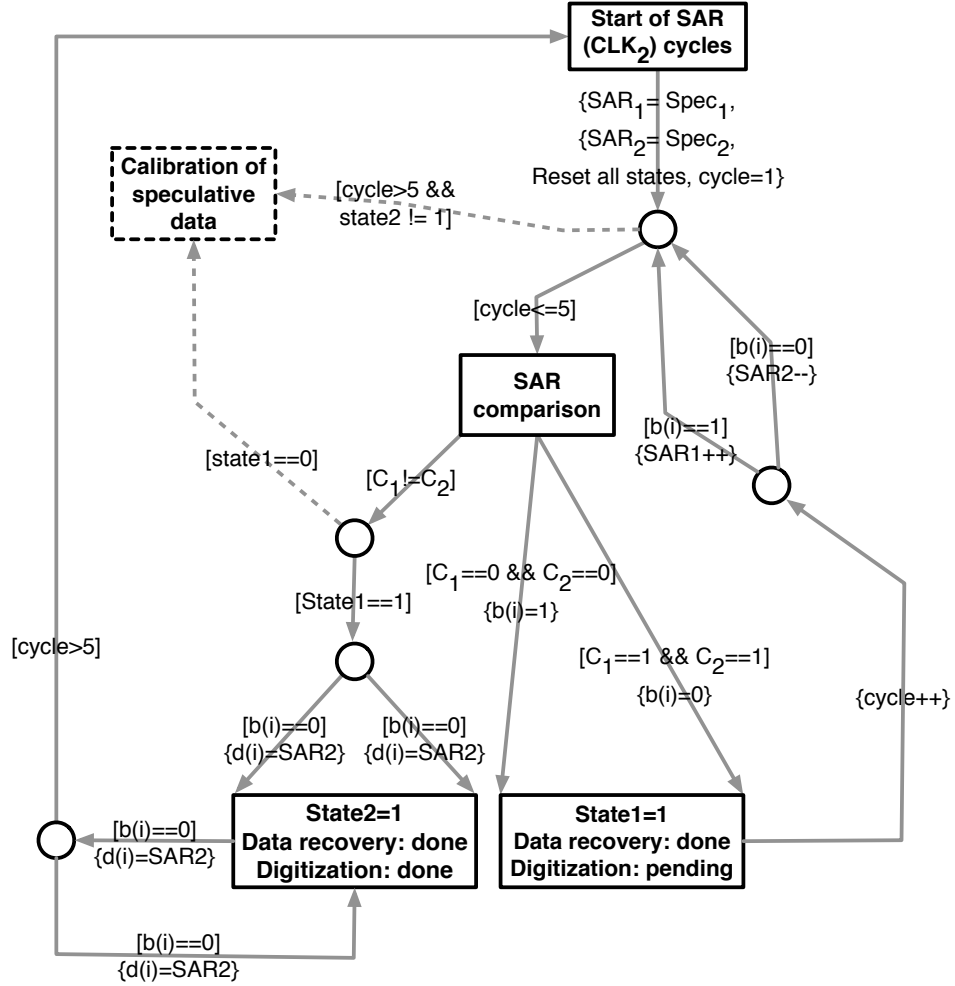


Figure 3.4: The hybrid speculative/SAR digitization algorithm implemented as a finite state machine. `[]` and `{}` indicate IF and DO statements, respectively.

3.3. Speculative/SAR digitization algorithm

of current sampled bit) and $ab(i-1)$ are reduced compared to that at the TX side. The value of $ab(i)$ depends on its preceding bits, as if the channel has a memory [26]. Hence, if a full-flash ADC is used in the AFE, only a few comparators will be decisive in digitizing $ab(i)$ at each sampling cycle of ADC. This is due to the fact that $ab(i)$ will not cross the threshold of the rest of the comparators. Through the hybrid speculative/SAR digitization algorithm of Fig. 3.4, we exploit channel's memory to quickly speculate the digitized value of each received bit based on the 4 previously recovered bits, and then use the conventional SAR digitization cycles to fine-tune the speculated value to yield $d(i)$. As shown in the algorithm of Fig. 3.4, a finite state machine (FSM) uses the speculated value to narrow down the SAR search domain. The SAR step (dashed horizontal lines in Fig. 3.3) takes over the speculative step of the algorithm from the points specified by the two speculated values (solid vertical lines in Fig. 3.3). In this work, due to the fact that there are typically two separated domains based on either transmitting a '1' or a '0', two comparators (C_1 and C_2) are used to perform the SAR cycles for each of the two cases $b(i)=0$ or $b(i)=1$. Breaking the SAR search domain into two separate paths enhances the speed of digitization and data recovery functions. As shown in Figs. 3.3 and 3.4, in the speculative step of the hybrid algorithm, the thresholds of comparators C_1 and C_2 are simultaneously adjusted at the beginning of each SAR sampling cycle. Note that the thresholds of C_1 and C_2 are chosen such that they fall below, and above the speculated analog values for $b(i) = 1$ and $b(i) = 0$, respectively. Interestingly, the proposed speculative/SAR digitization algorithm resembles the SASDFE architecture proposed in Chapter 2. Therefore, as explained in the

3.3. Speculative/SAR digitization algorithm

next Section, in the proposed hardware implementation, we merge the digitization and DFE loops to achieve hardware efficiency, and systematically reduce the power consumption.

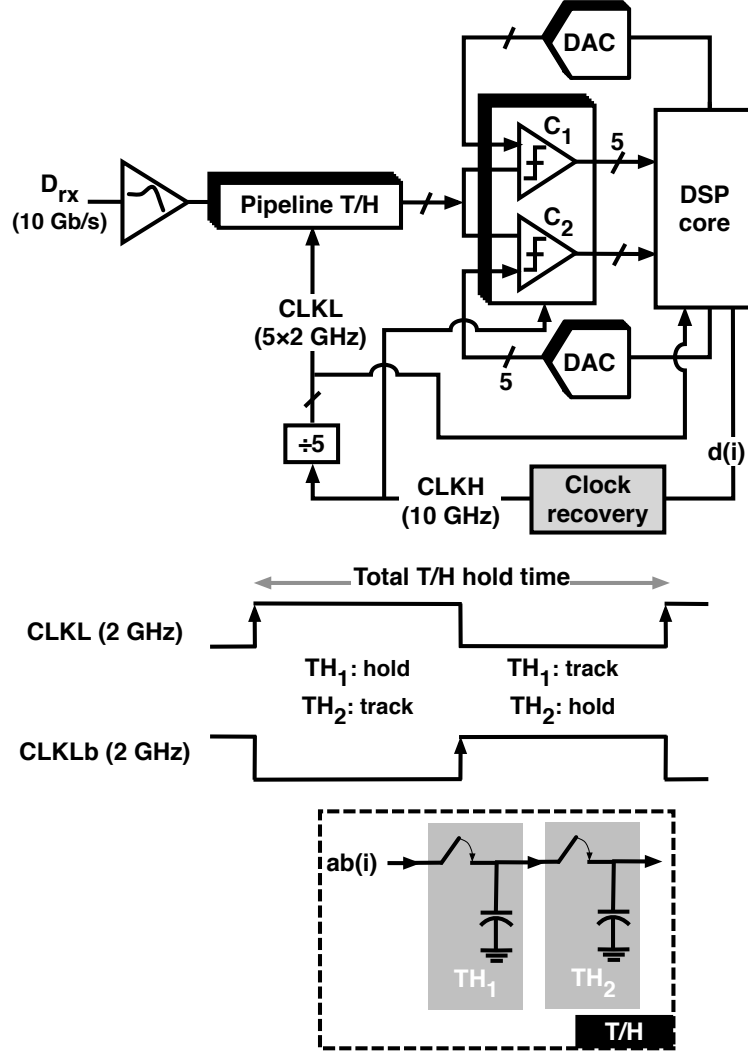


Figure 3.5: Block diagram of the proposed RX. All clocks and analog signals are differential. The clock recovery loop is not integrated into the prototype chip.

3.4 Implementation of the proposed algorithm

Figure 3.5 shows the block diagram of the proposed DSP-based RX, which is a modified version⁷ of the SASDFE architecture proposed in Chapter 2. The RX is implemented as 5 time-interleaved channels. Following the termination and peaking block, the received data from the channel is sampled by a two stage track-and-hold (T/H). As shown in the timing diagram at the bottom of Fig. 3.5, the sampling time of T/H in each channel is controlled by one of the five phases⁸ of the 2 GHz clock $CLKL$. The pipelined arrangement of T/H allows to keep the sampled analog signal $ab(i)$ constant for 5 sampling cycles in C_1 and C_2 comparators, controlled by the 10 GHz clock $CLKH$. As shown in Fig. 3.6, the 5 phases of $CLKL$ are generated by a divide-by-10 function applied to $CLKH$, followed by multiply-by-2 using XOR and XNOR gates. The delay ring is implemented using 10 latches. Unlike the conventional divide-by-5 circuits [48] that yield only three phases with 40% duty cycle, the proposed architecture of Fig. 3.6 achieves 5 phases (i.e. 10 differential phases) with 50% duty cycle. To minimize deterministic jitter in $CLKL$ phases, inputs and outputs of all latches are equally loaded. Additionally, the frequency-doubling XOR and XNOR gates are implemented as shown in the bottom of Fig. 3.6 to yield equal propagation delays.

Following the T/H, the sampled data, $ab(i)$, is equalized, recovered, and ultimately digitized by the SASDFE loop shown in Fig. 3.7. Note that,

⁷While the principal of the operation is the same as Fig. 2.10b, the implementation of Fig. 3.7 is slightly modified to enable timing closure in the feedback loop.

⁸5 phases single-ended, or equivalently 10 phases differential.

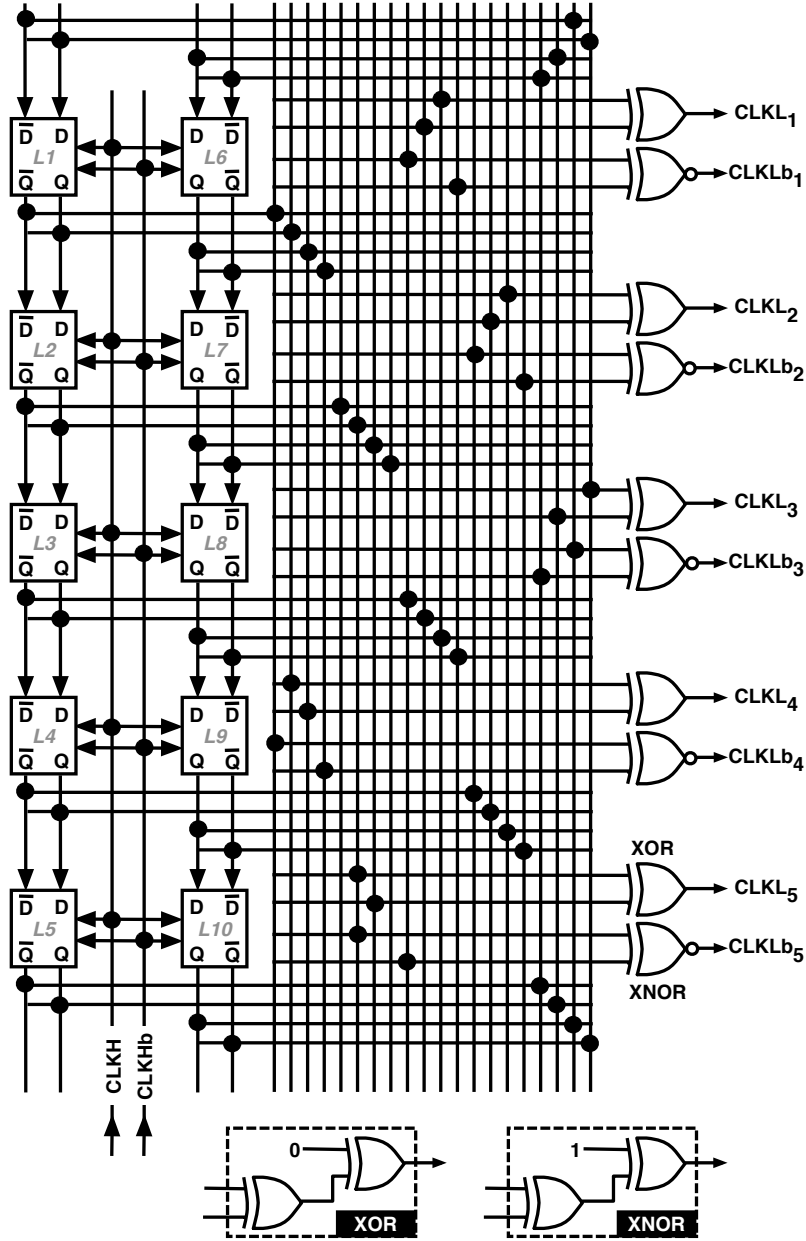


Figure 3.6: Schematic of the divide-by-5 circuit generating five differential phases of the 2 GHz clock $CLKL$, from the 10 GHz clock $CLKH$.

3.4. Implementation of the proposed algorithm

$ab(i)$ is the received bit which has been distorted by the channel and has an analog nature, $d(i)$ is the digitized value of $ab(i)$, and b_{CHX} ⁹ denotes the recovered bit from each channel, which is known to the receiver only after data recovery. Finally, $b(i)$ refers to the most recent recovered bit, in the overall stream of recovered bits from the 5 channels. As shown in Fig. 3.7, each sub-ADC¹⁰ has two comparators whose thresholds are adjusted using digital-to-analog converter (DAC). The comparators have a CML topology [49], and the DACs are implemented with a current-steering architecture [50]. The latches inside the comparators operate in a pipeline manner and are controlled by differential clock $CLKH-CLKHb$ which is recovered from the received data¹¹. As demonstrated in the timing diagram of Fig. 3.8, there are 5 SAR sampling cycles within the 500 ps time that T/H keeps $ab(i)$ constant. Based on characterizing the channel, the thresholds of C_1 and C_2 are set in a manner to recover the data (i.e., b_{CHX}) in the first SAR cycle. The four remaining SAR cycles are performed to find the digitized value of $ab(i)$, $d(i)$, which is in turn used by the DSP-based clock recovery algorithms such as Mueller-Muller [33] to update the phase of $CLKH$. As explained in Chapter 2, adjusting the thresholds of C_1 and C_2 in each SAR cycle of the RX channel shown in Fig. 3.7 is equivalent to implementing a 4-tap DFE. Thus, the demonstrated implementation of the RX architecture is suitable for a channel that $d(i)$ of the most recent sampled bit $ab(i)$ is mostly influenced by the last four bits $b(i-1)$, $b(i-2)$, $b(i-3)$, and

⁹“X” refers to the channel number.

¹⁰the comparator pair C_1 and C_2 in each channel make a sub-ADC, while the top level ADC consists of 5 time-interleaved sub-ADCs.

¹¹Note that the DSP-based clock recovery algorithm has not been integrated into the prototype chip.

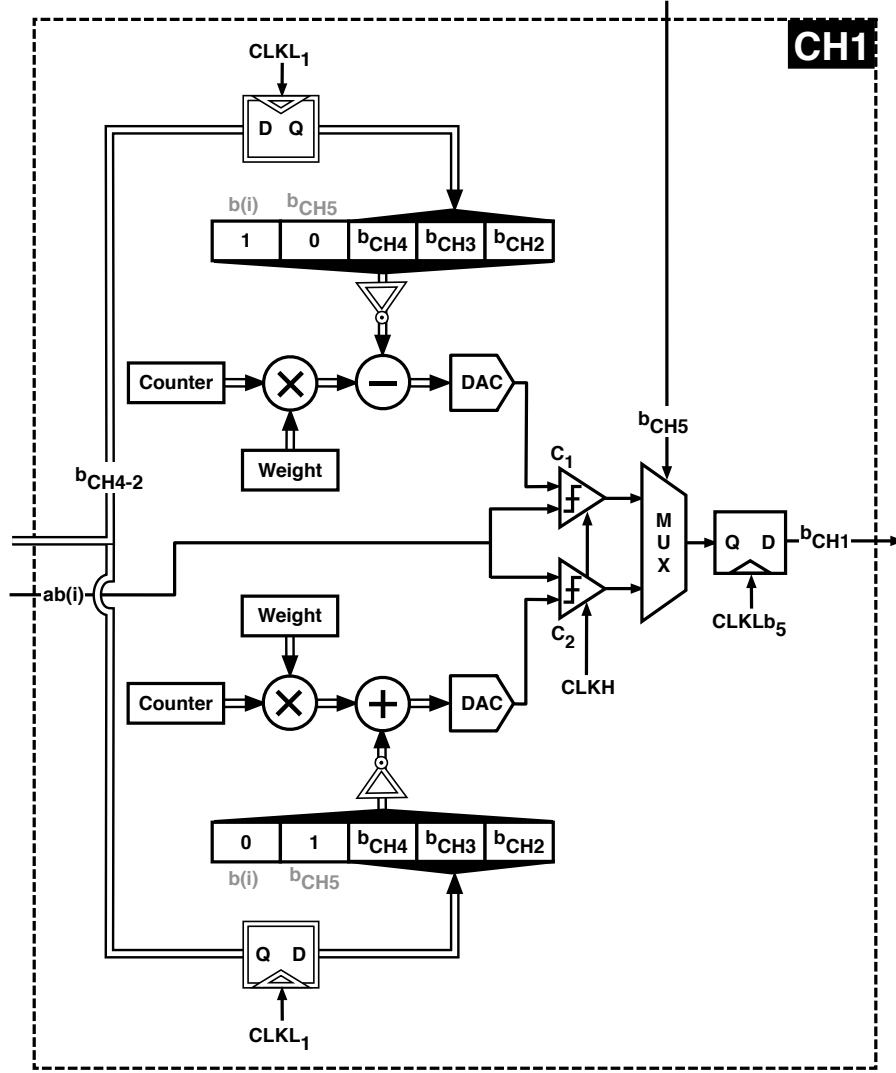


Figure 3.7: Detailed block diagram of each channel in the time interleaved RX architecture of Fig. 3.5.

$b(i - 4)$, which have preceded $b(i)$ (i.e. 4 significant post-cursor ISI taps). The arrangements of the bits in the two 5-bit registers of Fig. 3.7, which is given for channel 1 (i.e., $CH1$), is noteworthy. While both upper and

3.4. Implementation of the proposed algorithm

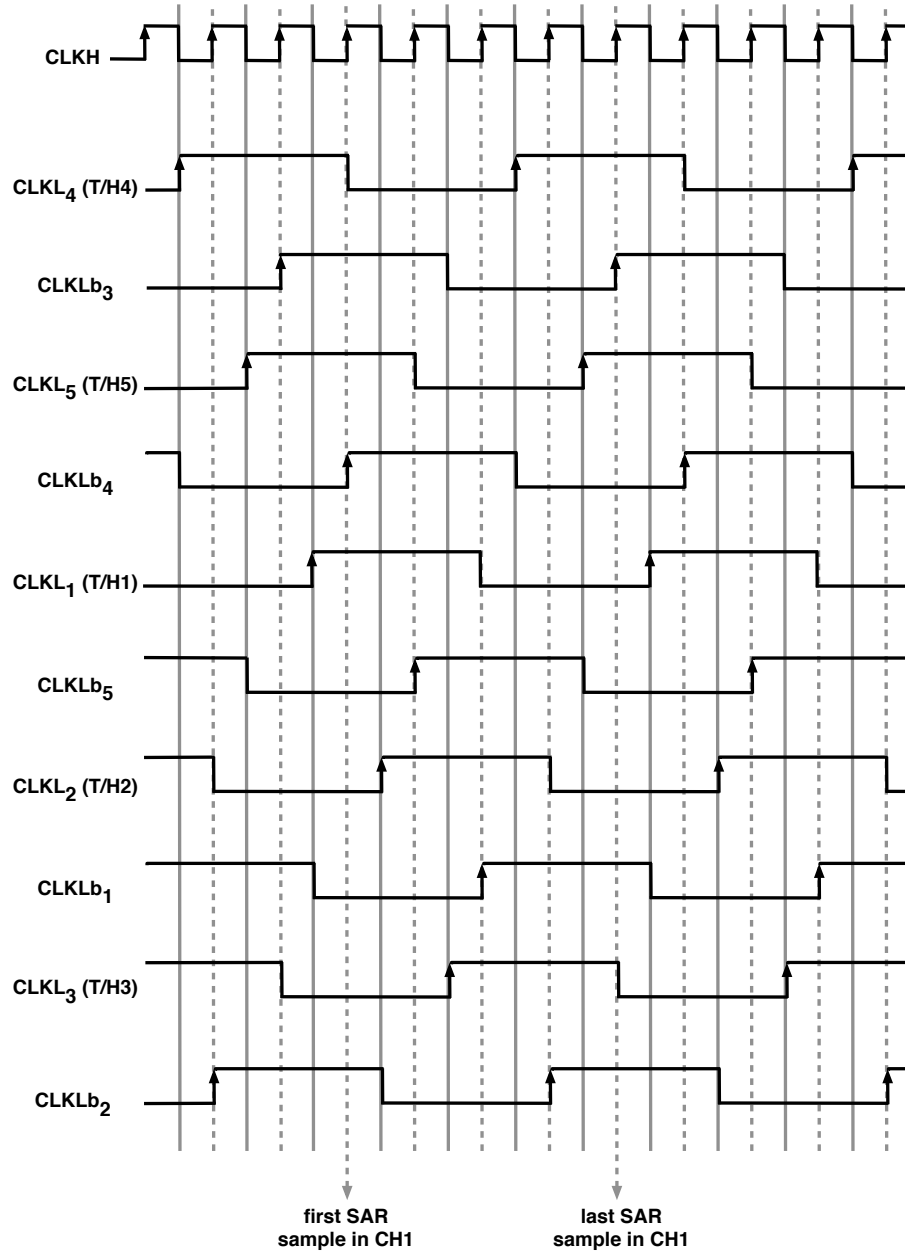


Figure 3.8: Timing diagram of the five time-interleaved channels.

3.4. Implementation of the proposed algorithm

lower registers share the last three bits, the first two bits are different. The first bit from left is the MSB and speculates the value of $b(i)$ (which is yet to be recovered). This differentiates the search domain of C_1 from that of C_2 based on $b(i)$, and helps the SAR search algorithm to converge faster. The second bit from the left speculates the value of the bit recovered by the previous channel, in this case b_{CH5} ¹². The advantage of such speculation is increasing the timing margin of the feedback loop from 100 ps to about 200 ps. Indeed, such speculation resembles a 1-tap loop unrolling in DFE. The last three bits, b_{CH4} to b_{CH2} , account for the three remaining post-cursor ISI taps. In channel $CH1$, data is recovered in the first SAR cycle by selecting one of the MUXed outputs of comparators using b_{CH5} as control signal. It is noteworthy that as in the algorithm of Fig. 3.4, the thresholds of comparators C_1 and C_2 are initially¹³ chosen such that both are either below or above $ab(i)$, at the first SAR cycle outcomes of C_1 and C_2 are equal¹⁴. Then, the curious reader might question the reasoning behind doing a selection through the MUX. The answer is that first, by the time that FF samples the MUX decision, the outcomes of C_1 and C_2 might not be the same anymore due to successive sweeping. Second, the selection allows to choose the decision of the comparator which has the higher voltage margin, and thus achieving a better BER performance. Figure 3.9 shows the top level view of distribution of the recovered bit in each channel, b_{CHX} , to other channels. Note that at the first SAR sampling cycle in each channel, the two 5-bit registers in each channel CHX (see Fig. 3.7) require

¹²Or equivalently $b(i-1)$ when considering all channels.

¹³At the beginning of SAR cycles.

¹⁴which is used for data recovery.

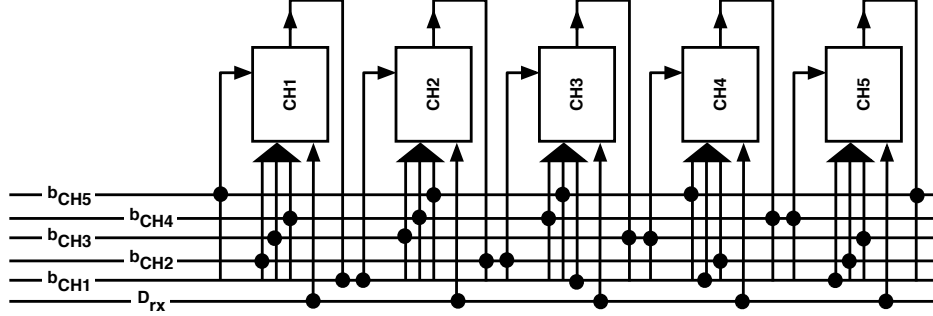
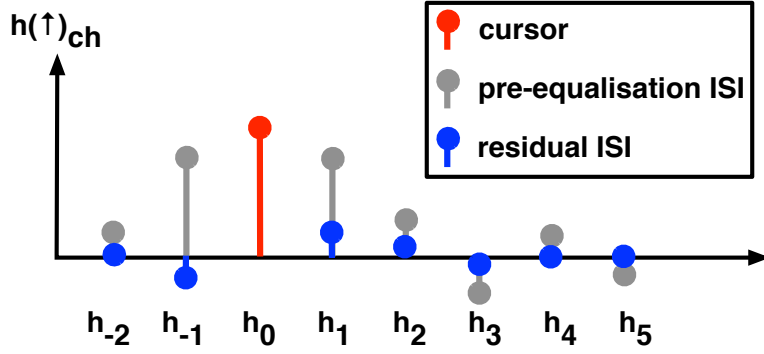


Figure 3.9: A Block diagram of time-interleaved channels, demonstrating the distribution of the recovered data of each channel, b_{CHX} , to other channels.

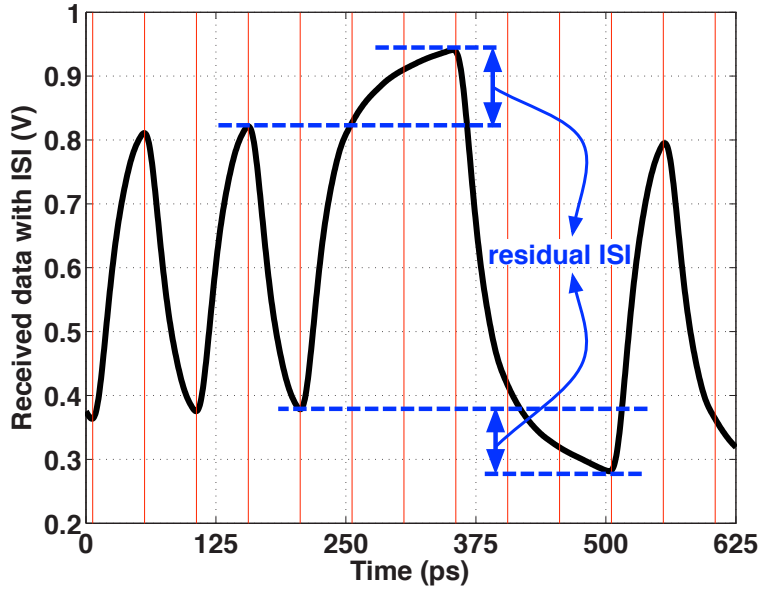
the b_{CHX-2} , b_{CHX-3} , and b_{CHX-4} , while b_{CHX-1} and b_{CHX} (i.e., $b(i)$) are speculated.

3.4.1 Necessity of SAR cycles

Considering the speculative step in digitization algorithm of Fig. 3.4, one may doubt in the necessity of the SAR step, reasoning that if the channel is characterized well enough, the value from the lookup table is indeed the digitized value of the received signal. To elaborate on the need for the SAR step, let's consider the pre-equalization and post-equalization impulse responses of Fig. 3.10a of the channel; where the post-equalization response still has a number of non-zero ISI taps. Therefore, in the post-equalized data, D_{eq} , of Fig. 3.10b, although the '1' and '0' levels are distinguishable from each other, the amplitude of D_{eq} in each UI is modulated by non-zero ISI taps. Such ISI taps are referred to as residual ISI. Even with an adaptive channel equalization, such residual ISI is usually inevitable in RX. As explained in Chapter 2, forcing all post-cursor ISI taps to zero may be



(a)



(b)

Figure 3.10: Residual ISI in channel impulse response after the speculative digitization step (a), and the effect of residual ISI in changing data levels (b).

very power inefficient, or impossible¹⁵.

If the distortion in D_{eq} is not captured at baud-rate, it can mislead the CR algorithm and result in data dependent wandering around the optimal locking point (i.e., where the maximum vertical eye-opening occurs). In contrast, if the CR algorithm receives a precise digital representation of D_{eq} in each UI, it would be able to effectively track data dependent jitter (DDJ).

3.5 Power/resolution trade-off in ADC and DAC

In the proposed ADC, although the number of comparators remain constant as the resolution increases, the resolution of the DAC should increase accordingly. Therefore, at the first glance, it may seem that the power consumption of the DAC offsets the power savings of the proposed ADC, resulting in an overall power consumption comparable to that of a full-flash architecture. However, a closer look at the elements of the high speed comparator and DAC reveals that power-consumption/resolution trade-off in high speed ADCs is substantially more aggressive than in DACs operating at comparable speeds. Our comparators are similar to that in [49] having a preamplifier, two CML latches, and a CML-to-CMOS stage; all of which drawing static current. On the other hand, if we neglect the typically low power consumption of the digital logic, the price that we pay to increase the resolution in a current-steering DAC is confined to that of a differential pair with a tail current source [51]. It is important to mention that while all of the CML blocks inside the comparator are constantly drawing static cur-

¹⁵Due to the self loading of the equalizer taps.

rent, the current sources inside the DAC can be completely switched on/off based on the value of the digital code, further decreasing DAC's power consumption at the price of a slightly compromised conversion speed. With the proposed ADC structure, we are pushing the power toll of increased resolution towards the digital logic (low power consumption) and DAC (fair power consumption), as opposed to the power-hungry comparators of flash ADC.

3.6 Measurement results and comparison

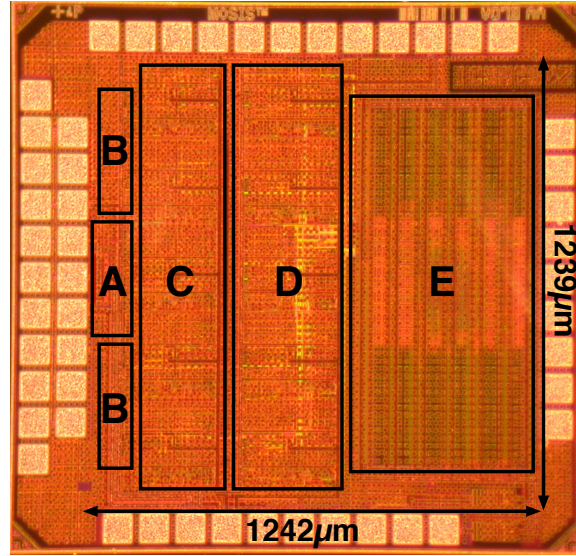
As a proof-of-concept, an RX chip incorporating a 4-tap SASDFE is designed and fabricated in a 65-nm CMOS technology. Figure 6.5a shows the chip layout that occupies 1.242×1.239 mm (excluding the pads). To enable digitization of the sampled signal, and facilitate a baud-rate clock-recovery algorithm, 5 channels of SASDFE are time-interleaved at the RX front-end. This allows for 5 SAR digitization cycles to adjust the speculated level of the distorted received bit and find the digitized signal value. Each channel runs at 10 GS/s which considering the 5 SAR cycles yields an overall digitization and data recovery speed of 2 GS/s and 2 Gb/s, respectively. The 5 parallel channels used in this prototype provide a total data recovery speed of 10 Gb/s. Figure 3.11b shows the measured eye diagram of the full rate recovered data. The eye edges are rounded due to the bandwidth limitation of measurement instrument. The circuit achieves a BER of better than 10^{-12} in response to a $2^7 - 1$ pseudorandom binary sequence (PRBS) from a channel with 19 dB loss at 5 GHz, while consuming overall power of 263

3.6. Measurement results and comparison

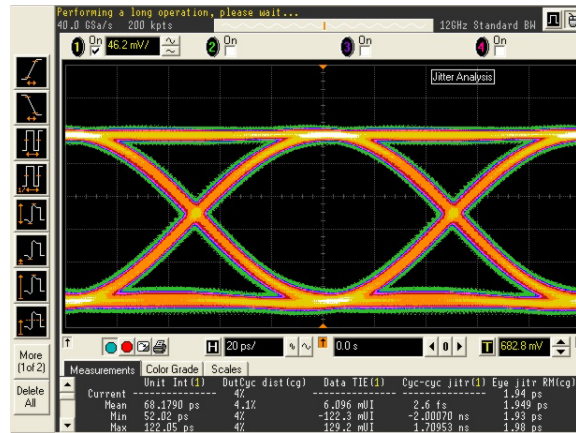
mW (all 5 channels collectively) from a 1 V supply. Table 3.1 compares the characteristics and performance metrics of this work with recently published ADC-based receivers. It can be seen that the proposed RX has a better¹⁶ power efficiency FoM compared to those of [27, 40–42, 52]. Additionally, the systematically reduced comparator count in this work results in a smaller die area for RX, compared to [41, 42, 52].

¹⁶A lower number for power efficiency FoM is considered to be better.

3.6. Measurement results and comparison



(a)



(b)

Figure 3.11: The die micrograph of the prototype implemented in 65-nm CMOS (a); where the blocks A, B, C, D, and E are variable gain amplifier, clock phase generation, comparator array, DAC array, and DSP core, respectively. The measured eye diagram of the recovered 10 Gb/s data (b).

Table 3.1: PERFORMANCE SUMMARY AND COMPARISON

	ISSCC 2007 [27]	JSSC 2008 [42]	JSSC 2009 [41]	ISSCC 2009 [52]	JSSC 2010 [40]	This work [53]
Technology (nm)	65	90	130	65	65	65
Data Rate (Gb/s)	12.5	10	4.8	10.31	5	10
Power (mW)	330	4500	300	1200	178	263
mW/(Gb/s) FoM	26.5	450	62.5	116.4	35.6	26.3
Area (mm ²)	0.45	32	1.69	15	0.51	1.53
ADC topology	Full-flash	Pipeline	Pipeline	Full-flash	Interpolating- flash	Hybrid SAR
Nominal ADC resolution (bits)	4.5	8	5	6	5	5
Over sampling factor	1	1	1	1	2	1
Interleaving fac- tor	2	8	4	4	2	5
DFE taps	5	No	6	Dynamic	No	4 ^a
FFE taps	2	25	No	Dynamic	2	No
Off-chip block	No	No	CR	No	No	CR

^a Each one of the two SASDEFEs has 4 taps.

3.7 Chapter summary

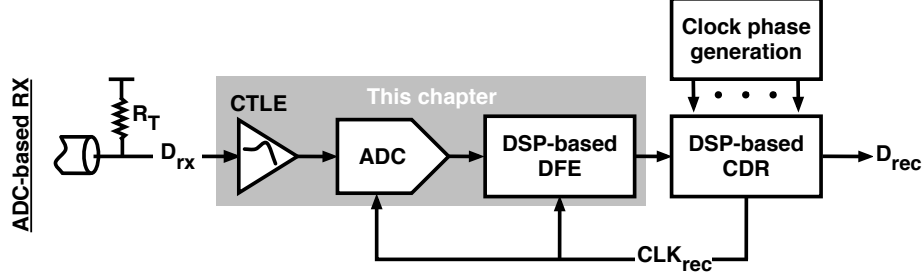


Figure 3.12: Graphical illustration of ADC and DFE blocks addressed in this Chapter, and their interaction with other RX blocks.

In this Chapter, a low-power architecture for high-speed ADC-based wireline RX is presented. As illustrated in Fig. 3.12, we seek the power reduction goal through system-level enhancements of the digitization front-end and DFE, similar to the SASDFE proposed in Chapter 2. As an alternative to the power-hungry flash ADCs, a custom digitization algorithm is developed which utilizes the channel low-pass characteristic in order to speculate the digitized value of the sampled signal and achieve a fast converging SAR ADC. The hybrid speculative/SAR digitization algorithm allows to reach a digitization speed of 2 GS/s per channel. Additional power savings are achieved by obviating the need for the multi-stage buffers preceding the ADC, and by embedding the data recovery and DFE functions within the ADC algorithm. The timing margin of the DFE feedback loop is improved by means of 1-tap loop unrolling, and the 5-way time-interleaved implementation of RX.

Chapter 4

Quadrature clock generation in RX

Due to the orthogonality of quadrature clock phases, Φ_I and Φ_Q , they are used at the front-end of “wireless” receivers to decode the data that has been encoded in the phase of received signal. A simple form of such decoding can be done through mixing two copies of the received data, which are provided by a splitter, one with Φ_I and the other with Φ_Q . Two well known modulation schemes that utilize phase encoding are quadrature phase shift keying (QPSK), and quadrature amplitude modulation (QAM); where in the former the data is merely encoded in phase of signal, whereas in the latter data has been encoded in both phase and amplitude of signal. The other potential use of quadrature phases in wireless RX is image rejection in low-IF receivers [54].

In “wireline” systems, however, it is most common to encode the data in the amplitude of transmitted signal as in binary or pulse amplitude modulation (PAM) signaling. While in its conventional form, wireline RX may not need quadrature clock phases, as discussed in Chapter 5, we utilize Φ_I and Φ_Q for data phase shifting, and frequency doubling at CDR front-end.

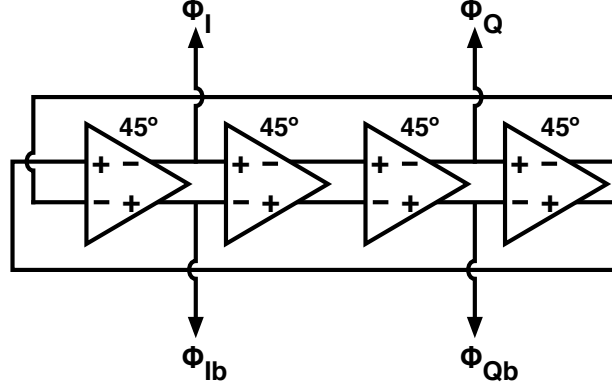


Figure 4.1: Schematic of a quadrature ring oscillator.

In this chapter, at first, we discuss some of the well-known methods for generating quadrature clocks as discussed in literature, and subsequently present the proposed quadrature clock generation technique. This chapter concludes with an analysis of the power consumption and jitter of the proposed method.

4.1 Ring oscillators

Figure 4.1 shows the architecture of a differential 4-stage ring oscillator which generates 8 equally spaced phases. Four out of the eight phase can be used as differential quadrature clock pairs, Φ_I - Φ_{Ib} and Φ_Q - Φ_{Qb} . To have a sustainable oscillation, the signal traveling through the loop should experience 360° of total phase shift, $\Delta\Phi_{total}$, which is provided by the ring of Fig. 4.1 as following:

$$\Delta\Phi_{total} = 360^\circ = \underbrace{180^\circ}_{\text{logical}} + \underbrace{4 * 45^\circ}_{\text{frequency dependent}} \quad (4.1)$$

4.1. Ring oscillators

The logical and frequency dependent phase shifts are provided by the cross-connection in the feedback loop, and the phase shift of the inverter at the frequency of the clock (f_0), respectively.

The curious reader may wonder, if only 90° separated phases are required and not the additional 45° phases, why the ring oscillator of Fig. 4.1 employs $4 \times 45^\circ$ scheme for frequency dependent delay and not $2 \times 90^\circ$? Specifically, this question is legitimate as in first glance the $2 \times 90^\circ$ may provide less phase jitter as employs half the number of noisy active elements in the ring. Although such reasoning is partially true, it should be noted that a stand alone inverter without an explicit load capacitance¹⁷, C_L , may have a smaller propagation delay compared to the desired propagation delay, $t_{p,inv}$, as given by

$$t_{p,inv} = 90^\circ = \frac{1}{4} \times \frac{1}{f_0} \quad (4.2)$$

Thus, compared to the $4 \times 45^\circ$ scheme, the $2 \times 90^\circ$ requires a larger C_L . While $2 \times 90^\circ$ scheme offers less active elements, from a power consumption standpoint, it may not provide an overall power saving as a larger capacitance should be driven by each inverter. Also, a higher $t_{p,inv}$ usually translates to a higher time constant in the output of each inverter, which aggravates the effect of clock jitter. The $4 \times 45^\circ$ configuration provides sharper clock edges compares to the $2 \times 90^\circ$ configuration.

¹⁷ C_L is not explicitly shown in Fig. 4.1.

4.2 LC oscillators

4.2.1 Differential LC oscillators

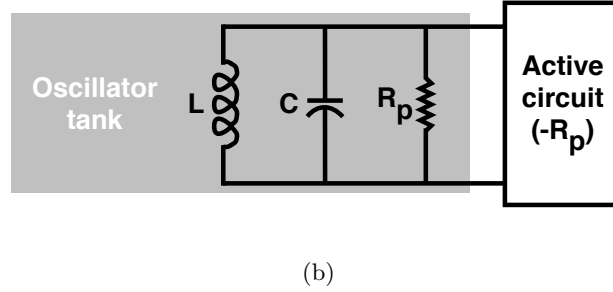
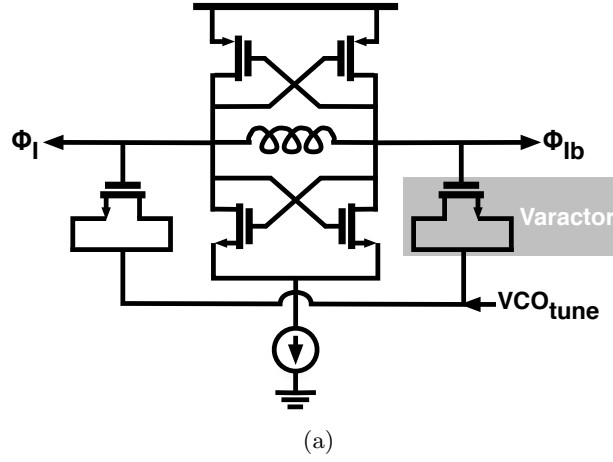


Figure 4.2: Schematic of an LC VCO (a), and canceling the parasitic resistance of inductor, R_p , in LC tank using an active element (b).

Figure 4.2a shows a typical architecture for an LC voltage controlled oscillator, VCO, in which both NMOS and PMOS cross coupled pairs are used to re-use the current and provide a higher negative resistance $-R_p$ [55]. Figure 4.2b illustrates the fundamental of oscillation in the tank formed by the inductor, L , capacitor, C , parallel resistance of inductor, R_p , and the

actively generated negative resistance $-R_p$. As R_p and $-R_p$ cancel each other, VCO should provide a sustainable oscillation at frequency f_0 given by

$$f_0 = \frac{1}{2\pi \times \sqrt{L \times C}} \quad (4.3)$$

unlike the ring oscillator which oscillates based on delay generation in feedback loop, the LC oscillator oscillates due to exchange of energy between magnetic and electric fields.

4.2.2 Quadrature LC oscillators

Two LC tanks can be injection locked (coupled) to each other to generate Quadrature phases. Figures 4.3a and 4.3b show two possible forms of injection locking, where the former illustrates current-mode injection locking using transistors, and the latter utilizes magnetic coupling between the two tanks. Coupling through active devices (Fig. 4.3a) degrades the phase noise of the overall quadrature oscillator due to the thermal and flicker noise of coupling devices [56]. While magnetic coupling (Fig. 4.3b) provides a better phase noise performance, the large area required by the coupling transformer makes it an inferior design choice.

4.3 Phase noise and power trade-off

Each of the discussed clocking methods are subject to a trade-off among area, power, and phase noise. In this section, we discuss such trade-off in

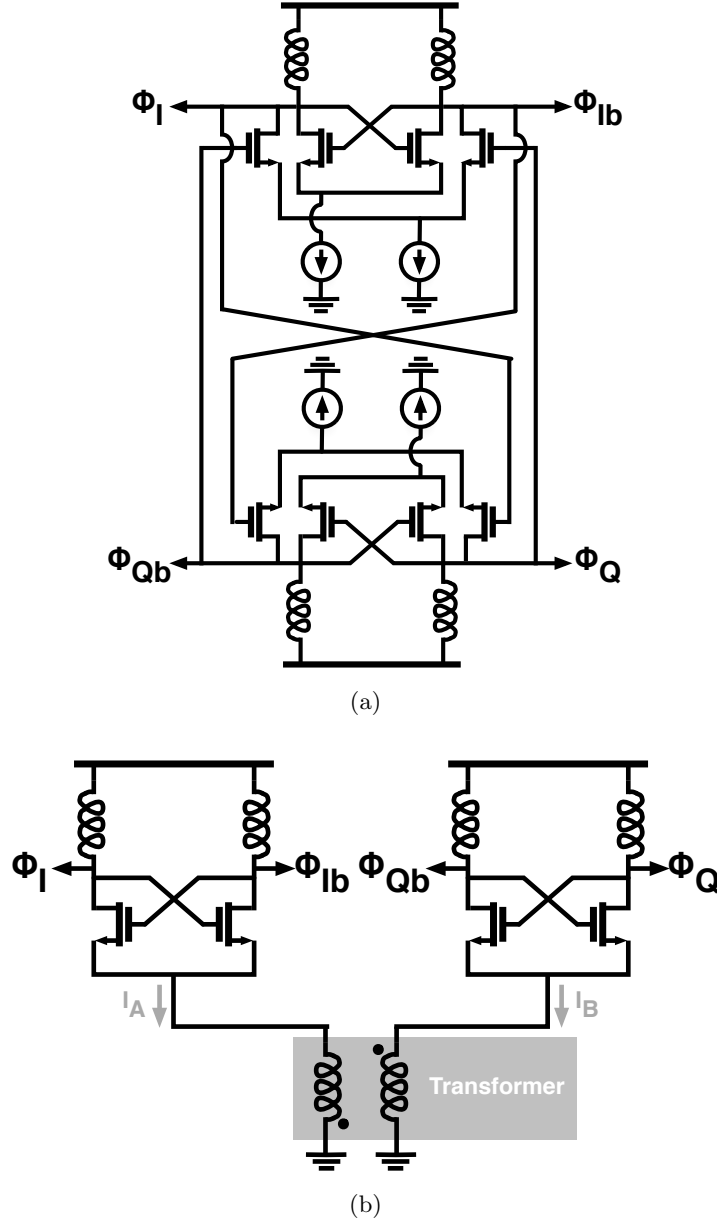


Figure 4.3: Quadrature clock generation using two current-coupled LC oscillators (a), and another method of coupling using a transformer (b).

LC tank VCO, ring VCO, and the proposed injection-locked QPG clocking method.

4.3.1 Phase noise in LC VCO

Considering the simplified LC tank of Fig. 4.2b, the phase noise, $\mathcal{L}_{lc}(\Delta\omega)$, of the LC VCO at frequency offset $\Delta\omega$ is given by the following equation [55]

$$\mathcal{L}_{lc}(\Delta\omega) = 2kT \left(\frac{3}{8}\gamma + 1 \right) \left(\frac{R_p}{\frac{v_{sw}^2}{2}} \right) \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \quad (4.4)$$

where ω_0 is the main oscillation frequency, and $v_{sw,lc}$ is the differential peak swing which can be written as

$$v_{sw,lc} = \left(\frac{4}{\pi} \right) \left(\frac{R_p I_{lc}}{2} \right) = \frac{2I_{lc}R_p}{\pi} \quad (4.5)$$

Hence, considering that

$$R_p = Q \times L \times \omega_0 \quad (4.6)$$

we can re-write Eq. 4.4 as

$$\mathcal{L}_{lc}(\Delta\omega) = \pi^2 kT \left(\frac{3}{8}\gamma + 1 \right) \left(\frac{\omega_0}{4LQ^3 I_{lc}^2 \Delta\omega^2} \right) \quad (4.7)$$

4.3.2 Phase noise of ring oscillator

The first source of phase noise in a ring oscillator is the uncorrelated noise of input devices in each inverter, that modulate the inverter delay and result in phase noise. The second source of phase noise in ring oscillators is the $\frac{1}{f}$ (flicker) noise of tail current source in each inverter. As the current through tail current sources are mirrors of a golden reference current, these noise sources are correlated. The latter noise source results in significant phase noise in ring oscillators and is inversely proportional to the tail current, I_{inv} , in each inverter; hence, trading-off with the power consumption. For the phase noise of a ring oscillator we can write

$$\mathcal{L}_{ring}(\Delta\omega) = \left(\frac{2kT}{I_{inv} \ln 2} \right) \left(\frac{7\gamma}{4v^*} + \frac{1}{v_{sw,ring}} \right) \left(\frac{\omega_0}{\Delta\omega} \right)^2 \quad (4.8)$$

where $v_{sw,ring}$ is the peak differential swing per stage, and $v^* \propto (v_{gs} - v_{th})$.

4.3.3 $\mathcal{L}(\Delta\omega)$ -power-area trade-off in ring and LC oscillators

While a ring oscillator occupies an area equal to a fraction of smallest on chip inductor, its phase noise is considerably higher than a well-designed LC oscillator [55].

To investigate the phase noise/power trade-off between ring and LC oscillators, we set $\mathcal{L}_{lc}(\Delta\omega)$ of Eq. 4.7 equal to $\mathcal{L}_{lc}(\Delta\omega)$ of Eq. 4.8, and find the relationship between the tail currents as following

$$\frac{I_{inv}}{I_{lc}} \approx \frac{8 \times Q^2 \times V_{DD}}{v^*} \quad (4.9)$$

4.4. Proposed quadrature clock generator

while for the total current in an N stage ring oscillator we can write

$$I_{ring} = N \times I_{inv} \quad (4.10)$$

This reveals a steep trade-off between phase noise and power in ring oscillators as compared to the considerably more relaxed trade-off in LC oscillators. Therefore, based on Eqs. 4.9 and 4.10, a 4-stage ring oscillator (that provides quadrature phases) should approximately dissipate $1000\times$ the power of an LC oscillator which has a tank Q of 2.5.

4.4 Proposed quadrature clock generator

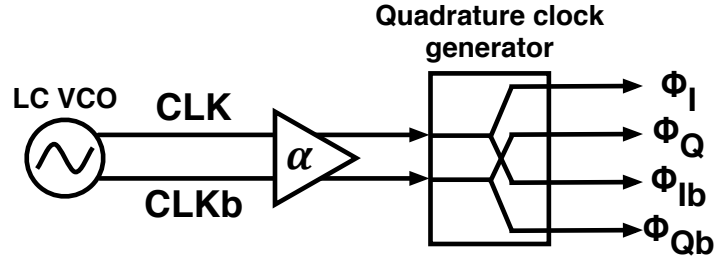


Figure 4.4: Quadrature clock generation using coupling a differential VCO to the quadrature phase generation block.

In this work, quadrature clock phases are generated using injection locking of a delay ring to a differential LC VCO. Figure 4.4 shows how the quadrature clock generator (QCG) block is injection locked through a transconductance stage to the relatively low-jitter clock phases, CLK and $CLKb$, generated by a differential LC VCO.

Figure 4.5 illustrates the implementation of injection locking (coupling) in

4.4. Proposed quadrature clock generator

$$\alpha = \frac{I_{cpl}}{I_{ss}} \quad (4.11)$$

Figure 4.6 shows the block diagram of the QCG block, which com-

Figure 4.5: Unilateral coupling through current injection into the QPS ring.

4.4. Proposed quadrature clock generator

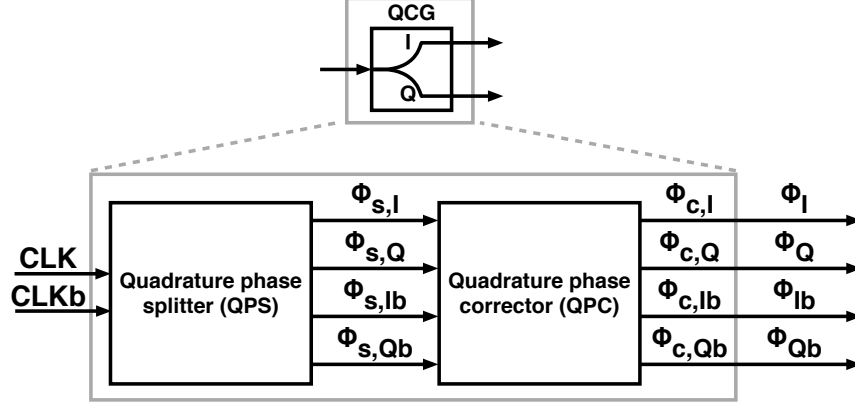


Figure 4.6: Quadrature clock generator.

inversion and buffering use inductive peaking to reduce their propagation delay and to sharpen the edges of their output signal. Sharp clock edges are necessary to increase the signal to noise ratio at the output of succeeding stages (i.e., mixers) [55]. The eight single-ended inverters (four differential CML inverters) used in the delay loop are resistively loaded. Given the delay loop structure, each inverter provides 45° (i.e., $\frac{1}{8} \times 360^\circ$) of frequency dependent phase shift (delay) between its input and output signal¹⁸. These delay-loop inverters are used for averaging and splitting clock phases [57].

In the QPS stage, the differential VCO clock, $CLK-CLKb$ is split into four phases, $\Phi_{s,I}$, $\Phi_{s,Q}$, $\Phi_{s,Ib}$, and $\Phi_{s,Qb}$ which are nominally separated by 90° from each other. However, the quadrature phases may deviate from their ideal position for example due to the jitter resulting from mismatches in propagation delay of the inverters. To alleviate this issue, the QPC stage is used to generate corrected clock phases: $\Phi_{c,I}$, $\Phi_{c,Q}$, $\Phi_{c,Ib}$, and $\Phi_{c,Qb}$.

¹⁸In this manuscript, we refer to such inverter arrangement as $8 \times 45^\circ$ configuration.

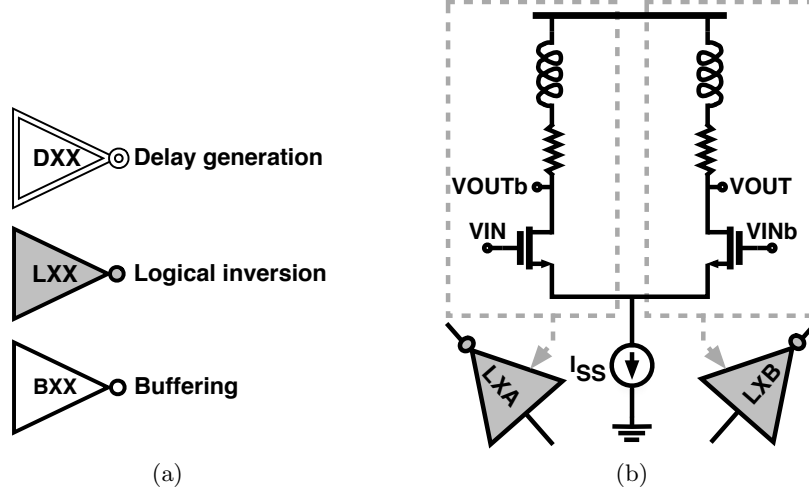


Figure 4.7: (a) Legend indicating the type and function of inverters used in QPS and QPC sub-blocks. (b) Format of CML half-inverters used in QPS and QPC.

4.5 Enhancing the power efficiency of QCG

While a ring of 8 half CML inverters, each generating 45° of frequency dependent phase shift, was used in QPS (Fig. 4.8a) and QPC (Fig. 4.8b) to shield the input and output phases from each other, such architecture may not be power efficient/feasible given a certain CMOS process¹⁹.

To characterize the power consumption of the QCG block with $8 \times 45^\circ$ configuration, let's consider the half inverter of Fig. 4.9 which is driving a discrete load capacitance C_L , in addition to the gate capacitance of the next inverter, c_{gg} . For sake of delay analysis, we can simplify this circuit to the one shown in Fig. 4.10. For the output voltage, V_o we can write

¹⁹Note that a 90 nm CMOS process is used to implement the QCG.

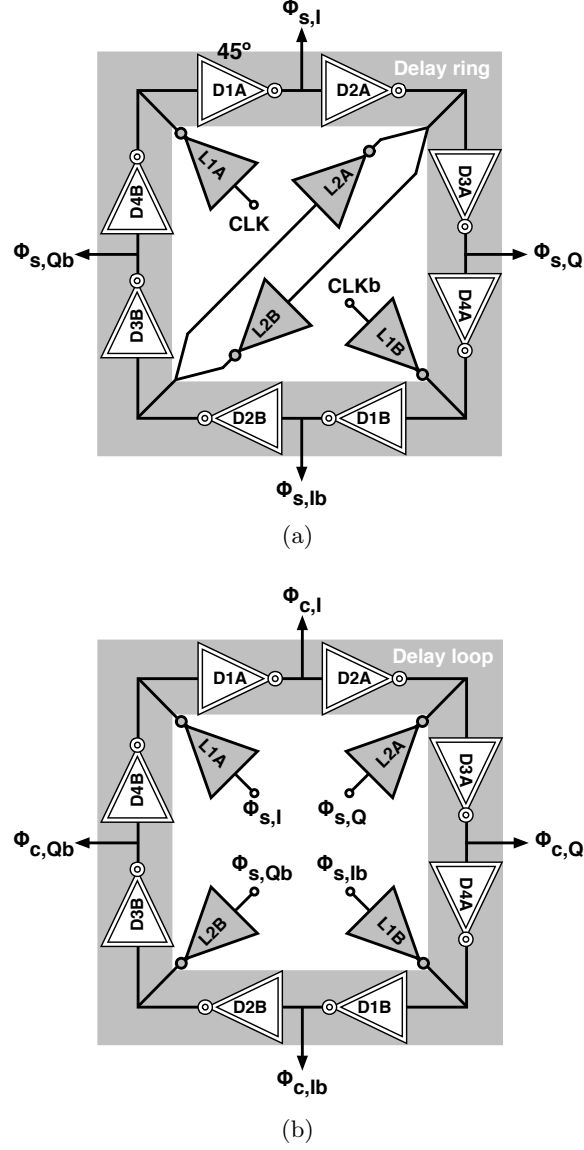


Figure 4.8: QPS sub-block (a), and QPC sub-block (b) in $8 \times 45^\circ$ configuration.

$$V_o = (V_{DD} + I_d \times R_{eq}) \times e^{\frac{-t}{C_{total} \times R_{eq}}} - I_d \times R_{eq} \quad (4.12)$$

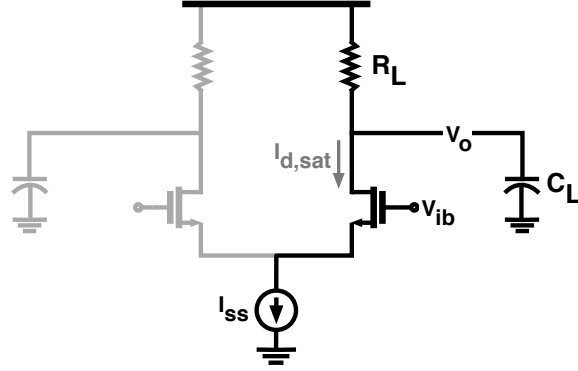


Figure 4.9: AC representation of the half CML inverter.

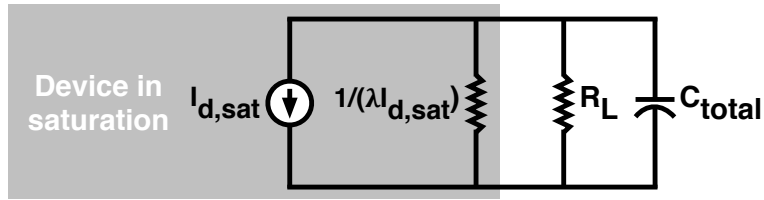


Figure 4.10: Simplified model used for delay calculation.

where λ is the channel length modulation factor. For R_{eq} we have

$$R_{eq} = (R_L || \frac{1}{\lambda I_d}) \quad (4.13)$$

and considering the self loading capacitance of M_1 , c_{dd} , the total capacitance at node V_o , C_{total} , is given by

$$C_{total} = c_{gg} + c_{dd} + C_L \quad (4.14)$$

4.5. Enhancing the power efficiency of QCG

Using Eq. 4.12, to find the %50 delay, t_p , we set

$$V_o = v_{sw} = \frac{V_{DD} - 2 \times v_{od}}{2} = \frac{I_d \times R_L}{2} \quad (4.15)$$

where v_{sw} is the peak swing, and a headroom of $2 \times$ the overdrive voltage, v_{od} , is allocated to keep both the tail current source and the input device, M_1 , in saturation ²⁰. Solving Eq. 4.12 while using the simplifying assumption of $\lambda \rightarrow 0$

$$t_p \approx -R_L C_{total} \times \ln \left(\frac{3I_d R_L}{4(v_{od} + I_d R_L)} \right) \approx 0.51 \times R_L C_{total} \quad (4.16)$$

To write Eq. 4.16 based on the parameters of M_1 , let's consider the following equations and definitions: effect of self-loading of M_1 on its transconductance is given by

$$g_m = \frac{A\omega_{bw} \times C_L}{1 - \frac{A\omega_{bw}}{\omega_T \times c_{gg} c_{dd}}} \quad (4.17)$$

we write the product of gain and bandwidth of M_1 , $A\omega_{bw}$, as

$$A\omega_{bw} = \frac{1 \times n_\tau}{\frac{1}{8} \times \frac{1}{f_0}} = 32 \times f_0 \mid n_\tau = 4 \quad (4.18)$$

where 4 times the settling time constant, τ , is considered (i.e., $n_\tau = 4$) to reach the %98 of the final value. Also,

$$\omega_T = \frac{g_m}{c_{gg}} = \frac{\omega_{bw} \times (c_{gg} + c_{dd} + C_L)}{c_{gg}} \quad (4.19)$$

²⁰ $v_{od} \approx 200$ mV is a good estimate for the design.

4.5. Enhancing the power efficiency of QCG

where ω_{bw} is the angular unity²¹ gain bandwidth at the V_o node, ω_T is the unity gain bandwidth of M_1 . Using Eqs. 4.16 to 4.19, we can write

$$t_p = \frac{0.51 \times 2 \times 0.8}{v^*} \times \frac{C_{total}}{g_m} = \frac{1}{8 \times 12.5 \text{ GHz}} \quad (4.20)$$

$$A\omega_{bw} = \frac{0.51 \times 2 \times 0.8}{t_p \times v^*} > 32f_0 \quad (4.21)$$

Based on Eq. 4.21, the $8 \times 45^\circ$ configuration mandates a unity gain bandwidth, f_{bw} , greater than 64 GHz at the output node, V_o . To understand

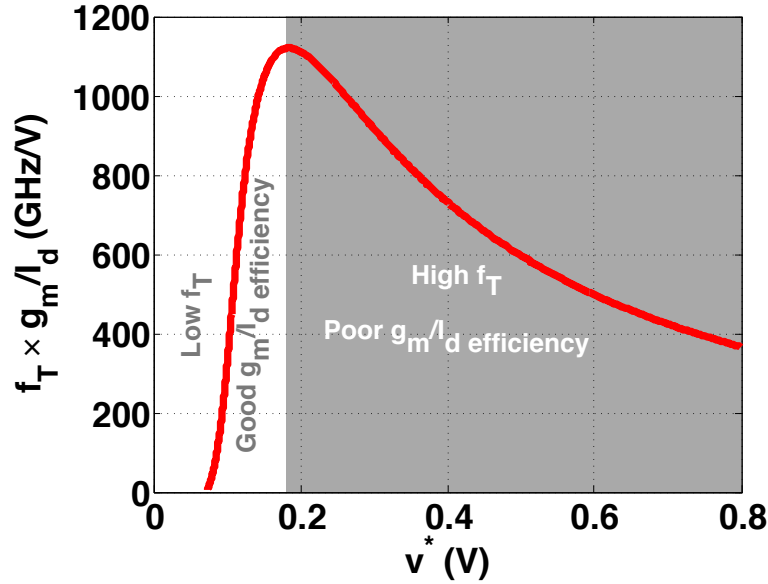
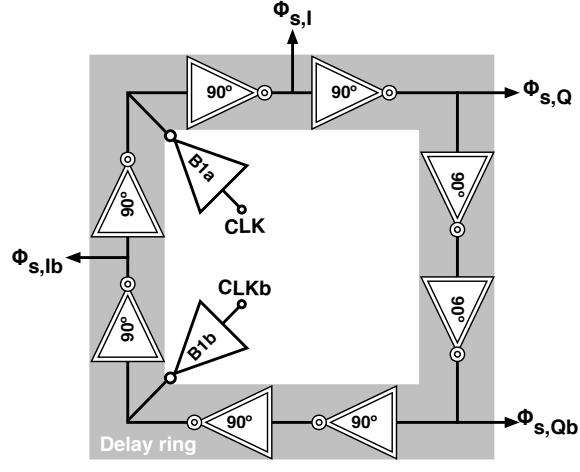


Figure 4.11: Speed versus power efficiency of an n-channel device in 90nm CMOS.

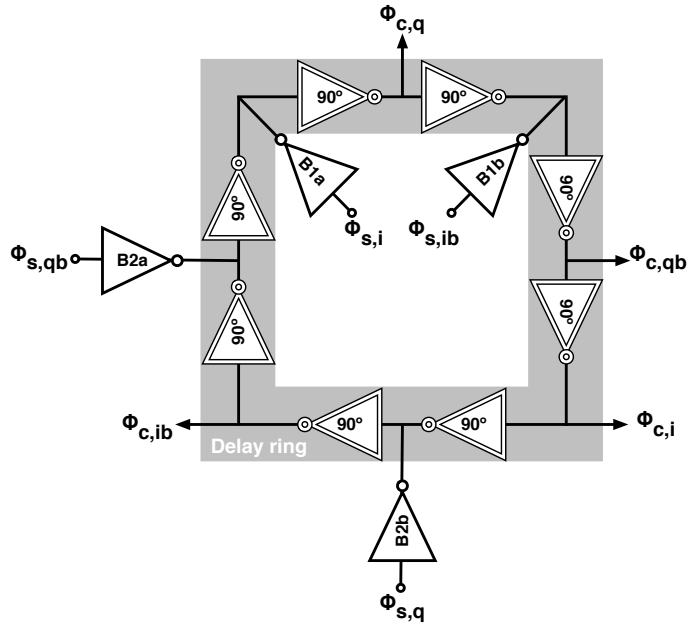
the power penalty of such high bandwidth requirement, let's consider the

²¹As the inverters act as buffers, we set $A = 1$.

intrinsic speed versus power efficiency of an N-channel device. Figure 4.11 shows the $\frac{f_T \times g_m}{I_d}$ FoM for an NMOS in 90-nm technology. The peak of FoM graph, where device offers the best trade-off between speed and power efficiency, occurs at $v^* \approx 200$ mV. For $v^* > 0.2$ V the device provides good speed but poor power efficiency, while $v^* < 0.2$ V results in good power efficiency at the price of lower speed (lower f_T). An f_{bw} value comparable to maximum f_T of device (i.e., $f_{bw} = f_{T,max}$) can push the operation point of the device towards the right region, in which the device quickly becomes power-inefficient, and requires large v_{od} . Therefore, to allow for a lower required f_{bw} at node V_o , we can modify the architecture of the QCG from a $8 \times 45^\circ$ configuration to the $8 \times 90^\circ$ configuration shown in Fig. 4.12. Figures 4.12a and 4.12b show the modified architectures for QPS and QPC sub-blocks in which the delay ring inverters have a frequency dependent phase shift of 90° at the clock frequency, f_0 . This reduces the required f_{bw} at node V_0 of ring inverters to ≈ 32.5 GHz. Equation 4.21 sets an upper limit for v^* , while as shown in Fig. 4.13, the lower limit is partially set by the sensitivity of t_p to variation in v^* . Figure 4.14 shows the power consumption of a single inverter in each of the configurations versus v^* . The exponential increase in the power consumption of the inverter for the lower values of v^* is noteworthy. Specially, Eq. 2.10 suggests that given a certain g_m , the power consumption is proportional to v^* , while Fig. 4.14 suggests an inverse relationship. Such inverse relationship for lower values of v^* (e.g., $v^* < 0.2$ V) can be explained by considering the self loading effect of the transistor. As the f_T of the device degrades in this region and gets closer to f_{bw} , the power penalty due to driving the self loading capacitance of the



(a)



(b)

Figure 4.12: QPS sub-block (a), and QPC sub-block (b) in $8 \times 90^\circ$ configuration.

device (c_{dd}) becomes significant. Therefore, power consumption is the other key factor in determining the lower limit of v^* .

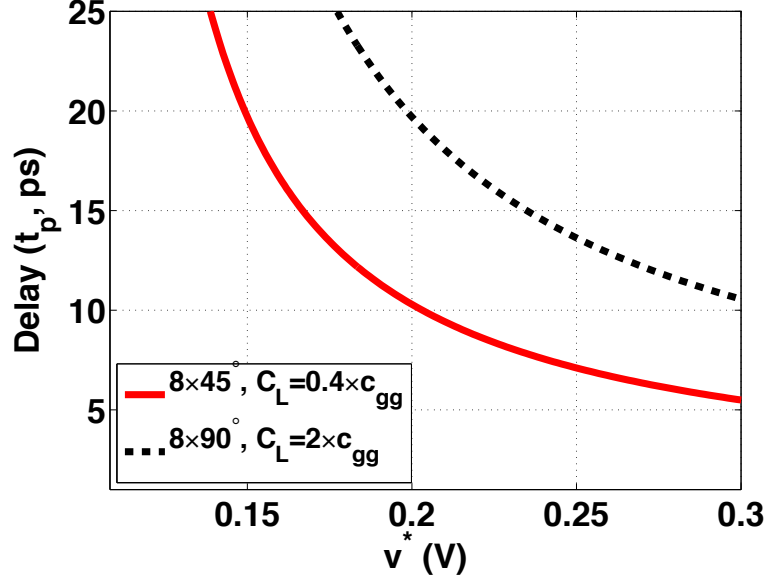


Figure 4.13: Delay of inverter as a function of v^* .

Note that for each graph in Figs. 4.13 and 4.14, a certain amount of C_L has been used to set the desired delay (i.e., for $f_0 = 12.5$ GHz, inverter delays should be equal to 10 ps and 20 ps for $8 \times 45^\circ$ and $8 \times 90^\circ$, respectively).

As Figure 4.15 suggests, one remedy is to coarsely set $v^* \approx 0.2$ V, and then fine tune the value of t_p using C_L . Fig. 4.15 reveals another interesting result; while operating in the left hand region of Fig. 4.11, increasing the delay through adding C_L , versus decreasing v^* can significantly reduce the power consumption of each delay stage (inverter).

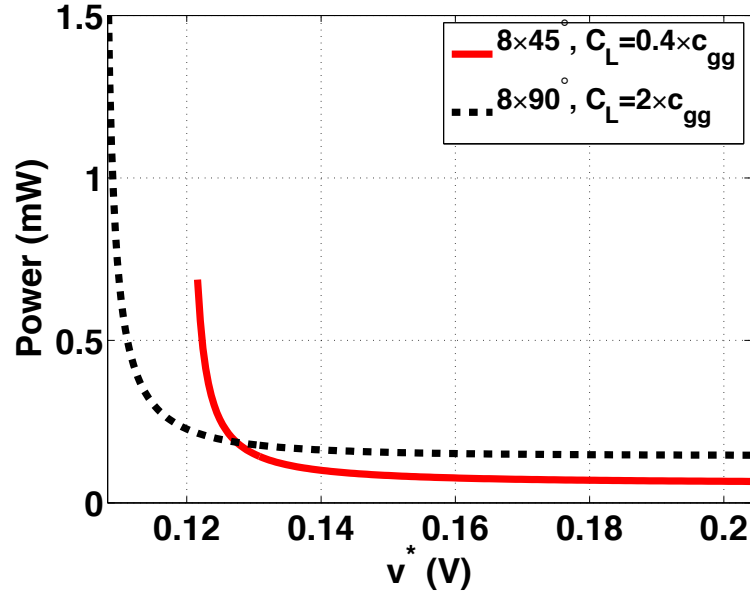


Figure 4.14: Power consumption of the inverter as a function of v^* .

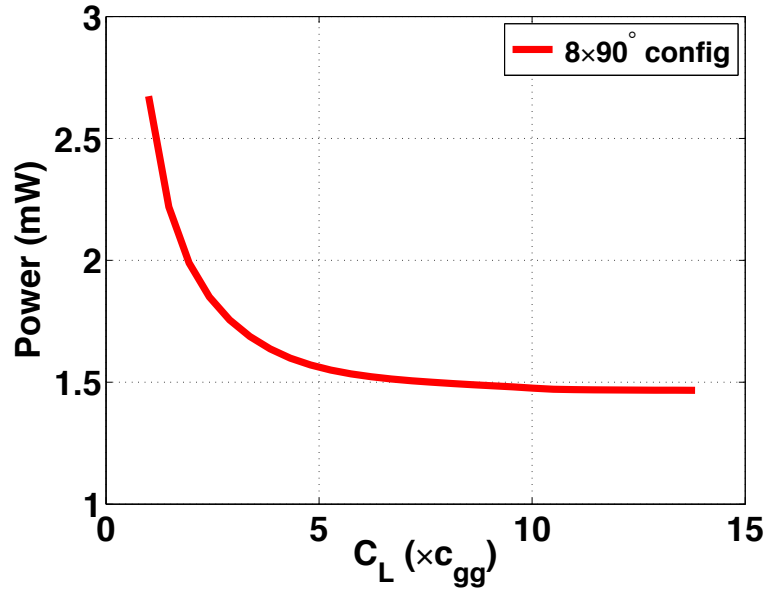


Figure 4.15: Effect of using a discrete load capacitance, C_L , on power consumption per inverter stage. Plotted for a constant value of t_p .

4.6 Jitter in QCG block

To analyze the jitter²² performance of the proposed QCG, let's consider the half inverter of Fig. 4.9. The AC voltage at node V_o is given by

$$V_o = v_{sw} \sin(\omega_0 t + \phi_1) + n(t) \quad (4.22)$$

where $\omega_0 = 2\pi \times 12.5 \text{ GHz}$ ²³, ϕ_1 is the arbitrary phase of the waveform, and $n(t)$ is a term representing the contribution of all noise sources (i.e., noise of passives and actives). Hence, the variance of absolute time jitter, σ_τ^2 , and variance of phase jitter, σ_ϕ^2 , are given [58] as

$$\sigma_\phi^2 = \omega_0^2 \times \sigma_\tau^2 = \frac{\sigma_n^2}{v_{sw}^2} \quad (4.23)$$

Based on Eq. 4.23, to reduce the jitter contribution of each inverter, we should either increase v_{sw} , or decrease σ_n^2 . We discuss the trade-offs associated with each of these options.

4.6.1 Maximizing voltage swing

While connecting the cascaded inverters in the DC-coupled format shown in Fig. 4.16 provides the lowest C_L at the timing critical node, V_o , such approach limits the maximum v_{sw} achievable at V_o . In a $8 \times 90^\circ$ configuration, the voltages at nodes V_o and Vb_i can be written with respect to each other

²²Jitter and phase noise are used interchangeably in this manuscript, where the former refers to quality of clock edges in time domain, whereas the latter refers to purity of clock spectrum in frequency domain.

²³The VCO clock, CLK , is considered to have a frequency of 12.5 GHz.

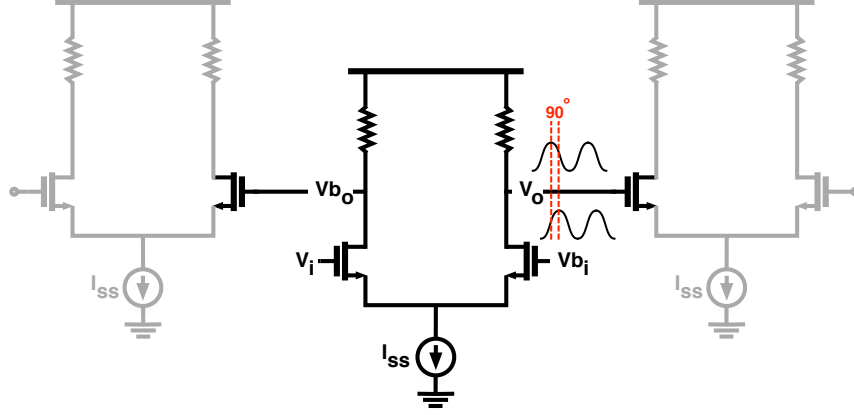


Figure 4.16: DC-coupled connection between the inverter stages.

as

$$V_o = v_{sw} \sin(\omega_0 t + \frac{3\pi}{2}) \quad (4.24)$$

$$V_{b_i} = v_{sw} \sin(\omega_0 t) \quad (4.25)$$

to keep input device M_1 in saturation we should have

$$V_o - V_{b_i} = -\sqrt{2} \times v_{sw} \sin(\omega_0 t + \frac{\pi}{4}) > -v_{th} \quad (4.26)$$

where v_{th} is the threshold voltage of M_1 . Assuming $v_{th} = 380 \text{ mV}$, for Eq. 4.26 to hold true, we should have

$$v_{sw} < \frac{v_{th}}{\sqrt{2}} \approx 0.27 \quad (4.27)$$

4.6. Jitter in QCG block

which indeed limits the maximum swing achievable ²⁴ at node V_o . Note that the $8 \times 45^\circ$ configuration offers a higher upper-bound for DC-coupled swing as we have

$$v_{sw} < \frac{v_{th}}{\sqrt{2 - \sqrt{2}}} \approx 0.5 \quad (4.28)$$

which indicates that the $8 \times 45^\circ$ configuration allows for the desired v_{sw} of 0.4 V. Therefore, to choose either $8 \times 45^\circ$ or $8 \times 90^\circ$ configuration, we should consider parameters such as f_0 , $\frac{f_T \times g_m}{I_d}$ of devices (Fig. 4.11), v_{sw} , sensitivity of t_p to v^* variations (Fig. 4.13), and power efficiency of inverters (Fig. 4.14) given the values chosen for v^* and C_L .

The AC-coupled version of the circuit shown in Fig. 4.16 deserves some attention. Figure 4.17 illustrates AC-coupled biasing of inverter stages through a “T” connection. The voltage at the gate of device M_3 is attenuated through the capacitive voltage division of the coupling capacitor C_{cop} with the gate capacitance of M_3 , c_{gg} , for which we can write

$$V_{g3} = \frac{V_o \times C_{cop}}{C_{cop} + c_{gg}} \quad (4.29)$$

Hence we choose $C_{cop} \approx 10 \times c_{gg}$. Also, we set the cutoff frequency of the high-pass filter formed by C_{cop} and R_1 well below f_0 . Hence, we have

$$\frac{1}{R_1 \times C_{cop}} \ll f_0 \quad (4.30)$$

²⁴Note that without considering the biasing of succeeding and preceding stages, the maximum achievable v_{sw} , in each CML inverter stage is ≈ 0.4 V (i.e., $\frac{V_{DD} - 2v^*}{2}$) in a 90-nm technology with 1.2 V supply.

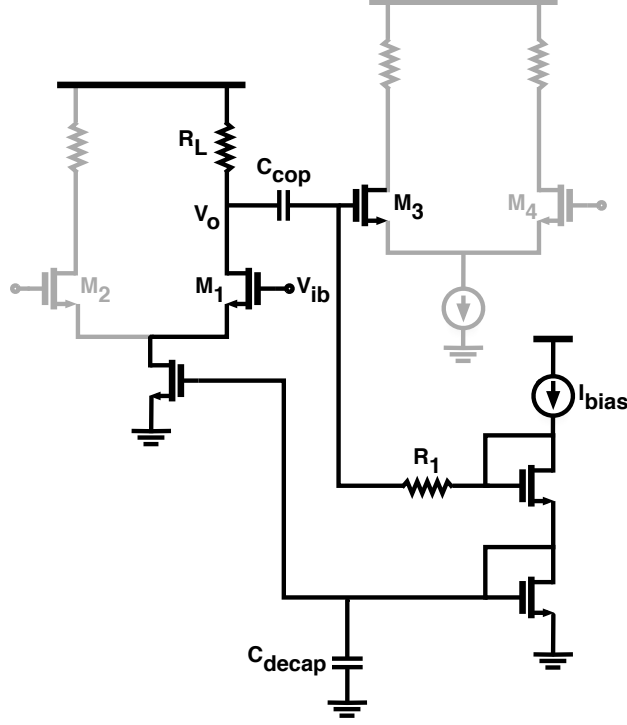


Figure 4.17: AC-coupled connection between the inverter stages.

A decoupling capacitor, C_{decap} , is used at the gate of the tail current to avoid the modulation of I_d through high frequency deterministic and random noise. As the value of C_{decap} need not precisely match a specific value²⁵, it is realized through forming metal-oxide-metal (MoM) caps using the metal layers that are used to fill the chip.

²⁵The larger the value of C_{decap} , the lower the bandwidth at gate of tail current source would be, hence C_{decap} would be capable of filtering noise up-to lower frequencies.

4.6.2 Noise of actives and passives in inverter stage

The mean square noise voltage, $\overline{v_n^2}$, at the V_o node in the differential inverter of Fig. 4.9 is given by

$$\overline{v_n^2}(f) = 2 \times (R_L || r_{o1})^2 \times \left(\underbrace{\frac{K g_{m1}^2}{C_{ox} W L f}}_{\frac{1}{f} \text{ noise}} + \underbrace{\frac{8KT g_{m1}}{3} + \frac{4KT}{R_L}}_{\text{thermal noise}} \right) \quad (4.31)$$

note that the factor $2 \times$ in Eq. 4.31 is due to the fact that the noise voltage power of a differential stage is twice that of a single-ended stage [34]. To find the phase noise spectral density, $S_\phi(\Delta f)$, we can write

$$S_\phi(\Delta f) = 2\mathcal{L}_{inv}(\Delta f) = \frac{\overline{v_n^2}(f)}{v_{sw}^2} = \frac{4 \times \overline{v_n^2}(f)}{(I_d \times R_L)^2} \quad (4.32)$$

where $\mathcal{L}_{inv}(\Delta f)$ is the single-sided phase noise spectrum of V_o around f_0 . From Eq. 4.32, we can calculate the variance of the period jitter, $\sigma_{pj,inv}^2$, as

$$\sigma_{pj,inv}^2 = \left(\frac{1}{\pi f_0} \right)^2 \int_0^{\frac{f_0}{2}} \sin^2 \left(\frac{\pi \times \Delta f}{f_0} \right) S_\phi(\Delta f) d\Delta f \quad (4.33)$$

While due to the $\frac{1}{f}$ term in Eq. 4.31 an explicit answer for the integral of Eq. 4.33 does not exist, by ignoring the contribution of flicker noise to $\overline{v_n^2}(f)$ we can write

$$\sigma_{pj,inv}^2 = \left(\frac{2}{f_0} \right) \times \left(\frac{R_L || r_{o1}}{\pi I_d R_L} \right)^2 \times \left(\frac{8KT g_{m1}}{3} + \frac{4KT}{R_L} \right) \quad (4.34)$$

4.6. Jitter in QCG block

Using the maximum allowable peak swing of $2v^*$, and based on Eqs. 4.15, and 2.10, we simplify Eq. 4.34 as

$$\sigma_{pj,inv}^2 = \left(\frac{1}{I_d} \right) \times \underbrace{\left(\frac{38KT}{3\pi^2 v^* f_0} \right)}_{\approx 2 \times 10^{-30}} \quad (4.35)$$

where we have assumed $R_L \ll r_{o1}$. Using Eq. 4.35 we can get to the RMS period jitter, $J_{pj,inv}$, by

$$J_{pj,inv} \text{ (fs)} = \sqrt{\sigma_{pj}^2} \approx \sqrt{\frac{2}{I_d}} \quad (4.36)$$

Eq. 4.36 shows that $J_{pj,inv}$ trades-off with $\frac{1}{\sqrt{I_d}}$. Thus revealing the steep power penalty in achieving a low-jitter design for a single inverter cell. As the noise in each of the 8 inverters in the rings of QPS and QPC are uncorrelated, for the total period jitter variance of the rings, $\sigma_{pj,rqp}^2$, we can write

$$\sigma_{pj,rqp}^2 = 8 \times \sigma_{pj,inv}^2 \quad (4.37)$$

Likewise, for the RMS period jitter contribution of QPS and QPC rings, $J_{pj,rqp}$, we have

$$J_{pj,rqp} \text{ (fs)} = 2\sqrt{2} \times J_{pj,inv} = \frac{4}{\sqrt{I_d}} \quad (4.38)$$

Equation 4.38 demonstrates the fundamental amount of jitter that would be added to the clock phases by the QPS and QPC rings.

4.7 Chapter summary

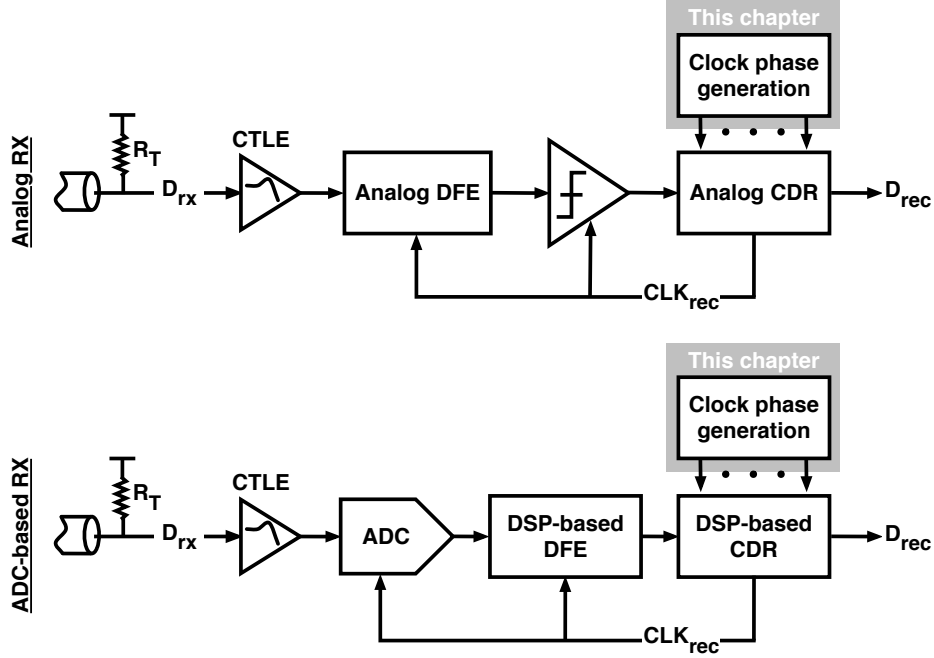


Figure 4.18: Graphical illustration of quadrature clock generation block introduced in this Chapter, and its interaction with other RX blocks.

An open loop method for generating quadrature clock phases from the differential clock provided by a VCO is presented. The proposed technique is utilized in the analog and digital CDRs presented in Chapters 5 and 6. The orthogonality of CLK_I and CLK_Q makes quadrature clock phases an integral part of most modern CDRs. Figure 4.18 shows the interaction of QCG with other blocks in analog and digital CDRs. While in a phase interpolator based CDR (i.e., dual-loop CDR), QCG clock phases are feed-forwarded to the interpolation/DLL loop, in a PLL based CDR (i.e., the single-loop CDRs presented in Chapter 5), the QCG is located in the main feedback

4.7. Chapter summary

loop. When quadrature clock phases are needed at various locations in a large system-on-a-chip (SoC), the QCG block allows to locally generate the phases and avoid the challenges and distortions associated with routing the phases over long distances. Finally, this Chapter analyzes the phase noise performance of the QCG. Such analysis helps to determine the optimum number of QPC blocks which follow the QPS block.

Chapter 5

Analog CDR in high-speed links

Clock and data recovery (CDR) systems play a vital role in high-speed wireline links to achieve power and hardware efficient data transmission at bit error rates (BERs) better than 10^{-12} . In this Chapter, we investigate analog CDR architectures, and propose a PLL-based CDR suited for multi-Gb/s speeds, which exploits a mixer as phase detector (PD).

5.1 Line codes in serial links

While there are numerous line coding methods discussed in literature [59], this manuscript focuses on non-return to zero (NRZ) signaling. Such line coding has universally become the method of choice for transmitting binary data across wireline channels. Let's consider the waveforms in Fig. 5.1, which represent return to zero (RZ) and NRZ lines codes along with a baud-rate clock. For a data pattern of consecutive '1's and '0's, the number of transitions in an RZ code are equal to that of baud-rate clock and twice the transitions in NRZ code. Therefore, unlike the RZ code, NRZ does not have a clock component in its spectrum. Due to the presence of a clock

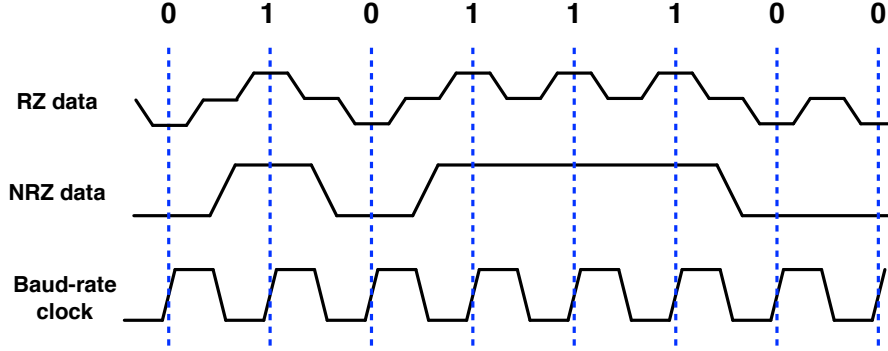


Figure 5.1: Comparison of RZ data, NRZ data, and the baud rate clock.

component in RZ code, a clock can be directly extracted from the data; thus, it is also called a self-synchronizing code. In Contrast, NRZ signaling needs additional measures to recover the frequency of the clock. However, as the transitions in NRZ coding are half of RZ coding for a similar data pattern, NRZ signaling makes more efficient use of channel bandwidth. Also, NRZ coding offers better signal transmission efficiency compared to RZ coding. This is due to the fact the NRZ code sustains the peak voltage swing at TX driver for 1 UI time interval (as opposed to 0.5 UI interval in RZ); hence, it transmits the maximum amount of energy to the channel.

5.2 Clock recovery using high-Q filter

Figure 5.2 shows the spectrum of a 12.5 Gb/s NRZ data (i.e., $f_{baud} = 12.5$ GHz), where the spectrum has a null at f_{baud} . If we pass such signal through a nonlinear block, i.e., a mixer, all of its harmonics will mix with each other and produce sum and difference terms. Now, consider the two coherent harmonics at $f_{baud} - \Delta f$ and $f_{baud} + \Delta f$ frequencies, which are

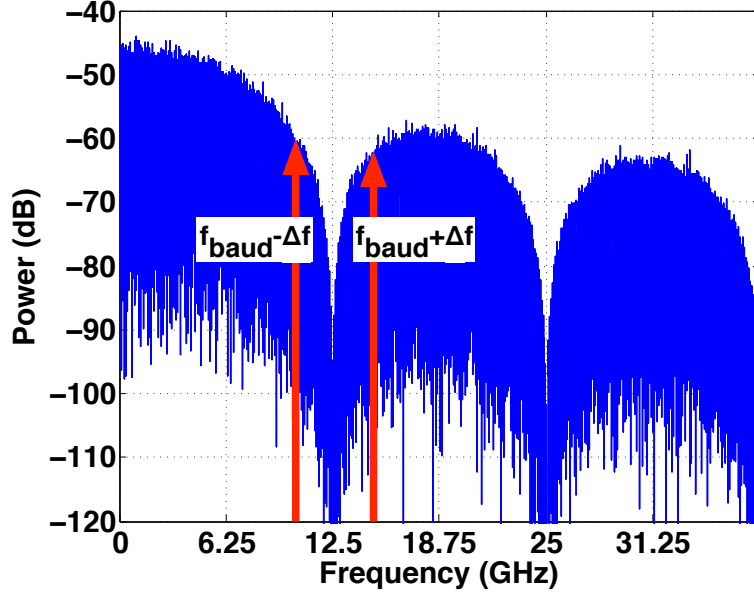


Figure 5.2: The harmonics around f_{baud} in the spectrum of NRZ data, which are used to extract the baud-rate clock.

annotated as two impulses in Fig. 5.2. Each of these harmonics can be represented by a sine wave in time domain as following

$$hrm_1 = A_1 \times \sin(2\pi(f_{baud} - \Delta f) + \phi_1) \quad (5.1)$$

$$hrm_2 = A_2 \times \sin(2\pi(f_{baud} + \Delta f) + \phi_2) \quad (5.2)$$

If we pass the sine waves of Eqs. 5.1 and 5.2 through a non-linear element, we would get a DC term and another term at $2f_{baud}$. In the same manner, the coherent terms around $\frac{f_{baud}}{2}$ and $2f_{baud}$ will produce tones at f_{baud} , and $4f_{baud}$, respectively. By filtering tones at frequencies higher or lower than f_{baud} , we would be able to recover a clock whose frequency is equal to the baud rate of data, and has an arbitrary phase. The system shown in Fig. 5.3

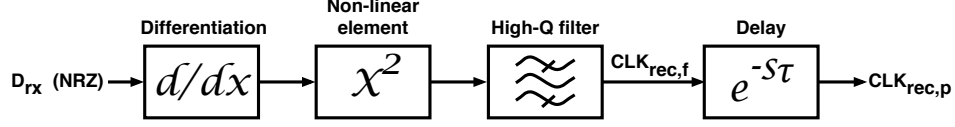


Figure 5.3: Block diagram showing the concept of high-Q filter based clock recovery

depicts the block diagram of such CR method. The signal is differentiated prior to mixing to equalize the amplitude of coherent terms, which in turn, maximizes the amplitude of the product. Note that the amplitudes of the peaks in Fig. 5.2 reduce with a -20 dB/dec slope. Thus, the zero provided by differentiation cancels out the pole and provides a flat response. If all undesired harmonics are filtered-out by the high-Q filter, the signal coming from this block, $CLK_{rec,f}$, is a clock with frequency of f_{baud} .

A delay block is used after the filtering stage to align the phase of the clock to the middle of UI (i.e., middle of the data eye), thus recovering $CLK_{rec,p}$, which is a clock with correct phase and frequency. The non-coherent terms produce tones that fall out of the bandwidth of the bandpass filter, hence being significantly attenuated. In this method, the quality factor of the filter should be very high (e.g., > 100) to sustain the oscillation even with long streams of a constant data. Therefore, this technique is called high-Q CR.

5.3 Monolithic high-Q clock recovery

While with a discrete implementation, the high-Q CR technique can operate at multi-Gb/s data rates, the high-Q filter does not lend itself to a monolithic

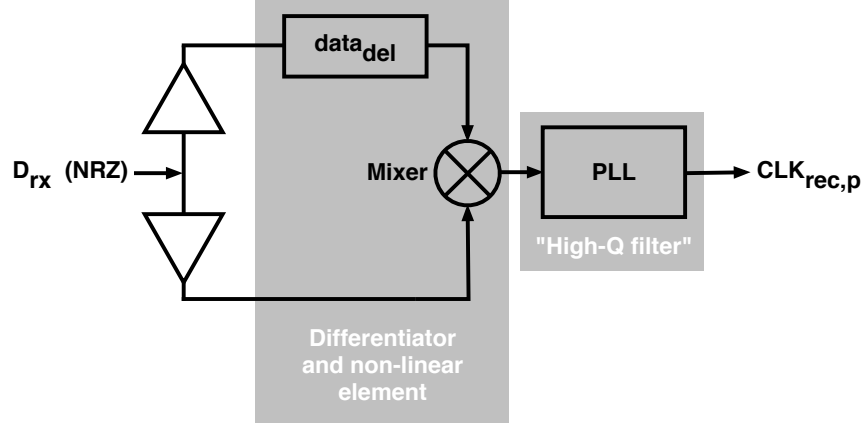


Figure 5.4: Block diagram of the monolithic high-Q CDR.

implementation. This is specially true in CMOS processes where due to the low resistance substrate, the Q of passive components is limited to < 10 at frequencies beyond 10 GHz [55, 60, 61]. However, a phase locked loop (PLL) with low closed loop bandwidth can mimic the response of a high- Q filter [62]. Instead of sustaining the oscillation using a passive filter, the architecture of Fig. 5.4 actively maintains the oscillation in $CLK_{rec,p}$, though a VCO. The combination of differentiation and non-linear processing is provided by splitting the received NRZ data, D_{rx} , delaying one version, and mixing it with the non-delayed version.

5.4 PLL-based clock recovery

While various CDR architectures have been discussed in literature (for an excellent review of CDR architectures refer to [63]), this Chapter is focused on full-rate PLL-based reference-less CDR architectures that use a mixer for linear phase detection. PLL-based CDRs can be categorized into two

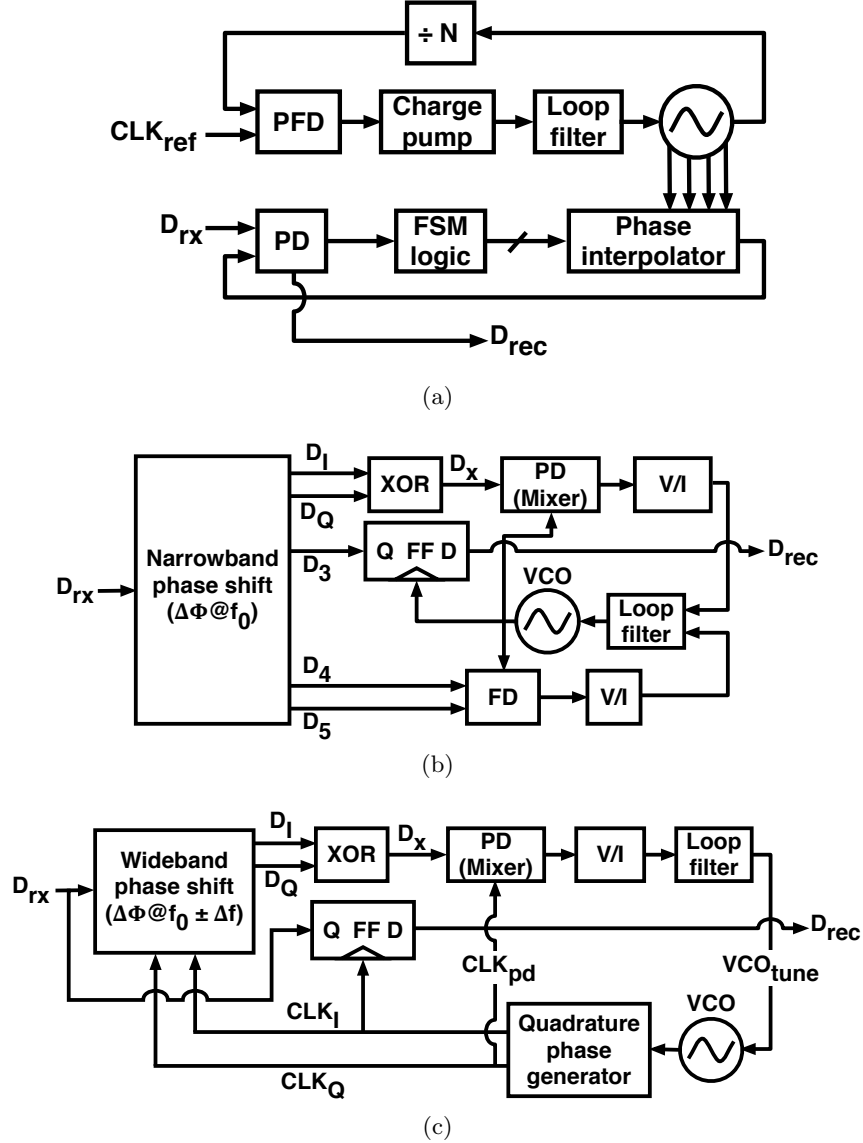


Figure 5.5: Phase-Interpolator-based CDR (a), conventional method of generating multiple data phases using delay elements, for mixer-based phase detection (b), wideband quadrature data phase generation in the proposed CDR (c). The blocks labeled as “V/I” and “FD” perform voltage-to-current conversion and frequency detection, respectively.

main groups: those that do not control VCO_{tune} , and those which adjust the phase and frequency of the clock by tweaking VCO_{tune} . A good example of the first group is phase-interpolator (PI) based CDR. Shown in Fig. 5.5a, such CDR interpolates among the quadrature phases provided by VCO, to adjust the phase of the PD clock. The frequency of the VCO is locked to multiples of an external reference using a secondary PLL loop.

Figure 5.5b shows a generic block diagram of the second group of PLL-based CDRs[64, 65], in which phase detection is performed using a mixer. A notable advantage of mixer-based phase detection is that unlike conventional linear phase detection methods [66], it does not require pulse generation and comparison for detection of the clock misalignment. Hence, mixer-based PDs are a suitable candidate for phase detection at data rates beyond 10 Gb/s [64]. In previous works, the various data phases required for equalization and phase/frequency detection are generated either actively through the delay of cascaded inverters [64, 65], or passively using emulated transmission lines [5]. In these methods, the phase shift is typically frequency dependent and thus the desired phase shift (e.g., 90°) is only achieved at or in a narrowband vicinity of a particular input frequency. In general, these conventional phase-shifters have a narrowband response and they are typically augmented by additional circuitry to adjust the phase shift. Note that the received data, D_{rx} , typically has a broadband spectrum; thus, the phase shifter should provide the desired phase shift over a wide frequency range which is a challenging task [55]. Additionally, if there is any variation between the nominal baud frequency, f_0 , (i.e., 12.5 GHz for 12.5 Gb/s data) and the actual baud frequency, f_{baud} , for example due to process, supply

or temperature (PVT) variations, the CDR performance will be degraded (e.g., additional jitter will be added to the data phases). In view of these challenges of conventional phase shifters, which typically have a narrowband response, we propose the architecture of Fig.5.5c. In this architecture, phase shifting of the data is achieved by first generating quadrature clock phases, CLK_I and CLK_Q , from the recovered clock; then, I/Q components of the received data, D_I and D_Q , are generated by means of mixing D_{rx} with CLK_I and CLK_Q . The proposed architecture applies a modified form of delay-based phase generation to the relatively narrowband recovered clock, as opposed to directly applying it to the broadband data.

Prior to discussing the details of the top-level block diagram of Fig. 5.7, first, we investigate the requirements and challenges of mixer-based phase detection.

5.5 Frequency doubling for mixer-based PD

In the CDR system of Fig. 5.5c, if we directly mix D_{rx} with CLK_{pd} ²⁶, we can write

$$V_{pd} = D_{rx} \otimes CLK_{pd} = \begin{cases} \frac{\alpha_1 \alpha_2}{2} [\cos(\frac{\omega t}{2} + \theta) + \cos(\frac{3\omega t}{2} + \theta)], & \Delta_D = 1 \\ \alpha_1 \alpha_2 \cos(\omega t + \theta), & \Delta_D = 0 \end{cases} \quad (5.3)$$

where $CLK_{pd} = \alpha_1 \cos(\omega t + \theta)$, $D_{rx} = \alpha_2 \cos(\frac{\omega t}{2})$, θ is the phase error in clock with respect to data eye center, and Δ_D is a binary (true/false) value that indicates whether data has a transition ('01' or '10') within 1 unit

²⁶For simplicity, the equations are only written for single-ended signals instead of differential signals.

interval (UI) of time t . It should be noted that in Eq. 5.3, the terms containing θ are practically zero as $\frac{3\omega}{2}$ and $\frac{\omega}{2}$ are well beyond the CDR loop bandwidth. In fact, due to the fairly low closed loop bandwidth, a DC term which is proportional to θ is desired as mixer output [64]. Such term can be generated by means of mixing CLK_{pd} and D_x , which the latter has a primary harmonic frequency equal to, and double of the frequency of primary harmonic in CLK_{pd} , and D_{rx} , respectively. For D_x , one can write

$$D_x = D_I \oplus D_Q = \begin{cases} \alpha_3 \cos(\omega t), & \Delta_D = 1 \\ \alpha_3, & \Delta_D = 0 \end{cases} \quad (5.4)$$

where $D_I = \alpha_3 \cos(\frac{\omega t}{2})$ and $D_Q = \alpha_3 \sin(\frac{\omega t}{2})$. Therefore, for the output voltage of the mixer V_{pd} we have

$$V_{pd} = D_x \otimes CLK_{pd} = \begin{cases} \frac{\alpha_1 \alpha_3}{2} [\cos(2\omega t + \theta) + \cos(\theta)], & \Delta_D = 1 \\ \alpha_1 \alpha_3 \cos(\omega t + \theta), & \Delta_D = 0 \end{cases} \quad (5.5)$$

which contains the phase error information in its DC term $\cos(\theta)$.

5.6 Implementation of mixer-based PD

Figure 5.6 shows the schematic of mixer-based PD. In this circuit, an active load is used to achieve both differential to single-ended conversion, and voltage-to-current conversion within the mixer [67]. As data and clock are applied to the gate and the source of the input devices, respectively; these devices operate within saturation and linear regions. Therefore, for the drain

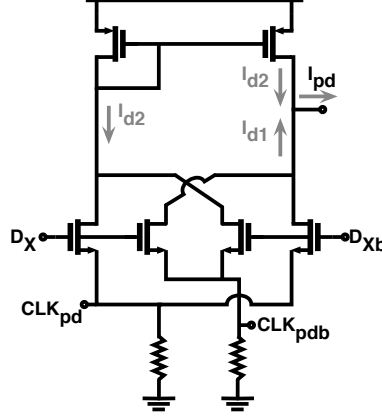


Figure 5.6: Schematic of the mixer used as phase detector.

current of device M_n , we can write

$$I_{dn} = \beta_1(v_{gs,n} - v_{th}) + \beta_2(v_{gs,n} - v_{th})^2 + \beta_3(v_{gs,n} - v_{th})^3 \quad (5.6)$$

where as an example, for device M_1 we have $v_{gs,1} = D_x - CLK_{pd}$. In the mixer, branch currents I_{d1} and I_{d2} add up at the output node and result in I_{pd} . Based on Eqs. 5.5 and 5.6, I_{pd} can be analytically written as

$$\begin{aligned} I_{pd} &= I_{d1} + I_{d2} \\ &\propto \begin{cases} 4\alpha_1\alpha_3\beta_2[\cos(4\pi f_{baud}t + \theta + \Phi_{opt}) + \cos(\theta - \Phi_{opt})], & \Delta_D = 1 \\ 8\alpha_1\alpha_3\beta_2[\cos(2\pi f_{baud}t + \theta)], & \Delta_D = 0 \end{cases} \end{aligned} \quad (5.7)$$

where θ represents the phase error in CLK_I with respect to the point in D_{rx} eye where the maximum vertical opening occurs, Φ_{opt} is a constant term representing the optimal phase offset (explained in Section 5.9). As the loop filter attenuates all components at 2ω and ω , for the phase detector

5.7. The proposed CDR architecture

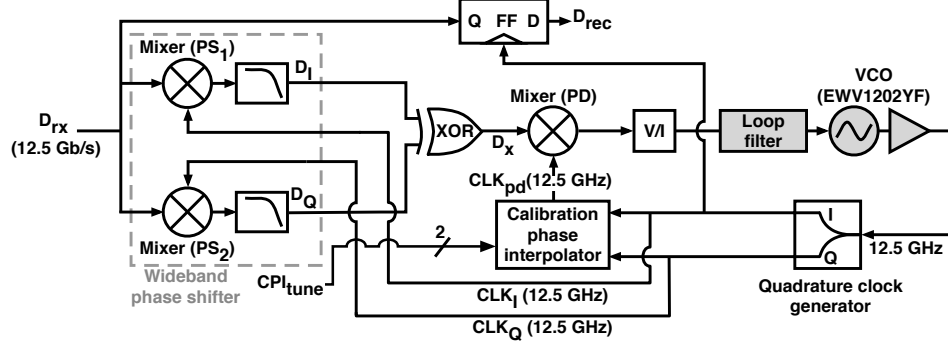


Figure 5.7: Detailed block diagram of the proposed CDR. In the proof-of-concept chip, the shaded blocks are off-chip.

characteristic, PDC , we can write

$$PDC \propto \cos(\theta - \Phi_{opt}). \quad (5.8)$$

Equation 5.8 reveals two important properties of the proposed architecture: First, among parameters β_1 , β_2 and β_3 ; only β_2 is present in I_{pd} . Thus, the phase error θ is measured while the devices operate in saturation. This is, indeed, a desired result for high-speed operation. Second, while no data transitions are present ($\Delta_D = 0$), I_{pd} will be silent; hence, it is not perturbing the VCO control voltage. The latter is crucial for minimizing clock jitter.

5.7 The proposed CDR architecture

Figure 5.7 shows the detailed block diagram of the proposed full-rate CDR topology, which uses a mixer as a linear PD. The shaded blocks are not integrated on the proof-of-concept prototype chip and are implemented off-chip.

5.7. The proposed CDR architecture

CLK_I , while PS_2 receives the quadrature clock component, CLK_Q . As fundamental harmonics of D_{rx} , CLK_I , and CLK_Q are at $f_{baud}/2$, f_{baud} , and f_{baud} , respectively; D_I and D_Q are signals whose fundamental harmonics are at $f_{baud}/2$ and are 90° separated in the time domain (or equivalently $\frac{1}{4 \times f_{baud}}$). As shown in Fig. 5.8, to avoid undesired higher frequency harmonics to reach the XOR and PD, and being down-converted to a frequency within the CDR loop bandwidth, second-order LC low-pass filters are used at the output nodes of the differential mixer [55].

To improve clock edge alignment and data recovery, CLK_{pd} and the CLK_I - CLK_Q pair should maintain a certain constant phase offset, Φ_{off} , relative to each other. As explained in section 5.9, the value of Φ_{off} depends on the amount of channel loss, or equivalently the post-equalization residual ISI in D_{rx} . Therefore, a calibration phase interpolator (CPI) is used to provide Φ_{off} , by interpolating between CLK_I and CLK_Q . Note that unless the channel is considerably time-variant, the CPI tuning signal, CPI_{tune} , needs to be adjusted once, at the startup cycle of the CDR operation. On-chip realization of a DSP-based calibration loop [70, 71] was beyond the scope of this work; therefore, for the purpose of testing the prototype chip, CPI_{tune} is manually set based on the loss of the channel used to transmit the data to the chip.

To confirm the potential of such architecture in tracking moderate frequency offsets without the help of a frequency detector, a single-loop topology is used in the implementation of the proposed CDR. If a wider frequency tracking range is required, the CDR architecture of Fig. 5.7 can be modified by adding a second loop containing a frequency detection mechanism and

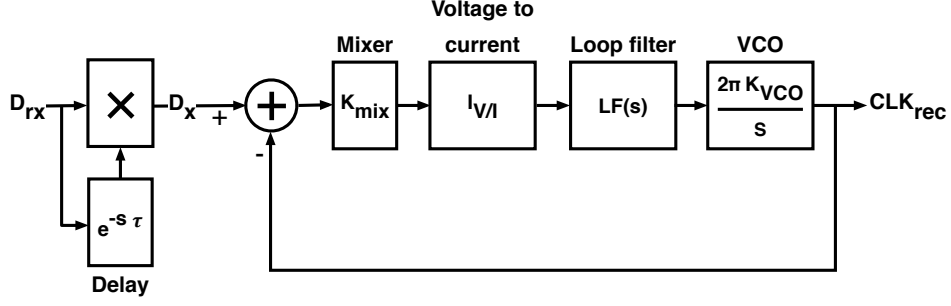


Figure 5.9: Linearized model of the proposed CDR.

transforming it to a dual-loop architecture.

5.8 Design of system-level parameters

For purpose of system level design, we simplify the CDR architecture of Fig. 5.7 to the feedback system shown in Fig. 5.9. If we approximate the recovered clock, CLK_{rec} , with a sinusoidal waveform, then we can write

$$CLK_{rec} = A_{clk} \times \sin(2\pi f_{baud} + \Phi_{clk}) \quad (5.9)$$

Depending on the amount of ISI and the bandwidth of the XOR gate, the up-converted data (output of XOR gate), D_x , can vary in form from an ideal square wave to a sine wave. Hence considering these two extremes we can write

$$D_x = \begin{cases} A_x \times \sin(2\pi f_{baud} + \Phi_x), & \text{sinusoidal} \\ A_x \times \text{sgn}(\sin(2\pi f_{baud} + \Phi_x)), & \text{square wave} \end{cases} \quad (5.10)$$

where $|D_x|$, and Φ_x are the amplitude and phase of up-converted data at a given time.

$$K_{mix} = \begin{cases} \frac{A_x A_{clk}}{2}, & \text{sinusoidal } D_x \\ \frac{2A_x A_{clk}}{\pi}, & \text{square wave } D_x \end{cases} \quad (5.11)$$

For the open loop transfer function, $OLTF(s)$, we can write

$$OLTF(s) = \frac{D_x(s)}{CLK_{rec}(s)} = \frac{2\pi K_{mix} |I_{v/i}| K_{vco} LF(s)}{s} \quad (5.12)$$

and the closed loop transfer function, $CLTF(s)$, can be written as

$$CLTF(s) = \frac{OLTF(s)}{1 + OLTF(s)} \quad (5.13)$$

5.8.1 Loop filter

There are two important design parameters associated with the loop filter of an analog CDR (or PLL), namely type, and order. The type of a CDR loop is regarded as the number of integrators in the $OLTF(s)$. The minimum type is ‘I’ as the VCO provides one integration, i.e. the ‘s’ in denominator of Eq. 5.12. The order is referred to the roll-off factor in $CLTF(s)$.

In this work, a type II architecture is utilized for the closed loop system to achieve a high DC closed loop gain, which in turn results in consistent steady state phase error. Additionally, having a second integration in the loop filter in addition to the integration provided by VCO, allows to use the entire tuning range of VCO. Therefore, the loop filter is designed as shown in Fig. 5.10. The transfer function of the loop filter, $LF(s)$ can be written

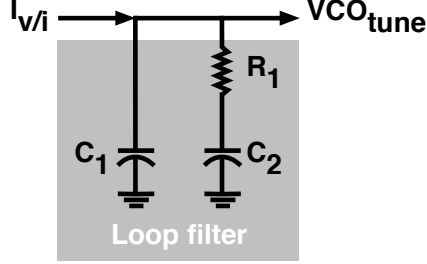


Figure 5.10: Type II, order 2 loop filter, as used in the proposed CDR.

as

$$LF(s) = \frac{VCO_{tune}(s)}{I_{v/i}(s)} = \frac{1 + sR_1C_2}{s(C_1 + C_2)(1 + sR_1C^*)} = \frac{K_{lf} \times (1 + \frac{s}{2\pi f_z})}{s \times (1 + \frac{s}{2\pi f_p})} \quad (5.14)$$

where C^* and the gain of loop filter, K_{lf} are given by

$$C^* = \frac{C_1C_2}{C_1 + C_2} \quad (5.15)$$

$$K_{lf} = \frac{\beta}{2\pi K_{vco}K_{mix}|I_{v/i}|} \quad (5.16)$$

and for β , and f_p we can write

$$\beta = \frac{2\pi^2 \times CDR_{bw} \times Q}{\frac{Q}{CDR_{bw}} + \frac{1}{f_z} - \frac{1}{Q \times CDR_{bw}}} \quad (5.17)$$

$$f_p = CDR_{bw} \times \left(\frac{1}{Q} + \frac{Q \times f_z}{Q \times CDR_{bw} - f_z} \right) \quad (5.18)$$

5.8. Design of system-level parameters

where CDR_{bw} , Q , f_z , and f_p are CDR closed loop bandwidth, loop filter quality factor, zero frequency, and pole frequency, respectively.

To avoid a large peaking in the $CLTF(s)$ frequency response, and hence potential instability, f_z is chosen such that

$$\frac{f_z}{CDR_{bw}} < \frac{1}{10} \quad (5.19)$$

Based on Eqs. 5.14 to 5.19, the values of loop parameters are chosen as indicated in Table 5.1

Table 5.1: VALUES OF LOOP PARAMETERS

Symbol	Description	Value
CDR_{bw}	loop bandwidth of CDR	6.5 MHz
β	numerator in Eq. 5.16	6.112e+13
f_p	pole frequency	9.544 MHz
f_z	zero frequency	0.325 MHz
f_z/CDR_{bw}	ratio of zero frequency to the closed loop bandwidth	0.05
K_{lf}	DC gain of loop filter	2.528e+7

5.8.2 System-level performance

Based on the values given in Table 5.1, the simulated frequency response of the closed loop CDR is shown in Fig. 5.11, which illustrates the predicted roll-off factor of -40 dB/dec. The integrations in VCO and loop filter each contribute -20 dB/dec.

In optical standards such as OC192 [72], the amount of peaking should remain below 0.1 dB over all frequencies. Such stringent requirement is due to the fact that in typical usage, numerous CDRs are used along a long-

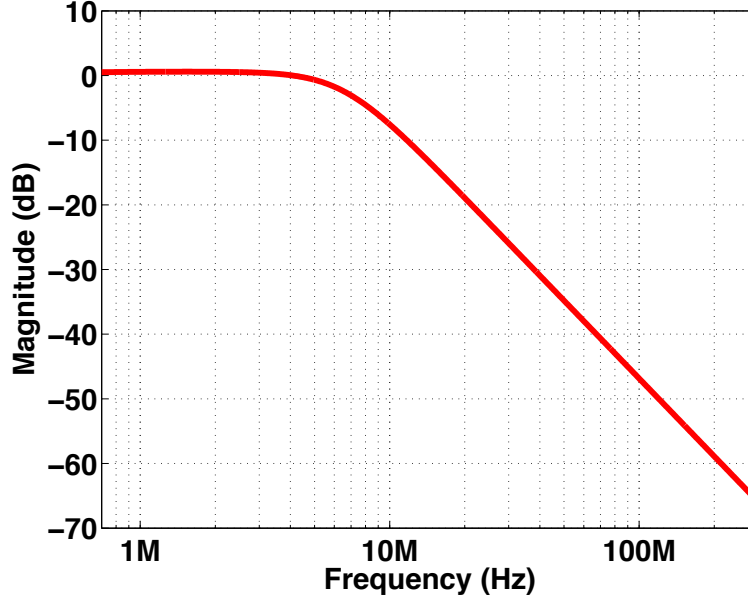


Figure 5.11: Frequency response of the closed loop CDR.

haul fiber channel to repeat the signal and avoid signal loss at the RX end of channel. As the CDRs are cascaded, the peaking amounts add-up in frequency domain, which can potentially make the overall system unstable. Figure 5.12 reveals the step response of the CDR. The amount of overshoot in the step response has a direct relationship with the value of $\frac{f_z}{CDR_{bw}}$. Figure 5.13 shows the response of CDR to an abrupt change in the data rate, DR , of the received data. As DR changes from the nominal value of 12.5 Gb/s to the offset data rate of 12.6 Gb/s, the CDR demonstrates an unstable response known as cycle slipping, during which gradually adjusts the VCO frequency. While cycle slipping, the frequency of VCO is constantly changing in a non-monotonic fashion. Therefore, during such period the CDR is prone to making bit decision errors. The duration of cycle slip has an inverse

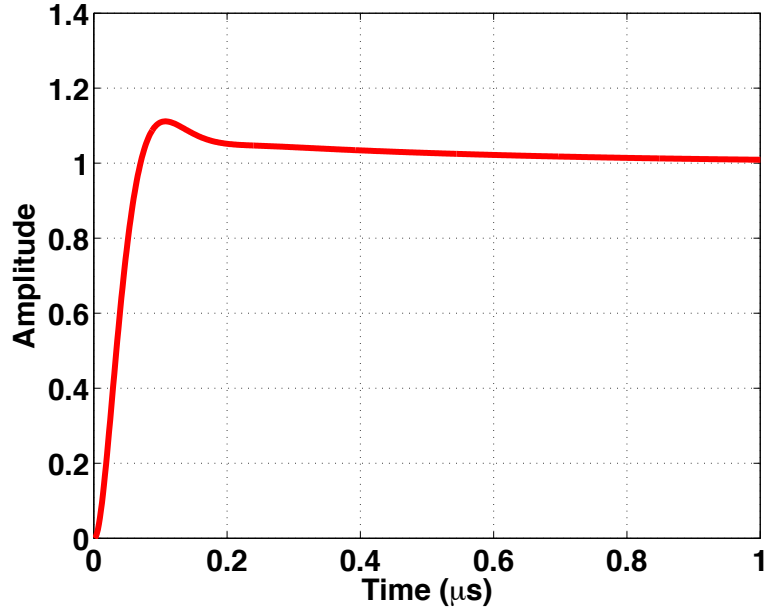


Figure 5.12: Step response of the CDR.

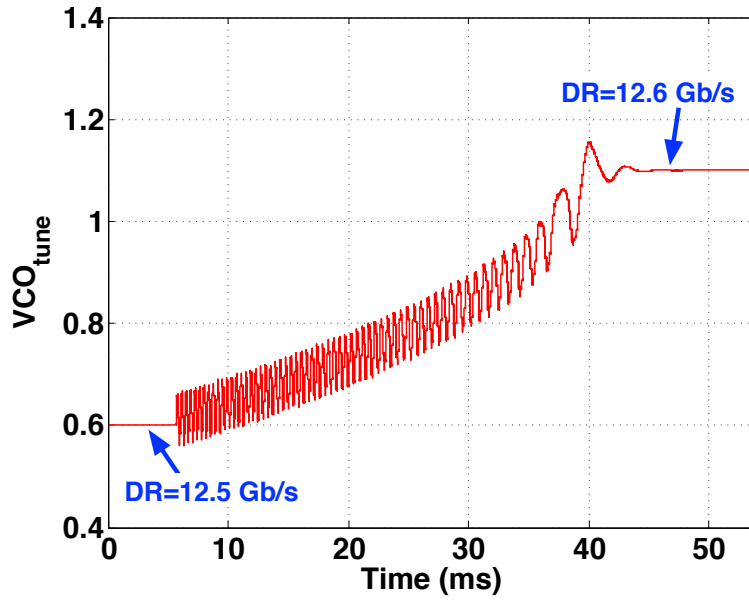


Figure 5.13: Frequency locking behavior of the CDR when the DR is switched from 12.5 Gb/s to 12.6 Gb/s.

relationship with CDR_{bw} .

5.9 Calibration phase interpolator

Depending on the channel frequency response, the optimal position for sampling the data (where maximum vertical eye opening occurs) can deviate from the center of the unit interval [71]. Figure 5.14a shows normalized PDC graphs for various values of channel loss. To obtain each PDC graph, the CDR feedback path is opened and the phase of CLK_{pd} is swept with respect to phase of CLK_I , while the sampling edge of CLK_I is forced to align with the optimal sampling point of D_{rx} . As these PDC graphs are plotted for the optimal sampling point, the vertical axis is labeled as PDC_{opt} . Also, the zero crossing of each PDC graph is denoted as Φ_{opt} . The horizontal axis of Fig. 5.14a represents the phase offset between CLK_{pd} and CLK_I , Φ_{off} . It can be observed that within a π domain of Φ_{off} values, for each PDC graph, there is only one point²⁷ for which we have $\Phi_{off} = \Phi_{opt}$. Note that the PD error signal at Φ_{opt} is zero, hence, it is the only point at which CDR can sustain lock. For other values of Φ_{off} such that $\Phi_{off} \neq \Phi_{opt}$, the closed loop CDR may still lock to a certain point of the D_{rx} eye; however, such point would be sub-optimal. If we plot Φ_{opt} versus different values of channel loss, we would get the graph of Fig. 5.14b, which demonstrates that Φ_{opt} is a strong function of the channel loss (or residual ISI in D_{rx}), an undesired result indeed. Therefore, using CPI block, we allow a degree of freedom in CLK_{pd} , through Φ_{off} , to decouple it from CLK_I (CLK_Q). By adjusting

²⁷The other point in the 2π domain flips the polarity of PDC in Eq. 5.8.

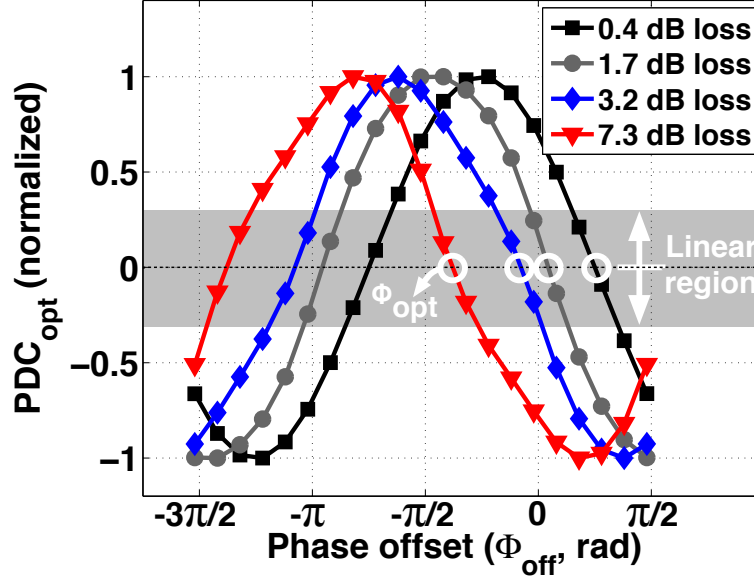
CPI_{tune} , one can interpolate between CLK_I and CLK_Q to generate the desired phase shift, $\Phi_{off} = \Phi_{opt}$. For a constant BER, such calibration technique allows for tolerating more residual ISI in D_{rx} , and hence lower power consumption in equalizer [53]. Note that in the conventional CDR of Fig. 5.5b, although D_I and D_Q are decoupled from CLK_{pd} , the integrity of the 90° phase shift between D_I and D_Q still depends on the frequency content of D_{rx} , e.g., the magnitude of the harmonics in D_{rx} ; therefore, conventional CDR of Fig. 5.5b is more sensitive to under/over equalization of D_{rx} .

5.10 Performance of QCG block

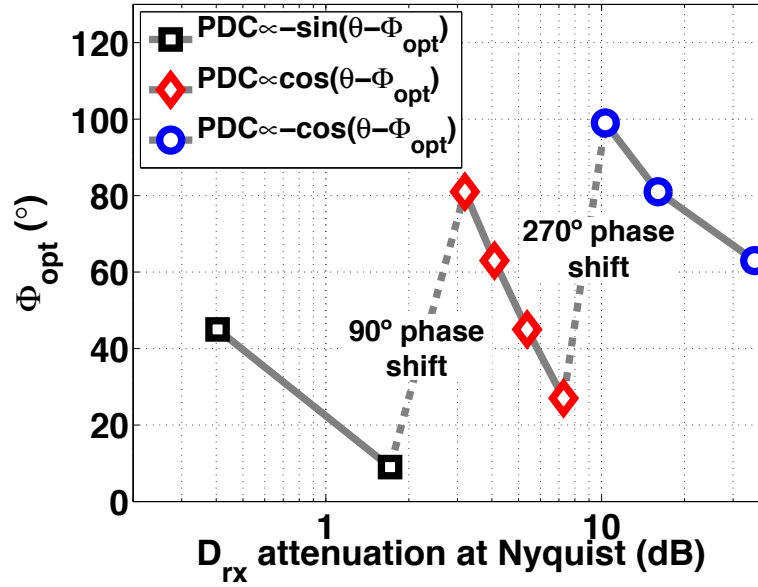
Figure. 5.15a shows the Monte Carlo simulations of RMS phase jitter of the quadrature phases in cascaded inverters, QPS without QPC²⁸, and QPS with QPC. The addition of the QPC sub-block enhances the quality of the quadrature phases by reducing the RMS phase jitter due to deterministic variations in the delay of inverters (e.g., due to mismatches in layout). However, cascading more than one quadrature phase correction stage (QPC) is avoided due to area considerations, and the fact that the overall jitter in clock phases will gradually become dominated by the random noise of the inverters.

As QCG block is located in CDR's feedback path, the quality of the generated clock phases directly affects the CDR performance in phase detection and frequency tracking. In particular, in the presence of a frequency offset

²⁸note that throughout this manuscript, the cascaded combination of QPS and QPC sub-blocks are called "quadrature phase generator" (QPG).

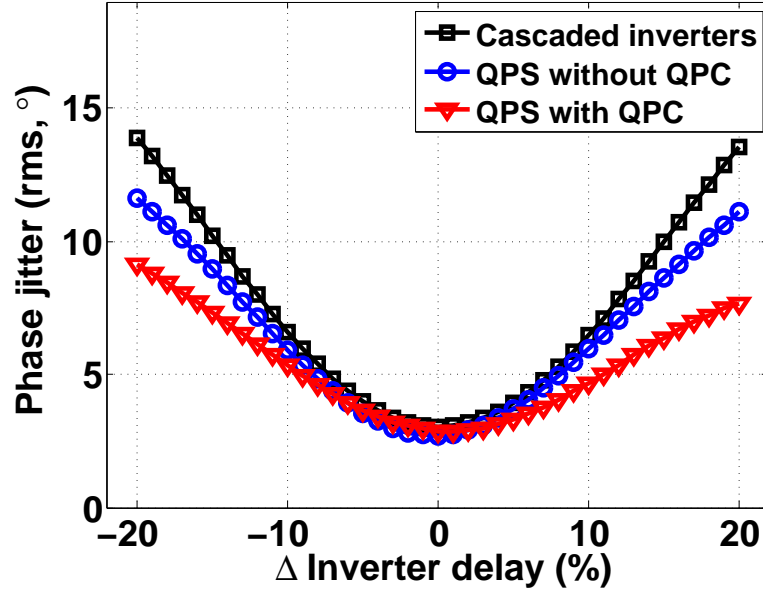


(a)

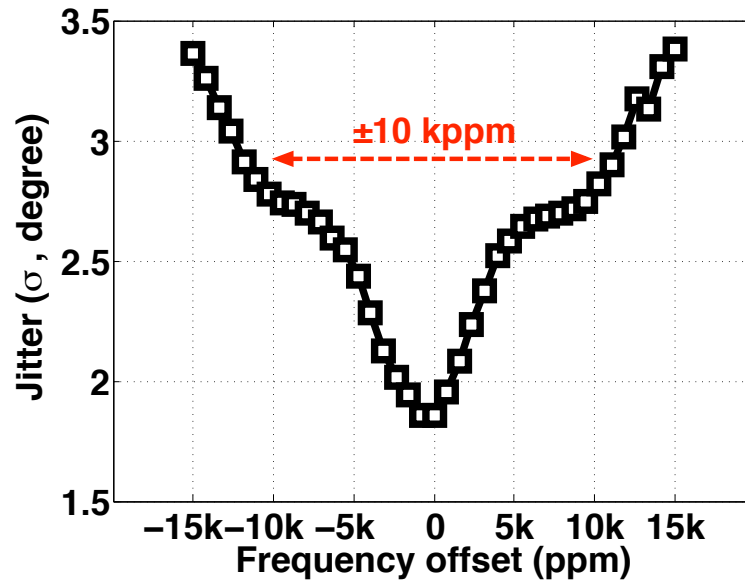


(b)

Figure 5.14: Normalized PDC_{opt} as a function of Φ_{off} (a). Variation in Φ_{opt} due to various amounts of channel loss (b).



(a)



(b)

Figure 5.15: Phase jitter in generated clock phases as a function of inverter delay variation (a). Jitter performance of QCG versus offset from f_0 (b).

between TX PLL and RX CDR, QCG should be able to provide low-jitter phases over the part of VCO tuning range that falls within the operation range of the CDR. Figure 5.15b shows the standard deviation of jitter in outputs of QCG versus frequency offset from f_0 (i.e., nominal f_{baud}). As can be seen from the figure, the QCG block achieves a satisfactory performance within ± 10 kppm offset from f_0 of 12.5 GHz. Note that this value sets the upper limit for the frequency tracking range of the overall CDR. Figure 5.16 compares the power spectral density (PSD) of the signal D_x , when D_I and D_Q are generated using the conventional narrowband phase shifting method, and the proposed wideband phase shifting method. In respect to the desired harmonic at 12.5 GHz, the PSD graphs of the conventional and proposed phase shifting methods reveal jitters of 4 ps_{rms} and 2.32 ps_{rms} in D_x , respectively.

5.11 Experimental results

The chip is designed and fabricated in a 90-nm CMOS technology. Figure 5.17 shows the die micrograph which occupies 0.98×0.84 mm² excluding the pads. As mentioned earlier, the chip integrates all the non-shaded blocks shown in Fig. 5.7. The CDR's loop bandwidth is set to about 6.5 MHz through the external second-order type-II loop filter. In order to close the CDR loop, an external VCO (Endwave EWV1202YF) is controlled by filtered output of PD, to provide the recovered differential clock back to the test-chip. The VCO provides ± 0.25 GHz of symmetrical tuning range around an f_0 of 12.5 GHz. The free running phase noise of VCO is mea-

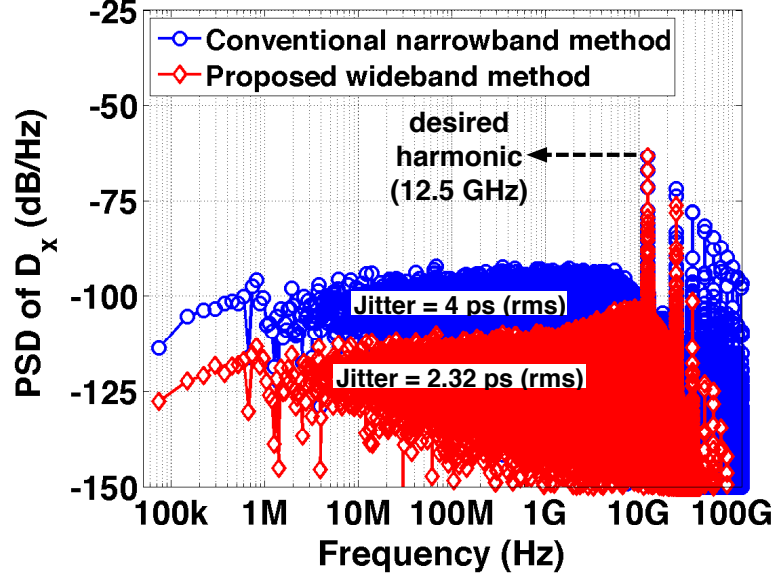


Figure 5.16: Comparison of power spectral densities of D_X , while D_I and D_Q are once generated similar to [64], and then through the proposed wideband phase shifting method.

sured to be -106 dBc/Hz at 100 kHz offset. A $2^{31} - 1$ PRBS data pattern with 4.1 dB attenuation at 6.25 GHz is fed to the chip through high-speed probes. The measured eye diagram of the recovered data is shown in Fig. 5.18, which has a vertical eye-opening of 283 mV. The edges of the eye diagram are rounded due to the bandwidth limitation of the equipment (Agilent DSO81304A). To verify the integrity and robustness of the proposed CDR, jitter tolerance is measured with a BER threshold of 10^{-12} . Figure 5.19 illustrates the jitter tolerance performance which satisfies the extrapolated OC-192 mask. The CDR achieves a BER of $< 10^{-12}$ over a range of 212.5 Mb/s (± 8.5 kppm), while on-chip components consume 84 mW from a 1.2 V supply. Table 5.2 summarizes the performance of

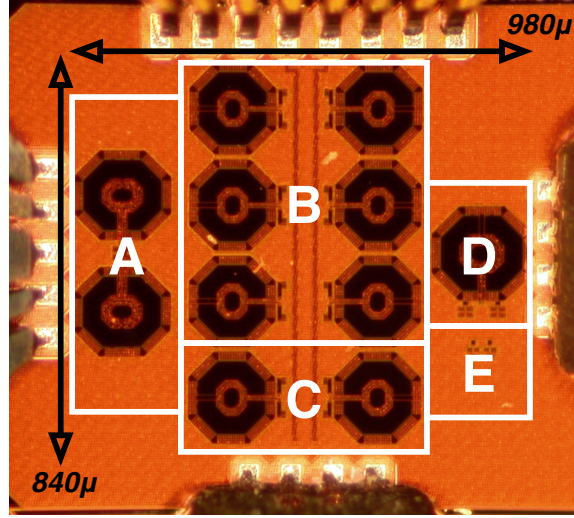


Figure 5.17: Die micrograph of the prototype chip implemented in 90-nm CMOS; where the blocks A, B, C, D, and E are dynamic phase shifter, quadrature clock generator, phase interpolator and buffering, XOR gate, and phase detector.

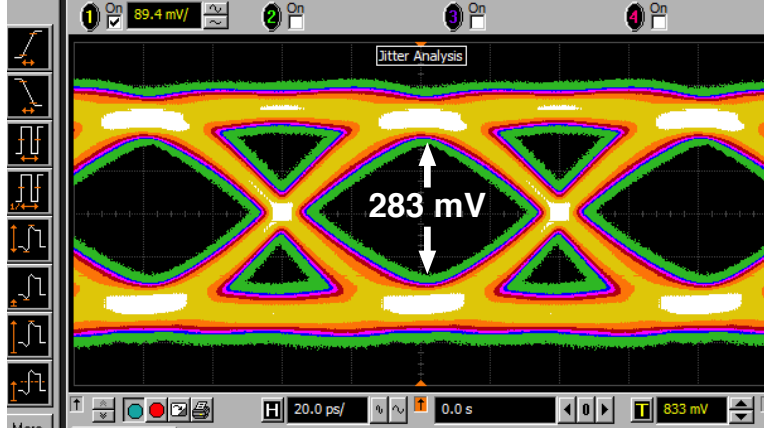


Figure 5.18: Measured eye diagram of the recovered data.

this work and compares it with recently published CDRs. Note that the proof-of-concept implementation of the proposed CDR utilizes a single-loop architecture; A wider operation range may be achieved by using a frequency

tracking mechanism similar to [64] and [5]. However, even with a single-loop implementation, the operation range of this work outperforms those of [24] and [66]. As seen in Table 5.2, this work has a better power consumption FoM compared to [5, 64, 66, 73]. Although, [24] reports a lower FoM, it should be noted that it is fabricated in faster CMOS process (i.e., 65 nm versus 90 nm in this work) while operating at a lower data rate; additionally, [24] doesn't include an on-chip VCO.

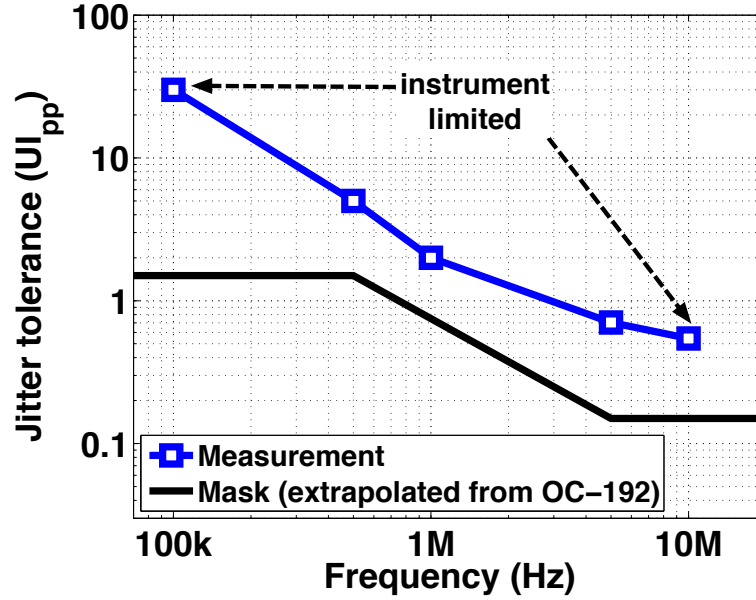
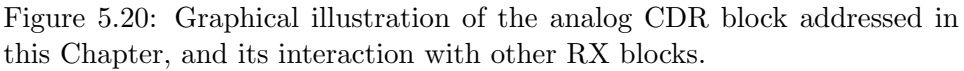


Figure 5.19: Measured jitter tolerance.

5.12 Chapter summary

A wideband technique for quadrature data phase generation at multi-Gb/s data rates is demonstrated. Based on the proposed technique, an analog CDR architecture employing a mixer-based PD is proposed. Figure 5.20



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Table 5.2: PERFORMANCE SUMMARY AND COMPARISON

	JSSC 2009 [64]	TCAS-II 2011 [73]	JSSC 2012 [5]	JSSC 2012 [24]	TCAS-I 2012 [66]	This work [74]
Technology (nm)	90	130	65	65	180	90
Supply (V)	1.5	1.5	1.6	1	1.8	1.2
Data rate (Gb/s)	20	16	40	10	5	12.5
CDR loop BW (MHz)	10	4	2.4	10	N/A	6.5
Operation range (ppm)	$\pm 23.75k$	N/A	$\pm 30k^a$	± 350	$\pm 244^b$	$\pm 8.5k$
Architecture	Dual-loop, Full-rate	Dual-loop, Half-rate	Dual-loop, Quarter- rate	Dual-loop, Half-rate	Dual-loop, Quarter-rate	Single- loop, Full-rate
PD type	Linear (Mixer- based)	Bang-Bang	Linear (Mixer- based)	Bang-Bang	Linear	Linear (Mixer- based)
Clocking scheme: (# of phases) \times {GHz}	$(2) \times \{20\}$	$(4) \times \{8\}$	$(4) \times \{10\}$	$(4) \times \{5\}$	$(4) \times \{1.25\}$	$(4) \times \{12.5\}$
Power (mW)	154	160	520	45	71.9	84 ^c
mW/(Gb/s) FoM	7.7	10	13	4.5	14.38	6.72 ^c
Area (mm ²)	0.853	0.134	1.147	1.7	4.37	0.823

^a The symmetrical operation range around nominal data rate is reported here.^b Using the PD loop only.^c Excludes off-chip components.

Chapter 6

Hardware-efficient eye monitoring technique for clock and data recovery

Owing to flexibility and power efficiency of digital signal processing techniques, digital clock and data recovery has become a prominent choice in serial link receivers that operate based on IEEE 802.3-2008 group of standards, where data rates are equal to, or below 10 Gb/s [75]. However, at higher data rates as mandated by IEEE 802.3-ba/bg standards, realization of a full-rate DSP-based architecture is subject to feasibility of high-speed and relatively low-power signal quantization and processing at RX. While at data rates beyond 10 Gb/s a flash analog-to-digital converter is usually used at the front-end of DSP-based RX, the high power consumption of the comparator array is a major design concern [23]. In this Chapter, we propose a digital phase detection technique that utilizes four comparators to extract timing information from data transitions within a window of three consecutively received data bits.

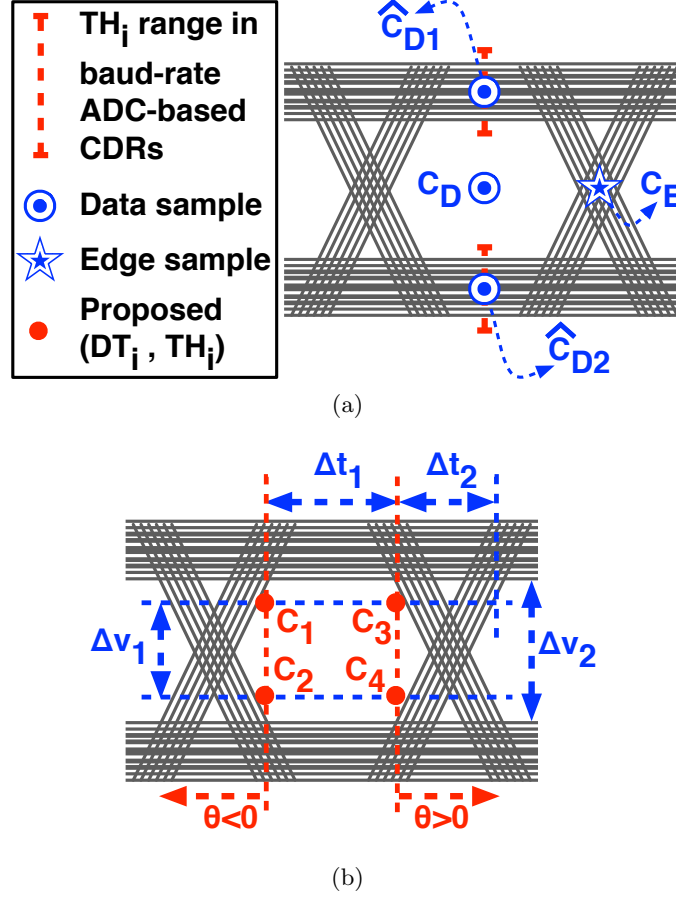


Figure 6.1: The arrangement of DT_i and TH_i for comparators in binary and ADC-based CDRs (a), and the arrangement in proposed CDR (b).

6.1 Digital clock recovery methods

Considering the decision time of comparators, DT_i , where i is the identifying tag of each comparator, conventional digital clock recovery methods fall into two categories, namely, baud-rate or over-sampling. In the former, during each unit interval data is sampled once, whereas in the latter, sampling is performed at multiple time instances within each UI. Additionally, based

on the number of comparators with different decision thresholds, TH_i , CR schemes can be regarded as either binary, where there is only one comparison threshold, or ADC-based, where there are more than one comparison thresholds. Two well-known combinations of DT_i and TH_i , are Alexander (Bang-Bang) [76] and Mueller-Muller [33]; where the former is binary and usually 2×-oversampled, and the latter is ADC-based and baud-rate. As noted on the conceptual eye diagram of Fig. 6.1a, in Mueller-Muller CR, \hat{C}_{D1} and \hat{C}_{D2} represent two groups of data-sampling comparators that operate in the vicinity of the data levels. However, in Alexander CR, C_D is a single data-sampling comparator and C_E is a single edge-sampling comparator.

6.2 Proposed CDR technique

Figure 6.1b shows the decision coordinates, (DT_i, TH_i) , of four comparators, $C_{i,i=1:4}$, as used in this work to monitor the equalized received data, D_{eq} ; where

$$\Delta t_1 = DT_3 - DT_1 = DT_4 - DT_2 \quad (6.1)$$

$$\Delta t_1 + \Delta t_2 = 1UI \quad (6.2)$$

$$\Delta v_1 = TH_1 - TH_2 = TH_3 - TH_4 \quad (6.3)$$

6.2. Proposed CDR technique

Table 6.1: PHASE DETECTION TRUTH TABLE FOR THE ARRANGEMENT SHOWN IN FIG.6.1B.

	$C_1C_2C_3C_4$				
		$\Delta_{t1} \begin{matrix} \leq \\ \geq \end{matrix} \Delta_{t2}^b$		$\Delta_{t1} > \Delta_{t2}$	
Data ^a	$\theta = 0$	$-\Delta_{t2} \leq \theta < 0$	$0 < \theta \leq \Delta_{t2}$	$\theta < -\Delta_{t2}$	$\theta > \Delta_{t2}$
000	0000	0000	0000	0000	0000
001	0000	0000	0001	0000	0011
010	1111	0111	1101	0011	1100
011	1111	0111	1111	0011	1111
100	0000	0100	0000	1100	0000
101	0000	0100	0001	1100	0011
110	1111	1111	1101	1111	1100
111	1111	1111	1111	1111	1111

^a $b_{n-1}b_nb_{n+1}$ ^b Δ_{t1} less than, equal to, or larger than Δ_{t2}

θ is the phase error, and Δv_2 is the vertical eye opening in D_{eq} . Note that the coordinates (DT_i, TH_i) are essentially defined by Δt_1 and Δv_1 values. Each comparator samples D_{eq} once in every UI. Such arrangement enables extracting timing information from data transitions within a 3-UI window of consecutively received data bits denoted by $b_{n-1}b_nb_{n+1}$. At the n^{th} UI, the binary representation of analog signal D_{eq} , b_n , is the current bit, b_{n-1} is the previous bit, b_{n+1} is the next bit, and $C_1C_2C_3C_4$ is the 4-bit word formed by the binary decisions of the four comparators. The phase detection (PD) truth table for the comparator arrangement of Fig. 6.1b is provided in Table 6.1. Column 1 shows the eight possible values for the 3-bit word $b_{n-1}b_nb_{n+1}$. Column 2 ($\theta = 0$) represents the phase-locked state, columns 3 and 4 ($0 < |\theta| \leq \Delta_{t2}$) represent the vicinity-of-lock state, and columns 5 and 6 ($|\theta| > \Delta_{t2}$) represent the out-of-lock state. While the $C_1C_2C_3C_4$ words in columns 3 and 4 are true for all possible relationships between Δt_1

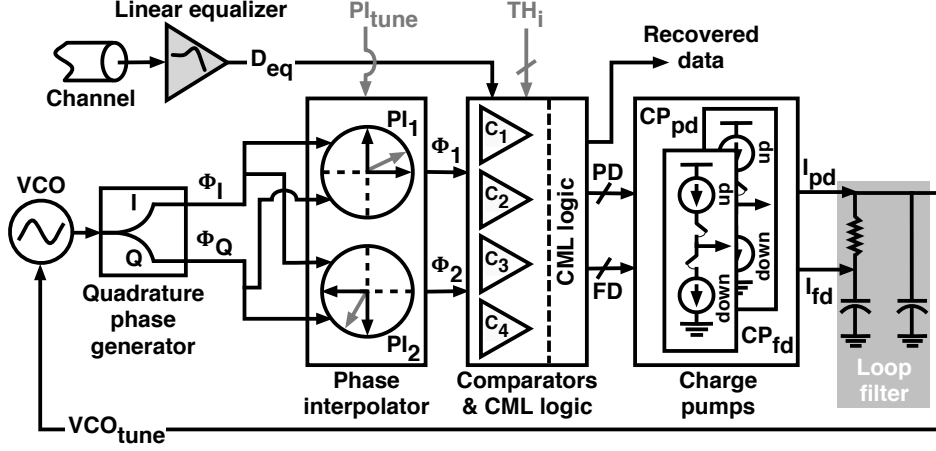
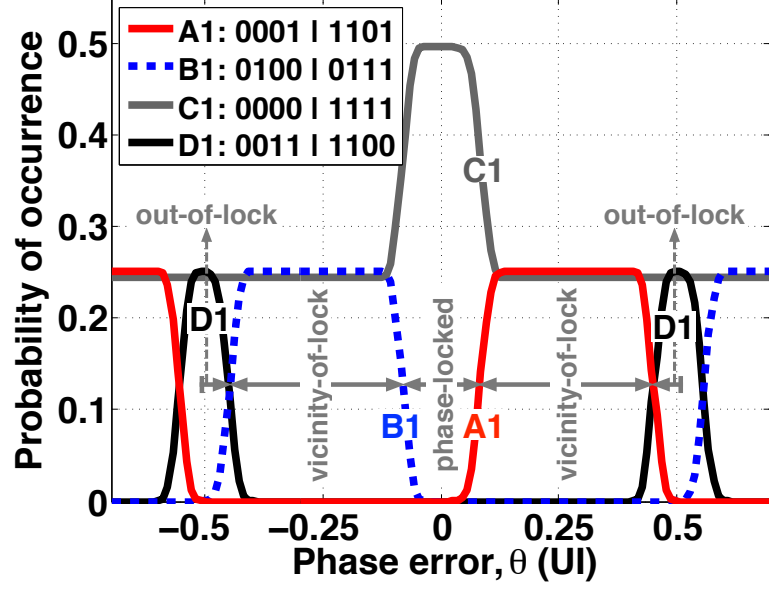


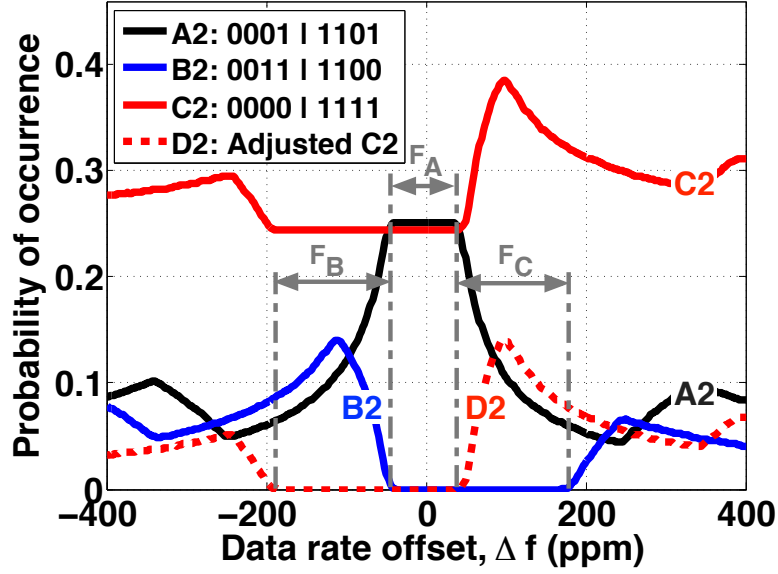
Figure 6.2: The proposed CDR architecture; shaded blocks and signals are off-chip.

and Δt_2 , as explained later, only $\Delta t_1 > \Delta t_2$ is used in this work. To detect all possible timing scenarios using the $b_{n-1}b_nb_{n+1}$ sequence, the amount of ISI equalization prior to phase detection should be enough to cancel the significant pre-cursor and post-cursor ISI taps, except the first pre-cursor tap, h_{-1} , and first post-cursor tap, h_1 , in the channel impulse response. However, if $|h_{-1}|$ and $|h_1|$ are too large, i.e., with a magnitude comparable to that of the main tap of the channel, $|h_0|$, a portion of them should be canceled by the equalizer to open D_{eq} eye such that (DT_i, TH_i) coordinates can be set within the eye as in Fig. 6.1b. The specifications of Δv_1 and Δt_1 are discussed later in this Chapter.

The architecture of the proposed full-rate CDR is shown in Fig. 6.2. A quadrature phase generator [57, 68] is used to split the differential clock from VCO into in-phase, Φ_I , and quadrature, Φ_Q , components that are 90° out of phase. Subsequently, the differential clock phases Φ_1 and Φ_2 that are needed



(a)



(b)

Figure 6.3: Phase detection characteristic (a), and frequency detection characteristic of the proposed CDR (b).

6.2. Proposed CDR technique

for setting $DT_{1,2}$ and $DT_{3,4}$ are generated by the phase interpolator block which consists of two phase interpolator sub-blocks, namely, PI_1 and PI_2 . Both PI_1 and PI_2 share the external tuning current PI_{tune} ; however, PI_1 interpolates between Φ_I and Φ_Q , while PI_2 interpolates between $\overline{\Phi_I}$ and $\overline{\Phi_Q}$. $\overline{\Phi_I}$ and $\overline{\Phi_Q}$ represent 180° out-of-phase versions of Φ_I and Φ_Q , respectively. With this approach, Φ_1 and Φ_2 can be tuned such that $90^\circ < \Phi_2 - \Phi_1 < 270^\circ$. Note that

$$\Phi_2 - \Phi_1 = \Delta t_1 \times \frac{360^\circ}{1UI} \quad (6.4)$$

Figure 6.4a shows the schematic of the PIs. The bias voltages V_{b1} and V_{b2} are generated using the PI control circuit shown in Fig. 6.4b. The main function of the control circuit is to generate a differential signal from the current PI_{tune} .

The $C_1C_2C_3C_4$ word is processed by phase detection and frequency detection (FD) logic to control the up/down signals of PD charge pump, CP_{pd} , and FD charge pump, CP_{fd} . While CDR is in the vicinity-of-lock state (columns 3 and 4 in Table 1), data recovery, i.e., recovering b_n , is done based on a majority vote among C_1 to C_4 ; i.e., the current bit (b_n) is ‘1’ (‘0’) if the majority of bits in $C_1C_2C_3C_4$ word are ‘1’ (‘0’). The logic block is implemented using current-mode logic (CML) gates. I_{pd} and I_{fd} , which are the output currents of CP_{pd} and CP_{fd} , are averaged using the CDR loop filter, and adjust the control voltage of oscillator, VCO_{tune} . Figs. 6.3a and 6.3b show the PD and FD characteristics of the proposed CDR, respectively. Each graph in these figures is associated with two values for

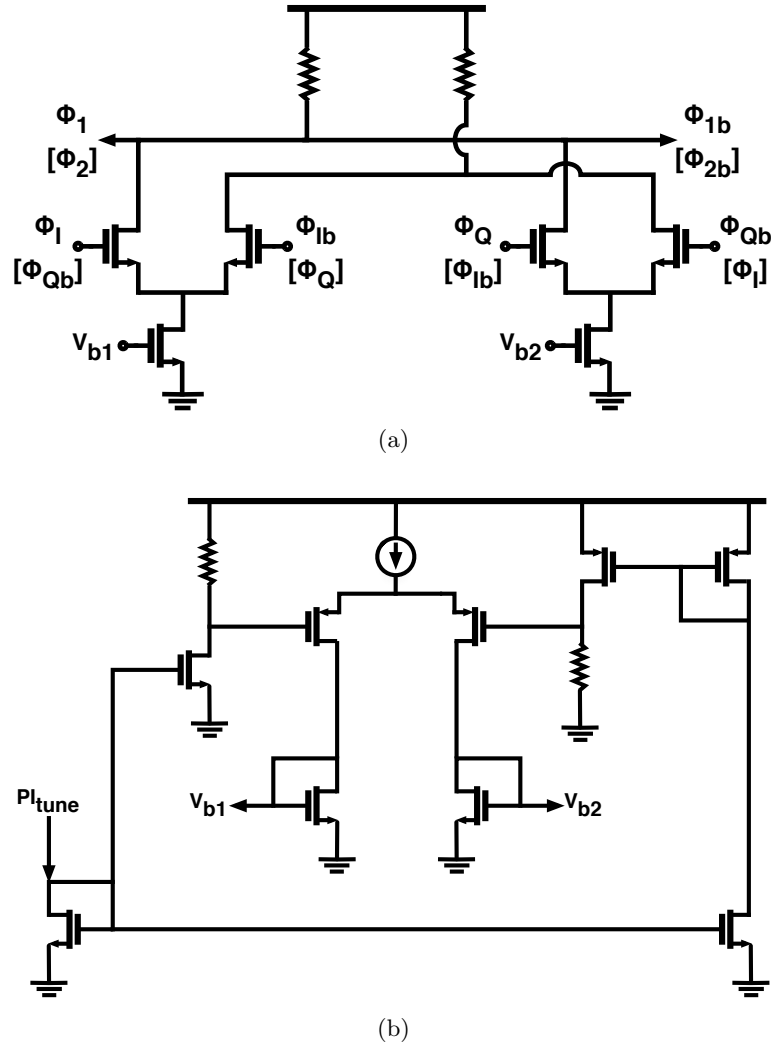


Figure 6.4: The schematic of PI_1 and $[PI_2]$ (a), and the control circuit for PIs (b).

$C_1C_2C_3C_4$, as one relates to ‘0’→‘1’ data transition and the other relates to ‘1’→‘0’ transition. In Fig. 6.3a, the words whose probability of occurrence (PO) is shown in graphs $A1$ and $B1$, are used as indicators for $0 < \theta \leq \Delta t_2$ and $-\Delta t_2 \leq \theta < 0$, respectively. Detecting either of 0011 or 1100 words, whose PO is shown in graph $D1$, indicates that CDR is in the out-of-lock state. When CDR is in such state, I_{pd} is deactivated, and CDR re-locks through adjusting I_{fd} based on the FD characteristic. In the FD characteristic (Fig. 6.3b), the $C_1C_2C_3C_4$ words associated with graphs $B2$ and $D2$ are indicators of $\Delta f < 0$ and $\Delta f > 0$ states, respectively; where Δf is the frequency offset of the recovered clock. When Δf is in the range indicated as F_A in Fig. 6.3b, I_{fd} is deactivated since small frequency offsets are trackable through tuning VCO_{tune} using I_{pd} . When Δf is within the ranges indicated as F_B and F_C in Fig. 6.3b, i.e., $|\Delta f|$ is relatively large, the current supplied to the loop filter is I_{fd} and therefore, VCO_{tune} is controlled by FD logic. While CDR operates in region F_B , on the occurrence of 0011 or 1100 words, $I_{fd,up}$ current is supplied to the loop filter. However, in region F_C , although the occurrence of 0000 or 1111 words is an indication of $\Delta f > 0$, drawing $I_{fd,down}$ current from loop filter based on occurrence of these words saturates VCO_{tune} . This is due to the fact that as shown in Fig. 6.3b, unlike graph $B2$, graph $C2$ has a non-zero PO over all Δf values. Hence, to allow for proper frequency detection, only those 0000 words that are either preceded by 0001, or succeed by 1101 are used to control $I_{fd,down}$. In contrast, a 1111 word is only used when it is either preceded by 1101, or succeed by 0001. The PO of such adjustment is shown in graph $D2$ of Fig. 6.3b.

6.2. Proposed CDR technique

Among the three possible configurations, $\Delta t_1 < \Delta t_2$, $\Delta t_1 = \Delta t_2$, and $\Delta t_1 > \Delta t_2$, this work utilizes $\Delta t_1 > \Delta t_2$ as it yields indicator words for out-of-lock state, and provides codes that are unique to each one of the PD and FD states. $\Delta t_1 < \Delta t_2$ and $\Delta t_1 = \Delta t_2$ configurations are avoided since the former results in codes that are common among PD and FD states, and the latter lacks out-of-lock indicator word(s). However, we still limit Δt_1 such that $\Delta t_1 \lesssim 1.25 \times \Delta t_2$. This ensures that the $D1$ graph in Fig. 6.3a has the desired maximum PO of 0.25, while avoiding the unnecessary²⁹ extension in the span of region where $PO_{D1} > 0$.

Based on the measured S-parameters of the channel used in the test setup, and those of the external linear equalizer (LE), simulations are preformed in Matlab to find the optimal placement of (DT_i, TH_i) coordinates within eye of D_{eq} . To converge to an optimal solution while considering the RX power budget, the amount of peaking in LE is set to its minimum that provides enough Δv_2 , such that ensures a value for Δv_1 ($\Delta v_1 < \Delta v_2$) exists for which $\Delta t_1 > \Delta t_2$; and PD and FD characteristics are symmetrical around $\theta = 0$ and $\Delta f = 0$ points, respectively. For a measured post-equalization loss of 3.9 dB at Nyquist frequency, simulations yield $\Delta t_1 = 1.24 \times \Delta t_2$, and $\Delta v_1 = 0.69 \times \Delta v_2$; which are used to generate PD and FD characteristics of CDR as shown in Figs 6.3a and 6.3b. Based on Δt_1 and Δv_1 values, the DC voltages PI_{tune} , $TH_{1,3}$, and $TH_{2,4}$ are supposed to be calibrated at the start of CDR operation. While such calibration can be performed using a DSP core [52], its implementation is beyond the scope of this work.

²⁹Note that D_1 region serves as out-of-lock indicator, and does not provide information regarding the sign of phase error.

Therefore, in this work, we have manually adjusted the PI_{tune} , $TH_{1,3}$, and $TH_{2,4}$ voltages.

6.3 Measurement results

As a proof-of-concept, a 12.5 Gb/s CDR chip is designed and fabricated in a 90-nm CMOS technology. Fig. 6.5a shows the die micrograph which occupies $0.93 \times 0.825 \text{ mm}^2$ excluding the pads. The loop bandwidth of the CDR is set to 5 MHz through an external loop filter. A $2^{31} - 1$ pseudo-random binary sequence (PRBS) data with 3.9 dB attenuation at 6.25 GHz is fed to the chip using high-speed probes. The measured eye diagram of the recovered data is shown in Fig. 6.5b, which has a jitter of 16.9 ps,pp. The recovered clock reveals a jitter of 1.13 ps,rms. The CDR achieves a bit error rate (BER) of $< 10^{-12}$ while tracking data rate offsets over a range of 4.57 Mb/s (± 183 ppm), without the help of a separate frequency detection mechanism. The on-chip blocks (excluding buffers) consume 277 mW from a 1.2 V supply.

6.4 Chapter summary

An eye-monitoring CDR is proposed, in which, unlike the conventional sampling CDRs, the comparators are positioned within the data eye. Figure 6.6 demonstrates the potential application of such CDR architecture in a digital RX, where a CTLE is used to partially open the data eye to address the conditions introduced in Section 6.2. The QCG block proposed in Chapter 4 is used to provide the inputs of phase interpolators. The proposed phase-

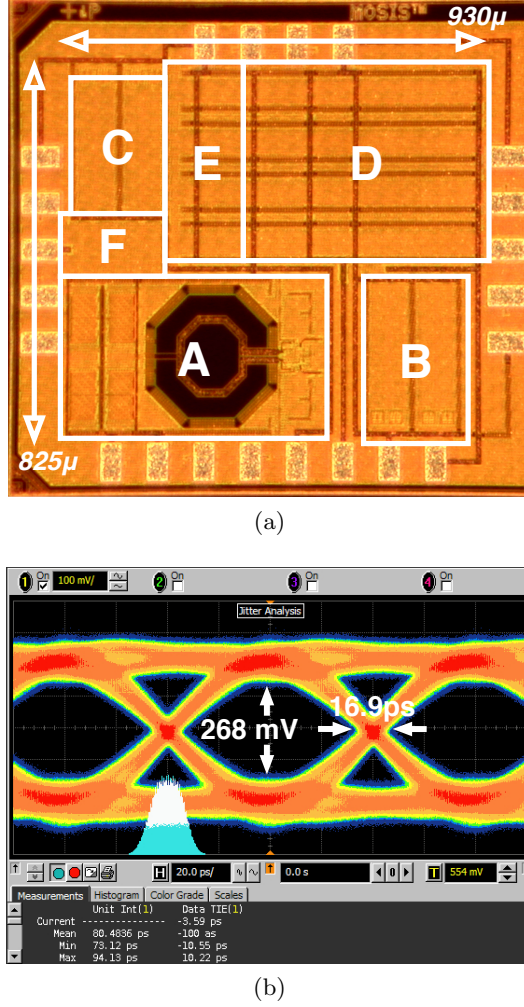


Figure 6.5: Die photo of the prototype chip implemented in 90-nm CMOS (a); where A, B, C, D, E and F are VCO, quadrature phase generator, phase interpolator, comparator array, CML logic, and charge pumps, respectively. The measured eye diagram of the recovered 12.5 Gb/s data (b).

detection technique reduces the number of power-hungry comparators at the front-end of DSP-based CDRs, thus potentially decreases the area and power required for phase detection. The approach enables both correcting clock phase errors, and tracking small clock frequency offsets in multi-Gb/s

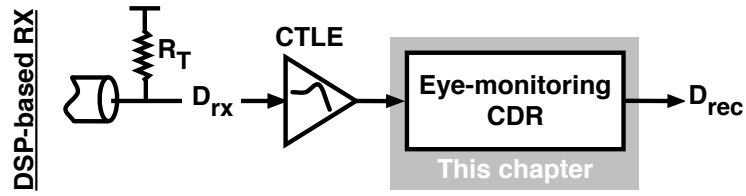


Figure 6.6: Graphical illustration of digital CDR block addressed in this Chapter, and its interaction with other RX blocks.

serial link receivers.

Chapter 7

Conclusion

7.1 Research contributions

This thesis addresses some of the system-level and circuit-level challenges associated with reducing the power consumption of multi-Gb/s wireline receivers. Several key functions of an RX, including equalization, clock recovery, and generating multiple phases of the clock have been analyzed. The following are the key contributions of this thesis (as partially published in [32, 53, 68, 74, 77]):

- The power consumption of high speed DFEs is examined and a solution to integrate the DFE within the front-end ADC is proposed. The idea is validated through implementing a 10 Gb/s DSP-based RX in a 65 nm CMOS technology.
- The DSP-based RX operates based on the proposed speculative/SAR digitization algorithm, which is specifically designed for wireline applications. The algorithm allows for digitizing and recovering the data using two comparators. Decision feedback equalization is achieved as a natural product of this algorithm. The RX chip demonstrates the feasibility of digitizing a 10 Gb/s data stream with 5 bits of resolu-

tion using 2 comparators, versus 31 ($2^5 - 1$) comparators needed in a full-flash front-end ADC.

- Techniques and challenges of quadrature clock generation are analyzed. An open-loop architecture based on active delay stages is proposed. The power consumption of delay stages is investigated and a circuit-level design technique is suggested which allows to achieve the desired delay at certain clock frequency, while minimizing the power consumption. The proposed architecture is embedded within both analog and digital CDRs, and its performance is evaluated.
- An analog CDR, which utilizes a mixer-based PD is proposed. Using the developed QCG block, a method for wideband data phase shifting is implemented. While the prototype 90 nm chip contains a 12.5 Gb/s version of this architecture, the architecture is suited for higher data rates where an ADC-based front-end is not feasible.
- A hardware-efficient digital CDR architecture is proposed that enables monitoring, and tracking the phase and frequency of the random data. The architecture utilizes 4 comparators that are clocked from the phases generated by QCG block. The comparators monitor the data eye at baud-rate, and provide a digital 4-bit word that is subsequently used to extract (recover) the phase and frequency of the clock. The 12.5 Gb/s prototype CDR, implemented in 90 nm CMOS, demonstrates a system level solution to reduce the comparator count. Unlike the conventional ADC-based RX which choose the number of comparators based on the required digitization resolution, in the pro-

posed approach the comparator count is fundamentally set based on the shape of the data eye formed by the eight possible combinations of three consecutive bits. While avoiding data digitization, the digital eye-monitoring CDR allows for detecting phase and frequency offsets in the sampling clock in respect to the data eye.

7.2 Performance comparison

To choose the optimum RX architecture for a serial link, in addition to power consumption, one should consider the BER and jitter performance of the potential CDRs compatible with chosen RX topology. For the BER of an RX we can write [78]

$$BER = 0.5 \times \operatorname{erfc}\left(\frac{WC_1}{\sqrt{2}\sigma_{noise}}\right) \quad (7.1)$$

where WC_1 , and σ_{noise} are worst case amplitude of the bit ‘1’ at sampling time instance, and RMS noise voltage. Note that σ_{noise} represents both thermal voltage noise, and the voltage noise to to the random jitter in sampling clock, RJ_{clk} . To convert the RMS value of RJ_{clk} , σ_{clk} , to σ_{noise} we can write [58]

$$\sigma_{noise} = \frac{v_{sw} \times 2\pi f_{clk} \times \sigma_{clk}}{\sqrt{2}} \quad (7.2)$$

where v_{sw} is the signal swing. On the other hand, to calculate the contribution of data dependent jitter, DDJ^{30} , to σ_{clk} , for bang-band CDR we can

³⁰Or equivalently jitter due to ISI.

write [79]

$$\sigma_{clk} = \sqrt{\frac{\sqrt{2\pi}\theta_{step}\sigma_{ddj}}{8}} \quad (7.3)$$

θ_{step} is the phase step of the CDR loop per decision cycle of PD, and has the following relationship with the phase step of a binary bang-bang PD, $\theta_{step,b}$,

$$\theta_{step} = \frac{\theta_{step,b}}{2^n - 1} \quad (7.4)$$

in which, n represents the sampling resolution. Additionally, for a linear CDR (i.e. one with mixer-based PD) we have [80]

$$\sigma_{clk} = \sigma_{ddj} \sqrt{\frac{3\omega_n t_{bit}}{\sqrt{2}}} \quad (7.5)$$

where ω_n , and t_{bit} are the natural frequency of the CDR loop, and duration of each bit, respectively. Figure 7.1 compares the sampling time margin versus amount of residual ISI in data, among bang-bang CDRs with various resolutions in data and edge samplers, linear CDR (Chapter 5), and eye monitoring CDR (Chapter 6). In Fig. 7.1, BER= 10^{-12} has been considered which simplifies Eq. 7.1 to

$$WC_1 = 7 \times \sigma_n \quad (7.6)$$

Figure 7.1 suggests that the sampling time margin for bang-bang CDRs improves if the resolution of data/edge samplers increases. For large values

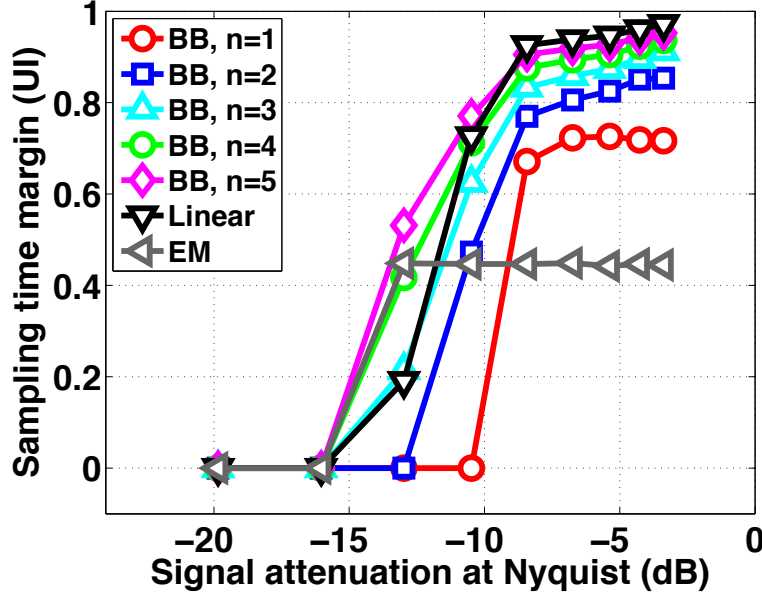


Figure 7.1: Comparison of the sampling time margin of bang-bang CDR, analog CDR (with mixer-based PD), and eye monitoring CDR, as function of different amounts of residual ISI in signal. BB, and EM refer to bang-bang and eye monitoring architectures.

of n , the power penalty of samplers may be partially offset by the lower power consumption in CTLE. This is due to the fact that for a constant BER, higher sampling resolution allows to tolerate more loss, and hence, reduce the peaking demanded from CTLE. Additionally, note that if the frequency response of channel has deep notches (i.e., due to via stubs), equalization using CTLE may not be the feasible/optimal approach, and a multi-tap high-resolution DFE may be inevitable.

From Fig. 7.1 we can see that a linear analog CDR typically offers lower sampling time margin at left half of the signal loss spectrum, as the high residual ISI in data modulates the gain of the mixer-based PD and results

7.2. Performance comparison

Table 7.1: SELECTION OF CDR ARCHITECTURE BASED ON CHANNEL LOSS

Channel loss at Nyquist	CDR architecture
Low	Bang-bang (low-resolution) ^a
Low-Medium	Linear (Mixer-based)
Medium-High	Eye monitoring
High	Bang-bang (high-resolution)

^a Although linear CDR provides a marginally better jitter performance in this category, it might not be as area efficient.

in excessive jitter. However, for the right side of the signal loss spectrum (i.e., low loss channels), linear PDs prove to be a superior choice as they not prone to the power versus sampling resolution trade-off of a digital RX.

Finally, the eye monitoring CDR proves useful when data has higher residual ISI (i.e. higher σ_{ddj}). This can be explained by considering that the timing-threshold coordinates (DT_i, TH_i) of comparators are located within the data eye as opposed to the sampling scheme where they are distributed in the range set by ISI. While this is beneficial for lossy channels³¹, the timing margin of such CDR architecture is fundamentally limited by the $\Delta t_1 \lesssim 1.25 \times \Delta t_2$ condition discussed in Chapter 6 (i.e., the flat region of the corresponding time margin curve in Fig. 7.1). This partially diminishes the advantage of such architecture while communicating through low-loss channels. Table 7.1 summarizes the above discussion.

³¹Because DDJ does not modulate the bit decision of the comparators

7.3 Future work

The channel characteristics, data transmission rate, and power budget are three main factors which should be considered in the design process of modern wireline RX. The first factor is usually dictated by the network infrastructure, the second factor is set by the particular standard of operation, and the last factor depends on the application and operation medium (e.g., chip-to-chip versus long-haul links). While the wireline channels have experienced relatively minor improvements over the years, wireline data rates have constantly increased in each generation of IEEE 802.3 group of standards. Although power consumption is mostly a degree of freedom in the design process, it is indeed the most prominent differentiating factor among RX is the same class. Therefore, reducing the power dissipation of wireline RX (and TX), is expected to remain an interesting area of research. Note that although the proposed techniques are targeted towards wireline RX, with minor modification, they can be employed at the baseband of wireless RX too. The following items are the potential future tasks that can be done to exploit the results of this thesis, and further enhance the power versus performance trade-off in both analog and digital RX:

- While offering great flexibility and enhancing sophisticated digital signal processing, an ADC-based RX architecture is still not considered an optimal solution at very high data rates (e.g., > 25 Gb/s). One can further minimize the power consumption through exploiting high-speed comparator architectures other than CML. The main challenge would be providing a sampling and conversion speed at least equal to

baud rate; a difficult task beyond 10 Gb/s.

- The trade-off between achieving sharp edges at comparator output versus having low comparator latency remains a challenge. Specifically, the delay of cascaded latches may introduce large latencies, which may not be tolerated if the comparator falls within the timing critical loop of DFE. In such scenario, reducing comparator latency to a small portion of UI would be necessary; otherwise, either the timing would be violated at the summing node, or less than optimal settling time would result in digitization (quantization) error.
- While this thesis focuses on binary signaling, it should be noted that multi-level signaling is an active area of research. An advantage of ADC-based RX over binary RX is that it can recover both binary and multi-level data with minimal adjustment to the DSP-based algorithm; whereas in an analog RX, the hardware should be mostly redesigned. The proposed speculative/SAR digitization algorithm can be modified to accommodate multiple data levels. Furthermore, adaptively adjusting the comparator thresholds to digitize > 25 Gb/s data streams poses interesting challenges.
- In applications that require dense arrays of TX/RX pairs, realizing a separate QCG block for each transceiver may not be area efficient. On the other hand, if transceivers share the QCG, maintaining the integrity of quadrature clock phases over long distances is challenging. Finding an algorithm for distributing an optimal number of QCG blocks within a large chip is a notable design challenge.

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Appendix A

Additional circuit schematics

While the schematics of the majority of circuits used as building blocks of the proposed RX architectures are provided and discussed in the Chapters of this thesis, schematics of a few circuits (that are not among the core contributions) are provided in the following Sections.

A.1 Comparator

The comparators used in the designs presented in Chapters 3 and 6 have a CML structure. Figure A.1 shows the structure of one comparator which consists of preamplifier, latch, and CML-to-CMOS circuits. The comparator is preceded by a track and hold (T/H) circuit. The differential signal pair $A_{in}-Ab_{in}$ is the analog input to T/H, and d_{out} is the 1 bit digital output of the comparator. Note that voltage level at the output of the CML latches in comparators shown in Fig. 3.5 need to be converted from low-swing CML domain to rail-to-rail swing in CMOS domain. This is due to the fact that the DSP core is implemented with CMOS gates. However, as in architecture of Fig. 6.2, the comparators are followed by CML logic gates, the CML-to-CMOS circuit of Fig. A.2c is not needed.

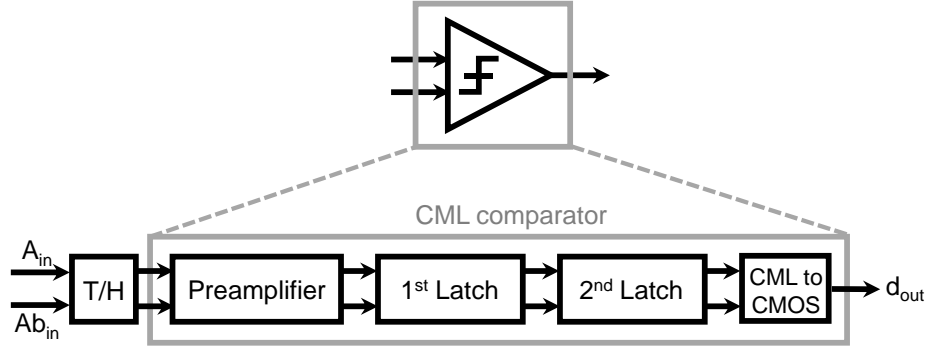


Figure A.1: Block diagram of the CML comparator.

A.2 Digital-to-analog converter

Figure A.3 shows the schematic of a current steering DAC similar to the one used in architecture of Fig. 3.5. Note that to avoid timing errors while converting the digital bits $d_{n,n=1:4}$ to the differential signals used to control the gates of the steering devices in transconductance stages, an XOR gate is used both as buffer (while one input is set to ‘0’) and as inverter (while one input is set to ‘1’).

Additionally, to achieve a better linearity, the current sources in the DAC are implanted in a thermometer-coded manner instead of the binary-weighted alternative.

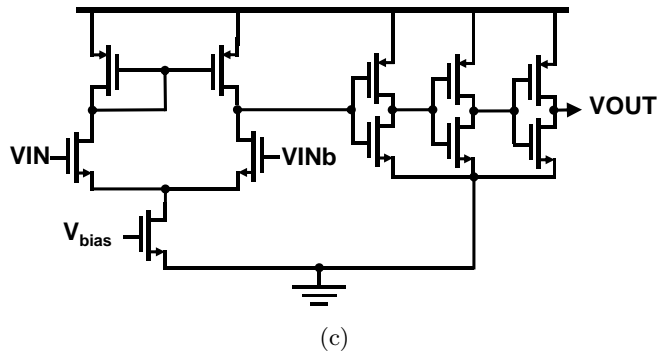
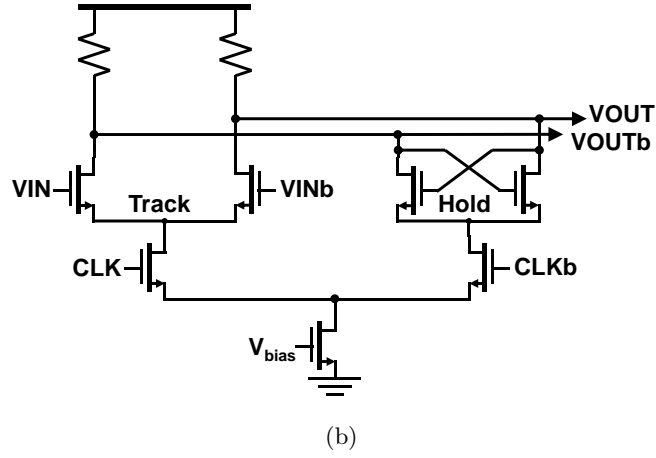
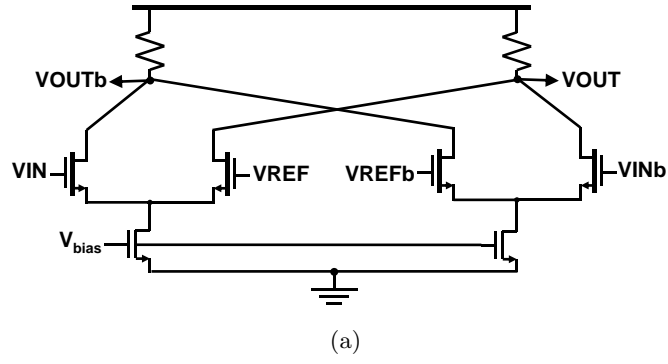


Figure A.2: Preamplifier (a), latch (b), and CML-to-CMOS circuits.

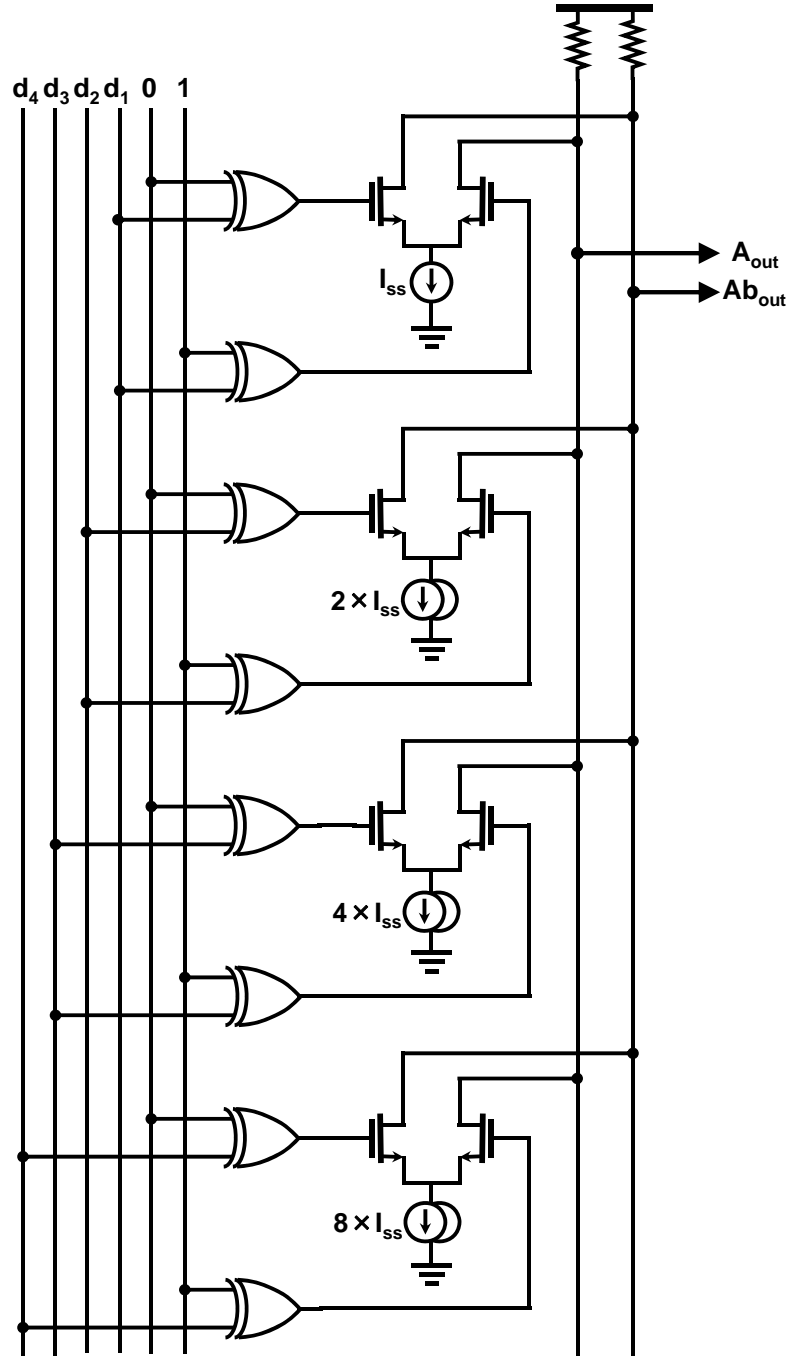


Figure A.3: Schematic of a 4-bit current steering DAC.