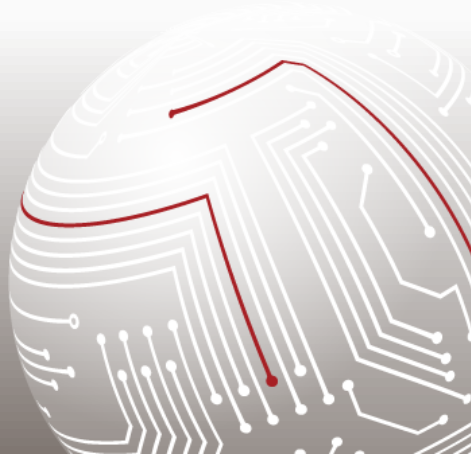
Global Standards for the Microelectronics Industry

HBM4 Mechanical Test Vehicle (MTV4) Design Requirements

Joint Presentation by SK hynix / Intel

04/02/2024

TG423B3



References

- Committee 1st showing
  - (Reference spreadsheet) MTV netlist draft_SKH_Micron_Intel_12052023_r00.xls
  - tg423b3^20231205^x^SKhynix^HBM4 Mechanical Test Vehicle Standardization Proposal.pdf
- MTV4 Daisy Chain
  - Ballot drafts: tg423b3^20240201^1883.62^SKhynix^HBM4 Mechanical Test Vehicle Daisy Chain_r00_clean.pdf
  - JEDEC HBM4 TMTV Modification.pdf
  - HBM4_MTV_JEDEC_02_02_2024.xlsx → All references used in this slides are pointing to that file
  - TG423B3^20240206^xxxx.yy^NVIDIA^Call_471-20240206-TG423b3-Meeting-Minutes.pdf

Backgrounds

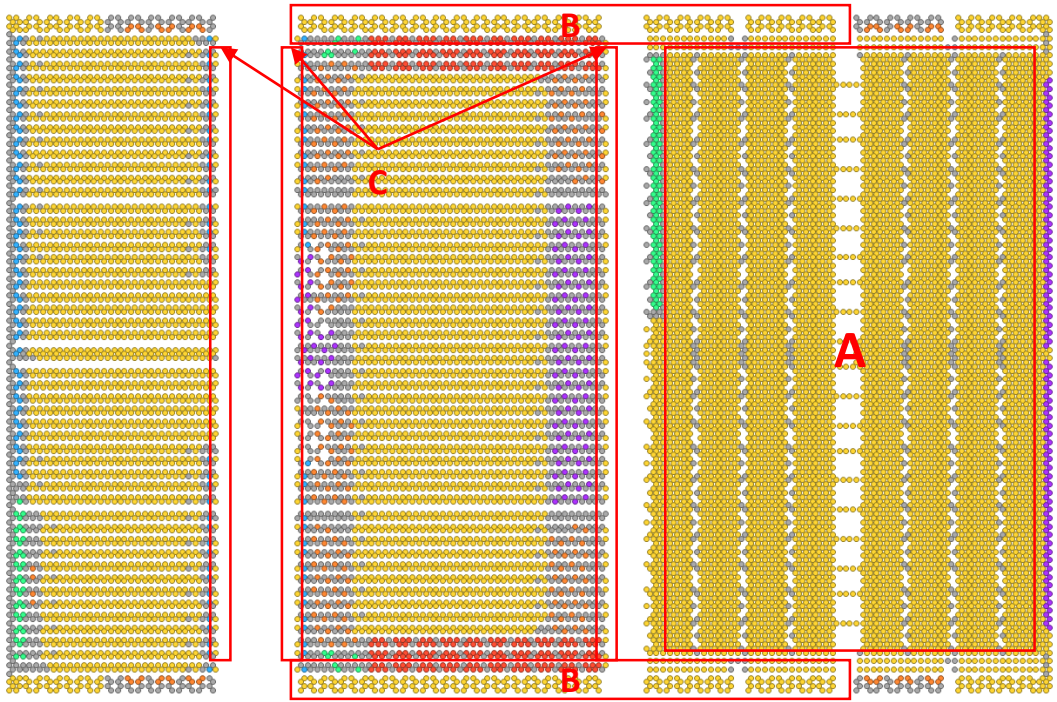
- This presentation is intended to define design requirements and key components of MTV
  - Naming conventions, Structures, Design Requirements, and connection rules of each chain classes
    - EDM
    - Heater
    - Thermal Sensor
    - IMAX – Partially Optional
    - TSVDC
    - C4DC

C4DC

- Naming conventions
  - *[Structure]_[Si routing style]_[Location]*
  - Structure Type: C4DC
  - Routing style: HORIZONTAL vs VERTICAL

- Example
  - *C4DC_HORIZONTAL_C4* = C4DC which is Horizontally routed in the corner (C4 location)

C4DC Pin-outs



- Consists of Edge DC(E#), Horizontal DC, Vertical DC, Corner DC(C#)

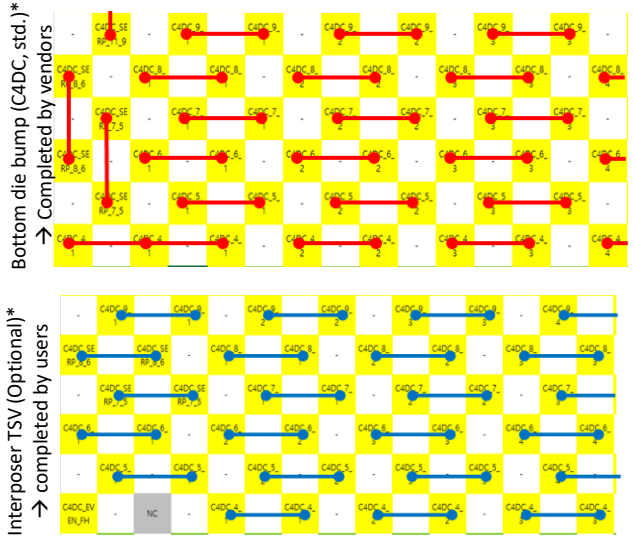
Addressed Intel's requirements

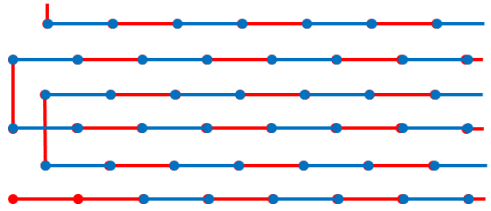
- A: C4DC orientation in the PHY must be vertical
- B: C4DC link by skipping 1 bump in middle to ease package trace route-out strategy without loosing C4DC coverage
- C: Added 1 column of C4DC near transition region
- Thermal sensors for TSVEM is vendor specific features, only applied to the designated area as "Vendor Specific" nets

- This slide is reference only. See the netlists for details and exact pin locations

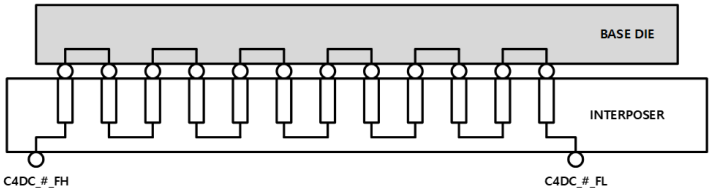
Interoperability with C4DC & Base die Daisy Chains (Optional)

- Suppliers may expand C4DC to base die daisy chains to have better test coverages* → details will be consulted by vendors datasheets or documentations





Routing to stich bottom die and base die (Example)



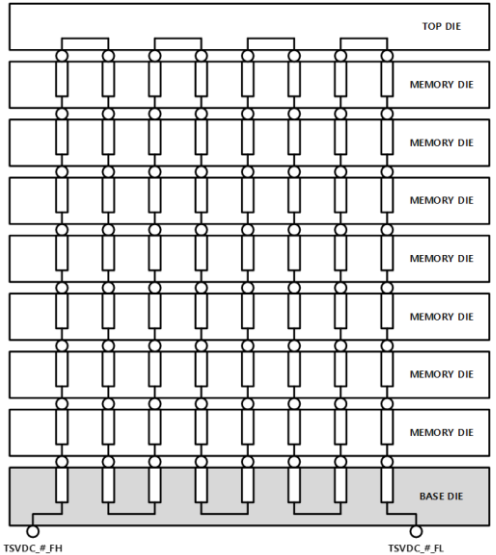
Routing to stich bottom die and base die (cross sectional view, Example)

* Netnames in this slide are intended for illustrating BCDC and C4DC connections only when vendors are decided to support Base die daisy chain

TSVDC

- Naming conventions
  - *[Structure]_[Group#]_[FH/MH/ML/FL]*
  - Structure Type: TSVDC
  - Group#: 1-64

- Example
  - *TSVDC_16_FH* = Force High bump for TSVDC Group 16



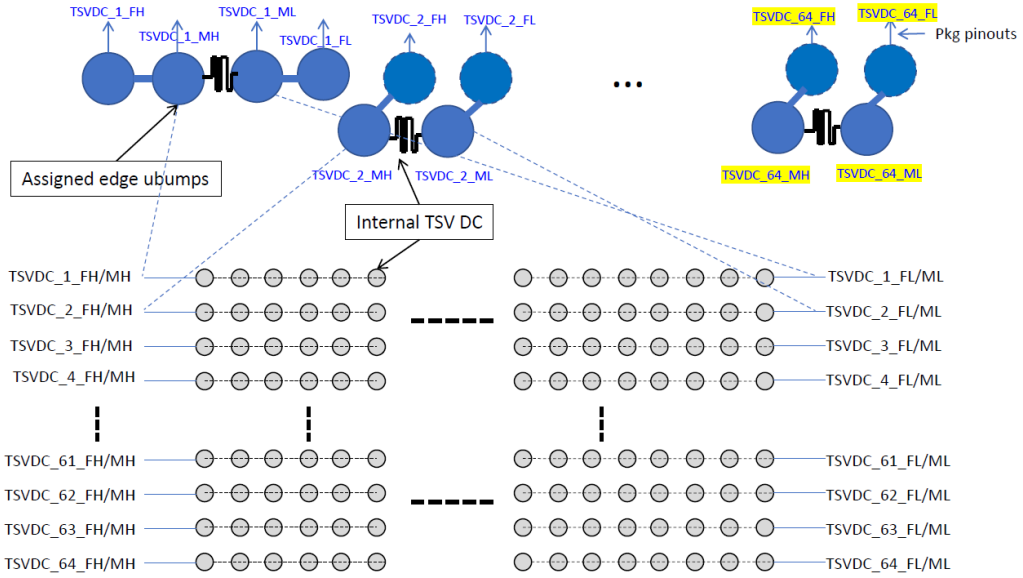
Routing example of TSVDC (cross sectional view)

TSVDC design requirements

Category	Value (Units)	Requirements	Remarks
TSVDC	Larger than 85% TSV Coverage	• Test of Resistance & probe for leakage vs adjacent TSV Chain. • Need to ensure larger than 85% coverage covers high and low stress area	
4 pin TSV DC if R < 10 Ohms; Otherwise 2 pin TSVDC is ok	64 chains → 32 chains near edge + 32 chains in core	• To cover highest stress location (for edge most TSVs)	
FI Requirement		• Absolute minimum: isolate if fail is in memory stack or ubump • ubump and TSVDC are not chained together	
4 wire ubump DC	4 rows	• Bump assignment ensures users can account for this	
Bump assignment, pin-outs, core and edge C4DC		• Refer to the netlist	

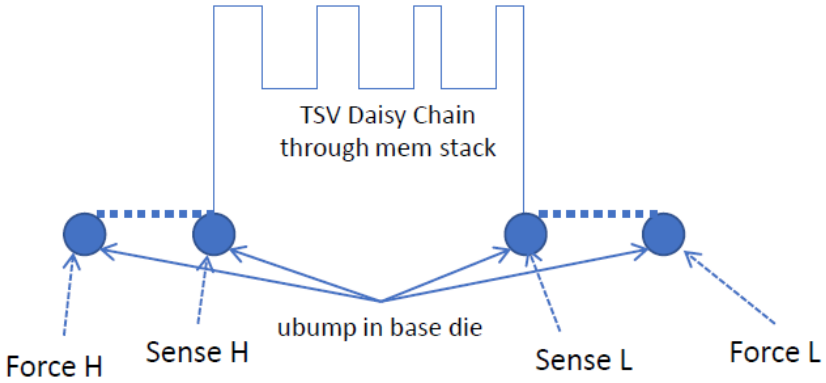
Internal TSVDC Connections

- TSVDC leakage and resistance tests must be enabled and cover more than 85% of risky TSV locations



4 Point Daisy Chain: TSV & ubump

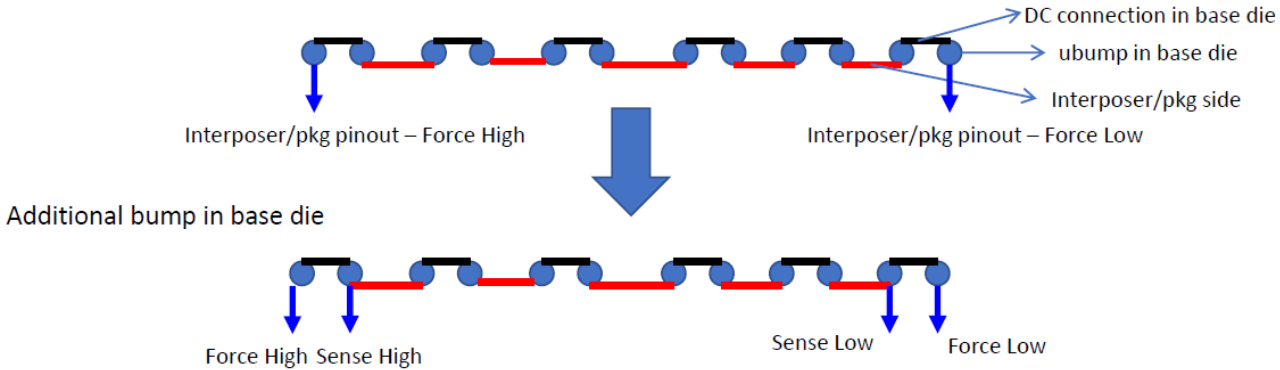
- Implement up to 2 TSV DC pairs as 4 wire measurement – sample accurate R measurement



4 wire implementation of TSV chain

4 Point Daisy Chain: TSV & ubump

- Implement up to 2 ubump DC rows as 4 wire measurement – sample accurate R measurement



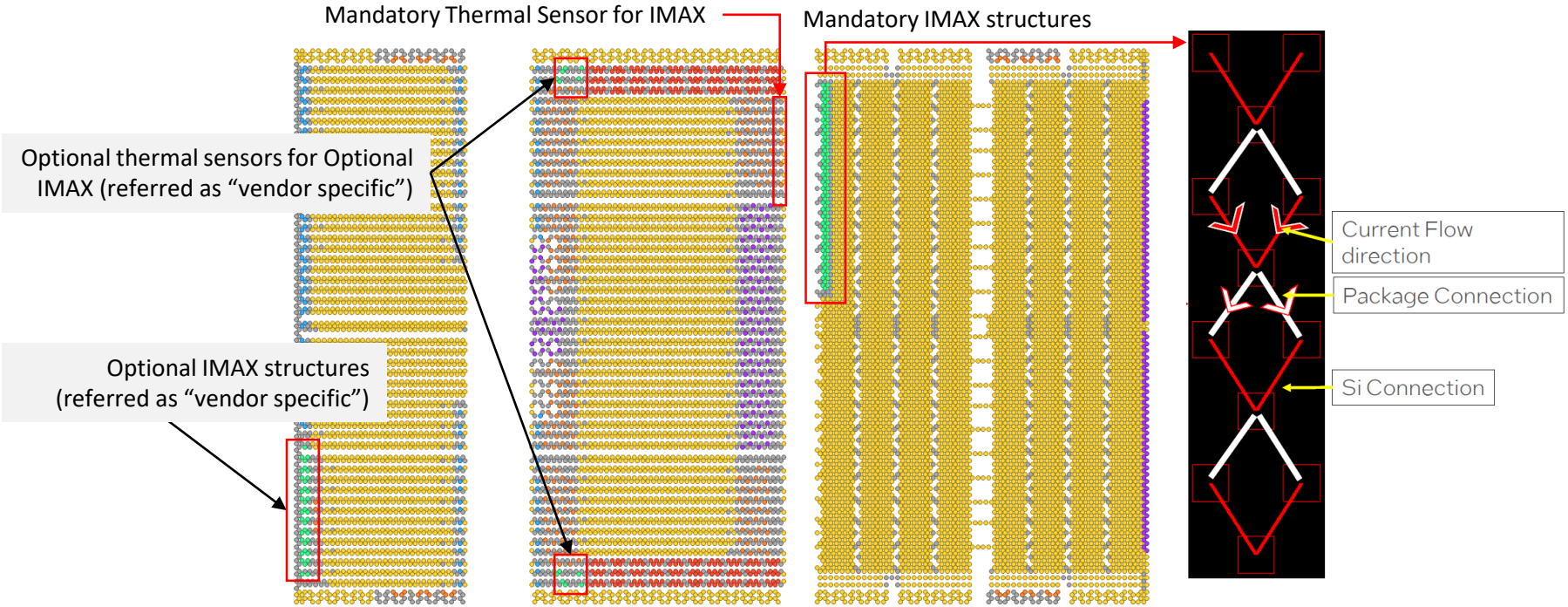
IMAX (Partially Vendor Specific)

- Naming conventions
  - *[Structure]_[Location]_[FH/MH/ML/FL]*

- Rules
  - IMAX1 represents mandatory IMAX structures
  - Suppliers may implement optional IMAX structures to enhance testability on the existing “Vendor Specific” netlist locations on the spreadsheet (See next page)
  - In the case where the supplier does not support optional IMAX structures, “vendor specific” nets should be treated as “No connects (usable neither users nor vendors)”
    - TG may decide the exact meaning on “No connects” and potentially address on voting comments
    - Option A: “electrically isolated nets and not usable by users” (TG needs to have clear directions on how the netlist is going to be changed?)
    - Option B: “reserved for vendor” consult with vendors spreadsheets
    - Option C: NC (strict rules as it is)

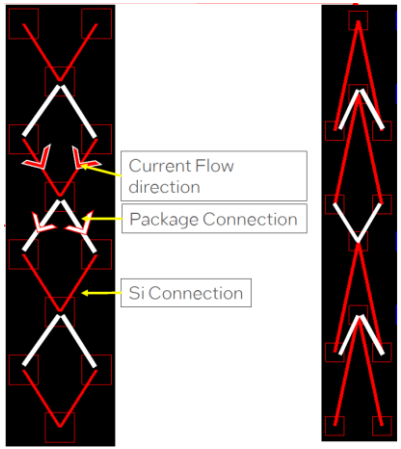
* Suppliers may implement TSVEM on the vendor specific regions (please refer to the spreadsheet) with pre-defined connections rules between and user and suppliers.

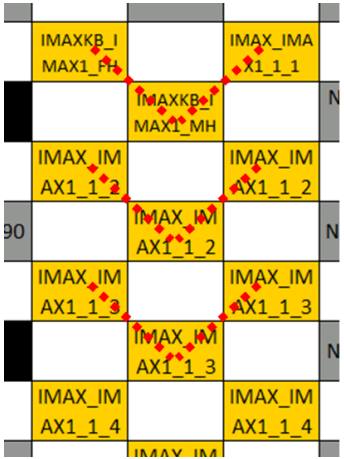
IMAX Pin-outs

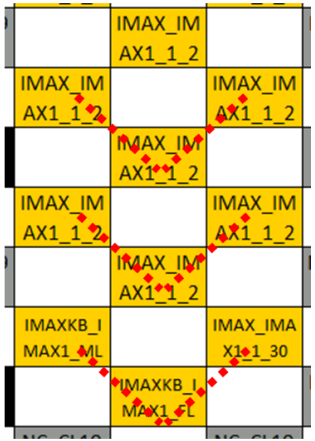


IMAX Connection Rule

- Groups of signals have identical net names must be connected within the base die
  - Ex) [IMAXKB_IMAX1_FH , IMAXKB_IMAX1_MH , IMAX_IMAX1_1_1] , [IMAXKB_IMAX1_FL , IMAX_KB_IMAX1_ML , IMAX_IMAX1_1_30]







IMAX Design Requirements

Category	Value (Units)	Requirements	Remarks
Types of EM	Upto 3	Designated IMAX location(see the netlist) is Must-have, otherwise are optional	
# of structures	4	1 for C4EM (Must-have), 1 lower left (optional) 1 each of TSV-1 stack and TSV full stack EM (optional)	
Location	High stress region	Absolute minimum: 1 of each flavor to be located in highest stress region	
# Of Bumps	90 (center) / structure	See page 13 and 14 to see the inter-pkg connections. Target resistance for Si IMAX resistance as 1 Ohm	
Trace Width		Ensure to use max trace width allowed by suppliers design requirements	

EDM (Etch Damage Monitor)

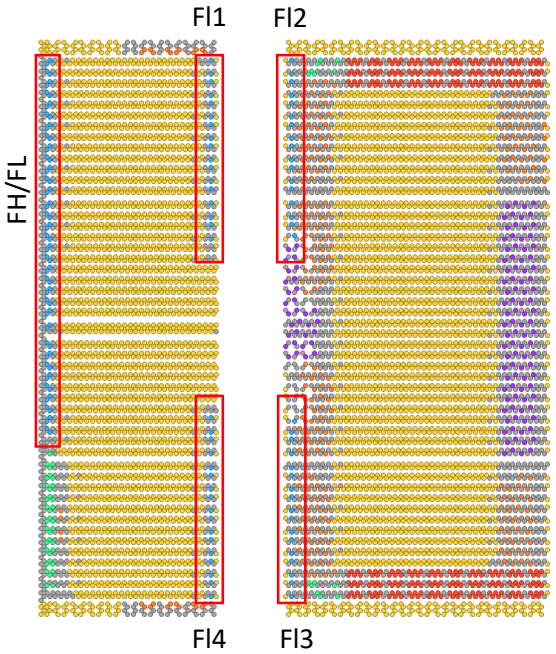
- Naming conventions
  - *[Structure]_[Die#]_[FH/MH/ML/FL]*
  - Example
    - *EDM_1H_FH* = EDM pin-out of Force High bump for 1H Memory die
    - *EDM_BASE_MH* = EDM pin-out of Measure High for Base Memory die

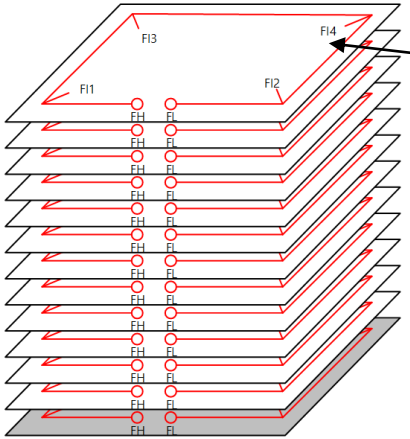
* Suppliers may implement TSVEM on the vendor specific regions (please refer to the spreadsheet) with pre-defined connections rules between and user and suppliers.

EDM Design Requirements

Category	Value (Units)	Requirements	Remarks
Edge Damage Chain - Base Die	Mandatory	As close to active device edge as permitted by suppliers design requirements, staircase covers all metal layers in stack	
Edge Damage Chain - Memory Die	Mandatory		
# of pinouts - Base Die	2 pins for FH 2 pins for FL	2 wire	
# of pinouts - each Memory die	2 pins for FH 2 pins for FL	2 wire, Users to pin out as 4 wire in package. Bumps to be assigned as per package requirement	
Max total base die/package pinouts	102	See the netlist	
Staircase/via pitch	20um (Max.)	For crack resolution	
Resistance	1MOhm (Max.)		
Minimum FI Requirement	1	Need to isolate which die is failing in the stack	
Additional FI requirement	4	Isolate failing edge on each die, by handprobe	
Edge damage chain – memory die coverage from the edge	500um (min.)	To ensure HMDC detection. To ensure base die EDM covers core die shadow *Note) Exception allowed in locations where design features (such as pads, routing lanes, TSV etc.) are located within 500um from edge.*	

EDM Connection & Pin outs

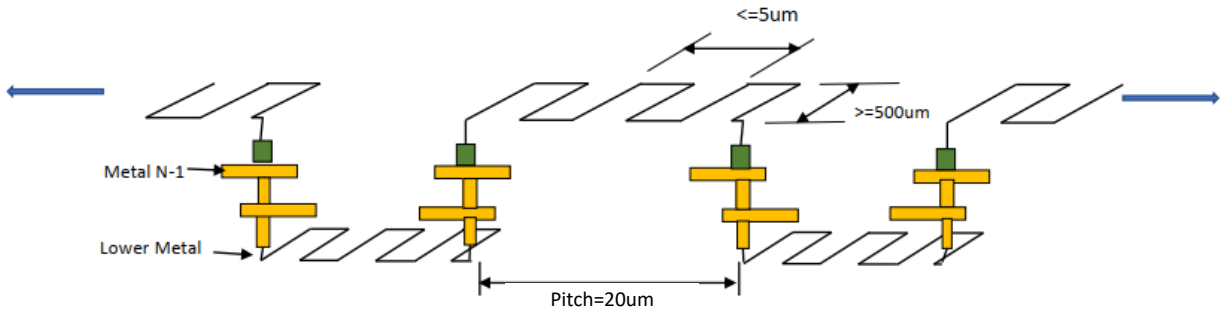




Structures about device active edges

- Minimum Requirements: 2 pinout/die to isolate falling die
- Additional Fl: pads in top metal layer, to isolate failing edge on each die for ease of FA

EDM Schematic



Heater(HTR) and Thermal Sensor(TS)

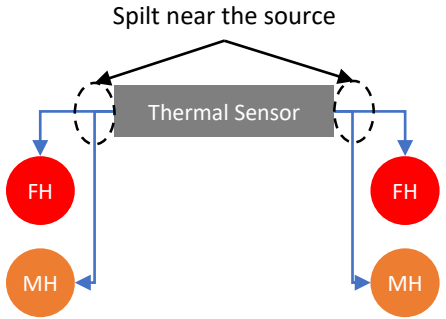
- Naming conventions → Base / Stacked / Top die have distinct requirements
  - *[Structure]_[Die]_[Location]_[FH/MH/ML/FL]*
  - *HTR_STACK_HTR1_FH* = Heater pin-out of Force High bump for rest of the stacked die excluding top and base die
  - *TS_BASE_OC1_MH* = pin-out of Measure High for Base Memory die of Off-center sensor i.e. OC1.

Category	Value (Units)
HTR	Structure Type: Heater
HTR1	Location of 1st HTR
HTR2	Location of 2nd HTR
TS	Structure Type: Thermal Sensor
M	Middle/Center of the Die
OC#	Off-Center
C#	Corner
E#	Edge
BASE	For the Base die
TOP	For the Top die
#H	For die in the stack. Ex) '2H' = 2H die in the stack

Base die HTR & TS Placement

- Heater
  - First heater covers the PHY region
  - Second heater covers the TSV region
  - Suppliers to correctly choose heater size, location of these heaters to match the source sizes, and locations in their product thermal model
  - Trace width and pattern must be uniform

- Thermal Sensor
  - Center/Middle (M) sensor to be located <250um of the die center.
  - 4 Corner sensors to be located <250um of the die edge.
  - OC1 sensor to be located <250um the product base die sensors to replicate them
  - OC2 sensor location, suggested by supplier, to be located at the center of the thermal bumps
  - 4 wire sensing for all sensors



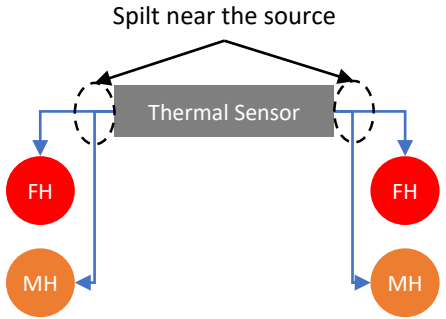
Base die HTR & TS Requirements

Category	Value (Units)	Requirements	Remarks
Thermal Bumps		Test vehicle to mimic product	
# of Heaters	2	One HTR to cover PHY region, the other one covers TSV region	
Heater Type	Resistive		
Heater Power	24-36W/Heater	Max output per heater in base die Total die power of 72 W (low resistance range) to 48W (high resistance range)	
Heater R	Low range: 100 Ohms (gives V, I, P of 60V, 0.6A, 36W) High Range: 150 Ohms (gives V, I, P of 60V, 0.4A, 24W)	Target HTR power is 24 - 36W Total routing resistance need to be <5% of overall resistance of HTR	
# of bumps	4 wire	4W; FH – 25, MH – 5, FL – 25, ML – 5	
# of sensors & Location	7	4 corner, 1 center, 2 off-center	
Sensor R	500-750 Ohm	Nominal value. Supplier to provide expected resistance variation due to process	
# of bumps	4 bumps/sensor	One bump each for FH, MH, FL, ML	
Sensor:4-wire	4 wire	4 wire is needed for base die sensors	
Sensor Area	Up to 250 x 250um	Preferred if area can be limited to 100x100um	

Top die HTR & TS Placement

- Heater
  - Two individually pinned out heaters to get total die power of >=72 W
  - Top die HTR 1&2 force & sense bumps refer to netlist.
  - Make the HTR1 slightly larger in x than HTR2. (< 1 mm difference)

- Thermal Sensor
  - Sensors should not lay directly on gap between two heaters (cold spot)
  - Center sensor to be located <250um of the die center
  - Edge and corner sensors to be located <250um from the die edge
  - OC1 and OC2 (Off-center) sensors should align vertically with their respective base die sensors
  - 4 wire sensing for all sensors

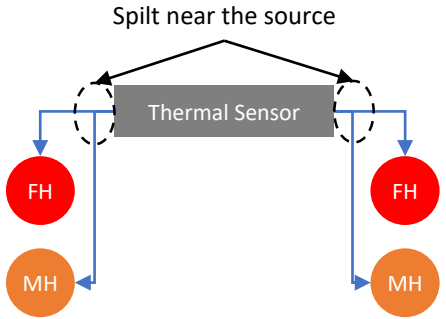


Top die HTR & TS Requirements

Category	Value (Units)	Requirements	Remarks
Thermal Bumps		to mimic product	
# of Heaters	2	Two individually pinned out heaters covering no less than 95% of die area in total	
Heater Type	Resistive		
Heater Power	>=36W/Heater	Max power output/heater Two individually pinned out heaters (H1 and H2) to get total die power of 48 ~ 72 W	
Heater R	100 ~ 150 Ohms (gives V, I, P of 60V, 0.6A, 36W)		
# of bumps (FH, FL, MH, ML)	4W	4W; FH – 25, MH – 5, FL – 25, ML – 5	
# of sensors	11 for Top memory die	Each sensor is independently pinned out	
Sensor R	500 ~ 750 ohms	Limit routing to 5% of sensor resistance	
# of bumps	4 bumps/sensor	One bump each for FH, MH, FL, ML	
Sensor:4-wire	4 wires		
Sensor Area	250 x 250 um	Preferred if design can be limited to 100x100um	

Stacked die HTR & TS Placement

- Heater
  - One heater for each die
  - Covers the DRAM bank area
  - All Heaters are connected in parallel
- Thermal Sensor
  - Sensors in each memory die must be independently pinned out
  - Center sensor to be located <250um of the die center
  - OC1 and OC2 sensors should align vertically with their respective base die sensors
  - 4 wire sensing for all sensors



Stacked die HTR & TS Requirements

Category	Value (Units)	Requirements	Remarks
Thermal Bumps		Test vehicle to mimic product	
# of Heaters	1 single HTR per memory die		
Heater Type	Resistive		
Heater Power	See next pages		
Heater R			
# of bumps (FH,FL,MH,ML)		4W; FH – 25, MH – 5, FL – 25, ML – 5	
# of sensors	3 for stacked memory dies	1 center & 2 off center. Each sensor in each memory die is independently pinned out	
Sensor R	500 ~ 750 ohms	Limit routing to 5% of sensor resistance	
# of bumps	4 bumps/sensor	One bump each for FH, MH, FL, ML	
Sensor:4-wire	4 wires		
Sensor Area	250 x 250 um	Preferred if design can be limited to 100x100um	

Stacked die HTR & TS Requirements (cont'd)

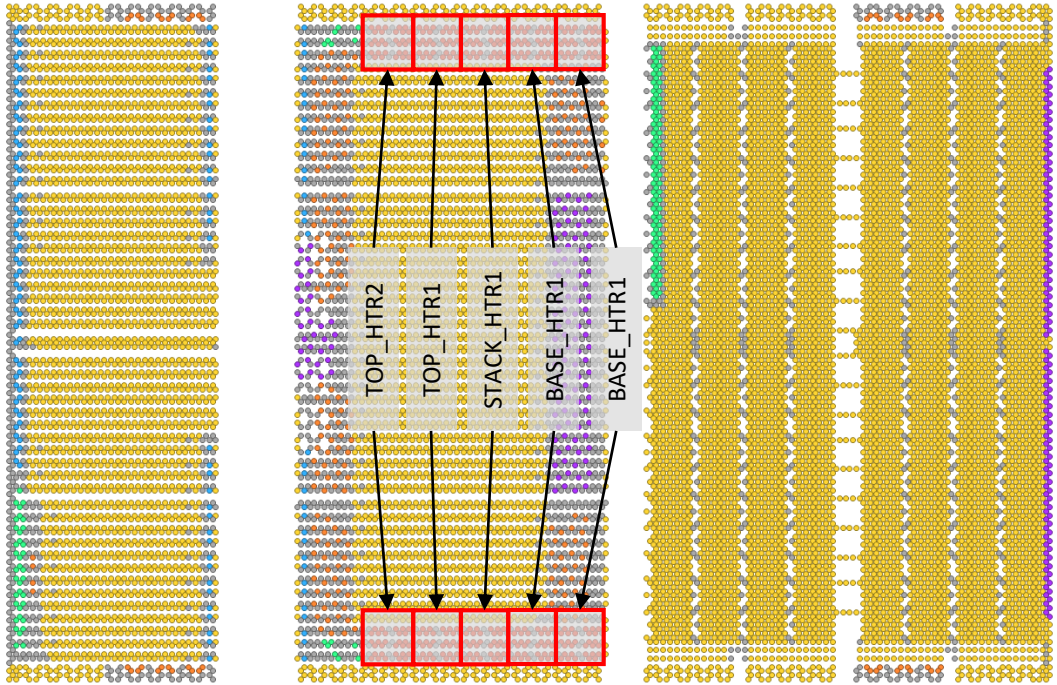
Low Range

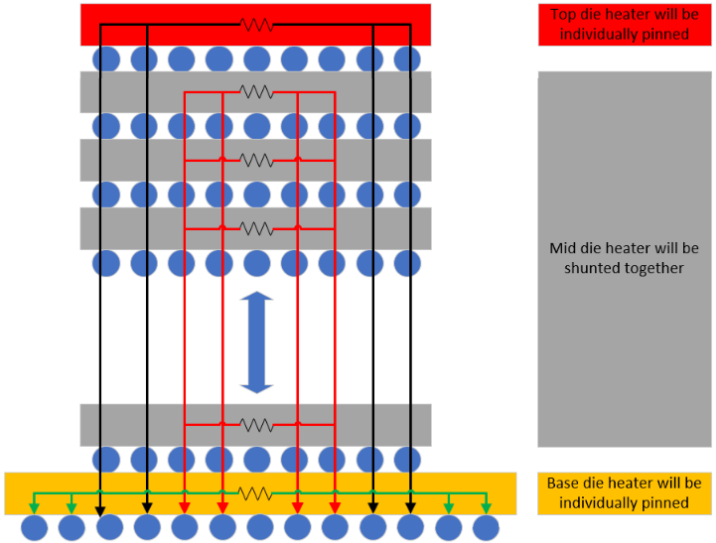
	8Hi	12Hi	16Hi
R/heater (Ohm)	1100	1100	1100
R overall (Ohm)	157.1	100	73.3
I (A)	0.38	0.60	0.82
V (V)	60	60	60
P (W)	22.9	36	49.1

High Range

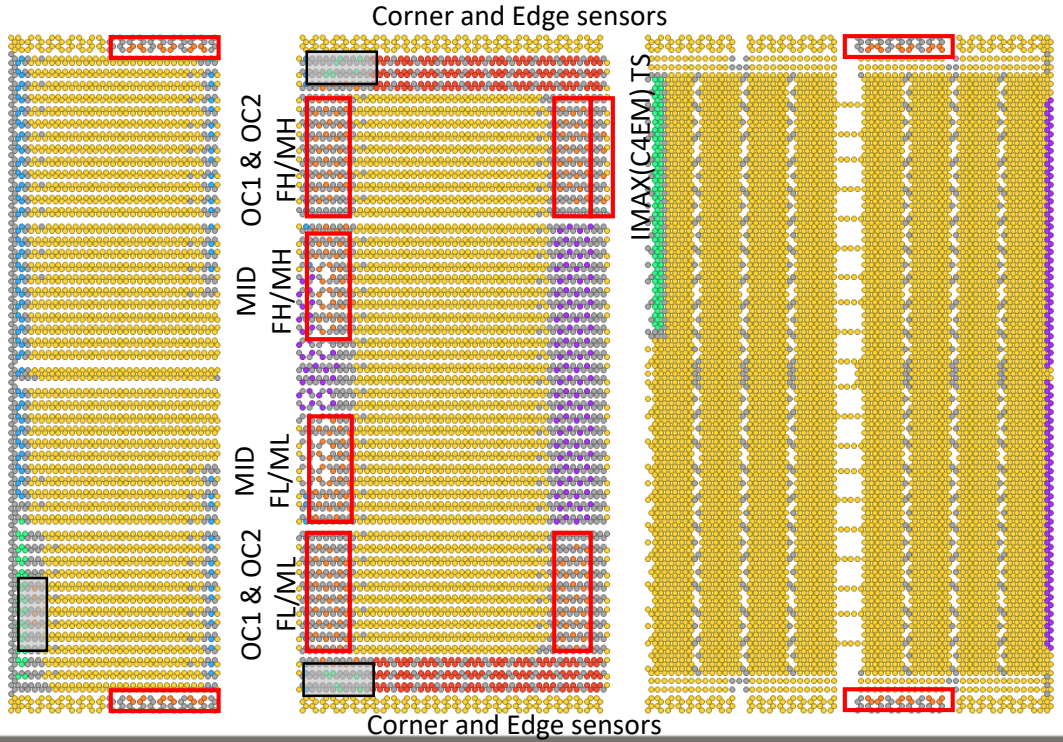
	8Hi	12Hi	16Hi
R/heater (Ohm)	1150	1150	1150
R overall (Ohm)	164.3	104.5	76.6
I (A)	0.37	0.57	0.78
V (V)	60	60	60
P (W)	21.9	34.4	47.0

HTR Pin-outs


TOP_HTR2
TOP_HTR1
STACK_HTR1
BASE_HTR1
BASE_HTR1


Top die heater will be individually pinned
Mid die heater will be shunted together
Base die heater will be individually pinned

TS Pinouts



Pin locations (refer to the netlist spreadsheet)

Reserved for Vendor specific Thermal sensor (ex. TSVEM, or optional C4EM etc.)

Motions

- Motion 1
  - HBM4 Mechanical Test Vehicle must support at least TSVDC, EDM, C4DC, IMAX, Thermal Sensors, and Heater structures

- Motion 2
  - TSVDC, EDM, C4DC, IMAX, Thermal Sensors, and Heaters structures of HBM4 Mechanical Test Vehicle support following design requirements defined as under below,
    - 2-A: C4DC (Page 4 to 6)
    - 2-B: TSVDC (Page 7 to 11, Table on the page 8)
    - 2-C: IMAX (Page 12 to 15, Table on the page 15)
    - 2-D: EDM (Page 16 to 19, Table on the page 17)
    - 2-E: Thermal Sensors and Heaters (Page 20 to 29, Tables on the page 22, 24, 26, and 27)

END OF DOCUMENTS