01 This moment in computing history
02 Silicon photonics to drive progress
03 CPO and challenges
04 New ideas are needed

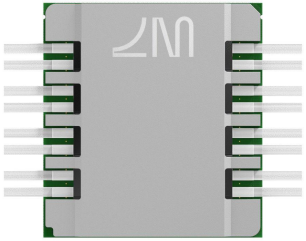
1 TEAM

2 OFFICES

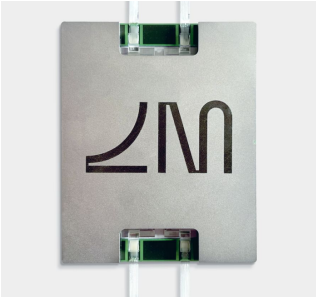
Boston

Mountain View

2 PRODUCTS

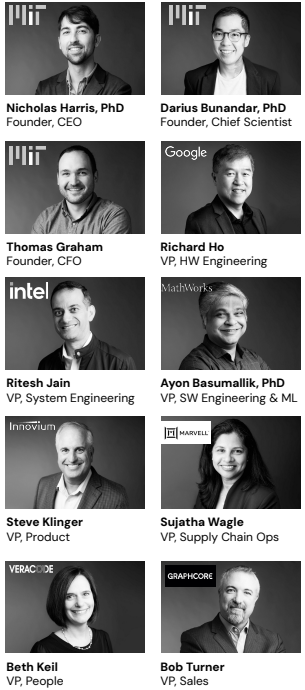


Passage

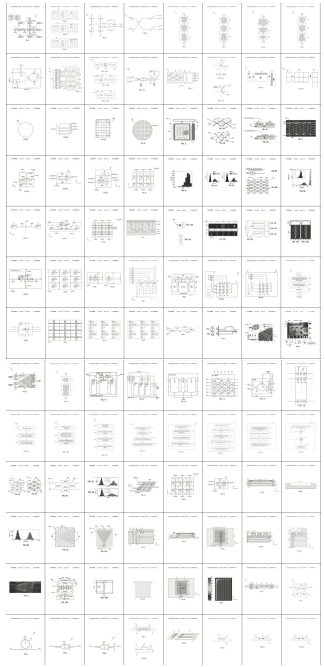


Envise

125 EMPLOYEES



150 PATENTS



$300mm Raised

Sequoia
GV (Google Ventures)
Spark Capital
Matrix Partners
Viking Global
Hewlett-Packard Enterprise
Massachusetts Institute of Technology
Stanford University

This moment in computing history.

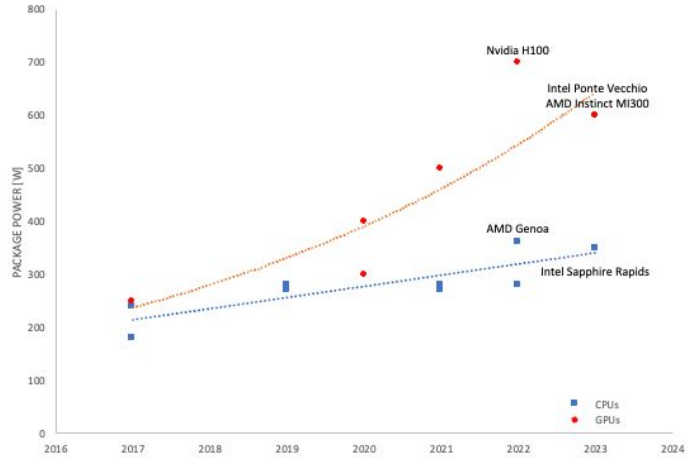
Interconnect is being transformed.

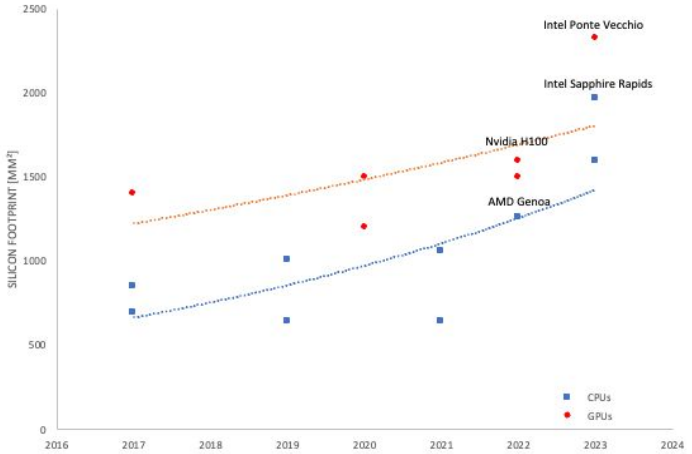
AI and Generative Models

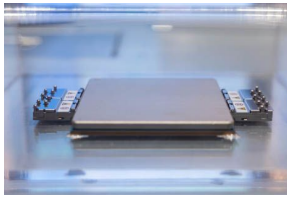
- Workloads spanning 10,000 accelerators running regularly
- Memory capacity, BW requirements exploding
- HBM and network I/O fighting for scarce shoreline
- Imbalanced memory, compute, networking → poor datacenter utilization
- Networking an increasing fraction of datacenter capex
- AI system costs are exploding; biggest companies spending billions
- Cost per user for AI workloads driving down cloud margins

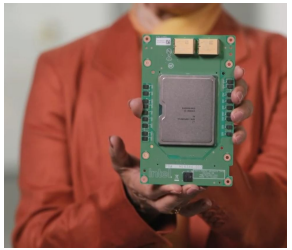
Dennard and Moore

- We're getting more transistors, but we can't use them
- From 300W to 800W in 6 years; spread these hot potatoes out
- Cost per chip ballooning
- Huge packages needed to increase single chip performance
- Water cooling is now standard in AI/HPC; immersion is next



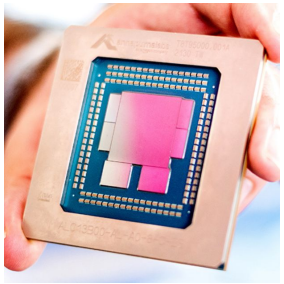


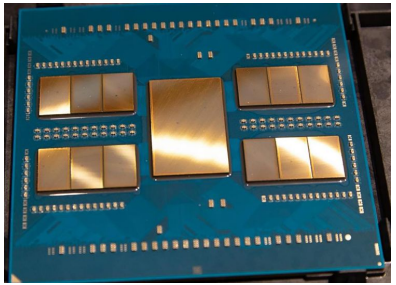


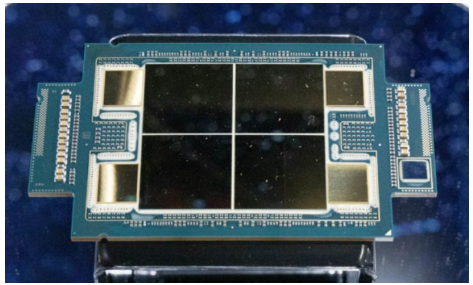


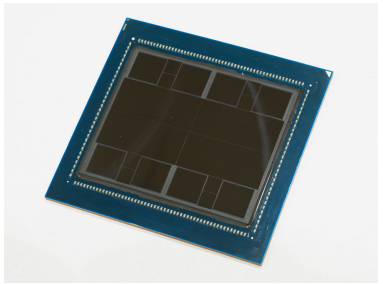
Packaging Defines Performance

- The competitive advantage of a chip company increasingly depends on its packaging capabilities.
- How many chiplets? Package body size? Max power delivery?
- Chip I/O bandwidth is capped by max TDP and package area.







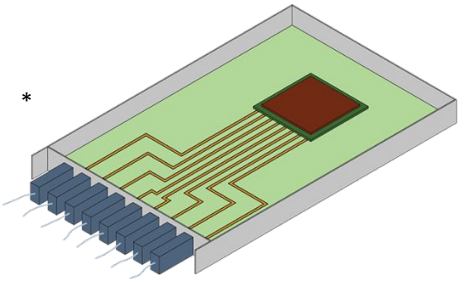


Silicon photonics as a tool to drive computing forward.

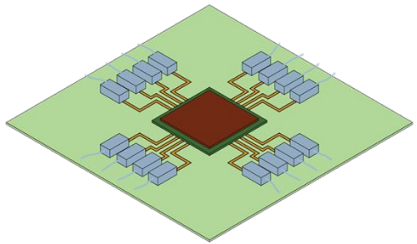
Optics Roadmap

Closer and closer to the chip

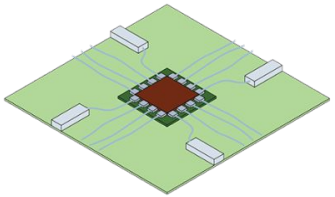
Gen I
Pluggable Optics



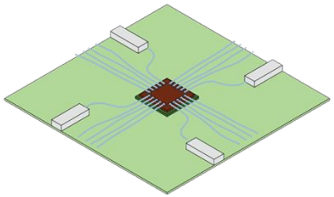
Gen II
On-board Optics



Gen III
2.5D Co-packaged Optics



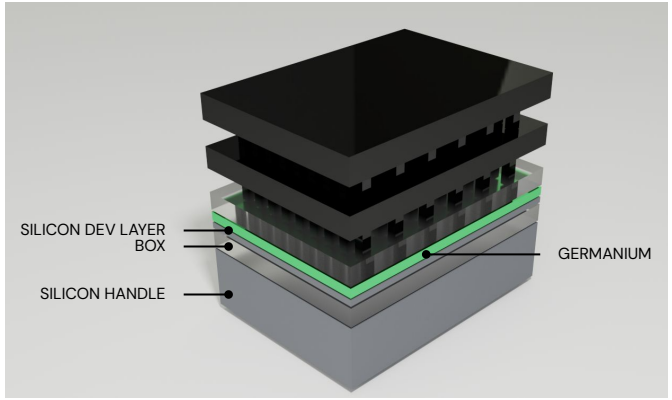
Gen IV
3D Co-packaged Optics

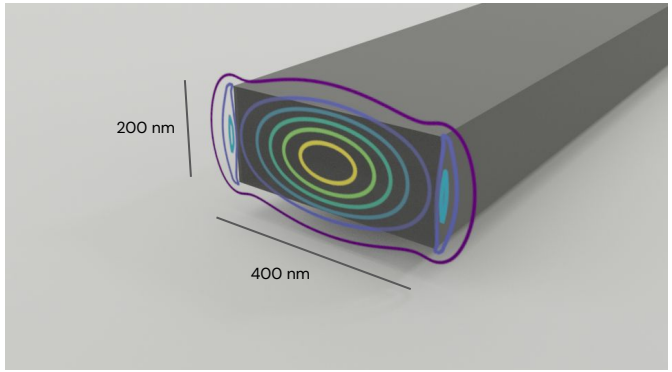


INCREASING BANDWIDTH, ENERGY EFFICIENCY

*Used with permission from Dr. John Bowers and adapted from an article in Applied Physics Letters (2021)

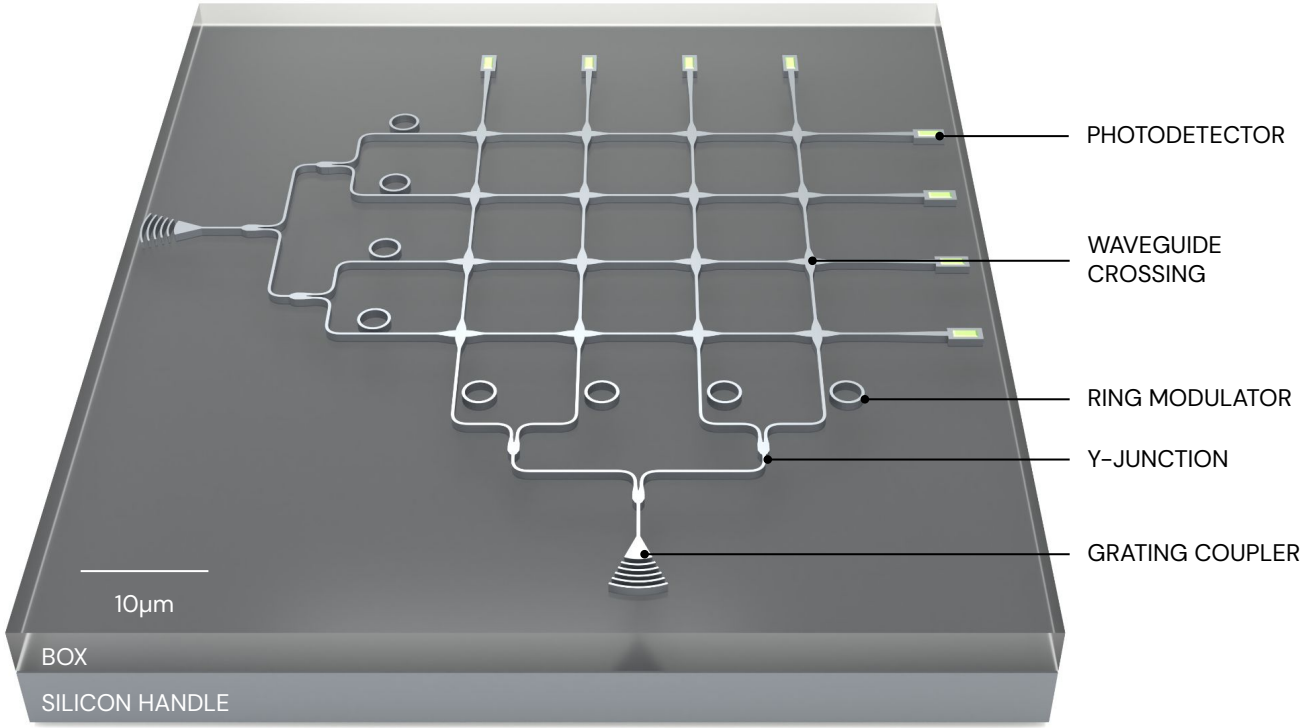
300mm CMOS Fab





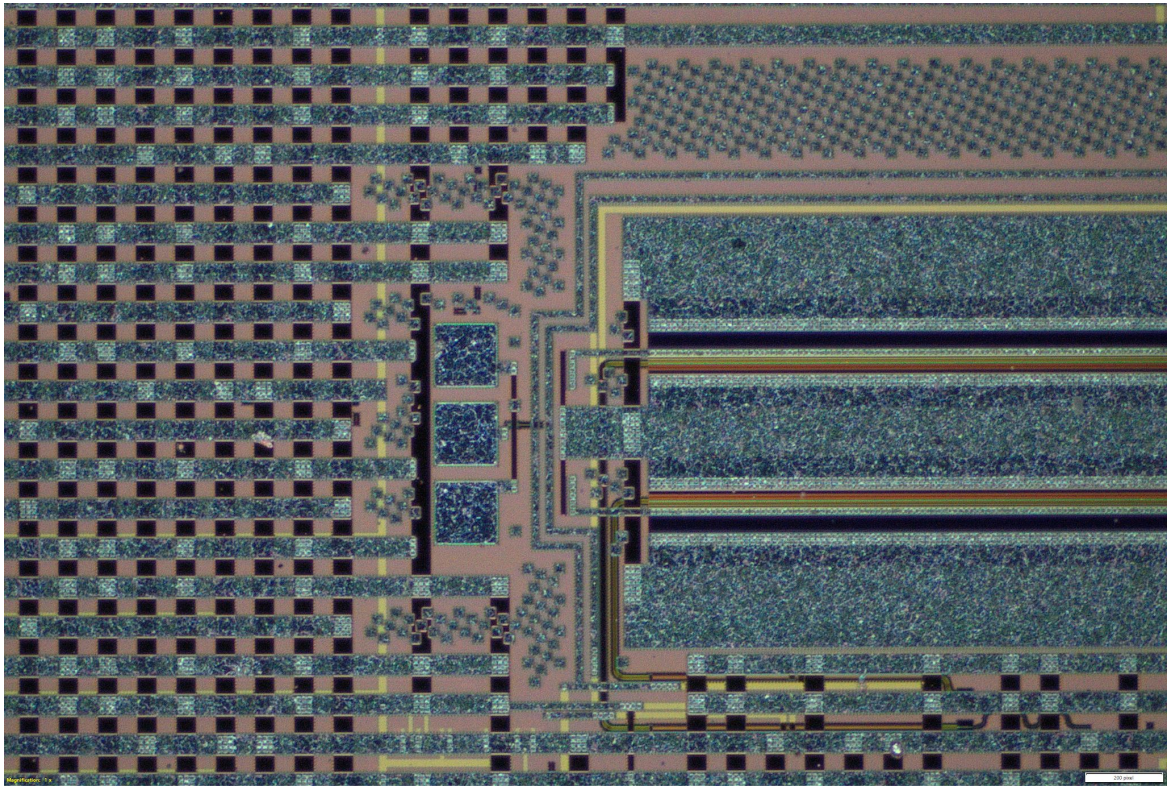
What does silicon photonics look like?

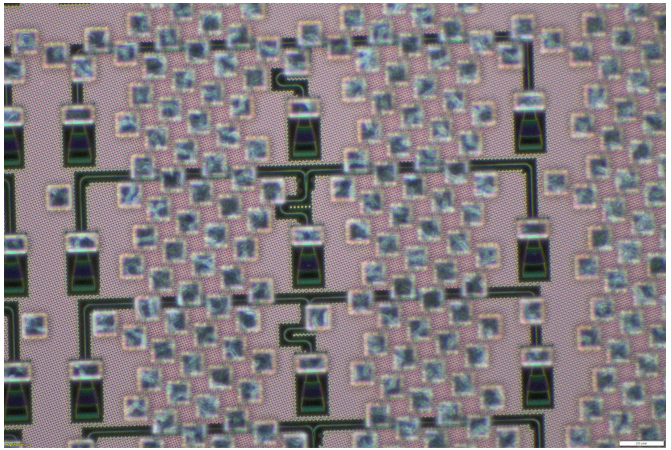
An example of a (random) photonic network

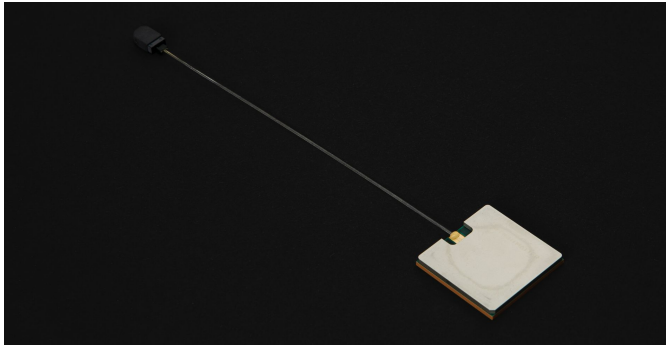


What does silicon photonics look like?

Photographs

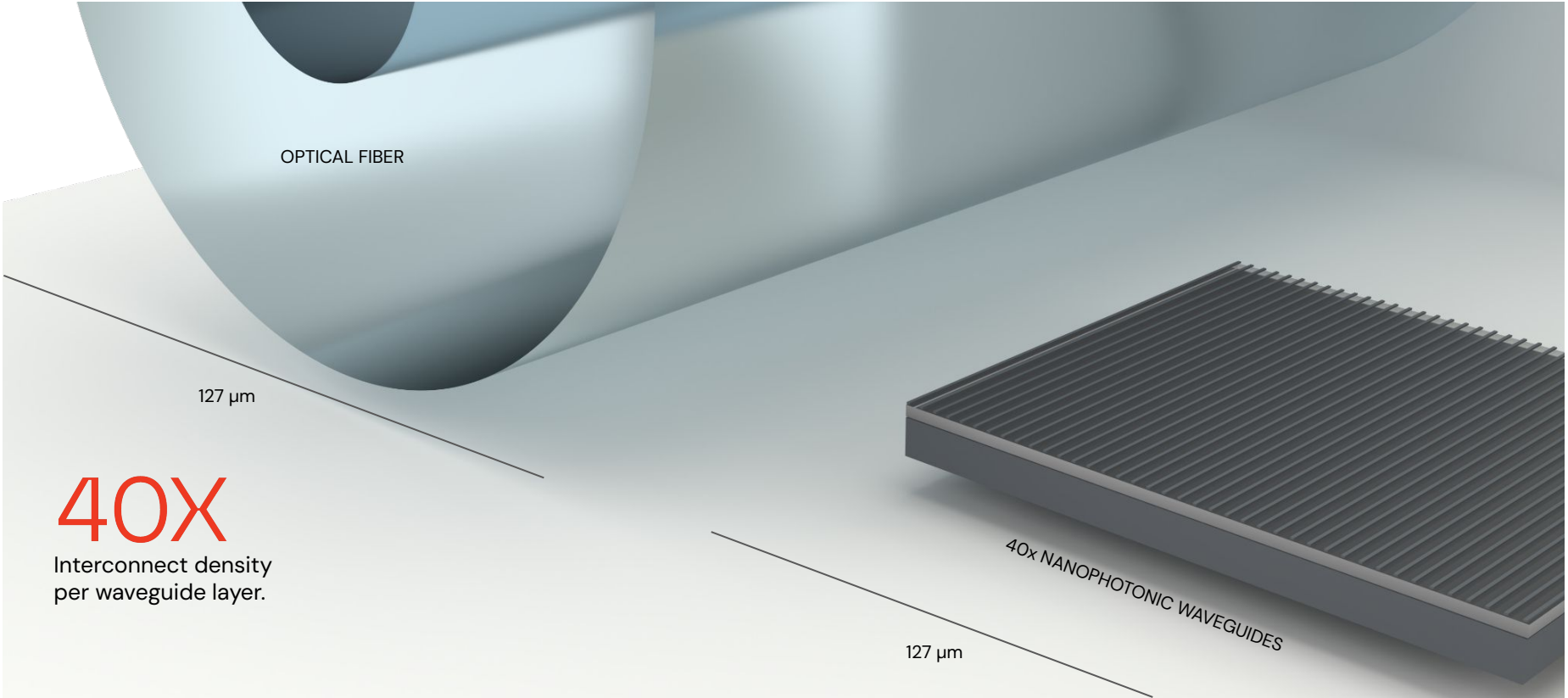






A Sense of Scale

Optical fibers versus nanophotonic waveguides



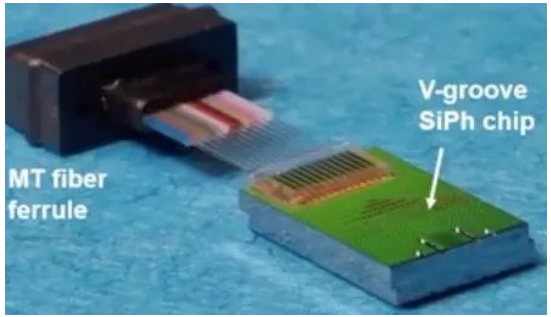
40X

Interconnect density
per waveguide layer.

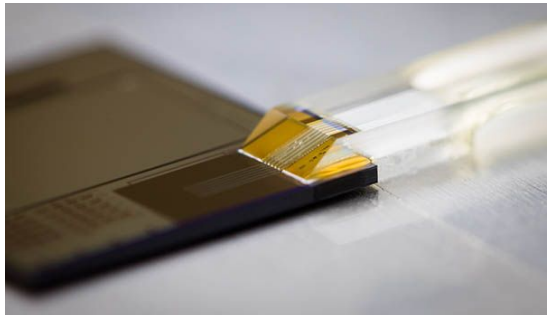
LIGHTMATTER

CPO and challenges.

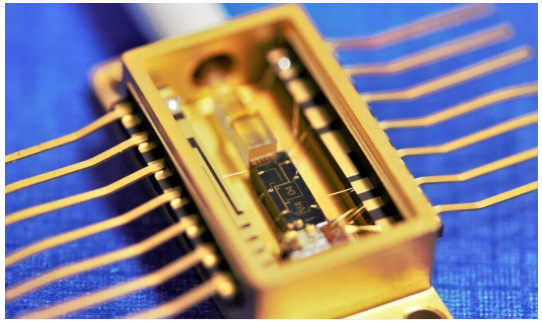
A call to action for the industry.



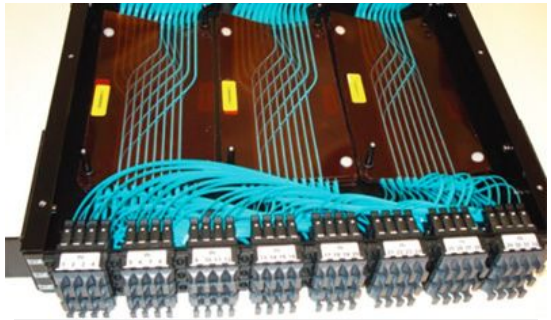
PACKAGING



IN-FIELD REPAIR



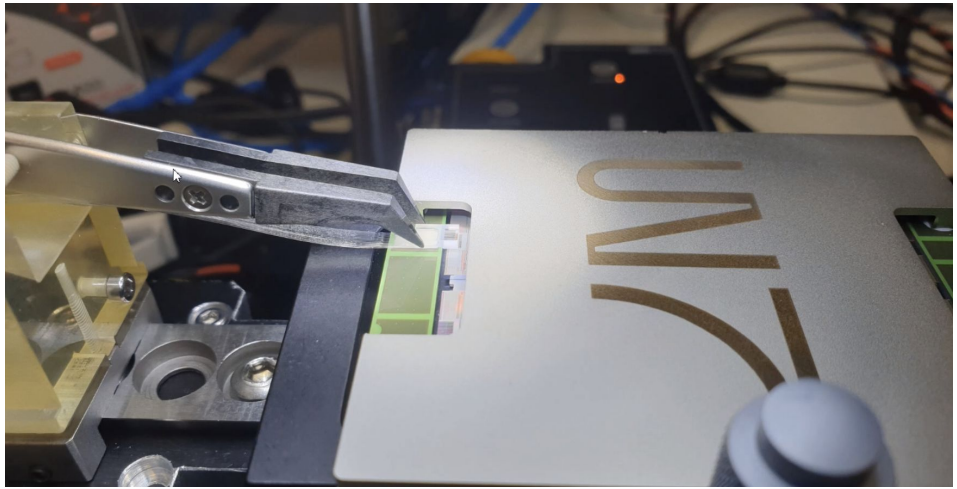
LASERS



FIXED NETWORK TOPOLOGIES

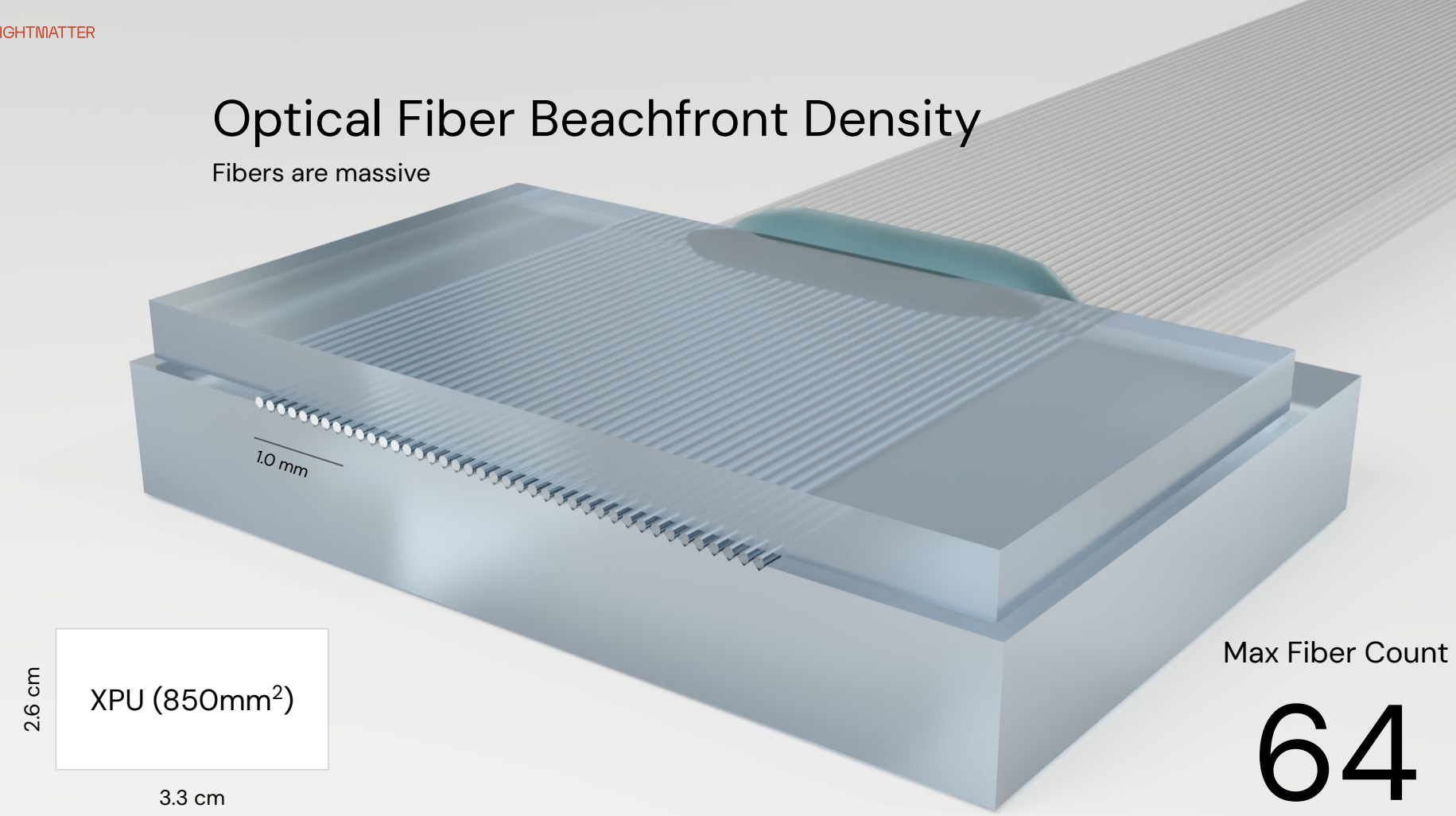
Optical Fiber Attach

An industry-wide challenge



Optical Fiber Beachfront Density

Fibers are massive

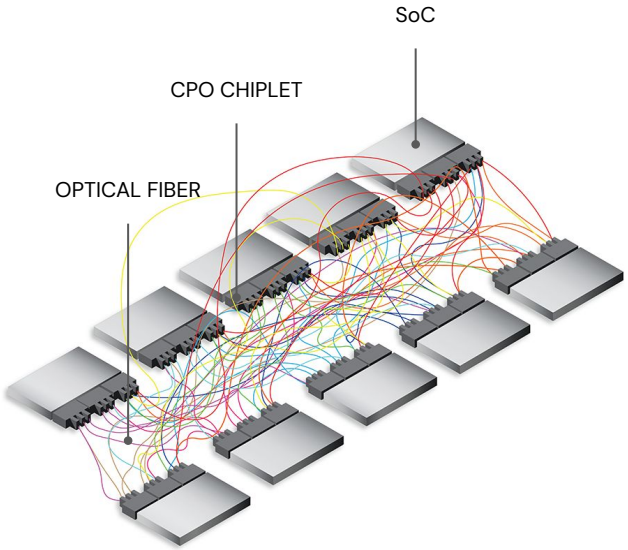


Max Fiber Count

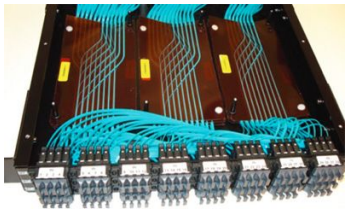
64

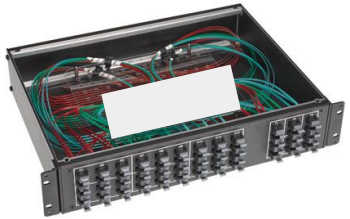
Optical Fiber Management

Serviceability, manufacturability, yield



CO-PACKAGED OPTICS ALL-ALL

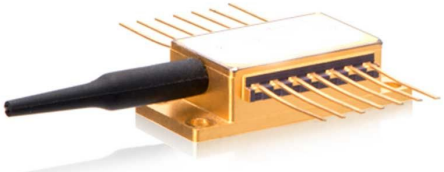


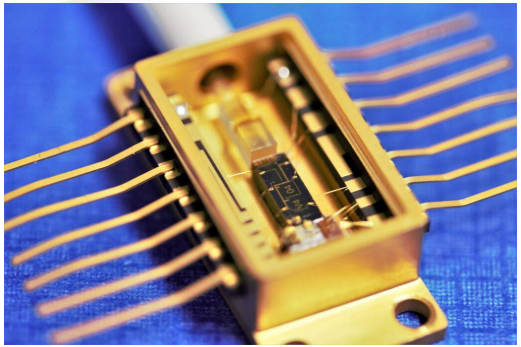


Lasers

- Performance
  - Max 8 colors
  - ~50 mW per laser
  - Max 8 lasers per laser chip
- Packaging and Form Factor
  - Too many laser modules to power just one chip's I/O.
  - Primitive packaging (wirebond)
  - Limited thermal budgets
  - Small mode field diameters for fiber coupling
  - Supporting components require board real estate
- Functionality
  - Color Multiplexing in laser die not generally available

They have wings but do not fly.

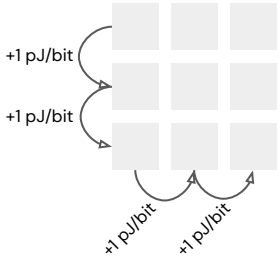




Chiplets and Co-packaged Optics Needed

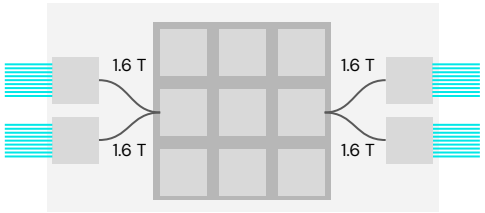
Challenges

MORE HOPS, MORE ENERGY



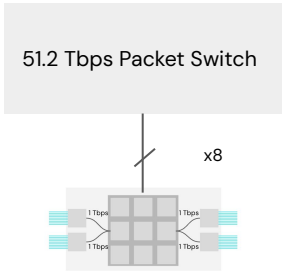
Each chiplet hop adds to communications energy consumption. Building large chiplet arrays this way will incur significant energy costs.

CHIPLET XPU & CPO



- Fibers have low beachfront density
- More wavelengths, more BW
- Static interconnect

FEW CHIPS PER SWITCH



Only 8x CPO enabled chips saturate an entire 51.2 Tbps switch. Compute to switch ratio is poor.

Supply Chain

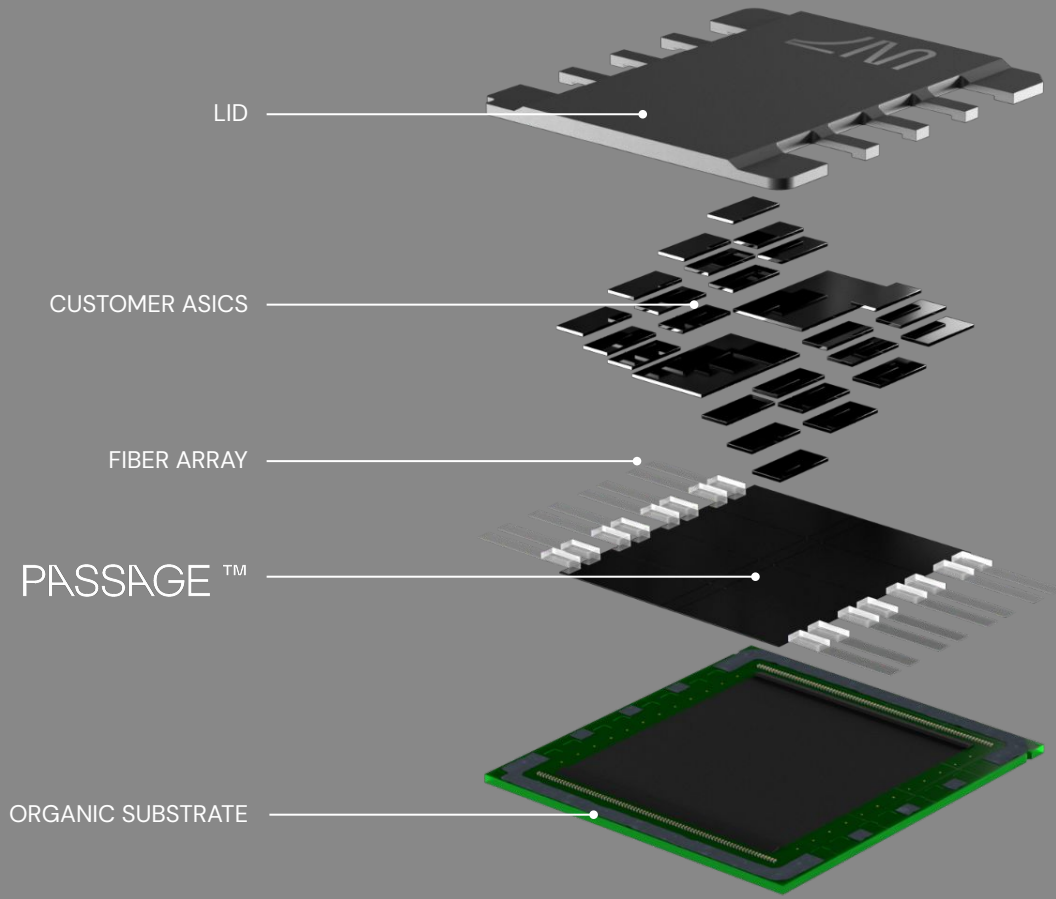
- Is the photonics supply chain ready to support the growth it is about to see?
- Boutique players often have the tech needed for scale.

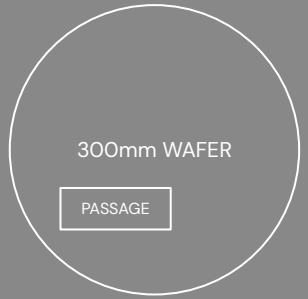
New ideas are needed.

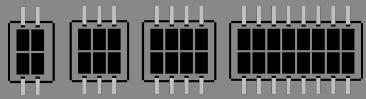
Recap

- Per-chip performance must scale. Chiplet packages can only get so big (latency, power)
- 10,000 GPU clusters are common place. I/O BW and latency must scale
- Shoreline limitation on BW
- CPO is growing the package footprint. Limited by beachfront.
- Fiber management is a major issue.
- Optical circuit switching is increasingly viewed as a path towards ultra-high performance, configurable interconnect.

How can you address all of these challenges in one pass?







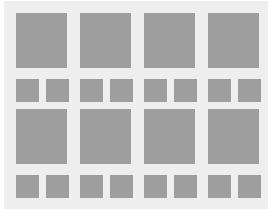
Uniform architecture allows flexible dicing based upon end application.

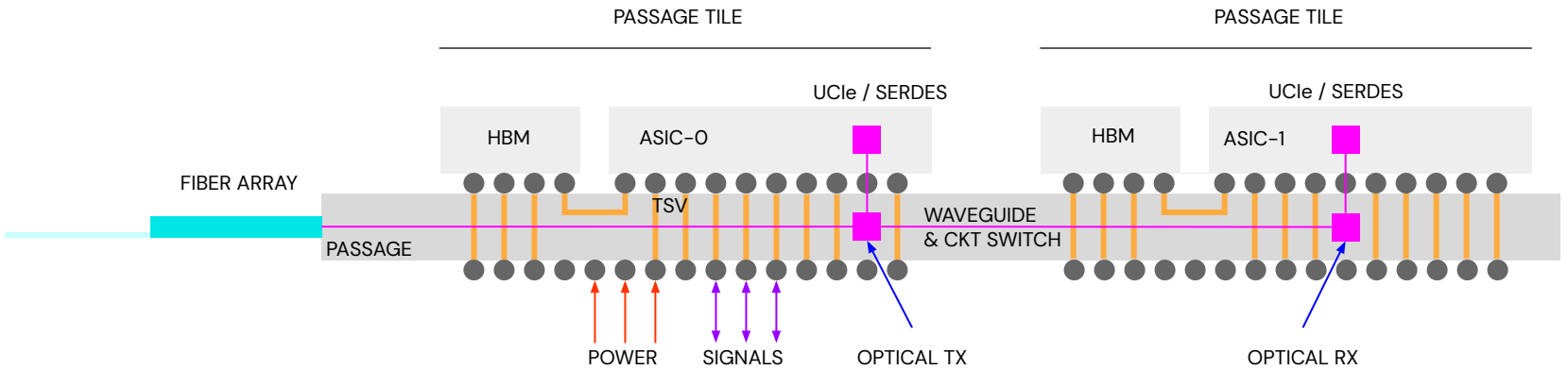
UCIe

Cross Section

Chip-on-wafer Packaging

TOP VIEW

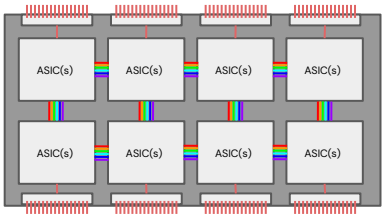




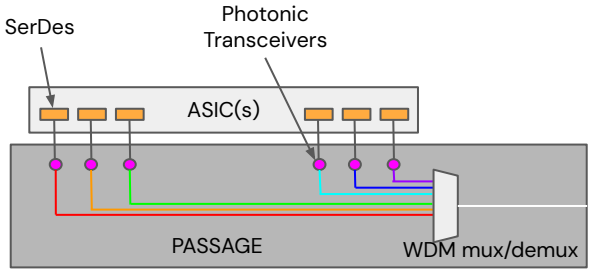
- Up to 700W of power delivery per ~800mm^2 area via TSVs.
- Cooling solution depends on tile ASIC TDP.

Photonic Datapath

Supported Speeds

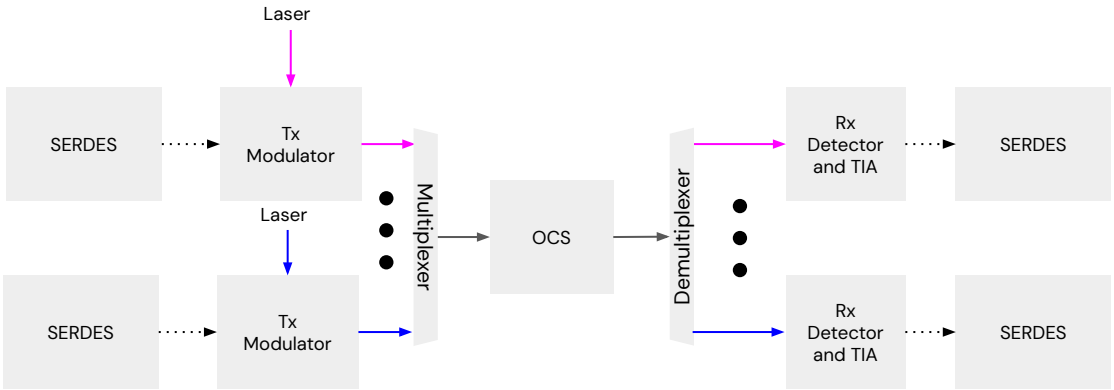


Top View



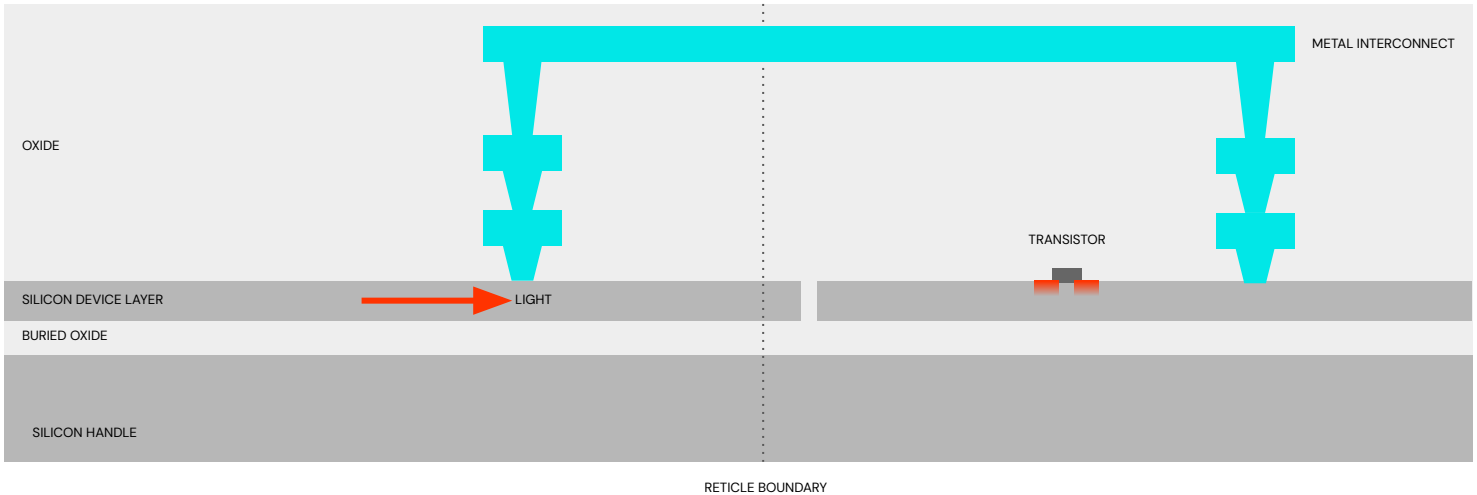
Side View

Modulation format	NRZ	PAM-4
Bandwidth per TX/RX (transceiver) pair	56 Gbps	112 Gbps
Wavelengths	8λ @ 200 GHz spacing	8λ @ 200 GHz spacing
Bandwidth per bank (of 8λ or 1 waveguide)	900 Gbps BiDi	1.8 Tbps BiDi
BER	10^{-15} (no FEC)	10^{-6}



How it works

Waveguide and metal stitching



0.004 dB

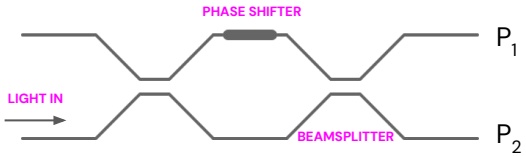
loss per reticle boundary crossing.

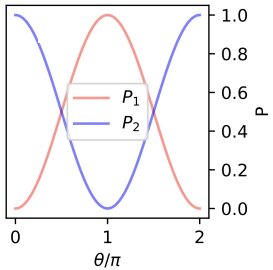
How it works

Optical Circuit Switching

MACH-ZEHNDER INTERFEROMETER

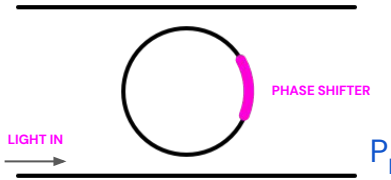
A spatial-mode router





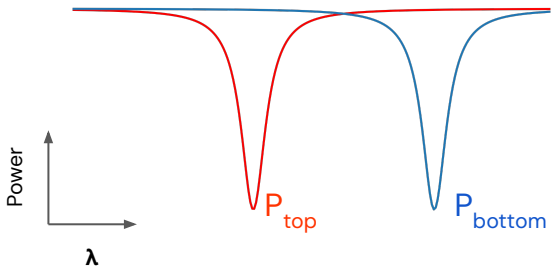
RING RESONATOR

A spectral-mode router



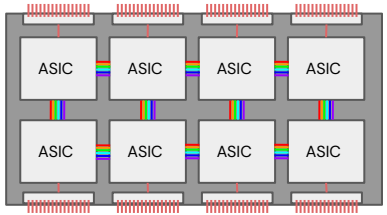
P_{top} (On Resonance)

P_{bottom} (Off Resonance)



Reconfigurable Topologies

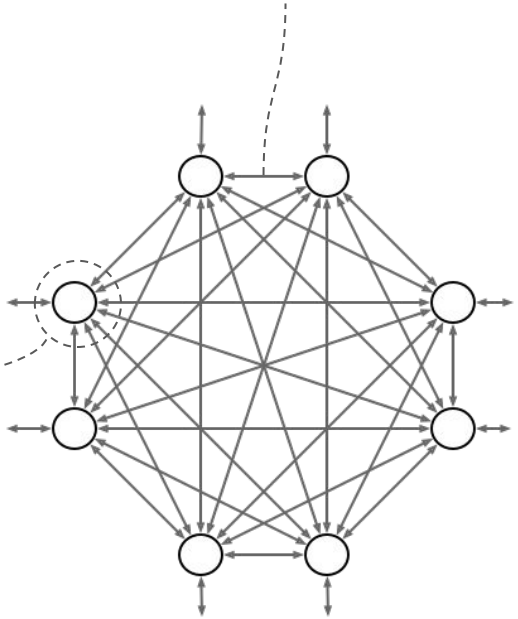
Optical Circuit Switching



Top View

1 TX/RX banks per line:
900 Gbps (NRZ)

Total bandwidth per ASIC:
7.2 Tbps (NRZ)

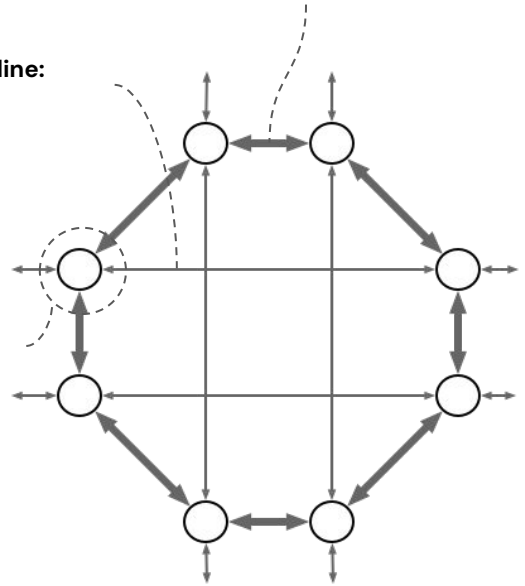


All-to-all configuration

3 TX/RX banks per line:
2700 Gbps (NRZ)
3x the original bandwidth

1 TX/RX banks per line:
900 Gbps (NRZ)

Total bandwidth per ASIC:
7.2 Tbps (NRZ)

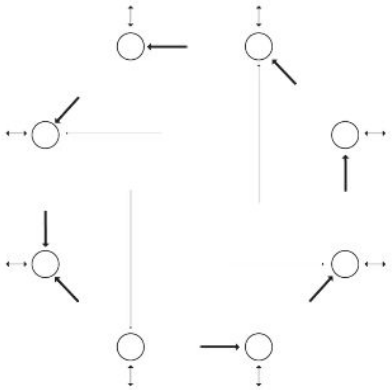


"1-D ring" configuration

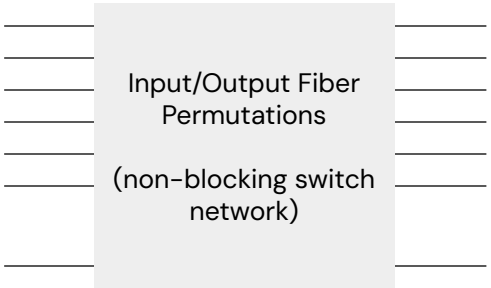
Reconfigurable Topologies

Optical Circuit Switching — Passage™ Native

INTRA- AND INTER-PASSAGE OCS

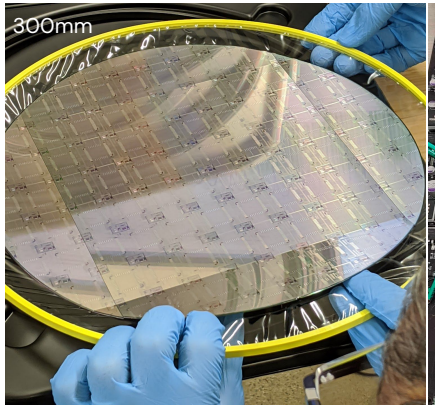


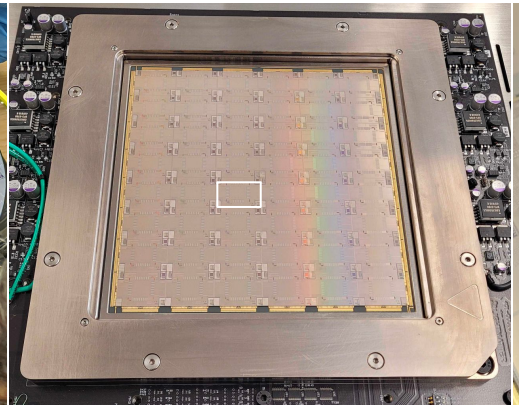
OPTICAL FIBER OCS

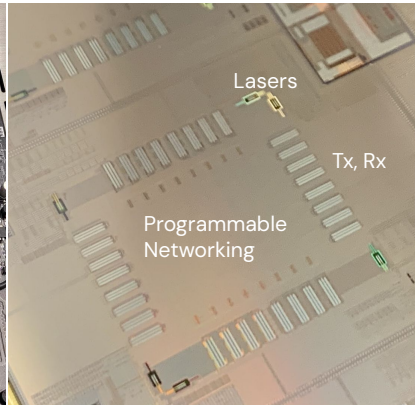


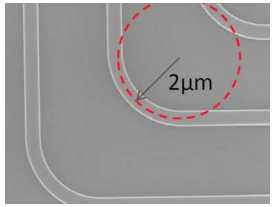
First-Generation Passage

The world's first photonic wafer-scale interconnect









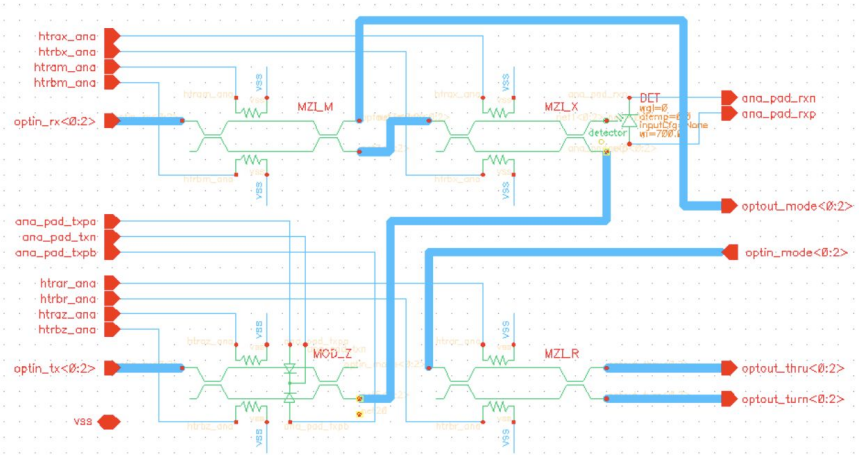
Photonic waveguides with ~4 µm pitch.

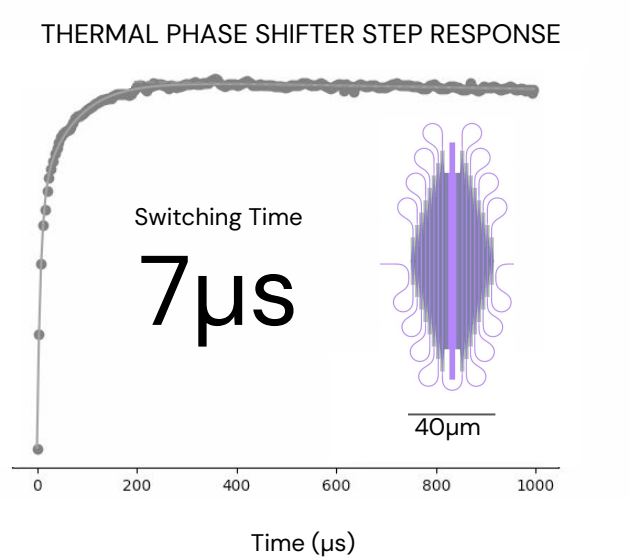
Passage™ Alpha Silicon

- <50 Watts
- 32 channels per site, 1.024 Tbps
- 32 Gbps per channel NRZ
- 48 x 800mm^2 tiles
- 288x 50 mW Lasers
- 6,144 DACs
- 6,144 MZIs
- 150,000 photonic components
- JTAG interface
- Integrated Lasers, transistors, photonics
- Programmable interconnect topologies

Circuit Switching

Controller and device performance



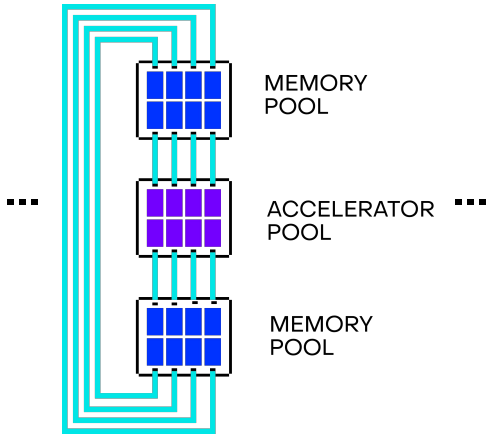


...AND THERE'S A PATH TO NANOSECONDS.

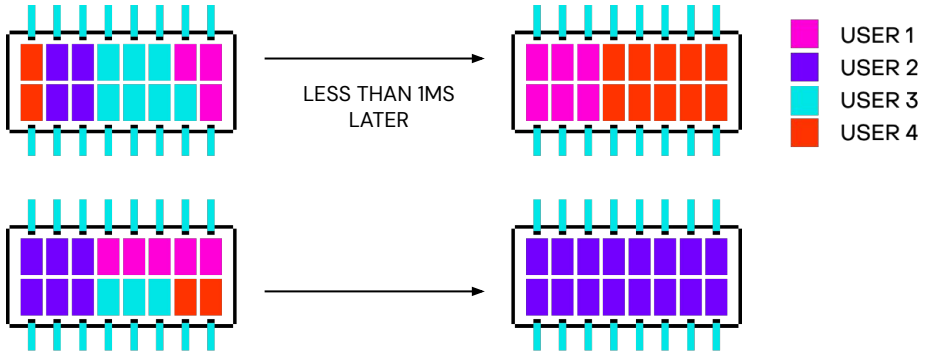
Solutions LM is Driving

A variety of applications

DISAGGREGATION



DYNAMIC COMPUTE ALLOCATION & AIR GAP ISOLATION



What is Passage?

Passage is a 3D co-packaged optics technology that combines a **self-contained** active optical interposer, advanced packaging technology and state of the art light sources to profoundly increase the capability of your ASICs.

- Multiplying bandwidth density
- Increasing serviceability
- Enabling volume manufacturing
- Reducing pJ/bit
- Reducing package size

THANK YOU