Level 4 Autonomous Driving SoC, leveraging chiplet, advanced package and UCIe

Vinayak Agrawal, Francois Piednoel, Igor Elkanovich, Dwaipayan Sil, Mirza Jahan

intel

ADAS
## Advanced Driving Assistance Systems

Advanced Driving Assistance Systems
From Level 2 to Level 4

- Society of Automobile Engineers Defines various levels of ADAS automation

- Many cars in showrooms today have Level2 ADAS systems

- By 2030, about a tenth of the cars are estimated to have Level4 ADAS by some estimates' lowest estimates are about 2%

- Compute requirements for Level4 ADAS systems are expected to be in over 2000TOPS range

LEVELS OF DRIVING AUTOMATION

Human driver monitors the driving environment			Automated driving system monitors the driving environment		
0	1	2	3	4	5
NO AUTOMATION	DRIVER ASSISTANCE	PARTIAL AUTOMATION	CONDITIONNAL AUTOMATION	HIGH AUTOMATION	FULL AUTOMATION
The human driver performs all the aspect of the dynamic driving task.	The human driver performs the driving task with some driving assist features	The vehicle has automated functions like acceleration and steering. The driver still monitors all driving tasks and can take control at any times	The vehicle performs most of the driving tasks but the driver must be ready to take the control of the vehicle at all times with notices	The vehicle performs all the driving tasks under certain conditions. The driver intervention is not necessary, but the driver's attention is still required	The vehicle performs all the driving tasks under all conditions. The driver intervention or attention is not required
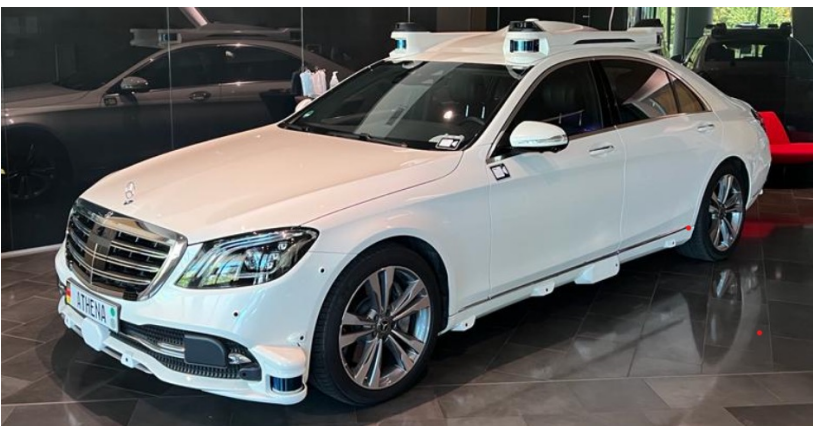
Mercedes Level4 test vehicle
Several Dozen sensors

HPC: Auto vs Datacenter – what is different?

- Regulated Industry:
  - Safety regulations NHTSA, NTSB and other agencies world over
  - Consumer protection - "Lemon Law" in US, state laws
  - Tied at-the-hip with insurance industry
  - Reporting requirements

- Very high-tech consumer goods, with long use life
  - More software than a PC
  - Brands matter a lot

- "Ecosystem" R&D model:
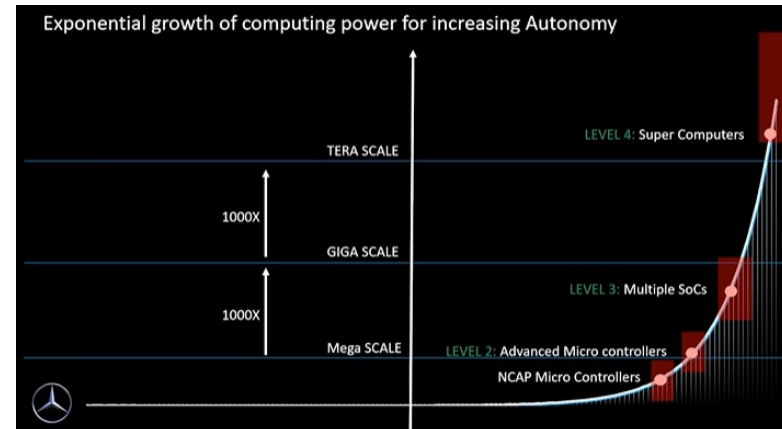 - Lots of re-use between rivals

- Relatively New – Growing FAST

Reliability

↓

Power

↓

Cost

Exponential growth of computing power for increasing Autonomy

TERA SCALE

1000X

GIGA SCALE

1000X

Mega SCALE

LEVEL 4: Super Computers

LEVEL 3: Multiple SoCs

LEVEL 2: Advanced Micro controllers

NCAP Micro Controllers

The New Moore's Law

Gordon Moore Predicted "Day of Reckoning"

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected

Cramming More Components onto Integrated Circuits
April 19, 1965 issue of *Electronics* magazine (Vol 38, page114-117)

Die Scaling slowing

- Scaling has significantly slowed over the last few years

  - SRAM bitcell sizes are not reducing any more

  - Analog Circuit sizes increase

  - Overall node-to-node gains are of the order of 1.3x to 1.5x (used to be more than 3x 15yrs ago)

- While system requirements increase, Moore's law no longer helps keep chip sizes in check
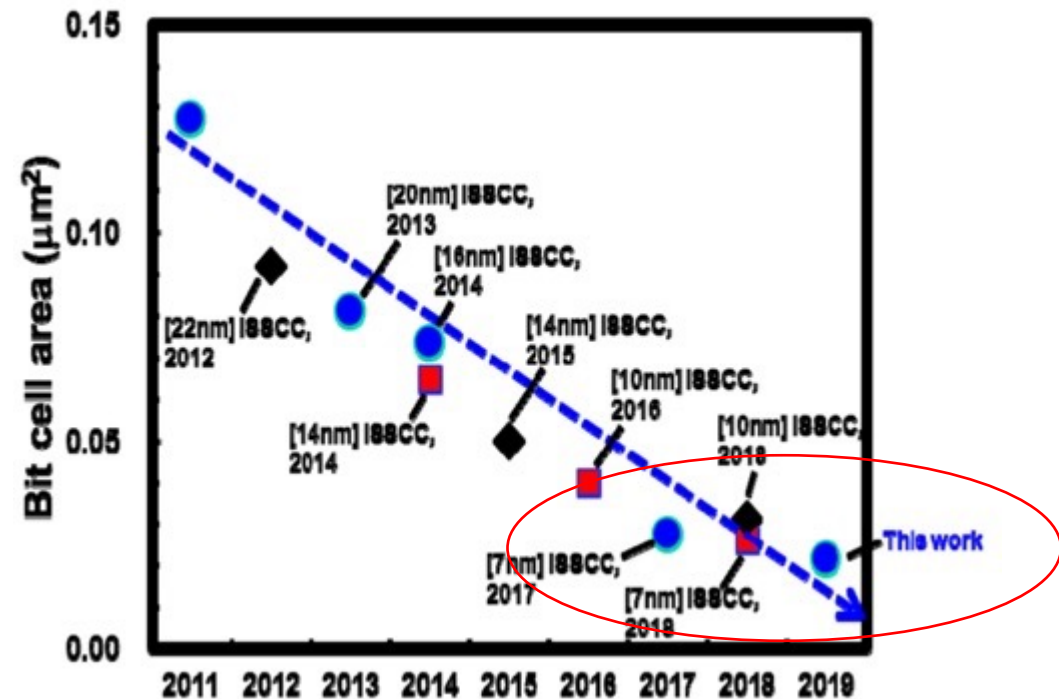
TSMC's 5nm 0.021um2 SRAM Cell Using EUV and High Mobility Channel with Write Assist at ISSCC2020 - SemiWiki

Large monolithic SoC

1. In photo-lithography, only a part of the wafer, called reticle is exposed at a time. Standard reticle size is 25mm*30mm max
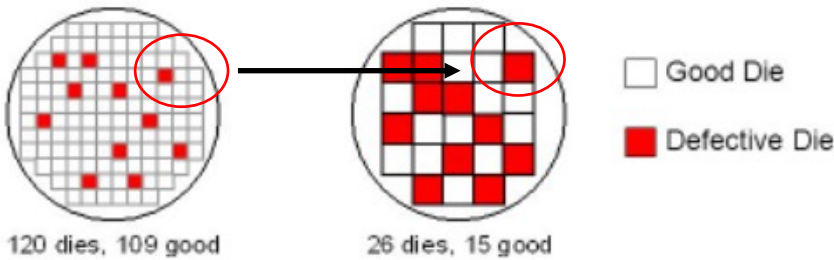
Die Size [mm2]	100	200	400
Mature Yield	REF	-13%	-32%

2. Wafers always have a few defects

- Yields of larger chips are worse for the same number of defects

3. Different nodes are optimal for different purposes

- IO and analog are better off with older and more mature nodes

- High performance compute typically requires state of the art logic node

Multi-Chip ADAS Systems

Intel Confidential

Multi-Chip PCB

- **Make specialized chips**
  - CPU, GPU, Accelerators, Ios

- **Connect them on a PCB**

Chips need to be connected to each other

- **Power:**
  - State of the art SerDes IP takes 5.5pJ/bit @100% bus utilization
  - In other words, a bus with 512GByte/sec average bandwidth, with 20% utilization will consume *110Watts of power*
    - A typical EV cosumes about 5kW total at 55mph

- **Practical Limits:**
  - A PCIe5 Serdes will need about 700 balls (about 400sqmm of package underbody) to support 512GBytes/sec
  - Better Chip-to-chip protocols with very-short range developed with 1/3rd the power; but at the expense of even more BGA balls

Too many chips interconnected – not scalable

Multi-Chip-Package; Chiplets

System In Package

- **Multi-chip-module packages have been around**

  - Camera, Smartphone systems

- **Presently they standard in High Performance Computing**

Intel Sapphire Rapids

- **Multiple Methods:**

  - Standard package with Organic Substrate

  - Embedded Silicon Bridge based

  - Full Interposer based (Silicon or organic)

  - Organic Interposer with embedded silicon bridge based
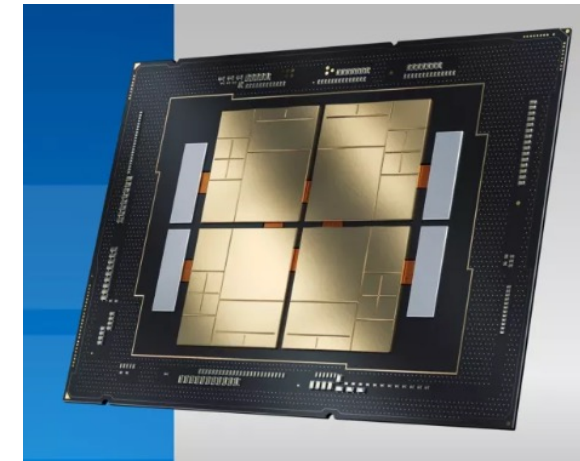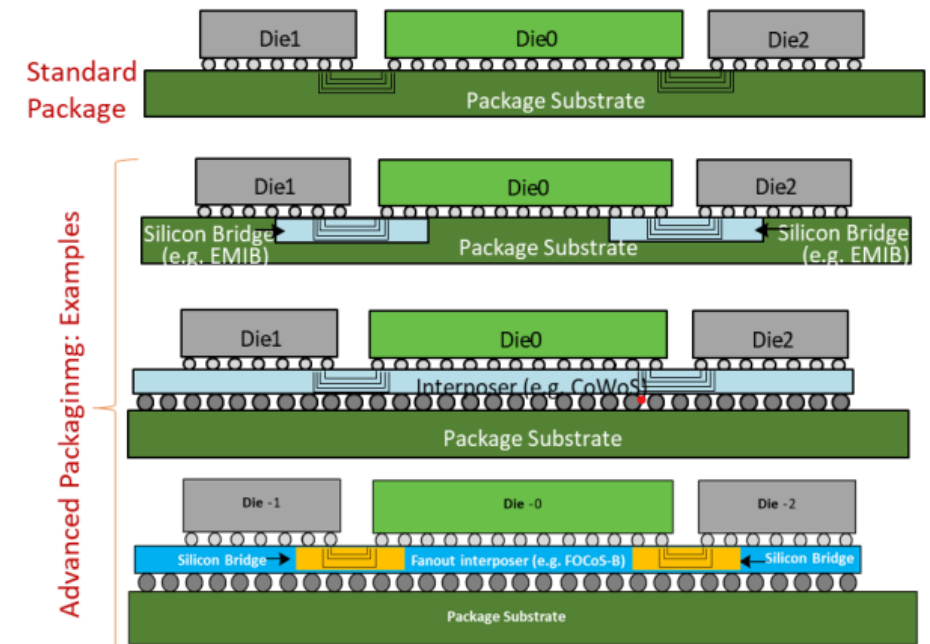
(b. Packaging Options: 2D and 2.5D)

Die Size and Yield

- Disaggregation to improve yield and reduce die cost

- Disaggregation also has area overhead

  - D2D, Scribe/ER etc.

    - $A_{c1} + A_{c2} > A_{die}$

    - ~ 10% area increase

- Example: ~20% yield improvement by disaggregating 400mm^2 die into 2x 220 mm^2 die

Die Size [mm2]	100	400	220
Mature Yield	REF	-32%	-15%

Die
$[A_{die}, Y_{die}]$

Chiplet 1
$[A_{c1}, Y_{c1}]$
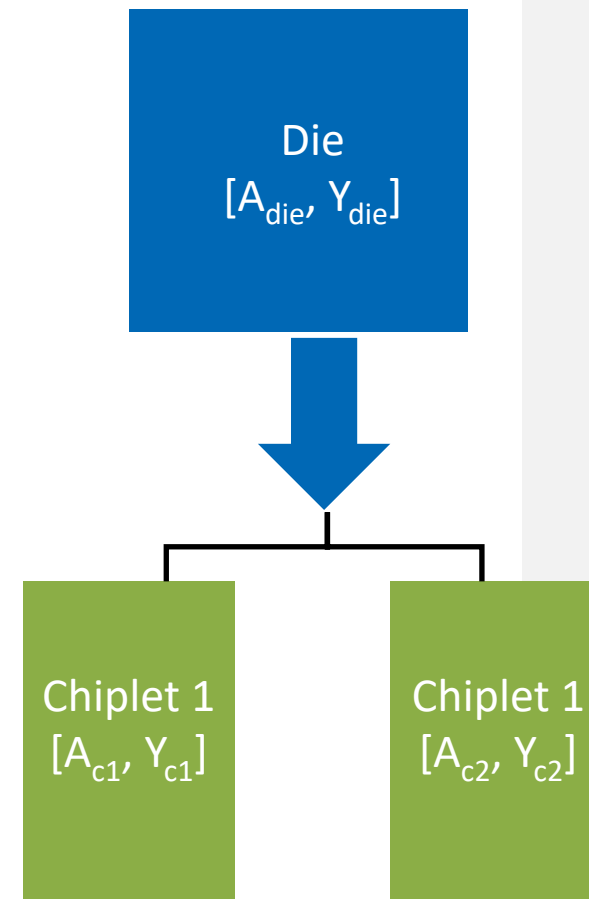
Chiplet 1
$[A_{c2}, Y_{c2}]$

Glink: Connecting Chiplets
GUC proprietary die-to-die IO

- Single ended, source-synchronous DDR signaling

- No Equalizers needed; very simple static phase CDR shared across lanes

- Very low power (0.3pJ/bit); excellent eye margins in 5nm testchip;

- CRC based error handling

- **Special Feature:**
  - Run-time eye measurement for early-detection of failure
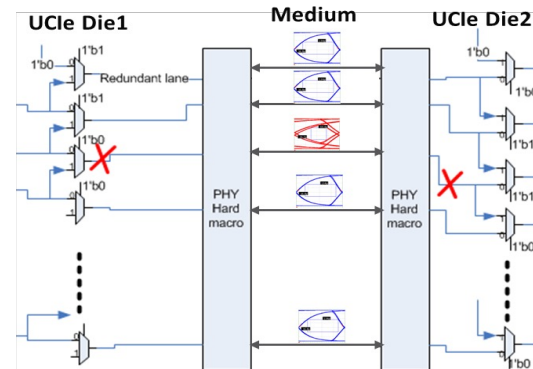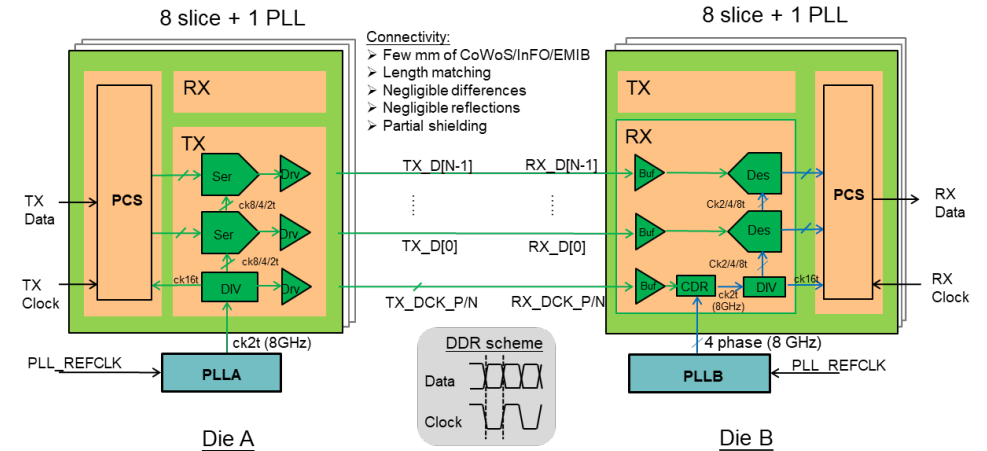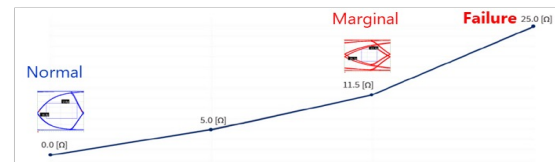
Fault Detection/Prevention
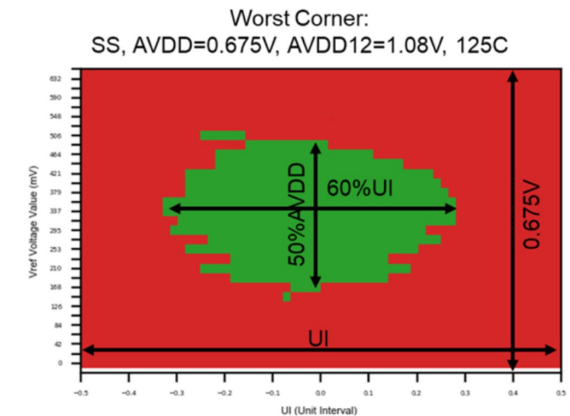
Measure Eye margin 5nm silicon. AVDD is Tx/Rx power supply, AVDD12 is PLL/clocking supply

Automotive Chiplet Interconnect

Safety	Serviceability	Ecosystem and Costs
▪ Goal:	▪ Goal:	▪ Goal:
• Avoid Injury at all costs	• Brand Image	• Share and Re-use chiplets
• Avoid Damage	• Reduced Financial Burden	• Reduce certification costs
▪ How?	▪ How?	• Reduce time to market
• Preventive Monitoring	• Automatic Field Repairs	▪ How?
• Every few months		• Standardize on an open-standard
• All the time		

Universal Chiplet Interconnect Express

http://www.uciexpress.org

UCIe Overview

Standard Specifications

Physical Layers	Protocols	Form Factors	Management
Initial D2D I/O	CXL™/PCIe®		
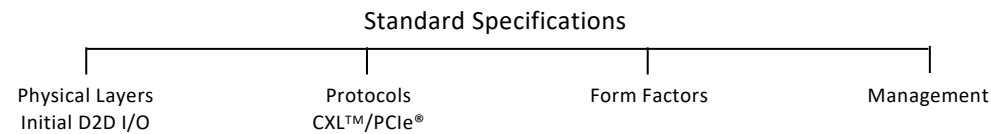
INITIAL FOCUS

- Physical Layer: Die-to-Die I/O with industry leading KPIs
- Protocol: CXL/PCIe for near-term volume attach
- Well-defined specification: ensure interoperability & evolution

CURRENT PLANS

Process Node	IP List	Supplier	F/E View[1]	B/E View[2]	Silicon Report
Intel 3	UCIe PHY	Intel	'23.Q2	'24.Q1	'24.Q3
Intel 18A	UCIe PHY	Eco-system	'23.Q2	'24.Q1	'24.Q3

Auto grade qualification schedule TBD

FUTURE GOALS

- Additional protocols
- Advanced chiplet form-factors
- Chiplet management
- And much more!
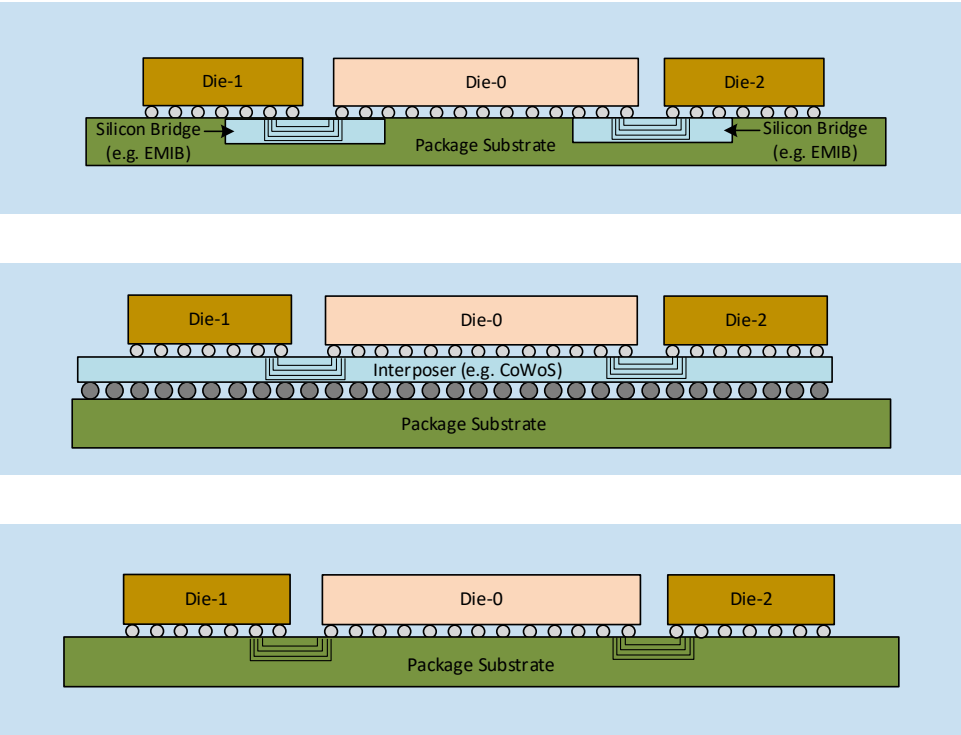
[1] Enables floor planning, includes pin-out and IP bounding box (internally referred as EV)
[2] Updates based on post-silicon learning and optimization (internally referred as FV)

Different flavors of packaging options supported to build an open ecosystem

Jumpstarting UCIe

Intel initiates open standard specification and development

- **Focus of UCIe 1.0 Specification**
  - **Physical Layer:** Die-to-Die I/O with industry-leading KPIs

  - **Protocol:** CXL™/PCIe® for near term volume attach
    - SoC construction issues are addressed since CXL/PCIe is a board-to-board interface
    - CXL/PCIe addresses common use cases
      - I/O attach with PCIe/CXL.io
      - Memory use cases: CXL.mem
      - Accelerator use cases: CXL.cache

  - **Well defined specification**: ensure interoperability and future evolution

STANDARD SPECIFICATIONS

Physical Layers	Protocols	Form Factors	Management
Initial D2D I/O	CXL™/PCIe®		

PROTOCOL LAYER

FIT AWARE / D2D INTERFACE (FDI)

DIE-TO-DIE ADAPTER

ARB/MUX (when applicable)
CRC/RETRY (when applicable)
LINK STATE MANAGEMENT
PARAMETER NEGOTIATION

RAW D2D INTERFACE (RDI)

PHYSICAL LAYER

LINK TRAINING
LANE REPAIR (when applicable)
LANE REVERSAL (when applicable)
SCRAMBLING/DE-SCRAMBLING (opt-in)
SIDEBAND TRAINING & TRANSFERS
ANALOG FRONT END
CLOCK FORWARD

Die-1 Die-0 Die-2
Package Substrate

(Standard Package)

Die-1 Die-0 Die-2
Silicon Bridge (e.g. EMIB) Package Substrate Silicon Bridge (e.g. EMIB)

Die-1 Die-0 Die-2
Interposer (e.g. CoWoS)
Package Substrate

(Multiple Advanced Package Choices)

Die -1 Die -0 Die -2
Silicon Bridge Fanout interposer (e.g. FOCoS-B) Silicon Bridge
Package Substrate

(Different flavors of packaging options supported to build an open ecosystem)

intel foundry services

UCIe Auto

- **Preventive Monitoring**
  - Eye Margin and other measurements supported as part of training
  - Proprietary measurements also supported
  - Register map defined for reporting of per lane (and other) measured data
- **Very low guaranteed FIT rates**
  - "guaranteed" is key
  - Standard will not allow parity based error counters in test mode for BER test
  - Test can be run weekly or monthly in parked car
- **Continuous BER monitoring**
  - Software based per-lane test (in addition to CRC) in mission mode
  - Accurate computation of BER per lane

- **Streaming Mode with CRC**
  - To allow development of protocols other than PCIe/CXL on UCIe
- **Field Repair**
  - Repairability present in 1.0 already
  - Monitoring to turn in into "automatic field repair"

Additions to UCIe in our System

UCIe Auto – In System

- **Link Monitor in mission mode**
  - Analog circuit measurements without breaking link between two chiplets

- **Cloud Based Diagnostics**
  - Measured parameter data will be uploaded to cloud
  - Data analysis across a fleet of cars; across temperature, age, driving conditions, batch

For on-die and on-cloud analysis and storage

Protocol Layer

Flit aware D2D interface (FDI)

Third party Monitoring And Analysis IP

Die-to-Die Adapter	ARB/MUX (when applicable) CRC/Retry (when applicable) Link State Management Parameter Negotiation

Raw D2D interface (RDI)

Physical Layer

| Sideband/ Global | Electrical/AFE [k slices] |

All links working → Link1 retrain → Link2 retrain → Link3 retrain → Link4 retrain → All links working
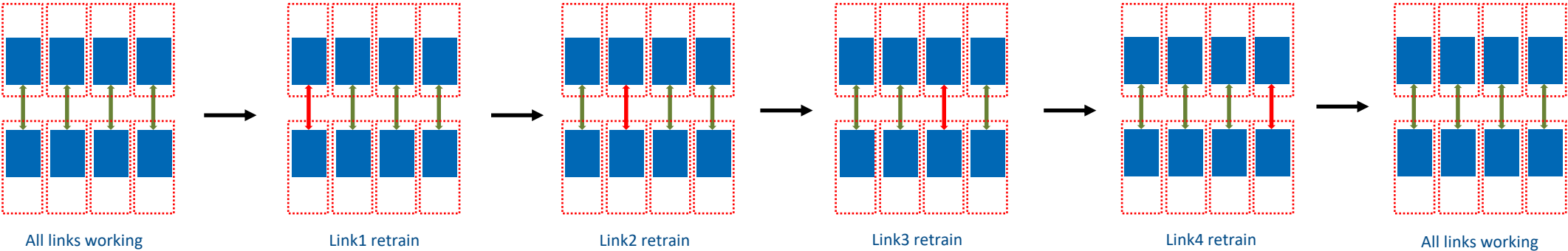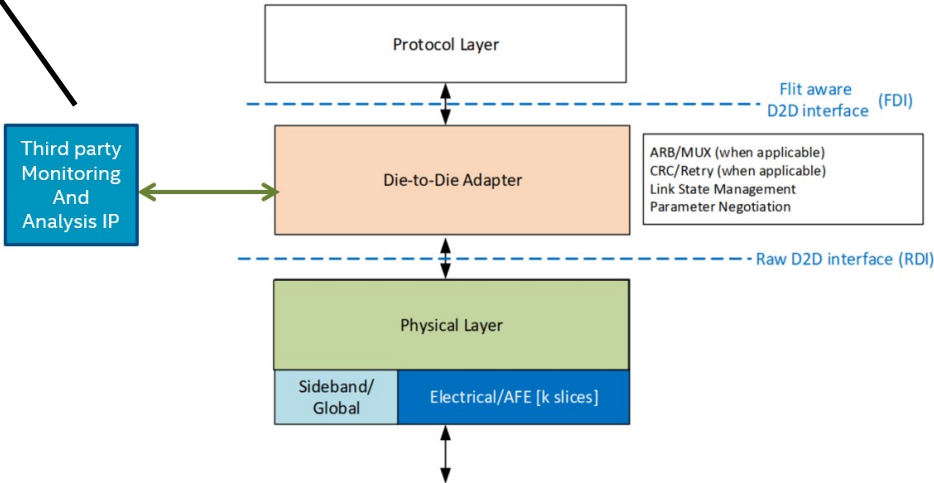
UCIe-Bumpmap

- UCIe in Advanced version defined a bumpmap that allows straight routes between chiplets, of about equal length

- Eases routing design, eliminated skew

- Rotation symmetric (e.g. a die can connect with itself)
  - Two chiplet with compliant bumpmap will be routable if IP locations can be aligned
  - However for multi-module usage, it may not always be possible

Standard Form Factor Defined

- For this program and in future programs we plan to use a 6 module + 1 module form factor as shown

- Total peak bandwidth this can support is over 1TByte/sec (512GByte/sec in each direction) on main link
    - Additional module supported with it's own power supply and higher ECC for Functional Safety subsystems
    - Can connect to 4+1 or 2+1 configurations also

- This will not have rotational-symmetry so additional system requirements needed

Standard 1TBps Auto D2D

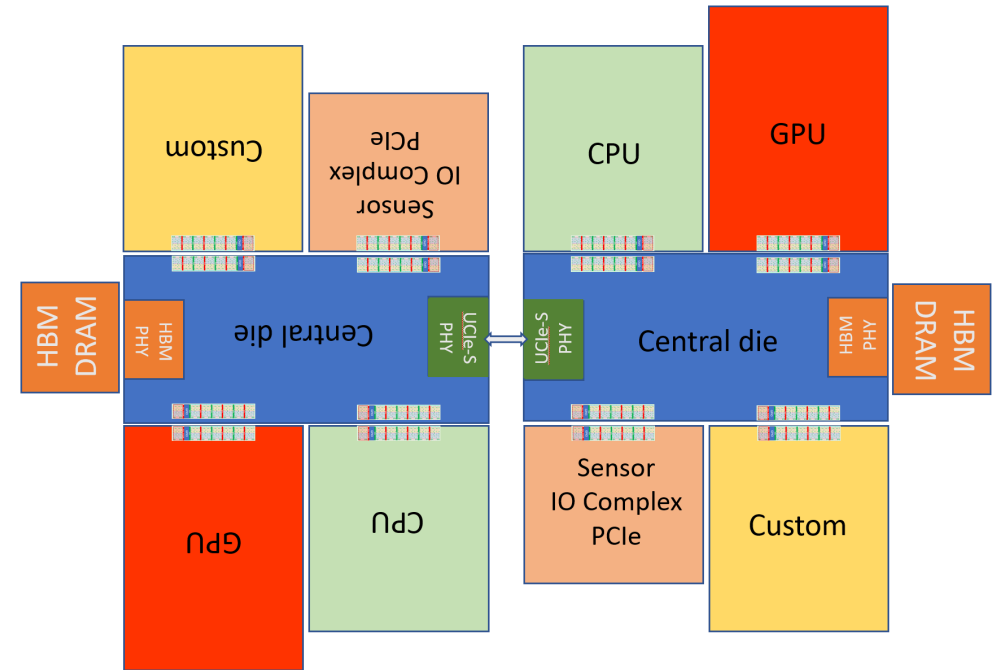Main NOC — FuSA NOC
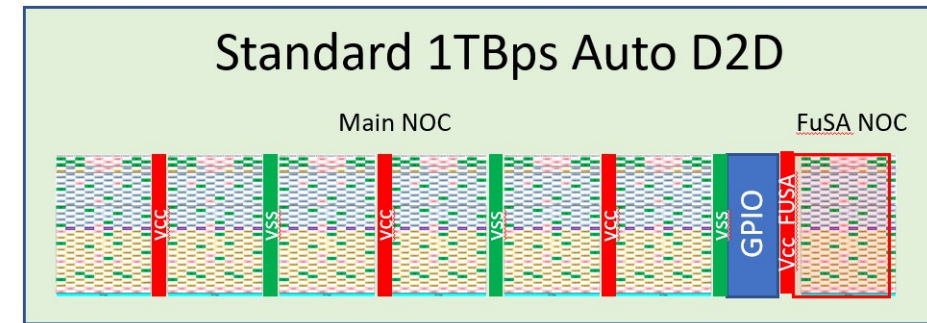
Putting it all Together

Standard Chiplet Based Architecture

- A central die with mirrored (not rotated) 6+1 configuration and "satellite chiplets" with unrotated 6+1 configuration will be used as shown
  - EMIB based package will be used to connect these in a single package

- While exact dimensions are not shown here, total Silicon Area without HBM memory will be significantly larger than 1000sqmm
  - Central die will contain mostly RAM but also Network on Chip and some processing;
  - CPU will be multi-core CPU
  - GPU is a GPU/Tensor chiplet
  - Custom Chiplet is an independent SoC that will support lower power modes (e.g. parked car, or Level 2 driving in conditions where higher is not possible)
  - Sensor/IO complex has interfaces for cameras, radard, Lidars, Ethernet and PCIexpress
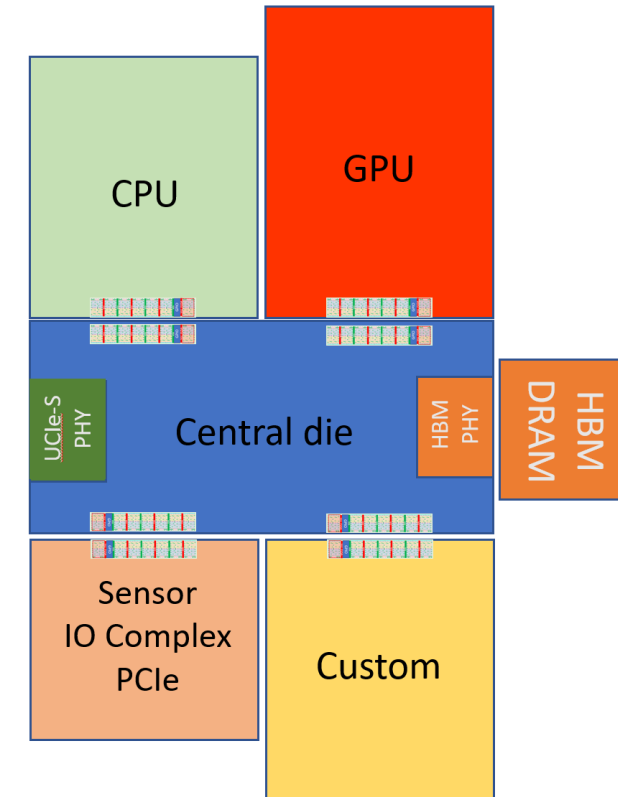
Level 4+ ADAS

- We anticipate adding more features as time go by

- Multiple Central chiplets can be connected within the same package using UCIe-S version of the PHY (designed to work with standard organic substrate)

- The choice of chiplet geometries will allow some mix-and-match capabilities post-manufacture
  - For example, an additional GPU can be used instead of one sensor die

Thank You

Intel Confidential