Status of the Advanced Packaging 2023

Market and Technology Report

YOLE Intelligence

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Part 1/1

IDENTITY CARD

What will you find in this report?

Markets

- Automotive & Mobility
- Defense & Aerospace
- Industrial
- Medical
- Mobile & Consumer
- Telecom and Infrastructure

Frequency update

- Quarterly
- Yearly

Systems tracked

Smartphones
Desktop PCs /Mac
Flash Cards
Laptop Chromebook
Laptop PC/Mac
Tablets
Workstations
Smartwatches
Game Stations
Buses
Light Commercial Vehicles
Passenger Cars (PC)
Routers & Switches
Cloud Computing
Enterprise
HPC
Server - Hyperscale
Server - Enterprise
Server - HPC
Military Drones
Missiles & Munitions
Autonomous Cargos
Autonomous Trucks

Technology

FCCSP
FCBGA
SiP
WLCSP
Fan Out
2.5D
3D
Chiplet
HI
Hybrid Bonding

Depth analysis

System
Module
Sub-module
Component
Process
Wafer
Material
Equipment

Key metrics

- 2018-2022-2028 Timeframe
- Players
- Trends
- Units
- Value
- Wafer
- Market shares
- Supply chain
- Strategy
- Financial analysis
- Business news
- Technology status
- Technology Roadmap

Quick summary

Big player reported record revenues as part of the $44.3 B total revenue of the Advanced Packaging market in 2022, while reducing CapEx spending for 2023 despite entering the chiplet era.

Key Features

The Advanced Packaging industry attained a market value of $44.3 billion in the year 2022. This market is expected to surpass $78 billion by 2028, showcasing a CAGR of 10% during the period from 2022 to 2028.
The largest market in 2022 was the 'Mobile & Consumer' sector, which accounted for more than 70% of the total revenue. However, it is expected that this share will decrease to 61% by 2028 as the 'Automotive' and 'Telecom & Infrastructure' sectors gain larger market shares. These two sectors are projected to be the fastest-growing markets by 2028, with respective CAGRs of 17% and 10%.
In terms of packaging technologies, the primary contributors to the market are flip-chip, 2.5D/3D, and SiP, which are expected to hold a combined market share of over 90% by 2028. Additionally, the top three platforms experiencing the highest growth rates are ED, 2.5D/3D, and flip-chip.

What's new?

New technology platforms added,
New assumptions,
Forecast updated.

GLOSSARY

ABF	Ajinomoto build-up film
AI	Artificial Intelligence
AIoT	Artificial Intelligence of Things
ASIC	Application Specific Integrated Circuit
AR	Augmented Reality
BE	Back-End
BGA	Ball Grid Array
CIS	CMOS Image Sensor
CSP	Chip Scaled Package
CPU	Central Processing Unit
DSP	Digital Signal Processor
DMS	Design Manufacturing Services
DTV	Digital TV
ED	Embedded Die (in laminate substrate)
EMS	Electronics Manufacturing Services
FE	Front-End
FI	Fan-In
FC	Flip-Chip
FO	Fan-Out
FPGA	Field Programmable Gate Array
GPU	Graphics Processing Unit
HB	Hybrid Bond

HBM	High Bandwidth Memory
HD	High Density (Fan-Out) OR High Definition (TV)
HPC	High Performance Computing
HVM	High Volume Manufacturing
I/O	Input/Output
IDM	Integrated Device Manufacturer
IC	Integrated Circuit
IIoT	Industrial Internet of Things
IoT	Internet of Things
KGD	Known Good Die
L/S	Line/Space
LED	Light Emitting Diode
M&A	Merger & Acquisition
mSAP	modified Semi-Additive Process
ODM	Original Design Manufacturer
OEM	Original Equipment Manufacturer
OSAT	Outsourced Semiconductor Assembly and Test
PC	Personal Computer
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PLP	Panel Level Packaging
PMIC	Power Management IC

PWB	Printed Wiring Board
QFN	Quad Flat No-Leads
QFP	Quad Flat Package
RDL	Redistribution Layer
RF	Radio Frequency
SAP	Semi-Additive Process
SiM	System in Module
SiP	System in Package
SMT	Surface Mount Technology
SoC	System on a Chip
SoIC	System on Integrated Circuits
STB	Set-Top Box
TSV	Through Silicon Via
TXVR	Transceiver
VR	Virtual Reality
WB	Wire Bond
WE	Wearables
Wi-Fi	Wireless Fidelity
WLP	Wafer Level Package

ABOUT THE AUTHORS

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COMPANIES CITED*

AMD, Amazon, Amkor, AOI Electronics, Applied materials, Ardentec, Arm, ASE, ASM, Besi, Carsem, China Resources Microelectronic, China WLCSP, Chipmore Technology, ChipMOS, Chippacking, Deca, Forehope, Formosa Advanced Technologies, ESWIN, GlobalFoundries, Global Unichip Corporation, Google, Graphcore, Greatek Electronics, Hana Micron, Hanmi, HiSilicon, Inari Berhad, Infineon, Institute of Microelectronics, Intel, JCET, King Yuan Electronics, LB Semicon Inc., Lingsen Precision Industries, Meta, Micron, Microsoft Corporation, Murata, Nepes, Nvidia, Orient Semiconductor Electronics, Payton Technology, Powertech Technology, Qorvo, Qualcomm, Samsung Electronics, Semco, SFA Semicon, Sigurd Microelectronics, SkyWater, Smart Equipment Technology, Sony, SK hynix, Skyworks, Taiji Semiconductor, Texas Instruments, TianShui Huatian, Tong Hsing, Tongfu Microelectronics Co., Ltd., Tower Semiconductor, TSMC, UMC, UniSem Berhad, UTAC, Walton Advanced Engineering, Wisol, Xinhuicheng, YMTC, Ziguang Hongmao and more.

*non-exhaustive list

REPORT OBJECTIVES

The *"Status of the Advanced Packaging Industry"* is a yearly overview report. The objectives of the report are:

- Advanced Packaging market overview
  - Drivers and dynamics
  - Future applications
  - Disruptions and opportunities
- Supply chain analysis
  - Overview of production by player (IDM, OSAT, foundry)
  - Shifting business models
  - Financial analysis of TOP 30 OSATs
- Technology trends and forecasts
  - Revenue, wafer, and unit forecasts by platform
  - Future development by platform
  - Impact of front-end scaling
  - Scaling and functional roadmaps

SCOPE OF THIS REPORT

System Integration Levels

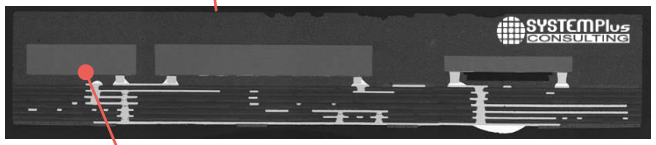
LEVEL 3:
End-System

iPhone 6s

LEVEL 2:
Module/Board

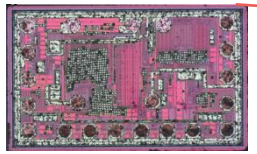
iPhone 6s
PCB

LEVEL 1:
Device/Component

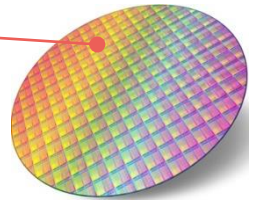


Qorvo RF SiP

LEVEL 0:
Semiconductor Die



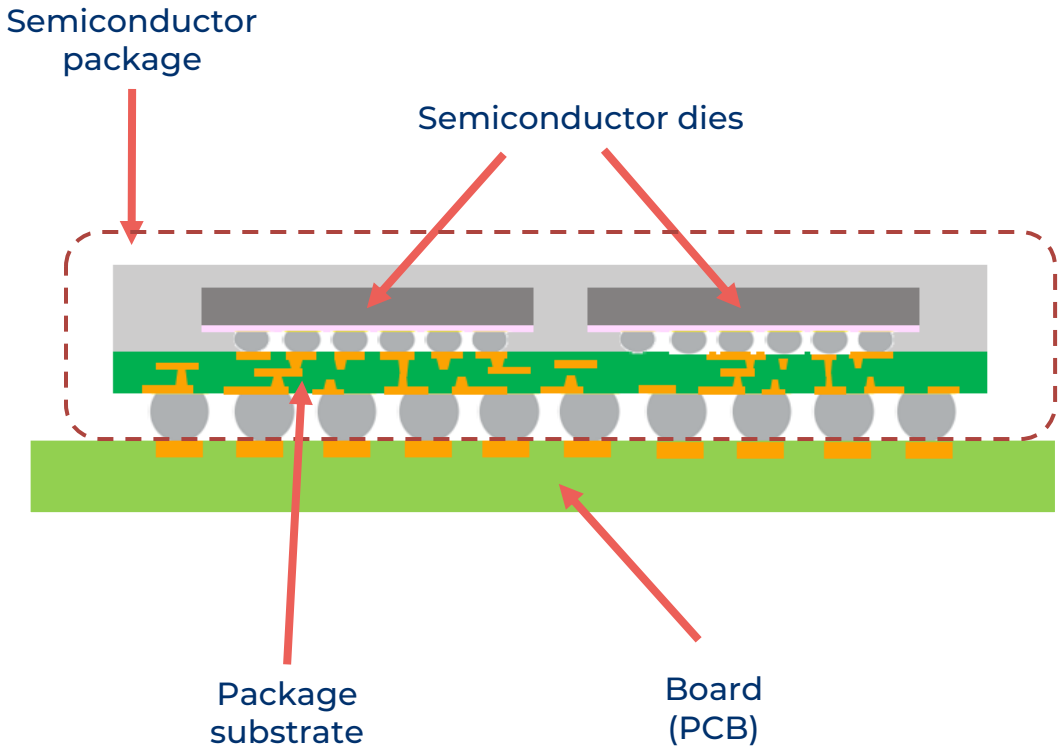
Power amplifier
in Qorvo RF SiP



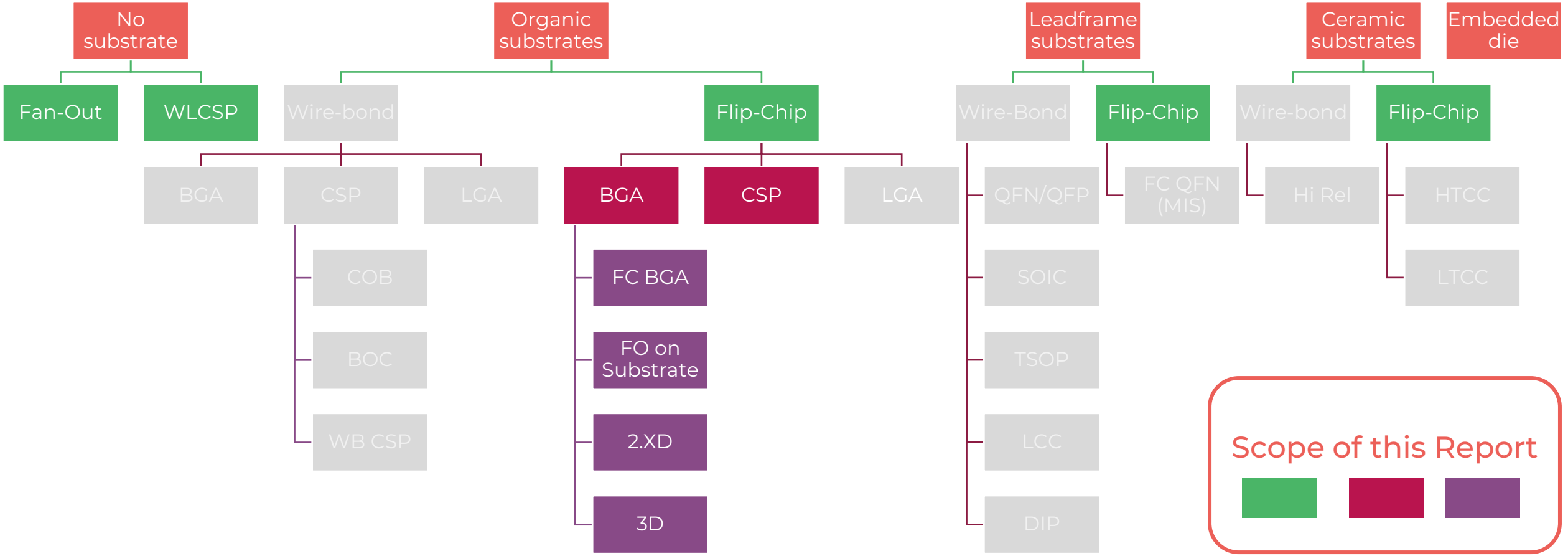
Semiconductor
wafer

Scope of this Report

LEVEL 1+2:
Device/Component + Module/Board

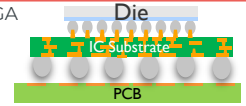
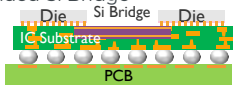
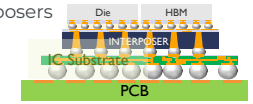
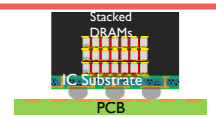
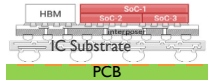
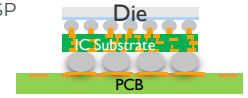
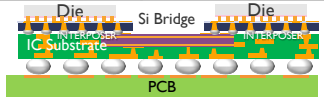
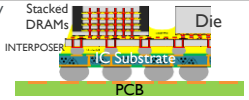
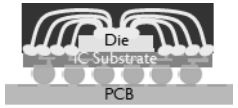
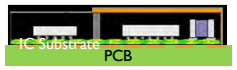
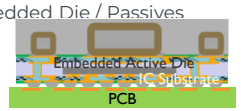
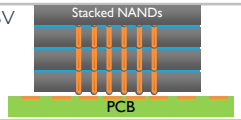
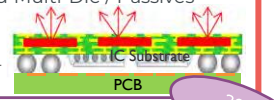
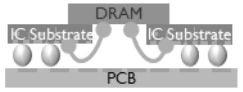
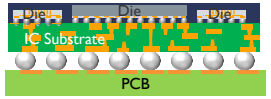
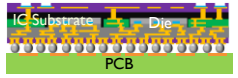
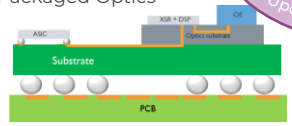
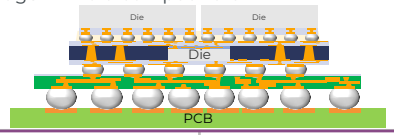
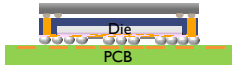
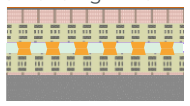
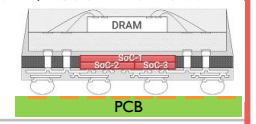
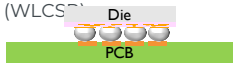
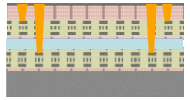
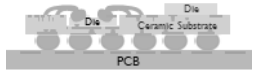
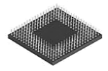
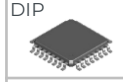


ADVANCED PACKAGING PLATFORMS



- 2.1D with thin-film layers with warpage issue, no HVM, excluded from AP platform
- 2.3D with separate build RDL substrate is LVM, excluded from AP platform

PACKAGING TECHNOLOGY SEGMENTATION BY SUBSTRATE TYPE

ARCHITECTURE	Traditional Packaging	ADVANCED PACKAGING				
SUBSTRATE TYPE	WIRE BOND	FLIP CHIP	EMBEDDED DIE	2.5 D	3D	EMERGING
IC Substrate (Organic)		FC BGA 	Embedded Si Bridge 	Si Interposers 	3DS TSV 	Hybrid Bonding - SoC on interposer  SOURCE: TSMC
		FC CSP 	Embedded Si Bridge + Si Interposers 		HBM TSV 	
	WB CSP WB BGA 	FC SiP Metal Shielding 	Embedded Die / Passives 		NAND TSV 	Embedded Multi-Die / Passives  SOURCE: JCET
	BOC 	Fan-Out on Substrate 	FOPLP 			Co-Packaged Optics  2023 Update
			Embedded Si Bridge in mold compound or RDL  2023 Update			
No Substrate	COB 	Fan-Out PoP 			Cu-Cu Hybrid Bonding – WoW 	Hybrid Bonding - SoC in Fan-Out  SOURCE: TSMC
		Fan-Out 				
		Fan-In (WLCSP) 			TSV, after bonding – WoW 	
Ceramic Substrate	LTCC HTCC 					
					CPGA 	
Lead frame Substrate	DIP  SOT/TSOP  QFN  QFP, LCC etc.	FC QFN 				

SCOPE OF THIS REPORT

METHODOLOGY

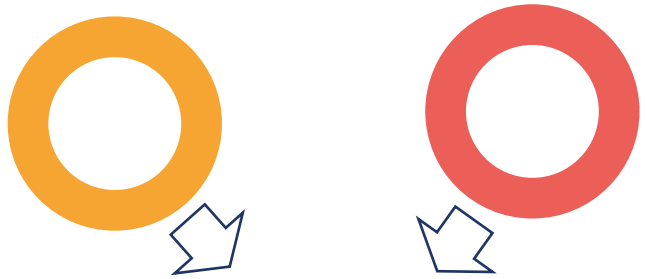
Yole's market forecast model is based on the matching of several sources:

Comparison with existing data

Monitoring of corporate communication

Using other market research data

Yole's analysis (consensus or not)



Comparison with prior Yole reports

Recursive improvement of dataset

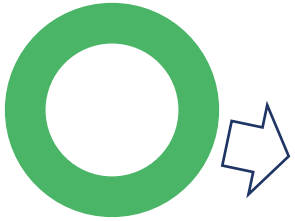
Customer feedback

Preexisting information

Top-down approach

Aggregate of market forecasts

@ System level

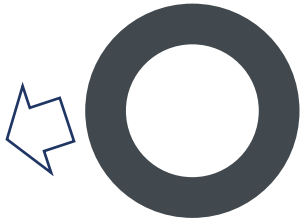


Market

Volume (in Munits)

ASP (in $)

Revenue (in $M)



Bottom-up approach

Ecosystem analysis

Aggregate of all players' revenues

@ System level

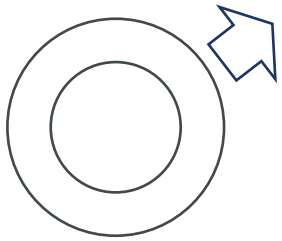
Primary data

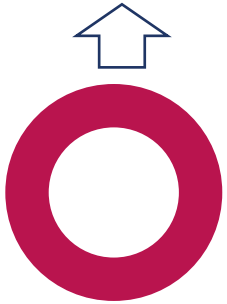
- Reverse costing
- Patent analysis
- Annual reports
- Direct interviews

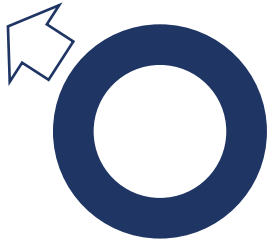
Top-down approach

Aggregate of market forecasts

@ Semiconductor device level







Bottom-up approach

Ecosystem analysis

Aggregate of key players' revenues

@ Semiconductor device level

Secondary data

- Press releases
- Industry organization reports
- Conferences

Semiconductor foundry activity

Capacity investments and equipment needs

Information Aggregation

WHAT'S NEW IN THE STATUS OF ADVANCED PACKAGING 2023?

- Updated the news in the Advanced Packaging market and segmented it into categories.
- Updated Advanced Packaging market data and forecasts (2022-2028):
  - By revenue, wafer, and unit.
  - By Advanced Packaging platforms: flip-chip, fan-out, fan-in, 3D stacked, System-in-Package, and embedded die.
- Analysis of the semiconductor business & supply chain.
- Updated 2022 - 2028 revenue, wafer, and unit forecasts by various application segments: consumer & mobile, automotive & transportation, telecom & infrastructure, medical, industrial, defense & aerospace
- Updated technology trends with new product technologies with a focus on the big players.
- Updated supply chain analysis with a focus on the production relocation from China and an overview of equipment & material suppliers
- Wafer starts market shares of manufacturers from different business models (IDM, OSAT, foundry) by the different Advanced Packaging platforms and their evolution.
- Updated financial analysis of the top 30 OSATs (2018-2022) with key financial metrics : 2022 Revenue, YoY growth, R&D spending, CapEx, Gross margin, and Net Margin.
- Updated M&A data, and different scenarios for OSATs for 2022-2028.

DEFINITIONS

NOTE:

From a logical viewpoint, the following terms are highly interchangeable, and their usage is unfortunately not consistent throughout the industry.

To avoid confusion and enable systematic segmentation, Yole uses the following definitions:

PCB: **Printed Circuit Board,** abbreviation commonly used for system boards – Yole distinguishes between PCB (boards) and semiconductor package substrates (also sometimes referred to as IC substrates).

Substrate: While a substrate can be considered on various system levels (e.g., a transistor Si substrate), the term substrate is used here for semiconductor package substrates (sometimes referred to as IC substrate), which are package components placed between the die and PCB built using semi-additive processing and lamination/build-up technology, namely WB/FC package substrates within FC CSP/BGA or WB CSP/BGA packages.

Thin film RDL: Particular form of **redistribution layer** formed by thin film technology; refers to RDLs of fan-in and fan-out WLP/PLP.

Interposer: Technically, any kind of substrate/RDL has the function of “interposing” between the die and PCB; however, for practical purposes, the term interposer is used for additional interconnect components on top of a substrate, in particular Si, glass or organic interposers.

WHAT WE GOT RIGHT, WHAT WE GOT WRONG

What we got right

- Semiconductor growth drivers moving from mobile to AI, HPC, Automotive & IoT.
- Changes to the semiconductor manufacturing supply chain dynamics and their impact.
- TSMC's strong emergence in AP business.
- Predicted M&As in the OSAT sector involving various scenarios.
- Predicted the impact of Trade War evolution and reshoring projects out of China to the rest of the world.

What we got wrong

- Substrate ASP has been increased in this year's forecast to reflect the impact of material shortages, affecting flip-chip, 2.5D/3D, and UHD FO platform ASPs and estimated revenues.
- 2.5D/3D ASP has been updated, and the number of stacked dies was reviewed.
- Units of CIS WSPY using W2W from Sony are lower than forecast last year, it impacts the overall 2.5D & 3D forecast.
- Update of dies' number per package for some 3D stack memory
- Update of die and package dimensions.
- Update of the Advanced Packaging Revenues forecast.

THREE-PAGE SUMMARY

ADVANCED PACKAGING MARKET TRENDS

Despite Industry Slowdown, Advanced Packaging Market Continues to Thrive in 2023

The semiconductor industry is expected to experience **a negative YoY growth of 6% in 2023**, generating a revenue of $555B due to the rising prices of materials and devices as the global economy weakens, and the demand for PCs and smartphones decreases. Despite this, it is expected to grow again by the end of 2023, and throughout 2024, the semiconductor market is still anticipated to show positive YoY growth.

Governments worldwide recognize the semiconductor industry as a strategic business and a matter of sovereignty. Several countries have announced plans to strengthen domestic supply chains. More than $800B has been reported in supporting the industry's domestic development, including proposals for Chip Acts in the US, EU, and South Korea.

Material costs for semiconductors are increasing, with TSMC announcing a price increase of up to 20% to customers. This may lead to a snowball effect on other IDMs, foundries, and OSATs, causing adjustments to their production costs.

The Advanced Packaging (AP) market, which was worth **$44.3B** in 2022, is expected to grow at a **CAGR $_{2022-2028}$ of 10.6%** to reach **$78B in 2028**. The traditional packaging market is expected to grow, but at a slower rate of 4.15% CAGR $_{2022-2028}$, with the total packaging market forecasted to grow at a CAGR $_{2022-2028}$ of 7.10% to $64.7B and $143.3B, respectively.

The AP market accounted for ~ **47% of the total packaging market in 2022**, and its share is continuously increasing due to megatrends. The Flip-Chip platform, which includes FCBGA and FCCSP, represented 51% of the AP market share in 2022. The highest revenue CAGR$_{2022-2028}$ is expected from ED, 2.5D/3D, and flip-chip at 30%, 19%, and 8.5%, respectively.

Mobile & Consumer constituted **70%** of **the total AP market in 2022**, with an expected growth rate of **7% CAGR$_{2022-2028}$**, constituting **61% of the AP revenue by 2028**. **Telecom & infrastructure** is **the fastest-growing segment**, with a revenue growth rate of around **17%,** and will account for **27%** of the AP market in **2028**. **Automotive & Transportation** will account for **9%**, whereas **other segments**, including medical, industrial, and aerospace/defense, will account for **3%** of the market.

Traditional packaging still dominates the market in terms of wafer production, with almost **73%** of **the total wafer production in 2022**. However, the **AP market** is continuously increasing its share of wafers, with its market share expected to increase from **~27% in 2022 to 32% in 2028**. In terms of unit count, traditional packaging accounts for more than 94% share, but AP shipments will increase at **~6% CAGR$_{2022-2028}$ to reach 101B units in 2028**.

ADVANCED PACKAGING TECHNOLOGY TRENDS

Innovating Beyond Moore's Law: Chiplets and Hybrid Bonding Open New Frontiers

While technology node scaling was once the main driver of semiconductor innovation, new markets and applications are emerging with an emphasis on device functionality. **Advanced Packaging has become crucial** for innovation in this field, as it increases the value of semiconductor products **by adding functionality and improving performance while also lowering cost**. As a result, **major semiconductor companies** like TSMC, Intel, and Samsung **are increasingly turning to chiplet and heterogeneous integration strategies, using AP technology to complement front-end scaling efforts.**

One key trend driving Advanced Packaging is the adoption of a chiplet approach to attain heterogeneous integration. This approach partitions an SoC chip into multiple dies with different IP blocks, scaling only those that require advanced technology nodes and later integrating all chiplets using 2.5D or 3D packaging technology. This strategy improves overall yield and reduces cost**. Another popular trend** and a high-potential enabling technology in interconnect technology is **Hybrid Bonding** (HB), which allows for metal-metal and oxide-oxide face-to-face stacking with <10 µm bump pitch. Wafer-to-wafer hybrid bonding technology is already used for CIS and 3D NAND stacking, while various players are also working on 3D SoC using wafer-to-wafer or die-to-wafer hybrid bonding for e.g., for memory-on-logic stacked 3D IC for PC, HPC and data center applications.

TSMC is currently **the leader in high-end Advanced Packaging** (out of memory market), since it started CoWoS production in 2012. Since then, it has introduced various products to its high-end packaging portfolio, with new offerings such as 3D SoIC, InFO_SoW, and other high-density fan-out variants from the InFO line, and new CoWoS variants. In 2022, **Intel was the number one in terms of investments in Advanced Packaging**, and due to its new IDM 2.0 strategy, the company will continue consolidating its packaging solutions, such as EMIB, Foveros, and Co-EMIB, and improving them**.** With Intel's core business not going so well in 2023 mainly due to macroeconomic factors, we expect TSMC to surpass Intel in terms of investments in advanced packaging during the year. **Samsung** is one of the top memory providers, and it offers **Advanced Packaging solutions for its HBM and 3DS products**, as well as fan-out panel level packaging and silicon interposers, allowing the company to commercialize high-end performance products such as I-Cube, H-Cube, and X-Cube.

It is important to note that Advanced Packaging involves different equipment, materials and processes compared to traditional packaging, such as new substrate materials, lithography processes, laser drilling, CMP, and KGD tests. AP players are investing vast amounts into developing and introducing these new materials and processes. Overall, heterogeneous integration using Advanced Packaging technologies is driving semiconductor innovation and enabling the improvement of overall system performance while lowering cost.

ADVANCED PACKAGING SUPPLY CHAIN DYNAMICS

The Semiconductor Supply Chain: The New Geopolitical Battleground

The semiconductor value chain, including Advanced Packaging, has gained increased attention since 2020 due to a chip shortage, security of supply, competitiveness, and strategic dependencies. **Governments worldwide** are seeking to exert more control over this crucial value chain to better understand its complexity and **assess the competitiveness of their domestic ecosystems**. To address this, governments are investing through local **"Chip Acts"** in their own capacity to understand the semiconductor value chain, identify interdependencies and chokepoints, and deploy **policy tools to strengthen domestic semiconductor ecosystems**. The conflict between the US-China for technology dominance is causing disruptions in the industry's supply chains. As a result, semiconductor companies are struggling to get adequate chip and equipment suppliers, and this could potentially constrain growth within the industry.

Additionally, the AP supply chain is also impacted, as AP is seen as the key strategy for the after-Moore's law era. **The AP market is expected to grow to $78B by 2028.** However, the geopolitical aspects at the heart of escalating trade tensions between the US and China are stressing the industry's supply chain. At the same time, it led to governmental support plans of $52B in the US and $143B in China, next to tax credits. In addition to the rising labor costs, this led to a **new value chain extending from China** to Vietnam with Samsung establishing two major plants in the region. **Vietnam, Thailand, India, and Malaysia are eyeing opportunities for production relocation from China**. The relocation from China is a positive move for **supply chain diversification** and minimizing any possible shortages. However, it also poses a **risk in terms of the ability to replace China's production capacity.**

Seven players, including 3 IDMs (Intel, Samsung, Sony), a foundry (TSMC), and the top 3 global OSATs (ASE, Amkor, JCET) process over **80% of Advanced Packaging wafers**. OSATs accounted for 65.1% of the AP wafers in 2022. Foundry is taking AP business from OSATs with 12.3% and IDM with 22.6%.

OSATs are expanding their testing expertise, while traditional pure test players are investing in packaging & assembly capabilities. Top OSATs are investing in IC testing capacity to capture the test market, and pure test houses, such as KYEC and Sigurd Microelectronics, are adding packaging/assembly capabilities in their service offering through M&As or investing in R&D.

Overall, **there is a paradigm shift in the packaging / assembly business** – traditionally the domain of OSATs and IDMs. Players from different business models, viz. Foundries, Substrate/PCB suppliers, and EMS/ODMs are entering packaging and assembly, cannibalizing the OSAT business.

Substrates have been in tight supply since the post-pandemic era, due to strong demand for high-end CPUs, GPUs, and 5G networking chips by major chipmakers. The high inflation and geopolitical tensions continued to negatively impact materials supply and in 2021-2022, and ABF substrates delivery lead time has been extended to nearly three quarters and prices have risen ~15 to 25%. In 2023, the decreasing demand on mobile and consumer and the slow-down of the sever market growth reduced the pressure on the IC substrate market and helped to ease the shortage as many companies have cut/stopped the orders. The investment in capacity expansion by substrate suppliers and the entry of new players on high-end substrate manufacturing, such as SEMCO and LG Innotek, may also help ease the shortage to some extent.

Substrate suppliers are investing significant CapEx for needed capacity expansion as they try to secure their supply for customers with whom they already hold long-term agreements. Nevertheless, it will take some time before this capacity comes online, and therefore, the supply constraints have continued throughout 2022 and could last for another 2 years until the supply chain is balanced.

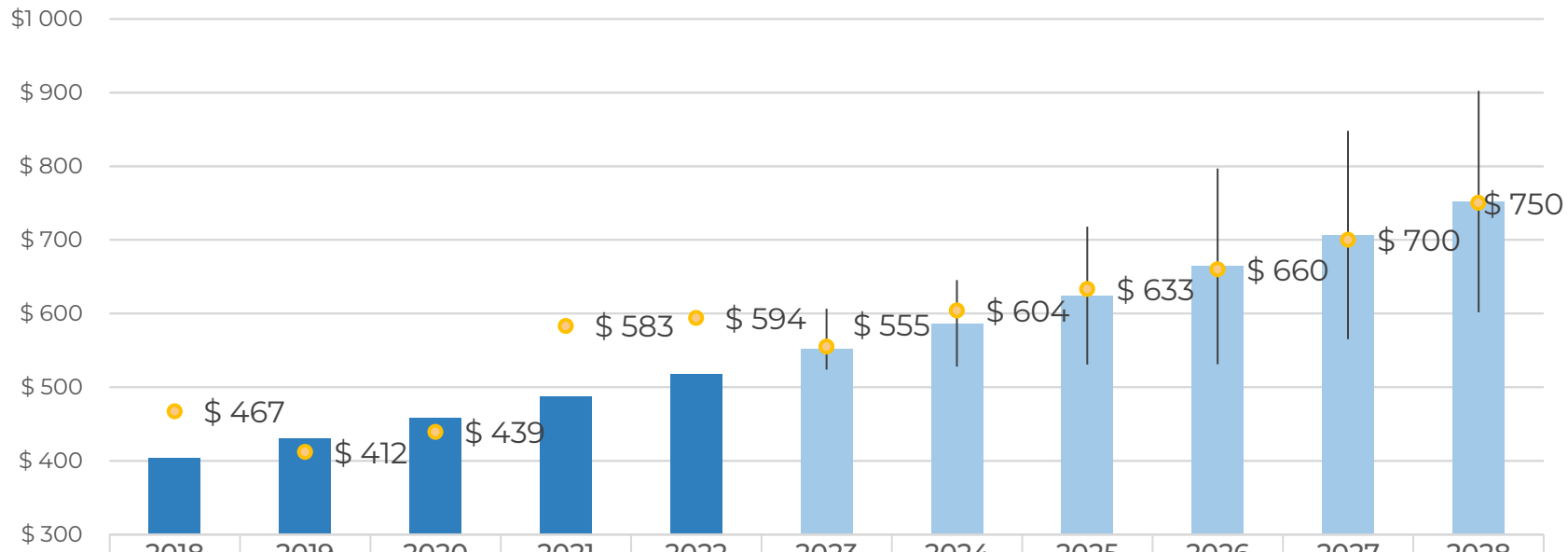
EXECUTIVE SUMMARY

SEMICONDUCTOR INDUSTRY OUTLOOK

The semiconductor market reached $594B in 2022, despite signs of economic decline in the world economy. However, the market is expected to re-adjust with an estimated YoY growth rate of -6% to reach $555B by 2023. This decline is due to a combination of factors, including decreasing buying power and consumer sentiment affecting demand, as well as the global economic crisis in 2023. This crisis has led to fab overcapacity and decreasing average selling prices (ASPs), causing a drop in revenues for semiconductor companies. While the semiconductor market has shown resilience in the past, it will face challenges in the coming years as it adjusts to changing economic conditions.

Following its jump of 32 % from 2020 to 2021, the semiconductor market grew to $594B in 2022, recording a stabilizing growth of 1.9 %.

Semiconductor Market revenues $B - 2018/2028 - Confirmed and expected - as of 02/2023



	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
Baseline value	$ 405	$ 430	$ 458	$ 487	$ 518	$ 552	$ 587	$ 624	$ 664	$ 707	$ 752
High						$ 607	$ 645	$ 718	$ 797	$ 848	$ 902
Low						$ 524	$ 528	$ 531	$ 531	$ 565	$ 602
Confirmed/Expected Revenues	$ 467	$ 412	$ 439	$ 583	$ 594	$ 555	$ 604	$ 633	$ 660	$ 700	$ 750

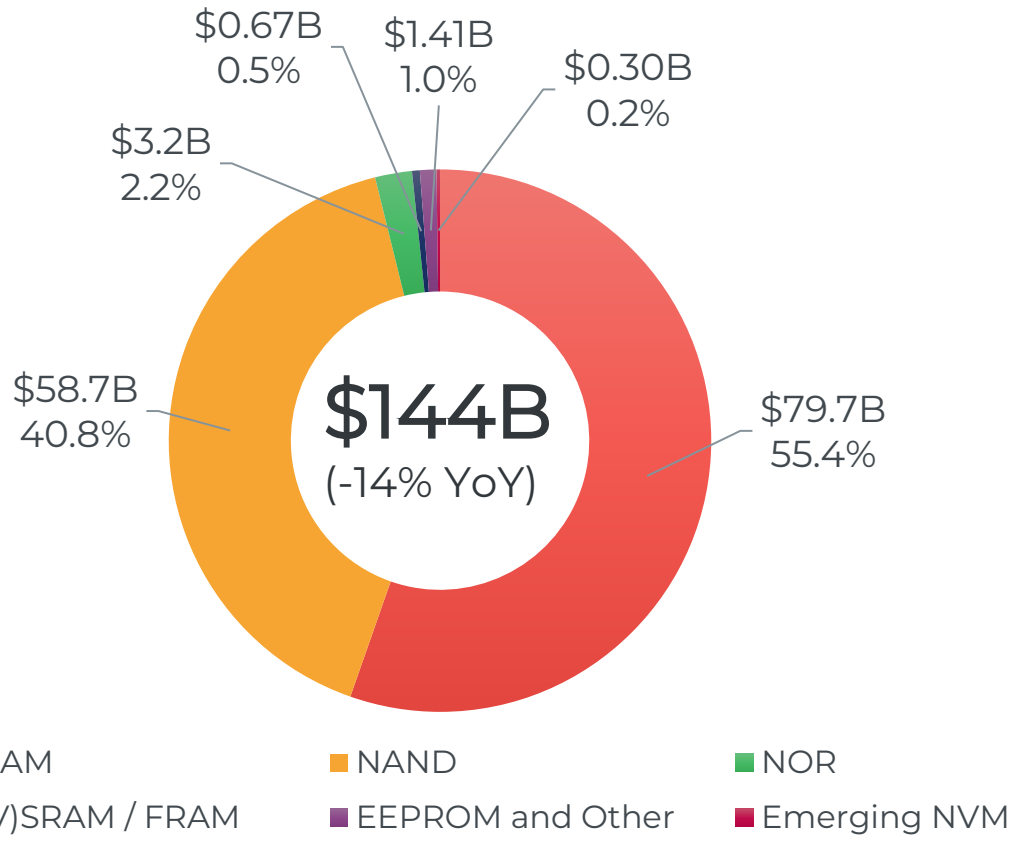
Data source: WSTS, Yole estimation

STAND-ALONE MEMORY MARKET – OVERVIEW

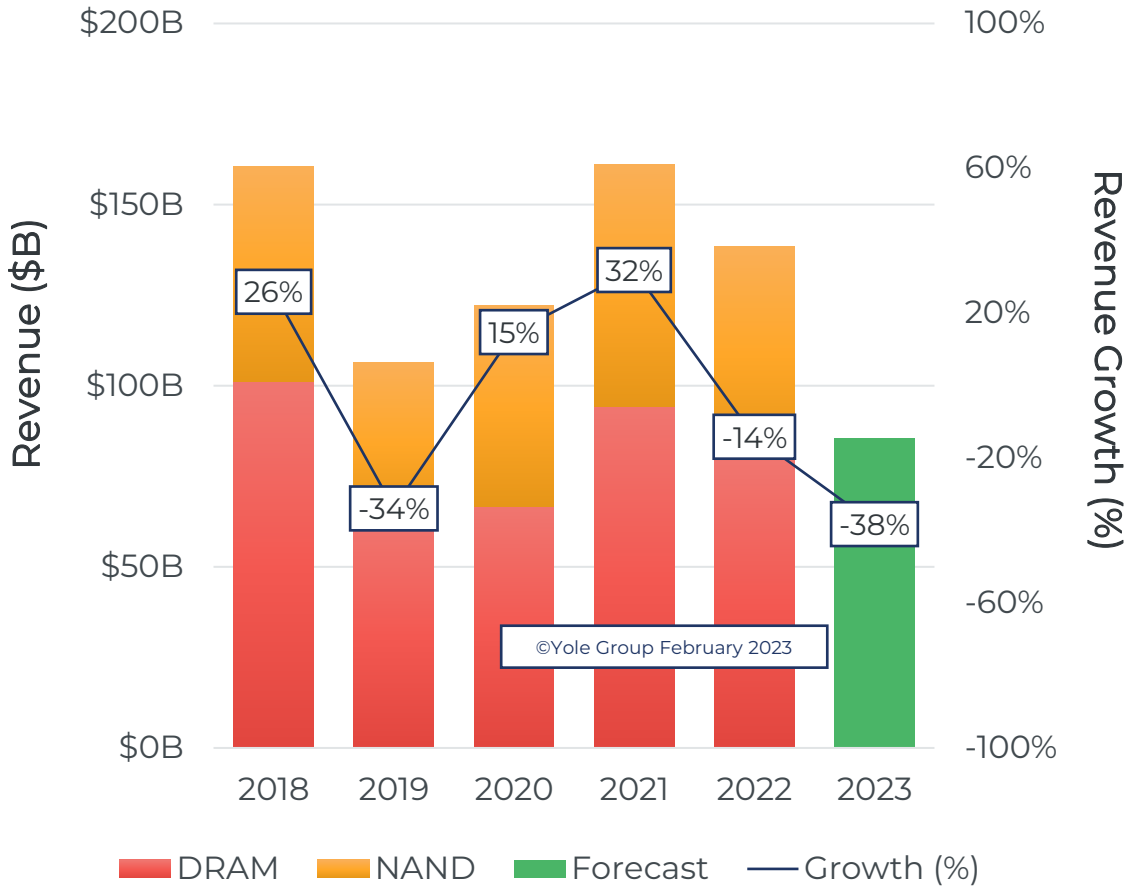
NAND and DRAM account for ≈96% of the overall stand-alone memory market.*

Combined NAND and DRAM revenue is estimated to be ≈ $144B in 2022, down 14% from 2021.

2022 memory market - breakdown by technology



NAND and DRAM market evolution



__Note__: Stand-alone memory revenue includes chips and wafers, as well as memory modules and solid-state drives sold by memory IDMs.
Source: NAND and SRAM Market Monitors – Q1 2023

NEW TRENDS & DRIVERS: OPPORTUNITY FOR SEMICONDUCTOR PACKAGING

Require back-end and assembly innovations: panel-level packaging, high-accuracy bonders, TCB, D2W/W2W bonding, and photonics integration in packages. As for materials, there is a need to develop new dielectric materials, mold compounds, underfill, solder interconnects, and TIMs to meet the stringent performance and reliability requirements demanded by next-generation hardware.

System requirements

- computing power
- speed
- bandwidth
- functionality

- Lower latency
- Lower power
- Lower cost

- System integration
- More sensors
- More memory
- Hardware-software compatibility

Opportunities for different devices

Megatrends create business for variety of ICs from high end xPUs to low end discretes

- CPUs, GPUs, SoCs, APUs, FPGAs
- ASICS, DSPs, MCUs
- MEMS/Sensors
- Power ICs/discretes
- Memory
- Optoelectronics

Opportunity for packaging

Create business opportunities for both advanced and traditional packaging platforms

Advanced packaging (WLPs, flip-chip, TSV) business opportunity supported by AI/ML, Mobile, AR/VR, 5G, smart automotive

Traditional packaging (wire-bond lead-frame based) business opportunity created by IoTs, Industry 4.0, and smart automotive

Mega trends like mobile, automotive, IoT, and industry 4.0, require a variety of MEMS sensors that create opportunities for both traditional & Advanced Packaging

Opportunity for fab/front-end

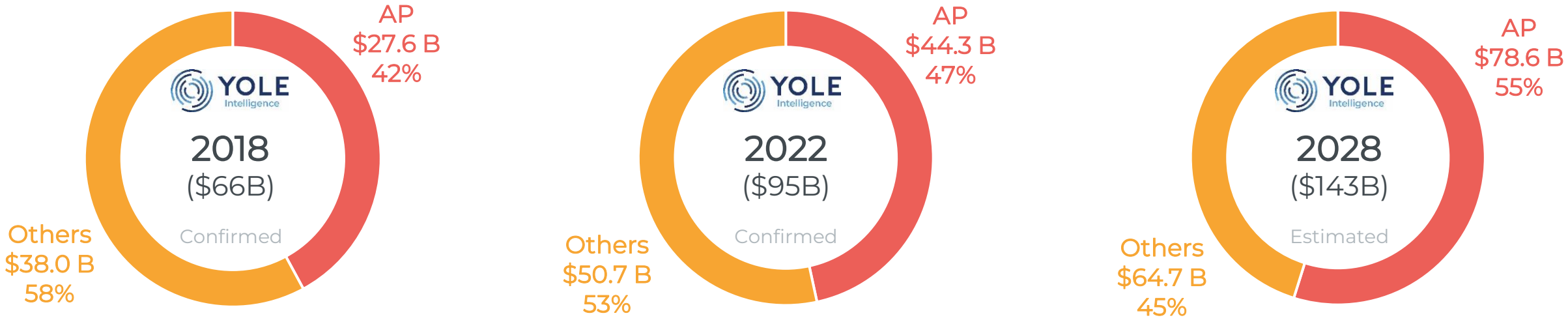
Front-end scaling slows but continues: Moore's Law keeps going but at a slower pace => high-end fab business continues growing (5nm & below)

More & more heterogeneous integration to support functionality, faster time to market, and low cost: More than Moore's => Resurgence of legacy fabs => Increasing business

8" wafer fabs and related tools demand to remain strong

ADVANCED VS TRADITIONAL TECHNOLOGIES OVERVIEW 2018 to 2028

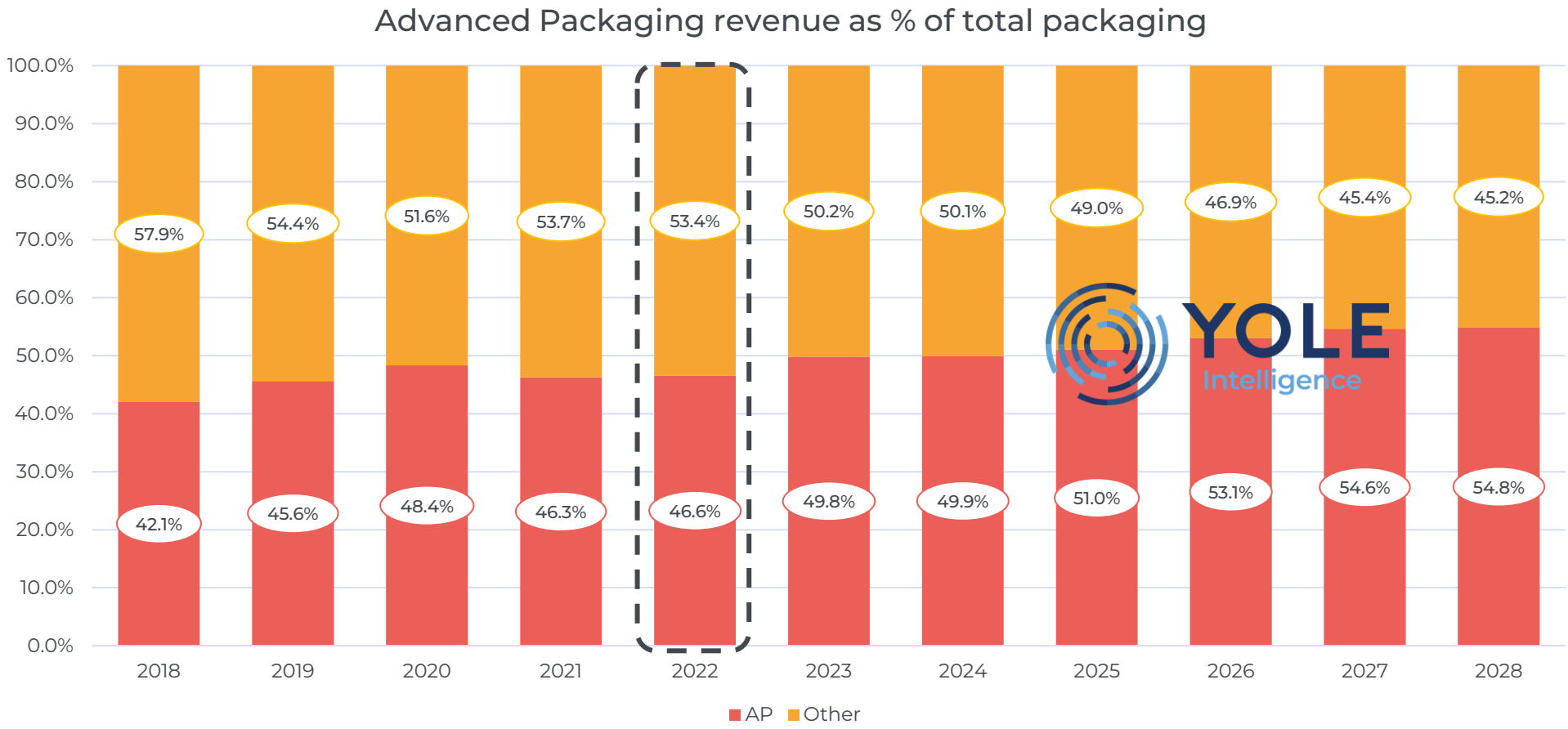
Revenue Split ($B)



- Advanced Packaging revenue is growing at a fast pace, and it is catching up with traditional packaging.
- In 2022, the revenue generated by Advanced Packaging was 47% of the total packaging market. By 2028, Advanced Packaging's revenue will increase to approximately 58% of the total packaging market. This indicates a significant growth in the market share of Advanced Packaging over the next few years.

ADVANCED VS TRADITIONAL PACKAGING MARKET SHARE EVOLUTION 2018-2028

Advanced Packaging revenue will exceed traditional packaging revenue by 2025.

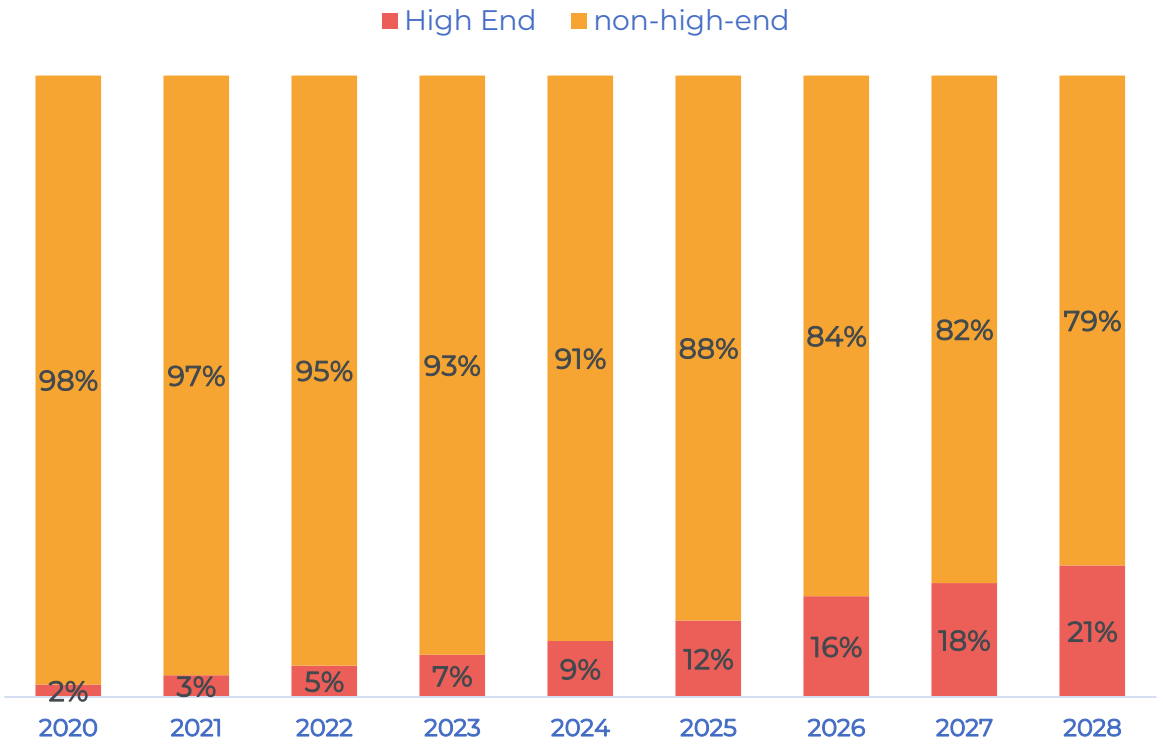


In 2022, the AP market share was ~47%. Due to strong momentum in the AP market driven by megatrends, the percentage of AP in the total semiconductor market is increasing continuously and will reach more than ~51% of the market by 2025.

ADVANCED PACKAGING VALUE MOVING TOWARDS HIGH-END TECHNOLOGIES

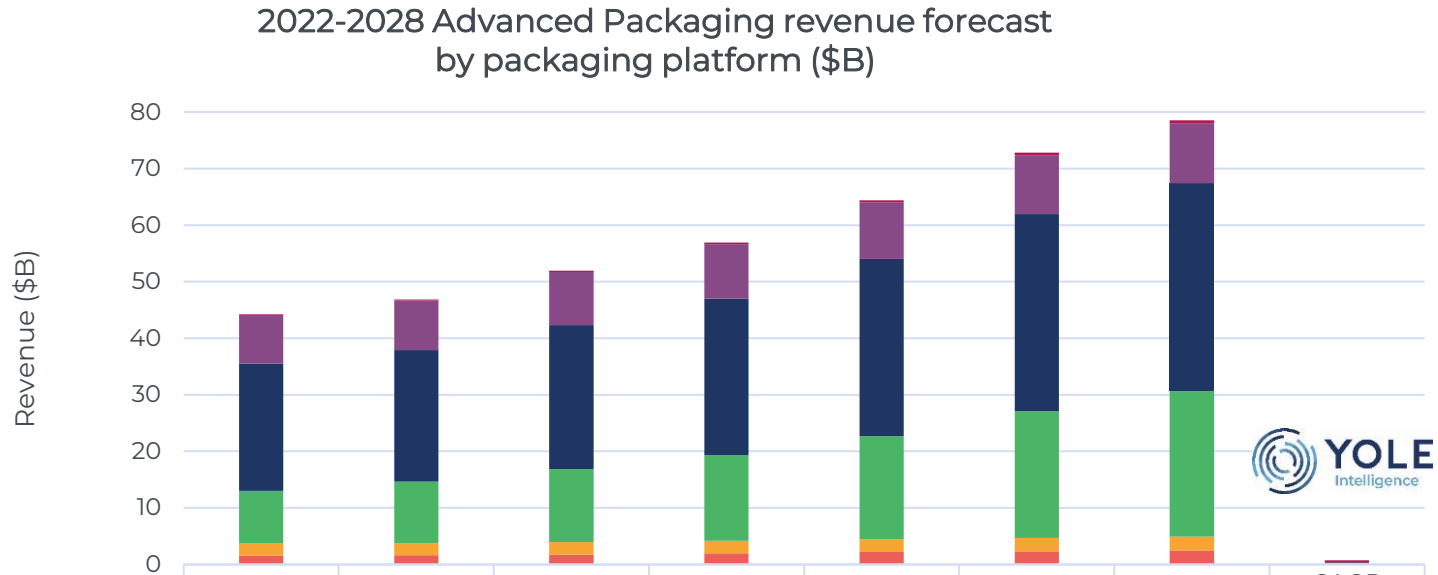
- Although Moore's Law has remained relevant for over five decades, it is no longer cost-efficient for advanced nodes and lesser leading-edge manufacturers can keep up.
- The industry is now diligently utilizing advanced packaging technologies to put multiple advanced and/or matured chips in a single package, also known as heterogeneous integration.
- Coupled with High-end Performance Packaging, the system-level 3D interconnect density (3D ID) trend is not only sustained but accelerates to new highs. This is driven by high-end market segments such as AI, datacenter, supercomputers, data mining, networking, autonomous driving, Co-Package Optics and high-end PC and gaming.
- Hereafter, the need for more performance for this market segments is triggering a value transfer towards high-end packaging technologies within the whole advanced packaging market.
- In 2022, high-end performance packaging represented 5% of the total AP market value. **By 2028, high-end packaging is estimated to reach 21% of the total AP market value.**
- The value transfer is due to technology transference – growing adoption of high-end 2.5D/3D packaging technologies – and to the fact that these technologies allow increased performance, and hence come at a higher cost, contributing to higher revenues.
- Foundries and IDMs – the ones leveraging front-end capabilities – are the ones that are profiting the most from the value transfer. So far on the OSAT ecosystem, only the top ones like ASE, Amkor and JCET, have the capabilities to partner up with foundries and IDMs and actively participate in the high-end packaging supply chain.

High-end vs. Non High-end Packaging revenues ratio evolution (2020 – 2028)



High-end Performance Packaging is defined by Yole as a forefront packaging technology that adds value to device performance with ***high IO density (≥16/mm²) and fine IO pitch (≤130µm).***
This includes technologies generally defined as 2.5D/3D integration such as UHD FO, Embedded Si bridge, Si Interposer, 3D stacked memories and 3D SoC.

ADVANCED PACKAGING REVENUE FORECAST 2023-2028



	2022	2023	2024	2025	2026	2027	2028	CAGR (2022-2028)
ED	0.10	0.15	0.22	0.28	0.36	0.48	0.51	30.40%
SiP	8.63	8.77	9.38	9.62	9.98	10.38	10.66	3.59%
Flip-Chip	22.53	23.28	25.49	27.70	31.35	34.90	36.72	8.48%
2.5D/3D	9.20	10.87	12.90	15.14	18.25	22.38	25.77	18.72%
WLCSP	2.21	2.11	2.16	2.24	2.29	2.38	2.42	1.58%
FO	1.59	1.63	1.77	1.95	2.16	2.33	2.47	7.65%
TOTAL	44.26	46.83	51.92	56.92	64.40	72.84	78.55	10.03%
YoY Growth	10%	6%	11%	10%	13%	13%	8%	

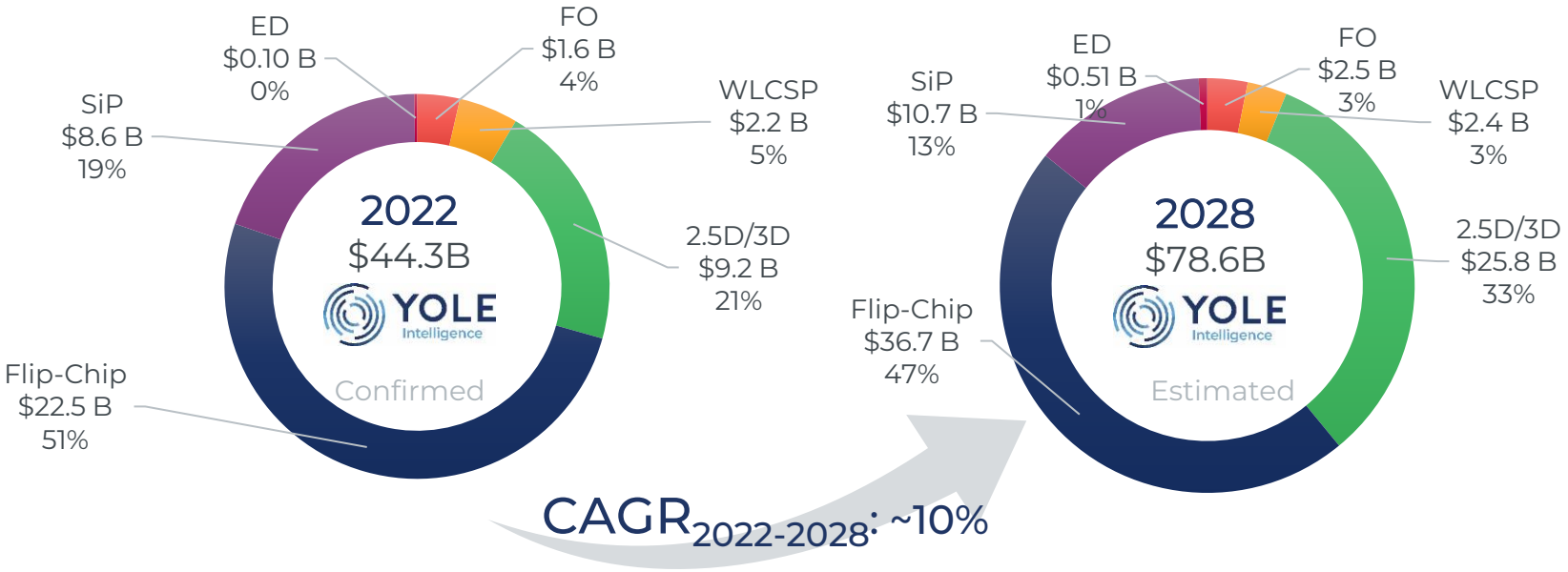
- The Advanced Packaging market was worth ~$44.3B in 2022. It is expected to grow at a ~ 10% $CAGR_{2022-2028}$ to reach ~$78.6B in 2028.
- The market increased by 10% realizing a strong growth in 2022, still driven by the aggressive post-pandemic semiconductor demand.
- We expect the post-2022 global semiconductor demand will normalize in 2023 with a slight decline. The world political conflicts, the geopolitical tensions, and increased inflation scenarios faced in 2022 and early 2023 will have a negative influence on the semiconductor market in 2023.
- Although the packaging market is expected to be affected by the overall semiconductor market decline, the demand for Advanced Packaging will continue to increase as its importance and complexity keep increasing for the advanced device nodes and complex form factors. Nevertheless, AP market growth will be softer in 2023 compared to the previous year.

Data source: Advanced Packaging Monitor – Q1 2023

* Flip-Chip includes: FCCSP and FCBGA. It includes bumping, assembly and materials revenues.

ADVANCED PACKAGING REVENUE FORECAST 2023-2028

BREAKDOWN BY TECHNOLOGY



Flip-chip	$CAGR_{2022-2028}$ ~ 8.5%
SiP	$CAGR_{2022-2028}$ ~ 3.6%
Fan-out	$CAGR_{2022-2028}$ ~ 7.6%
Fan-in WLP	$CAGR_{2022-2028}$ ~ 1.6%
2.5D/3D	$CAGR_{2022-2028}$ ~ 18.7%
Embedded Die	$CAGR_{2022-2028}$ ~ 30.4%

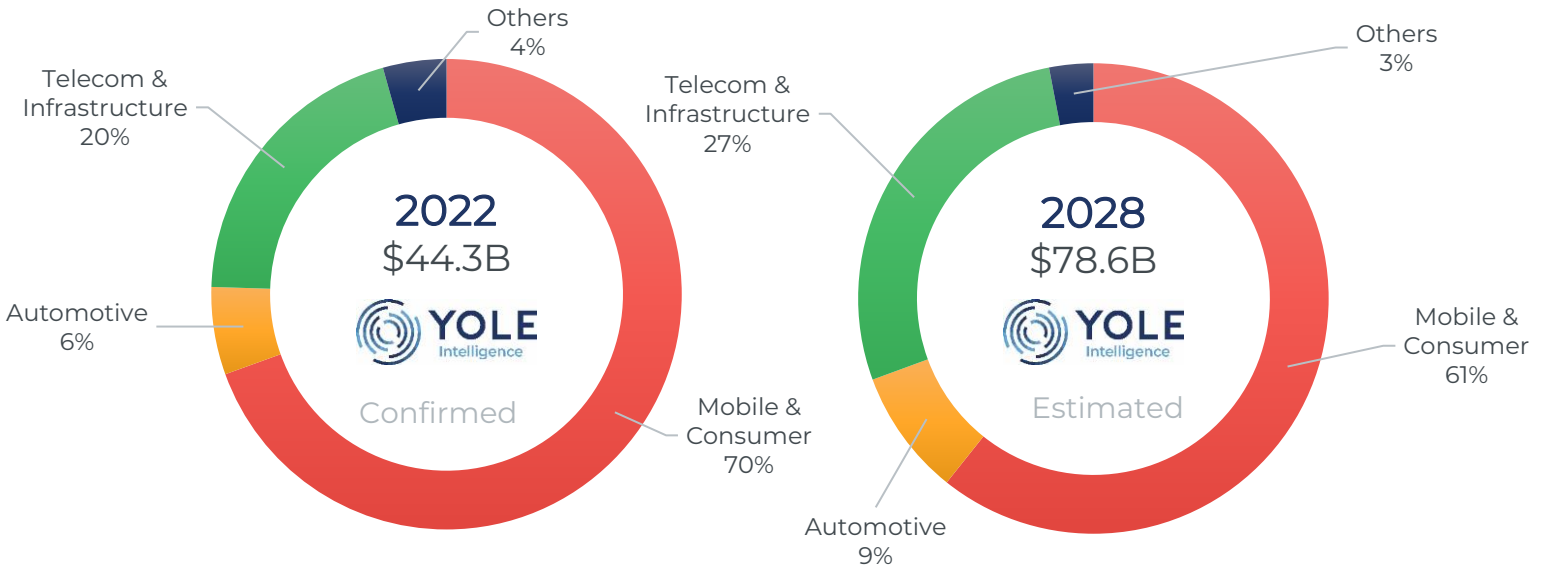
* Flip-Chip includes: FCCSP and FCBGA. It includes bumping, assembly and materials revenues.

- The Flip-Chip platform (includes FCBGA and FCCSP) has the highest market share, with 51% of the market in 2022.
- Highest growth $CAGR_{2022-2028}$ is expected from ED (in laminate substrate), 2.5D/3D, and flip-chip at 30%, 18.7%, and 9%, respectively, as high-volume products further penetrate the market:
  - FO in mobile, networking, HPC, and automotive.
  - 2.5D/3D in AI/ML, HPC, data centers, CIS, 3D NAND, MEMS/sensors.
  - ED in automotive, mobile, and medical end markets.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING REVENUE FORECAST 2023-2028

BREAKDOWN BY MARKET



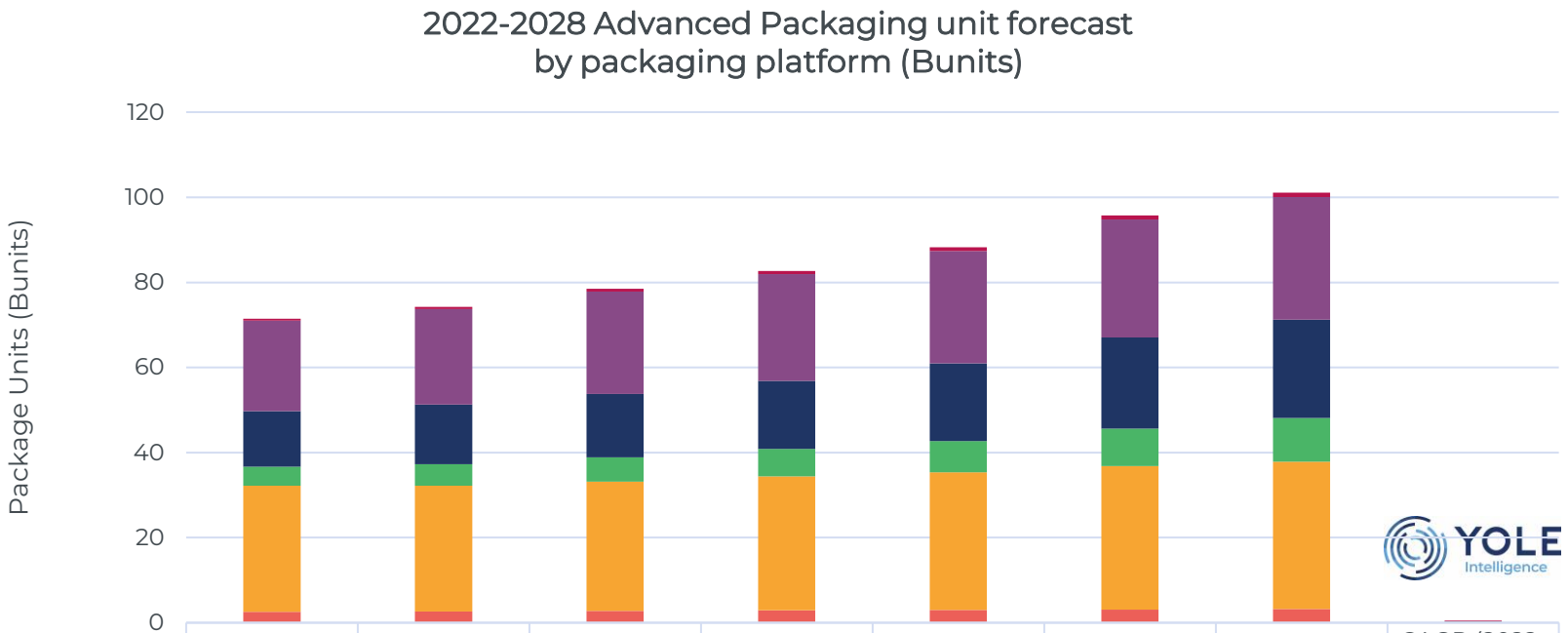
Mobile & Consumer	$CAGR_{2022\text{-}2028}$ ~ 7%
Automotive & Transportation	$CAGR_{2022\text{-}2028}$ ~ 10%
Telecom & Infrastructure	$CAGR_{2022\text{-}2028}$ ~ 17%
Others*	$CAGR_{2022\text{-}2028}$ ~ 10%

* Others include medical, industrial, & aerospace/defense segments

- The Mobile & Consumer segment constituted 70% of the total Advanced Packaging market by revenue in 2022. It will grow with an 8% CAGR and constitute 61% of the Advanced Packaging revenue by 2028. This market will be driven by increased silicon content in mobile and consumer devices and the need for more complex packaging technology due to 5G growth and more stringent system performance requirements.
- Telecom & Infrastructure is the fastest-growing segment (CAGR ~17%) in the Advanced Packaging market by revenue and will account for 27% of the market in 2028. This is driven by 5G deployment and the thriving of HPC/AI applications, with more demanding requirements at the system and package level.
- Automotive & transportation will account for 9%, and its growth will be driven by vehicle electrification, and hence the increased silicon content inside vehicles and the need for more advanced packaging solutions in ADAS, radar, infotainment and overall automotive computing systems.
- Other segments, including medical, industrial, and aerospace/defense, will account for 3% of the market.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING UNIT FORECAST 2023-2028



	2022	2023	2024	2025	2026	2027	2028	CAGR (2022-2028)
ED	0.4	0.5	0.7	0.8	0.9	1.0	1.1	16.41%
SiP	21.2	22.5	24.1	25.1	26.4	27.7	28.8	5.24%
*Flip-Chip	13.1	14.0	14.9	16.0	18.3	21.4	23.1	9.95%
2.5D/3D	4.5	5.1	5.7	6.4	7.3	8.8	10.3	14.76%
WLCSP	29.6	29.6	30.4	31.5	32.4	33.7	34.6	2.62%
FO	2.5	2.6	2.8	2.9	3.0	3.1	3.2	3.89%
TOTAL	71.4	74.3	78.5	82.7	88.2	95.8	101.1	5.97%
YoY Growth	0.3%	4%	6%	5%	7%	9%	6%	

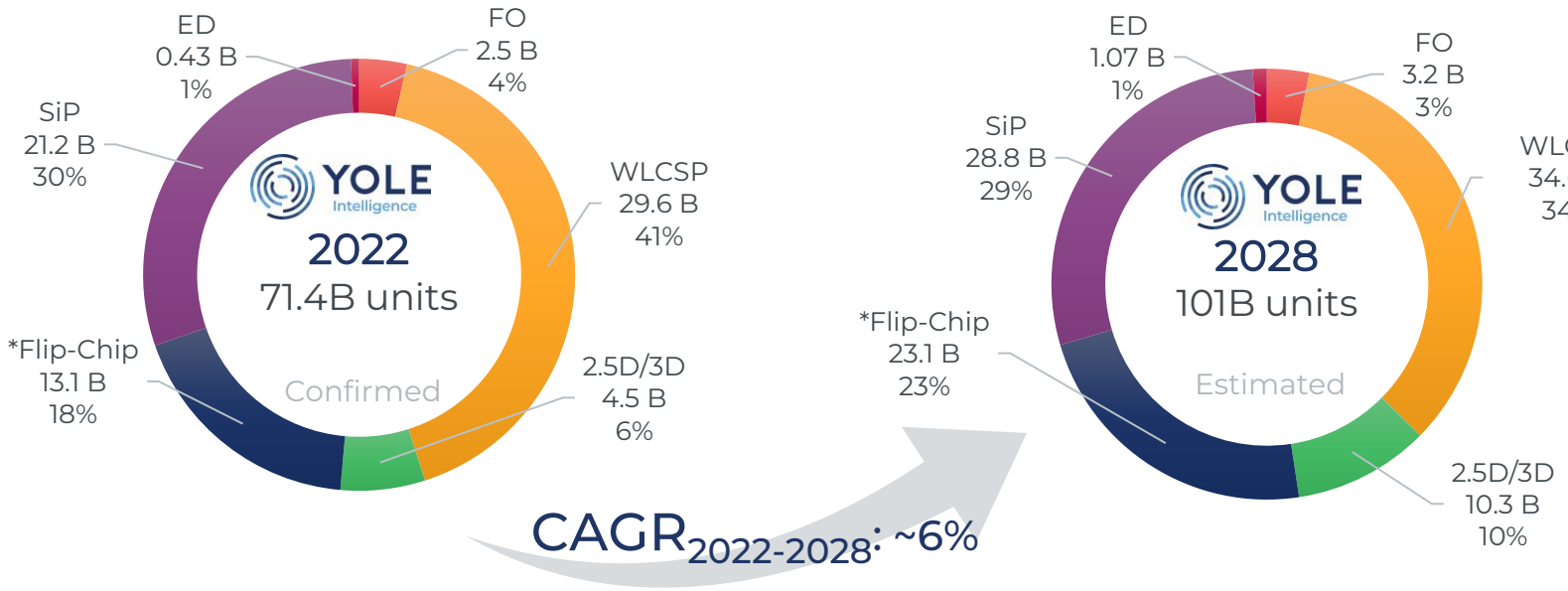
* Flip-Chip includes: FCCSP and FCBGA.

Data source: Advanced Packaging Monitor – Q1 2023

- Advanced Packaging shipments will increase at a ~6% $CAGR_{2022-2028}$ to reach 101.1B units in 2028.
- Concerning unit count, WLCSP packages will remain dominant.
- 2.5D/3D packages will grow at a ~ 15% CAGR to reach ~ 10.3B in 2028. Growth in units is driven by 3D memory, Si interposer, 3D NAND, SoC, and CIS.
- ED package share is ~1% of the total AP shipments. However, it will grow at 16.4% $CAGR_{2022-2028}$ to reach ~ 1.07B by 2028. This growth will be led by increased adoption in mobile (e.g., envelope tracker), automotive & base stations.
- Fan-out package units will grow with a 3.9% CAGR from 2022 to 2028 to 3.2B units in 2028.
- Flip-chip packages (FCBGA and FCCSP) will grow at a CAGR of ~ 10% to reach ~23.1B units in 2028.

ADVANCED PACKAGING UNIT FORECAST 2023-2028

BREAKDOWN BY TECHNOLOGY



Flip-chip	$CAGR_{2022-2028}$ ~ 10%
SiP	$CAGR_{2022-2028}$ ~ 5.2%
Fan-out	$CAGR_{2022-2028}$ ~ 3.9%
Fan-in WLP	$CAGR_{2022-2028}$ ~ 2.6%
2.5D/3D	$CAGR_{2022-2028}$ ~ 14.8%
Embedded Die	$CAGR_{2022-2028}$ ~ 16.4%

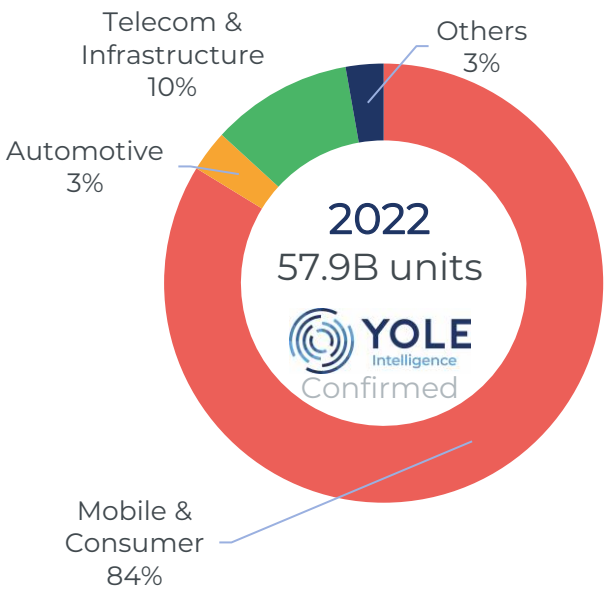
* Flip-Chip includes: FCCSP and FCBGA

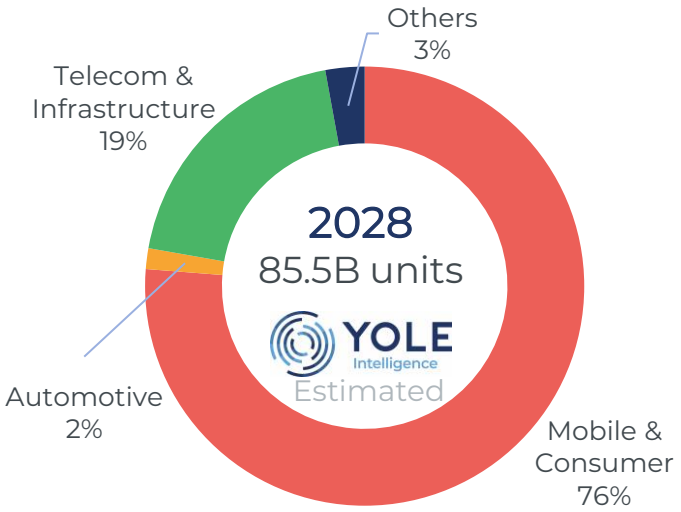
- The number of fan-in WLP packages will increase by ~ 2.6% CAGR until 2028 to reach ~34.6B units. However, its share of total Advanced Packaging shipments will decrease from 41% in 2022 to 34% in 2028. This is mainly attributed to the relatively slow growth rate of the mobile segments, where fan-in WLP has the major share.
- 2.5D/3D package shipments will increase by ~15% CAGR until 2028 to ~10.3B units.
- ED package share is ~1% of the total AP shipments. However, it will grow at 16% $CAGR_{2022-2028}$ to reach ~1.07B by 2028. The growth will be led by increased adoption in mobile (e.g., envelope tracker), automotive & base stations.
- Fan-out package units will grow by ~ 4% CAGR from 2022 to 2028 to 3.2B units.
- Flip-chip packages (FCBGA and FCCSP) will grow at a CAGR of ~10% to reach ~23.1B units in 2028.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING UNIT FORECAST 2023-2028

BREAKDOWN BY MARKET





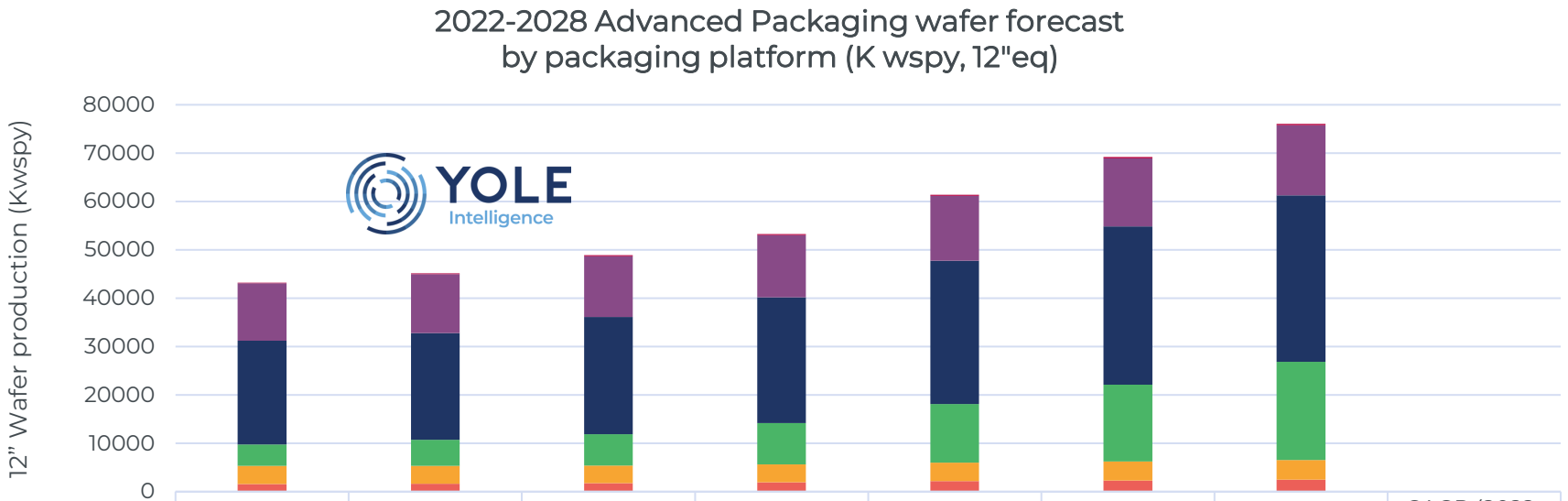
Mobile & Consumer	$CAGR_{2022-2028}$ ~ 4%
Automotive & Transportation	$CAGR_{2022-2028}$ ~ 11%
Telecom & Infrastructure	$CAGR_{2022-2028}$ ~ 24%
Others*	$CAGR_{2022-2028}$ ~ 11%

* Others include medical, industrial, & aerospace/defense segments

- The Mobile & Consumer segment constituted 84% of the Advanced Packaging units shipped in 2022. These will grow at a 4% CAGR and constitute 76% of the Advanced Packaging units by 2028.
- Telecom & Infrastructure is the fastest-growing segment in the Advanced Packaging market by units and will double its market share from 10% in 2022 to 19% by 2028.
- In terms of package units, the Automotive & Transportation market will decrease its share to 2% in 2028, however the market will growth will a healthy 11% CAGR.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING WAFER FORECAST 2023-2028



	2022	2023	2024	2025	2026	2027	2028	CAGR (2022-2028)
ED	134	167	209	234	267	308	332	16.41%
SiP	11890	12174	12562	12856	13368	14017	14481	3.34%
*Flip-Chip	21420	22010	24191	25958	29603	32750	34364	8.20%
2.5D/3D	4423	5436	6488	8546	12108	15841	20329	28.94%
WLCSP	3782	3692	3661	3739	3842	3914	4052	1.15%
FO	1572	1635	1762	1933	2183	2341	2491	7.98%
TOTAL	43220	45114	48872	53265	61371	69170	76050	9.88%
YoY Growth	6%	4%	8%	9%	15%	13%	10%	

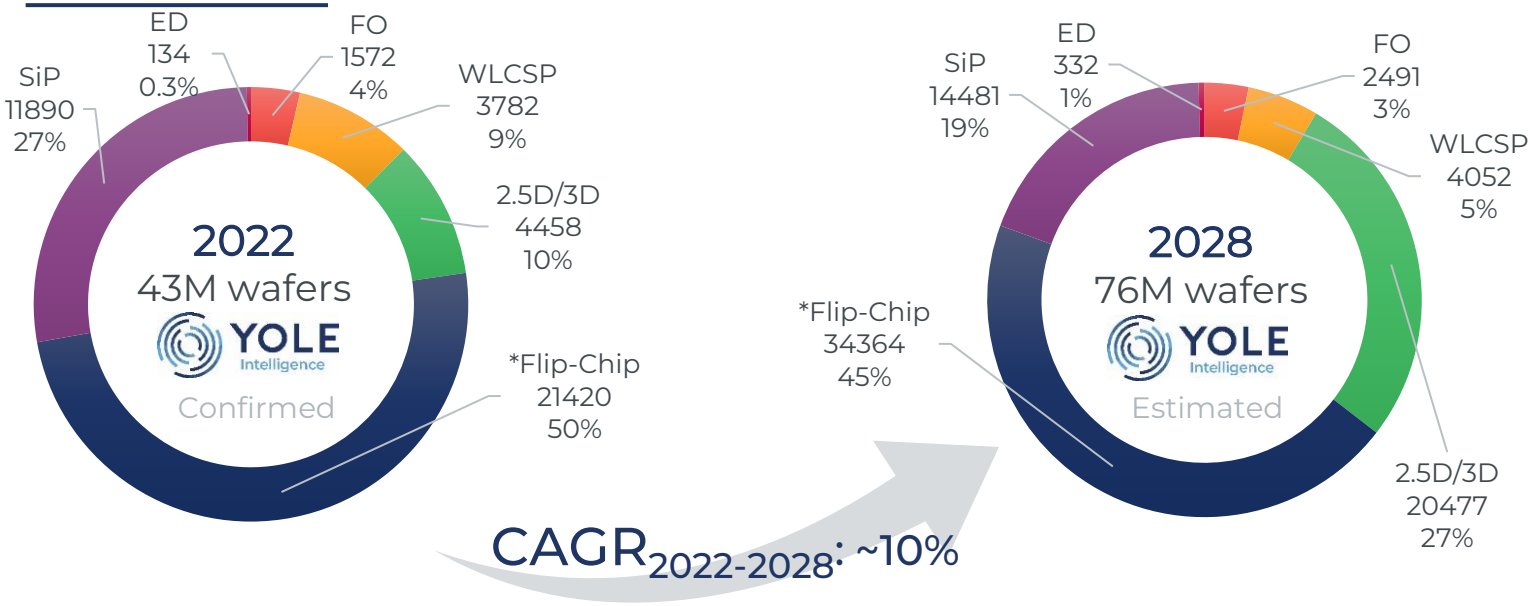
- Advanced Packaging wafer production reached ~43M 12" wafers in 2022. It is expected to grow at a ~10% $CAGR_{2022-2028}$ to reach ~76M wafers in 2028.
- Highest wafer CAGR remains with 2.5D/3D (29%), ED (16.4%), and flip-chip (8.2%).
- ED's share of AP wafers is low (1%), but it'll grow at an impressive CAGR of 16.4% from 2022 to 2028 to reach ~332K wafers.
- Growth areas for:
  - FO in mobile, networking, HPC, and automotive.
  - 2.5/3D in AI/ML, HPC, data centers, CIS, 3D NAND.
  - ED in automotive, mobile, and 5G base stations.

Data source: Advanced Packaging Monitor – Q1 2023

* Flip-Chip includes: FCCSP and FCBGA. It includes bumping, assembly and materials revenues.

ADVANCED PACKAGING WAFER FORECAST 2023-2028

BREAKDOWN BY TECHNOLOGY



Flip-chip	$CAGR_{2022-2028}$ ~ 8.2%
SiP	$CAGR_{2022-2028}$ ~ 3.3%
Fan-out	$CAGR_{2022-2028}$ ~ 8%
Fan-in WLP	$CAGR_{2022-2028}$ ~ 1.2%
2.5D/3D	$CAGR_{2022-2028}$ ~ 29%
Embedded Die	$CAGR_{2022-2028}$ ~ 16.4%

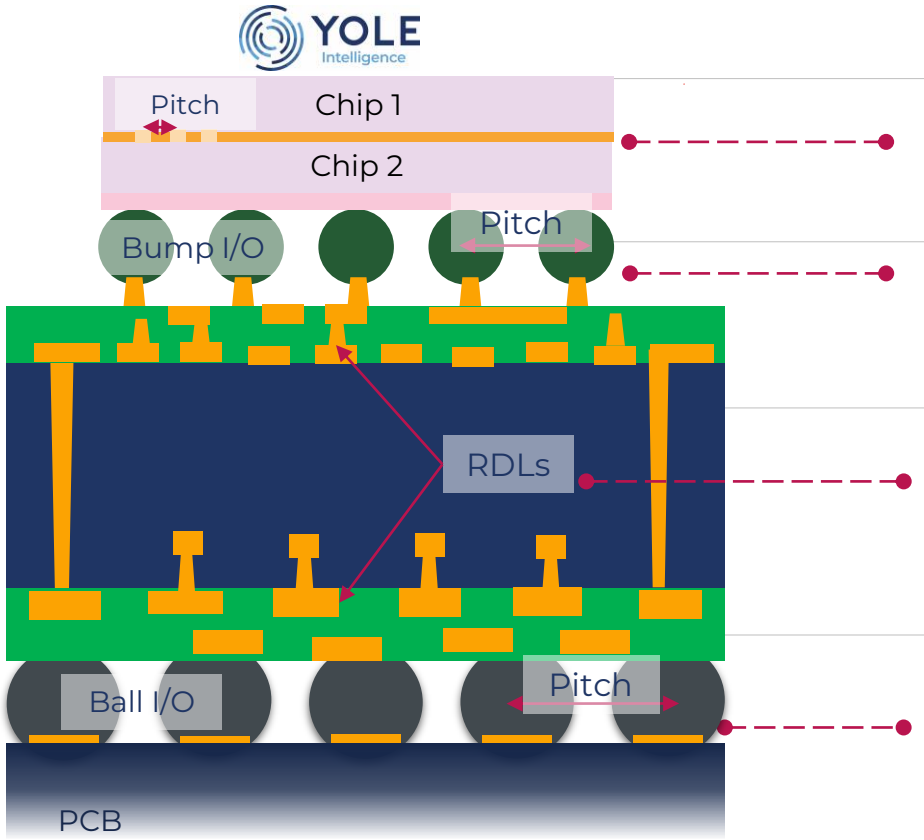
* Flip-Chip includes: FCCSP and FCBGA

- Concerning wafer starts, 2.5D/3D package wafer starts will increase by 29% CAGR until 2028 compared to 2022 to reach ~20M wafers. This is mainly attributed to the high demand for 3D memory, 3D NAND, Si interposer, and 3D SoC, driven by HPC and networking applications & CIS growth due to an increase in the number of smartphone cameras.
- ED's package share is < 1% of the total AP wafers. However, it will grow at 16.4% $CAGR_{2022-2028}$ to reach ~ 332K by 2028. The growth will be led by increased adoption in mobile (e.g., envelope tracker), automotive & base stations.
- Flip-chip technology presents the largest wafer production share (50% in 2022), and it will grow at a CAGR of ~8.2% to reach ~41.6M wafers in 2028, representing 45% of the total AP wafers.
- Fan-Out wafer production will grow 4% to reach ~2.4M in 2028.
- The number of fan-in WLP wafers will increase by 1.2% by 2028 compared to 2022 to reach almost 4M wafers. Its share of total Advanced Packaging shipments will decrease from 9% in 2022 to 5% in 2028. This is mainly attributed to the relatively slow growth rate of the mobile segments, where fan-in WLP has the major share.

Data source: Advanced Packaging Monitor – Q1 2023

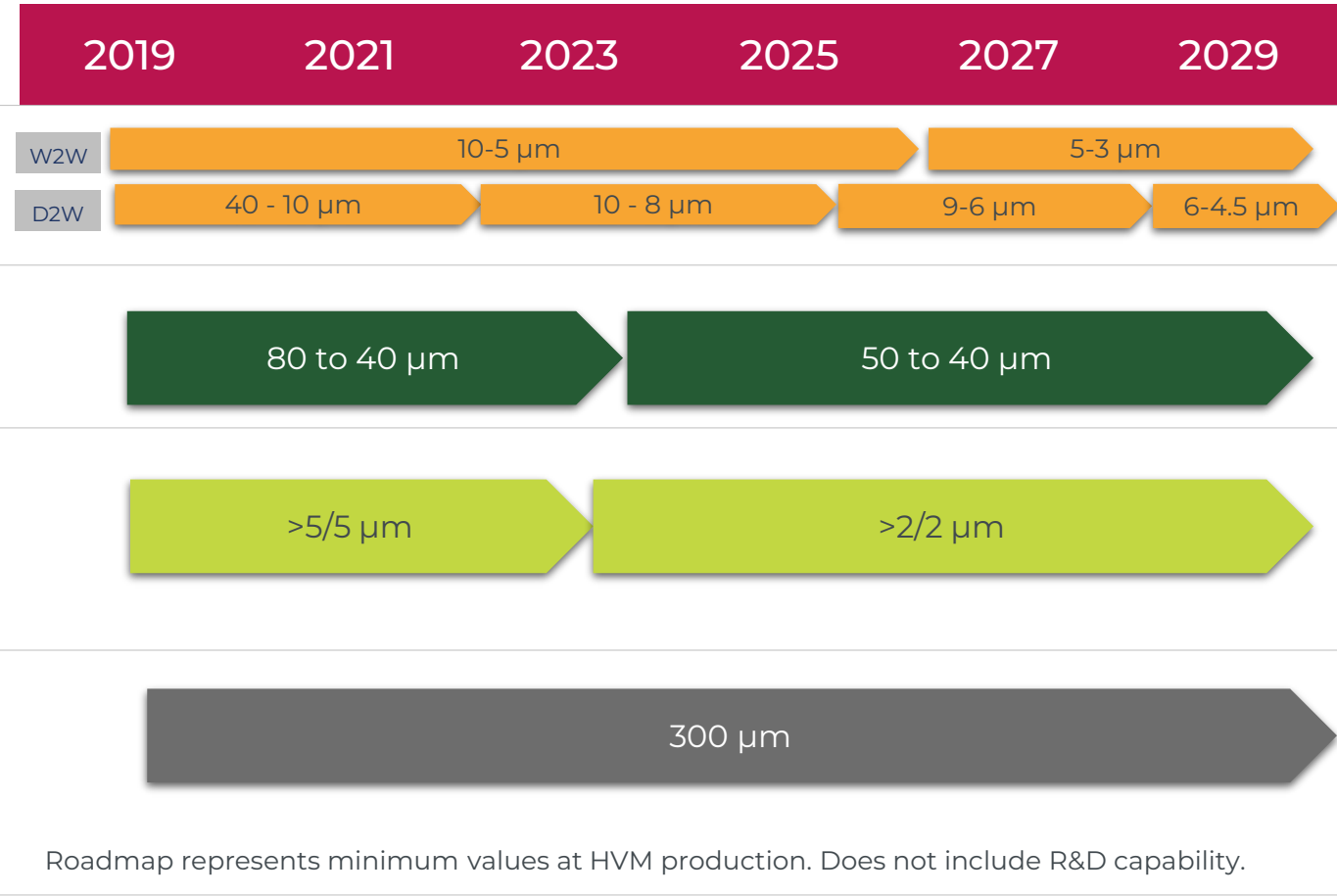
ADVANCED PACKAGING ROADMAP: I/O PITCH AND RDL L/S

A typical flip-chip IC Substrate



Schematic not drawn to scale

Advanced Packaging Technology Roadmap



Roadmap represents minimum values at HVM production. Does not include R&D capability.

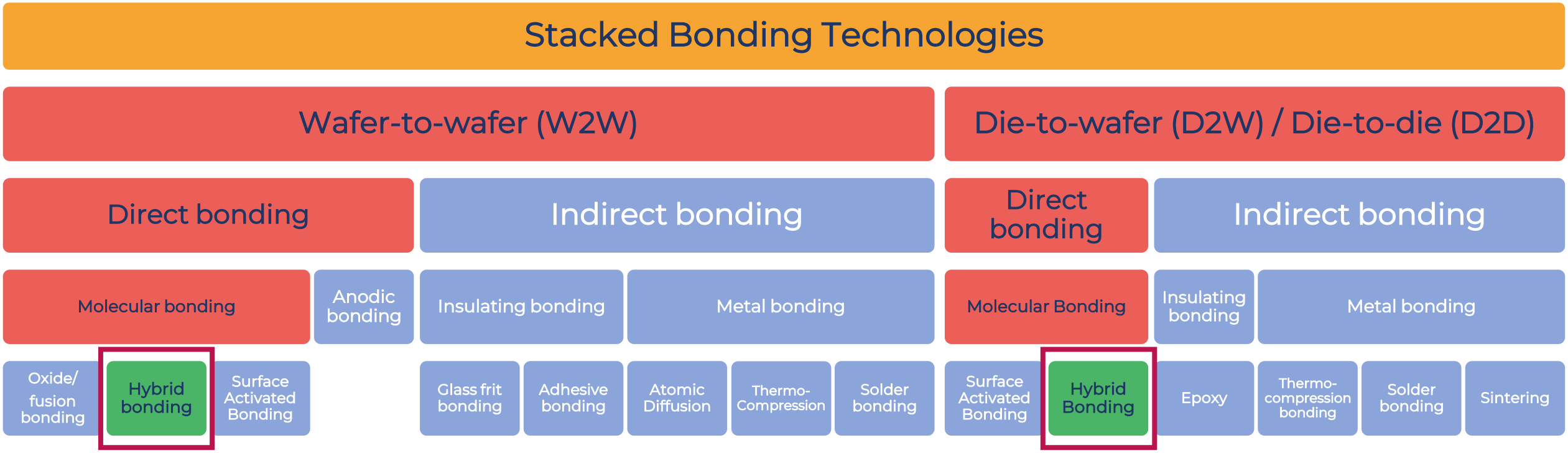
Bump I/O pitch is scaling much faster than Ball I/O pitch which drives a finer RDL L/S at IC substrate package level.

HYBRID BONDING

Where is hybrid bonding?

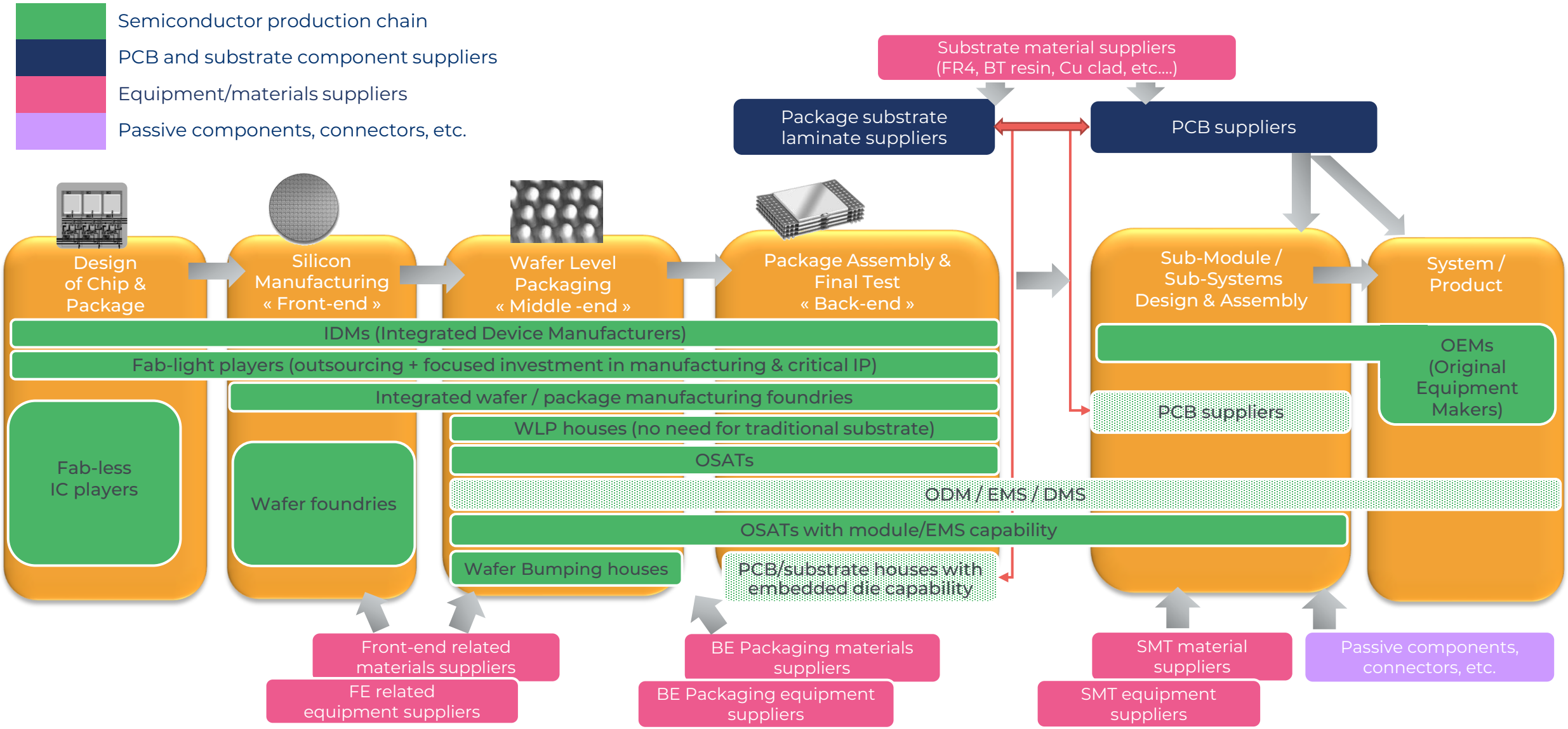
Wafer-to-Wafer (W2W)
Die-to-Wafer (D2W)
Die-to-Die (D2D)

- The interconnection process between chips and substrates is based on either W2W or D2W assembly. This assembly can be done directly or with intermediate material.
- Hybrid bonding is a direct, molecular bonding of two functional materials : dielectric (thin film such as SiO_2 or polymer) and metal interconnects (copper, tungsten, etc.).
    - Hybrid bonding can be used in W2W and D2W (including D2D) assembly.



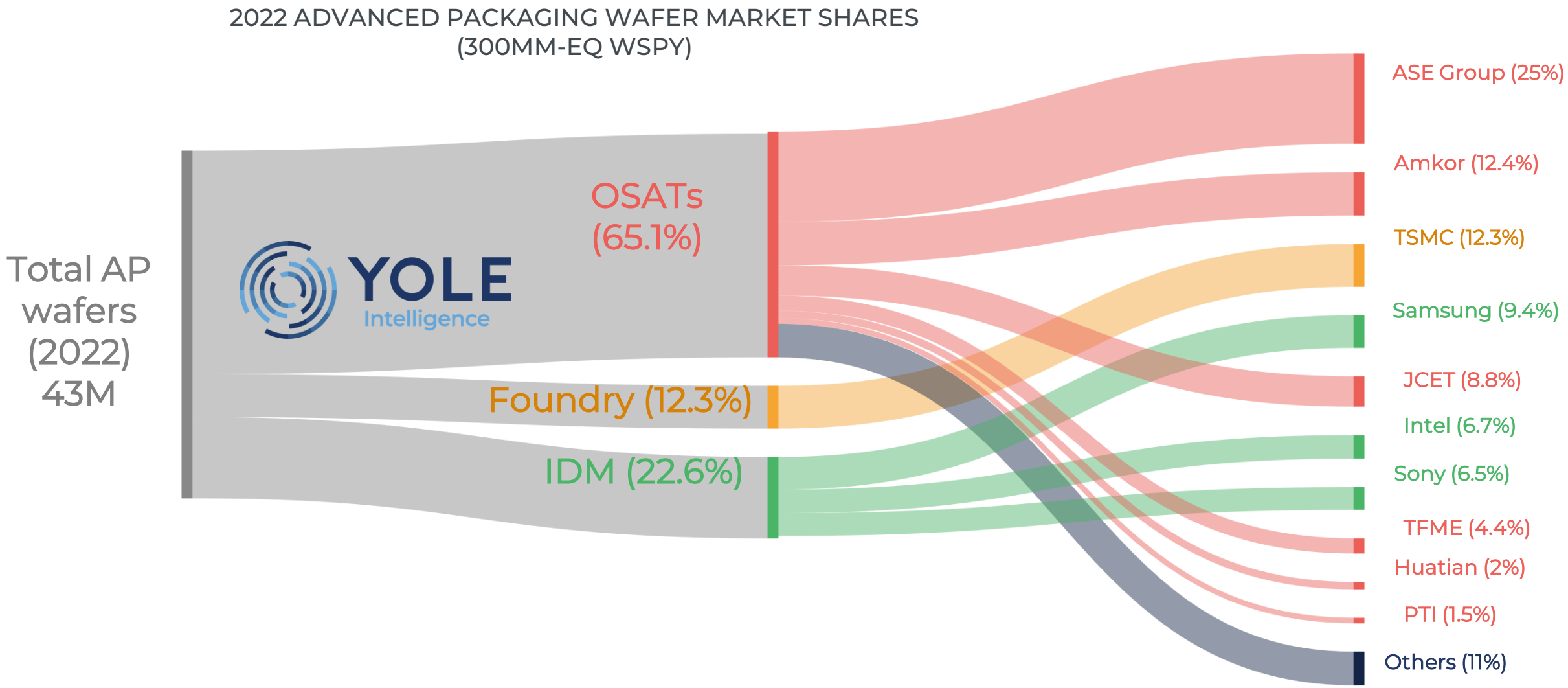
Hybrid bonding

SEMICONDUCTOR SUPPLY CHAIN – WHAT IS CHANGING?

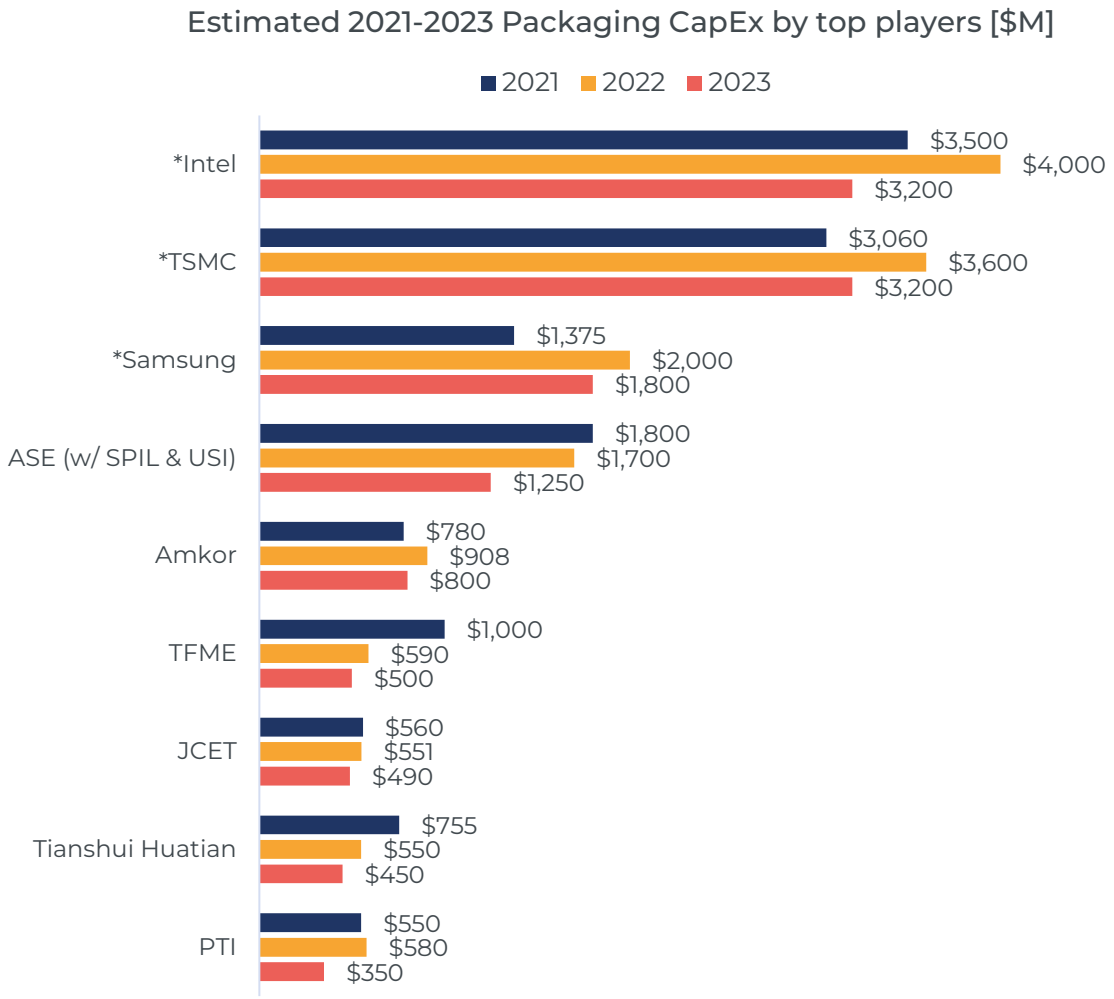


ADVANCED PACKAGING 2022 WAFERS MANUFACTURERS' MARKET SHARES

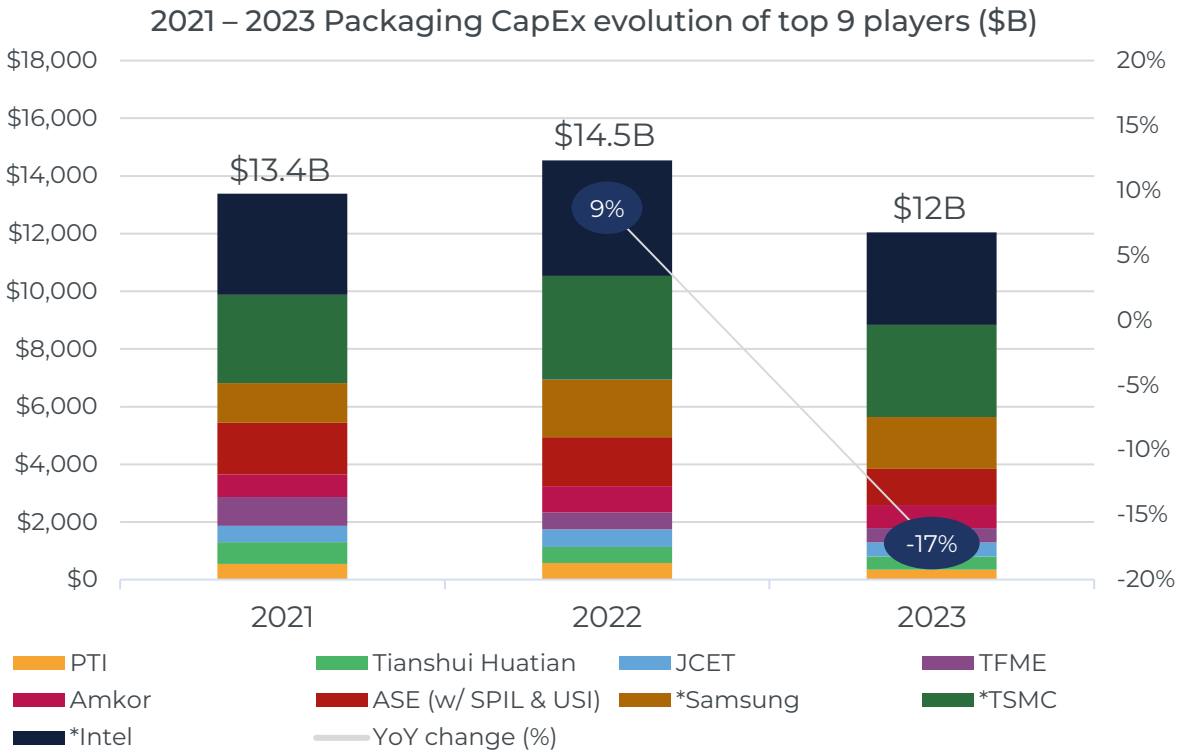
Breakdown by business model



2021-2023 CAPEX HIGHLIGHTS FOR PACKAGING PLAYERS



*Intel, TSMC, and Samsung's packaging CapEx were estimated based on earnings statements and announcements of investments, since packaging is not their primary business focus. All CapEx data is estimated based on information gathered during **Q1-2023**



In 2023 the packaging CapEx of the top nine players is expected to reach $12B, which is 17% lower than the previous year.

Packaging companies are being cautious about their investments and capacity increases and are decreasing their CapEx for 2023 with decreases from 10% to 40% compared to the previous year. The current macroeconomic situation is causing lower consumer confidence and therefore slowdown in demand, leading to high inventory levels and lower capacity utilization at semiconductor companies.

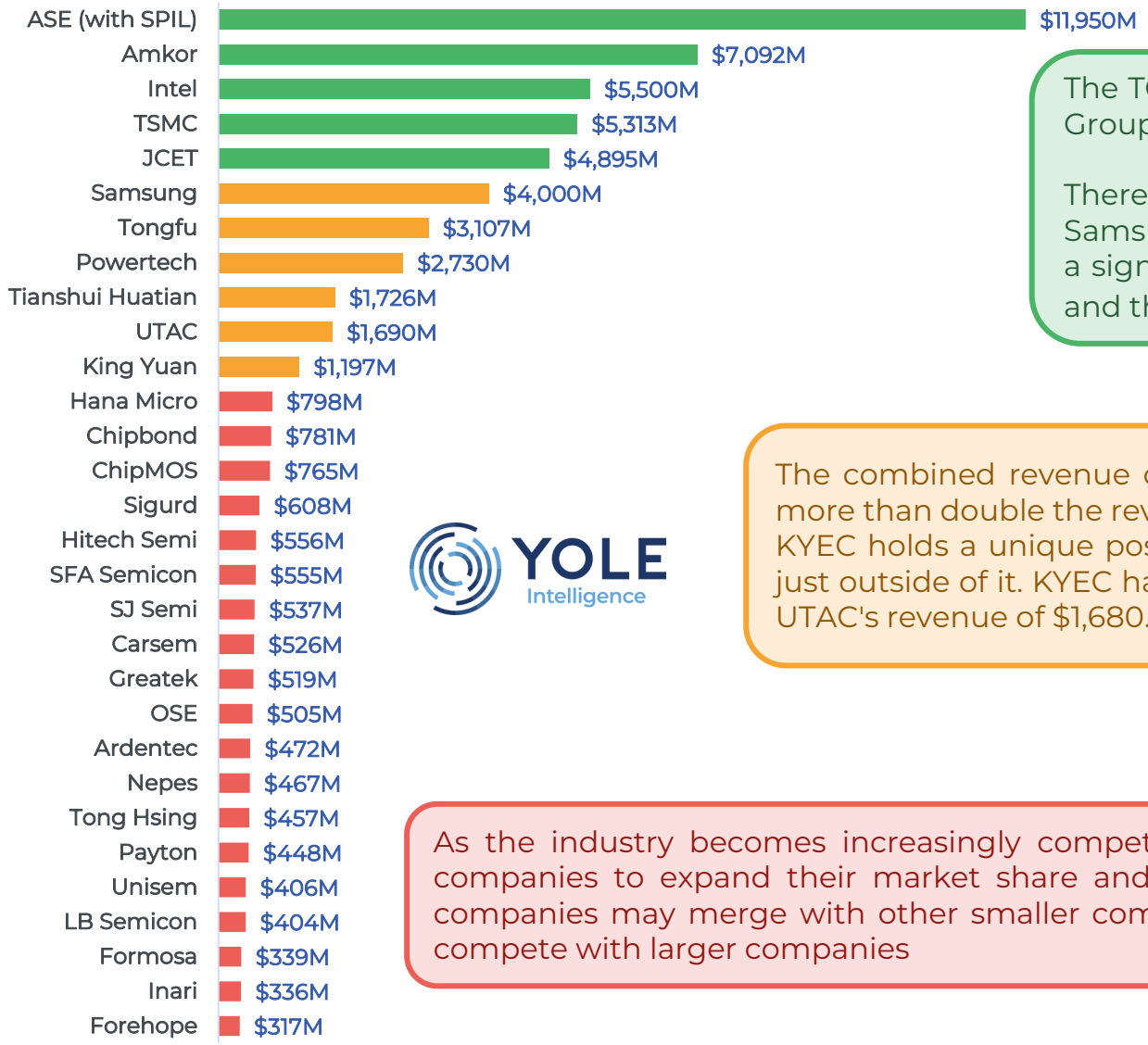
FINANCIAL OVERVIEW FOR TOP 30 PLAYERS

Revenue in 2022

Big players were separated from the rest.

The top 8 players dominate the market in revenue and continue with heavy investment in CapEx and R&D.

TOP 30 players ranking by 2022 revenue [$M]



The TOP 6 players hold a significant market share, with ASE Group having the highest revenue at $11,950 M.

There is a noticeable drop in revenue from JCET to Samsung and TFME, with a difference of $800 M, indicating a significant difference in market share between the TOP 6 and the rest of the companies.

The combined revenue of the TOP 11 companies amounts to $49 B, which is more than double the revenue of the remaining players combined.
KYEC holds a unique position in this group as it is close to the top 10 but falls just outside of it. KYEC has a revenue of $1,200, which is only slightly lower than UTAC's revenue of $1,680.

As the industry becomes increasingly competitive, larger companies may look to acquire smaller companies to expand their market share and gain a competitive advantage. Additionally, smaller companies may merge with other smaller companies to combine resources and expertise to better compete with larger companies

OSAT MARKET ECOSYSTEM

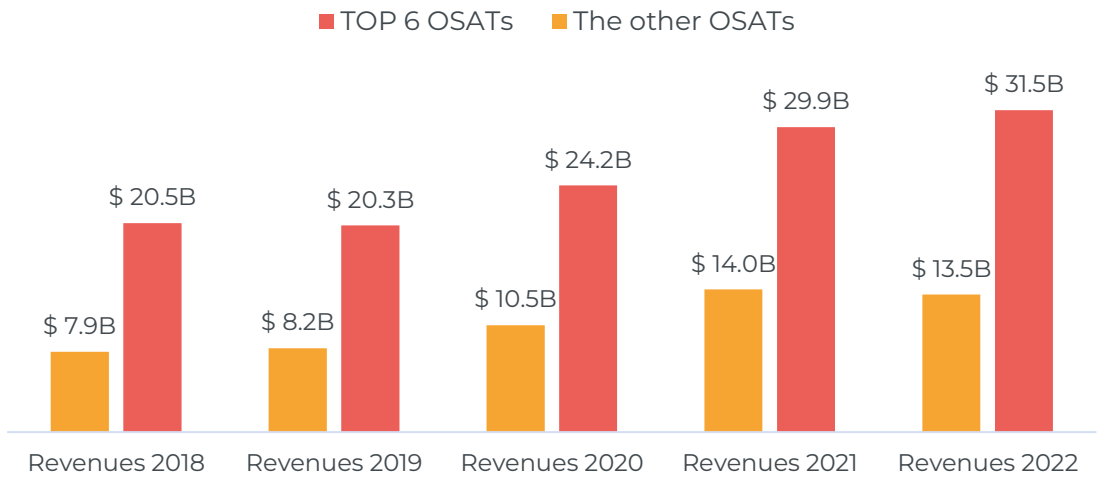
Focus on the TOP 6 OSATs

TOP SIX OSATs

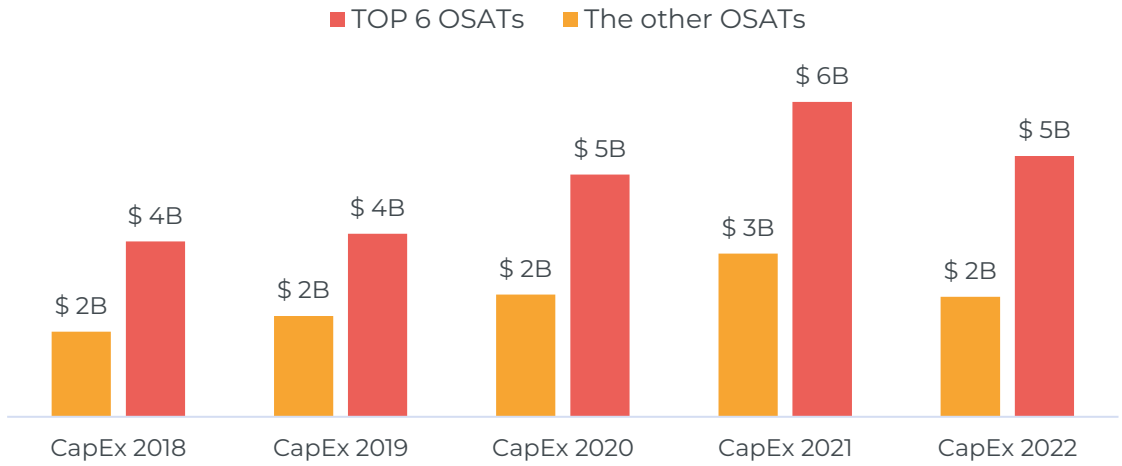
The other OSATs*

- The packaging market is strongly dominated by big players and the top six OSATs have taken 70% of the OSAT market in 2022.
- These are the companies not only investing the most but also investing more in advanced packaging technologies.
- Apart from IDMs and foundries, these are the companies with potential to penetrate the high-end performance packaging segment.
- On one side, the top OSATs hold strong collaborations with IDMs and foundries and as these collaborations get stronger, OSATs will slowing enter the high-end packaging supply chain.
- One another hand, top OSATs are allocating most of their CapEx to develop their own advanced packaging solutions. Hence, we expect their revenues to be increasingly driven by the advanced packaging segment.

Revenue Comparison: TOP 6 OSATs vs. The other OSATs



CapEx Comparison: TOP 6 OSATs vs. The other OSATs



* Non-exhaustive list of OSATs

KEY FINANCIAL SUMMARY: 2022

#1 player by different financial parameters

Relative R&D Expenditure (% of revenue)

12% nexperia

Relative CapEx (% of revenue)

53% FHEC

*FHEC: Forehope Electronic (China)

Net Margin (%)

54% tsmc

Revenue [$M]

$11 950M (with SPIL)

Revenue YoY growth Rate (%)

SJSEMI SJ Semiconductor (Jiangyin) Corporation 141%

Gross Margin %

tsmc 59.6%

SEMICONDUCTOR INDUSTRY CONTEXT

GLOBAL SEMICONDUCTOR BUSINESS GROWTH

The global semiconductor industry recorded a minor growth of 1.1% reaching $602 B. The semiconductor market is expected to see a decline in 2023.

- The World Bank projects that increasing living costs, ongoing supply restrictions in some industries, world political conflicts, and an increase in global consumer price inflation could cause the global economy's growth to drop from 6% in 2021 to 3.2% in 2022 and 2.7% in 2023. The World Bank forecasts a $CAGR_{2023\text{-}2028}$ of 3%, which is the lowest since 1990. The average over the two last decades was 3.8%
- The demand across industry sectors remained unequal through 2022, while global semiconductor sales increased by 1.9% from the previous year. Global demand for semiconductors decreased significantly in 2022 (by a staggering 2%) to $594B. The growth of the semiconductor industry is anticipated to decline in 2023 as electronics demand declines due to decreasing consumer expenses, inventory failures, and the current supply chain issues.
- High-end chip demand is still increasing, driven by the megatrends of AI (especially), 5G & HPC, metaverse, and autonomous vehicles. The consumer electronics sector, however, is currently slowing down. The semiconductor sector is experiencing a wave of instability that will endure until 2024 and beyond due to rising manufacturing costs, inflation, geopolitical unrest, and the conflict between Russia and Ukraine. However, all these variables work to raise semiconductor ASP, indicating that market value will keep rising. The semiconductor market is anticipated to earn $550 billion in revenues in 2023.

	2021		2022	
	2021 ($B)	YoY (%)	2022 ($B)	YoY (%)
Global GDP (at current prices)	97,076	6.1% - 13,39%	101,561	7.6%
Semiconductor sales	595	25%	602	1.1%
IC sales	463	28.2%	480	3.7%
Discrete/Opto/Passives	93	15%	100.2	7.8%
PCB industry	73 - 78	16% - 9,93%	82.4	5.6% - 12.8%
Contract manufacturing (EMS/ODM)	500	4.8%	560	12%

Data source: WSTS, Yole estimation

GROWTH MOMENTUM ACROSS SEMICONDUCTOR SUPPLY CHAIN

Advanced Packaging will exceed global and semiconductor industry growth with a 10.6% $CAGR_{2022\text{-}2028}$

- The Advanced Packaging market is expected to have a $CAGR_{2022\text{-}2028}$ of 10.6%, reaching $73B in 2028. The rise in semiconductor ASP and substrate shortage will impact Advanced Packaging technologies, and OSATs can be forced to increase their prices. Electronics manufacturing services (EMS) are also expected to grow at a ~7-8% CAGR in the next five years. While the traditional packaging market will grow at a 3.2% $CAGR_{2022\text{-}2028}$, the total packaging market will grow at a 6.9% $CAGR_{2022\text{-}2028}$, reaching $130B in 2028.
- New production capacity from substrate factories will gradually become available, and many packaging suppliers have been digesting inventory, causing their orders for materials to slow down. Demand for lower-end substrates will weaken, and the growth rate for high-end ABF substrates has started to decrease (but should remain positive in 2023). Unimicron has cut CapEx for 2023, and other companies are expected to follow suit to reduce operating risks. Despite the supply situation being better, the high-end substrate market is still not completely safe from supply constraints.

Industry	Estimated $CAGR_{2022\text{-}2028}$
Global GDP	3%
Contract manufacturing services	~ 5-6%
PCB industry	4.5%
Semiconductor industry	8-9%
Total semiconductor packaging	3.8%
Advanced Packaging	~ 10.6%
Traditional packaging	~3.2%

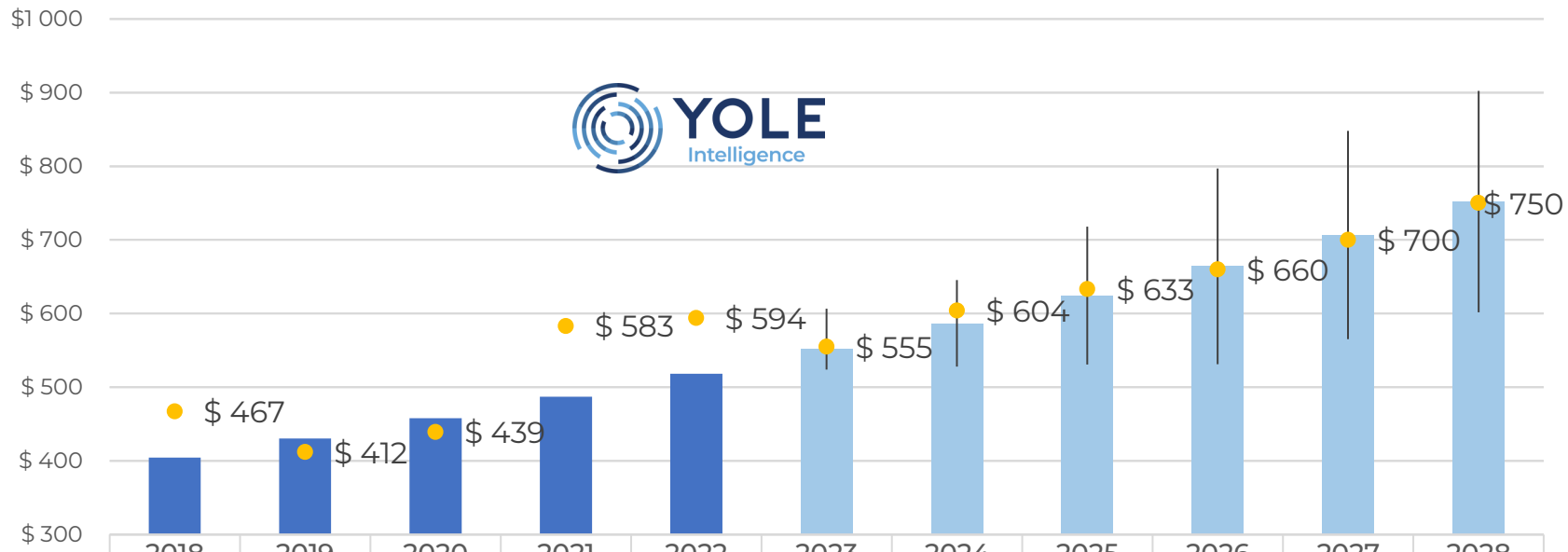
Data source: World Bank

SEMICONDUCTOR INDUSTRY OUTLOOK

The semiconductor market reached $594B in 2022, despite signs of economic decline in the world economy. However, the market is expected to re-adjust with an estimated YoY growth rate of -6% to reach $555B by 2023. This decline is due to a combination of factors, including decreasing buying power and consumer sentiment affecting demand, as well as the global economic crisis in 2023 and the inventory failures. This crisis has led to fab overcapacity and decreasing average selling prices (ASPs), causing a drop in revenues for semiconductor companies. While the semiconductor market has shown resilience in the past, it will face challenges in the coming years as it adjusts to changing economic conditions.

Following its jump of 32 % from 2020 to 2021, the semiconductor market grew to $594B in 2022, recording a stabilizing growth of 1.9 %.

Semiconductor Market revenues $B - 2018/2028 - Confirmed and expected - as of 02/2023



	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
Baseline value	$ 405	$ 430	$ 458	$ 487	$ 518	$ 552	$ 587	$ 624	$ 664	$ 707	$ 752
High						$ 607	$ 645	$ 718	$ 797	$ 848	$ 902
Low						$ 524	$ 528	$ 531	$ 531	$ 565	$ 602
Confirmed/Expected Revenues	$ 467	$ 412	$ 439	$ 583	$ 594	$ 555	$ 604	$ 633	$ 660	$ 700	$ 750

Data source: WSTS, Yole estimation

THE SEMICONDUCTOR GROWTH MOMENTUM STOPS IN 2023

Influenced by macroeconomic factors and the global economic decline, the semiconductor market will see a negative YoY growth of 6% in 2023, reaching $550B.

- After getting over the COVID-19 impacts on the supply chain, the semiconductor industry continues to have short and mid-terms disruptions in the supply chain due to geopolitical tensions. In 2022, the price inflation and the Russia-Ukraine war covered both the post-pandemic demand and the resurgence. They caused a supply bottleneck in the global semiconductor market, leading to a chip shortage. This shortage continues with some signs of recovery in 2023 but is estimated to recover fully only after 2023.
- The semiconductor industry showed a stabilization through the 2022 year, with a YoY gain of 1.9% over the previous year, thanks to the significant rise in demand still in the first part of the year, maintaining a growth in consumer, computer, 5G, and automotive semiconductors. However, supply problems persisted into 2022, causing a lack of chips, substrates, and other materials, as well as long lead times for equipment. To increase the industry's resilience in the upcoming years, semiconductor businesses are investing in capacity. Government-supported plans were announced for local semiconductor ecosystems while their impact on the global supply chain might appear late in 2023 and the upcoming years.
- In 2023, the global economy continues to be affected by the political conflicts, the lasting supply constraints across several sectors, increasing geopolitical issues, global consumer price inflation and ongoing inventories digestion. Besides, an estimated negative YoY growth of -6% is expected, reaching $550B in revenue for the entire year. However, the 2nd half of 2023 is expected to witness the start of a recovery of the semiconductor industry for the upcoming years.
- The US-China trade war is pushing local chip manufacturing with more announcements of new fabs and expansion of existing fabs, supported by local governments with attractive incentives, not only inside the US, or China but inside other countries too. These efforts reflect the will to avoid future semiconductor supply chain disruptions by securing the supply in the long term amidst all the current constraints.
- Raw material constraints, especially the substrate materials used in Advanced Packaging platforms, e.g., flip-chip and fan-out, have continued to be one of the critical concerns. Substrate suppliers are increasing CapEx investments for needed capacity expansion as they try to secure their supply for customers with whom they already hold long-term agreements. In 2023, the decreasing demand on mobile and consumer and the slow-down of the sever market growth reduced the pressure on the IC substrate market and helped to ease the shortage.
- Some foundries and OSATs are expected to announce lower prices in 2023, due to overcapacity and the decreasing demand. OSATs have experienced a drop in utilization rates in Q4 2022 and all of Q1 2023. Price pressure is a result, and many businesses are being compelled to lower ASPs. As a result, OSATs are cutting back on their planned Capex for 2023 and deferring plans for capacity development.

NEW TRENDS & DRIVERS: OPPORTUNITY FOR SEMICONDUCTOR PACKAGING

Require back-end and assembly innovations: panel-level packaging, high-accuracy bonders, TCB, D2W/W2W bonding, and photonics integration in packages. As for materials, there is a need to develop new dielectric materials, mold compounds, underfill, solder interconnects, and TIMs to meet the stringent performance and reliability requirements demanded by next-generation hardware.

System requirements

- computing power
- speed
- bandwidth
- functionality

- Lower latency
- Lower power
- Lower cost

- System integration
- More sensors
- More memory
- Hardware-software compatibility

Opportunities for different devices

Megatrends create business for variety of ICs from high end xPUs to low end discretes

- CPUs, GPUs, SoCs, APUs, FPGAs
- ASICS, DSPs, MCUs
- MEMS/Sensors
- Power ICs/discretes
- Memory
- Optoelectronics

Opportunity for packaging

Create business opportunities for both advanced and traditional packaging platforms

Advanced packaging (WLPs, flip-chip, TSV) business opportunity supported by AI/ML, Mobile, AR/VR, 5G, smart automotive

Traditional packaging (wire-bond lead-frame based) business opportunity created by IoTs, Industry 4.0, and smart automotive

Mega trends like mobile, automotive, IoT, and industry 4.0, require a variety of MEMS sensors that create opportunities for both traditional & Advanced Packaging

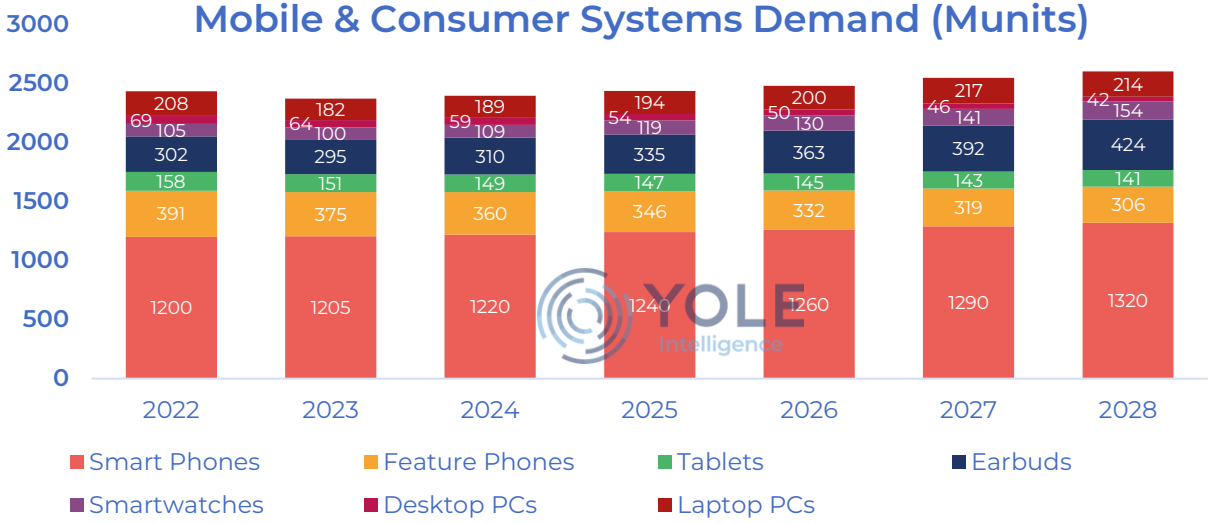
Opportunity for fab/front-end

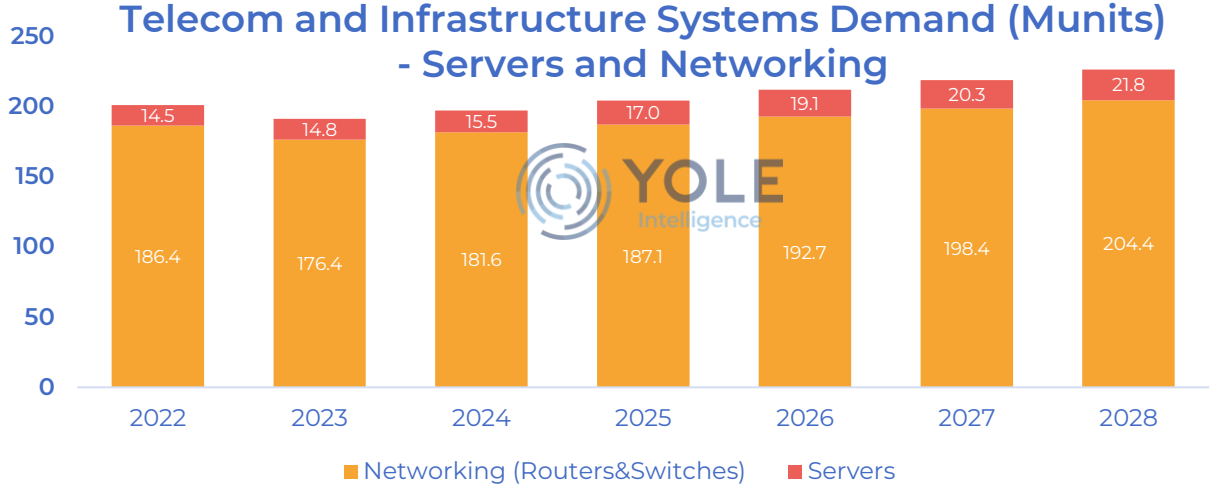
Front-end scaling slows but continues: Moore's Law keeps going but at a slower pace => high-end fab business continues growing (5nm & below)

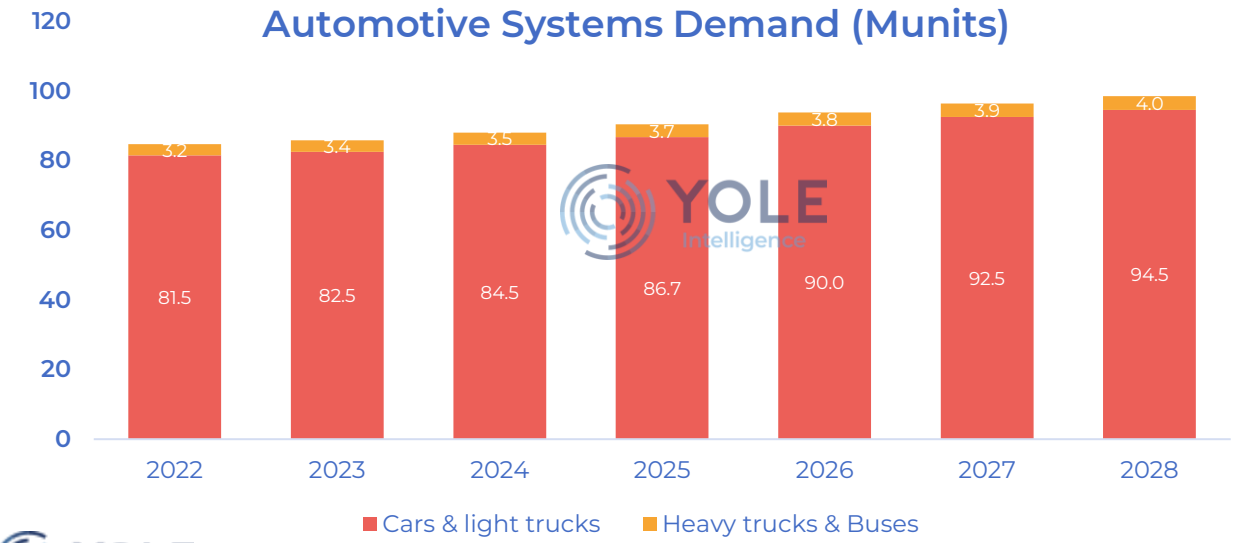
More & more heterogeneous integration to support functionality, faster time to market, and low cost: More than Moore's => Resurgence of legacy fabs => Increasing business

8" wafer fabs and related tools demand to remain strong

END-SYSTEMS DEMAND (2022-2028)





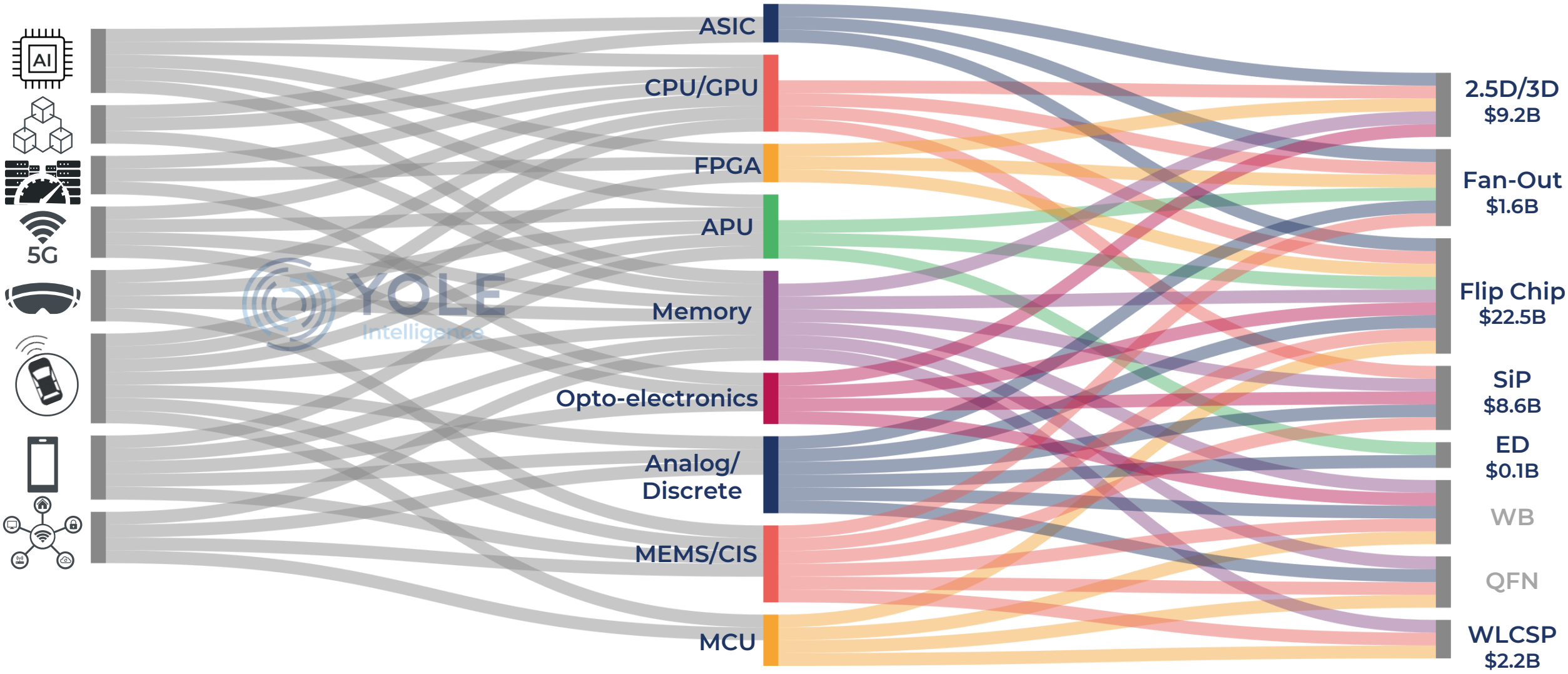


- Smartphone and tablet market will remain saturated over the next five years with 1% and -1% $CAGR_{2022-2028}$, while wearable devices (smart watches and earbuds) will have an average of ~16.4% $CAGR_{2022-2028}$.
- The total smartphone & PC (laptop and desktop) demand, in terms of units, will experience an average ~2.6% $CAGR_{2022-2028}$.
- Overall automotive demand is expected to have a 3% $CAGR_{2022-2028}$ driven by Infotainment and ADAS applications.
- Telecom & Infrastructure demand is set to soar to new heights as the Coronavirus pandemic drives higher growth with a 4% CAGR for the next few years.

*End-system units from Q1 2023 estimation

SEMICONDUCTOR PACKAGING OPPORTUNITIES

The Incredible Complexity To Meet the Growing Demand for Semiconductor Hardware



CHIP SHORTAGE TO EASE IN 2023, WITH CHALLENGES AHEAD

The chip shortage issue is expected to end in 2023.

The semiconductor industry is expected to witness an end to the chip shortage in 2023, but with an oversupply risk in the short term. While increasing capacity and changes in chip demand are easing the shortage, the dependency on semiconductors for emerging technologies such as electric and autonomous vehicles requires a need for capacity qualification. However, unpredictable end-system demand and supply due to geopolitical crises, and other factors pose ongoing risks.

As excess inventory was accumulated, the affected companies must optimize their inventories, focus on bottleneck management, and transition to advanced technology nodes to mitigate the impact of the shortage. Meanwhile, worldwide governments are pledging billions to shore up their chip supply chains, and the CHIPS Act in the US seeks to boost innovation and production in the semiconductor industry. Despite some lead time stabilization and decline, lead times remain far longer than average pre-pandemic lead times, creating ongoing challenges for the industry.

Big fab players invested billions of dollars on new wafer fab facilities in the past year. More investments are focusing on 300 mm wafers and fewer on 200 mm wafers. Products are expected from the new fabs in 2024. This is expected to reduce the excess demand for 300 mm wafers though it could take longer for 200 mm wafers.

Manufacturers are investing in long-term partnerships, joint ventures, and collaborations to develop or acquire chip capacity. Some major OEMs are considering moving chip design in-house, a trend to more flexible supply chain platforms.

In summary, the industry has started to notice relief from the chip shortage at some IDMs and foundries at the beginning of 2022 compared to the worst constraints reported in 2021. While 2024 could be the year to bring demand and supply into balance, it is expected that supply will exceed demand in the next 2 to 5 years.

U.S. VS. CHINA TECH WAR – TIMELINE

May 15, 2019
The U.S. Department of Commerce adds Huawei to the Entity List.

June 21, 2019
Additional Chinese tech companies, such as Sugon, Hygon, and Haiguang are added to the Entity List.

December 18, 2020
SMIC added to Entity List with restricted access to key technologies.

January 20, 2021
Joe Biden inaugurated as new U.S. President.

April 8, 2021
U.S. adds seven Chinese super-computing players to entity list for alleged military support.

June 6, 2021
White House ranks semiconductor manufacturing as no. 1 in "building resilient supply chains" report.

July 6, 2022
U.S. pressures ASML to halt sales of critical equipment to China (DUV lithography).

July 30, 2022
Lam Research and KLA prohibited from selling 14nm or below equipment to China as U.S. tightens export restrictions on semiconductor equipment.

August 9, 2022
The U.S. Congress passes the **CHIPS Act.**

August 12, 2022
U.S. implements export ban on advanced IC design EDA software to China (3nm or below).

August 13, 2022
U.S. launches export ban on high-performance GPUs to China.

August 31, 2022
U.S. bars Nvidia and AMD from selling advanced AI chips to China

October 7, 2022
BIS announces comprehensive sanctions on Chinese semiconductors with restrictions on U.S. personnel.

December 16, 2022
Biden blacklists Chinese AI chip sector players including YMTC and 21 major players.

CHIP INVESTMENTS ACCELERATE AS GOVERNMENTS STEP UP EFFORTS

Semiconductor support-plans to face geopolitical tensions

Science and chips act

- Signed in August 2022.
- A total budget of $278B in spending over a decade.
- The biggest share is for scientific R&D and commercialization (>$200B)
- A tax credit of $24B for chip production
- $3B for leading-edge technology and wireless supply chain.
- $2.5B for Advanced Packaging programs.
- Out of the total $278B, $52B is for production, R&D, and workforce development.

EU CHIP ACT

- Signed in April 2023.
- Double the EU's share of global chip production by 2030 (up to 20%).
- Reduce its vulnerability to geopolitical shocks.
- $3.5B was allocated to support large-scale technological capacity building and innovation across the EU in the semiconductor sector
- R&D tax credits.
- $43B support plan for the european semiconductor industry.

China act

- To be implemented in 2024 Q1.
- Target self-sufficiency in chip production.
- $143B support package for the local semiconductor. ecosystem, allocated over 5 years (by 2028).
- Corporate revenue tax exemptions of around $20B.
- Preferential tax policies for the local semiconductor industry.

K-CHIP ACT

- Passed in March 2023.
- Secure the chip production leadership.
- Safeguard economic priorities and foster a vibrant semiconductor industry for the country.
- Increase tax credit to 15% from the current 8% for major companies investing in manufacturing facilities.
- For smaller and medium size companies, the tax break goes to 25%, up from 16%.

Strategy for semiconductors and the digital industry

- Aiming to maintain 10% of the market by 2030.
- The Japanese government is providing a subsidy of up to 476B yen ($3.68 B) to support and develop chip technologies.
- The government will cover 1/3 of the semiconductor equipment investment of any company in exchange of 10 years guarantee of domestic shipments during any possible shortages.

CHINA SEMICONDUCTOR BUSINESS UPDATE

What Governmental Initiative Could China Adopt To Remain Competitive?

In October 2020, the Chinese government revealed a five-year economic plan aimed at driving growth through the use of advanced technology and balancing external and domestic demand. This plan forms the basis of the **"Made in China 2025"** initiative, which is designed to make China technologically independent and self-reliant as a strategic objective. The Chinese president has emphasized the importance of "independent, safe, and controllable" supply chains, which implies a dual approach that includes second sourcing as a backup for a relatively complete semiconductor industry supply chain. The ultimate goal is for China to achieve 70% self-sufficiency in semiconductor manufacturing by 2025.

To support this goal, the Chinese semiconductor industry will receive over $143 billion in support over the next five years, three times the size of the US Chips Act. The plan includes a 20% subsidy on the purchase of domestic chipmaking equipment and tax credits, aimed at supporting the expansion of wafer fabs, assembly and packaging plants, and R&D facilities.

However, Chinese companies are limited to supporting chip manufacturing on more mature process nodes and are unable to compete at the leading edge. The support plan might reinforce the decoupling of China from the other countries over rising tensions regarding semiconductors, which are now seen as a major strategic sector.

The US government has been tightening the embargo on semiconductors, and the October 2020 increase in export controls has made it more difficult for Chinese chip makers to get supplies and support for chipmaking equipment.

As a result of these actions, China is taking steps to encourage and support domestic semiconductor production through subsidies and tax credits. However, even with this support, China is unlikely to be able to compete at the leading edge of chip manufacturing in the near- to medium-term. To do so, China will need to invest in R&D to develop techniques such as immersion-deep ultraviolet lithography and extreme ultraviolet lithography across a breadth of chipmaking technologies.

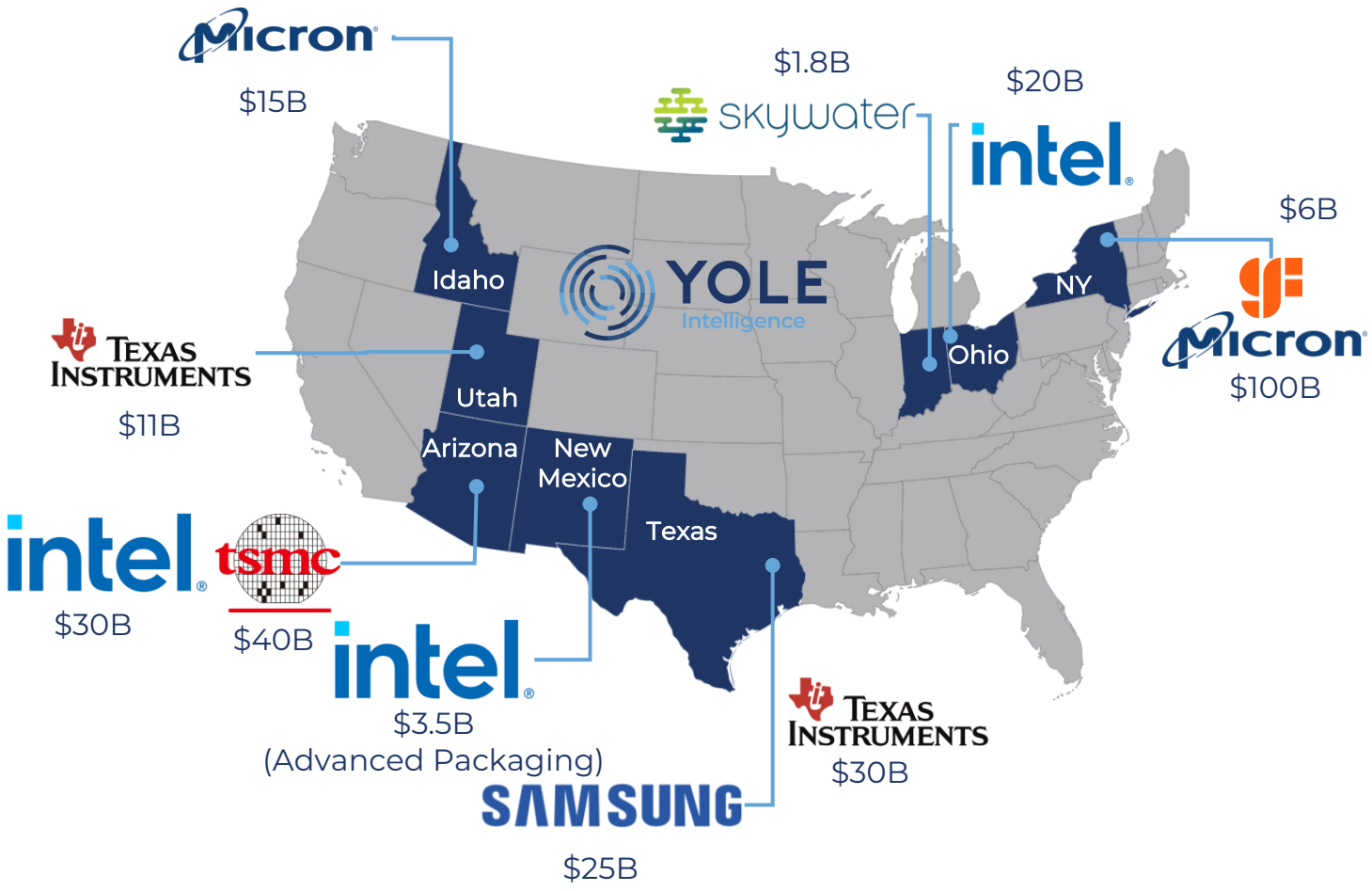
While China still lags behind the US in semiconductor technology, there is potential to catch up by striving for more breakthroughs and innovation. It is predicted that it will take at least a decade for China to achieve self-reliance in leading-edge technologies, but acquisitions or mergers with companies possessing similar technologies could shorten that time. To improve its chances of technological leadership, China needs to continue focusing on useful strategies, such as regular reviews of government plans, incorporating leading-edge technology content in universities, identifying talent for key development technologies, investing more in R&D, filing more patents, and leveraging M&As to support company growth.

US CHIPS AND SCIENCE ACT

Massive Investments in Semiconductor Plants

The US is finally breaking ground for brand-new chip plants. Five major chipmakers, including Intel, TSMC, and Samsung Foundry are building new semiconductor production facilities in the US, and they are set to spend over $70 billion on US fabs by 2025. Intel is investing $30 billion in two new fabs in Arizona, GlobalFoundries is building a new fab in New York that costs around $6 billion, and TSMC and Samsung Foundry are building new fabs in Arizona and Texas. Texas Instruments is also building a new massive fab in Texas, for about $30 billion over a decade.

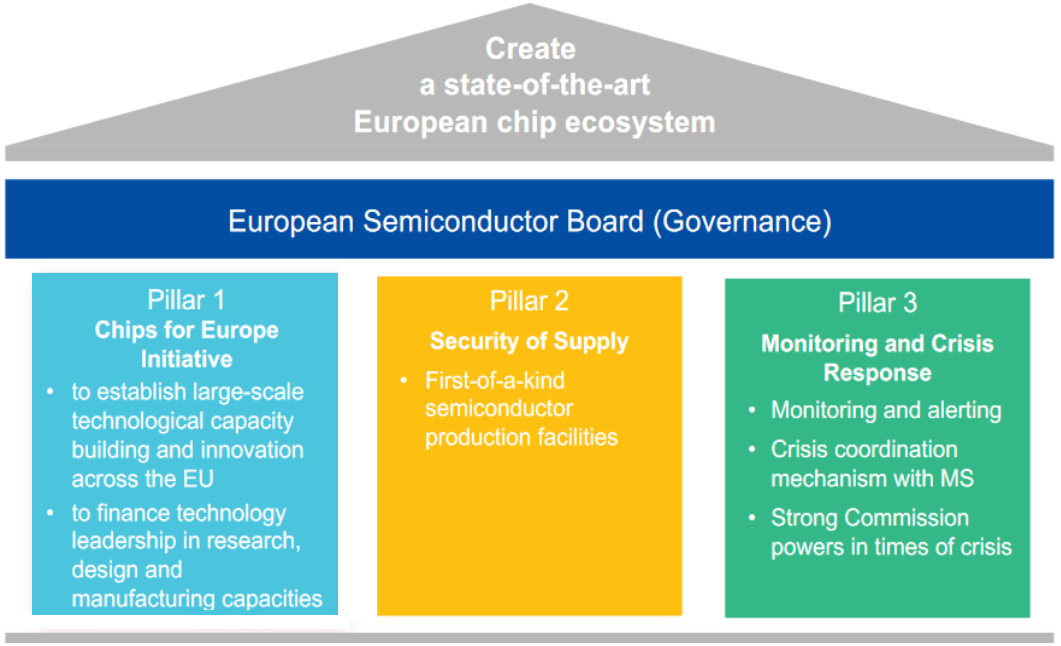
The total investment might hit the $200 billion mark (or even exceed it) over the next decade.
The investment is being made possible by incentives from local authorities, government subsidies, engineering talent, and the existing semiconductor production supply chain. However, it is uncertain whether these new American fabs will be able to compete against the upcoming Gigafab projects in South Korea and Taiwan.



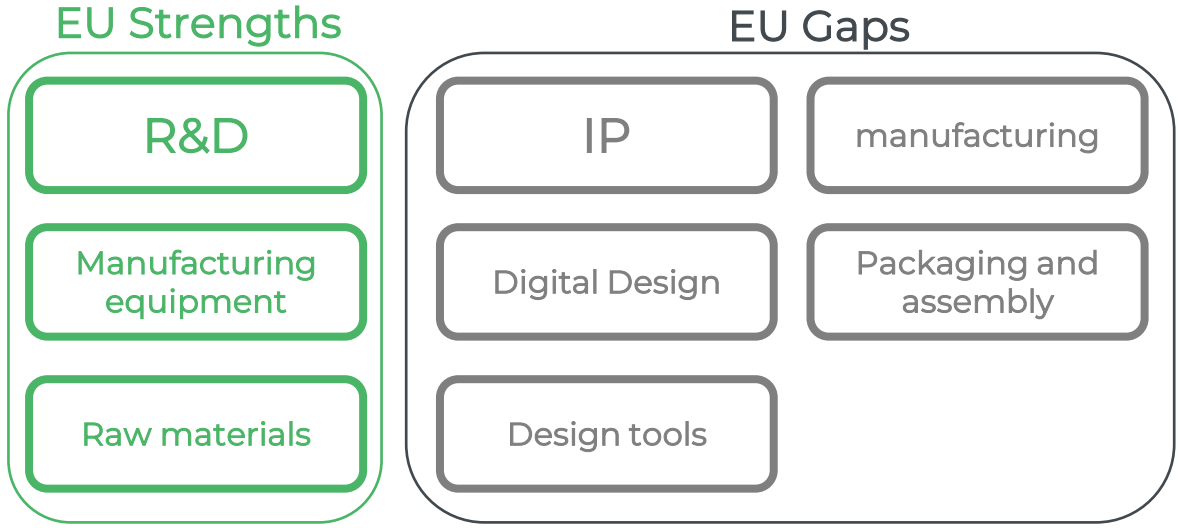
EUROPEAN CHIPS ACT (1/2)

The European Chips Act was announced in 2022, as the current supply shortage has highlighted Europe's reliance on imported chips. It aims at encouraging semiconductor production in the European Union. The goal is to reduce the EU's exposure to supply chain risks and regain a bigger market share. The EU Chips ACT has three pillars: research, development, and innovation, a new state aid exemption for semiconductor manufacturing, and measures to monitor and intervene in the supply chain if necessary.

The plan is part of the "Chips for Europe" investment plan and aims to establish Europe as a leader in the semiconductor market by increasing production to 20% with a € 43B investment. As of 2022, Europe accounts for less than 10 percent of global semiconductor production.



Source: EU



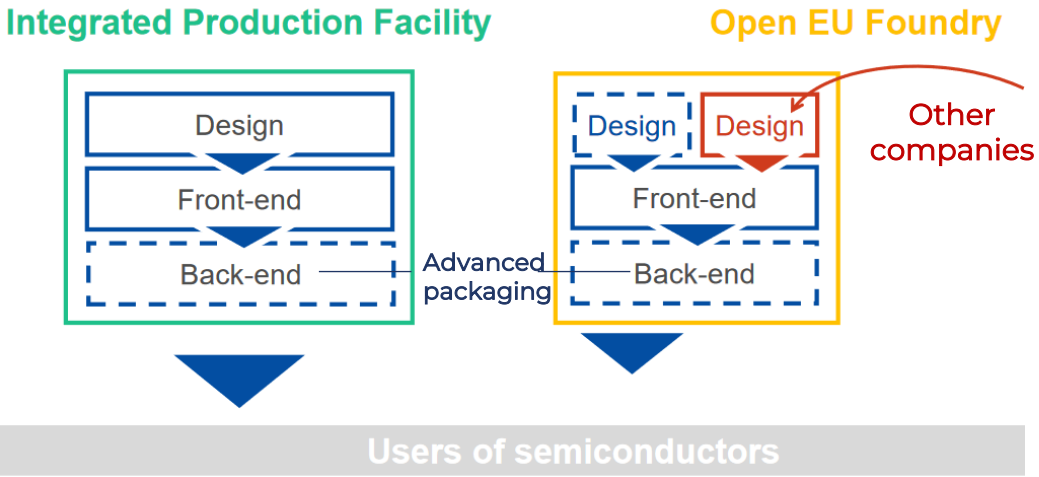
Today, the EU is strong in R&D, raw materials, and manufacturing equipment. With the EU Chips Act, the aim is to maintain the leadership in these segments and work on reducing the gap in the other segments, which leads to reducing Europe's dependence on imported chips and ensuring a reliable supply chain.

EUROPEAN CHIPS ACT (2/2)

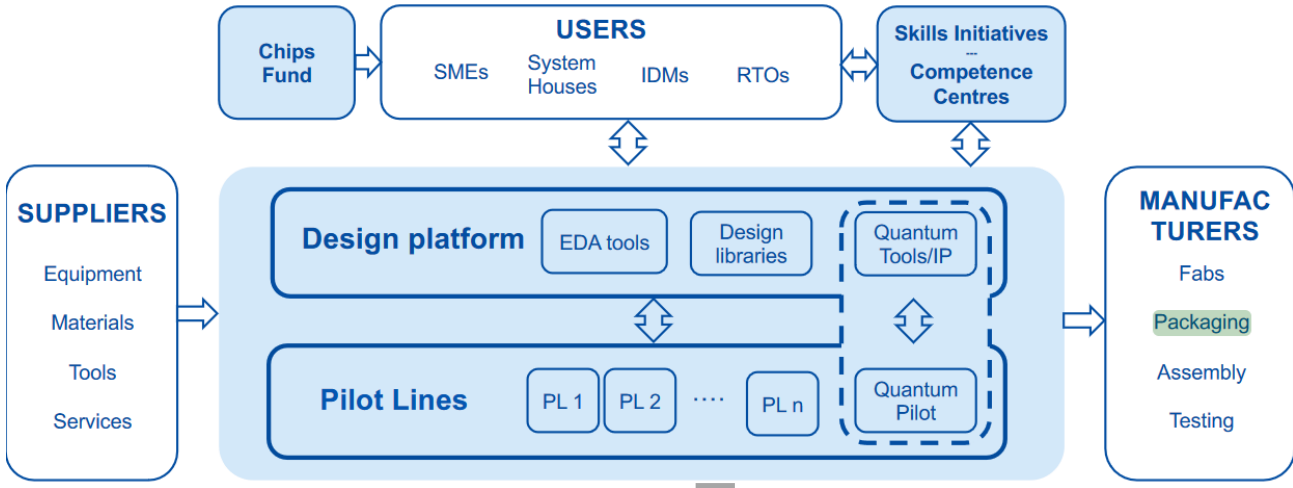
The Advanced Packaging as The Second Pillar of EU Chips Act

The second pillar of the EU Chips Act aims to implement projects that assure a secure and resilient supply chain. It focuses on two types of first-of-a-kind facilities, IPF and OEF, in order to bridge the gap from lab to fab by taking advantage of the R&D leadership in manufacturing, packaging, and testing.

- **Integrated Production Facility (IPF):** A vertically integrated first-of-a-kind facility that produces the chips they design and market
- **Open EU Foundry (OEF):** First-of-a-kind facility that (also) produces chips that are designed and marketed by unrelated undertakings.

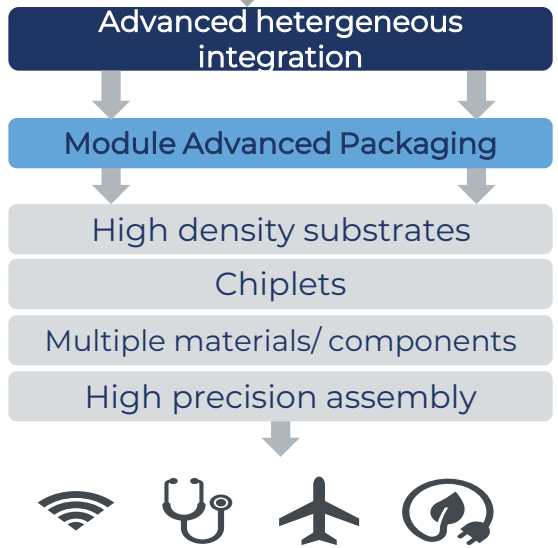


Source: EU



Source: EU

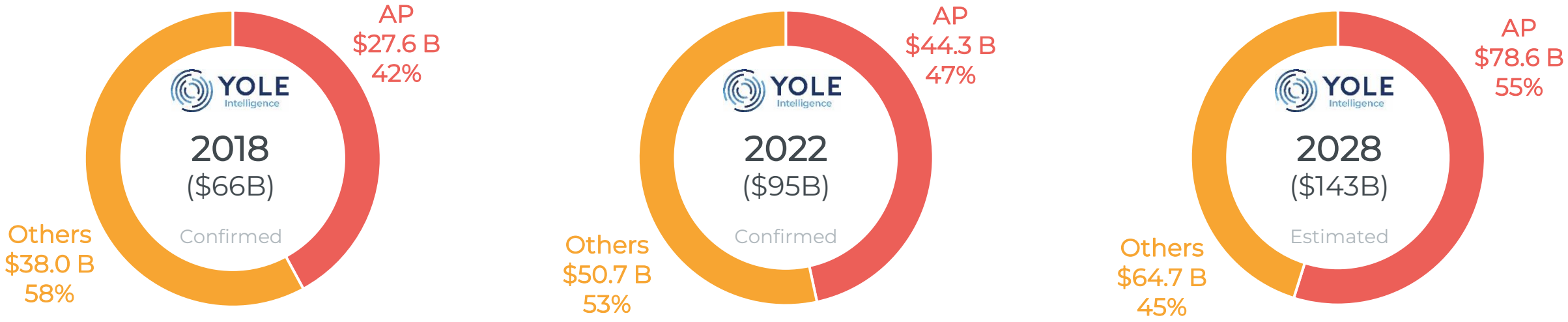
The EU Chips Act depends on several Pilot Lines covering front-end, back-end, etc.
One of the important Pilot lines is heterogenous integration.



ADVANCED PACKAGING MARKET FORECASTS

ADVANCED VS TRADITIONAL TECHNOLOGIES OVERVIEW 2018 to 2028

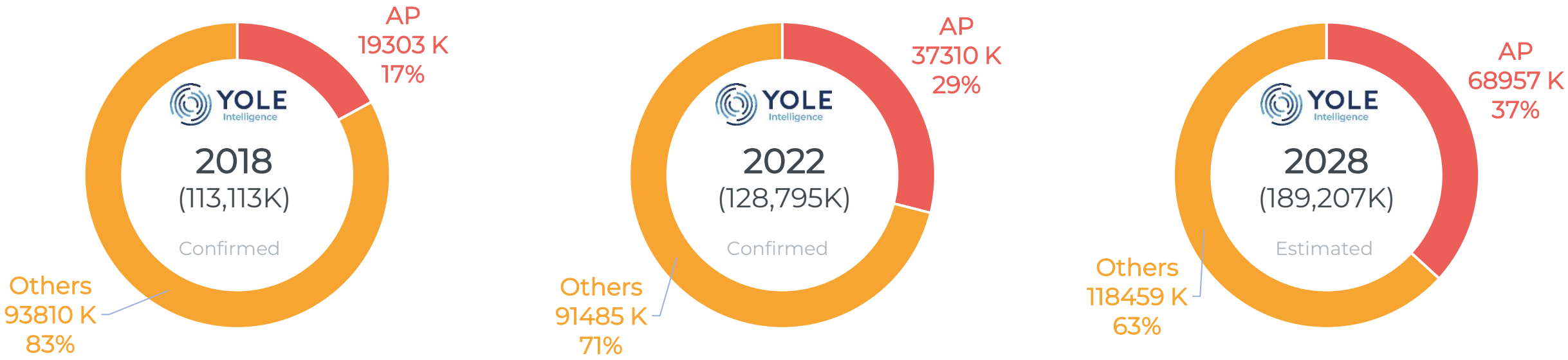
Revenue Split ($B)



- Advanced Packaging revenue is growing at a fast pace, and it is catching up with traditional packaging.
- In 2022, the revenue generated by Advanced Packaging was 47% of the total packaging market. By 2028, Advanced Packaging's revenue will increase to approximately 58% of the total packaging market. This indicates a significant growth in the market share of Advanced Packaging over the next few years.

ADVANCED VS TRADITIONAL TECHNOLOGIES OVERVIEW 2018 to 2028

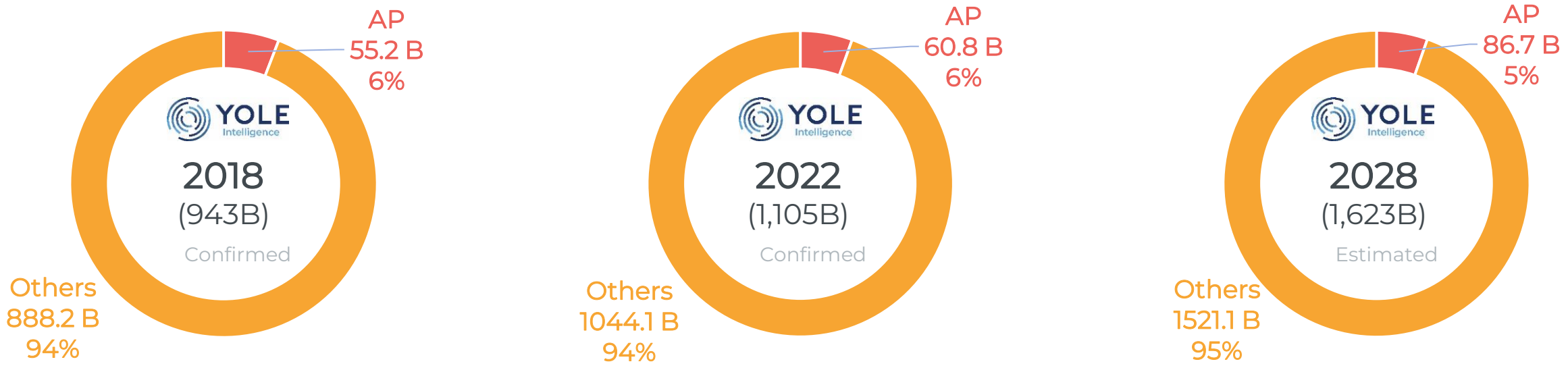
Wafer Split (300mm eq K WSPY)



- In terms of 300mm-eq wafers, traditional packaging still dominates with almost 71% of the total market in 2022. However, Advanced Packaging is continuously increasing its share of wafers, and its market share will increase from ~29% in 2022 to 37% in 2028.
- The value of an AP wafer is almost the double that of a traditional packaging one, resulting in a high-profit margin for the manufacturers. AP wafer growth is propelled by advanced technology adoption in larger package size devices, resulting in increased wafer output.

ADVANCED VS TRADITIONAL TECHNOLOGIES OVERVIEW 2018 to 2028

Unit Split (Bunits)



In terms of units, traditional packaging accounts for more than 90%. This is because small dies are mostly packaged using traditional packaging. So even though traditional packaging constitutes 71% of total wafers, in units, it constitutes ~94% of total chips packaged.

MARKET EVOLUTION OF SEMICONDUCTOR PACKAGING

Advanced Packaging vs Traditional Packaging Forecast (2018-2028)

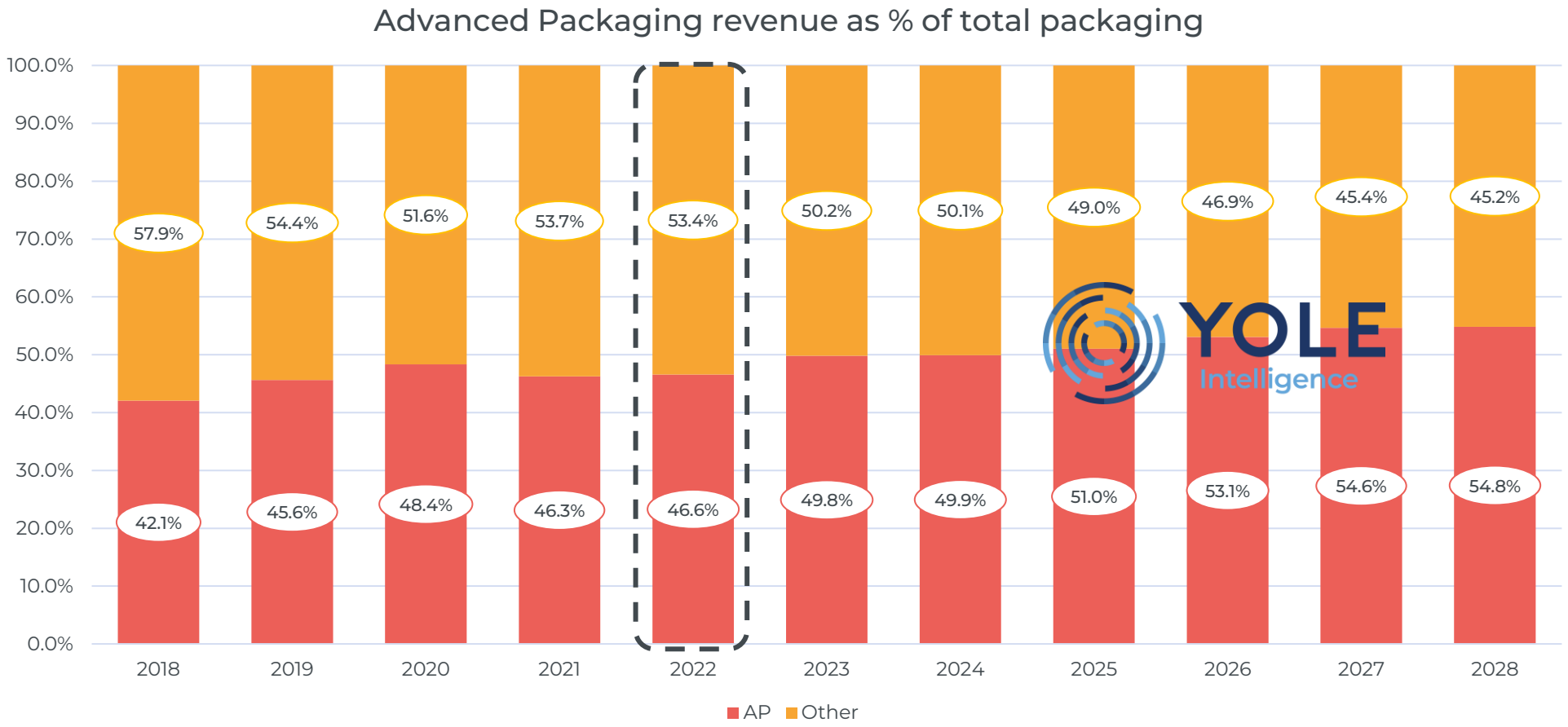
2018-2028, SEMICONDUCTOR PACKAGING, MARKET FORECAST ($B)

	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	CAGR (2022-2028)
AP	$27.6 B	$29.3 B	$35.3 B	$40.3 B	$44.3 B	$46.8 B	$51.9 B	$56.9 B	$64.4 B	$72.8 B	$78.6 B	10.05%
Other	$38.0 B	$34.9 B	$37.7 B	$46.8 B	$50.7 B	$47.2 B	$52.1 B	$54.6 B	$57.0 B	$60.4 B	$64.7 B	4.15%
Total	$65.6 B	$64.1 B	$73.0 B	$87.1 B	$95.0 B	$94.0 B	$104.0 B	$111.5 B	$121.4 B	$133.2 B	$143.3 B	7.10%

The total IC packaging market was worth $95B in 2022. Advanced Packaging (AP) was worth $44.3B and is expected to grow at $CAGR_{2022-2028}$ of 10% to reach $78.6B in 2028. At the same time, the traditional packaging market will grow at a $CAGR_{2022-2028}$ of 4.15%, and the total packaging market will grow at a $CAGR_{2022-2028}$ of 7.1% to $64.7B and $143.3B, respectively.

ADVANCED VS TRADITIONAL PACKAGING MARKET SHARE EVOLUTION 2018-2028

Advanced Packaging revenue will exceed traditional packaging revenue by 2025.



In 2022, the AP market share was ~47%. Due to strong momentum in the AP market driven by megatrends, the percentage of AP in the total semiconductor market is increasing continuously and will reach more than ~51% of the market by 2025.

SEMICONDUCTOR PACKAGING – MARKET FORECAST

YoY Growth Rate (by Revenue) Evolution of AP vs Traditional & Total Packaging Market

AP market is expected to increase by 6% in 2023, while the traditional packaging market will decrease by 8% in the same year.

2018-2028 YoY Growth (%) of Advanced Packaging, Others and Total Semiconductor Packaging Revenue

	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
AP	7%	6%	17%	12%	9%	6%	10%	9%	12%	12%	7%
Other	4%	-9%	8%	19%	8%	-8%	10%	5%	4%	6%	7%
Total	5%	-2%	12%	16%	8%	-1%	10%	7%	8%	9%	7%

The AP market increased by 9% YoY (2021/2022), while the traditional packaging market increased by 8% in the same year.

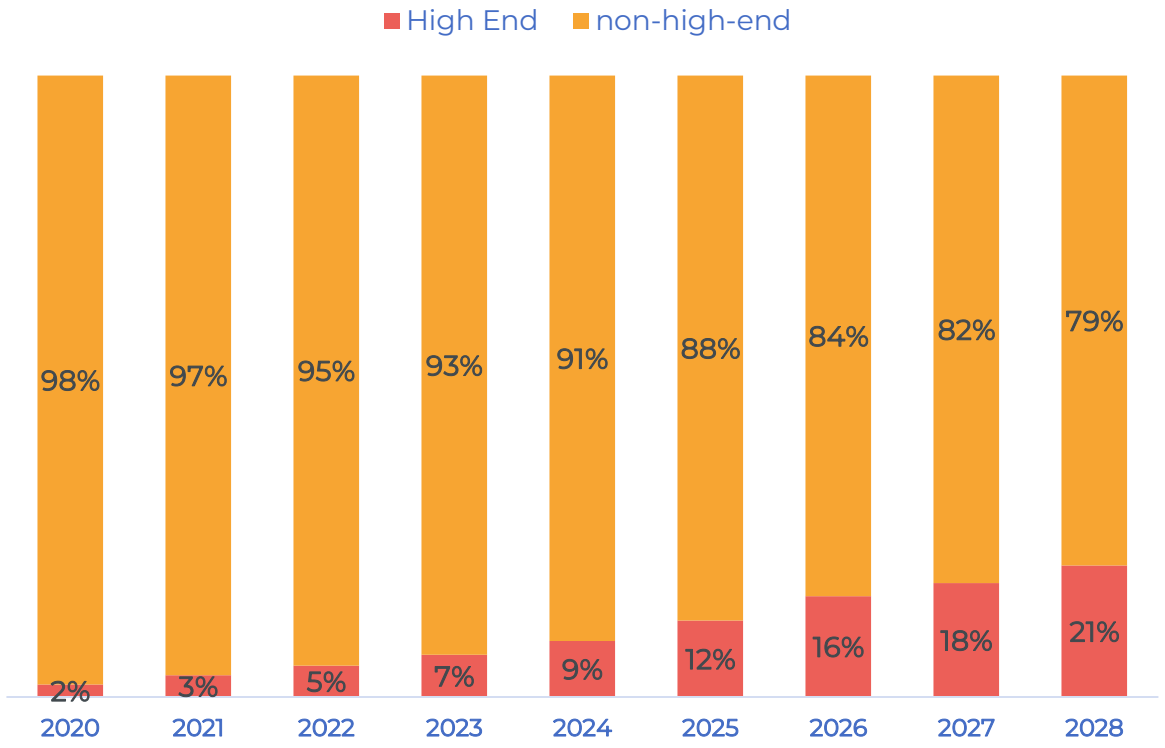
We expect the total assembly & packaging market to decrease by 1% in 2023, with traditional packaging market decreasing by 8%, affected by the overall semiconductor downturn, ongoing inventory digestion, over-capacity and falling prices.

Nevertheless, the AP market is expected to thrive and increase by 6% during this period. Despite the economic downturn affecting the overall semiconductor and packaging markets, AP should benefit from the still steady demand on the AI/HPC and automotive segments. Furthermore, AP market is driven by the adoption of more complex and advanced packaging solutions which present a higher ASP.

ADVANCED PACKAGING VALUE MOVING TOWARDS HIGH-END TECHNOLOGIES

- Although Moore's Law has remained relevant for over five decades, it is no longer cost-efficient for advanced nodes and lesser leading-edge manufacturers can keep up.
- The industry is now diligently utilizing advanced packaging technologies to put multiple advanced and/or matured chips in a single package, also known as heterogeneous integration.
- Coupled with High-end Performance Packaging, the system-level 3D interconnect density (3D ID) trend is not only sustained but accelerates to new highs. This is driven by high-end market segments such as AI, datacenter, supercomputers, data mining, networking, Co-Package Optics and high-end PC and gaming.
- Hereafter, the need for more performance for this market segments is provoking a value transfer towards high-end packaging technologies within the whole advanced packaging market.
- In 2022, high-end performance packaging represented 5% of the total AP market value. **By 2028, high-end packaging is estimated to reach 21% of the total AP market value.**
- The value transfer is due to technology transfer – growing adoption of high-end 2.5D/3D packaging technologies – and to the fact that these technologies allow increased performance, and hence come at a higher cost, contributing to higher revenues.
- Foundries and IDMs – the ones leveraging front-end capabilities – are the ones that are profiting the most from the value transfer. So far on the OSAT ecosystem, only the top ones like ASE, Amkor and JCET, have the capabilities to partner up with foundries and IDMs and actively participate in the high-end packaging supply chain.

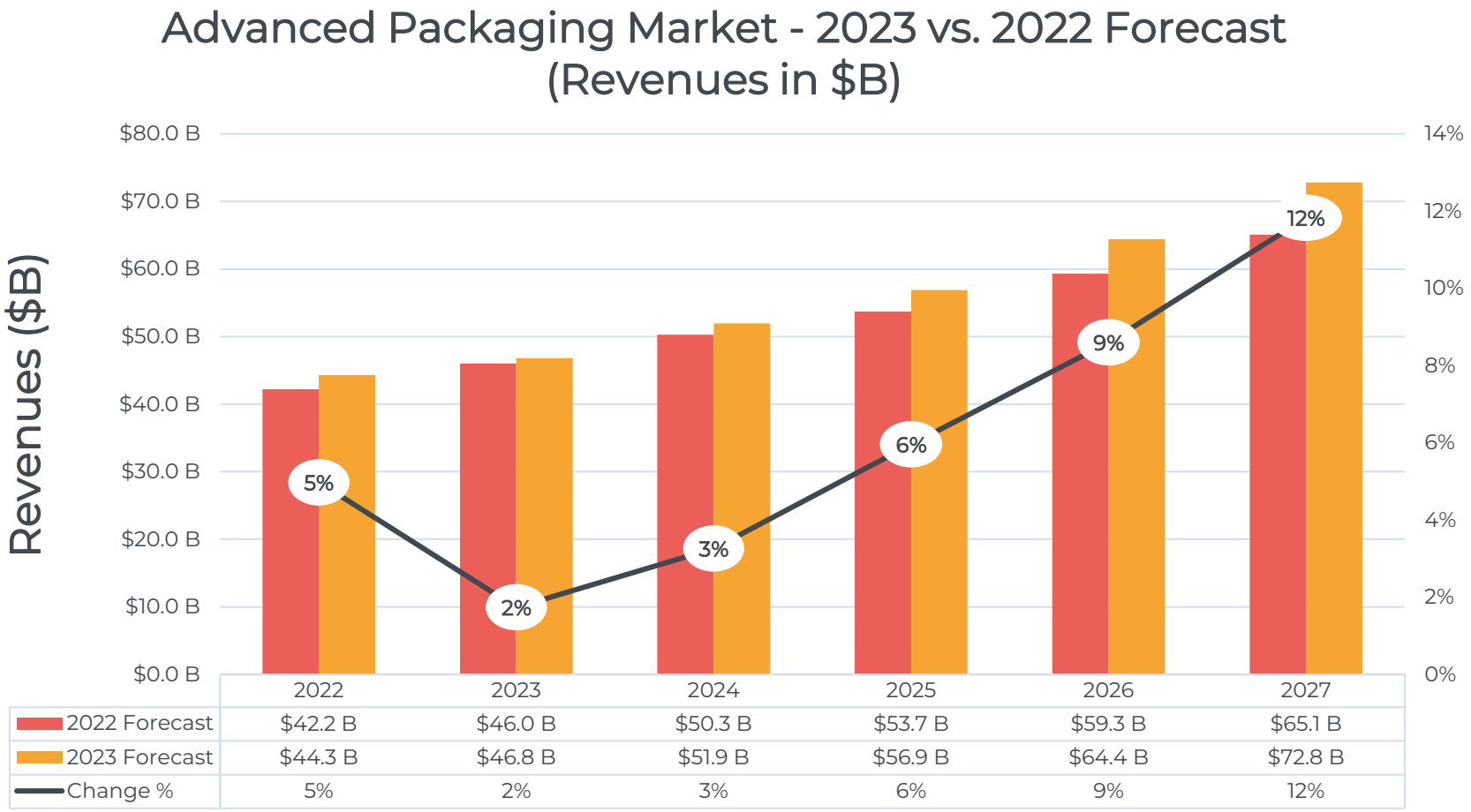
High-end vs. Non High-end Packaging revenues ratio evolution (2020 – 2028)



High-end Performance Packaging is defined by Yole as a forefront packaging technology that adds value to device performance with ***high IO density (≥16/mm²) and fine IO pitch (≤130µm).***
This includes technologies generally defined as 2.5D/3D integration such as UHD FO, Embedded Si bridge, Si Interposer, 3D stacked memories and 3D SoC.

WHAT HAS CHANGED IN THE MARKET FORECAST?

Advanced Packaging market – 2023 vs. 2022 forecast



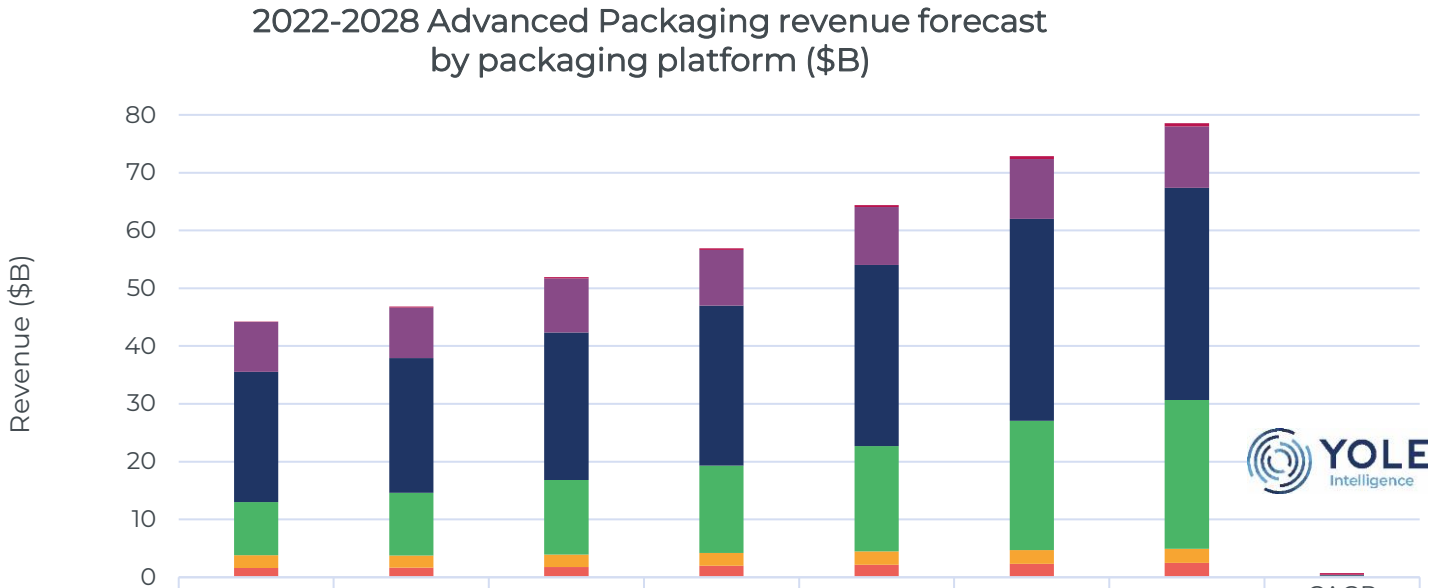
	2022	2023	2024	2025	2026	2027
2022 Forecast	$42.2 B	$46.0 B	$50.3 B	$53.7 B	$59.3 B	$65.1 B
2023 Forecast	$44.3 B	$46.8 B	$51.9 B	$56.9 B	$64.4 B	$72.8 B
Change %	5%	2%	3%	6%	9%	12%

In 2022 and 2023 the demand for consumer electronics has slowed for several end systems.

- Desktop, laptop, and tablet demand are expected to slow down during 2023.
- Smartphone demand has slowed down in 2022. In 2023 smartphone demand is expected to slightly increase but remain flat.
- Demand appears to be softening on data center, HPC and automotive, but growth is still healthy for the coming years. Automotive should remain more resilient with semiconductor shortage expected to ease further.

End-system demand across all AP platforms has been updated to reflect these changes.

ADVANCED PACKAGING REVENUE FORECAST 2023-2028



	2022	2023	2024	2025	2026	2027	2028	CAGR (2022-2028)
ED	0.10	0.15	0.22	0.28	0.36	0.48	0.51	30.40%
SiP	8.63	8.77	9.38	9.62	9.98	10.38	10.66	3.59%
Flip-Chip	22.53	23.28	25.49	27.70	31.35	34.90	36.72	8.48%
2.5D/3D	9.20	10.87	12.90	15.14	18.25	22.38	25.77	18.72%
WLCSP	2.21	2.11	2.16	2.24	2.29	2.38	2.42	1.58%
FO	1.59	1.63	1.77	1.95	2.16	2.33	2.47	7.65%
TOTAL	44.26	46.83	51.92	56.92	64.40	72.84	78.55	10.03%
YoY Growth	10%	6%	11%	10%	13%	13%	8%	

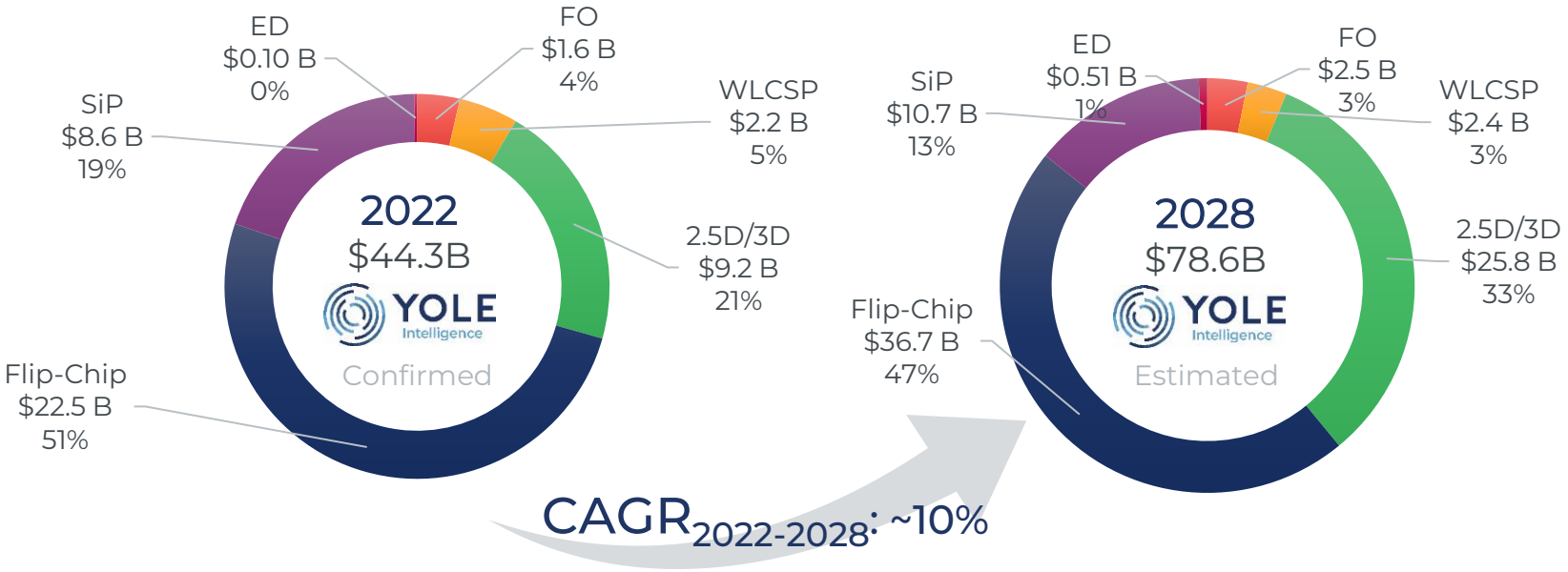
Data source: Advanced Packaging Monitor – Q1 2023

- The Advanced Packaging market was worth ~$44.3B in 2022. It is expected to grow at a ~ 10% $CAGR_{2022-2028}$ to reach ~$78.6B in 2028.
- The market increased by 10% realizing a strong growth in 2022, still driven by the aggressive post-pandemic semiconductor demand.
- We expect the post-2022 global semiconductor demand will normalize in 2023 with a slight decline. The world political conflicts, the geopolitical tensions, and increased inflation scenarios faced in 2022 and early 2023 will have a negative influence on the semiconductor market in 2023.
- Although the packaging market is expected to be affected by the overall semiconductor market decline, the demand for Advanced Packaging will continue to increase as its importance and complexity keep increasing for the advanced device nodes and complex form factors. Nevertheless, AP market growth will be softer in 2023 compared to the previous year.

* Flip-Chip includes: FCCSP and FCBGA. It includes bumping, assembly and materials revenues.

ADVANCED PACKAGING REVENUE FORECAST 2023-2028

BREAKDOWN BY TECHNOLOGY



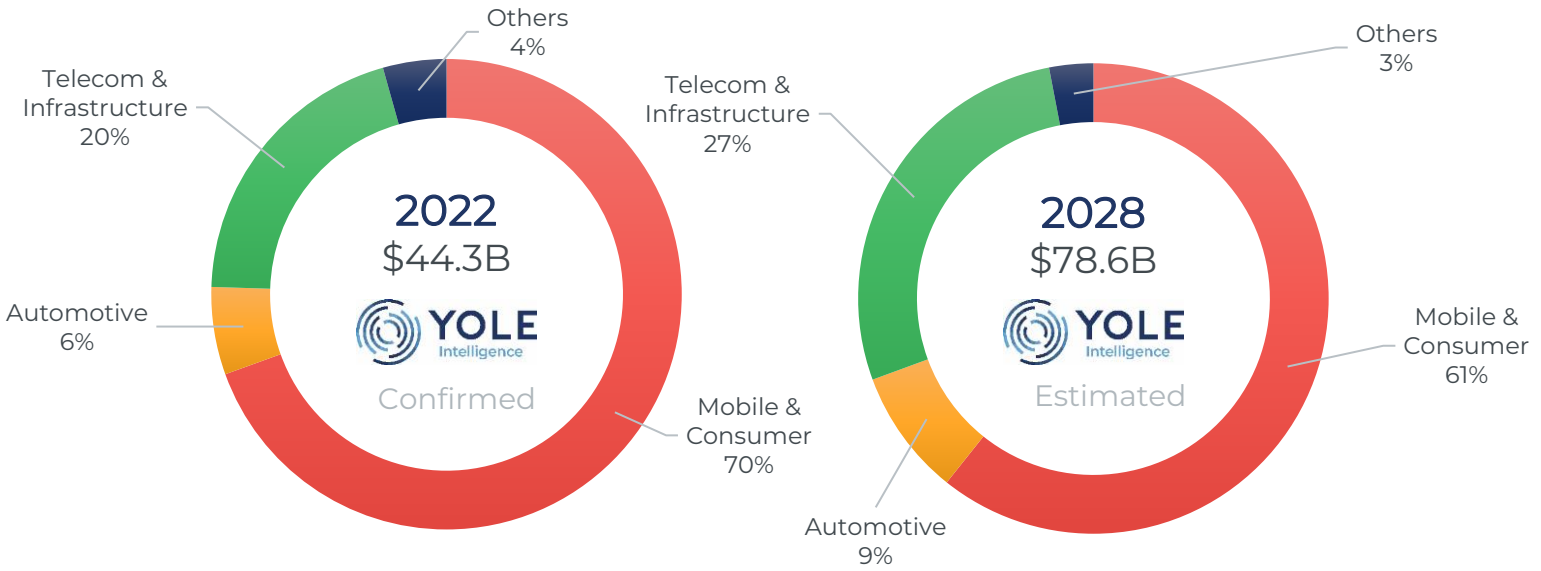
Flip-chip	$CAGR_{2022\text{-}2028}$ ~ 8.5%
SiP	$CAGR_{2022\text{-}2028}$ ~ 3.6%
Fan-out	$CAGR_{2022\text{-}2028}$ ~ 7.6%
Fan-in WLP	$CAGR_{2022\text{-}2028}$ ~ 1.6%
2.5D/3D	$CAGR_{2022\text{-}2028}$ ~ 18.7%
Embedded Die	$CAGR_{2022\text{-}2028}$ ~ 30.4%

* Flip-Chip includes: FCCSP and FCBGA. It includes bumping, assembly and materials revenues.

- The Flip-Chip platform (includes FCBGA and FCCSP) has the highest market share, with 51% of the market in 2022.
- Highest growth $CAGR_{2022\text{-}2028}$ is expected from ED (in laminate substrate), 2.5D/3D, and flip-chip at 30%, 18.7%, and 9%, respectively, as high-volume products further penetrate the market:
  - FO in mobile, networking, HPC, and automotive.
  - 2.5D/3D in AI/ML, HPC, data centers, CIS, 3D NAND, MEMS/sensors.
  - ED in automotive, mobile, and medical end markets.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING REVENUE FORECAST
BREAKDOWN BY MARKET



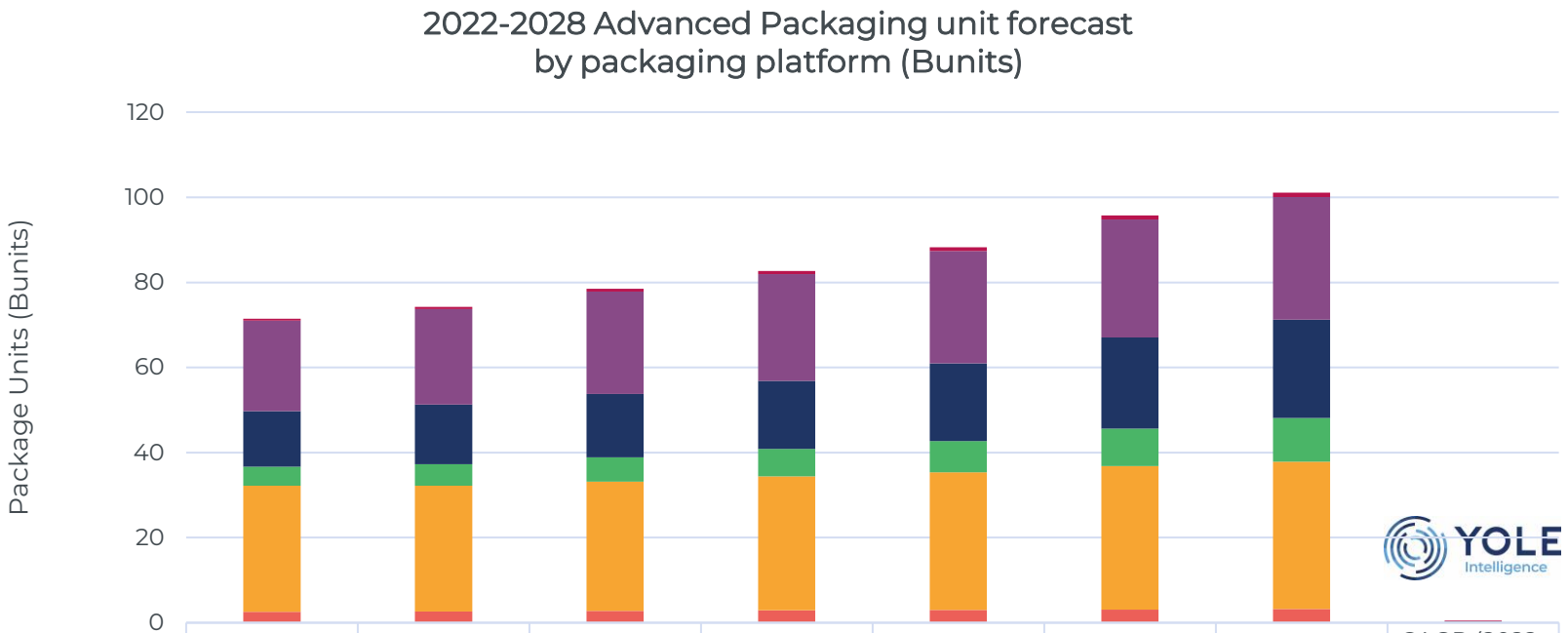
Mobile & Consumer	$CAGR_{2022\text{-}2028}$ ~ 7%
Automotive & Transportation	$CAGR_{2022\text{-}2028}$ ~ 10%
Telecom & Infrastructure	$CAGR_{2022\text{-}2028}$ ~ 17%
Others*	$CAGR_{2022\text{-}2028}$ ~ 10%

* Others include medical, industrial, & aerospace/defense segments

- The Mobile & Consumer segment constituted 70% of the total Advanced Packaging market by revenue in 2022. It will grow with an 8% CAGR and constitute 61% of the Advanced Packaging revenue by 2028. This market will be driven by increased silicon content in mobile and consumer devices and the need for more complex packaging technology due to 5G growth and more stringent system performance requirements.
- Telecom & Infrastructure is the fastest-growing segment (CAGR ~17%) in the Advanced Packaging market by revenue and will account for 27% of the market in 2028. This is driven by 5G deployment and the thriving of HPC/AI applications, with more demanding requirements at the system and package level.
- Automotive & transportation will account for 9%, and its growth will be driven by vehicle electrification, and hence the increased silicon content inside vehicles and the need for more advanced packaging solutions in ADAS, radar, infotainment and overall automotive computing systems.
- Other segments, including medical, industrial, and aerospace/defense, will account for 3% of the market.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING UNIT FORECAST 2023-2028



	2022	2023	2024	2025	2026	2027	2028	CAGR (2022-2028)
ED	0.4	0.5	0.7	0.8	0.9	1.0	1.1	16.41%
SiP	21.2	22.5	24.1	25.1	26.4	27.7	28.8	5.24%
*Flip-Chip	13.1	14.0	14.9	16.0	18.3	21.4	23.1	9.95%
2.5D/3D	4.5	5.1	5.7	6.4	7.3	8.8	10.3	14.76%
WLCSP	29.6	29.6	30.4	31.5	32.4	33.7	34.6	2.62%
FO	2.5	2.6	2.8	2.9	3.0	3.1	3.2	3.89%
TOTAL	71.4	74.3	78.5	82.7	88.2	95.8	101.1	5.97%
YoY Growth	0.3%	4%	6%	5%	7%	9%	6%	

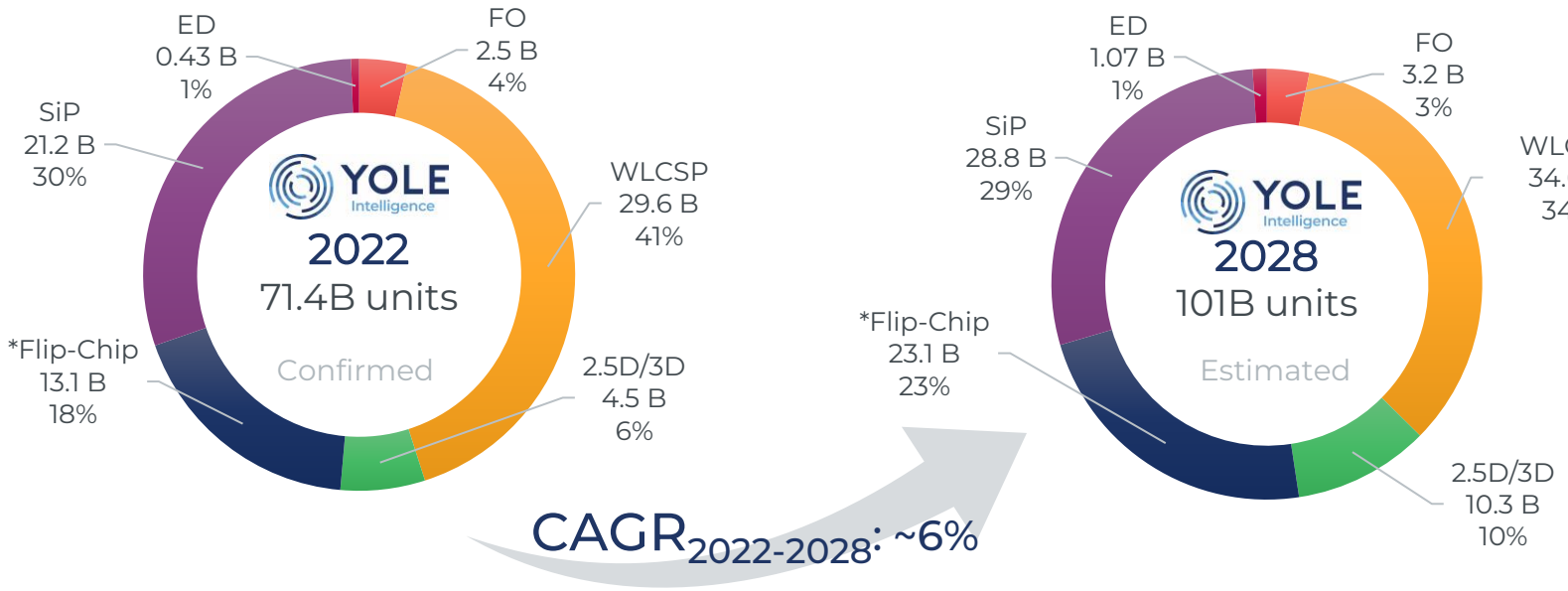
* Flip-Chip includes: FCCSP and FCBGA.

- Advanced Packaging shipments will increase at a ~6% $CAGR_{2022-2028}$ to reach 101.1B units in 2028.
- Concerning unit count, WLCSP packages will remain dominant.
- 2.5D/3D packages will grow at a ~ 15% CAGR to reach ~ 10.3B in 2028. Growth in units is driven by 3D memory, Si interposer, 3D NAND, SoC, and CIS.
- ED package share is ~1% of the total AP shipments. However, it will grow at 16.4% $CAGR_{2022-2028}$ to reach ~ 1.07B by 2028. This growth will be led by increased adoption in mobile (e.g., envelope tracker), automotive & base stations.
- Fan-out package units will grow with a 3.9% CAGR from 2022 to 2028 to 3.2B units in 2028.
- Flip-chip packages (FCBGA and FCCSP) will grow at a CAGR of ~ 10% to reach ~23.1B units in 2028.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING UNIT FORECAST 2023-2028

BREAKDOWN BY TECHNOLOGY



Flip-chip	$CAGR_{2022-2028}$ ~ 10%
SiP	$CAGR_{2022-2028}$ ~ 5.2%
Fan-out	$CAGR_{2022-2028}$ ~ 3.9%
Fan-in WLP	$CAGR_{2022-2028}$ ~ 2.6%
2.5D/3D	$CAGR_{2022-2028}$ ~ 14.8%
Embedded Die	$CAGR_{2022-2028}$ ~ 16.4%

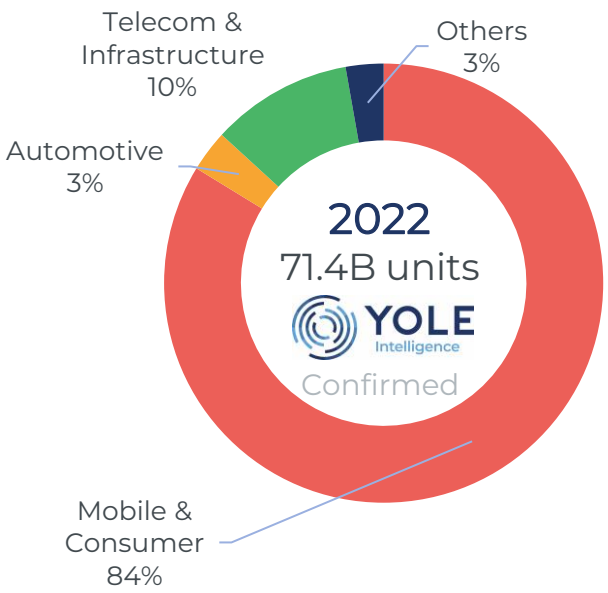
* Flip-Chip includes: FCCSP, FCBGA

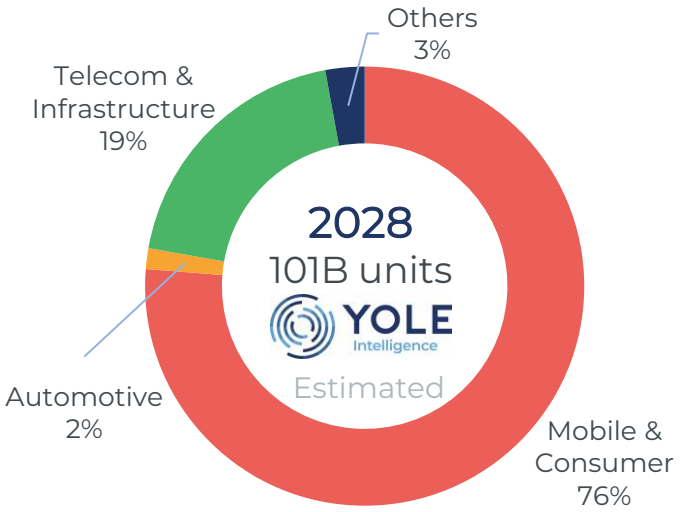
- The number of fan-in WLP packages will increase by ~ 2.6% CAGR until 2028 to reach ~34.6B units. However, its share of total Advanced Packaging shipments will decrease from 41% in 2022 to 34% in 2028. This is mainly attributed to the relatively slow growth rate of the mobile segments, where fan-in WLP has the major share.
- 2.5D/3D package shipments will increase by ~15% CAGR until 2028 to ~10.3B units.
- ED package share is ~1% of the total AP shipments. However, it will grow at 16% $CAGR_{2022-2028}$ to reach ~1.07B by 2028. The growth will be led by increased adoption in mobile (e.g., envelope tracker), automotive & base stations.
- Fan-out package units will grow by ~ 4% CAGR from 2022 to 2028 to 3.2B units.
- Flip-chip packages (FCBGA and FCCSP) will grow at a CAGR of ~10% to reach ~23.1B units in 2028.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING UNIT FORECAST: BREAKDOWN BY MARKET

BREAKDOWN BY MARKET





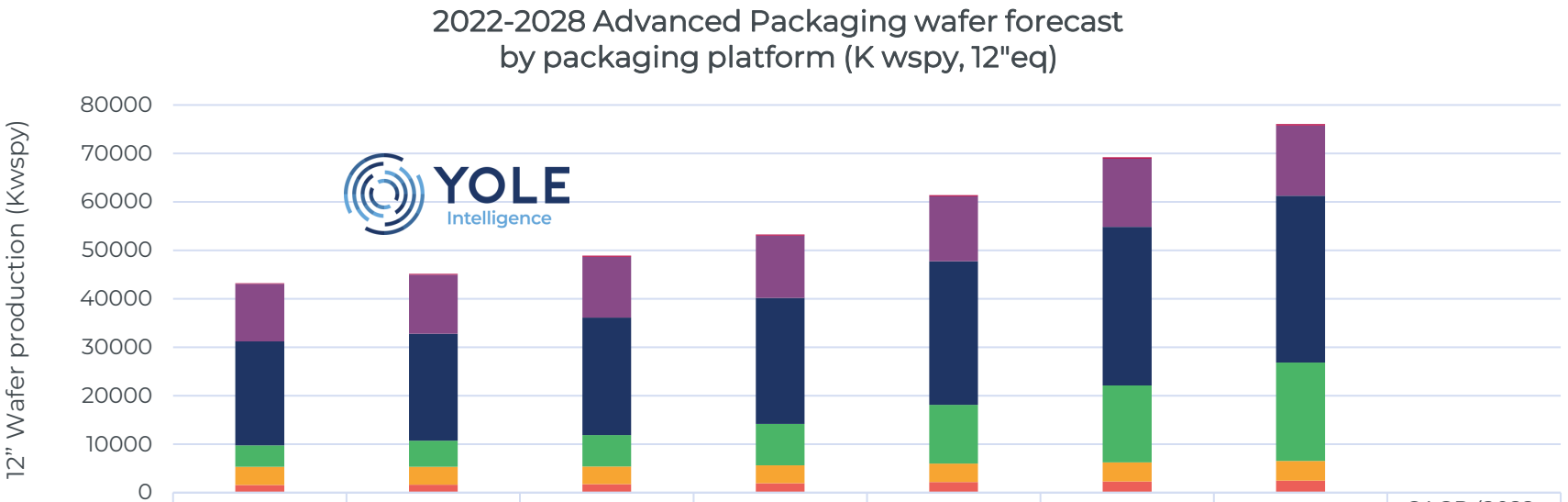
Mobile & Consumer	$CAGR_{2022-2028}$ ~ 4%
Automotive & Transportation	$CAGR_{2022-2028}$ ~ 11%
Telecom & Infrastructure	$CAGR_{2022-2028}$ ~ 24%
Others*	$CAGR_{2022-2028}$ ~ 11%

* Others include medical, industrial, & aerospace/defense segments

- The Mobile & Consumer segment constituted 84% of the Advanced Packaging units shipped in 2022. These will have a 4% CAGR and constitute 76% of the Advanced Packaging units by 2028.
- Telecom & Infrastructure is the fastest-growing segment in the Advanced Packaging market by units and will double its market share from 10% in 2022 to 19% by 2028.
- In terms of package units, the Automotive & Transportation market will decrease its share to 2% in 2028, however the market will growth will a healthy 11% CAGR.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING WAFER FORECAST 2023-2028



	2022	2023	2024	2025	2026	2027	2028	CAGR (2022-2028)
ED	134	167	209	234	267	308	332	16.41%
SiP	11890	12174	12562	12856	13368	14017	14481	3.34%
*Flip-Chip	21420	22010	24191	25958	29603	32750	34364	8.20%
2.5D/3D	4423	5436	6488	8546	12108	15841	20329	28.94%
WLCSP	3782	3692	3661	3739	3842	3914	4052	1.15%
FO	1572	1635	1762	1933	2183	2341	2491	7.98%
TOTAL	43220	45114	48872	53265	61371	69170	76050	9.88%
YoY Growth	6%	4%	8%	9%	15%	13%	10%	

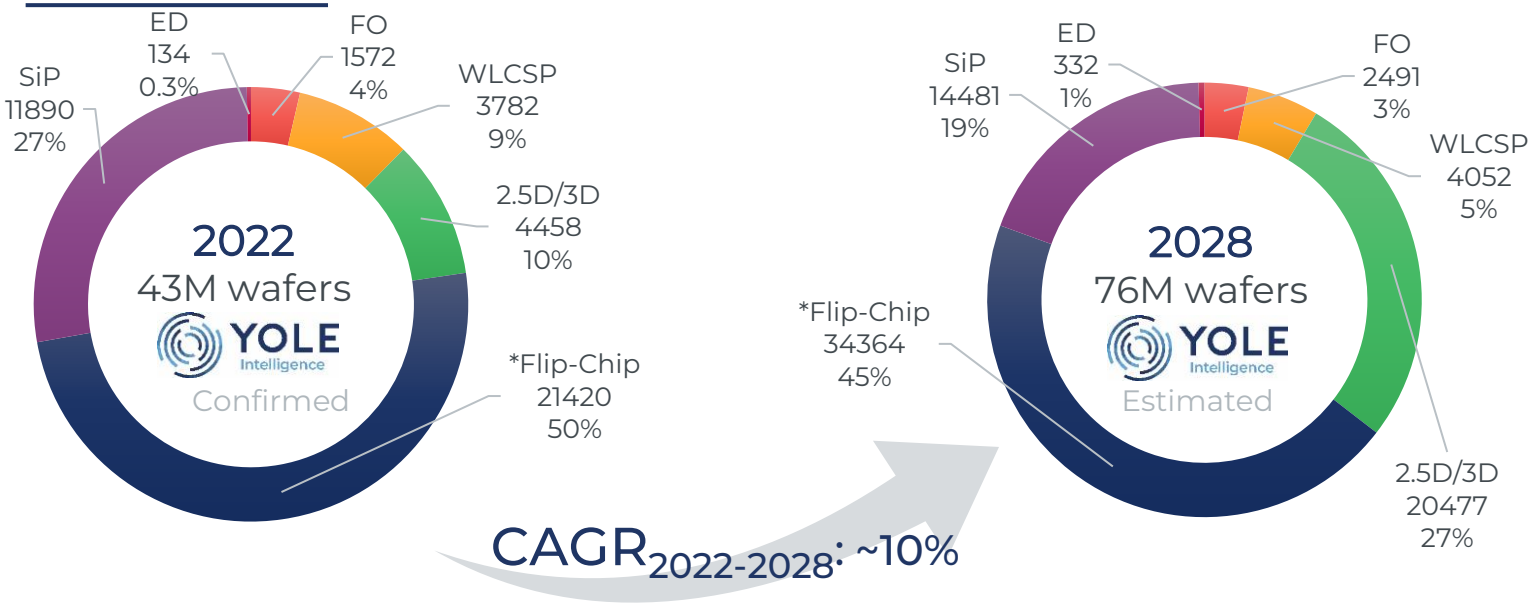
- Advanced Packaging wafer production reached ~43M 12" wafers in 2022. It is expected to grow at a ~10% $CAGR_{2022-2028}$ to reach ~76M wafers in 2028.
- Highest wafer CAGR remains with 2.5D/3D (29%), ED (16.4%), and flip-chip (8.2%).
- ED's share of AP wafers is low (1%), but it'll grow at an impressive CAGR of 16.4% from 2022 to 2028 to reach ~332K wafers.
- Growth areas for:
  - FO in mobile, networking, HPC, and automotive.
  - 2.5/3D in AI/ML, HPC, data centers, CIS, 3D NAND.
  - ED in automotive, mobile, and 5G base stations.

Data source: Advanced Packaging Monitor – Q1 2023

* Flip-Chip includes: FCCSP and FCBGA. It includes bumping, assembly and materials revenues.

ADVANCED PACKAGING WAFER FORECAST 2023-2028

BREAKDOWN BY TECHNOLOGY



Flip-chip	$CAGR_{2022-2028}$ ~ 8.2%
SiP	$CAGR_{2022-2028}$ ~ 3.3%
Fan-out	$CAGR_{2022-2028}$ ~ 8%
Fan-in WLP	$CAGR_{2022-2028}$ ~ 1.2%
2.5D/3D	$CAGR_{2022-2028}$ ~ 29%
Embedded Die	$CAGR_{2022-2028}$ ~ 16.4%

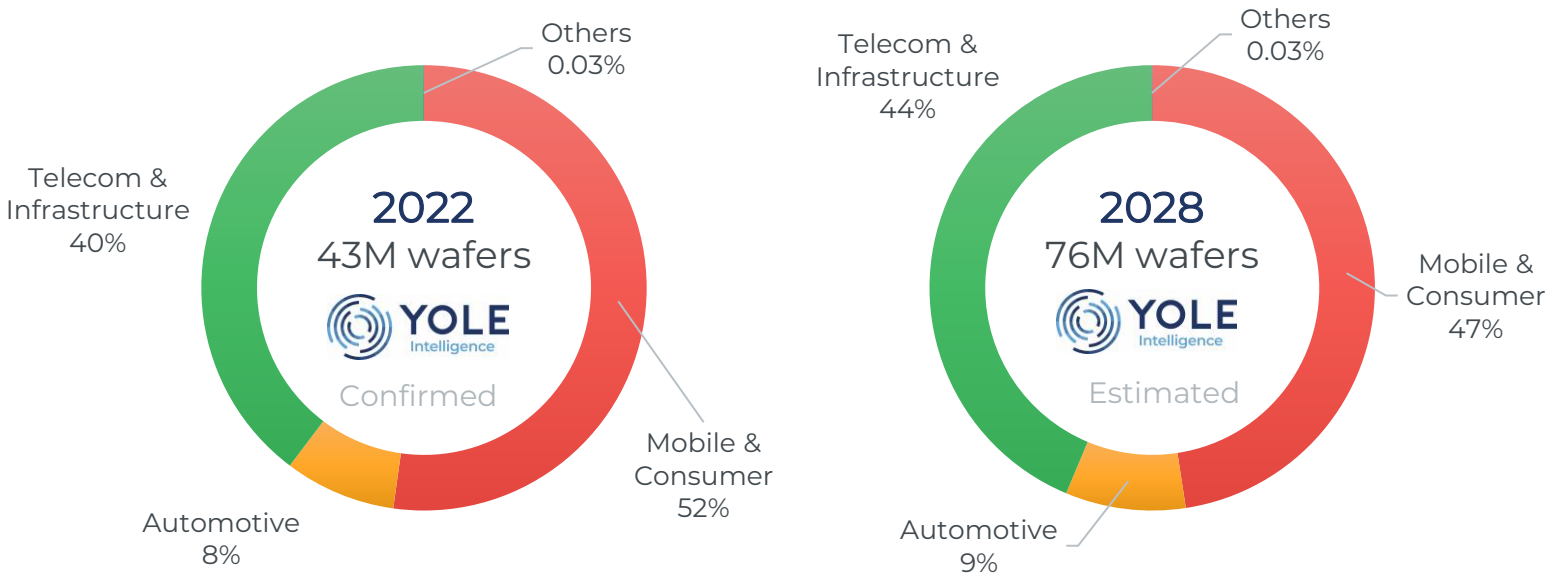
* Flip-Chip includes: FCCSP and FCBGA

- Concerning wafer starts, 2.5D/3D package wafer starts will increase by 29% CAGR until 2028 compared to 2022 to reach ~20M wafers. This is mainly attributed to the high demand for 3D memory, 3D NAND, Si interposer, and 3D SoC, driven by HPC and networking applications & CIS growth due to an increase in the number of smartphone cameras.
- ED's package share is < 1% of the total AP wafers. However, it will grow at 16.4% $CAGR_{2022-2028}$ to reach ~ 332K by 2028. The growth will be led by increased adoption in mobile (e.g., envelope tracker), automotive & base stations.
- Flip-chip technology presents the largest wafer production share (50% in 2022), and it will grow at a CAGR of ~8.2% to reach ~41.6M wafers in 2028, representing 45% of the total AP wafers.
- Fan-Out wafer production will grow 4% to reach ~2.4M in 2028.
- The number of fan-in WLP wafers will increase by 1.2% by 2028 compared to 2022 to reach almost 4M wafers. Its share of total Advanced Packaging shipments will decrease from 9% in 2022 to 5% in 2028. This is mainly attributed to the relatively slow growth rate of the mobile segments, where fan-in WLP has the major share.

Data source: Advanced Packaging Monitor – Q1 2023

ADVANCED PACKAGING WAFER **2023 - 2028** FORECAST

BREAKDOWN BY MARKET



Mobile & Consumer	$CAGR_{2022-2028}$ ~ 7%
Automotive & Transportation	$CAGR_{2022-2028}$ ~ 10%
Telecom & Infrastructure	$CAGR_{2022-2028}$ ~ 17%
Others*	$CAGR_{2022-2028}$ ~ 10%

* Others include medical, industrial, & aerospace/defense segments

- In wafer starts, Mobile & Consumer constituted 52% of the Advanced Packaging units shipped in 2022. It will have at 7% CAGR and constitute 47% of the Advanced Packaging units by 2028.
- Telecom & Infrastructure will grow at 10% CAGR and account for 44% of Advanced Packaging wafer starts in 2028.
- In terms of wafer starts, the Automotive & Transportation segment will increase its share from 8% to 9% by 2028.

PACKAGE ASP BY TECHNOLOGY

Package Technology	2022 ASP/mm² [$/mm²]
UHD FO	0.0787
HD FO	0.0218
Core FO	0.0087
WLCSP (8" wafer)	0.0060
WLCSP (12" wafer)	0.0057
FC CSP (APU)	0.0100
FC CSP (RF)	0.0140
FC CSP (Baseband)	0.0070
FC CSP (PMIC)	0.0150
FC CSP (Memory)	0.0090
FC BGA (Computing)	0.0380
FC BGA (Server)	0.0150
FC BGA (Others)	0.0400
HBM	0.1500
3DS	0.0600
3D NAND Stack	0.0300
3D SoC	0.0700
Si Interposer	0.0500
Active Si Interposer	0.1100
EMIB	0.0700
Co-EMIB	0.07 (EMIB) – 0.11 (Foveros)

ASP = Average Selling Price

Packaging platforms include the cost of the materials and process steps such as: *Bumping, Assembly, RDL, TSV, bonding, IC substrate, integration processing like back grinding, die singulations, etc.*, meaning these are generally included in the ASP.
Front-end die ASP and final package testing ASP is not included.

An average gross margin is considered in the ASP for each type of packaging platform.

2.5D & 3D packaging technologies are generally more expensive than other solutions as they require more complex processes.

Advanced Packaging Platforms Summary

ADVANCED PACKAGING PLATFORMS*

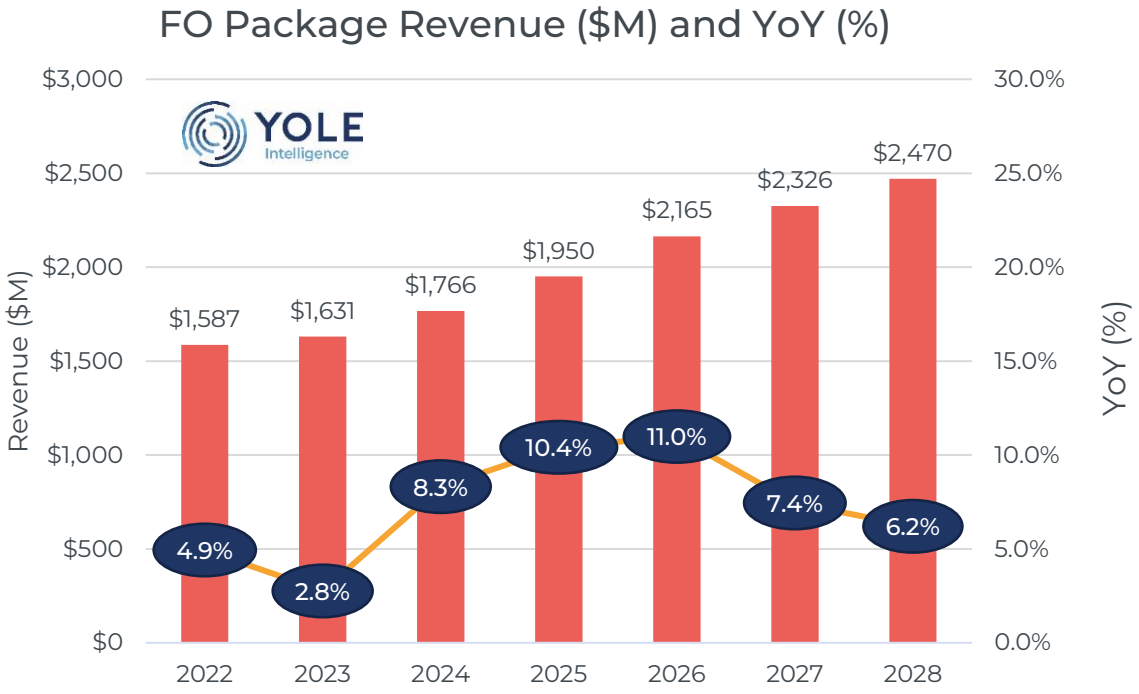
Fan-Out Packaging	WLCSP Fan-In Packaging	System-in-Package (SiP)	FCBGA Packaging	FCCSP Packaging	2.5D/3D Stacked Packaging

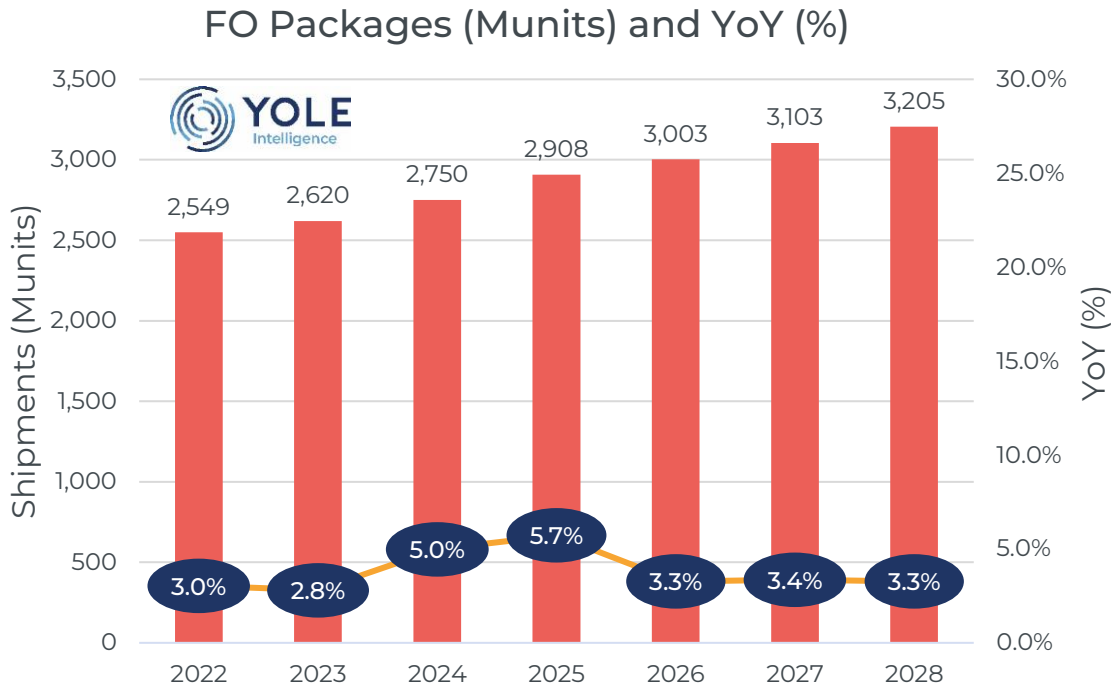
• Core FO
• HD FO
• UHD FO
  • Multi-die
	• Fan-In	• FC + WB
		  • Mainly RFs
		  • Multi-die
		  • IC Substrate
		• FC
		  • Mainly RFs
		  • Multi-die
		  • IC Substrate
		Some of the SiPs are also included in FO/2.5D/3D/BGA. Did not include those in this module to prevent oversizing the market.
			• FC of BGA
			  • Multi-die
			  • IC Substrate
			Si interposer excluded in this module. Si interposer is accounted for in Module 2.5D/3D stacking packaging.
				• FC of CSP
				  • Multi-die
				  • IC Substrate
					• CIS
					• 3D NAND
					• 3D SoC
					• Embedded Si Bridge
					• Active/Passive Si Interposer
					• 3DS
					• HBM

Packaging platforms*: Assembly, Bumping, RDL, TSV, bonding, integration processing like back grinding, die singulations, etc. are generally included in market sizing.
IC Substrate is not generally included in market sizing unless otherwise stated.
Die ASP and final package testing ASP are not included in market sizing

Source: Yole Intelligence,
Advanced Packaging Market Monitor Q1 2023

FAN-OUT PACKAGE GROWTH

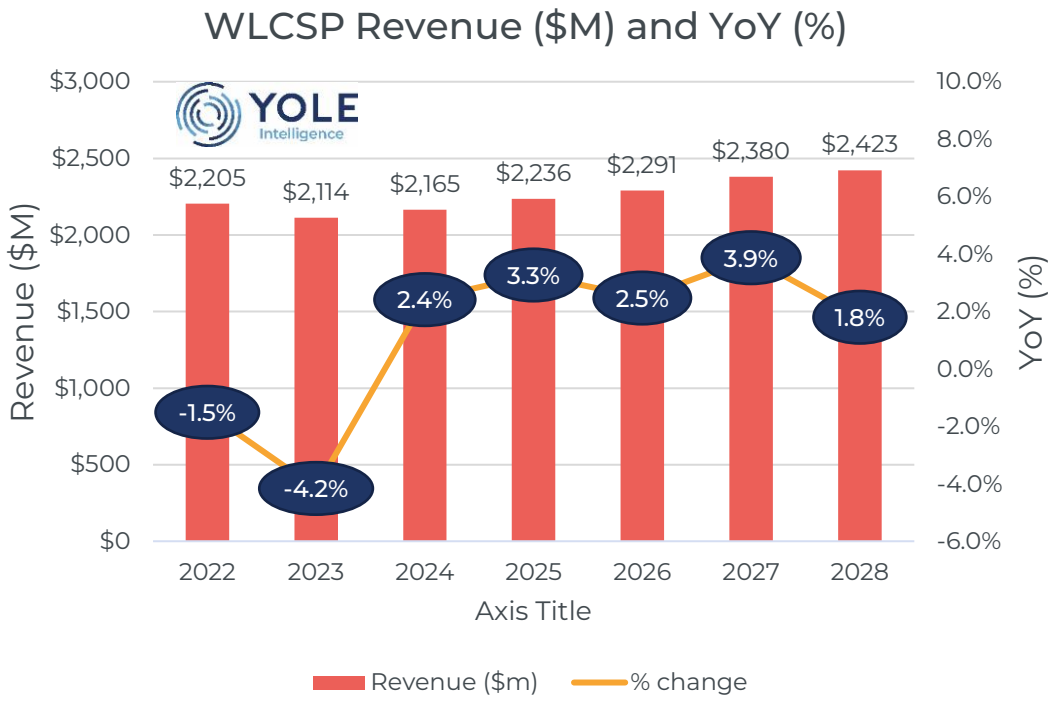


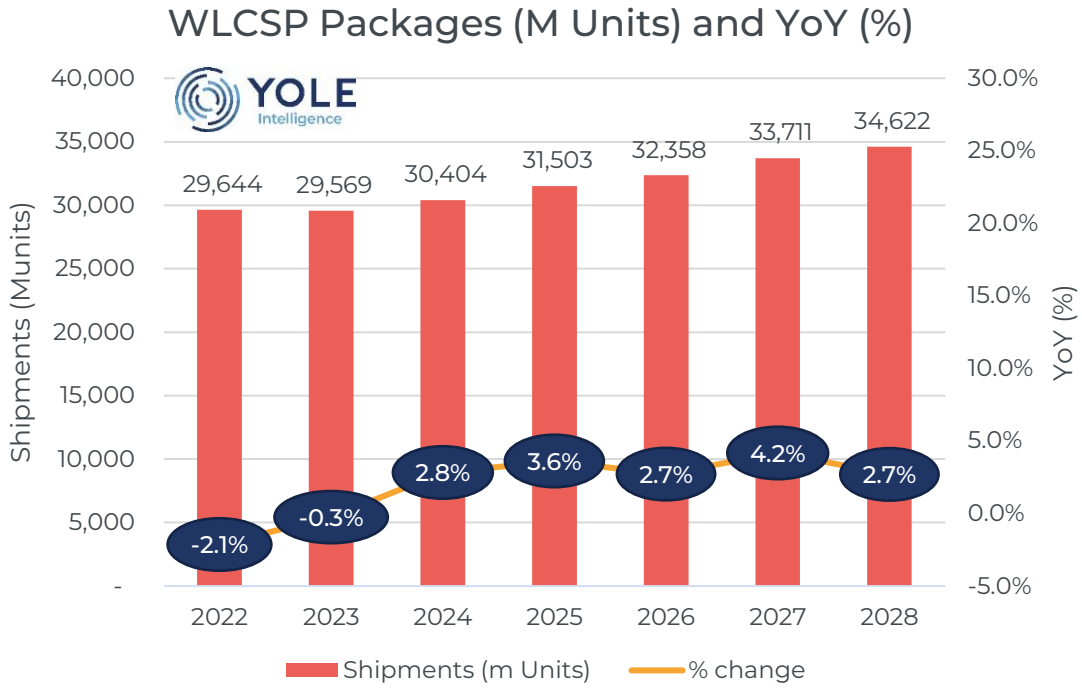


Fan-Out revenue forecast is lower than last year forecast due to the exclusion of IC substrate and flip-chip assembly from fan-out on substrate packages' ASP, which are now reported under the FCBGA market forecast. The slowdown in demand for smartphones and consumer electronics has also affected the decrease in units. However, the fan-out market has sustained a healthy 4.9% growth in 2022 and is expected to grow 2.8% in 2023.
The expected revenue for fan-out package is $1.6B in 2022 and is set to grow with a CAGR of 8% to $2.5B in 2028, with a growth of 3.9% in package units over the next five years.
FOPLP technology is driven mainly by Samsung Electronics, PTI, Nepes, and ASE/Deca Technologies, with the FOPLP market reaching $41M in 2022 and set to grow at a 31% CAGR to reach $208M over the next five years. The primary platform for PLP adoption is Core-FO, while HD-FO and UHD-FO adoption will grow in the future – with UHD-FOPLP adoption expected to be driven mainly by prominent packaging trends and the cost-benefit. However, after many years of development, large panel processing still presents technical challenges and a lack of sufficient demand to achieve the desired cost benefit. Although there are emerging companies investing in FOPLP, its mainstream production has not taken off yet.

Source: Yole Intelligence - Advanced Packaging Market Monitor Q1 2023

WLCSP PACKAGE GROWTH



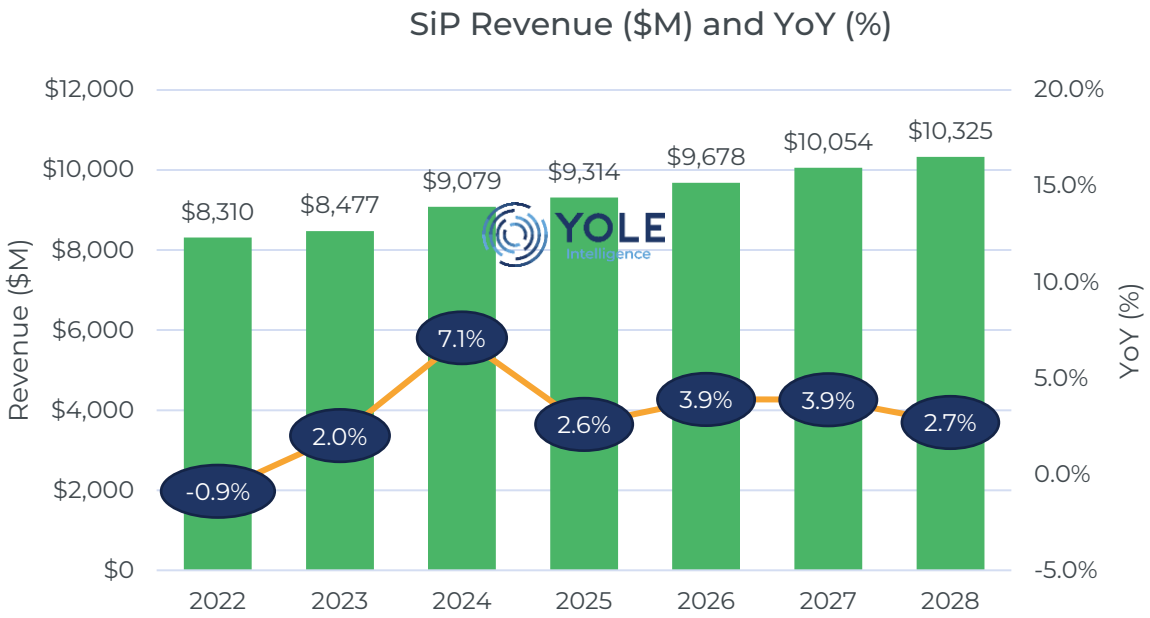


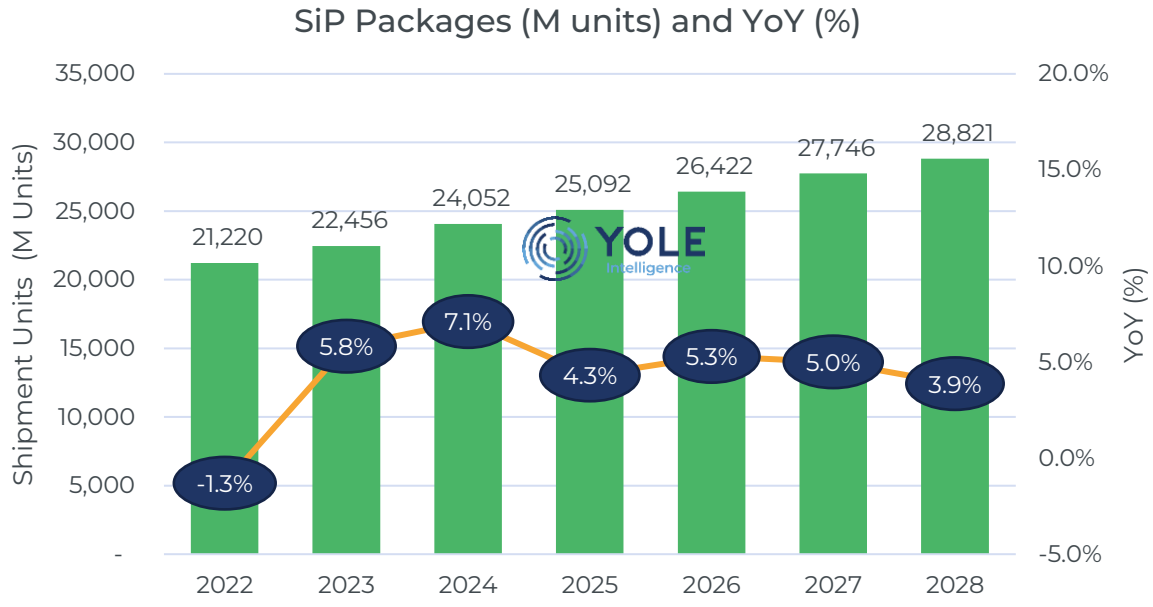
- The WLCSP market is experiencing softness in demand due to the slowdown in the consumer electronics market and the macroeconomic situation. The first half of 2023 is expected to remain weak, while Q3 2023 and Q4 2023 are expected to see growth momentum.

- In 2022, WLCSP revenue and package units decreased, but revenue is expected to grow at a CAGR of 1.6% to reach $2.4B in 2028, with package units expected to grow at a CAGR of 2.6% to reach 34.6 B units in 2028. In 2023, demand is expected to remain weak and shipments flat, with a decrease in revenue and units due to the softness of the mobile and consumer market.
- However, from 2023 onwards, the ASP is expected to decrease with technology maturity.

Source: Yole Intelligence - Advanced Packaging Market Monitor Q1 2023

SIP PACKAGE GROWTH



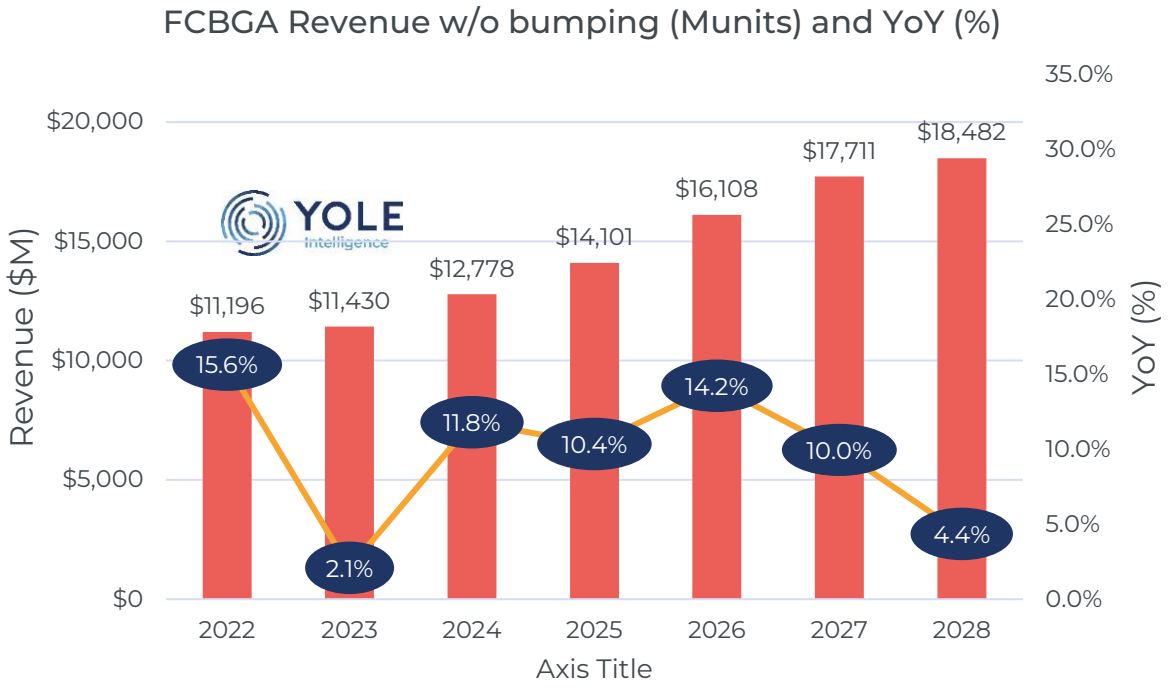


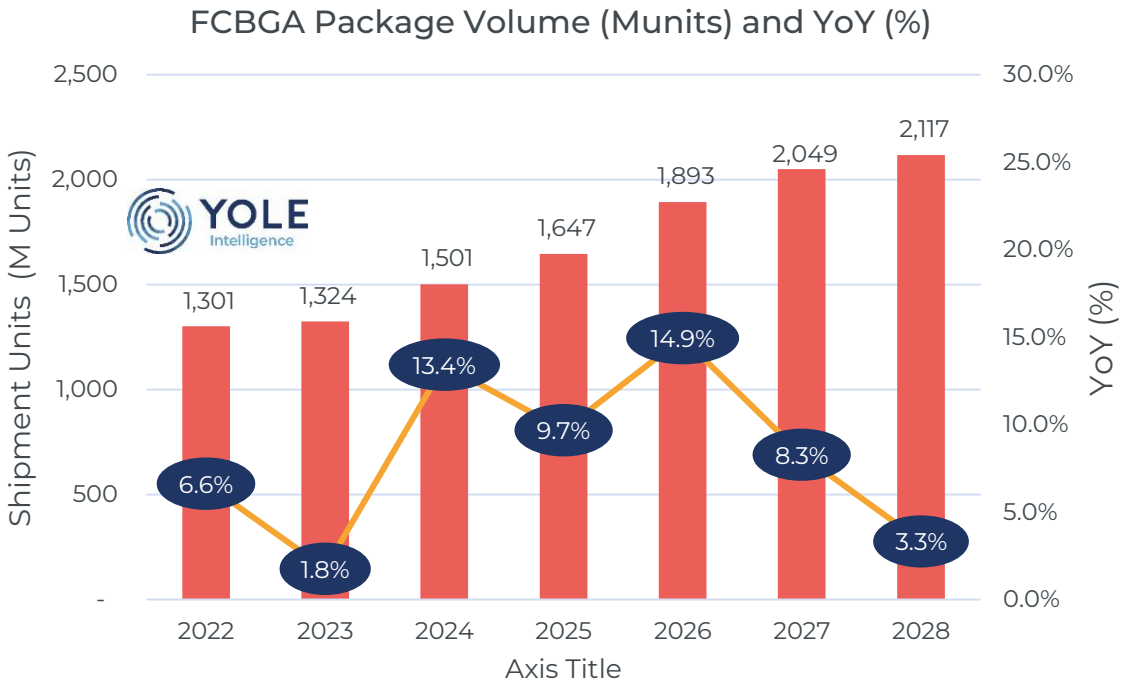
- In 2023, the SiP market is expected to face weak demand in the first half due to macroeconomic conditions, leading to lower package supplier utilization. However, the market is anticipated to recover in the second half. The SiP market is expected to grow at a 3.7% CAGR from 2022 to 2028, driven by the mobile and consumer market, dominated by 5G, RF connectivity, MEMS, and sensors. Amkor and ASE are the leading SiP suppliers, with other OSATs and IDMs taking significant market shares.

- Handset systems accounted for 80% of SiP package units in 2022, with RF connectivity modules being the most significant component type. The ability to package RF SiP quickly will be crucial for suppliers to break out and propel RF SiP growth.

Source: Yole Intelligence - Advanced Packaging Market Monitor Q1 2023

FCBGA PACKAGE GROWTH

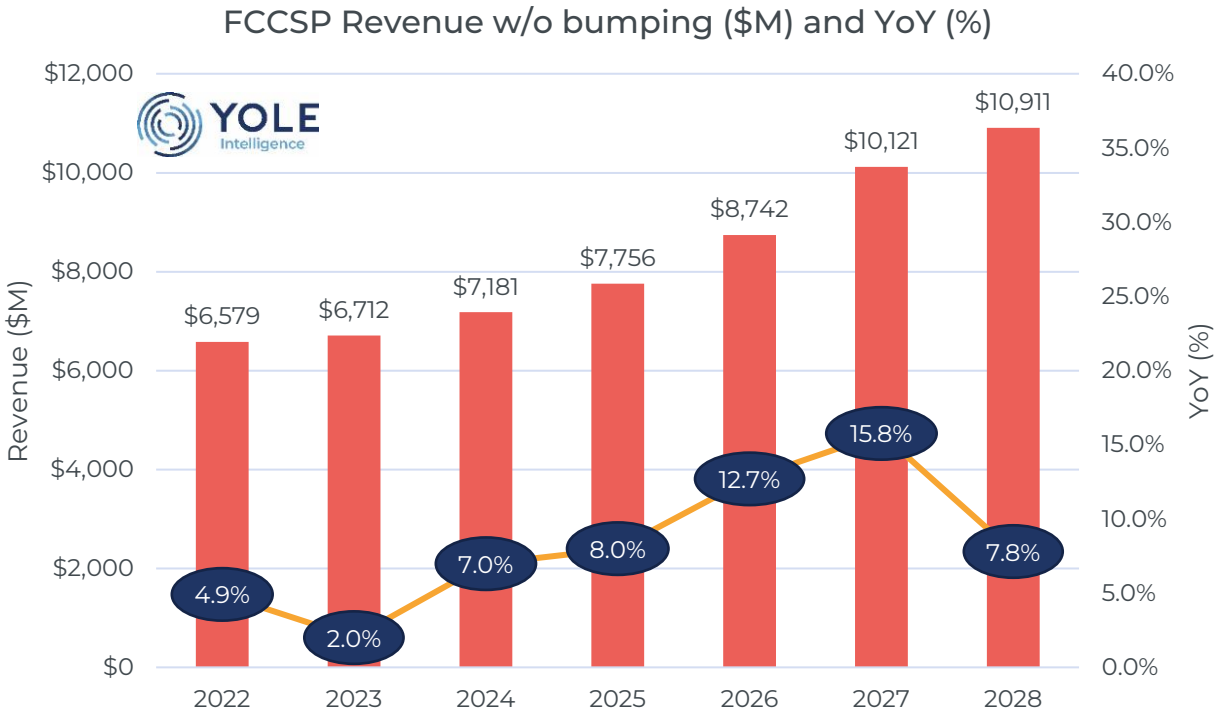


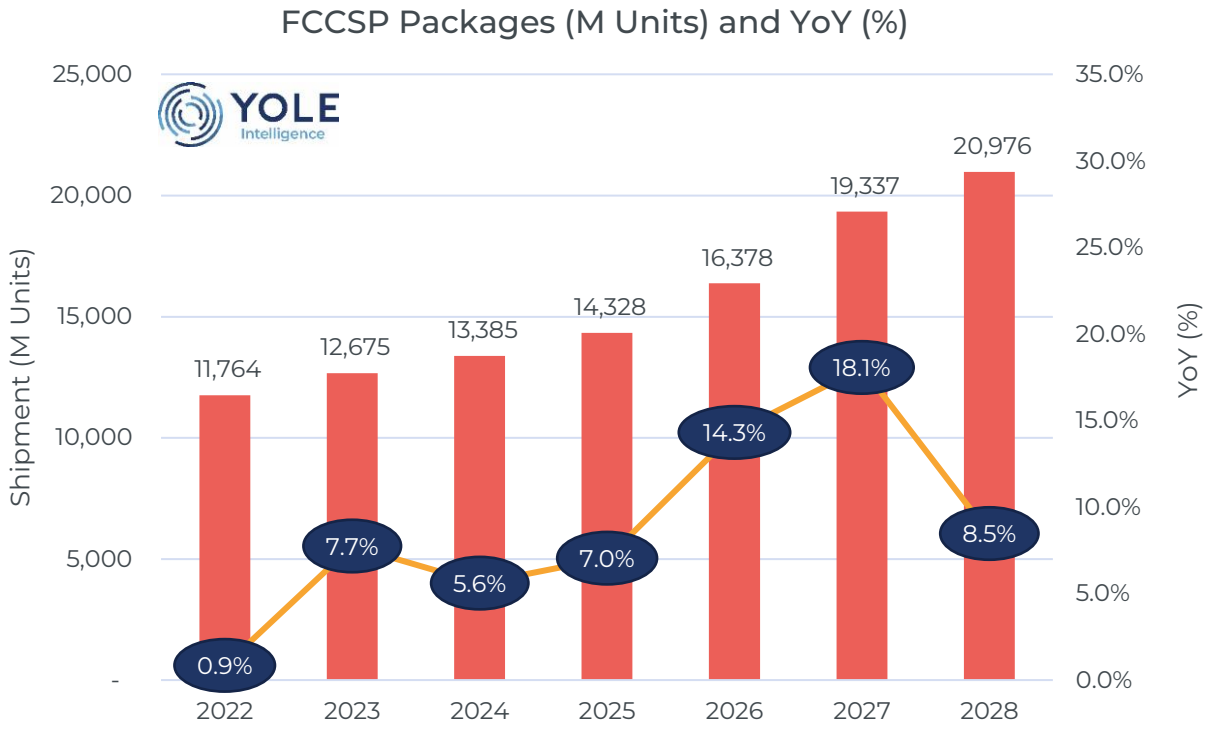


- The addition of the Industrial and Infrastructure end market has led to a higher forecast for FCBGA revenues. Although FCBGA sales growth is slow at 2.1%, high-end demands in HPC and automotive have led to a slight increase in sales. ABF substrate supply has been a constraint, but the supply/demand gap is expected to be smaller in 2023 due to flat demand.
- Investments by LG Innotek and Zhejiang Chuanghao Semiconductor Co., Ltd. are expected to reduce Japanese dominance in the substrate market. The Apple M1 Ultra SoC is the most advanced FCBGA product.
- Key players in FCBGA include ASE w/SPIL, Amkor, and JCET. FCBGA is mainly used for CPUs, GPUs, networking ASICs, and automobile infotainment and ADAS modules.

Source: Yole Intelligence - Advanced Packaging Market Monitor Q1 2023

FCCSP PACKAGE GROWTH

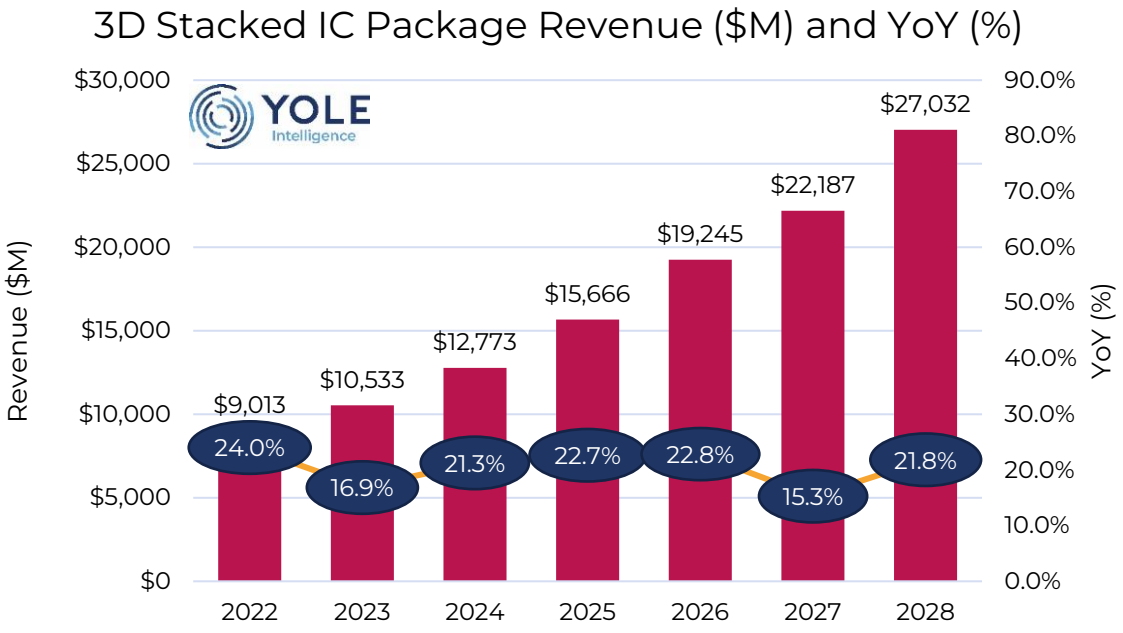


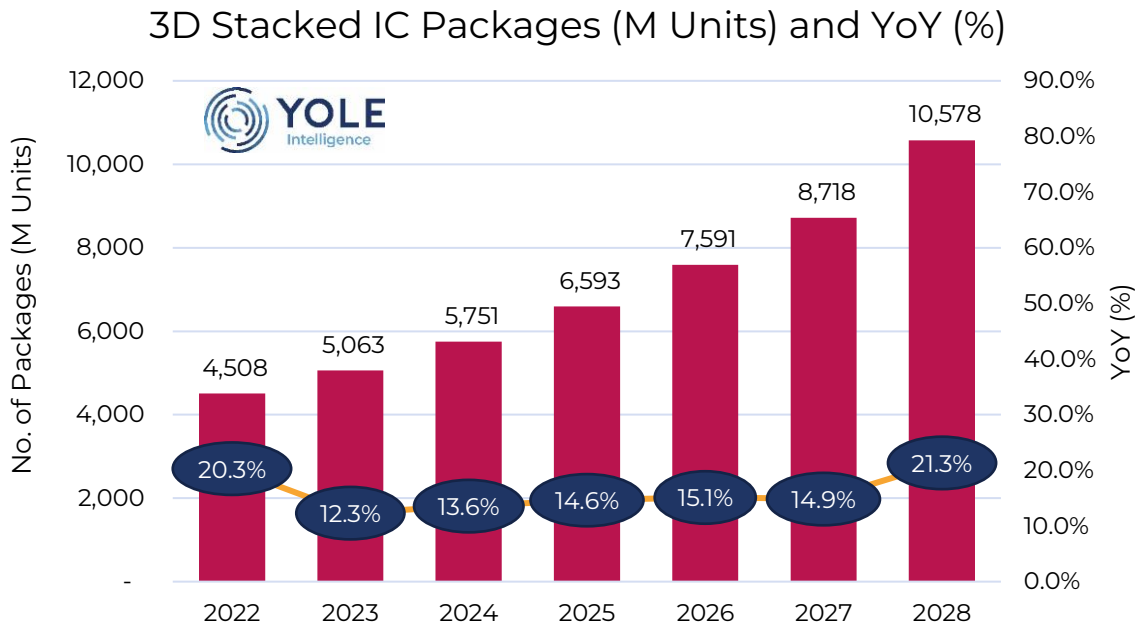


- The FCCSP market is expected to grow by 6.8% in 2023, driven by data center DRAM market growth and demand in the automotive industry.
- Despite a decline in mobile and consumer demand, overall demand for FCCSP is expected to have slow growth.
- The volume is expected to grow at a CAGR of 10.1% between 2022-2028, with flat volume in 2022 and a YoY growth of 7.7% in 2023. FCCSP is predominantly used for baseband, application processors, RF transceivers, RF modulators for 5G smartphones, PC, data centers, automotive memory devices, and PMIC-based devices.
- The key players in FCCSP are ASE w/SPIL, Amkor, and JCET.

Source: Yole Intelligence - Advanced Packaging Market Monitor Q1 2023

3D STACKED (2.5D/3D) PACKAGE GROWTH





- The 3D-stacked IC wafer market is expected to grow at a 29% CAGR over the next six years, driven by 3D NAND, CIS, HBM, and 3DS technologies. Mold Interposer, 3D SoC D2W, and Co-EMIB technologies have the highest CAGRs of 123%, 76%, and 76%, respectively. AMD is using TSMC's SoIC technology for its Ryzen and Milan-X products. SK Hynix and Samsung are supplying HBM3 to Nvidia and are expected to do the same in the future.

- The market outlook for 3D-stacked technologies is positive, driven by Intel, TSMC, and Samsung's efforts in chiplet and heterogeneous integration trends. Samsung, TSMC, Intel, SK Hynix, and Sony are key players in the supply chain for 3D-stacked package production.

Source: Yole Intelligence - Advanced Packaging Market Monitor Q1 2023

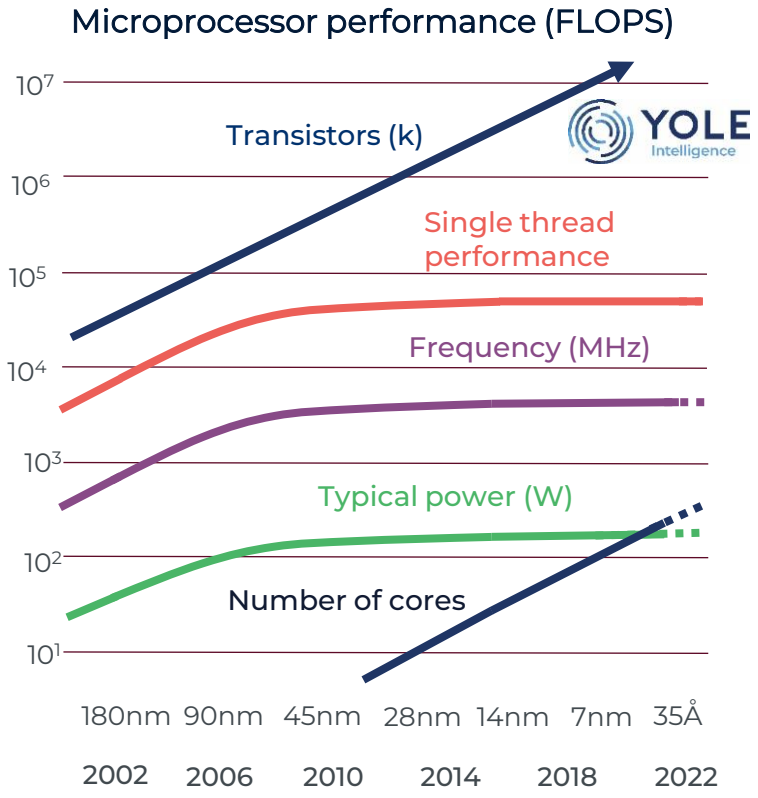
ADVANCED PACKAGING MARKET SUMMARY

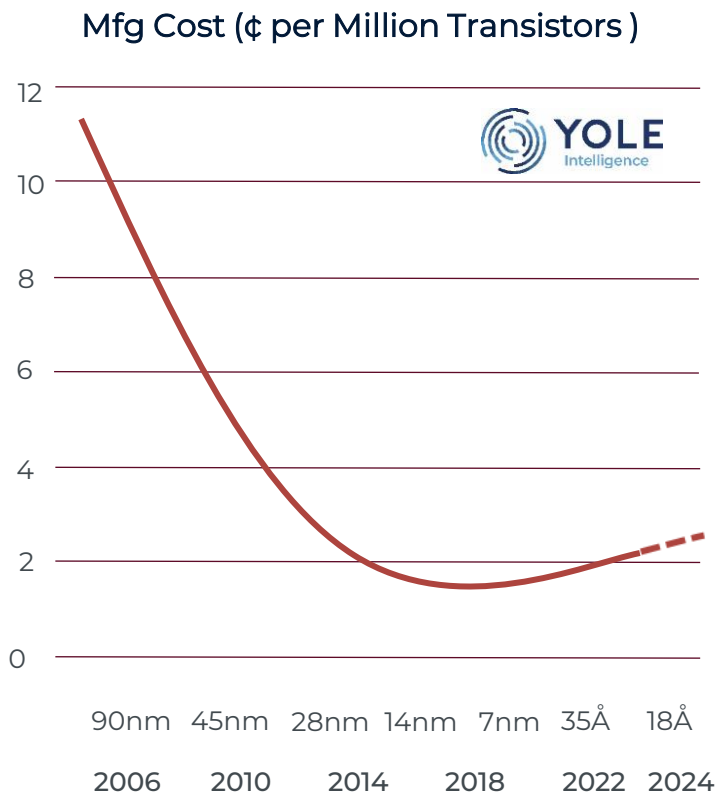
- While demand across industries was uneven through 2022, the global semiconductor revenue grew 1.9% compared to 2021. The revenue growth passed from two-digits growth (32%) in 2021 to single-digit growth in 2022. In 2022, semiconductors globally saw a slowing demand after the massive resurgence in demand in 2021, as inflation rises and end markets saw weaker demand, especially those related to consumer spending. With electronics demand normalizing and amid current supply chain uncertainties, the semiconductor market growth is expected to decrease in 2023.
- The Advanced Packaging market was worth **~$44.3B in 2022**. It is expected to grow at **~ 10% CAGR$_{2022-2028}$ to reach ~$78 in 2028**.
- Nevertheless, the demand for Advanced Packaging will continue to increase as its importance and complexity keep increasing for the advanced device nodes and complex form factors.
- **The total IC packaging market** was worth **$95B in 2022**. Advanced Packaging (AP) was worth $44.3B and is expected to grow at CAGR2022-2028 of 10% to reach $78B in 2028. At the same time, the traditional packaging market will grow at a CAGR$_{2022-2028}$ of 4.15%, and the total packaging market will grow at a CAGR$_{2022-2028}$ of 7.10% to $64.7B and $143.3B, respectively.
- In 2022, **the AP market** represented **47%** Of **the total IC packaging market**. Due to strong momentum in the AP market driven by megatrends, the share of AP in the total semiconductor market is increasing continuously and will reach about **51%** of the market **by 2025**. The highest AP market share belongs to the flip-chip platform (which includes FCBGA, FCCSP, and FC-sip), with 51% of the market in 2022. The highest revenue CAGR$_{2022-2028}$ is expected from ED (in the laminate substrate), 2.5D/3D, and flip-chip at 30%, 18.7%, and 9%, respectively, as high-volume products further penetrate the market.
- **Mobile & Consumer** constituted **70%** of **the total AP market in 2022**, with an expected growth rate of **7% CAGR$_{2022-2028}$**, constituting **61% of the AP revenue by 2028**. **Telecom & infrastructure** is **the fastest-growing segment**, with a revenue growth rate of around **17%,** and will account for **27%** of the AP market in **2028**. **Automotive & Transportation** will account for **9%**, whereas **other segments**, including medical, industrial, and aerospace/defense, will account for **3%** of the market.
- Concerning unit count, traditional packaging accounts for more than 94%. Advanced Packaging shipments will increase at ~6% CAGR$_{2022-2028}$ to 101B units in 2028. WLCSP packages will remain dominant.
- In terms of 300mm eq wafers, traditional packaging still dominates with almost 71% of the total market in 2022. However, AP is continuously increasing its share of wafers, and its market share will increase from ~29% in 2025 to 37% in 2028. The AP wafer production was **~43M 12" wafers in 2022** and is expected to grow at **~ 10% CAGR$_{2022-2028}$ to ~76M wafers in 2028**.

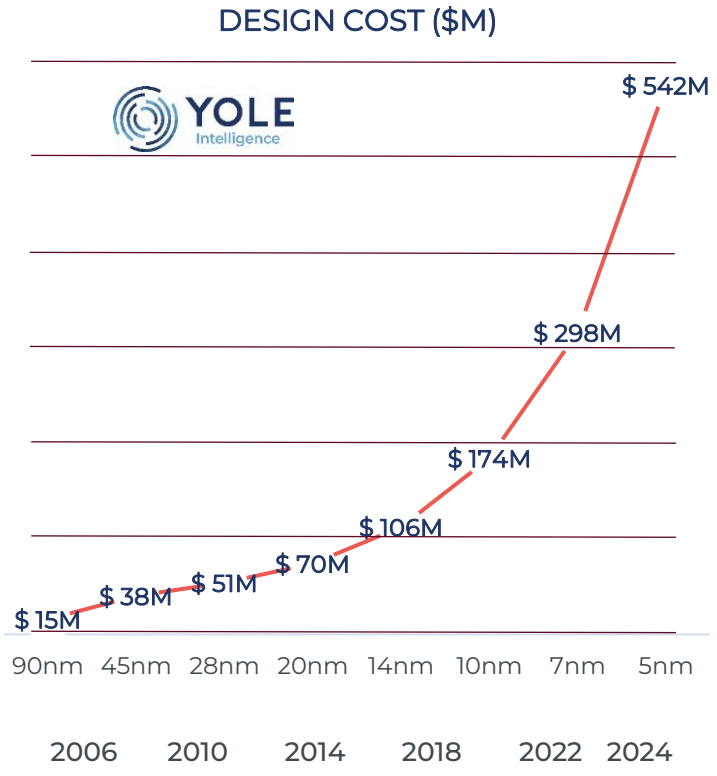
ADVANCED PACKAGING TECHNOLOGY TRENDS

THE PURSUIT OF MOORE'S LAW

Slowed down by increasing design costs but backed up by Advanced Packaging







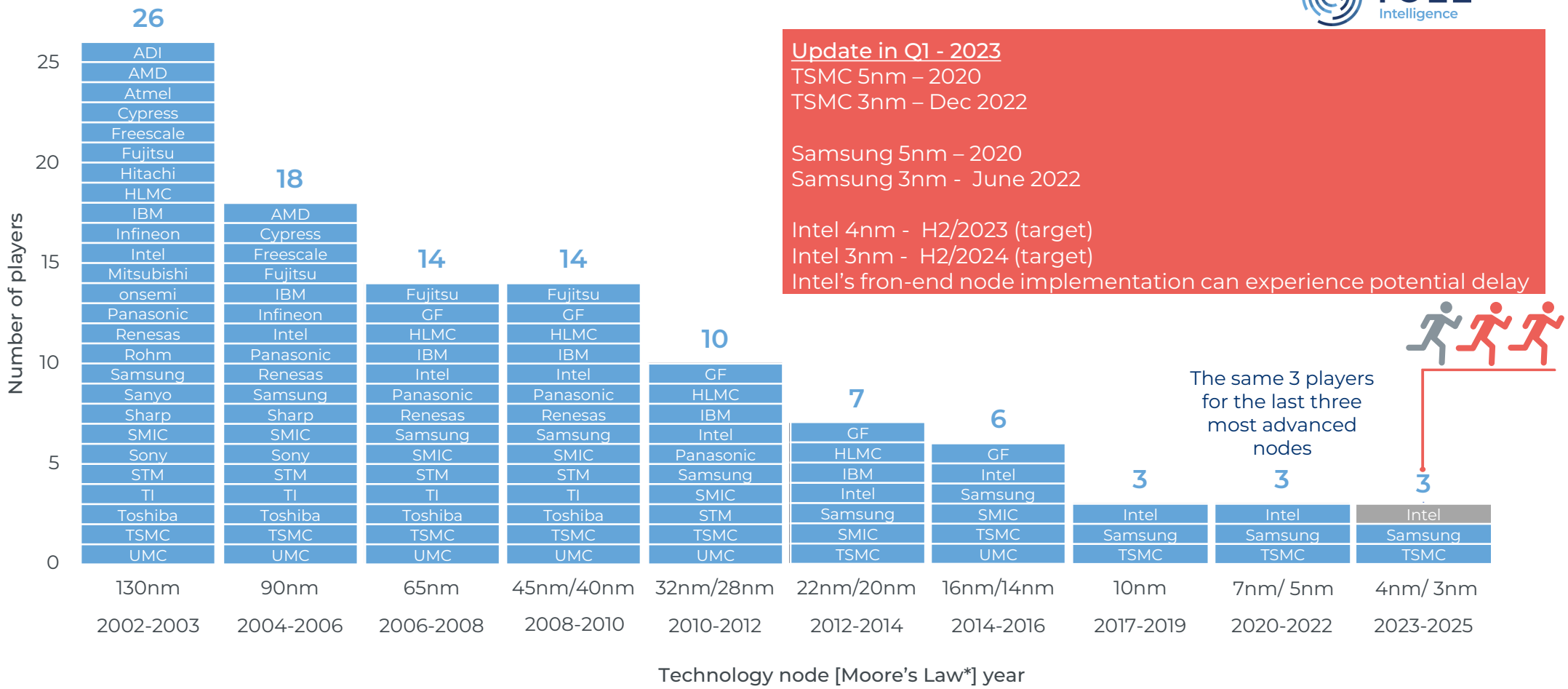
- Moore's Law still holds true but is decelerating due to the atomic limit, at almost 100B transistors per chip. This deceleration is mitigated, as it is backed up by the evolving advanced packaging, while at the same time, rising design costs and manufacturing complexity have led to a longer time-to-market.
- The cost of building new fabs for the most advanced nodes is exorbitant and often not worth the investment for many applications.
- To face this, the industry's approach lies in the adoption of the chiplets and utilizing different AP technologies to design and manufacture the latest SoCs using SiPs, which can reduce costs and time-to-market while enhancing system performance.

SEMICONDUCTOR INDUSTRY

Chronological Order of Players Pursuing Moore's Law

The global semiconductor industry has been guided by Moore's Law since 1965. Performance and cost were improved through node scaling. However, scaling limitations since 2002 have disrupted companies competing in this business, resulting in an oligopoly market with a handful of key players remaining.

Number of players with leading-edge semiconductor manufacturing capabilities



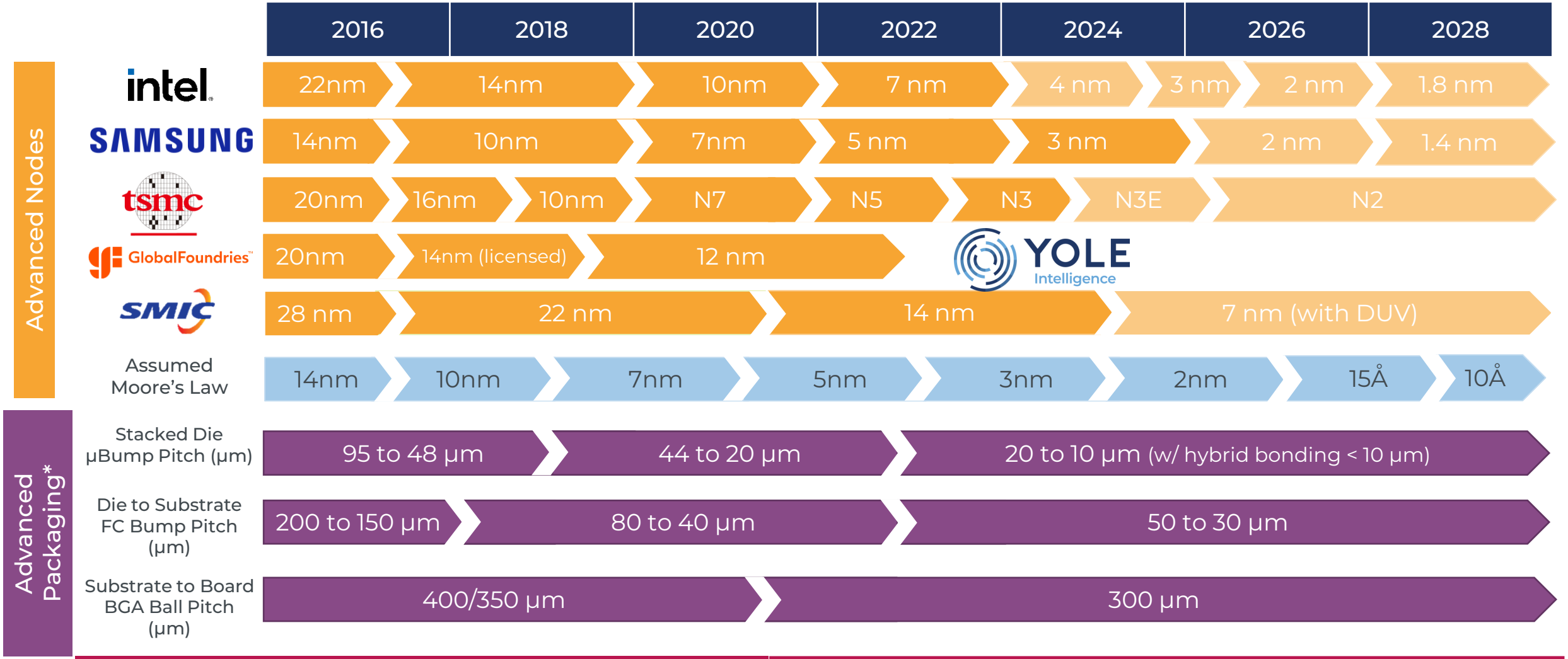
Update in Q1 - 2023
TSMC 5nm – 2020
TSMC 3nm – Dec 2022

Samsung 5nm – 2020
Samsung 3nm - June 2022

Intel 4nm - H2/2023 (target)
Intel 3nm - H2/2024 (target)
Intel's fron-end node implementation can experience potential delay

* Moore's law states that the number of transistors in an integrated circuit chip doubles every 2 years
* Data referenced from Intel and WikiChip
* Intel's node scaling roadmap is very aggressive to catch-up Samsung and TSMC; we are following this closely to check how this roadmap is respected

TECHNOLOGY ROADMAP: FROM NANO-SCALE TO MICRO SCALE



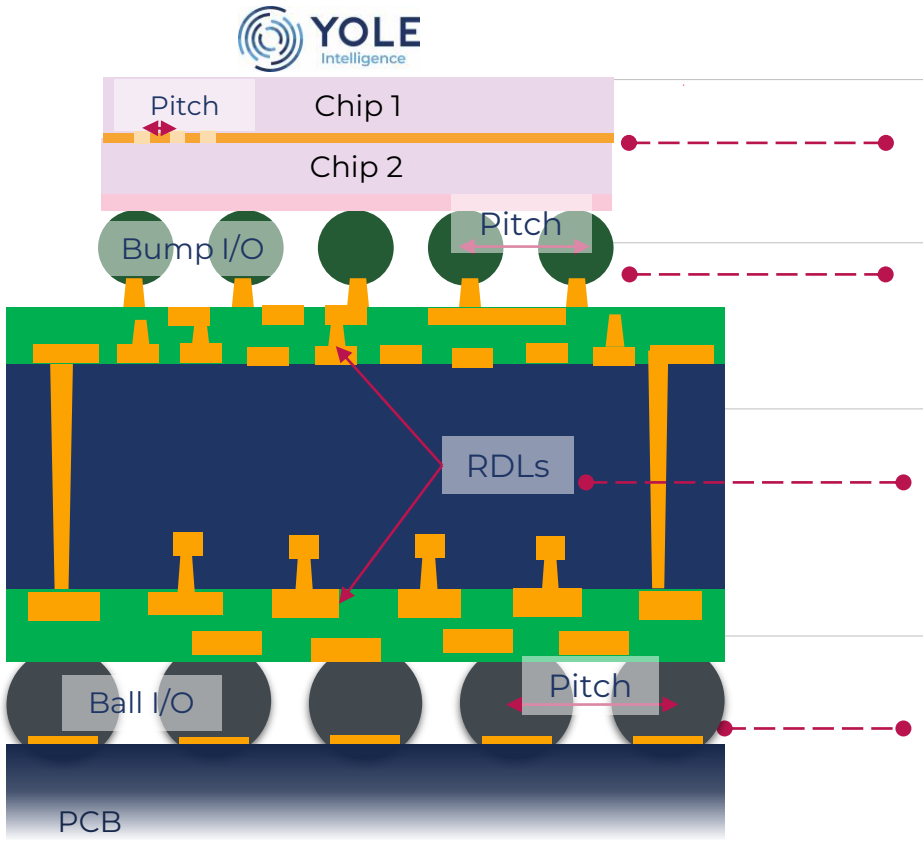
Industry is looking into the growing importance of functional roadmap

Advanced Packaging is essential to bridge the scale-gap between die and PCB

Average trends based on technology and industry expectation
*Minimum dimension

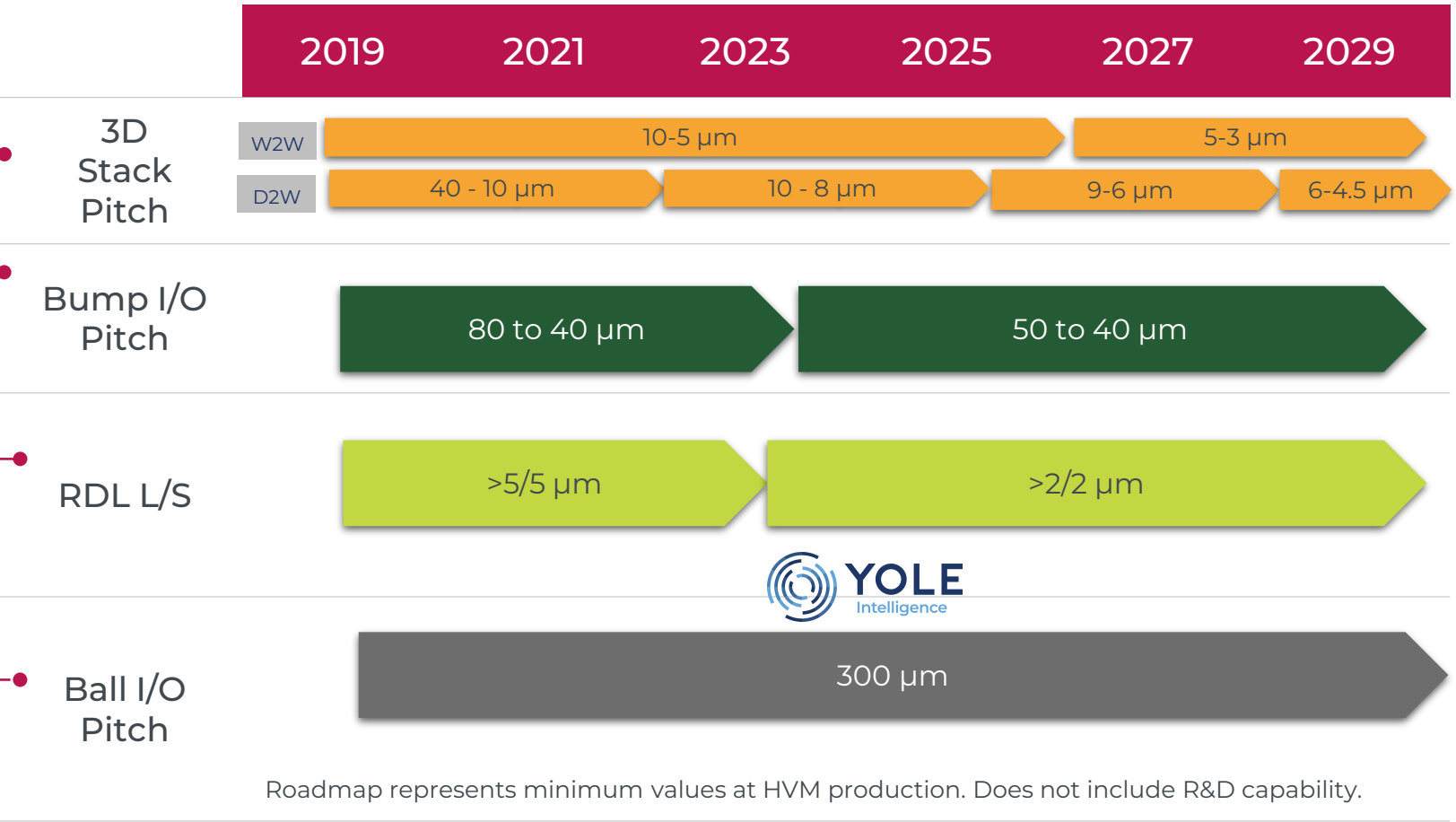
ADVANCED PACKAGING ROADMAP: I/O PITCH AND RDL L/S

A typical flip-chip IC Substrate



Schematic not drawn to scale

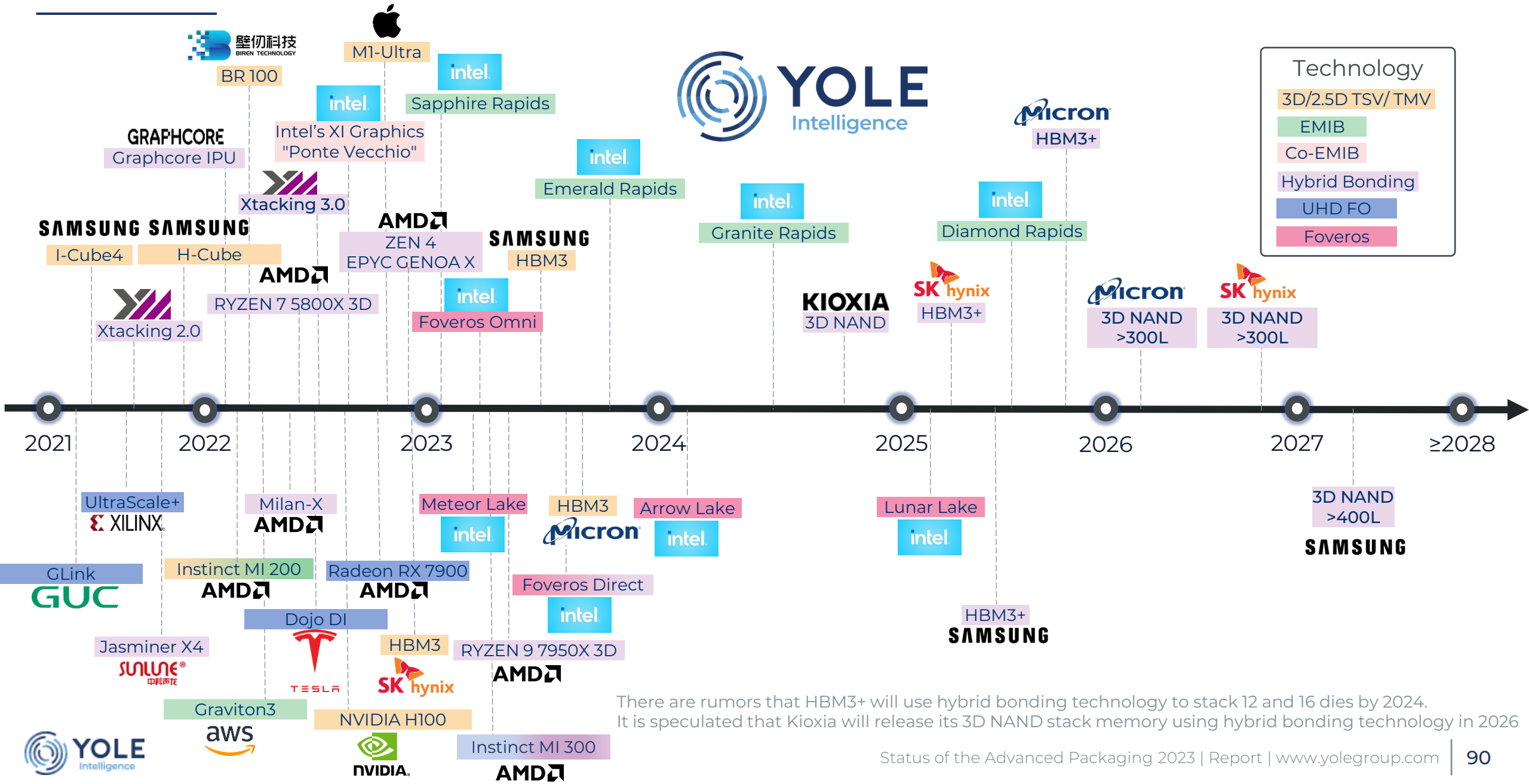
Advanced Packaging Technology Roadmap



Roadmap represents minimum values at HVM production. Does not include R&D capability.

Bump I/O pitch is scaling much faster than Ball I/O pitch which drives a finer RDL L/S at IC substrate package level.

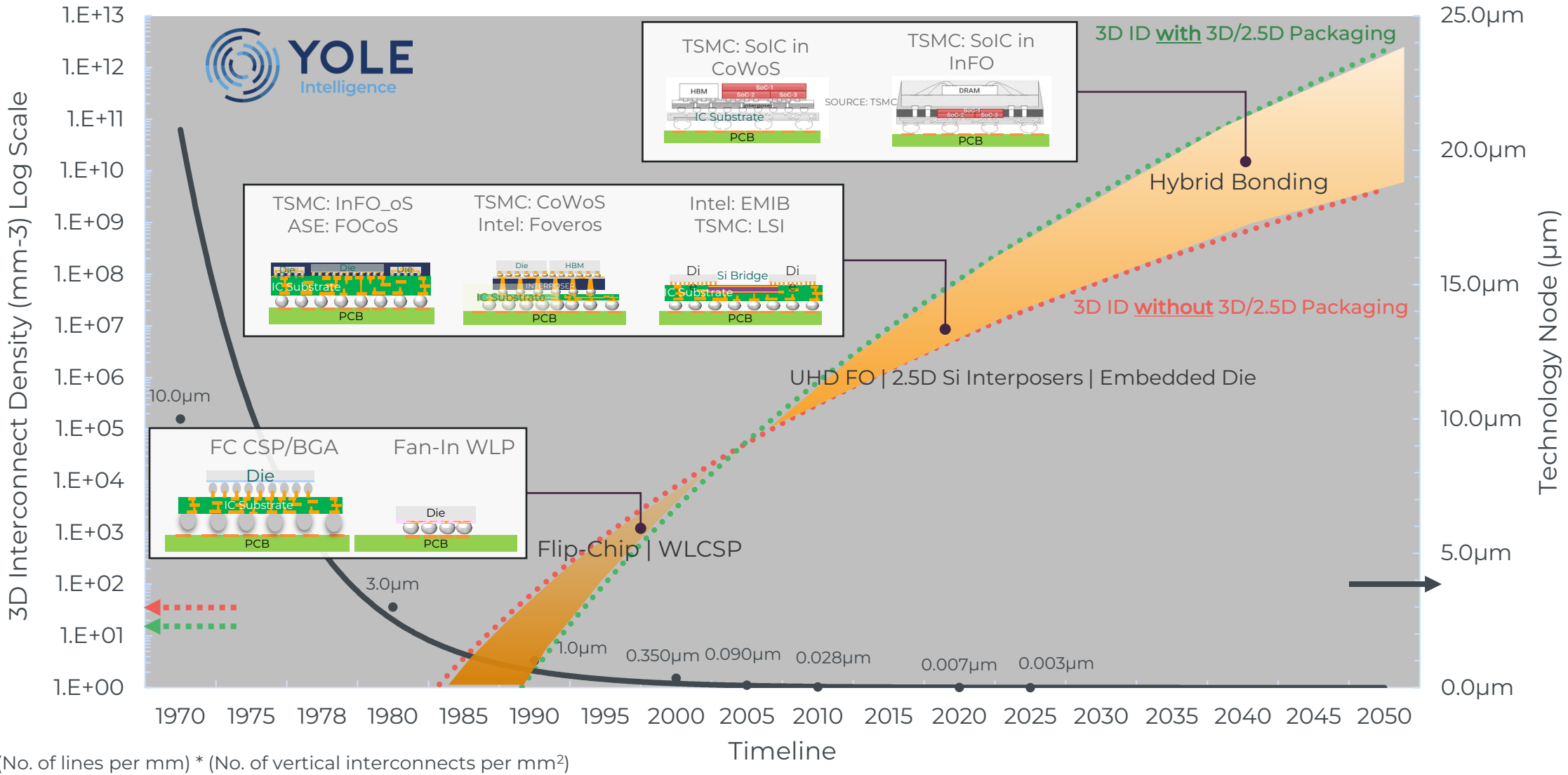
HIGH-END PACKAGING ROADMAP: APPLICATION-TECHNOLOGY



There are rumors that HBM3+ will use hybrid bonding technology to stack 12 and 16 dies by 2024.
It is speculated that Kioxia will release its 3D NAND stack memory using hybrid bonding technology in 2026

SEMICONDUCTOR PACKAGING ROADMAP

Combined Timeline of 3D Interconnect Density & Technology Node



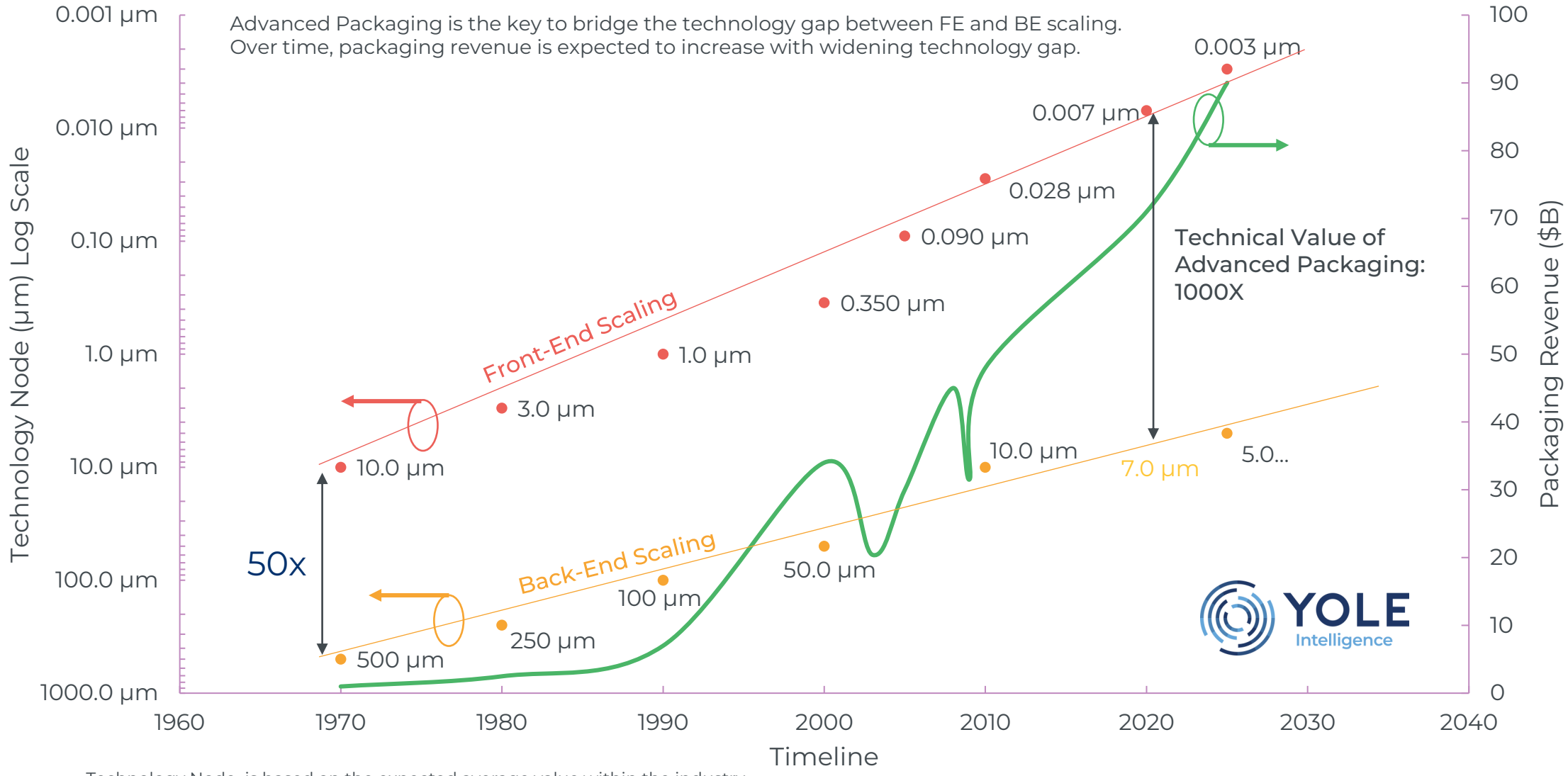
3D ID = (No. of lines per mm) * (No. of vertical interconnects per mm^2)

3D Interconnect Density Data adopted from TSMC

Technology Node here refers to front-end node and is based on the expected average value within the industry.

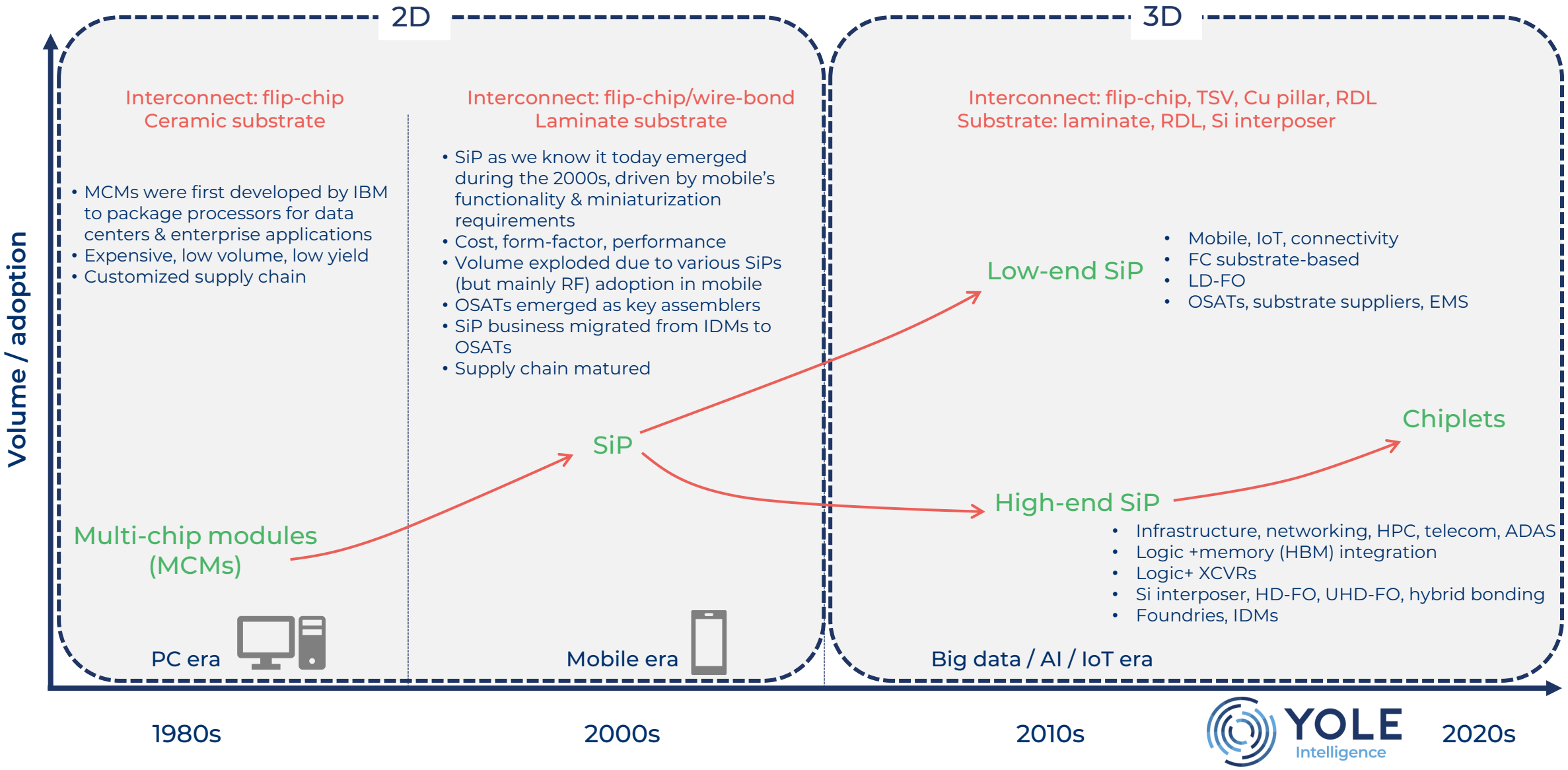
SEMICONDUCTOR PACKAGING VALUE ROADMAP

Combined Timeline of Technology Node & Packaging Revenue



Technology Node is based on the expected average value within the industry.
Packaging Revenue is based on Yole Group's market valuation and reference from external research.

SYSTEM-IN-PACKAGE (SIP) - HISTORICAL EVOLUTION

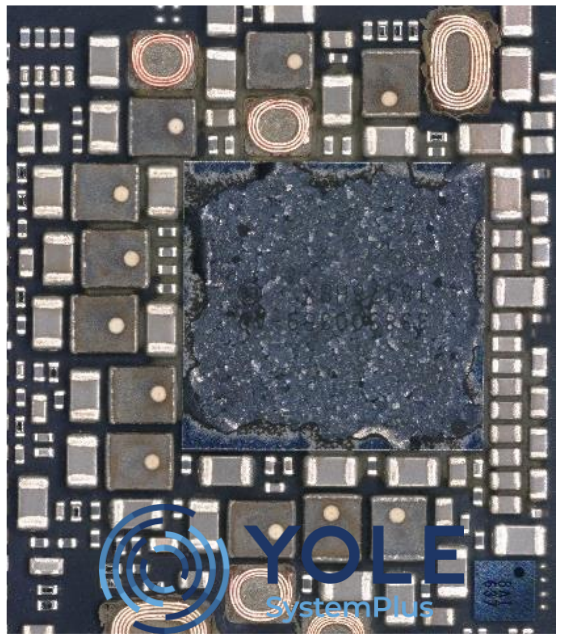


KEY DRIVERS FOR SIP VS. STAND-ALONE PACKAGES

Apple Watch S4
Non-Cellular (Standalone)
PMIC & Passives

37% Package Area Reduction

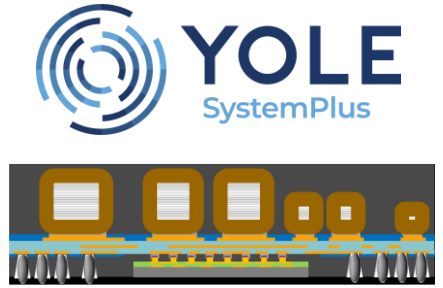
Apple Watch S4
Cellular (SiP)
PMIC & Passives

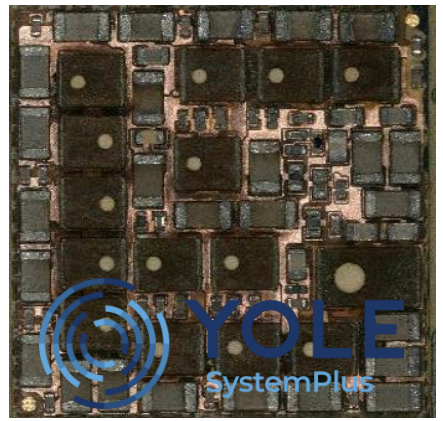


94.6 mm²

SiP Drivers

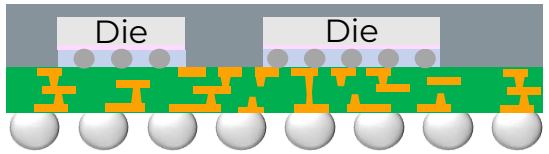
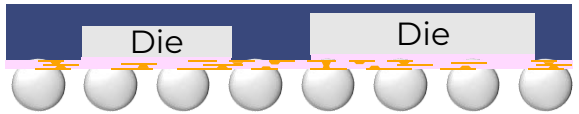
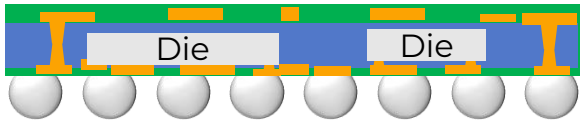
- Thinner / smaller form factor than individually packaged components
  - Reduced system board space compared to standalone packages
  - Improved power management and more room for battery
  - Increased performance and functional integration at a lower real estate
- Design flexibility compared to standalone packages
- Simpler cost effective SMT assembly process with fewer processes
- Cost-effective “plug-and-play” solutions
- Faster time-to-market (TTM)
- Allows better electromagnetic interference (EMI) isolation





59.94 mm²

ADVANCED PACKAGING: SIP TECHNOLOGIES

Package Type	SiP Capable Technologies		
	FC (IC Substrate)	Fan-Out	Embedded Die
Schematic (*Not drawn to scale*)			
Substrate level RDL Line/Space	5/5µm < L/S < 30/30µm	2/2µm < L/S < 30/30µm	9/12µm < LS < 50/50µm
Process	Panel: SAP / mSAP	Wafer/Panel: Thin film RDL	Panel: Lamination SAP
SiP: I/O area beyond die limit	Yes	Yes	Yes

COMPETITION

There is direct competition between FC substrates and Fan-out Packaging and Embedded Die. Embedded Die standardization, test methodology is not mature. Depending on performance, cost, and time-to-market, one or another can be a better option.

L/S RESOLUTION

Thin Film RDL has a clearer scaling path below L/S 5/5 µm and is considered to have an advantage over FC substrates in that area. For L/S between 5/5 µm and 15/15 µm, cost and performance will be critical in customer choice. Embedded die manufacturing yield is low for non-single die packages: Typically, 70–90% (need > 98%)

PROCESS

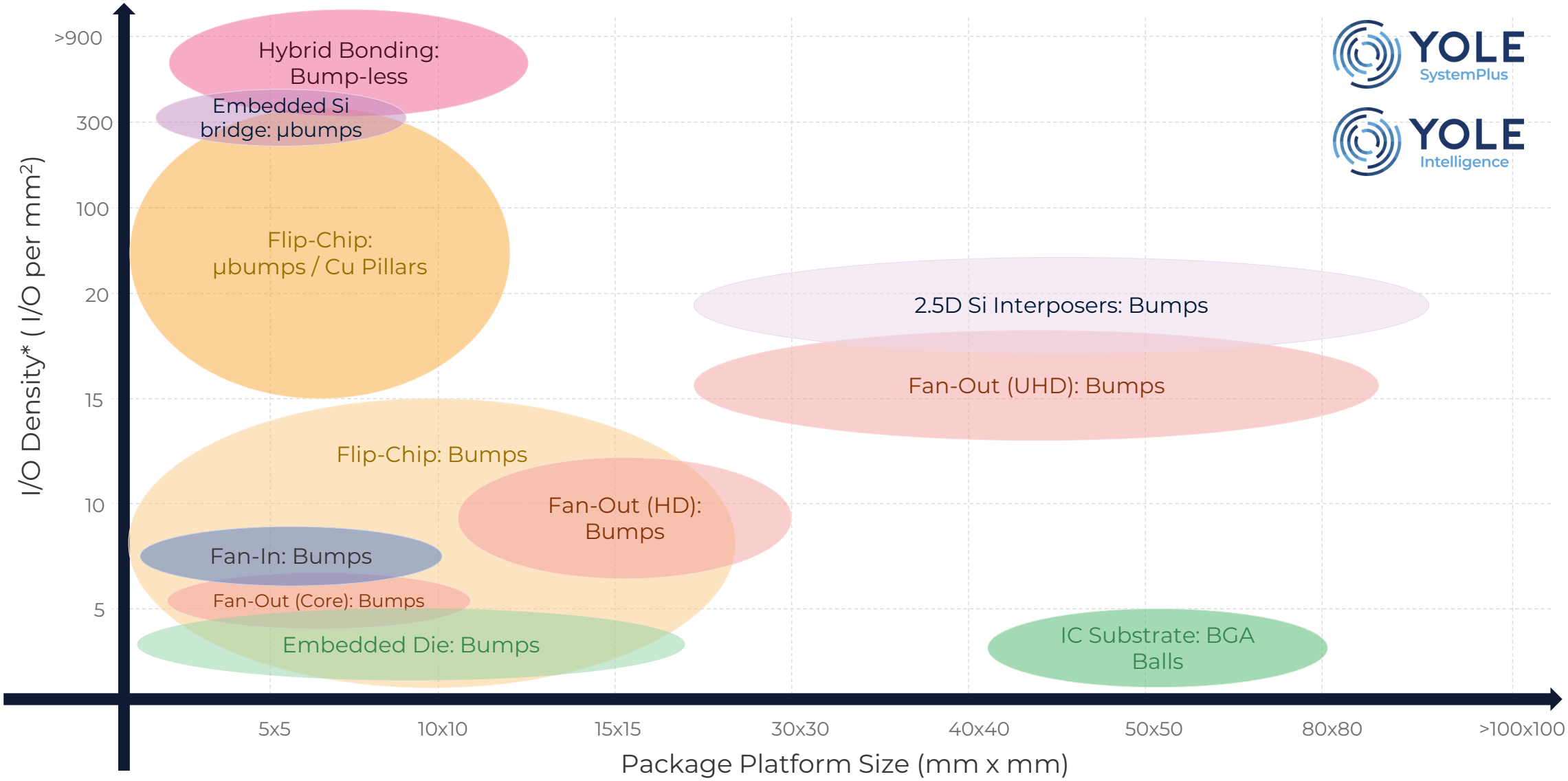
The SAP for substrates is represented by substrate manufacturers, while thin-film RDL technologies are manufactured by top OSATs, WLP houses and certain foundries (e.g., TSMC). SAP process is believed to offer good yields for high volume production down to L/S 5/5 µm. No issue with thin wafer handling, wafer warpage. Manufacturing yield is low for non-single die packages: Typically, 70–90% (need > 98%).

SiP POTENTIAL

FC IC Substrate is very mature. It has a coreless substrate in production, for HD SiP in low I/O products: typically for wireless and communication module packaging for smartphones/wearables. FO has good characteristics for SiP for low-end devices within a limited package size, <10mm x 10mm, such as radar in automotive and mid-end devices, and PMIC+APE in wearables. ED is a “component level” packaging of power and analog applications (IPD, MOSFETs, RFID, etc.) for low-end devices.

ADVANCED PACKAGING TECHNOLOGY ROADMAP

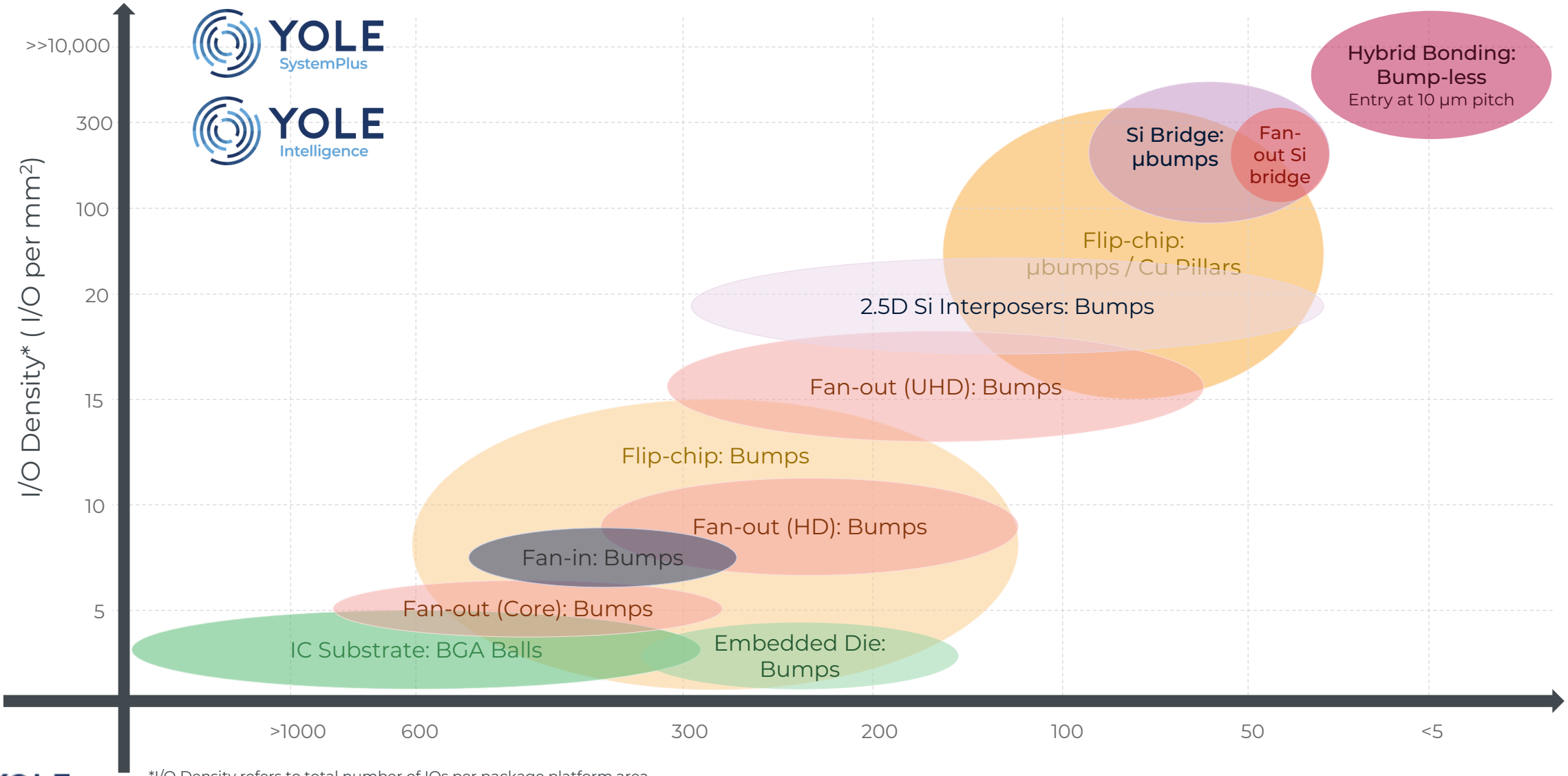
I/O Density vs Package Platform Size



*I/O Density refers to total number of IOs per package platform area.
Plot is generated based on Yole Group database, with reference to industry average value.

ADVANCED PACKAGING TECHNOLOGY ROADMAP

I/O Density vs IO Pitch



*I/O Density refers to total number of IOs per package platform area.
Plot is generated based on Yole Group database, with reference to industry average value.

HIGH VOLUME MANUFACTURING ROADMAP FOR FOWLP

Key parameters

The roadmap described here represents the minimum or maximum parameters found in fan-out packages throughout the industry. It is important to note that parameters depend on the application and, therefore, on package type and fan-out market class.

Parameters	≤2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
Maximum package size	20mm x 20mm				40mm x 40mm				>>50mm x 50mm	
Side-by-side dies	2~3				2~5				2~8	
Max # of RDLs	3x RDL				4x RDL				5x RDL	
Min. line/space	8µm/8µm			2µm/2µm					1.5µm/1.5µm	
Package min. thickness (without BGA)	250µm				200µm				150µm	
Minimum die size (X–Y directions)	900µm				500µm				200µm	
Maximum die size (X–Y directions)	10mm				20mm				30mm	
Minimum bump pitch	400µm			350µm			300µm		150 µm	
Minimum die-to-die distance	250µm				200µm				100µm	

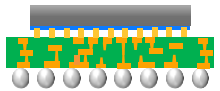
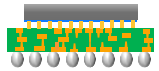
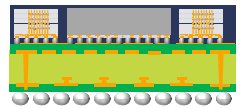
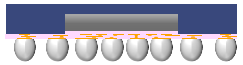
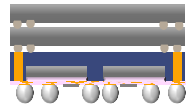
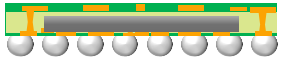
HIGH VOLUME MANUFACTURING ROADMAP FOR FAN-IN WLP

Key parameters*

Parameter	≤ 2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
Maximum package size	70-100mm^2					>100mm^2				
Max I/O count	400-600					>1000				
Max level of RDL	1-2 RDL									
Min. Line/Space	10/10µm				8/8µm				5/5µm	
Package min. thickness (without BGA)	200µm				150µm				80µm	
Passivation layer	PI/PBO/Low temp. Cure PI (<250C)					Low temp. Cure PI (<200C)				
Minimum bump pitch	300µm				250µm				150µm	

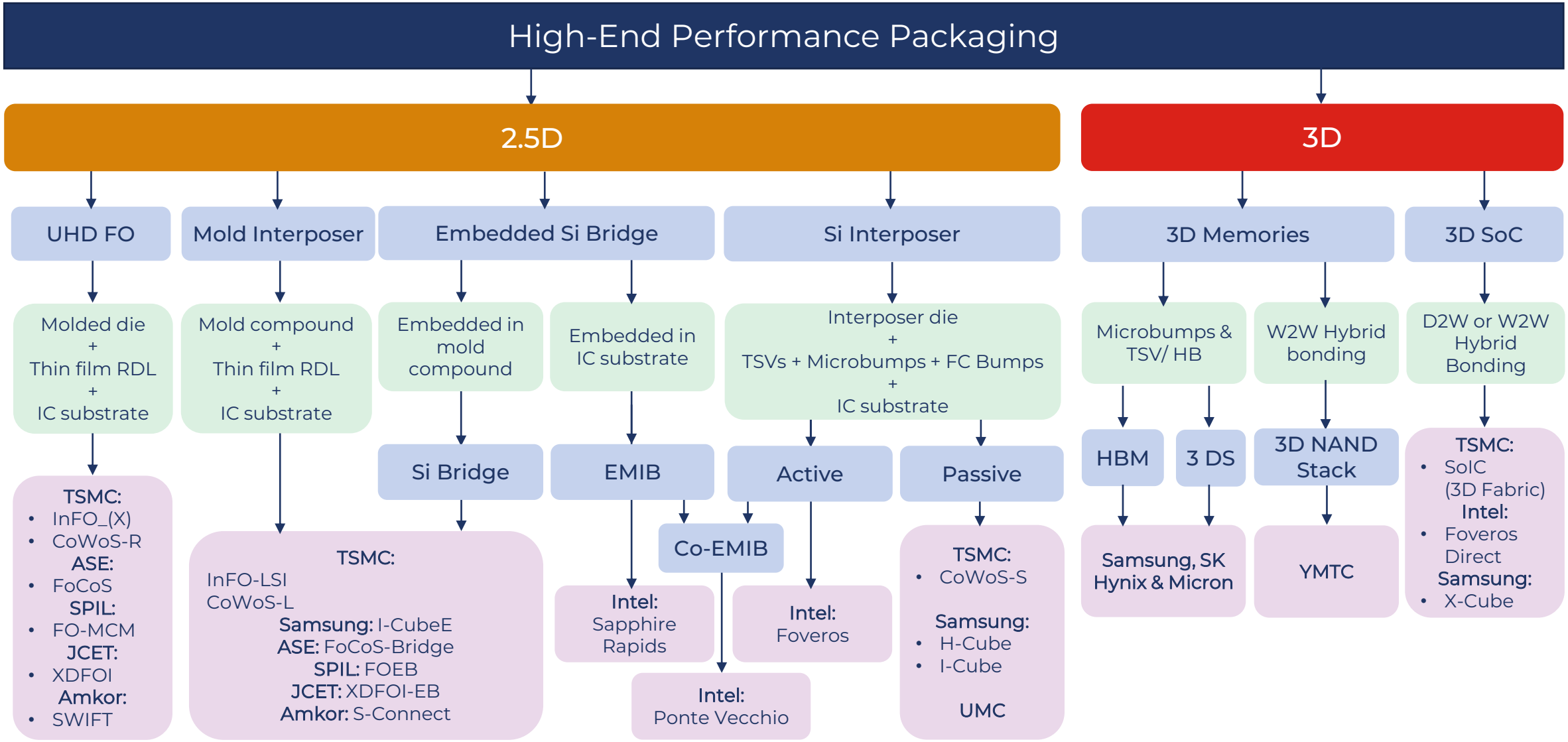
* Roadmap described here is for volume production and is an average of the expected different technologies in the market.

SIP TECHNOLOGY ROADMAPS - KEY PARAMETERS

Typical	Parameters	≤ 2022	2024	2026	2028	SiP Advancement
Flip-Chip (IC Substrate)	Substrate RDL L/S	≥ 8/8 µm		≥ 5/5 µm		FC BGA SiP
FC BGA	Substrate I/O Ball Pitch	≥ 300 µm				
	No. of I/O Ball Count	500 - 3000		>> 3000		
FC CSP	Max Package Size	80x80 mm		100x100 mm		Double-Sided FC SiP
	Max no. of Dies/Passives	≤ 35		≥ 35		
	Max level of RDLs	10 - 18x RDLs		>> 18x RDLs		
Fan-Out	Substrate RDL L/S	5/5 µm to 2/2 µm		> 1/1 µm		FO on Substrate
FO	Substrate I/O Bump Pitch	300-350 µm		150 µm		
	No. of I/O Bump Count	600 -1300		>> 1500		
	Max Package Size	30x30 mm		> 50x50 mm		HD FO SiP PoP
	Max no. of Dies/Passives	≤ 4		≤ 6		
	Max level of RDLs	3x – 4x RDL		≥ 4x RDL		
Embedded Die	Substrate RDL L/S	> 20/20 µm		> 10/10 µm		Embedded Interconnects
Embedded Die	Die I/O Pitch	250-80µm		50 µm		
	Die I/O Numbers	100-150		150-200		
	Max Package Size	> 15x15 mm		> 50x50 mm		Embedded Multi-Dies
	Max no. of Dies/Passives	≤ 3		≤ 4		
	Max level of RDLs	2x - 6x RDL		2x – 8x RDL		

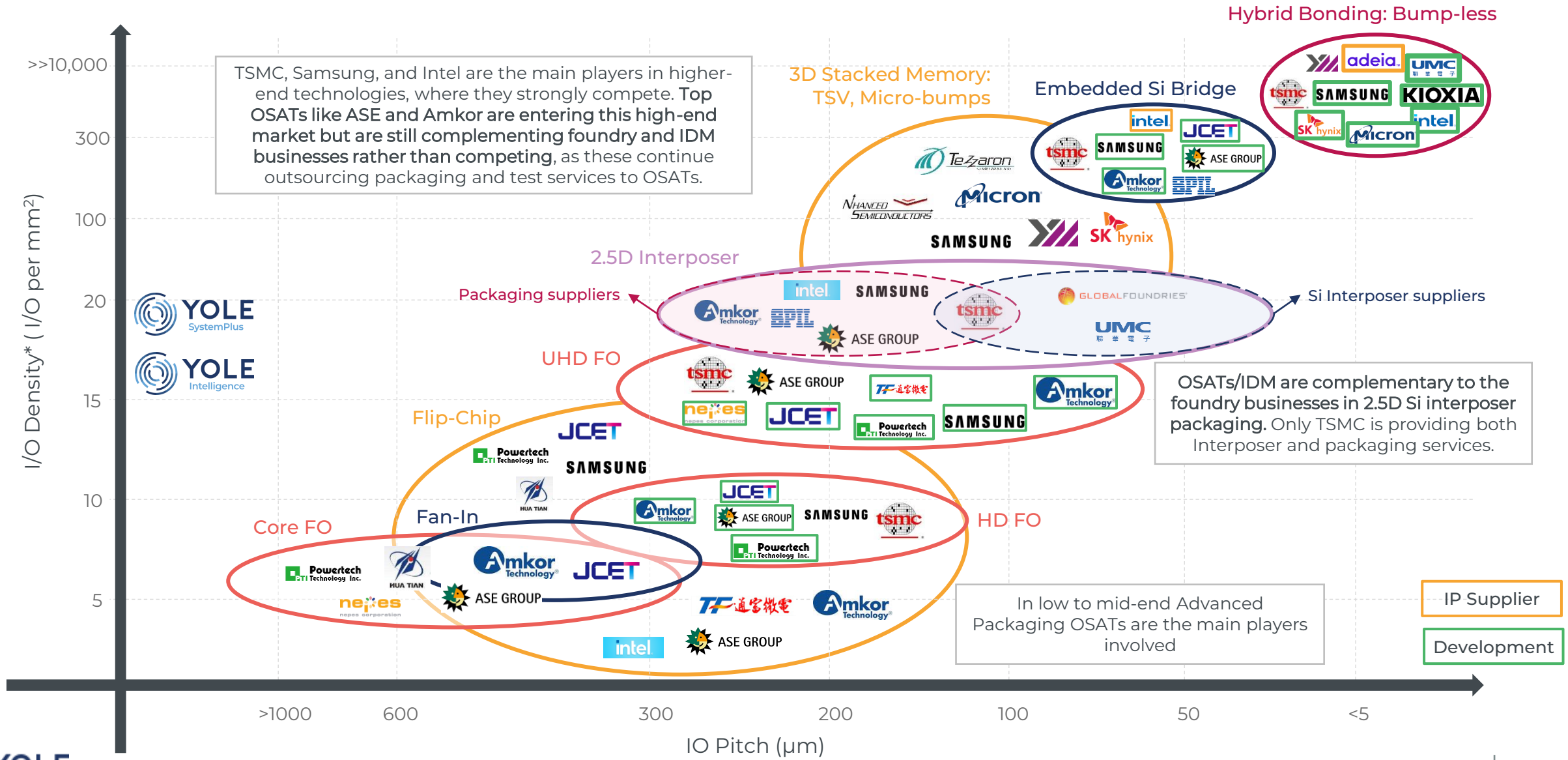
HIGH-END PERFORMANCE PACKAGING: ALL PLATFORMS

Yole's classification for 2.5D and 3D



ADVANCED PACKAGING – PLAYERS INVOLVED

Mapping of competitors based on technology



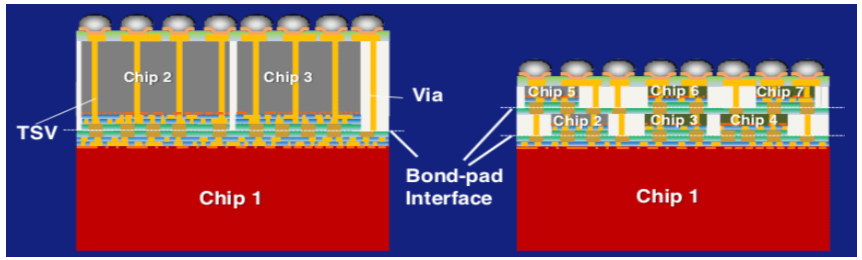
Non-exhaustive List of Players

3D SYSTEM ON CHIP (3D SOC)

Introduction: 3D SoC as the path forward to extend Moore’s Law

SoIC Chiplet Stacking

SoIC ImMC*



*ImMC: Immersion-in-Memory-Computing

SoIC is TSMC’s 3D SoC integration technology
Multi-tier each with multi-chip could be accomplished by known-good-die stacking.

Source: TSMC

Why 3D SoC?

- Moore's Law predicts transistor count doubles every two years on an integrated chip. This has remained true for almost all high-performance computing systems, including CPU, GPU, FPGA, mobile AP, and special AI accelerators. Despite the continuous increase in technical challenges and cost escalation, Moore’s Law remained healthy and strong for over five decades.
- Although transistor scaling continues through node-to-node migration, escalating big-data generation demands new high-performance computing, including AI/ML. It drives larger and larger systems, driving the industry beyond the current monolithic SoC lithographic and wafer-yielding management capacity. Hence the industry is aggressively adopting 3D SoC to address monolithic SoC’s limitations for such new demands.

What is 3D SoC?

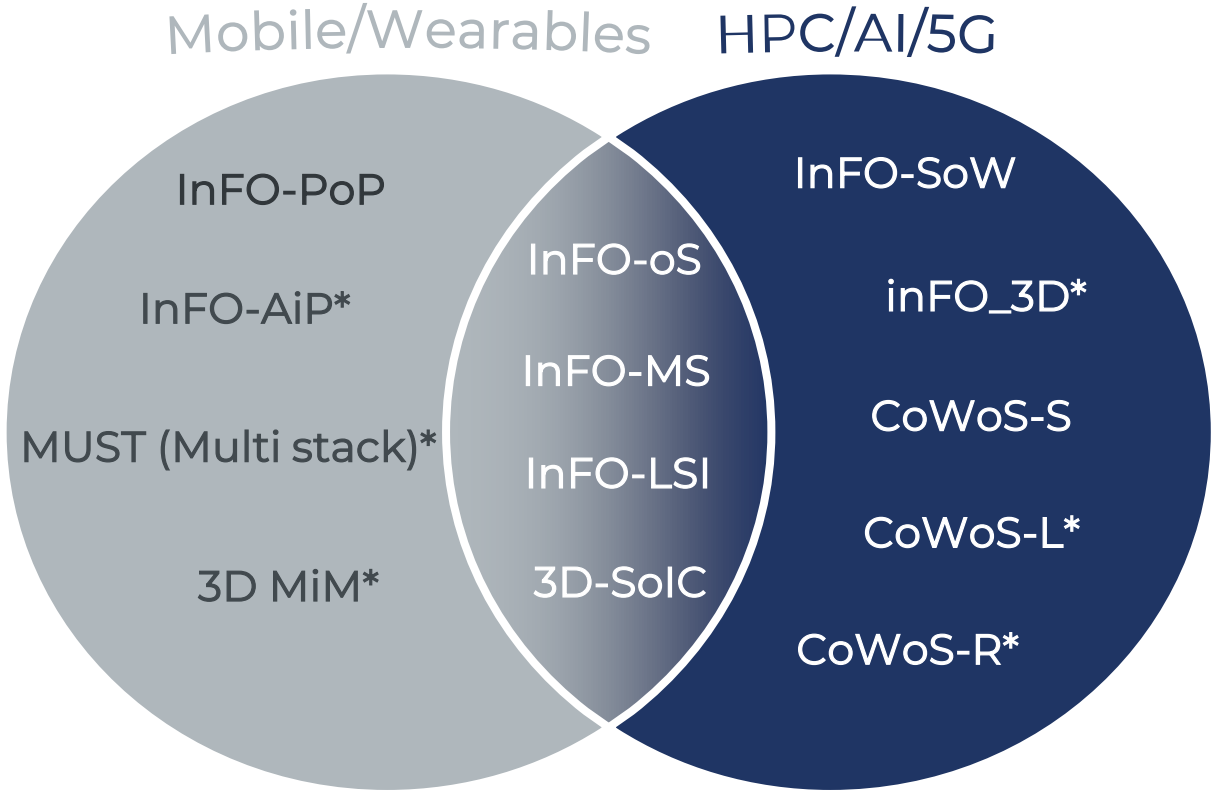
- A 3D system on chip is a system on a chip that was initially partitioned when designed and then stacked.
- 3D SoC can be logic on logic, memory on logic, or logic on memory.
  - It offers a solution for applications requiring an L4 cache memory, which is typical for applications with data flow.
- The stacking can be done by wafer-to-wafer bonding (direct or hybrid).
- The main rationale for stacking SoCs is the following:
  - Overcoming the issue of the size of the reticle for manufacturing large dies (like other partitioning applications);
  - Minimizing the interconnection lengths from mm length to µm length, moving from lateral to vertical connections;
  - Reducing footprint, increasing the total SoC surface.
- Besides some design constraints, thermal management remains the main technical challenge.

Technology Trends: Focus on TSMC

TSMC ADVANCED PACKAGING

TSMC has been at the forefront of developing cutting-edge Advanced Packaging solutions ranging from fan-out to 3D IC packaging. In 2011, TSMC introduced CoWoS, a high-end Advanced Packaging platform that utilizes silicon interposers for heterogeneous integration. Since then, TSMC has continued to introduce a series of innovative Advanced Packaging solutions such as InFO (and its multiple versions), SoIC, 3D Multi-stack (MUST) system integration technology, 3D MUST-in-MUST (also known as 3D-MiM fan-out package), and 3D SoW. Recently, TSMC merged its 2.5D and 3D packaging offerings into a single brand called "3D Fabric".

In addition to its wafer-level system integration (WLSI) platform, TSMC is investing in an Advanced System Integration fab to support 3D Fabric offerings, providing full assembly and test manufacturing capabilities.

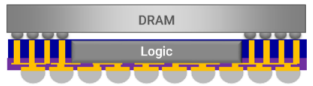
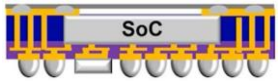
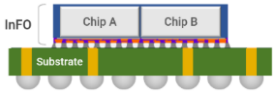
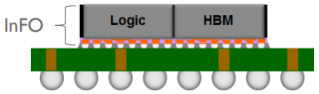
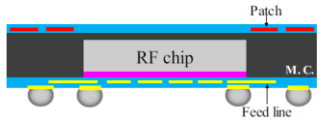
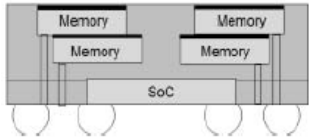
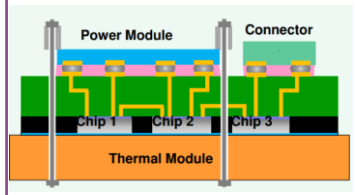
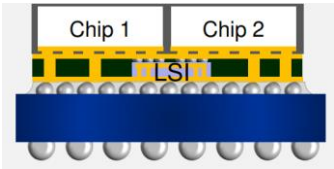


*Under development/qualification

**TSMC recently released an ultra-high-density version of SoIC. This version enables 3D multi-tier chip stacking, creating what TSMC calls Immersion-in-Memory Computing (ImMC). In one example of ImMC, a device could have three tiers where each tier has logic and memory dies, and different tiers are connected using hybrid bonding.*

TSMC ADVANCED PACKAGING – FAN-OUT

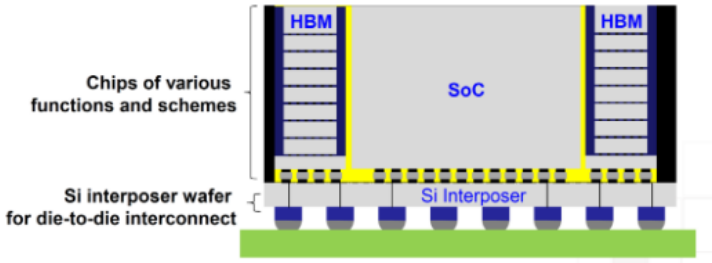
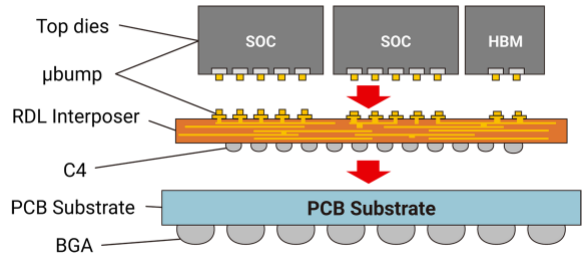
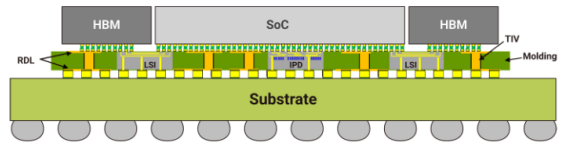
New InFO technologies

Metrics	InFO_PoP/ InFO_B	InFO_oS & InFO_MS	InFO_AiP	InFO_MiM	InFO_SoW	InFO_LSI
PRODUCTION	HVM since 2016	LVM since 2018	Qualification LVM expected in 2022/2023	Qualification	LVM since 2021	LVM since 2021
STATUS	High-volume production of Gen-3. Successful qualification of Gen-4.	Successful qualification of multiple 16nm SoC chips. Better yield.	Successful qualified. Enables low transmission loss and high antenna performance for mmWave system.	Validated better performance compared to FC.	Demonstrated industry-first full-wafer HI technology with good process control and high quality RDL.	Completed qualification in 2021.
APPLICATION	Mobile APU+Memory: smartphone, smartwatches, tablets	High Performance Computing: AI chips, servers; networking.	mmWave wireless communication: 5G, Wi-Fi, modems, sensors.	Advanced Mobile & HPC.	High Performance Computing: AI chips, servers; networking.	Computing; AI chips, servers; networking.
BENEFITS	Integrate systems with lower TTV compared to FC, at finer L/S for board-level I/O.	Enable better yield compared to a single large die SoC.	Enables low transmission loss and high antenna performance for mmWave system.	Validated and simulated better performance and form factor as compared to FC and TSV.	Higher bandwidth density, lower latency and PDN impedance compared to FC MCM.	Integrating SoC chips with UH-Bandwidth density at a lower cost than a Si Interposer and lower pitch and L/S compared with InFO_oS.
SCHEMATIC	InFO_PoP  InFO_B 	InFO_oS  InFO_MS 				

Source: TSMC

TSMC ADVANCED PACKAGING – 2.5D INTERPOSER

Chip-on-Wafer-on-Substrate (CoWoS®) technologies

Metrics	CoWoS-S	CoWoS-R	CoWoS-L
PRODUCTION	HVM since 2012	Risk production starting in Q2 2023	Production in 2024-2025 (assumed)
STATUS	Production	Qualification	Qualification
APPLICATION	HBM, HPC	HBM and SoC heterogeneous integration High-speed and AI	HPC
BENEFITS	Si Interposer 2.5D UH interconnection density. Si interposer can be passive or active circuitries Pitch and bandwidth density better than CoWoS-R	RDL interposer Lower cost, form factor and power and signal integrity benefits. Pitch and bandwidth density	RDL Interposer with LSI HD USR connections Local HD interconnection to eliminate large Si interposer for higher design complexity, high-speed performance and manufacturing cost. LSI with low profile and low parasitic discrete components.
Products	Broadcom, Google TPU Nvidia Hopper GPU Biren Technology BR100	N.A.	N.A
SCHEMATIC			

Source: TSMC

TSMC ADVANCED PACKAGING - 2.5D INTERPOSER

Chip-on-Wafer-on-Substrate (CoWoS-S®) Timeline

2012
CoWoS integrated four 28nm chips, providing customers high-performance FPGA components with the shortest time-to-market.

Logic + Logic
1.25x Reticle
1070~ mm² Size

2014
Produced the world's first 16-nm three-chip integrated device with networking capabilities using CoWoS.

2015
Produced the world's first 16-nm three-chip integrated device with networking capabilities using CoWoS.

Increased the interposer size considerably by a two-mask stitching process.

2016
Integrated multiple, large advanced chips on a single CoWoS module and started volume production in the first half of 2016. Integrated HBM2 with 20nm, 16nm, 12nm and 7nm multi-chip structure and super-HPC chips.

Logic + Logic/HBM2
1.5x Reticle
1280~ mm² Size

2017
Logic + Logic/4HBM2
1.75x Reticle
~1500 mm² Size

2019
Logic + Logic/4HBM2
1.85x Reticle
~1590 mm² Size

2020
Developing 5nm CoWoS Advanced Packaging technology. TSMC will continue to provide complete Si-to-package business model for CoWoS manufacturing.

Logic+Logic/6HBM2E
2x Reticle
~1700 mm² Size

2021
5th generation CoWoS-S includes enhanced power integrity, high speed die to die interconnect, new TSV structure and a higher thermal conductivity thermal interface material (TIM).

Logic + Logic/8HBM2E
3x Reticle
~2500 mm² Size

2022
Logic + Logic/8HBM3
3.3x Reticle
~2750 mm² Size

KEY POINTERS:

TSMC CoWoS integrates advanced node SoC Logic and HBM for high-performance applications by 2.5D interposer.

Notice that 2.5D interposer size has steadily increased to envelope more dies from 2012 to 2021.

Future
TSMC has displayed its ambition further by projecting 4x and 6x reticle size interposers with CoWoS-L/R, housing a total of up to 12 HBM stacks.

TSMC ADVANCED PACKAGING: LSI (LOCAL SILICON INTERCONNECT)

CoWoS-L technology

In 2020, TSMC classified its embedded Si bridge technology – called LSI (local silicon interconnect) – under chip-last packages in CoWoS and InFO platforms.

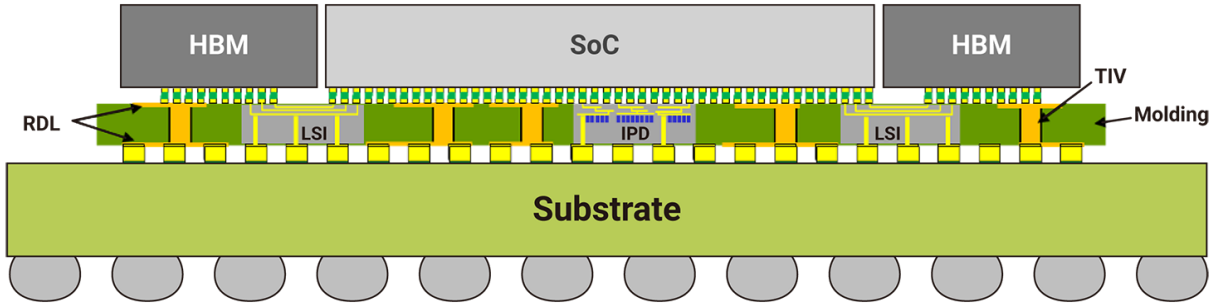
This combines the advantages of CoWoS-S and InFO technologies to provide the most flexible integration using an interposer with an LSI chip for die-to-die interconnect and RDL layers for power and signal delivery. The offering starts from a 1.5x-reticle interposer size with 1x SoC + 4x HBM cubes and will move forward to expand the envelope to larger sizes to integrate more chips.

TSMC plans to qualify CoWoS-L with 3.3x-reticle interposer for SoCs + 8 HBM3 in Q3-2023 and 4x-reticle interposer with 12 HBM3 in Q3-2024.

The key features of the **CoWoS®-L** service include:

- LSI chips for high routing density die-to-die interconnect through multiple layers of sub-micron Cu lines. The LSI chips feature a variety of connection architectures (e.g., SoC to SoC, SoC to chiplet, SoC to HBM, etc.) within each product and can also be used repeatedly for multiple products. The corresponding metal types, layer counts, and pitches align with the offering from CoWoS®-S.
- Molding-based interposers with a wide pitch of RDL layers on both the front-side and back-side and TIV (through interposer via) for signal and power delivery provide low loss of high-frequency signal in high-speed transmission.
- The capability of integrating additional elements, e.g., stand-alone IPD (integrated passive device), right underneath the SoC die to support its signal communication with better PI/SI.

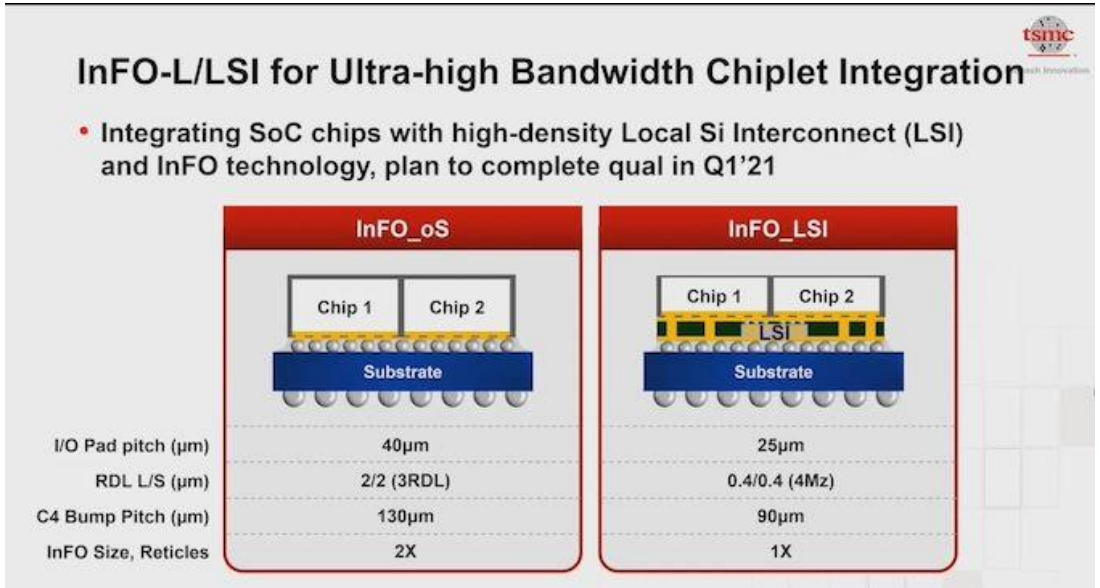
TSMC's CoWoS-L

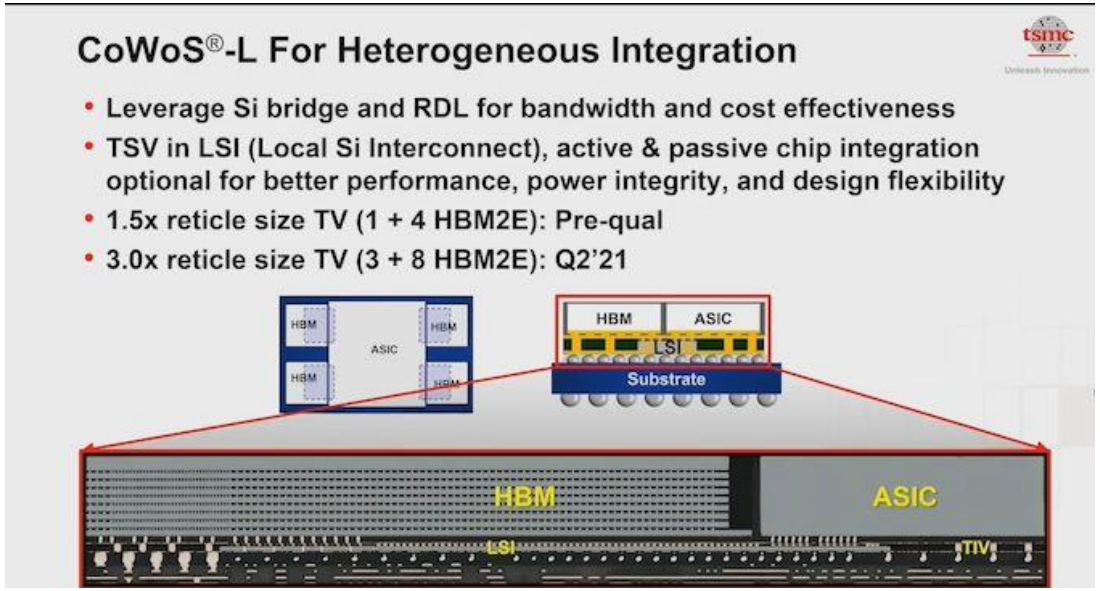


Source: TSMC

TSMC ADVANCED PACKAGING: LSI (LOCAL SILICON INTERCONNECT)

InFO-LSI and CoWoS-L technologies





Source: TSMC

TSMC's InFO integration with an LSI is called InFO-L or InFO-LSI and follows a similar structure – with the new addition of it integrating this new local silicon interconnect intermediary chip for communication between two chips.

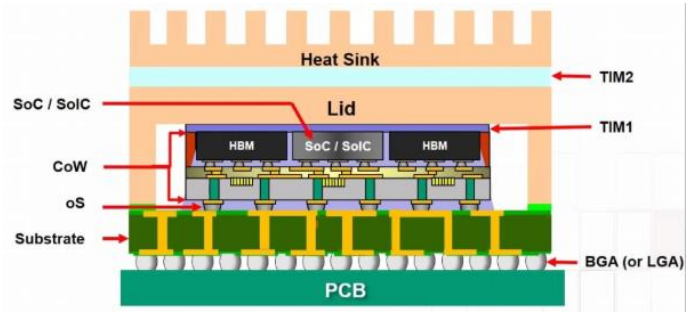
CoWoS-L is the new variant of TSMC's chip-last packaging technology. It adds in the LSI, which is used in combination with a copper RDL to achieve higher bandwidth than just an RDL packaging implementation (CoWoS-R) and will be more cost-effective than a full silicon interposer implementation (CoWoS-S).

TSMC describes the LSI as being either an active or a passive chip, depending on the chip designer's needs and cost sensitivities. LSI is expected to bring high-performance chip designs at a lower cost for the designer and the consumer.

TSMC ADVANCED PACKAGING – 3D SOIC

- TSMC's front-end 3D SoIC is a key technology pillar to advance the field of heterogeneous chiplet integration with reduced size and increased performance. It features ultra-high-density vertical stacking for high performance, low power, and minimal RLC (resistance-inductance-capacitance). SoIC integrates active and passive chips into a new integrated-SoC system, electrically identical to native SoC, to achieve a better form factor and performance. It is slated to go into mass production in 2021.
- SoIC is a “bumpless” interconnect method between multiple dies. Instead of solder bumps, SoIC uses Cu-Cu hybrid bonding. The SoIC solution enables known good dies of different sizes, process technologies, and materials to be stacked together directly.
- Compared to typical 3DIC solutions with micro-bumps, TSMC’s SoIC delivers higher bump density and speed while consuming much less power. What’s more, SoIC is a “front-end” integration solution connecting two or more dies before they are packaged. Therefore, a SoIC stack can be further integrated with other SoICs or chips in one of TSMC’s “back-end” Advanced Packaging technologies such as InFO or CoWoS, offering a powerful “3D-by-3D” system-level solution.

3DFabric building blocks



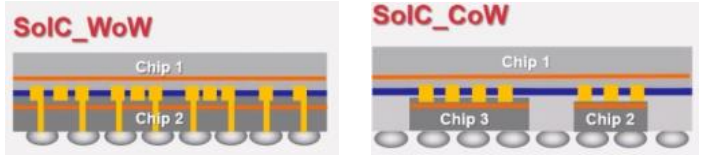
SoC/TSV
SoIC hybrid/Fusion Bond
Si, RDL, embedded Si/RDL interposers
Integrated IPDs/DTC
Mass reflow/LAB/TCB
Substrate
TIM & Thermal
PCB (BGA/LGA)

Path to SoIC: technical requirement

From Bump to SoIC

- Bonding alignment accuracy: 5-20 µm (bump) to <0.5 µm (bumpless)
- Bonding interface defect: 10 µm to <1 µm
  Topography: µm to nm
- CD/Pitch patterning: aligner/I-line to 248nm scatter
- Die warpage: 60-100 µm to 10-20 µm
  Stringent equipment capability & process control critical for high yield

Source: TSMC



GLOBAL UNICHIP CORP. (GUC) GLINK USING TSMC PACKAGING

GUC's new era of flagship SoC integrated by InFO and CoWoS

2020

GUC announced that it has successfully demonstrated the silicon-proven **GLink (GUC multi-die interLink)** interface product, using TSMC's 7nm process and InFO_oS advanced packaging technology for AI, HPC, and networking applications to do multi-die integration for system scaling. GLink uses both InFO and CoWoS packaging technologies: InFO_oS for modular, scalable, and high-yield multi-die ASICs; CoWoS for multi-die ASICs with HBM memory.

2021

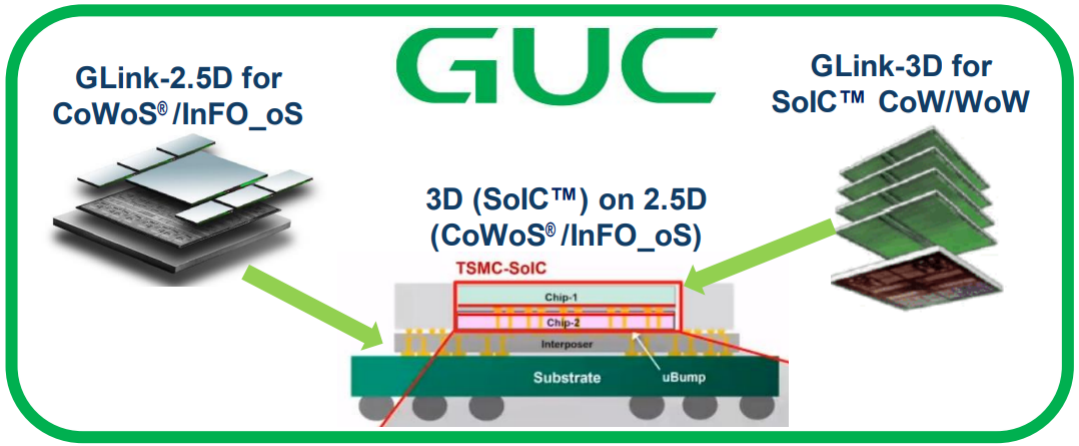
GLink 2.0 and Glink-2.5D based on InFO_oS and CoWoS are available. Customers are adopting GLink 2.0 for their next-generation products using TSMC's N5 and N6 and expect mass production to start in 2023.

GUC's **GLink-3D die-on-die interface IP** uses TSMC's N5 and N6 processes and 3DFabric™ advanced packaging technology. GLink-3D enables several 3D die stacks to be assembled using CoWoS® and InFO_oS, interconnected using Glink-2.5D links, and combined with HBM memory.

2022

GUC announces **2.5D and 3D Multi-Die Advanced Packaging Technology (APT) Platform** for AI, HPC, and Networking ASICs. The platform supports TSMC's CoWoS-S, CoWoS-R, CoWoS-L, InFO, and 3D-SoIC technologies. GUC provides a total solution: silicon-proven interface IPs, CoWoS® and InFO silicon-correlated design, signal, and power integrity, thermal simulation flows, and high-volume product-proven DFT, and production tests.

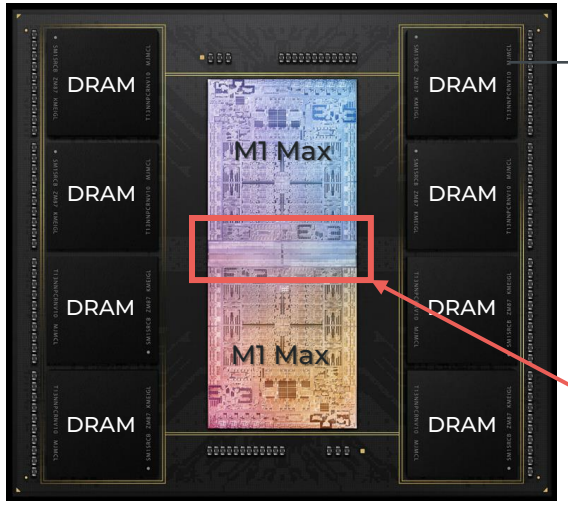
GUC announces the **GLink 2.3LL interface IP** for TSMC's CoWoS® and InFO chiplets integration platforms as the most efficient chiplet interface in the market.



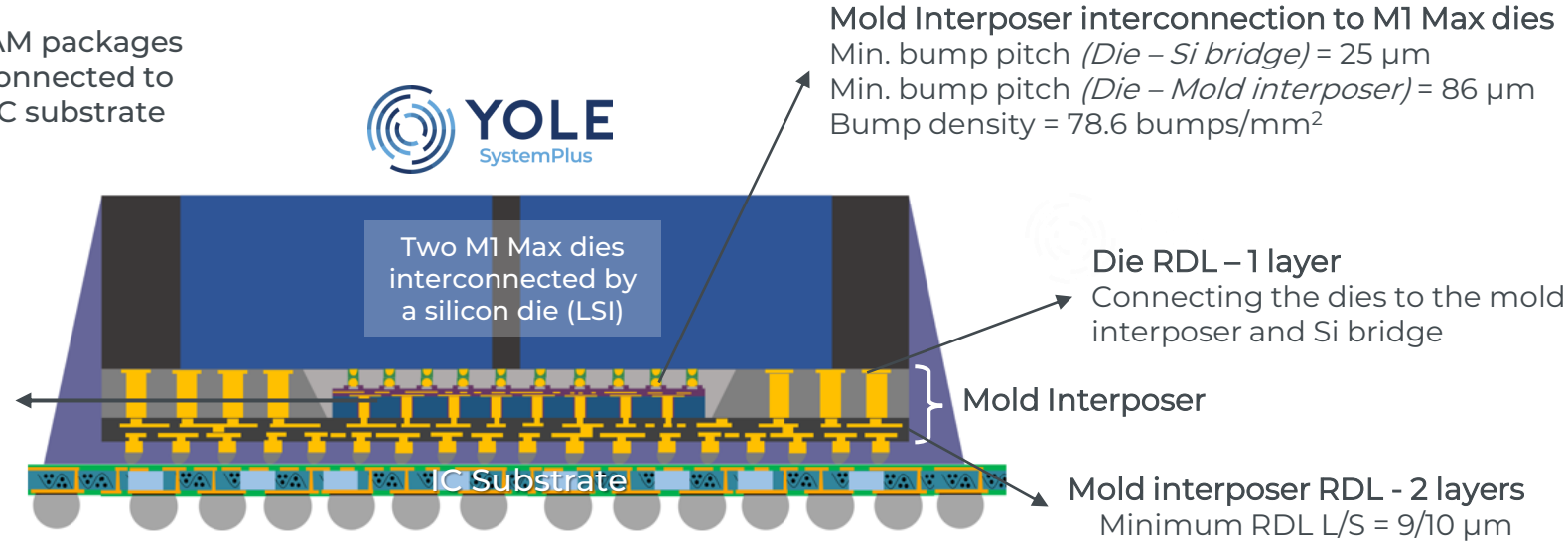
Source: Global Unichip Corp. (GUC)

TSMC INFO_LSI IN APPLE'S CHIP: M1 ULTRA
Fan-Out Si bridge for advanced PC applications

- In 2022, Apple released the M1 Ultra processor for its MacStudio desktop. The M1 Ultra combines two M1 Max dies interconnected using TSMC's InFO-L/LSI (Local Silicon Interconnect) packaging technology. The M1 Max was already designed with the interconnect circuitry at the bottom of the die, allowing it to interconnect two dies. The bump pitch is about 25 µm which corresponds to the LSI pitch.
- TSMC recently confirmed that Apple used its InFO_LSI packaging method to build its M1 Ultra processor and enable its UltraFusion chip-to-chip interconnect. Apple is thus the only company using TSMC's InFO_LSI technology so far and the first to adopt a Fan-Out Si Bridge package for a mobile and consumer application (in this case, for its desktop processor package).
- Apple's UltraFusion uses a silicon die to connect the chips, providing 2.5TB/s of low latency, inter-processor bandwidth.
- Apple's M2 Ultra and M3 chip will rely on TSMC's most advanced nodes (3 and 3E) and it is also expected to contain TSMC's Advanced Packaging Technology. The M2 Ultra chip will be probably released in Apple's Mac products (expected by H2 2023.)



M1 Ultra package featuring two M1 Max dies interconnected by a silicon die (LSI) and eight DRAM packages.
Source: Apple



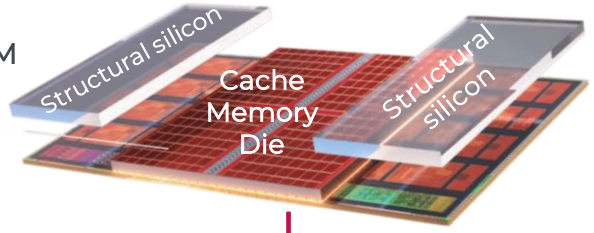
Scheme of Apple's M1 Ultra using TSMC InFO-L technology
Source: SPR22684 – Apple M1 Ultra SoC, Yole System Plus, 2022

TSMC 3D-SOIC IN AMD'S 3D V-CACHE TECHNOLOGY

AMD-TSMC teaming up: new processors and new V-Cache generations

AMD announced its third-generation AMD Epyc processor and its next-generation Ryzen, both using TSMC D2W hybrid bonding technology

3D V-Cache™ Technology

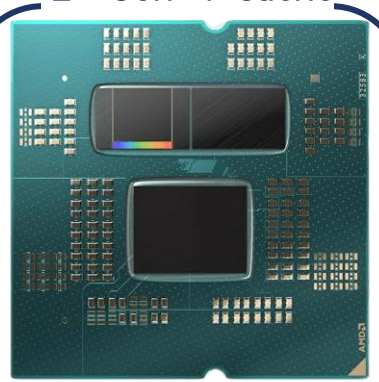


- >200X connection density compared to on-package 2D chiplet
- >15X interconnect density compared to microbump 3D
- > 3X interconnect energy efficiency compared to microbump 3D

1st Gen –V-Cache

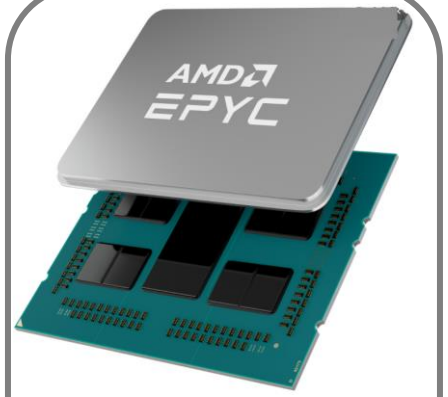
AMD Ryzen™ 7 5800X3D (Fastest in 2022)

2nd Gen –V-Cache



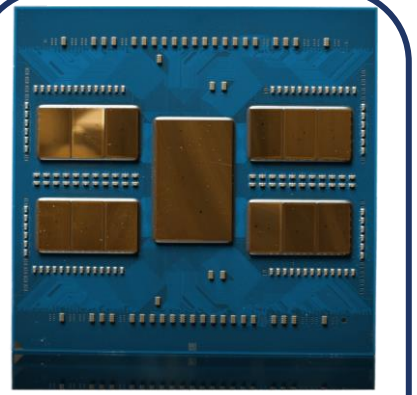
AMD Ryzen™ 9 7950X3D (Fastest gaming CPU in 2023)

1st Gen –V-Cache



AMD EPYC Gen 3 (Milan-X)

2nd Gen –V-Cache



AMD EPYC Gen 4 (Genoa)

Zen 3 architecture

Zen 4 architecture

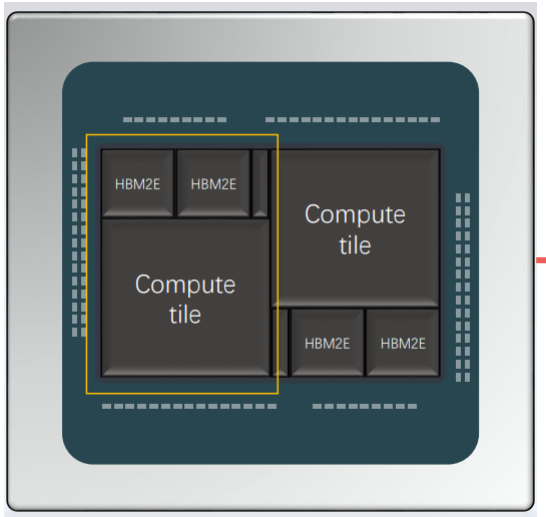
Source: AMD

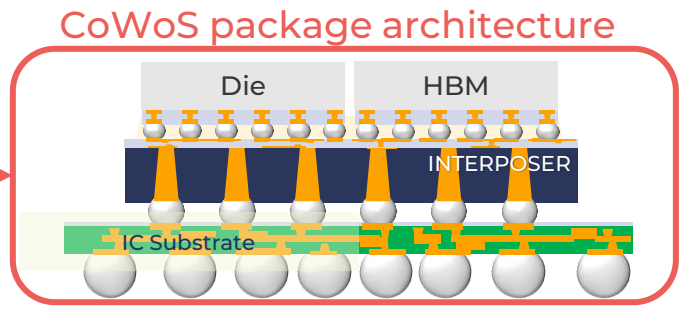
We expect a new generation of V-Cache technology by 2024 , for the Zen 5-architecture based CPUs, called «Granite Ridge», with TSMC 4 and 3 nm advanced nodes.

BIREN TECHNOLOGY BR100

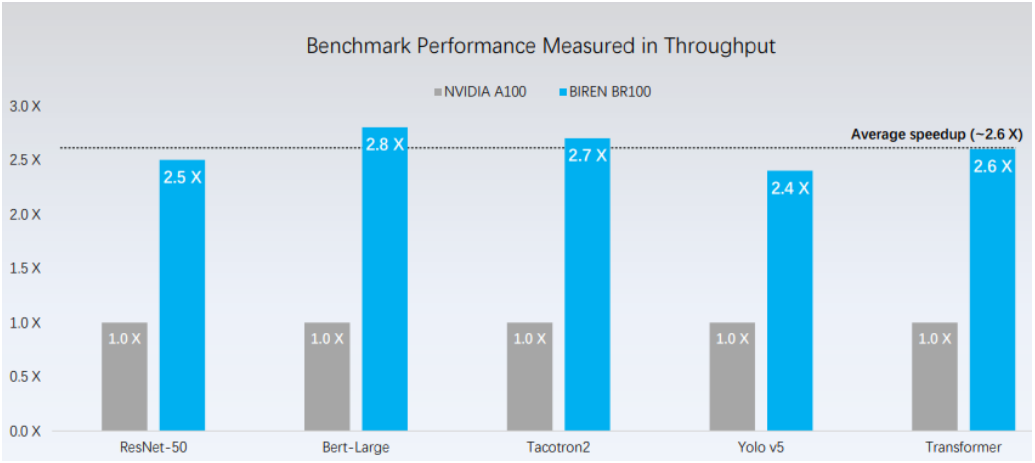
Chinese startup's general purpose GPU (GPGPU) using CoWoS technology from TSMC

- Announced in 2022 by Chinese enterprise BIREN Technology, BR100 is their first-generation general-purpose GPU which is dedicated to increasing productivity and lowering cost in AI training and inference in a data center.
- BR100 consists of 2 chiplets (dual die GPU) processed on TSMC 7nm node (77 billion transistors) and uses TMSC's CoWoS packaging technology (package area 1074mm^2) and comes with 4HBM2e memory up to 64GB. The die-to-die interconnect provides a high-speed bandwidth of 896 GB/s.
- Compared with a monolithic design, BR100 provides 30% more performance and 20% better yield. BIREN used Nvidia A100 as a benchmark for BR100 and it performed ~2.6X better over a range of benchmarks across domains including conversational AI, natural language processing, and computer vision compared to A100.





BR100 package overview with Compute tiles (GPU) and HBMs
Source: BIREN Technology

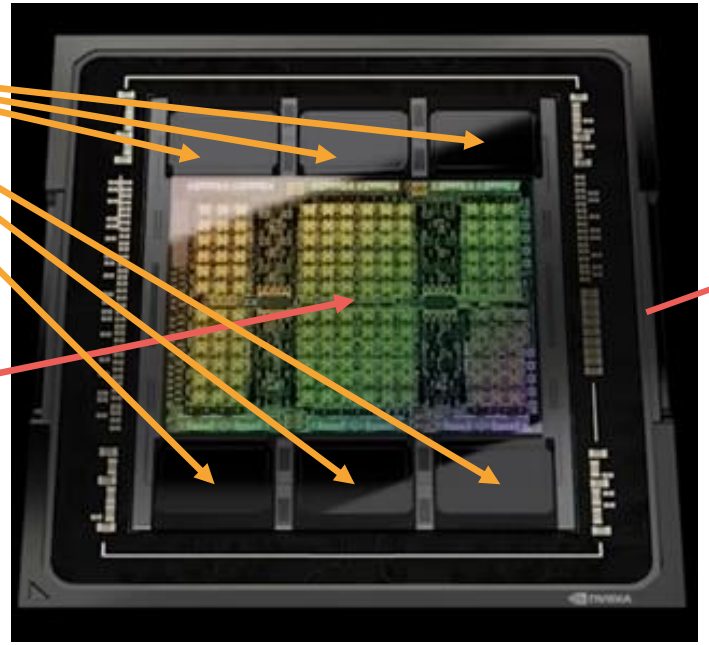


BIREN BR100 compared with NVIDIA A100 on various Accelerating Deep Learning Workload domains with BR100 performing ~2.6X better than A100
Source: BIREN Technology

NVIDIA H100
CoWoS-S technology from TSMC

NVIDIA released its Hopper Tensor Core GPU in 2022. It uses a Si Interposer for its package to interconnect the GPU (4N from TSMC) with 6 HBMs leveraging CoWoS-S technology from TSMC. It is the first ever product on the market to use HBM3 offering two times more DRAM bandwidth than its predecessor A100. The Hopper GPU is paired with the Grace CPU using NVIDIA's ultra-fast chip-to-chip interconnect, delivering 900GB/s of bandwidth, 7X faster than PCIe Gen5. This innovative design will deliver up to ten times higher performance for applications running terabytes of data for HPC, AI, and gaming markets. **A System + Consulting teardown of this product will be available at the beginning of Q3 2023.**

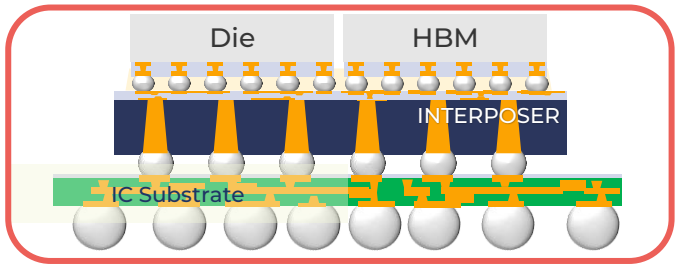
- **6 HBMs**
  - HBM3
  - 4.9 TB/s
  - SK Hynix
  - Samsung
- **GPU**
  - TSMC 4N
  - 80B transistors

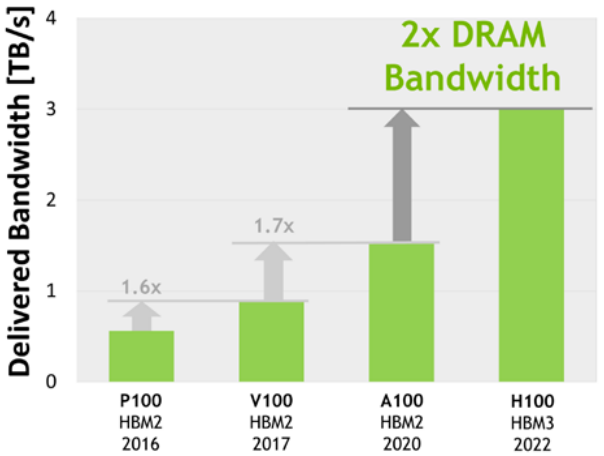


Nvidia H100 package top view
Source: Nvidia

Yole SystemPlus tear down available on this product

CoWoS package architecture





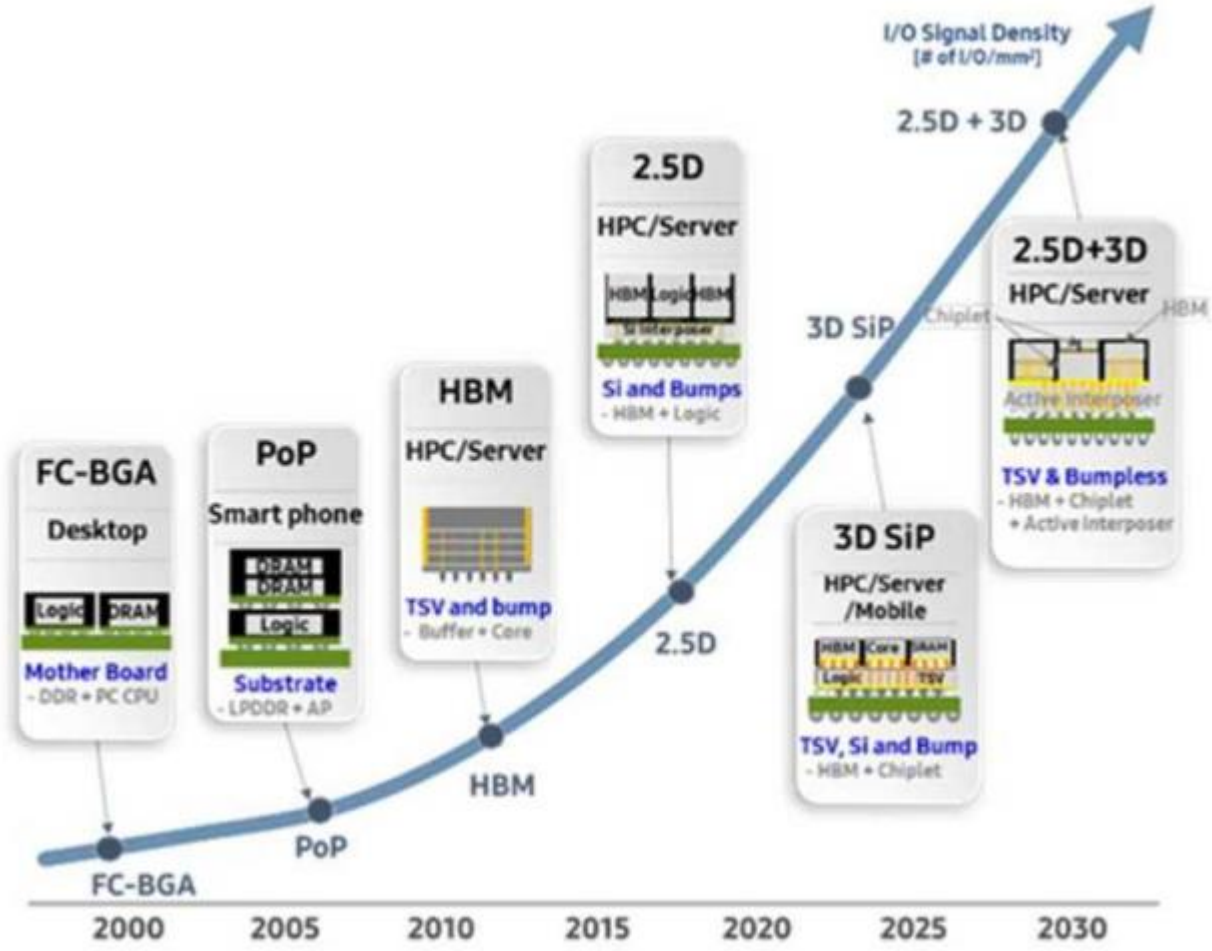
Memory bandwidth of Nvidia P100, V100, A100 & H100
Source: Nvidia

Technology Trends: Focus on Samsung

SAMSUNG'S ADVANCED PACKAGING TECHNOLOGY ROADMAP

Packaging technology evolution

With ambitious investments and a roadmap, Samsung aims to create innovative products using advanced packaging technology that goes beyond the limitations of semiconductors. Samsung plans to provide competitive package products for high-performance computing and artificial intelligence using high bandwidth memory (HBMs) through heterogeneous integration technology. Samsung will focus on developing next-generation 2.5-dimensional and 3-dimensional advanced package solutions based on redistribution layer (RDL), silicon interposer/bridge, and through-silicon-via (TSV) stacking technology. Samsung is leading the way in developing convergence package technology to overcome existing technological limitations. Samsung plans to mass-produce X-Cube (μ-Bump) and bump-less type X-Cube in 2024 and 2026, respectively and aims to develop more advanced packaging solutions that will revolutionize the semiconductor industry.



Source: "Advanced Package FAB Solutions (APFS) for Chiplet Integration", 2022 IEDM

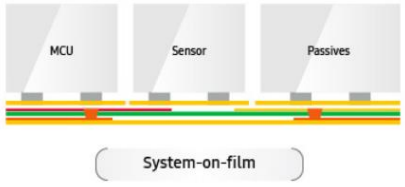
SAMSUNG ADVANCED PACKAGING TECHNOLOGY

Samsung has over 25 years of packaging experience, from memory to logic devices. The company aggressively invests in AP technology to boost its foundry business and emerge as a strong alternative to TSMC. Samsung and TSMC are the two foundries remaining engaged in cutting-edge front-end manufacturing, although Intel is hoping to catch up by 2024 with an aggressive technology roadmap toward their IFS business. Samsung Electronics is stepping up its game by strengthening the synergy between semiconductors and packaging. Samsung Foundry leads the way in packaging technology development with many innovations introduced into Samsung devices.

Samsung has pioneered the development of Advanced Packaging technologies in the past: the world's first TSV HVM for 3D memory, TSV SiP development for mobile APs, highest capacity NAND flash memory stacking technologies for SSDs, etc.

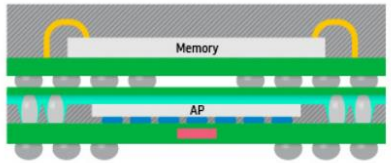
Samsung's AP platforms

Mobile/5G/Automotive
(Form factor, thermal, speed, memory B/W, reliability)

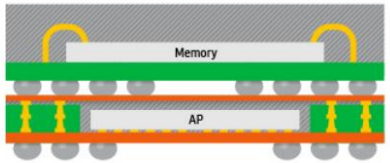


System-on-film

FOSiP

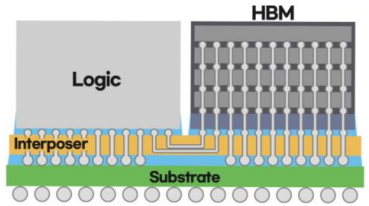


iPoP

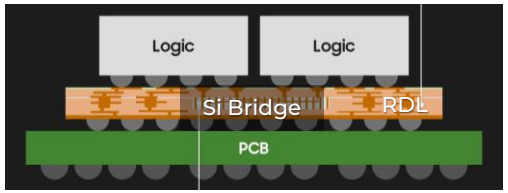


FOPLP-PoP

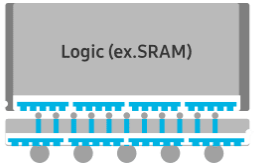
AI/Server/HPC
(Memory B/W, density, large size, high performance)



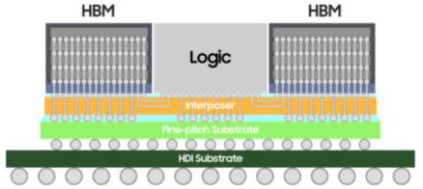
I-CubeS (2.5D Si-Interposer)



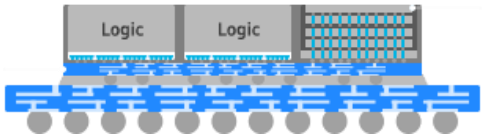
I-CubeE (2.5D Si bridge Interposer)



X-Cube (3DIC Logic Interposer)



H-Cube (Hybrid Interposer)



R-Cube (2.5D RDL Interposer)

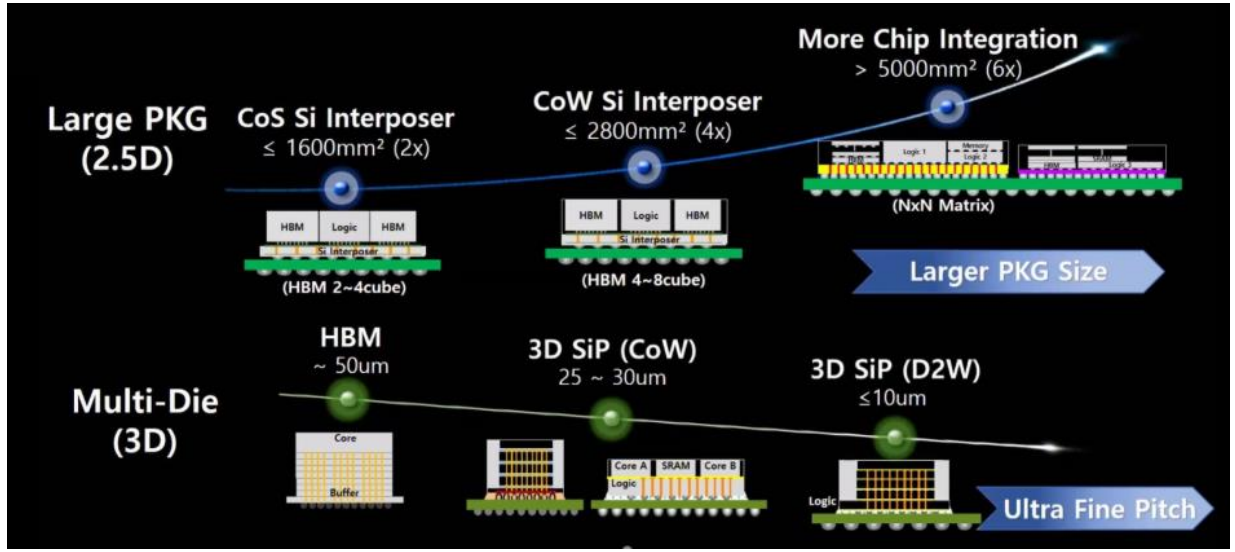
Source: Samsung

SAMSUNG ADVANCED PACKAGING TECHNOLOGY

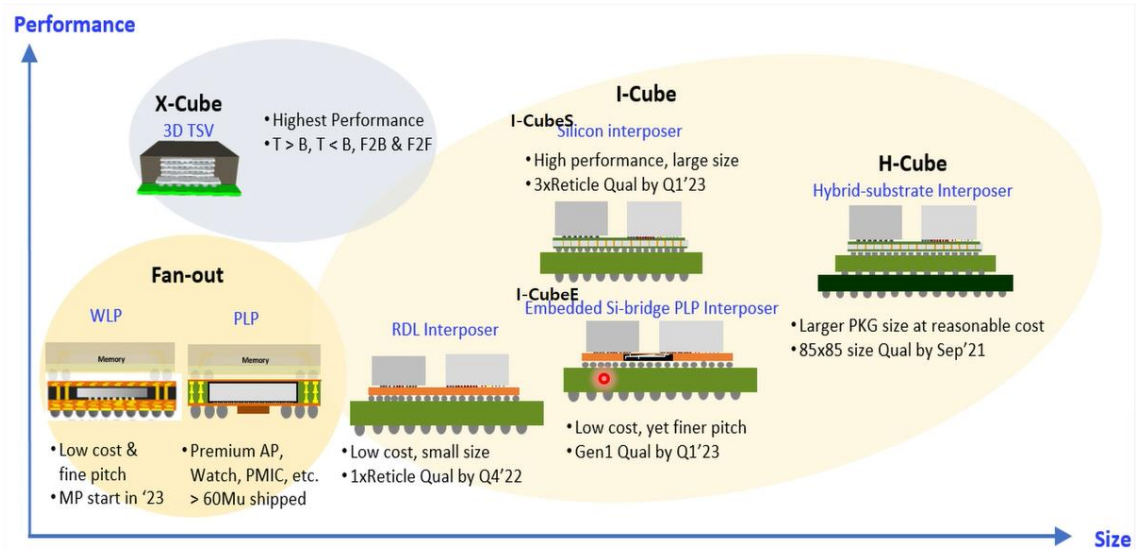
Recent developments

- Samsung Electronics invested in HD fan-out technology by acquiring the PLP line from SEMCO in 2019 for ~$750M to compete with TSMC for Apple's APU FE die and packaging business. Currently used for integrated APU package in Galaxy watch, the plan is to extend it to smartphone applications.
- Samsung has developed lower-cost RDL interposer cube technology (I-Cube™) to support higher memory bandwidth requirements in AI, HPC, networking & high-end graphics where the xPUs are integrated with HBM. Baidu's Kunlun AI chip uses Samsung's proven 14 nm process technology and makes use of the RDL interposer-Cube 2.5D packaging structure. The Baidu Kunlun AI accelerator is based on the company's XPU neural processor architecture that uses thousands of small cores that can be used for a wide variety of applications in the cloud and on the edge of AI processing. The chip provides up to 260 TOPS at 150 W and features 512 GB/s memory bandwidth using two HBM2 memory packages.

Samsung's package integration solution for AI/HPC/Server Platform



Samsung's CUBE series for heterogeneous integration



Source: Samsung

SAMSUNG ADVANCED PACKAGING TECHNOLOGY - 3D SOC

Samsung Electronics has started to develop devices that use hybrid bonding technology. One of the main objectives is to enhance the stacking capacity and reduce the pitch between connections by getting rid of TSVs. Applications are positioned for AI, cloud, mobile, and wearable.

Source: "Integrated Packaging Technologies for High-Performance Computing Systems: Challenges and Opportunities," IMAPS Keynote, Samsung Foundry

SAMSUNG'S 'BEYOND MOORE' APPROACH

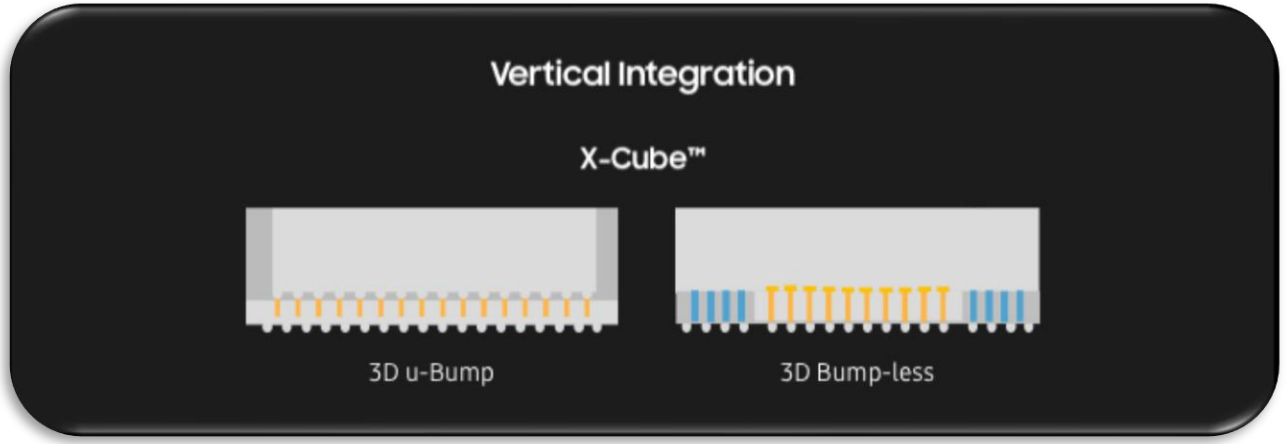
Advancements in Heterogeneous Integration

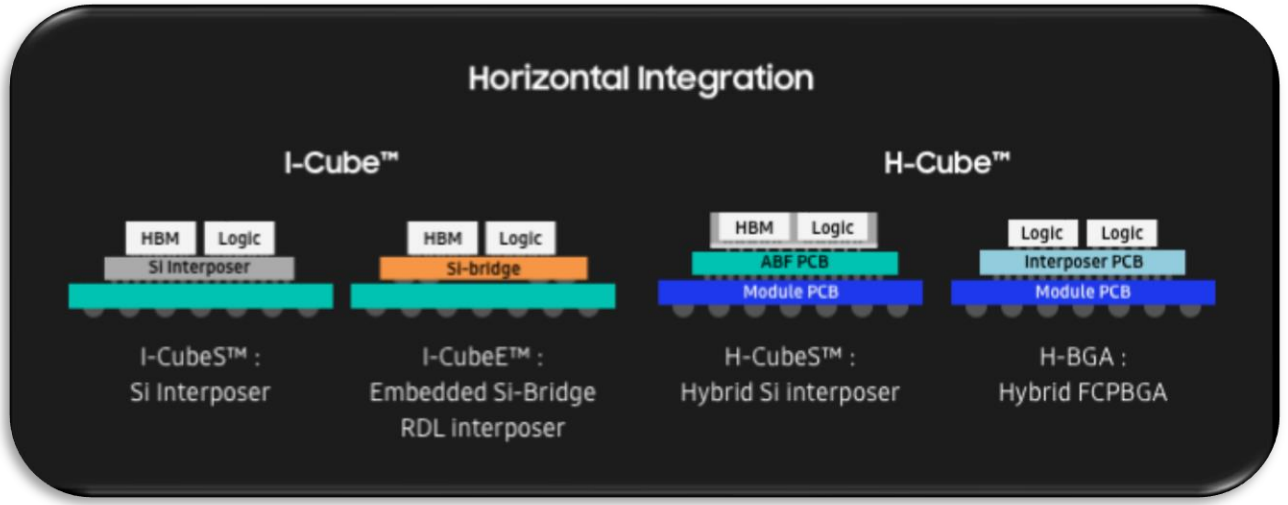
Samsung is pursuing a 'Beyond Moore' approach to chip development through advanced heterogeneous integration. It has developed three advanced package technologies, called I-Cube, H-Cube, and X-Cube,

X-Cube: a 3D solution for vertically stacking chips, will be available in two forms: with micro-bump (2024) and bump-less type (2026). The company's Cube solutions will offer flexible architecture to meet diverse customer needs and applications.

I-Cube is a 2.5D solution that satisfies customer demands for larger interposers, with I-CubeS offering an interposer made of silicon to carry eight HBMs and two logic dies, while I-CubeE provides a more cost-effective option and is expected to integrate up to 12 HBMs for mass production by 2025.

H-Cube: a 2.5D solution that converts a large ABF substrate into a combination of smaller ABF and FCBGA substrates and a larger HDI substrate. It is designed to address the industry's shortage of printed circuit boards (PCBs) while providing advanced PCB solutions at lower PKG cost and a better PCB supply chain.





Source: Samsung

SAMSUNG 2.5D/3D TECHNOLOGY SUMMARY

SAMSUNG

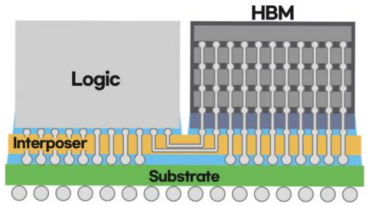
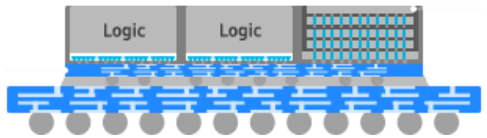
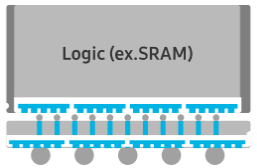
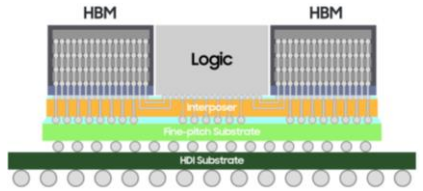
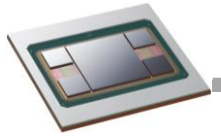
	I-Cube	R-Cube	X-Cube	H-Cube
Technology				
	2.5D Si-Interposer	2.5D RDL Interposer	3D Logic Interposer	3D Hybrid Interposer
Integration	CoS or CoW Si interposer + TSV	Logic to logic and logic with HBM modules + TSV less	CoW + WoW Si interposer + TSV	Low-cost package with Interposer, fine-pitch substrate and a module substrate
	• 4HBM • 1 logic	• 4 HBM • 2 logic	• 7LPP Logic die • 7LPP SRAM die	• 6 HBM Modules • 1 logic
Benefits	• Fine pitch • CoS: Low-cost with interim test • ISC, MIM in Si Interpower • CoW: More HBM modules	• Low cost • Fast turn-around-time • Greater design flexibility • TSV-less • Better signal and power integrity	• Higher density integration • Lower latency • Solder CoW • Greater scaling in size • Higher bandwidth	• Cost effective • Greater scaling in size • Larger package size • Greater integration flexibility

Image Source: Samsung

SAMSUNG ADVANCED PACKAGING ARCHITECTURES

SAMSUNG

Samsung is focusing on developing high-performance system packages with high bandwidth and fine interconnection while ensuring cost-effectiveness and reliability



I-Cube (2.5D)

1-HBM Si Interposer (2017)

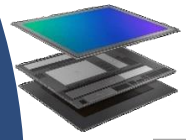
4-HBM Si Interposer (2019)

2-HBM Si Interposer MP (2020)

8-HBM Si Interposer (2020)

4-HBM Organic Interposer (2020)

I-CubeE Si Bridge Organic Interposer



X-Cube (3D)

3D CIS MP (2018)

3D SiP "X-Cube" (2020)

4-Stack DDR4 MP (2014)

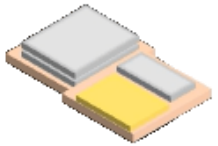
4-Stack HBM MP (2016)

8-Stack HBM MP (2018)

8-Stack DDR5 MP (2022)

12-Stack HBM MP (2023)

3.5D



3.5D SiP

FO

Wearable AP MP (2018)

Flagship AP (2020)

Flagship AP MP (2022)

2014 2016 2018 2020 2022 2024

I-Cube 2.5D

I-CubeS Si Interposer

I-CubeE 2.xD Si Bridge

X-Cube 3D

TCB

Hybrid Cu Bonding

Wafer on Wafer

3.5D

FOPKG

PLP

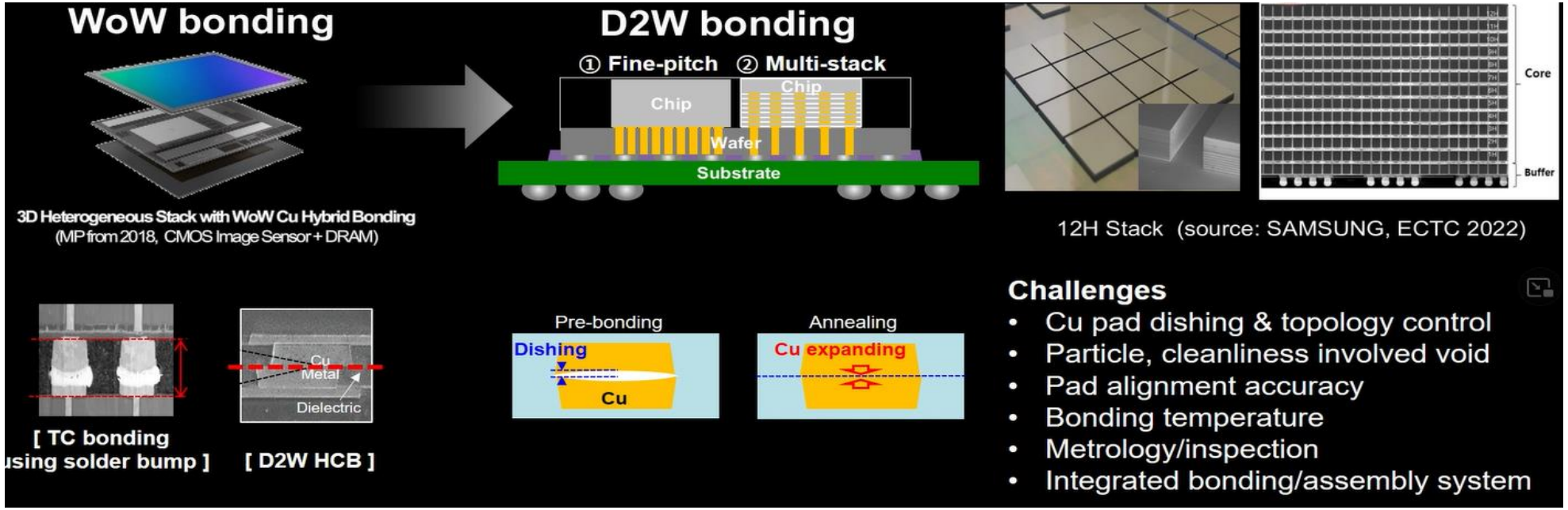
WLP

Source: "Advanced Package FAB Solutions (APFS) for Chiplet Integration", 2022 IEDM

X-CUBE : BUMPLESS – D2W HYBRID BONDING

SAMSUNG

Samsung's advanced packaging solutions feature hybrid bonding technology, which is being extended from W-2-W to D-2-W. This is crucial for the development of highly integrated 3D chiplets and HI.



Source: "Advanced Package FAB Solutions(APFS) for Chiplet Integration", 2022 IEDM

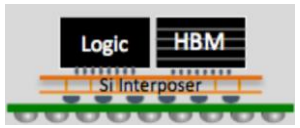
X-Cube 1st Gen			X-Cube 2nd Gen
µBump			Bumpless
7nm TSV	5-4nm TSV PDK		4-3 nm TSV
TSV-middle	TSV-Last		
Face-2-Back	Face-2-Face		
Bigger Bottom die		Bigger Top Die	
40 µm	25 µm	25 µm	
			

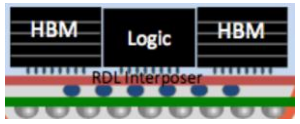
Source: Samsung

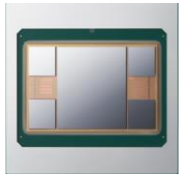
I-CubeS: 2.5D SILICON INTERPOSER

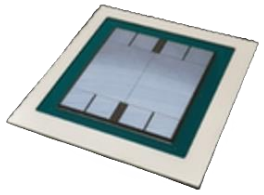
SAMSUNG

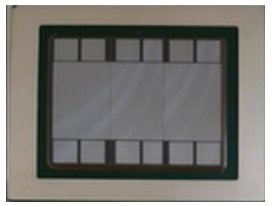
Characteristics	1st Gen (I-Cube2)	2nd Gen (I-Cube4)	3rd Gen (I-Cube6)	4th Gen (I-Cube8)	5th Gen
# of HBM	1xHBM	2xHBM	4xHBM	8xHBM	12xHBM
PKG area (mm²)	1806	2500	4225	7225	> 7225
Interposer area (mm²)	530	830	1500	2800	> 3200 (x4 recticle size)
Production status	HVM	HVM	Planned	Planned	R&D
Year	2017	2019	2020	2022	2024









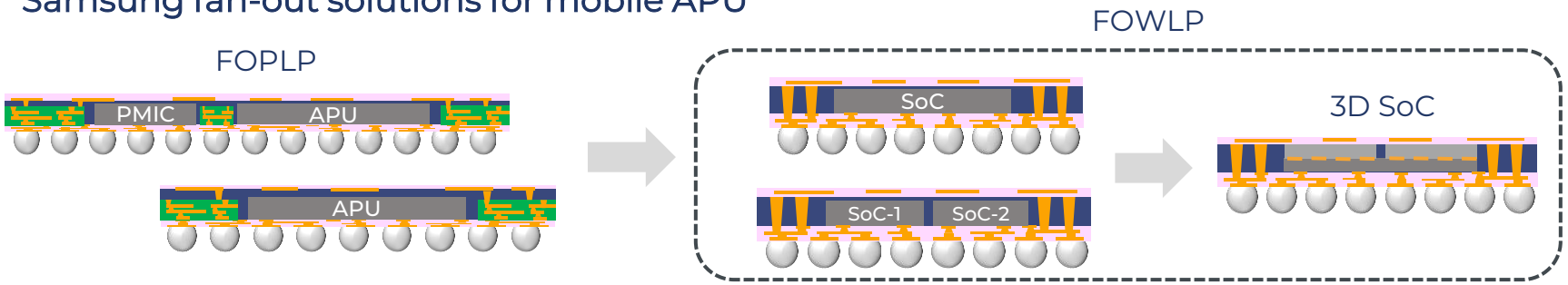


Using bigger packages and larger interposers has not only facilitated the integration of more High Bandwidth Memory (HBM) but also opened up possibilities for the development of new generations (6th Gen) of this technology with even greater levels of integration and performance enabled by ever-increasing bandwidth.

Source: Samsung

SAMSUNG FAN-OUT PACKAGE ROADMAP

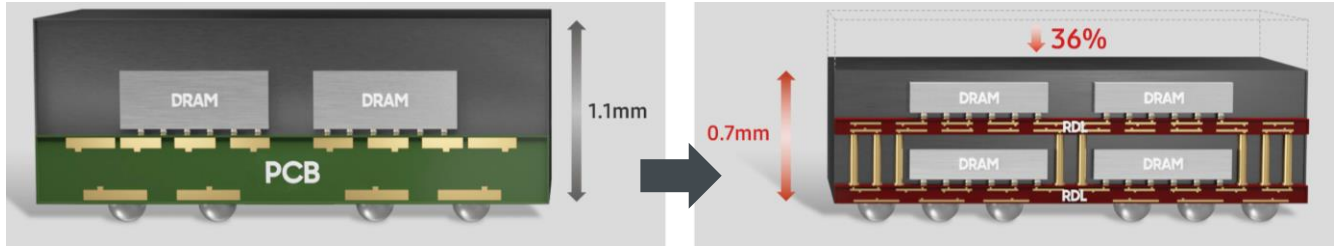
Samsung fan-out solutions for mobile APU



One possibility for Samsung is to develop FOWLP PoP solutions to compete with TSMC's InFO_PoP. In the future, chiplets might become a reality in the APU ecosystem, and hybrid bonding might be adopted. Samsung will explore that solution also to compete with TSMC 3D SoIC technology

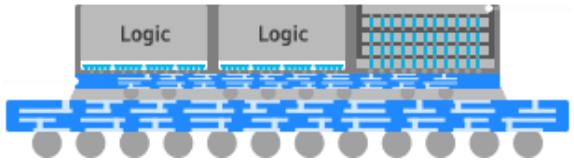
Samsung fan-out solutions for DRAM

Samsung will adopt FOWLP PoP technology for its graphics DRAM – GDDR6W – which should go into laptops by 2024-2025.



Source: Samsung

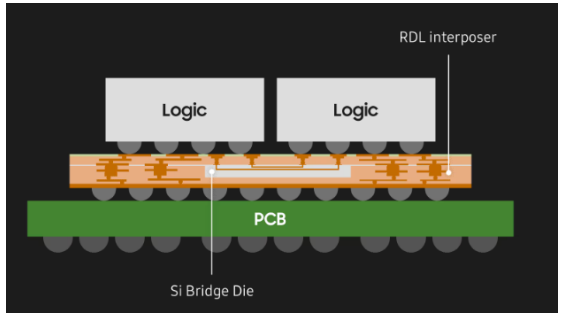
Samsung fan-out solutions for HPC / AI / Networking



Source: Samsung

R-CUBE

R-Cube is Samsung's RDL Interposer technology.
The packaging architecture enables the connection of logic-to-logic and logic to HBM modules with a high-density RDL interposer.



I-Cube E

The I-Cube E has an embedded Si structure which combines the advantages of Si bridge with fine patterning and RDL interposer with TSV-less structure and large interposer size by applying PLP.

Source: Samsung

Technology Trends: Focus on Intel

INTEL'S ADVANCED PACKAGING ROADMAP 2022

In 2021, Intel CEO Pat Gelsinger communicated his vision of "IDM 2.0", a significant evolution of Intel's IDM business model that includes huge manufacturing expansion plans and the establishment of the Intel Foundry Services (IFS) new business unit. Packaging is a crucial component of Intel's new IDM 2.0 strategy as its IFS business aims to be a combination of leading-edge process technology and Advanced Packaging.

Intel continues to advance in a chiplet-based architecture approach by using EMIB, Foveros & Co-EMIB architectures as a toolkit for the future. Ponte Vecchio will be the first Co-EMIB solution to access the market.

Enlarging its Advanced Packaging toolbox, Intel announced two other new technologies which are extensions of Foveros architecture: Foveros Omni and Direct. Foveros Omni should be available for volume manufacturing in 2023. Foveros Direct is also expected to arrive on the market in 2023 and will be Intel's first 3D SoC solution using hybrid bonding interconnect.

	Standard PKG	EMIB	Foveros	Foveros Omni	Foveros Direct
Bump pitch µm)	100	55-45	50-25	25	<10
Bump density	100/mm²	330-772/mm²	>400-1600/mm²	1600/mm²	>10000/mm²
Power (pJ/bit)	1.7	0.5	0.15	<0.15	>0.05

Source: Intel Accelerated 2021 Event

Foveros Omni will be probably delayed or cancelled

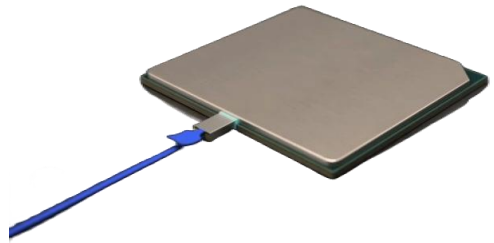
INTEL'S PACKAGING TECHNOLOGY

New technologies on the roadmap

Foveros Direct

- > 10x higher Interconenct Bump Density compared to Foveros.
- Higher Bandwidth at lower latency, power, and Die area.
- Foveros Direct will increase this lead to around x16 against the 1st Foveros.
-

Manufacturing in 2023 H2

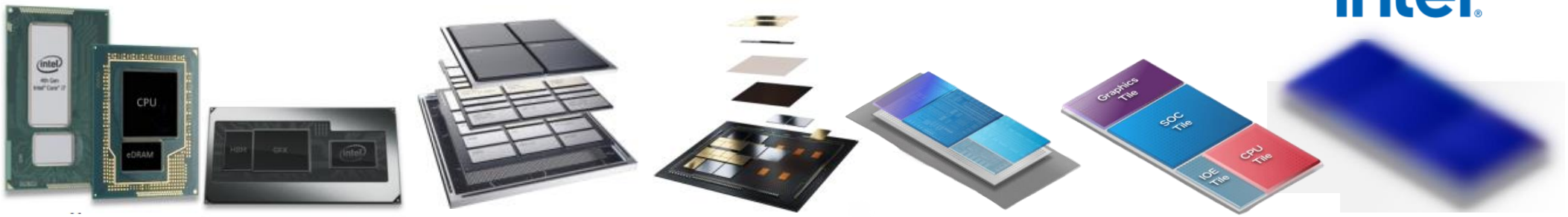


Pluggable optical

Intel unveiled "pluggable Optical", which is a smaller connector designed to connect directly to chip packages. This new pluggable form factor for co-packaged optics will be a game-changer in the world of silicon photonics. The new solution is a photonic integrated circuit and an electronic integrated circuit together on the XPU package, handling on-package electrical signaling to photonics. This package is apparently more akin to a specialized multi-fiber connector.

By 2025

INTEL'S DISAGGREGATION TIMELINE



	Haswell	Kaby Lake G	Lakefield	Ponte Vecchio	Meteor Lake	Arrow Lake	Lunar Lake
	2014	2017	2019	2022	2023	2024	2025
Packaging platform	2D MCP	2.5D+2D EMIB + MCP	3D 50 µm Foveros	2.5D/3D EMIB + Foveros	3D Foveros direct (36µm)	3D Foveros direct (36µm)	3D Foveros Next Gen (25 µm)
Technology process node	22 nm	14 nm	10 nm	Intel 7 nm TSMC N7/N5	Intel 4	Intel 20A	Intel 18A
Architecture	CPU/PCH/memory partionning	CPU/GFX partioning	Hybrid architecture CPU/PCH	47 tiles Compute/mem/ IO partioning	/	/	/

Source: Intel

Analyst's point of view

Reaching Intel's aggressive roadmap amid financial strain and product delays presents significant challenges. The delayed products could impact Intel's competitiveness, as it's pushed back to 2025. The plan to achieve five nodes in four years requires substantial investments, including building and equipping clean rooms. Balancing financial constraints, technological advancements, and catching up with competitors will be complex. Intel must manage resources, prioritize wisely, and execute effectively to remain competitive.

INTEL ADVANCED PACKAGING TECHNOLOGY: EMIB

EMIB (Embedded Multi-Die Interconnect Bridge) was developed by Intel as an alternative to Si interposer (e.g., CoWoS from TSMC).

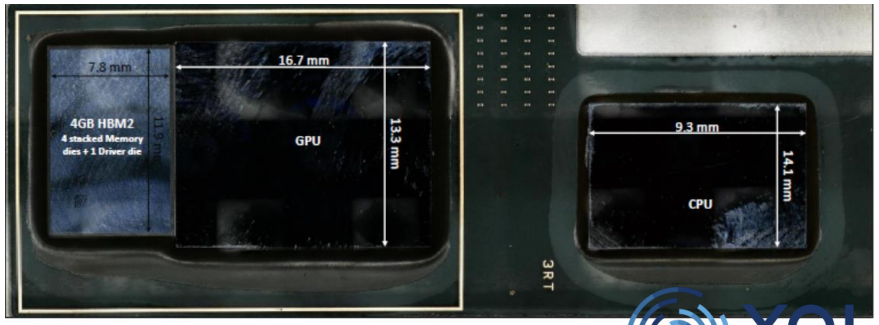
EMIB	Si interposer
• Localized high-density wiring • No practical limits to die size • Flexible : Allows bridge mix and match • Standard assembly process • Bridge manufacturing much simpler • Bridge silicon costs < Silicon interposer –No TSVs, significantly less silicon area • Increases organic substrate manufacturing complexity	• CTE Matched with Si : Low stress on low-K inner layer dielectrics • Excellent chip-attach alignment • Pitch scaling • Interposer size is typically limited by reticle field : active efforts in place to develop larger than reticle interposers • TSV capacitance impacts off-package signal integrity • Interposer attach adds an extra chip attach step

Applications

- FPGA + HBM (e.g., Stratix)
- FPGA + XCVR (Stratix 10)
- GPU+ HBM (As in Core i7-8809)

Future:

- ASIC + HBM
- Die partitioning (FPGAs, networking) - homogeneous integration
- Any other application where Si interposer is used.

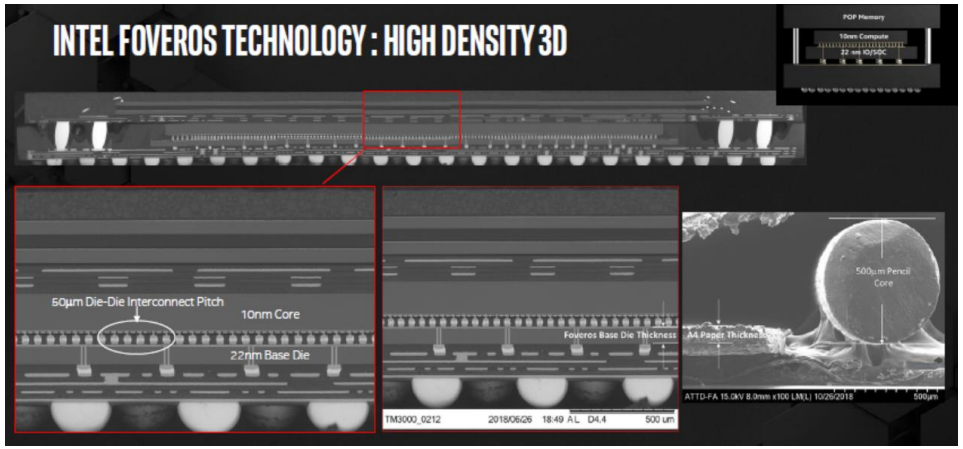


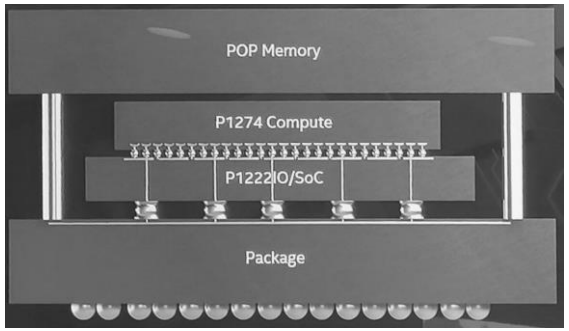
Sapphire Rapids will be the first product to ship in volume with EMIB. The next-generation EMIB will scale from 55 to 45µm pitch and be used on a 92 x 92 mm package – the world's biggest BGA package. The following generation is expected to be scaled to a 40 µm pitch.

INTEL ADVANCED PACKAGING TECHNOLOGY: **FOVEROS**

- Foveros 3D packaging is Intel's active interposer technology, designed as a step above its own EMIB design for either small form-factor implementations or those with extreme memory bandwidth requirements. It integrates low-power I/O and power delivery functions in an "active" Si interposer, and a high-performance compute logic die is stacked on top. For these designs, the power per bit of data transferred is extremely low, though the packaging technology must deal with the decreased bump pitch, the increased bump density, and the chip stacking technology.
- The active interposer contains the through-silicon vias and traces required to bring power and data to the chips on top, but the interposer also carries the PCH or IO of the platform. It is a fully working PCH, but with vias to allow chips to be connected on top. Current products use a core logic die with 10nm, and a base I/O die with 22 nm (acts as an active interposer with TSV).
- **Die-to-die interconnect pitch**: 50µm (current). Future: 20-35µm.
- **Applications**: Low-power applications. Mobile/tablet/phablet SoC using chiplet approach. Some products that debuted in the market in 2020 using Intel's Lakefield with Foveros package are Samsung Galaxy Book S, Microsoft Surface Neo, and ThinkPad X1. Xe-HPC architecture-based GPU for HPC in 2021. Intel is developing a 5G Modem SoC in partnership with MediaTek using Foveros technology.
- Intel's new product Meteor Lake will use Foveros technology and be done at a 36 µm bump pitch. It will be shipped starting in 2023.

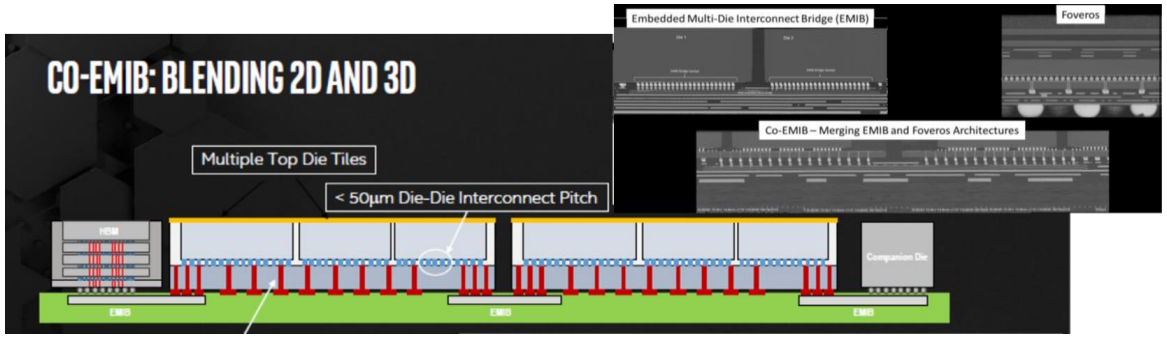
Source: Intel





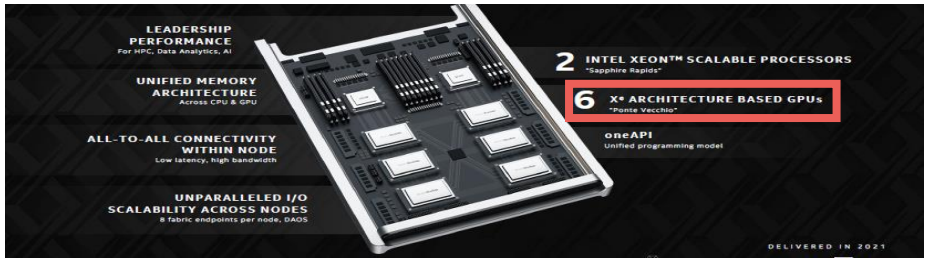
INTEL ADVANCED PACKAGING TECHNOLOGY: CO-EMIB

- **Co-EMIB** is the merging of Foveros & EMIB architectures. Co-EMIB technology links even more computing performance and capability together. It allows for the interconnection of two or more Foveros elements with essentially the performance of a single chip. Designers can also connect analog, memory, and other tiles with very high bandwidth and at very low power using Co-EMIB. The architecture enables a reticle-sized base die, and the EMIB bridge links two active interposers (base dies of Foveros) and an active interposer with other heterogeneous dies (e.g., HBM, XTVRs, etc.). Die-to-die interconnect pitch: below 50µm and in future to go to 10/20µm.

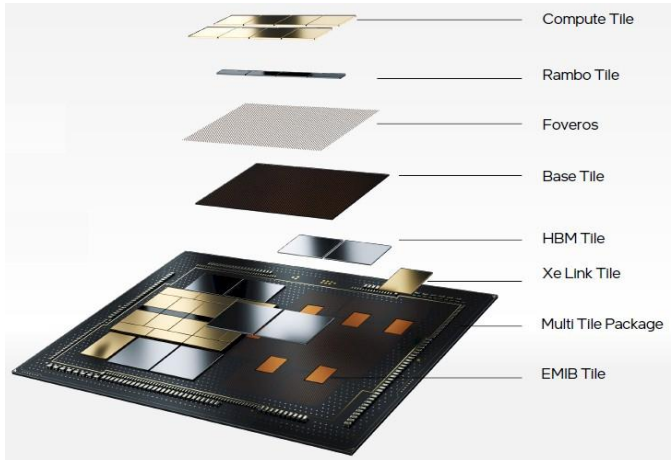


- Transition from solder to non-solder (Cu) based interconnect. Uses die-to-wafer hybrid bonding. Answer to TSMC's SoIC technology.

Intel's Xe Graphics "Ponte Vecchio" Architecture using Co-EMIB



Intel's first 'Exascale class' graphics solution using both chiplet technology (based on 7nm) and Foveros/die stacking packaging methods. Ponte Vecchio will also use EMIB technology, joining chiplets together.



Package specs

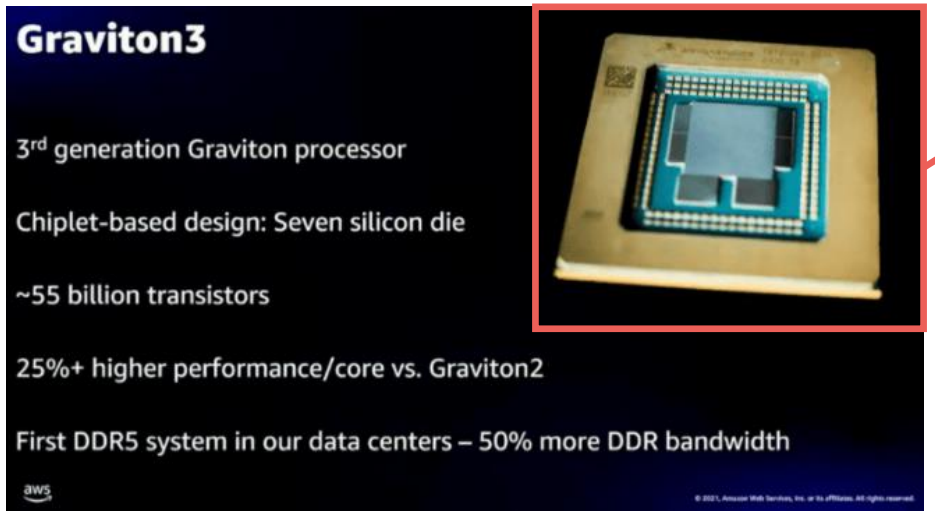
- D2D pitch ~36um
- Active top die count per stack ~ 16
- Max active top die size ~41mm^2
- Base die size ~650mm^2
- EMIB pitch ~55um
- Memory: 8 HBM 2E
- Package size: 77.5mm x 62.5mm
- # EMIB ~11

INTEL EMIB IN AMAZON'S GRAVITON3

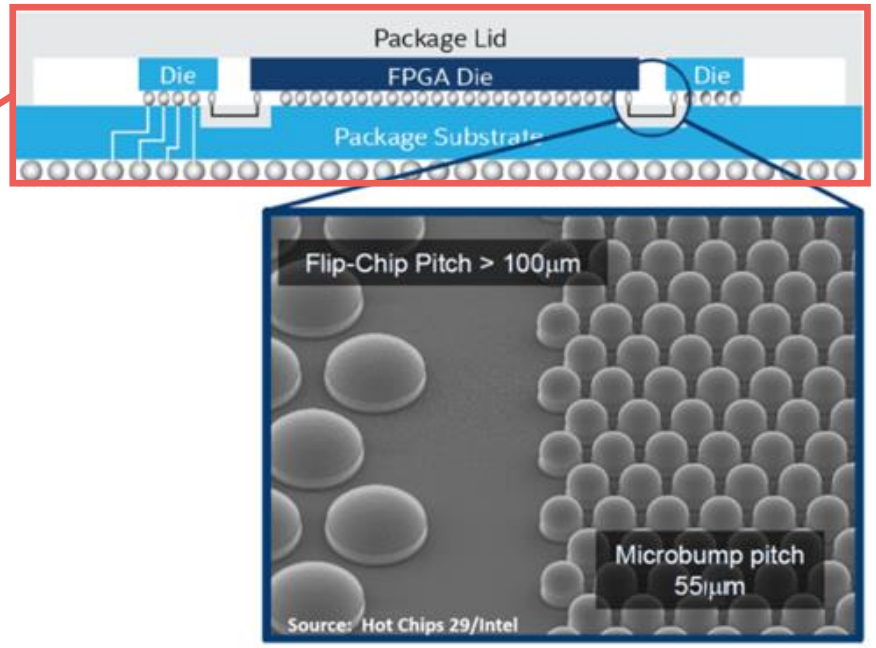
Is Amazon's AWS the first EMIB packaging customer of Intel Foundry Services?

It was announced at Intel Accelerated event in July 2021 that Amazon would be one of Intel Foundry Services (IFS) first customers, specifically for packaging.

Amazon launched its Graviton3 data center processor during its AWS, from November 30 - December 3, 2021. Gravitron3 is a chiplet product with seven dies and a total of 55 Bn transistors.



Graviton 3 Processor Presentation
Source: Amazon AWS



Intel's EMIB solution
Source: Hot Chips

Based on the Graviton3 package look, its interconnect bump pitch is reported to be 55µm - the same as EMIB. That, and the Amazon/Intel IFS packaging statement, make us believe that chiplets are linked with Intel's EMIB technology.

INTEL SAPPHIRE RAPIDS

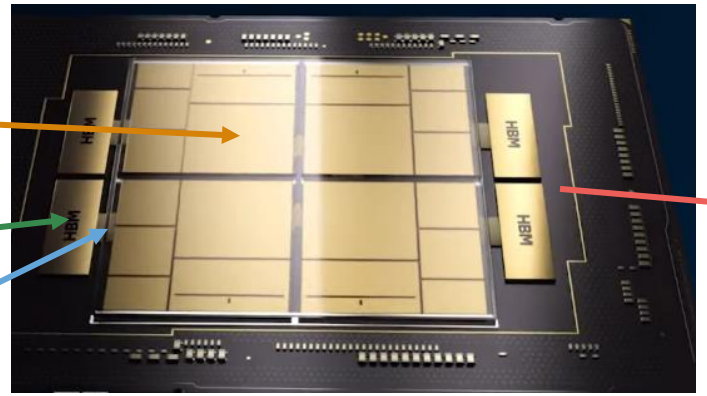
Intel's 4th Generation XEON CPU for Server application using EMIB technology

Sapphire Rapids Overview

CPU
- 4 chiplets
- INTEL 7 node
- 14 cores

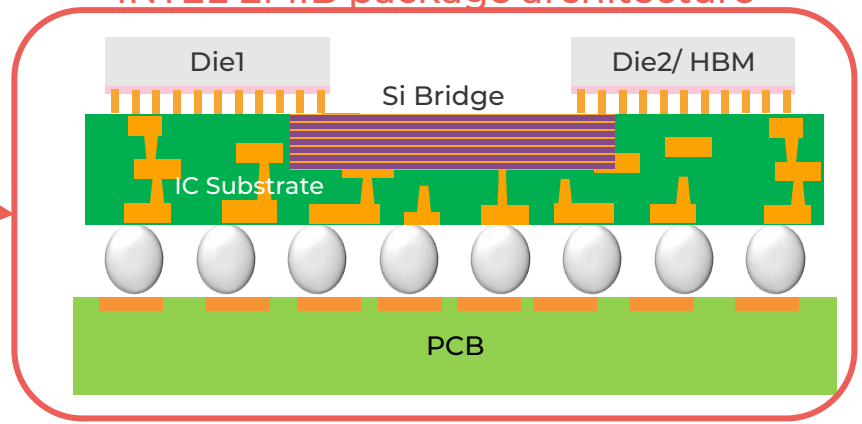
Memory (HBM variant)
- 4 HBMs
- 16GB

Package (HBM variant)
- 14 EMIBs



Sapphire Rapids package top view
Source: Intel

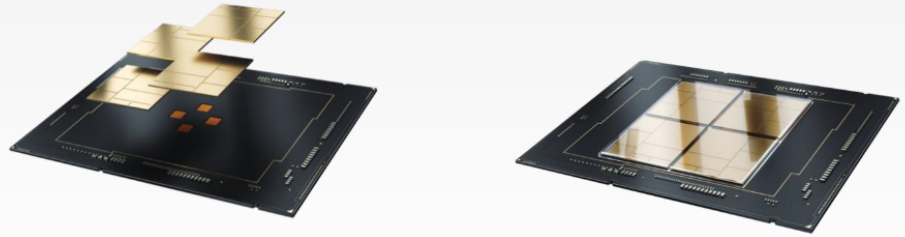
INTEL EMIB package architecture



- Released on 10th January 2023 as a successor to Ice Lake, Sapphire rapids contains 4 dies (chiplets) with 14 cores each based on INTEL 7 technology node.
- Comes in two package variants: Standard variant (4 dies); HBM variant (Standard + 4HBM of 16GB HBM2e).
- Each die and HBM is connected via EMIB which has a pitch size of 55µm and a core pitch of 100µm.
- Hence the standard version has 10 EMIB interconnects while HBM variant has 14 EMIB interconnects in total.
- Comparing Package Size with AMD EPYC Genoa (5428 mm²), the standard package of Sapphire Rapids is 22% smaller while the HBM variant is 5% larger than their AMD counterpart.
- EMIB link provides twice the bandwidth density and 4 times better power efficiency compared to standard package.
- Sapphire Rapids will be followed by Emerald Rapids later in 2023 while Intel has planned the next generation Granite Rapids and Diamond Rapids in 2024 and 2025 respectively.

Sapphire Rapids - EMIB Implementation

Sapphire Rapids package characteristics
Source: Intel



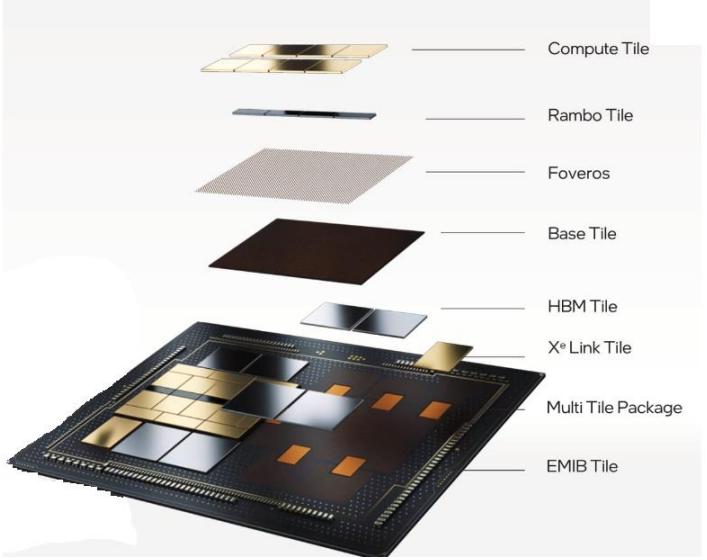
Attribute	SPR XCC	SPR HBM
Top Die Count	4	4, + 4 HBM2E
Max Top Die Size	~400 mm²	~400 mm²
EMIB Pitch	55µm	55µm
Core Pitch (minimum)	100µm	100µm
Memory (HBM)	N/A	4x 8H HBM2E
Package size	78 x 57 mm	100 x 57 mm
EMIB count	10	14

INTEL PONTE VECCHIO

PONTE VECCHIO Xe-HPC GPU is Intel's first data center General Purpose GPU using Co-EMIB

- Released at the end of 2022, Ponte Vecchio features Intel 7 and TSMC N7 and N5 processes and is built using INTEL Foveros and EMIB 2.5D packaging technology – also known as Co-EMIB.
- The Ponte Vecchio GPU is not a single chip but a combination of several chips and its chiplet powerhouse packs the most chiplets counting to 47 and hence different process nodes are used.
- It consists of 2 stacks and 8 HBM2e controllers leading to a HBM memory pool up to 128GB and contains 11 EMIB interconnects.
- The package information of Ponte Vecchio can be seen in the table. The package size is 4843.7 mm^2 and the 3D Foveros package pitch used is 36µm. Due to 2 stacks, the die size is 2 * 650 mm^2.
- The units responsible for I/O and high bandwidth components use INTEL 7 technology (area 640 mm^2) while Xe link uses TSMC 7nm process which is responsible for interconnection between GPUs.

Ponte Vecchio layout
Source: Intel

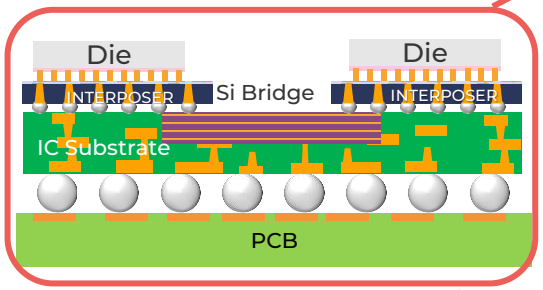


Ponte Vecchio Overview

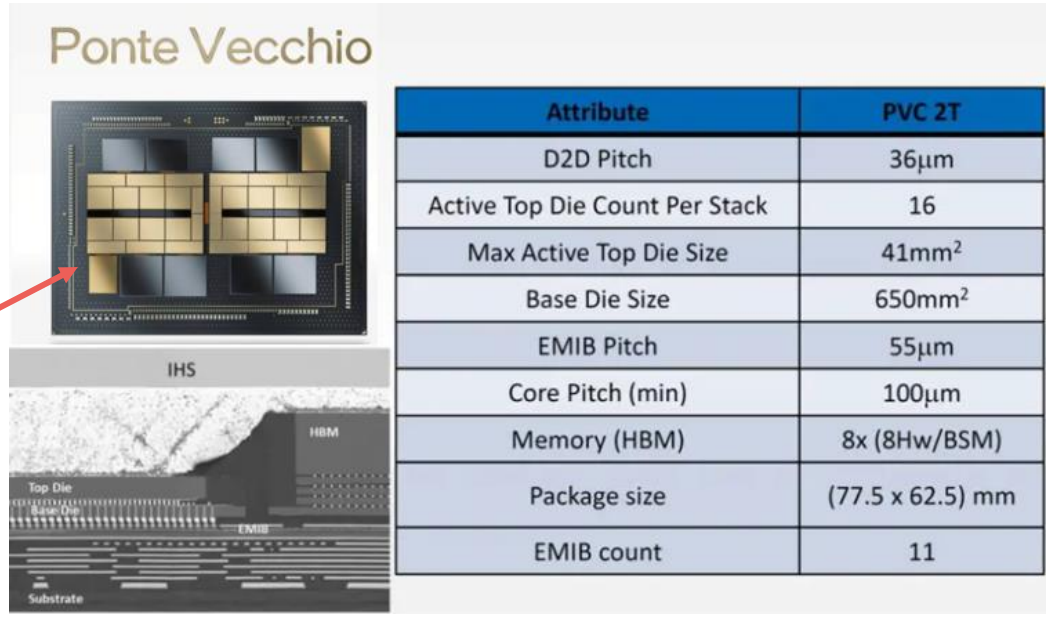
CPU
- 47 chiplets
- INTEL 7, TSMC N7 and N5 nodes
- Up to 128 cores

Memory
- 8 HBM2es
- 16GB each hence up to 128 GB

Package (Co-EMIB)
- 11 EMIBs
- Foveros (36 µm pitch)

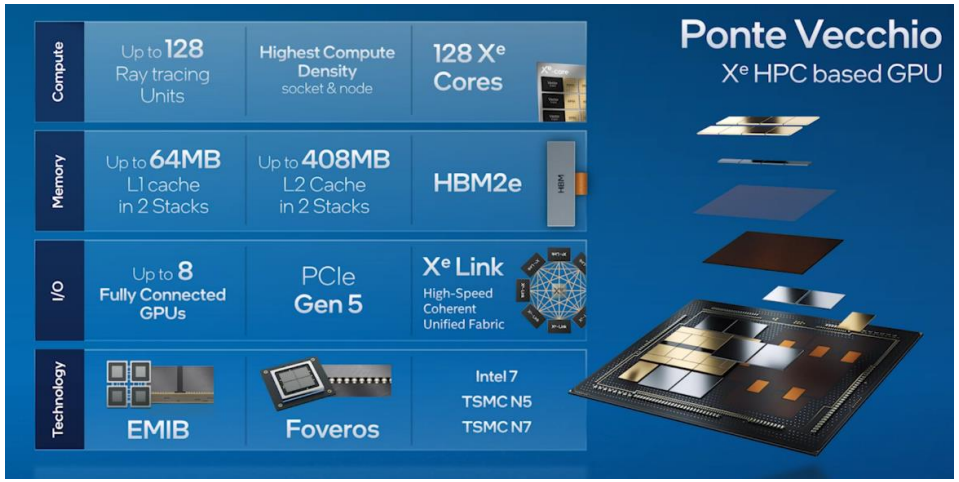


INTEL Co-EMIB package architecture



Attribute	PVC 2T
D2D Pitch	36µm
Active Top Die Count Per Stack	16
Max Active Top Die Size	41mm²
Base Die Size	650mm²
EMIB Pitch	55µm
Core Pitch (min)	100µm
Memory (HBM)	8x (8Hw/BSM)
Package size	(77.5 x 62.5) mm
EMIB count	11

Intel Ponte Vecchio package top view, layout and specifications
Source: Intel



Key specifications of INTEL Ponte Vecchio
Source: Intel

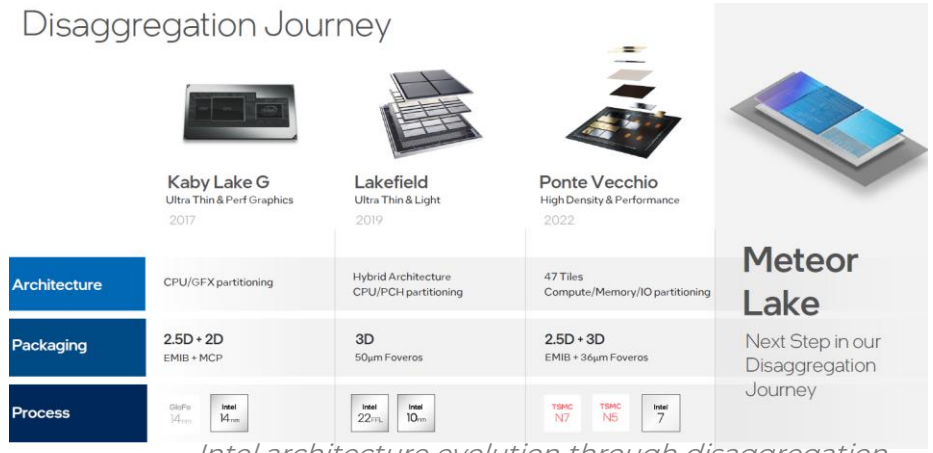
INTEL METEOR LAKE

Intel's 14th generation CPU using Foveros technology

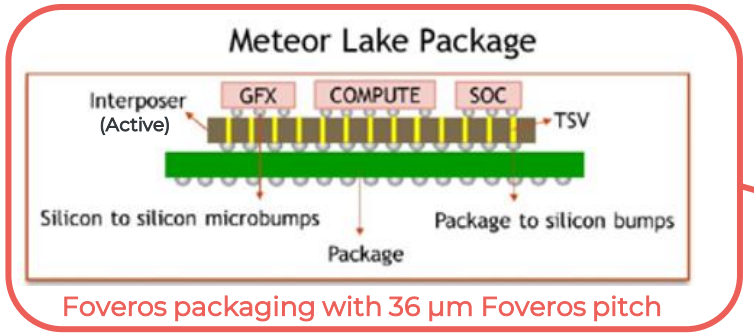
- Meteor Lake continues Intel's disaggregation chiplet journey, which Intel calls its new flexible Tiled Architecture. Advantages including flexibility with process nodes, which enables the ability to scale graphics and compute, along with I/O modularity, leading to lower power and discrete graphics performance.
- Expected in 2023, Meteor Lake is Intel's 14th generation CPU and uses 3D Foveros Technology.
- 3D Foveros packaging allows Intel to stack chiplets vertically atop one unifying base die with a Foveros interconnect.
- Meteor Lake uses 4 chiplets (tiles) on top of Foveros interposer (Base tile). The technology/application for the chiplets and base tile can be found in the table below
- The 4 chiplets are placed on top of a Foveros active interposer (base tile). The chiplets and the interposer are wired together with TSV connections. This Foveros interposer is manufactured with Intel's low cost and low power 2FFL process.
- Foveros uses a 36-micron bump pitch, which is an improvement on the 55 microns used in Lakefield. Foveros' roadmap includes 25- and 18-micron pitches and incorporates hybrid bonding interconnects to reach 1-micron bump pitches in the future.

Intel Meteor Lake Tile/Chiplet	Manufacturer / Node
CPU Tile	Intel / 'Intel 4'
3D Foveros Base Die	Intel / 22FFL (Intel 16)
GPU Tile (tGPU)	TSMC / N5 (5nm)
SoC Tile	TSMC / N6 (6nm)
IOE Tile	TSMC / N6 (6nm)

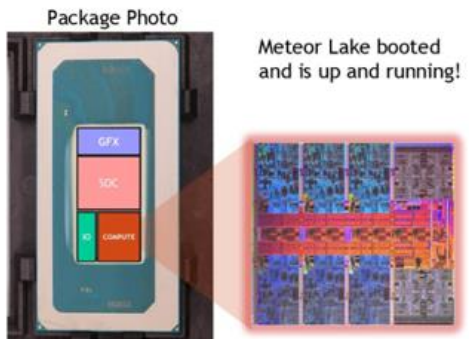
Meteor Lake Chiplet process nodes
Source: Intel



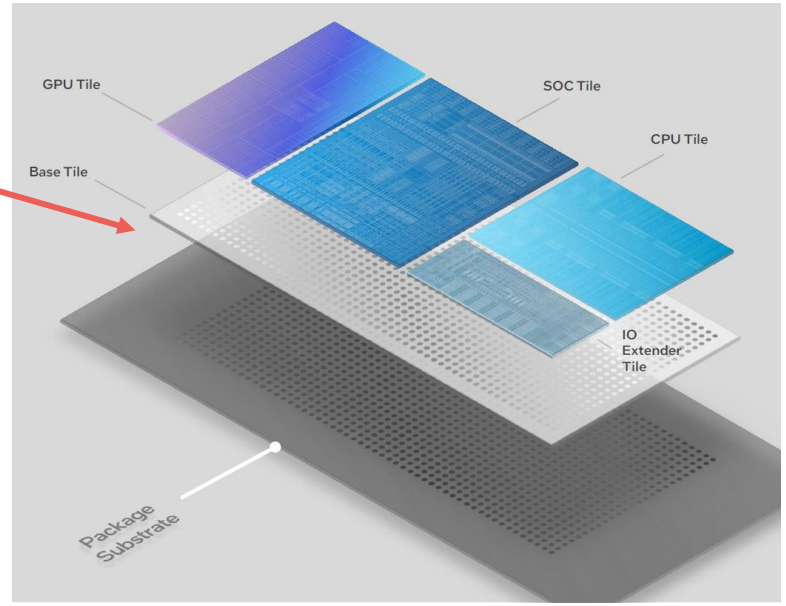
Intel architecture evolution through disaggregation
Source: Intel



Foveros packaging with 36 µm Foveros pitch



Photographic layout of the package
Source: Intel



Meteor Lake Layout: The different tiles (chiplets) perform a specific functionality and can be scaled individually because of process node flexibility; Source: Intel

INTEL: MOVING BEYOND METEOR LAKE

Arrow Lake and Lunar Lake are successor for Intel Meteor Lake using Foveros

Intel CPU roadmap has Arrow Lake and Lunar Lake planned as successors for Meteor Lake in 2024 and 2025 respectively. The use of disaggregated tiles (chiplets) enables the use of advanced process nodes which enables better IP refresh rate and form factor. Arrow Lake will have a better process node (Intel 20A) than Meteor Lake (Intel 4) with the same Foveros pitch (36 µm) while Lunar Lake will have a Foveros pitch of 25 µm. This enables one architecture to have multiple performance points by modifying the tile dimensions of different IP blocks. The use of disaggregated tiles enables a new era of System Level Integration due to scalable architecture, construction, flexible process nodes, and packaging in future generations.

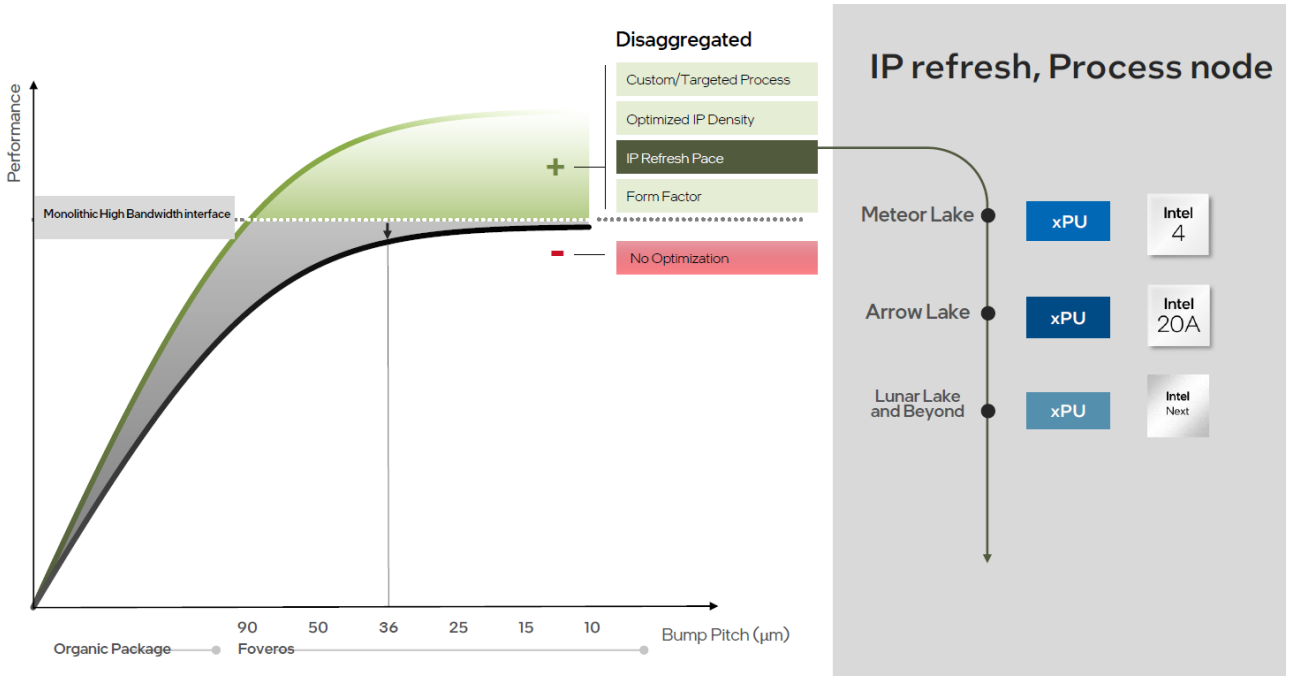
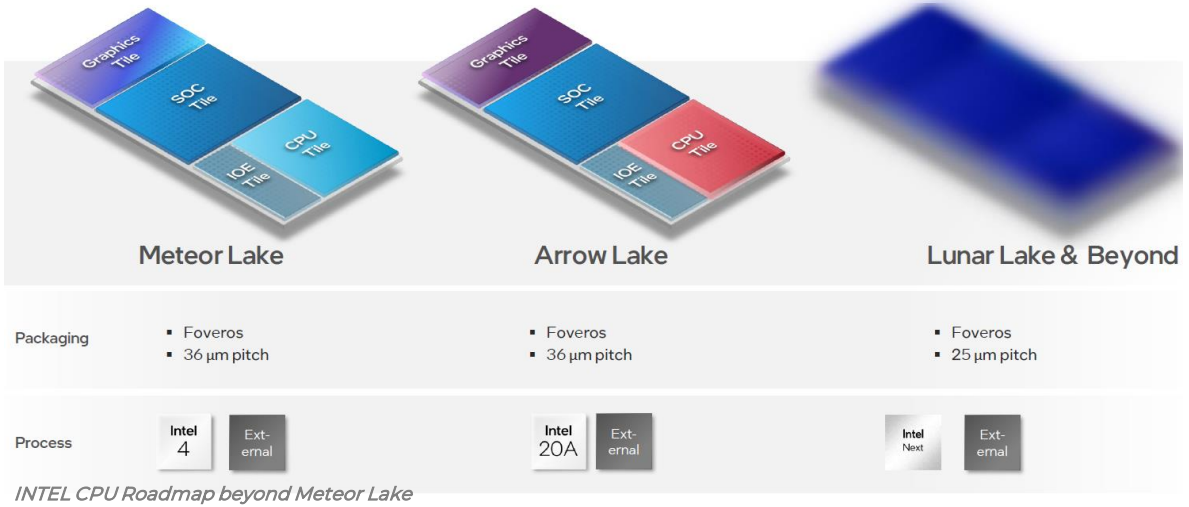
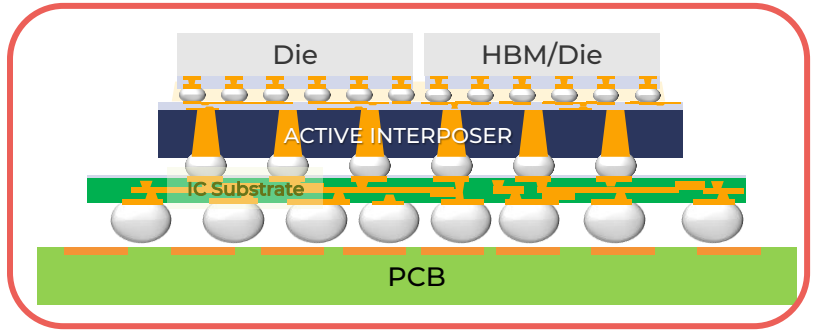


Figure shows the benefits of moving towards disaggregated tiles (chiplets) compared to monolithic SOC where no optimization is possible. By using INTEL 20A node for Arrow Lake, better performance than Meteor Lake can be achieved
Source: Intel



INTEL CPU Roadmap beyond Meteor Lake
Meteor Lake: INTEL 4, External Blocks + Foveros 36 µm pitch
Arrow Lake: INTEL 20A, External Blocks + Foveros 36 µm pitch
Lunar Lake: INTEL (next beyond 20A), External Blocks + Foveros 25 µm pitch
Source: Intel

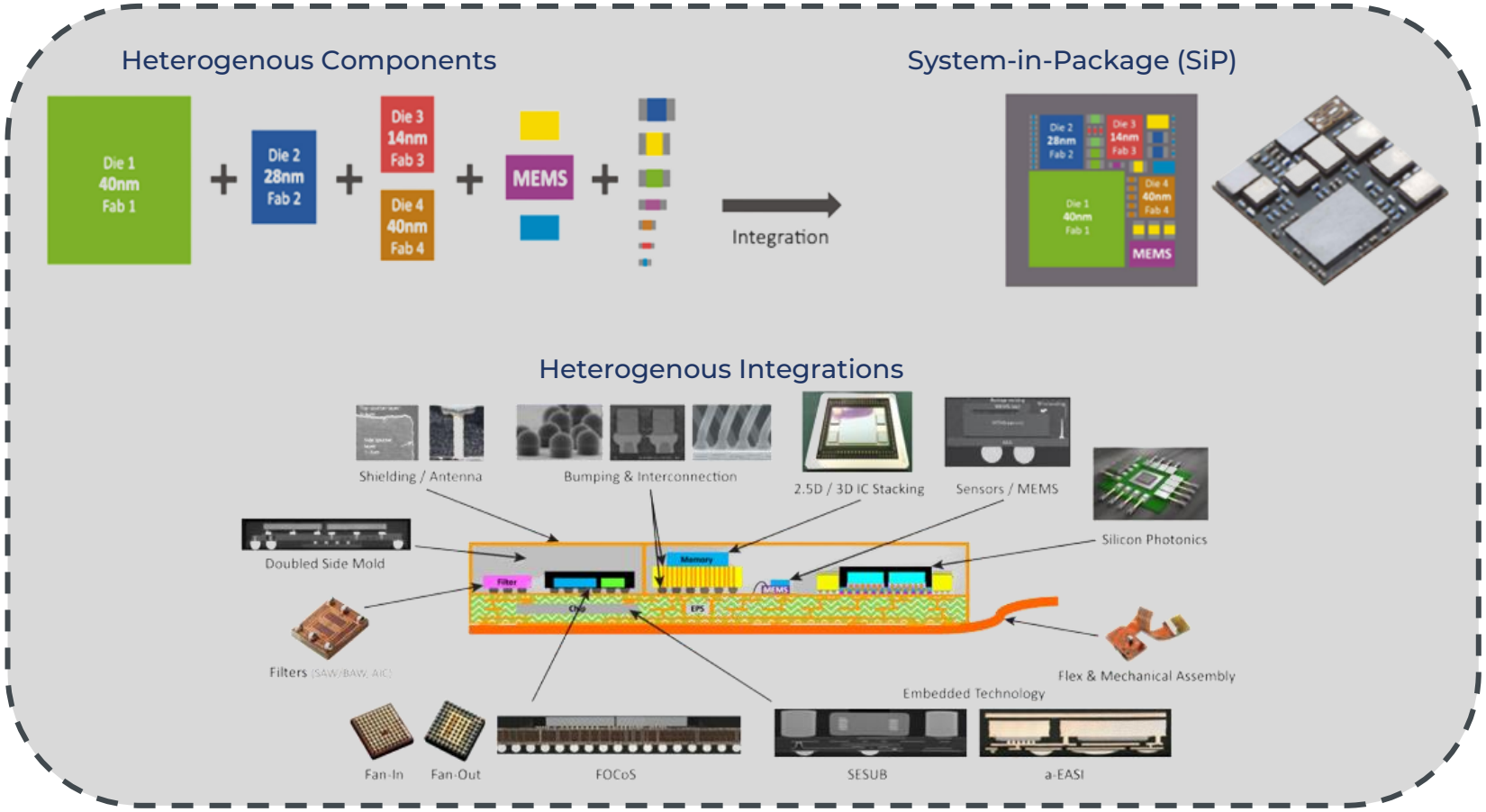
Foveros Package Architecture



Technology Trends: Focus on ASE

ASE'S ADVANCED PACKAGING TECHNOLOGY

- ASE has more than 90% of the packaging capabilities and offers a wide range of solutions, from traditional packaging to advanced packaging.
- **IC Package Solutions**: LF Packaging, WB BGA, FC Packaging, Wafer Level Packaging
- **Advanced Technologies:** Fan-out, 2.5D/3D Packaging, Silicon Photonics, SiP, AiP, MEMS and Sensors, Embedded Die Solutions
- ASE believes in Heterogeneous Integration (HI) and offers solutions to integrate multiple dies in the same package with smaller form factors.



FAN-OUT PACKAGING TECHNOLOGIES: ASE

ASE has a wide portfolio of technologies in fan-out packaging, including chip-first, chip-last, face-up, face-down, PoP, SiP and FO-on-substrate.

Production

eWLB

Licensed from Infineon since 2009
BB, RF, Codec, Car radar

- Pkg ~ 12x12
- RDL 12/12um
- 2L RDL
- Chip-First, Face-Down

M-Series

Licensed from Deca Production since 2018
BB, RF, PMIC, Codec

- Pkg ~ 12x12
- RDL 8/8um
- 2L RDL
- Chip-First, Face-Up

Development / Qualification

FOPoP

AP & Memory
Available since 2016

- Pkg ~ 15x15
- RDL 5/5um
- 3L RDL
- Chip-First, Face-Up

FOSiP

RF, FEM, Power, MCU
Available since 2017

- Pkg ~ 15x15
- RDL 5/5um
- 5L RDL
- Chip-First, Face-Up

Panel FO

RF, FEM, Power, Server
Available since 2019

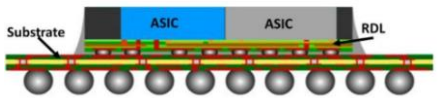
- Pkg ~ 67x67
- RDL 2/2um
- 5L RDL
- 300x300mm panels (Chip-Last)
  600x600mm panels (Chip-First)

Fan-Out Chip on Substrate (FOCoS) Solutions

- Networking, Server
- Pkg ~ 67x67
- RDL 2/2um
- 3L RDL
- Since 2016
- ASE In-house developed technology.

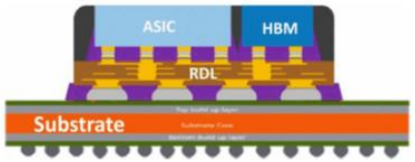
Production

FOCoS-CF (Chip First)

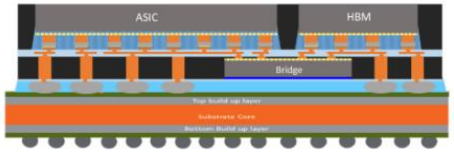


Development / Qualification

FOCoS-CL (Chip Last)



FOCoS-B (Bridge)



Source: ASE Group

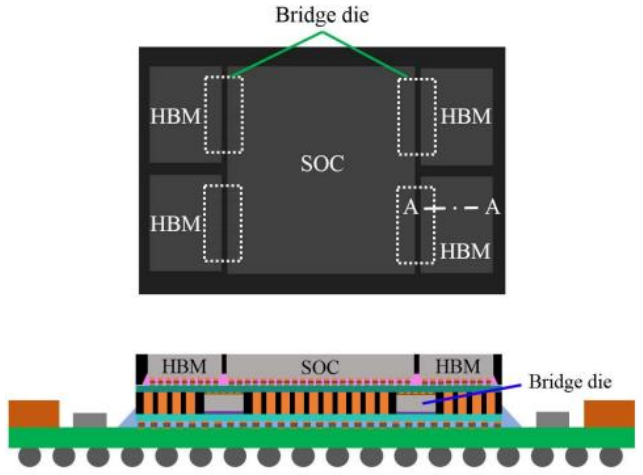
FAN-OUT PACKAGING TECHNOLOGIES: SPIL

SPIL (Siliconware Precision Industries Co., Ltd) is a member of ASE Technology Holding Co., Ltd., together with ASE and USI. SPIL leverages a diversified FOWLP product portfolio, addressing Core, HD and UHD FO technologies.

SPIL Fan-Out Wafer Level Packaging Portfolio

Source: SPIL

- **FO-Single Die** and **FO-Multi Die** started mass production since 2017.
- In 2021, SPIL entered the UHD FO supply chain when it started supplying AMD with its **FO-Embedded Bridge (FO-EB)** technology, utilized in AMD Instinct™ MI200 series accelerators (data center GPUs).
- **FO-EB features include:**
  - Within the organic interposer, there are embedded bridge dies, fabricated with Cu wires with L/S values ranging from 0.56~0.8µm.
  - Cu micro-bump pitch of 40µm
  - Fan-out routing technology enables routing capability ranging from 2/2 µm to 10/10 µm L/S, allowing a flexible power-ground connection platform to provide a lower-cost solution.
- SPIL's next generation of the FO-EB platform includes an embedded silicon bridge die with TSV (**FO-EB-T**). It preserves FOEB advantages while providing better electrical performance with direct signal and power transmission through TSV in silicon bridge die. The simulation data indicated that power consumption can be reduced by 55% against FO-EB without TSV.



Schematic diagram of FOEB package . Source: "Scalable Chiplet package using Fan-Out Embedded Bridge", SPIL: ECTC, 2020

ASE'S ADVANCED PACKAGING TECHNOLOGY

VIPack™ Platform

ASE introduced VIPack, comprising six core packaging technology pillars.

Fan Out Package-on-Package (FOPoP)	Fan Out Chip-on-System (FOCos)	FOCos – Bridge (embedded)	Fan Out System-on-Package (FOSiP)	2.5D/3D IC	Co-Pacakged optics

Integrated Design Ecosystem

In Jun 2022, ASE introduced VIPack™, an Advanced Packaging platform designed to enable vertically integrated package solutions. VIPack™ represents ASE's next generation of 3D heterogeneous integration architecture that extends design rules and achieves ultra-high density and performance. The platform leverages advanced redistribution layer (RDL) processes, embedded integration, and 2.5D and 3D technologies to help customers achieve unprecedented innovation when integrating multiple chips within a single package.

VIPack™ is comprised of 6 core packaging technology pillars to provide the capabilities necessary to enable trailblazing highly integrated silicon packaging solutions.

ASE'S ADVANCED PACKAGING TECHNOLOGY

VIPack™ Platform

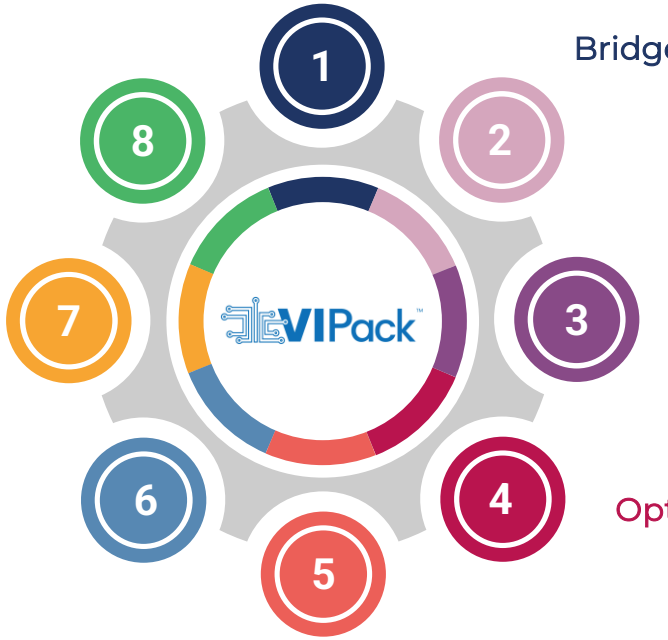
VIPACK uses advanced redistribution layer (RDL) processes, embedded integration, and 2.5D and 3D technologies to enable trailblazing highly integrated silicon packaging solutions required to optimize clock speed, bandwidth, and power delivery, and to reduce co-design time, product development, and time to market

8 ASIC/SoC Chips

7 I/O die and IP chiplets

6 Memory devices

5 TSV interposers

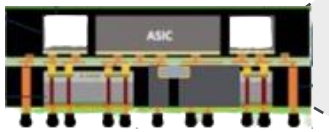


1 Bridge/Embedded Si/IVR

2 Photonics ICs

3 RLC Components

4 Optical/MEMs/Sensors

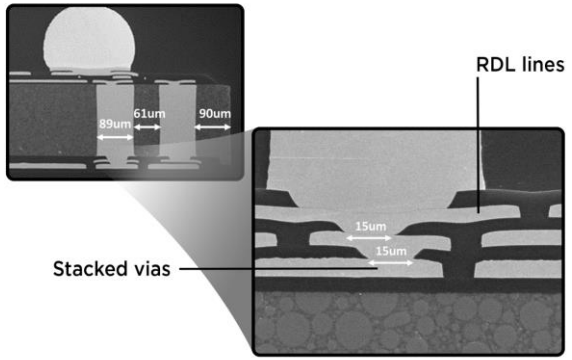


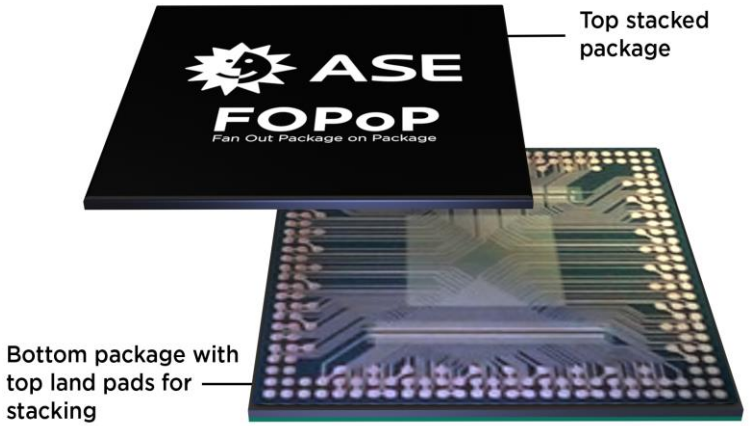
- Multi Die Integration w/50µm spacing
- Double or Triple sided encapsulation & CTE matching
- Layer-to-layer Cu Post up to 150 µm ht, 120 µm pitch
- Advanced RDL carrier handling & Multilayer stack
- Double sided RDL & Component Capability
- Ultra Low Loss interconnect- Hybrid bond- Solderless <30µm
- Micro Power Delivery Enablement – DTC for Advanced Si Noise Reduction, Bridge die
- Advanced RDL W/ created passives
- TSV-Last integration with stress mitigated Via

ASE'S ADVANCED PACKAGING TECHNOLOGY

ASE unveils new FOPoP solution for mobile and networking markets

- ASE has launched its most advanced Fan-Out-Package-on-Package (FOPoP) solution to improve package performance and enable next-generation solutions for application processors, antenna-in-package devices, and silicon photonics (SiPh) applications.
- The FOPoP package platform enhances high-performance needs by enabling RDL on both sides of the die for increased integration and functionality. Also, both landside caps and near-die deep trench capacitors can be implemented to meet the power integrity requirements of advanced nodes.





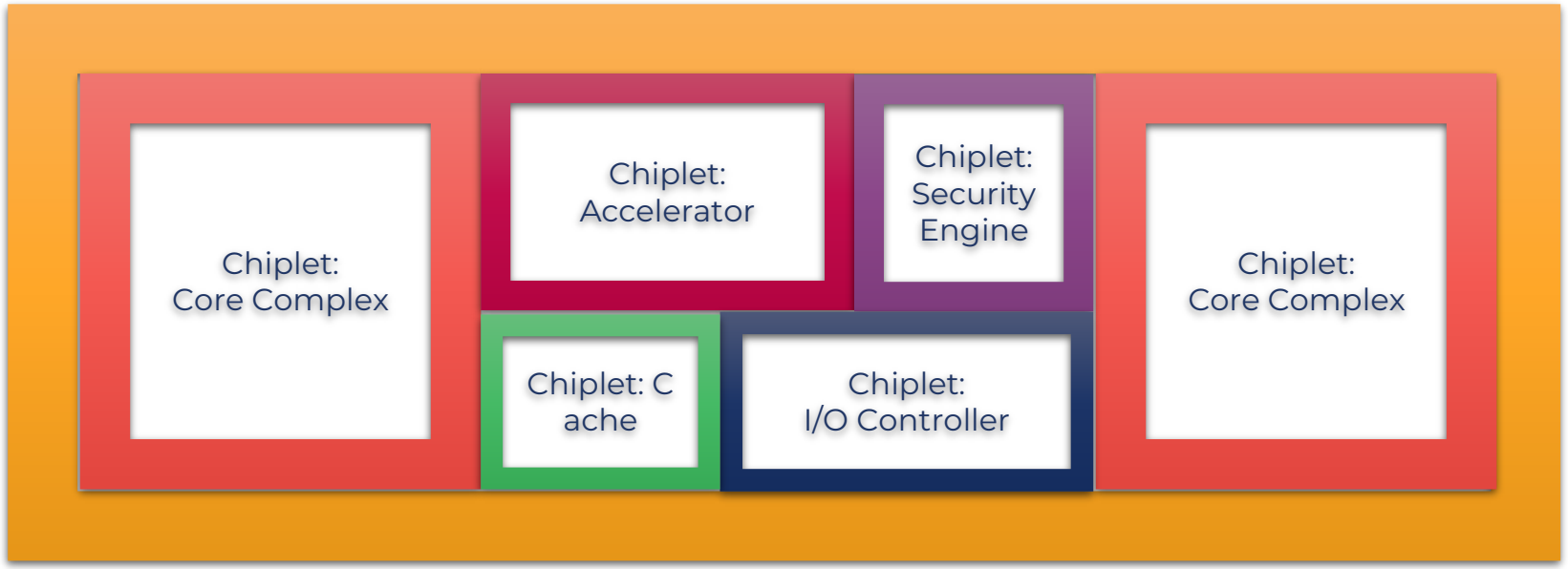
- FOPoP helps to enable the next generation of bandwidth from 400G - 800G pluggable optical transceivers and presents a highly viable integration solution for CPO. Moreover, it reduces the electrical path by 3x and enables a denser bandwidth by up to 8x, allowing engine bandwidth expansion up to 6.4 Tbps per unit.
- For mobile applications, the FOPoP package provides higher interconnection density and integration through a finer line space RDL, a shorter interconnect length resulting in better electrical performance, and a smaller, thinner form factor. It also achieves an almost 40% reduction in height over substrate-based package-on-package structures.

High End Performance Packaging and Chiplet Trends

WHAT CONSTITUTES A “CHIPLET” ?

Yole Group definition of a Chiplet

’Chiplet’ describe an emerging semiconductor design philosophy that combines two or more discrete die in a disaggregated or duplicated processor SiP design, allowing for more design flexibility, faster time to market, better yield, and thus an economic benefit over a possible monolithic alternative. *The functions of the discrete chiplets should be among the IP blocks found in a typical processor SoC, including, but not limited to: CPU, GPU, NPU, I/O and memory controllers and interfaces, cache memory, and analog functions (SerDes, PLLs, DAC, ADC, PHYs, etc)”*



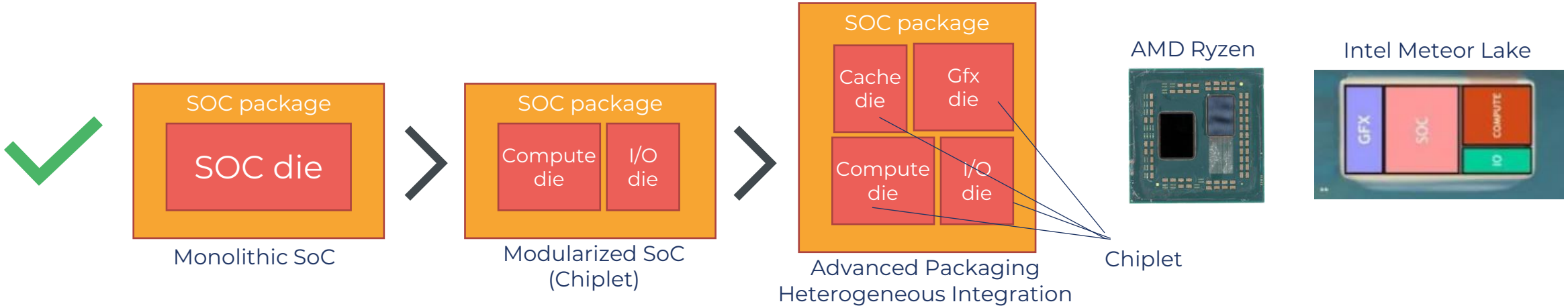
Advanced Packaging Platforms integrating chiplets

- FC BGA
- 2.5D
- 3D

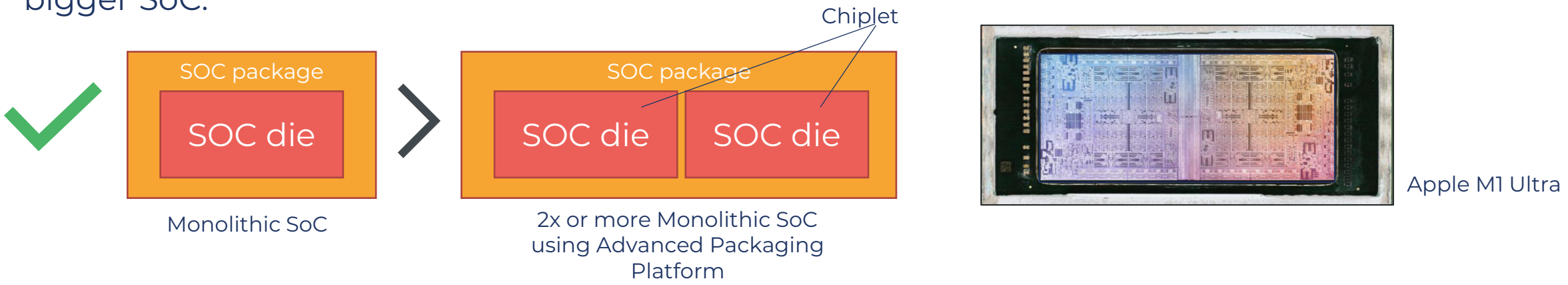
WHAT COUNTS AS A CHIPLET?

The answer is Disaggregation and Duplication

Disaggregation: the SoC monolithic die is partitioned in smaller chips with different functions, then interconnected in the same package.



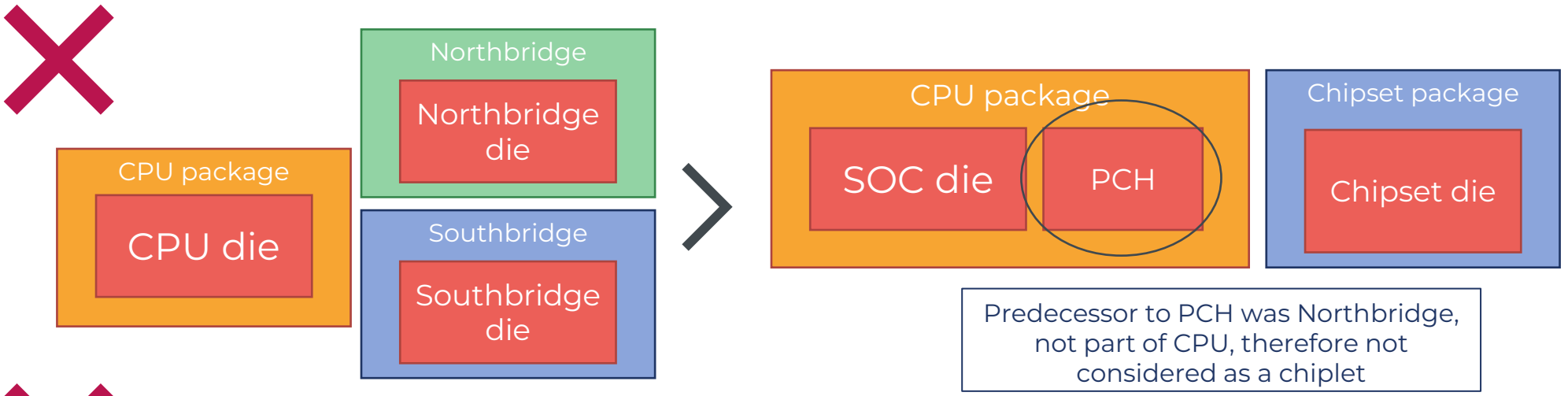
Duplication: two or more SoC monolithic dies are interconnected in the same package forming a bigger SoC.



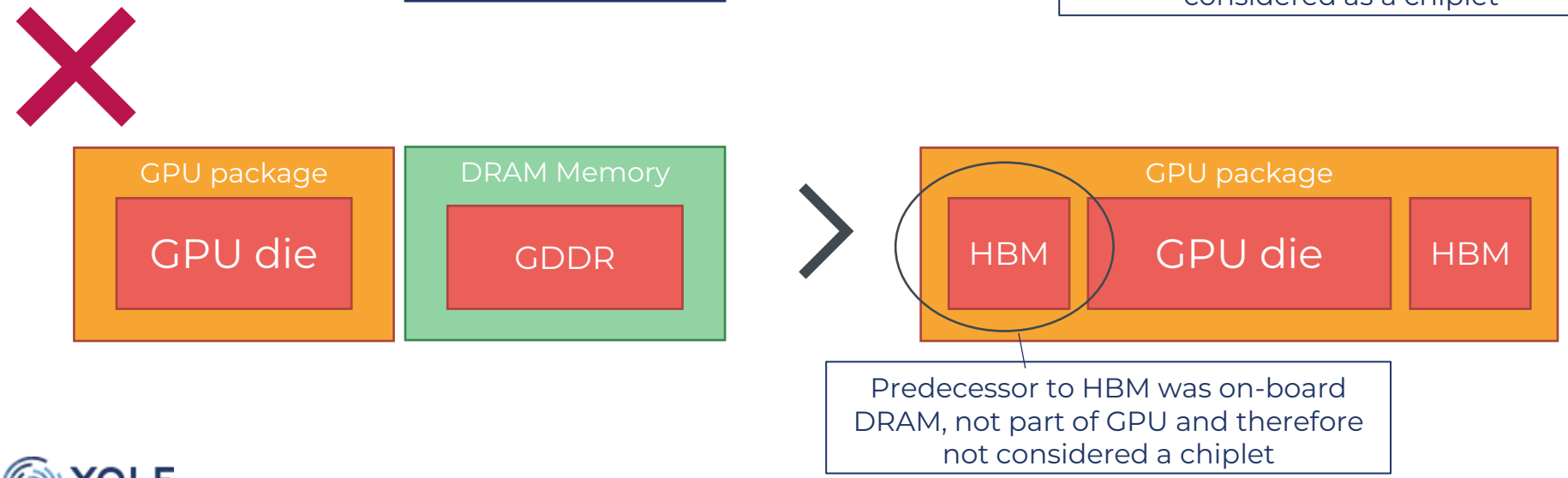
IS A SIP COMPONENT OBTAINED BY ACCUMULATION OF A CHIPLET?

Products obtained by accumulation are not chiplets

Accumulation: the interconnection of different chips in the same package which previously were in different packages. This is not a chiplet architecture!

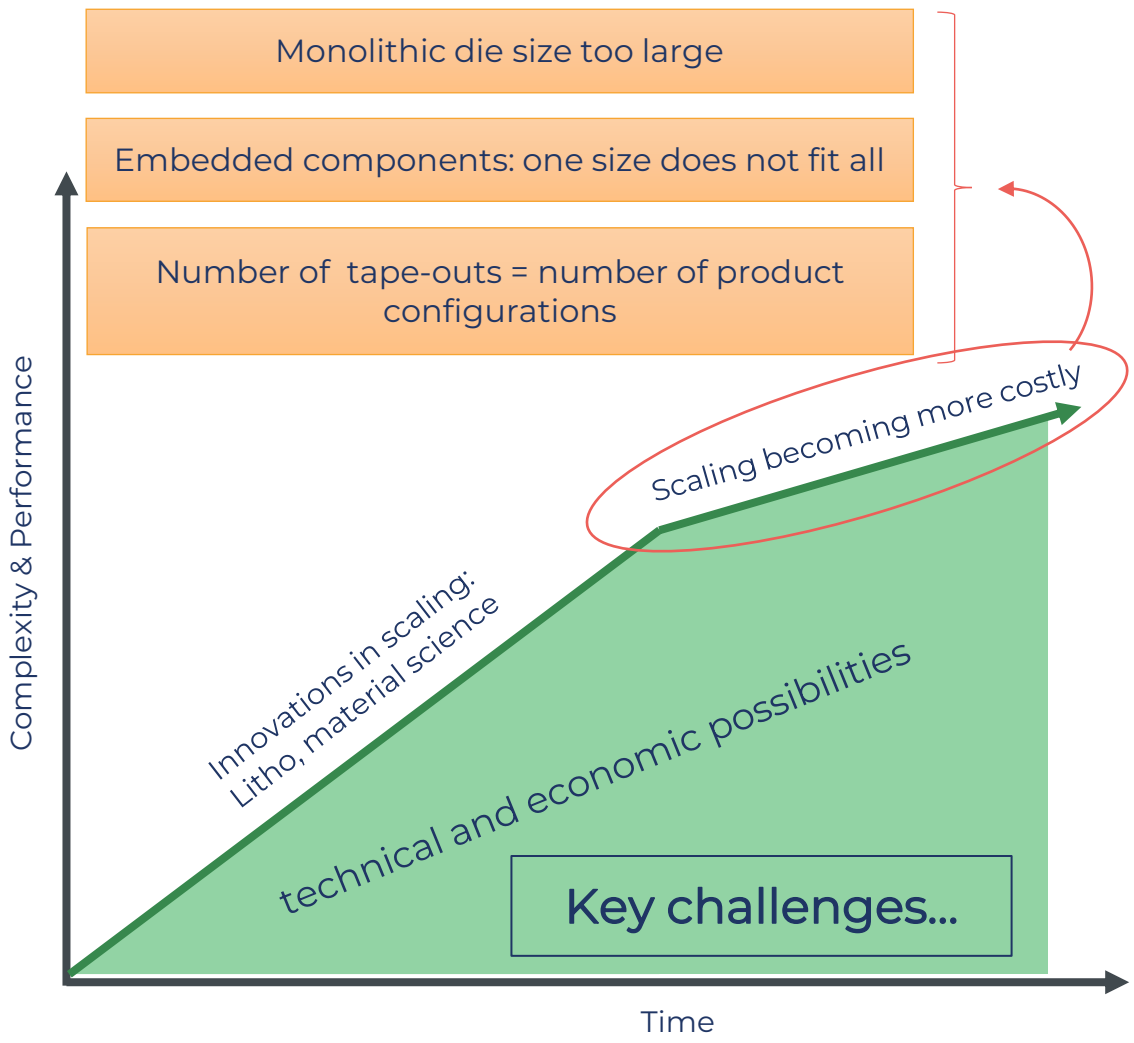


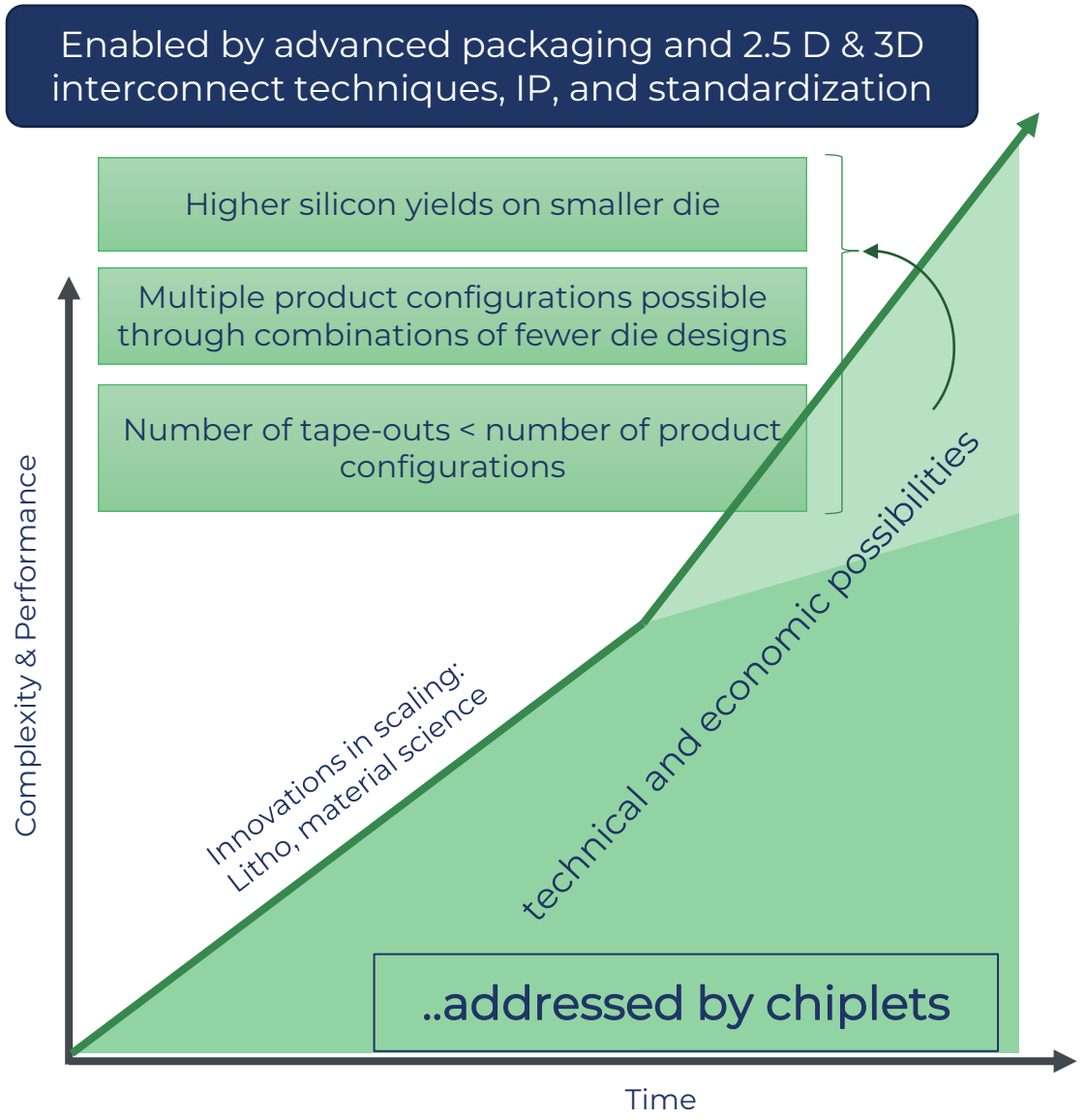
Intel Tiger Lake



Nvidia A100

POSSIBILITIES ARE EXPANDED BY CHIPLETS, CREATING OPPORTUNITIES FOR NEW MARKETS





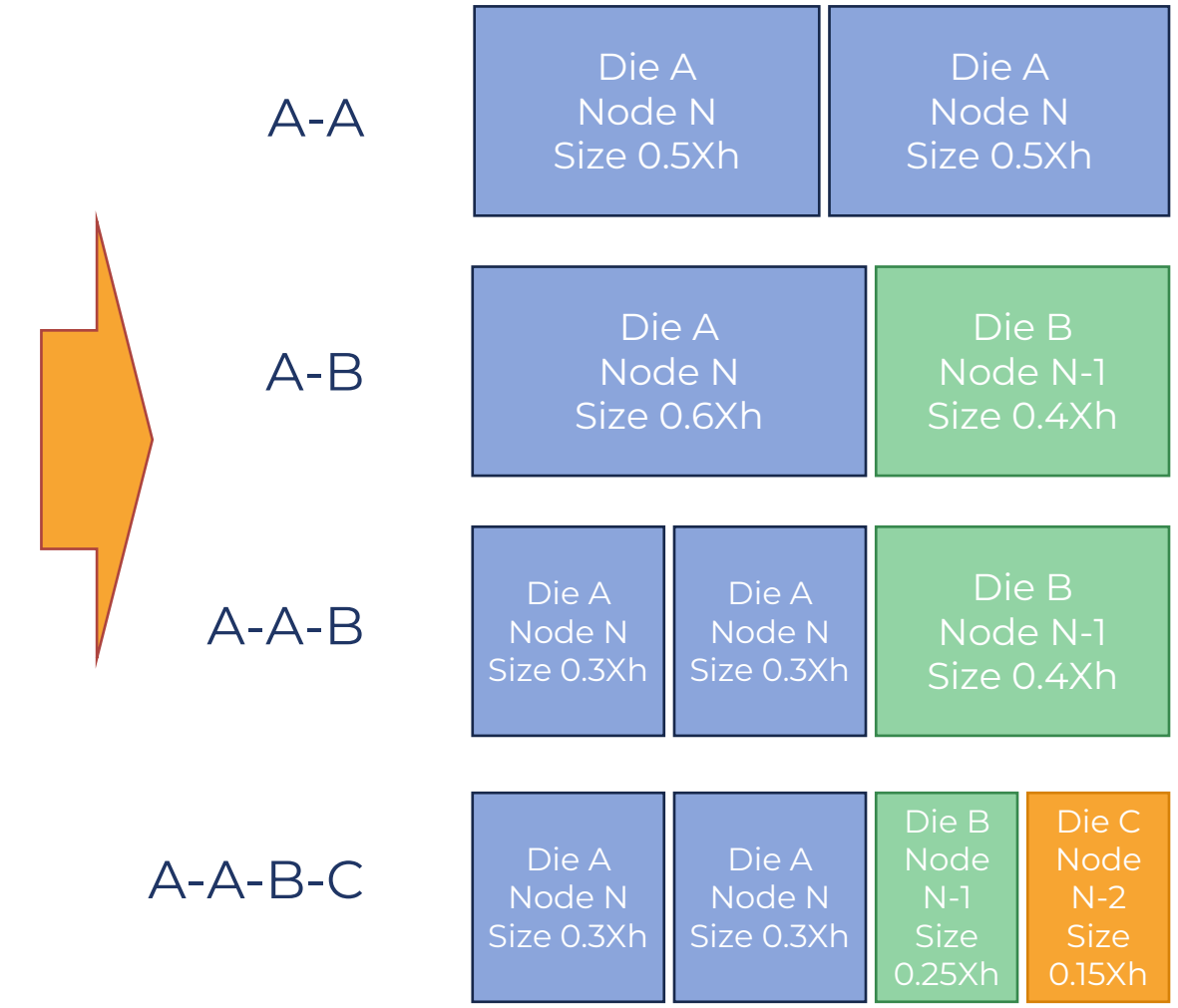
COST OF HYPOTHETICAL CHIPLET CONFIGURATIONS

Monolithic

Monolithic die
Node N
Size X
Wafer cost = f(N)

h = chiplet overhead (% of silicon area increase needed to enable chiplet configuration)

Disaggregated Chiplets



The chiplet cost model compares the cost of a packaged monolithic against a variety of chiplet-based equivalents, made from disaggregated die, where the silicon area, packaging costs, and wafer costs are treated as variables.

But how are these die connected?

Flip-chip on organic substrate
Flip-chip with RDL (UHD FO)
Mold Interposer + Si Bridges
Si Interposer
Si bridges
D2W/ W2W hybrid bonding (3D SoC)

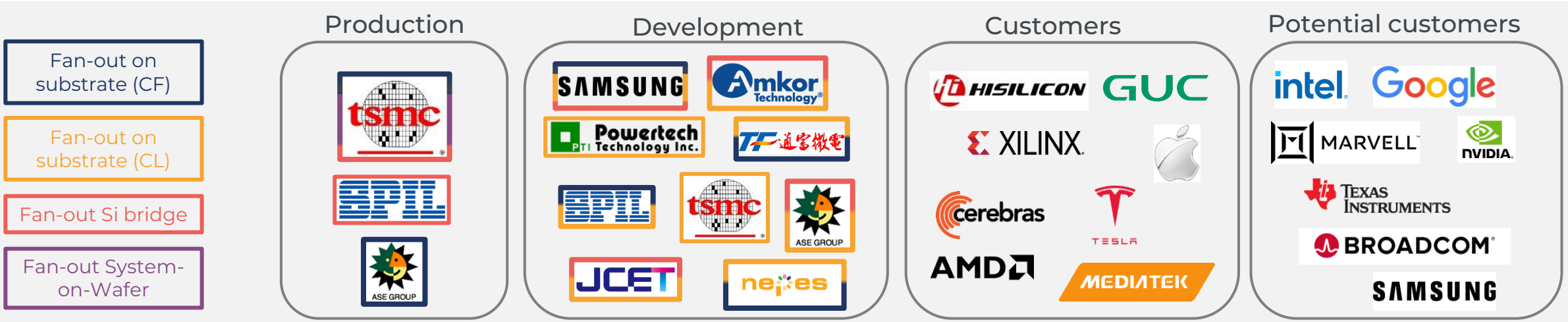
HIGH-PERFORMANCE COMPUTING APPLICATIONS

Fan-out packaging to enable multi-chip and chiplet integration

Chiplets are booming in HPC-related applications, including data centers, networking, data servers, and edge computing segments. Ultra-high-density fan-out technologies are being adopted in HPC and high-end PC applications to enable the integration of chiplets and heterogeneous integration. Until now, fan-out has been mainly used for Logic + Logic integration with a chip-first (CF) approach, but there is a vast potential to also leverage fan-out packaging for heterogeneous integration of (x)PU + HBM by using a chip-last (CL) approach.

Why choosing Fan-out RDL-based solutions for multi-die/chiplet integration?

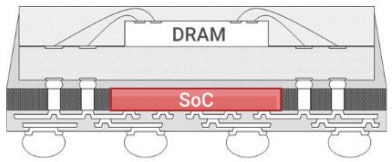
- Lower cost than Si Interposers
- High-density and high-bandwidth die-to-die interconnects, without any FEOL processes necessary
- High power and signal integrity
- CTE mismatch between RDL and IC substrate is lower than Si Interposer and IC substrate and, as a result, the package level thermal stress can be minimized for better package reliability
- Assembly process compatible with OSAT capabilities with no support from the foundry



HIGH-END MOBILE & CONSUMER PRODUCTS

Are chiplets the next innovation step in smartphone APUs?

High-density fan-out with a Package-on-Package configuration has been demonstrated to be a good replacement for the mainstream flip-chip solution. But what comes next for smartphone APUs?



InFO_PoP. *Source: TSMC*

FOPoP. *Source: ASE*

SWIFT. *Source: Amkor*

OSATs start qualifying FO-PoP solutions to compete with TSMC and Samsung. Examples are ASE / SPIL, Amkor, PTI and nepes

2016 ... 2022 ≥ 2024

Apple adopts TSMC's InFO_PoP technology

Potential for other players to adopt FO-PoP

SAMSUNG Qualcomm MEDIATEK

New

Google adopted FOPLP technology from samsung in its Tensor G2 APU

Google

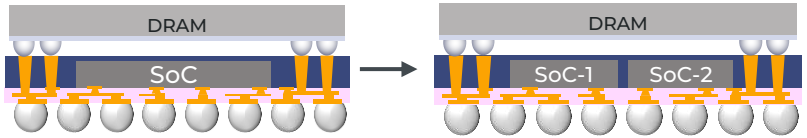
Chiplets?

The chiplet approach is a big trend, and there is a huge hype in the market to find the best advanced packaging solution to achieve high-density die-to-die interconnection. Fan-out RDL interconnections are one approach to achieving high-density connections in die partitioning.
The use of chiplets in the mobile APU could result in several advantages:

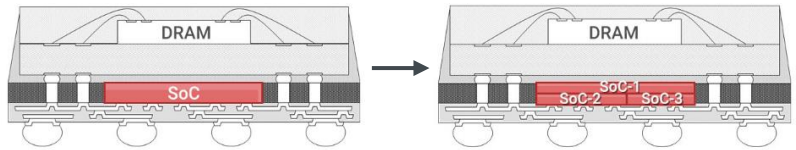
- **Decrease the cost of the system** – by dividing the monolithic SoC into various chiplets with different functions and only scaling the logic die to the more advanced node
- **Increase performance** – by integrating more than one logic die and improving the system's computing power.

Different approaches for integration

Side-by-side integration



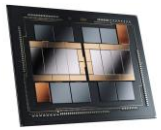
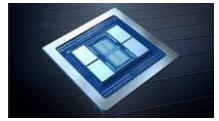
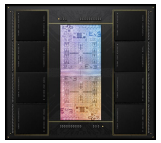
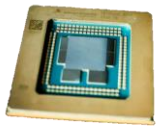
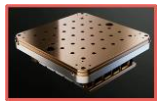
3D Stacking
TSV + microbumps or Hybrid bonding



TSMC example of chiplet integration with its 3D SoIC technology in mobile APU. *Source: TSMC*

EXAMPLE OF CHIPLET BASED PRODUCTS

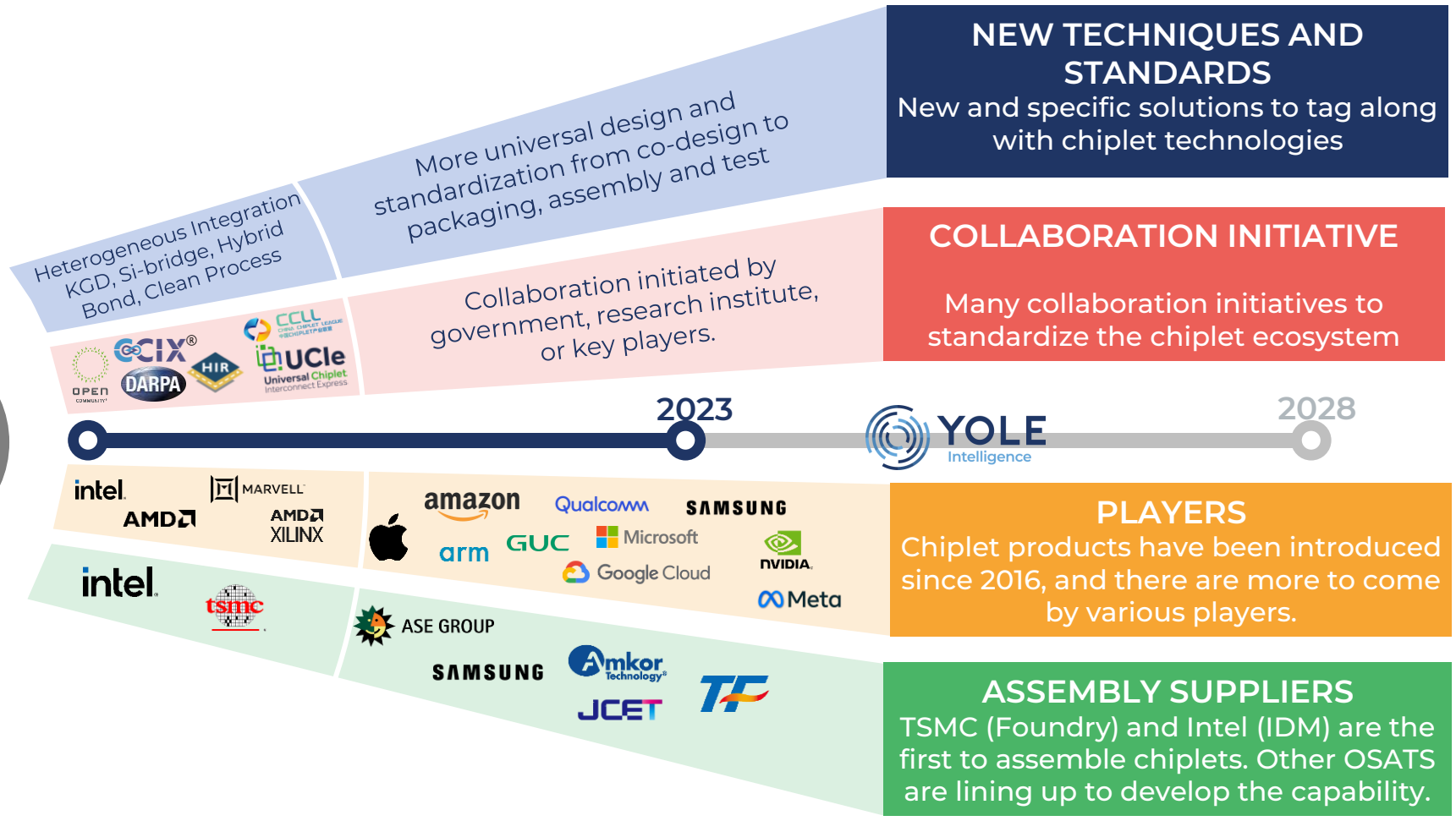
Commercialized & announced products

Company	Strategy	Products*
intel	Chiplet and heterogeneous integration is focus of IDM 2.0 strategy.	 Sapphire Rapids (EMIB) Launched Q1 2023  Ponte Vecchio (Co-EMIB) Available 2023  Meteor Lake (Foveros) Available 2023  Arrow Lake (Foveros) Available 2024  Foveros Direct Available 2024
AMD	AMD has now shipped several generations of PC and server processors using its chiplet interconnect platform Infinity Fabric (IF). AMD uses organic substrate to integrate chiplets.	 AMD Ryzen Series Ryzen 3000 Launched 2019  AMD Radeon Instinct™ MI200 Series Launched 2022  3D V-Cache in AMD Ryzen and EPYC Gen 3 Launched 2022  AMD Radeon RX7900 Launched 2022
	Apple recently released its M1 Ultra product which is a combination of two M1 Max dies interconnected using TSMC's LSI technology.	 M1 Ultra (with TSMC InFO_LSI) - launched 2022
amazon	Amazon launched their Graviton3 data center processor during their AWS in 2021. It is a chiplet product with seven dies and a total of 55 Bn transistors.	 Graviton3 (with Intel's EMIB technology) Launched 2022
TESLA	Dojo D1 is Tesla's in-house supercomputer for Machine Learning. 25 D1 chiplets packaged together.	 TESLA DOJO (TSMC's integrated fan-out system on wafer (InFO_SoW) package) Launched 2022
壁仞科技 BIREN TECHNOLOGY	BR100 GPU consists of 2 chiplets (dual die GPU) processed on TSMC 7nm node.	 Biren Technology BR100 (with TSMC CoWoS) Launched 2022

*Non-exhaustive list

CHIPLET EVOLUTION

Chiplet



NEW TECHNIQUES AND STANDARDS

New and specific solutions to tag along with chiplet technologies

COLLABORATION INITIATIVE

Many collaboration initiatives to standardize the chiplet ecosystem

PLAYERS

Chiplet products have been introduced since 2016, and there are more to come by various players.

ASSEMBLY SUPPLIERS

TSMC (Foundry) and Intel (IDM) are the first to assemble chiplets. Other OSATS are lining up to develop the capability.

Benefits

- Improved yield during manufacturing compared to SoCs
- Cost reduction due to smaller chiplet size
- Faster time-to-market with chip partitioning
- Reduced design and manufacturing costs with CPU core chiplets
- Thermal advantages due to chiplets being spread out across the package.

Challenges

- Increased package size due to the need for additional interfaces
- Higher packaging costs associated with chiplets
- More complexity and design effort required to implement chiplets
- Traditional design methodologies may be less effective for chiplets.

*Non-exhaustive list

UNIVERSAL CHIPLET INTERCONNECT EXPRESS (UCIE)

- The Universal Chiplet Interconnect Express (UCIe) is a recent industry effort (2022) that aims to allow companies to customize chips for unique workloads by integrating IP blocks that serve various functions and then packaging them according to an application. The idea is to provide a set of interface and power parameters that will allow chips to fit into a certain size and power envelope, much like building software with APIs.
- UCIe is based on well-known technologies such as PCIe and CXL, and it also addresses how chiplets are packaged. The UCIe effort is being driven by major hyper-scalers and chip IP vendors who want specialized chips that cater to their needs.

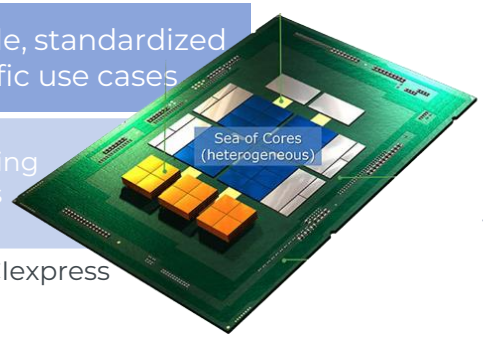
- The UCIe 1.0 specification was ratified to provide a complete standardized die-to-die interconnect with physical layer, protocol stack, software model, and compliance testing that will enable end-users to easily mix and match chiplet components from a multi-vendor ecosystem for system-on-chip (SoC) construction, including customized SoC.

Board members and UCIe adopters

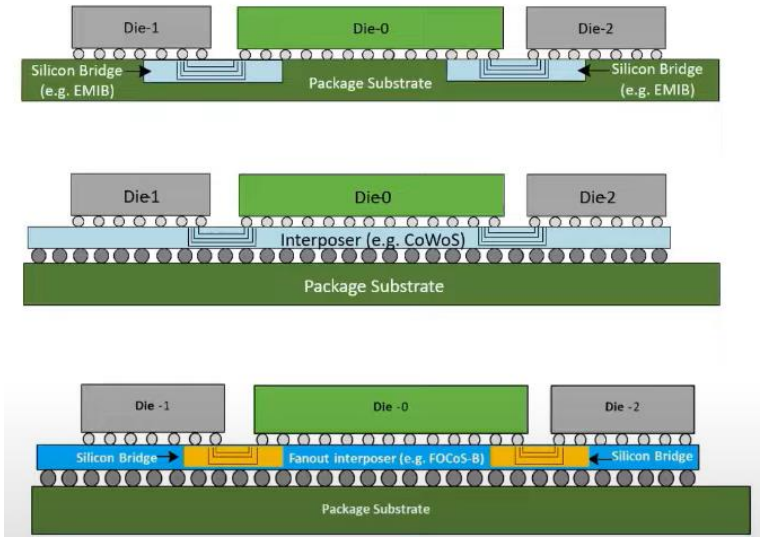
AMD, arm, Google, intel, Meta, Microsoft, tsmc, SAMSUNG, NVIDIA, Qualcomm, GUC, imec, MARVELL, SK hynix, Micron, JCET, TF, nepes, MEDIATEK, MICROCHIP, And others

MOTIVATIONS

- Allows creation of larger SoCs by combining multiple dies into a single package.
- Enables faster time-to-solution by reusing existing dies.
- Reduces costs across the product portfolio by optimizing process technologies, improving yields, and lowering IP porting and SKU costs.
- Provides customizable, standardized products for specific use cases
- Drives innovation by unlocking manufacturing and process-locked IPs for scaling



Source: UCIexpress



Source: UCIexpress

UCIe 1.0 enables an open ecosystem by supporting various Advanced Packaging platforms. It allows the manufacturing of dies anywhere and their assembly anywhere and offers greater flexibility for SoC design by allowing a mix of 2D and 2.5D in the same package.

Characteristics of UCIe 1.0	Advanced PKG
Width (each cluster)	64
Bump Pitch (µm)	25 – 55
Channel Reach (mm)	<= 2

Target for key metrics (2027-2028)	Advanced PKG
Power Efficiency (pJ/b)	0.25
B/W Density (GB/s/mm²)	188 – 1350 (for AP: 45 µ)
B/W Shoreline (GB/s/mm)	165 – 1317 (for AP: 45 µ)

Source: UCIexpress

OPEN DOMAIN-SPECIFIC ARCHITECTURE (ODSA)

A sub-project of Open Compute Project (OCP)

- ODSA was chartered in March 2019 within Open Compute Project (OCP).
- The ODSA subproject's mission is to define an open interface and architecture that enables the mixing and matching of silicon chiplets from different vendors via an open marketplace onto a single SoC. It is the first open physical and logical D2D interface and the first D2D interface to enable modular design by leveraging widely used transaction protocols.
- The ODSA interface supports various PHYs and packaging technology.

YOLE Intelligence

- d-Matrix has launched its second-generation chiplet platform for large AI chips using in-memory computing, called **Jayhawk**. It is the industry's **first Open Domain-Specific Architecture (ODSA) Bunch of Wires (BoW)-based chiplet platform**, offering energy-efficient die-die connectivity over organic substrates. Jayhawk uses a modular chiplet-based approach, providing scalability and efficiency for demanding ML workloads. Chiplets will be built based on both BoW and UCIe-based interconnects, allowing for a comprehensive and heterogeneous platform that is highly performant.

d-Matrix

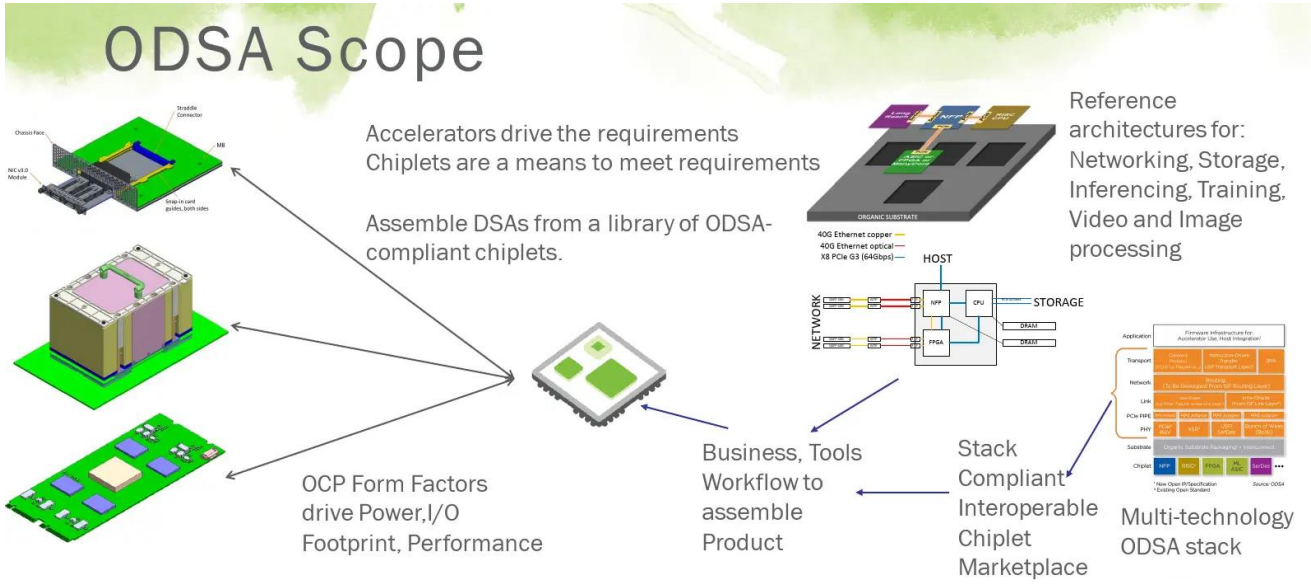
OPEN Compute Project®

Advantages

Chiplets can be seamlessly integrated into existing monolithic designs using current transaction protocols, allowing for the utilization of existing development tools, ecosystem, and software.

Abstraction layers provide flexibility for chiplet designers to choose the best components for their design while still ensuring compatibility with other chiplets. The choice of D2D PHY and packaging technology is no longer a critical decision that hinders the transition to chiplets.

Open D2D interfaces enable easy integration of heterogeneous chiplets from various vendors into a single product.



Source: ODSA

CHINA CHIPLET LEAGUE

First Advanced Cost-driven Chiplet Interface (ACC 1.0) released

- CCLL was founded in 2020 by Chinese R&D centers and players. The alliance's goal is to create an industrial platform based on local industrial policies, driven by the market and the industry, to encourage local companies to develop global Chiplet interconnection standards and a Chiplet technology open platform.
- In Feb 2023, CCLL announced the "Chip Interconnect Interface Standard - Advanced". The standard is a high-speed serial port standard optimized for domestic packaging and substrate supply chains, with a focus on cost control and commercial rationality. It was jointly drafted by the China Chiplet Industry Alliance and involves relevant industry standards.

Supplier: 长安汽车 CHANGAN AUTO; 东风汽车公司 DONGFENG MOTOR CORPORATION

Supplier: 经纬恒润 JINGWEI HIRAIN

Systems vendor: 科大讯飞 iFLYTEK; ONASIC 云海国创

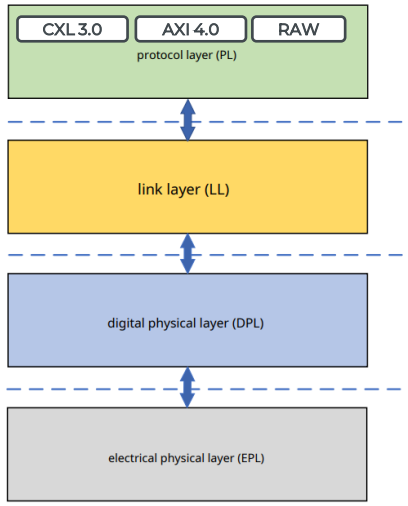
Chiplet solution vendor: Polar Bear Tech 北极雄芯

Ip vendors: 芯耀辉; Imagination

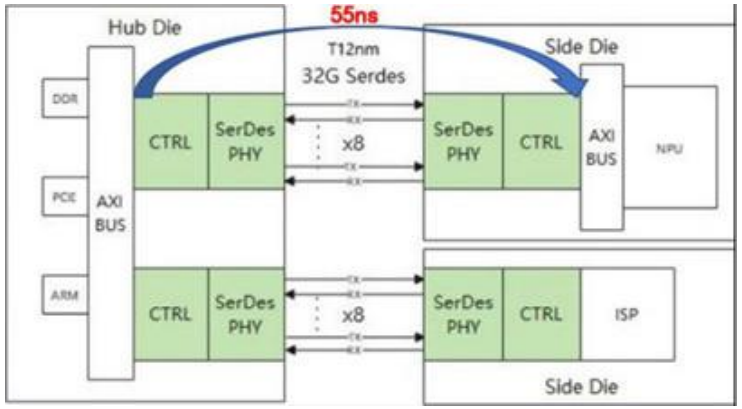
EDA: S2C EDA SOLUTIONS; 芯华章

OSATs: JSI; 摩尔精英 MooreElite.com

The Core Interconnect Interface Standard (ACC 1.0)

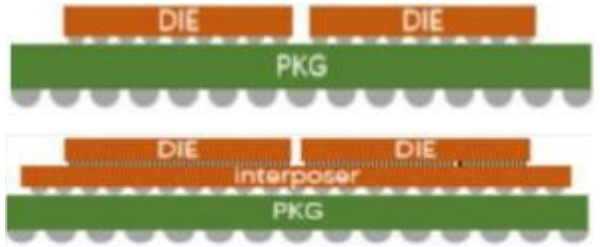


Structure Block Diagram (ACC 1.0)



D2D interface connection

YOLE Intelligence



Advanced Packaging

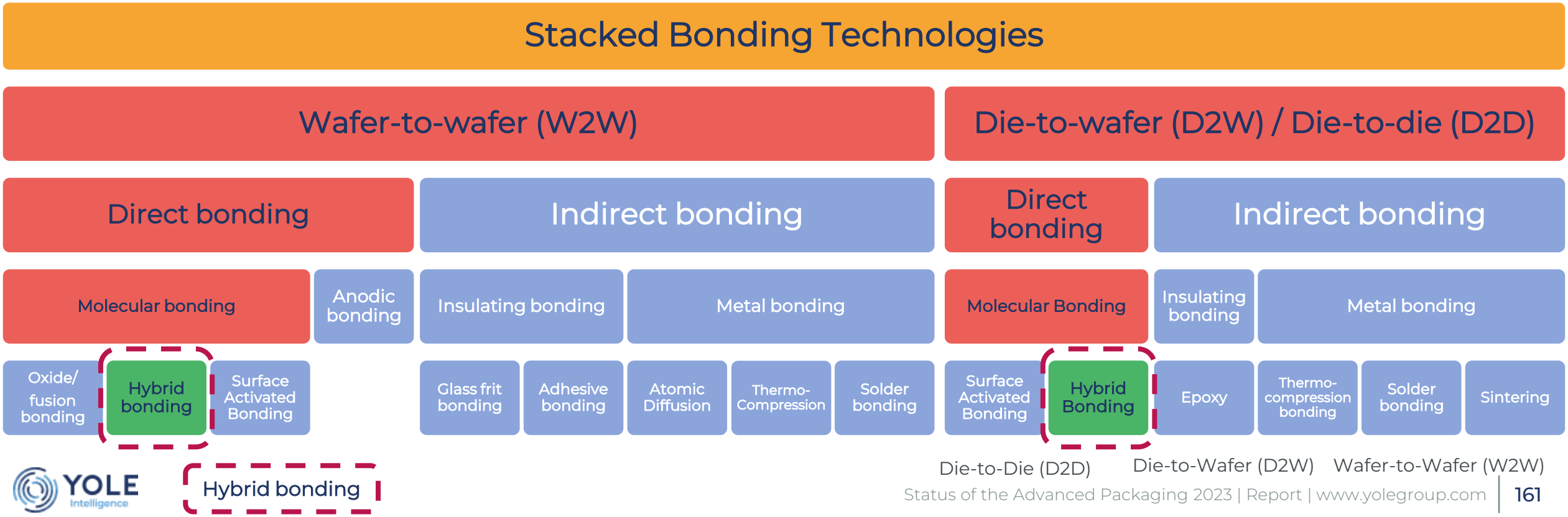
- **Low cost:** Supports 2D and 2.5D packages with optimized domestic substrates.
- **Small area:** Under the 12nm process, the area is 2.13 mm^2.
- **Fewer pins:** Uses high-speed serial SerDes transmission with only 38 signal pads.
- **Flexibility:**

Supports the misalignment of channels and comes with an eye chart analysis tool.

Hybrid Bonding Technology

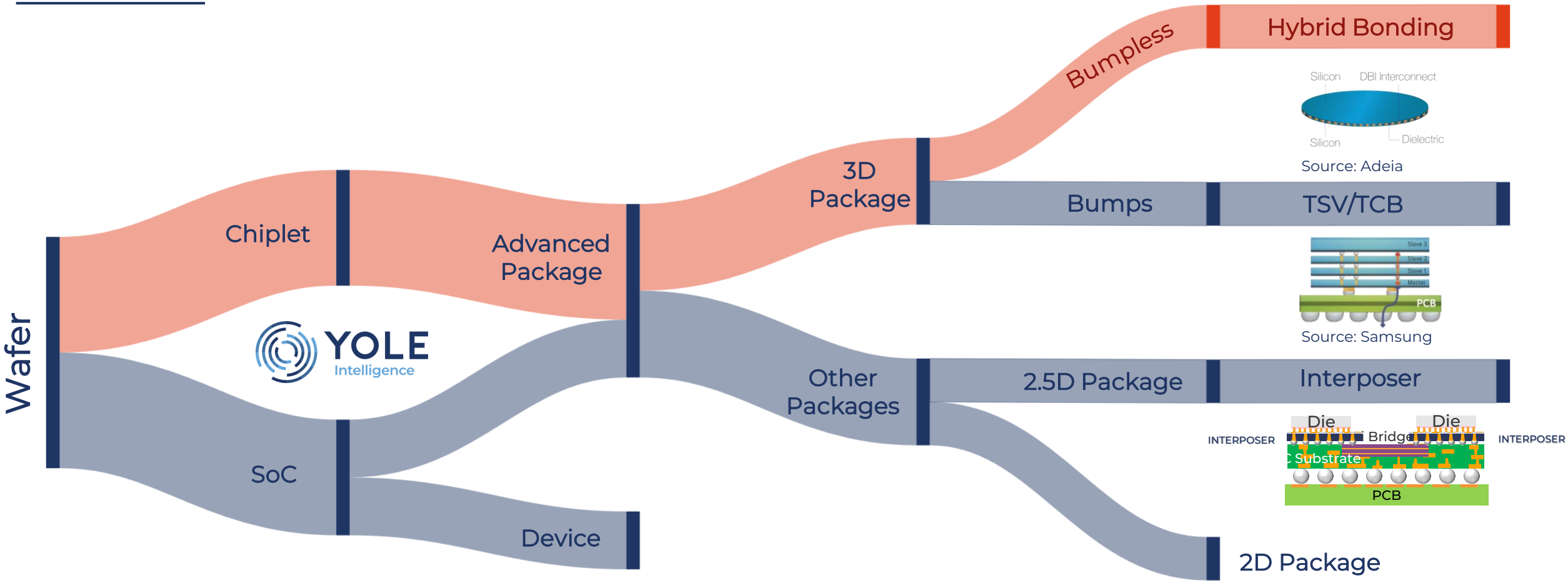
HYBRID BONDING
Where is hybrid bonding?

- The interconnection process between chips and substrates is based on either W2W or D2W assembly. This assembly can be done directly or with intermediate material.
- Hybrid bonding is a direct, molecular bonding of two functional materials: dielectric (thin films such as SiO_2 or polymer) and metal interconnects (copper, tungsten, etc.). **HB** is defined as a permanent bond that combines a dielectric bond with embedded metal to form interconnections. It has become known industry-wide, for example, as Direct Bond Interconnect (DBI®) from Xperi, although other players have developed the technology in parallel.
    - Hybrid bonding can be used in W2W and D2W (including D2D) assembly.



HYBRID BONDING

An Alternative of Transistor Scaling



Hybrid bonding is a direct, molecular bonding of two functional materials: dielectric (thin films such as SiO_2 or polymer) and metal interconnects (copper, tungsten, etc.). **HB** is defined as a permanent bond that combines a dielectric bond with embedded metal to form interconnections. It has become known industry-wide, for example, as Direct Bond Interconnect (DBI®) from Xperi, although other players have developed the technology in parallel.

HYBRID BONDING: ADVANTAGES AND CHALLENGES

Advantages

Advanced 3D Equipment Stacking	Hybrid bonding allows for the stacking of equipment in three dimensions, enabling higher performance and greater flexibility in system design
Maximum I/O	With hybrid bonding, it is possible to achieve maximum I/O density, resulting in faster data transfer rates and improved system performance.
Sub-10-µm Bonding Pitch	Hybrid bonding can achieve a bonding pitch of sub-10-µm, enabling the integration of even smaller components and devices.
Eliminates the Need for Bumps	Hybrid bonding eliminates the need for bumps, resulting in improved performance without power and signal loss
Higher Memory Density	Hybrid bonding allows for the integration of high-density memory, enabling the storage of more data in a smaller space
Expanded Bandwidth	By eliminating the need for bumps, hybrid bonding can expand bandwidth and improve signal transmission

Challenges

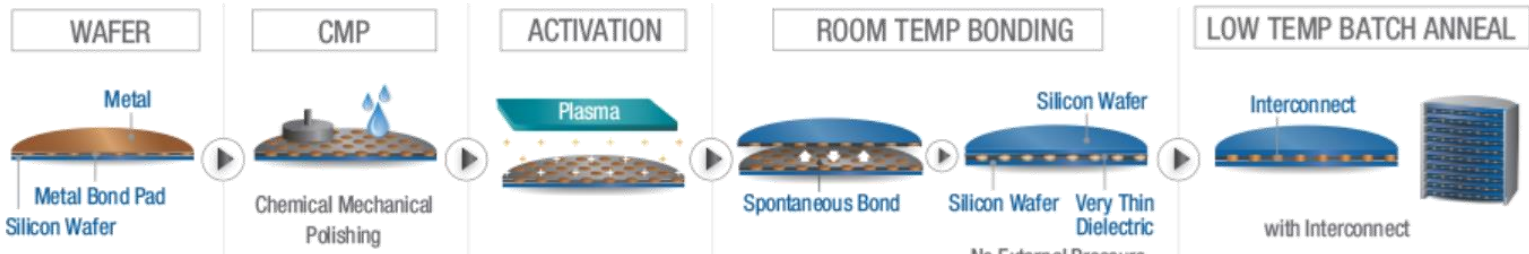
Surface Planarization and Cleanliness	are required to achieve high bond strength and yield. Any contaminants on the surface can negatively affect the bonding process, resulting in lower performance and yield
Interconnect Alignment	is crucial for low contact resistance. Misalignment can lead to poor electrical connectivity, resulting in reduced device performance.
High Annealing Temperature	The interconnect annealing temperature of 300 - 400°C is still too high for sensitive high-end devices such as memory and logic, which can lead to device degradation and failure.
Limited Throughput and Yield	The current limitations of the bonder (W2W or D2W) capabilities lead to limited throughput and yield, which is a significant challenge for large-scale production.
Pre-Bond and Post-Bond Electrical Testing	Electrical testing before and after bonding is difficult, and currently, there are no established standards for such testing
Long Lead Time for Equipment	The supply chain for specific equipment needed for the hybrid bonding process has a long lead time, which can delay the production schedule and increase costs.

HYBRID BONDING PROCESS FLOW

Note: shown here is the process flow established by XPERI (Adeia now), but other process developments have been done in parallel, e.g., Leti, Imec, TSMC ..etc.

W2W process flow

- Used for CIS, F2F logic, 3D NAND
- IN HVM from 2015/2016
- Specialized CMP tools and W2W bonders are used



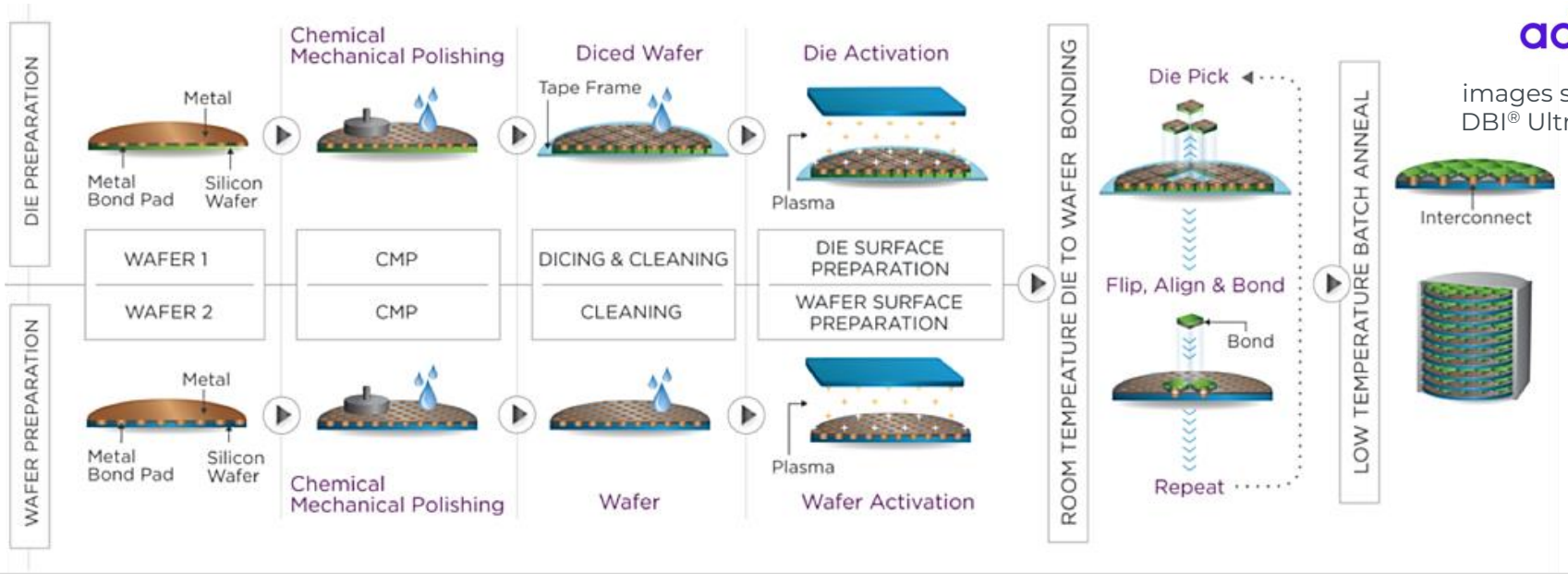
Interconnect patterning, CMP and activation done on both wafers

adeia

images source: Adeia DBI® process flow

D2W process flow

- Used for heterogeneous integration
- LVM expected in 2022
- Specialized CMP tools, singulation tools, and D2W flip chip bonders are used
- Singulated dies from source wafer are cleaned and activated collectively on tape frame (special plasma reactors or atmospheric plasma), and are transferred one-by-one to destination wafer



adeia

images source: Adeia DBI® Ultra process flow

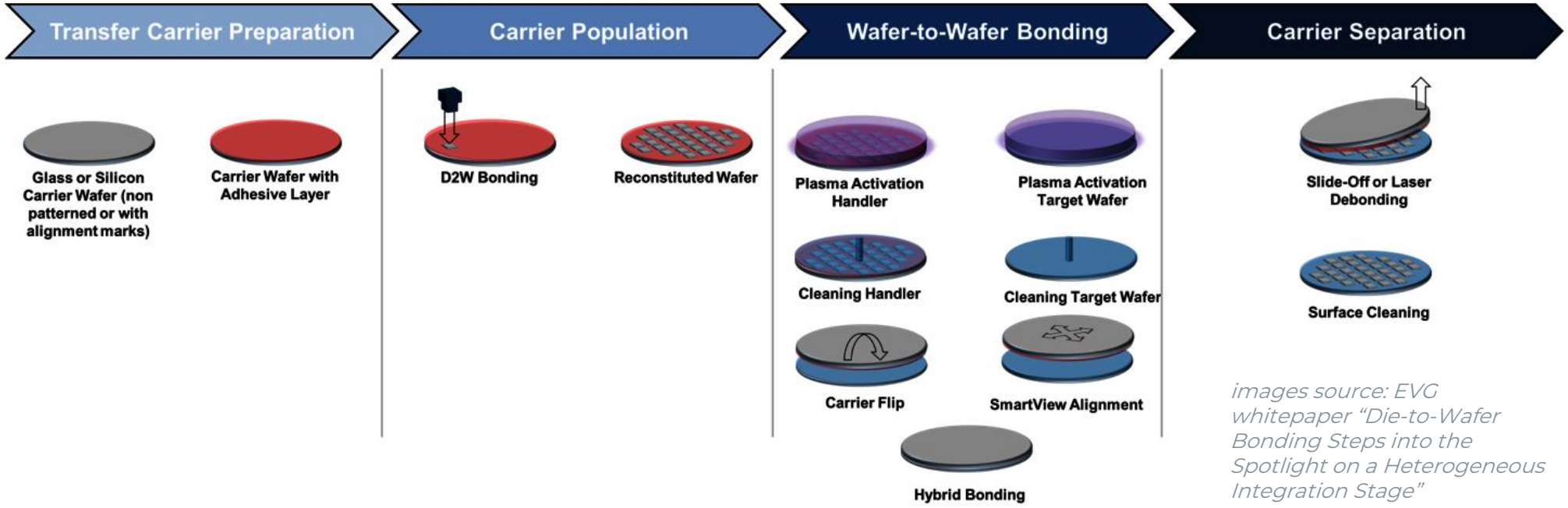
HYBRID BONDING PROCESS FLOW – COLLECTIVE D2W

Further diversification of the hybrid bonding process was proposed by W2W bonder equipment makers to increase the THP of the cleaning process (DP D2W, also called sequential D2W) and bonding process (Collective D2W). A variation of this process is presumably used in current TSMC stacking approach.

- Equivalent to DBI® Ultra process flow
- Collective cleaning done in 300 mm platforms with use of carriers and temporary bonding followed by debonding

Collective D2W

- Estimated to be used in SenSWIR Sony in 2020
- speculated to be used for HBM3+ in 2024/ 2025.
- Extension of DP D2W
- Collective cleaning **and bonding** done in 300 mm W2W bonder with use of carriers and temporary bonding followed by debonding
- High-precision die attach tools are needed for carrier population



images source: EVG whitepaper "Die-to-Wafer Bonding Steps into the Spotlight on a Heterogeneous Integration Stage"

HYBRID BONDING – SUPPLY CHAIN

Process

IP Providers

adeia, imec, cea leti, Fraunhofer, A*STAR Agency for Science, Technology and Research SINGAPORE

Fabless

OmniVision, AMD, Qualcomm, GRAPHCORE, arm, Meta

IDM and foundries

SK hynix, life.augmented, intel, SONY, UMC, SAMSUNG, skywater, GlobalFoundries, NANYA, KIOXIA, tsmc, Tower Semiconductor

Suppliers

Equipment suppliers

EVG, ASM INTERNATIONAL, Besi, PVA TePla, set, SUSS MicroTec, KLA, APPLIED MATERIALS

Materials suppliers

TEL TOKYO ELECTRON, Infinite Ideas, MSYS, ShinEtsu, CORNING, brewer science, DUPONT, HD MicroSystems

Manufacturers

IDM

SK hynix, life.augmented, NANYA, SONY, SAMSUNG, KIOXIA, intel, Micron

Foundries

tsmc, Tower Semiconductor, GlobalFoundries, UMC

Device providers

IDM

life.augmented, SK hynix, SONY, NANYA, SAMSUNG, intel, KIOXIA, Micron

Fabless

XILINX, AMD, OmniVision, Qualcomm, NVIDIA, GRAPHCORE, Meta, arm, Google

Govermental institutions

Sandia National Laboratories

Raytheon Technologies

SUMMARY

Scaling is no longer the only semiconductor driver – new markets and applications are developing with an emphasis on device functionality, and advanced Packaging (AP) is becoming crucial for semiconductor innovation. AP is seen to increase the value of a semiconductor product, adding functionality and maintaining/improving performance while lowering cost. Heterogeneous integration using Advanced Packaging technologies is propelling semiconductor innovation; a key trend is the adoption of a chiplet-based approach to attain heterogeneous integration by mixing and matching dissimilar IP blocks with different technology nodes.

Big IDMs and foundries, the pioneers of Moore's Law and mainly relying on front-end scaling for performance improvements, are increasingly looking at heterogeneous integration using AP technology to complement their front-end effort.

TSMC has emerged as the undisputed leader in high-end Advanced Packaging and is excelling in its development, production, investment, and IP protection. Its 3D Fabric solution comes with FOWLP and 2.5D/ 3D technologies in InFO and CoWoS platforms, which have been commercialized already in several products by OEMs like Apple, Xilinx, Tesla, and AMD.

Samsung Electronics is a pioneer in the development of 3D TSV stacking technology for HBM memory and is one of the few players that has invested in this technology since the 2000s. Samsung Electronics' AP portfolio includes SiP / flip-chip / fan-out technologies addressing mobile, 5G, and automotive markets, as well as four platforms – namely, I-Cube, R-Cube, X-Cube, and H-Cube – that support HPC, data center, AI, 5G, cloud, and network products.

Intel's IDM 2.0 strategy aims to strengthen its Advanced Packaging business, moving forward with a chiplet-based architecture approach with its EMIB, Foveros & Co-EMIB architectures. Enlarging its Advanced Packaging toolbox, Intel announced two other new technologies which are extensions of Foveros architecture: Foveros Omni and Direct.

In Advanced Packaging, players are pursuing higher levels of interconnect density through a 3D packaging platform. Cu Redistribution Layers (RDLs) and Cu vias are commonly adopted as interconnection solutions. The expectation is to move towards sub-micron pad pitch, driving the introduction of hybrid bonding (HB) technology that allows metal-metal and oxide-oxide face-to-face stacking with <10µm bump pitch. It has been demonstrated with W2W in CMOS Image Sensor (CIS) products and later with D2W and D2D development on other applications. HB is proven to be the key to Moore's Law at the system level. Various players are working on 3D SoC using HB, with memory-on-logic stacked 3D IC for HPC and data center applications. TSMC is the leading IP Player, and Samsung Electronics is the only company with similar patents that could potentially compete with TSMC. Intel is leveraging its collaboration partner CEA Leti to progress on HB.

Advanced packaging involves different equipment and processes than traditional packaging. Examples are new substrate materials, lithography process, laser drilling, CMP, KGD test, etc. AP players are investing huge amounts in developing and introducing new materials and processes.

NOTEWORTHY NEWS ON ADVANCED PACKAGING

NOTEWORTHY NEWS ON SEMICONDUCTORS

Secure Domestic Supply Chain

The trend towards regional independence in chip manufacturing is becoming increasingly important as countries seek to secure their semiconductor supply in the face of supply chain disruptions.

USA	Oct 2022	*U.S. government imposes new export regulations and adds 31 companies to 'the entity list' in response to China's growing market access to advanced technology*
USA	Aug 2022	*U.S. President Biden sent $53B to US Chipmakers by signing CHIPS Act into law*
Europe	Mar 2023	*Germany is being asked for an additional $5B for Intel's plant in Magdeburg*
Europe	Feb 2023	*The new UK government is under pressure due to the delay in publishing " The UK Chip Strategy" which* outlines UK efforts to support the local chip industry and players. UK will look to bolster its domestic strengths such as chip design, compound semiconductors, and R&D.
Europe	Nov 2022	*European Union agrees on 45-billion-euro plan to reduce dependency on Asia for chip production by 2030*
Europe	Aug 2022	*Italy's* new government is willing to discuss a possible multibillion-euro investment with Intel in Italy. The company was close to assuring a $5B investment in a plant in Italy.
Asia	May 2023	*China* Declares Micron's Products as National Security Risk, Banning them from Key Infrastructure Projects
Asia	Mar 2023	*India* and *US* to boost collaboration in the semiconductor industry through private-sector task forces and incentive plans
Asia	Jan 2023	*South Korea* announces tax breaks for semiconductor industry to compete with China, Japan, and Taiwan amidst the increasing global chip shortage.
Asia	Dec 2022	*China* plans a massive $143 billion support package to boost self-sufficiency in the semiconductors amidst U.S. restrictions
Asia	Dec 2022	*India announces its* willingness to increase investment in India Semiconductor Mission, stating $10 billion is only the beginning.
Asia	Nov 2022	*Japan* to invest $500 million in new chip company led by Sony and NEC to regain status as the leading maker of advanced chips.

NOTEWORTHY NEWS ON ADVANCED PACKAGING

Collaboration Activities

China Chiplet League Aims to Catch Up with UCIe, ODSA, and HIR focusing on chiplet and HI.

Mar 2023	*The China Chiplet League* is a group of Chinese companies engaged in chip design, production, packaging, and testing. They announced their own standard interface for combining multiple chiplets on a single substrate. The Chinese Chiplet Interconnect Interface Standard, also known as ACC 1.0 (Advanced Cost-driven Chiplet Interface 1.0), is meant to enable custom multi-chiplet designs developed by China-based companies. The goal of the China Chiplet League is to ensure that ACC 1.0 will be a cost-effective and feasible solution for Chinese chip designers.	CCLL CHINA CHIPLET LEAGUE 中国CHIPLET产业联盟
Mar 2022	*ASE, AMD, Arm, Google Cloud, Intel Corporation, Meta, Microsoft Corporation, Qualcomm, Samsung, and TSMC established the Universal Chiplet Interconnect Express (UCIe), an industry consortium that aims to bring the industry together by standardizing die-to-die interconnects and addressing the need for more customizable package-level integration. Nvidia and Alibaba joined as board members. The future versions of UCIe will support 3D-stacked chiplets and optical interfaces, which will further reduce interconnect trace length and area footprint and will replace SerDes-based interconnects to reduce power and increase reach. The adoption of UCIe will increase design productivity and reduce time-to-market.*	UCIe Universal Chiplet Interconnect Express
Dec 2021	*Heterogeneous Integration Roadmap (HIR) released its 2021 edition (3rd edition) with a total of 24 chapters to identify complex challenges and potential solutions for meeting technical requirements for the next 1-2 decades. HIR gathers experts from the semiconductor community worldwide to contribute to each chapter. HIR primarily integrates technologies including Chiplet and SiP-based architectures. The 4th edition will be released in 2023.*	HIR HETEROGENEOUS INTEGRATION ROADMAP
Mar 2019	*Open Domain Specific Architecture (ODSA) chartered within Open Compute Project (OCP). The mission is to define an open interface and architecture that enables the mixing and matching of silicon chiplets from different vendors via an open marketplace onto a single SoC. More than 10 companies announced the implementation of ODSA specifications.* d-Matrix announced Jayhawk, the industry's first Open Domain-Specific Architecture Bunch of Wires (BoW)-based chiplet platform for energy-efficient die-die connectivity over the organic substrate.	OPEN Compute Project ®

NOTEWORTHY NEWS ON ADVANCED PACKAGING

Investment and Capacity Expansion (1/3)

February 2023	**Intel is considering to boost its investment in Vietnam packaging plant** Intel is considering an increase its existing $1.5B investment in Vietnam to expand its chip testing and packaging plant. The investment may happen in the future years and include more than another $1B of investment. While the company did not yet announce any official new investment for Vietnam, alternative investments in Singapore or Malaysia are also possible. In the last year Intel announced other investments in packaging capacity in Rio Rancho, New Mexico ($3.5B), in Penang, Malaysia ($7.1B) and negotiations with Italy leveraging a $5B investment.
February 2023	**Chinese startup Cambricon gets new funds to advance 7nm chips for ChatGPT-like applications** China-based AI chip startup Cambricon Technologies has been approved to issue CNY1.672 billion (US$244.087 million) in A-shares to specific target investors, allowing the company to develop chip solutions associated with AI generated content concept and related applications like ChatGPT. So far, Cambricon has established a 7nm process chip design platform and an advanced multi-chiplet package. It has also independently designed the MLU-link multi-chiplet interconnection technology.
February 2023	**Amkor Technology and GlobalFoundries to Provide At-scale Semiconductor Test and Assembly Services in Europe** Amkor and GlobalFoundries (GF) announced that the two companies have formed a strategic partnership to enable an EU/US supply chain from semiconductor wafer production at GF to OSAT services at Amkor in Porto, Portugal. GF plans to transfer its 300mm bump and sort lines from its Dresden site to Amkor's Porto operations to establish the first at-scale back-end facility in Europe. GF will maintain ownership of its transferred tools, processes, and IP in Porto. This partnership will provide services within the EU and expand the US-European semiconductor supply chain, specially in the automotive market.
February 2023	**Integra Technologies Selects Kansas for Largest OSAT Semiconductor Project** Integra Technologies and Kansas Government announced the approval of Integra's Attracting Powerful Economic Expansion (APEX) incentive application for an expansion project holding a $1.8 billion investment on receiving federal CHIPS for America funding. Integra's expansion plans aim to support the U.S. semiconductor domestic supply chain with advanced OSAT services.
January 2023	**SPIL starts operating new plant in central Taiwan** OSAT firm Siliconware Precision Industries (SPIL) has kicked off operations at its new plant in Changhua, central Taiwan. This will be SPIL's main high-end packaging and testing base. The company plans to invest a total of NT$80 billion (US$2.64 billion) in the new plant project. The project will be completed in four phases and the second one will start by the end of 2024.

NOTEWORTHY NEWS ON ADVANCED PACKAGING

Investment and Capacity Expansion (2/3)

January 2023	**New China Resources Microelectronics (CR Micro) fab and backend site in Chongqing kicks off operations** China Resources Microelectronics (CR Micro) has kickstarted the operations of its new 12-inch fab and an advanced backend site in Chongqing, China. The backend site will focus on testing and packaging power semiconductors for automotive electronics and industrial control applications, utilizing module-, wafer-, architecture- and panel-level packaging processes. Chongqing branch of CR Micro is named SiPLP, as it will focus on testing and packaging components utilizing panel-level packaging processes.
January 2023	Zhejiang Chuanghao Semiconductor is investing a total of $1.5B for a new IC substrate production facility in YiWu, China. A groundbreaking ceremony took place in January 2023 and the building is scheduled to be completed in 2024. It will produce based FCCSP and FCBGA high-end substrate for China domestic and oversea customer.
November 2022	**ASE starts building a new Assembly and Testing Facility in Penang, Malaysia** The new facility at ASE Malaysia (ASEM) will comprise two buildings with a built-up area of 982,000 square feet. ASE is investing $300M over five years to expand its production floor space, procure advanced equipment, and train more engineering talent. The new Penang facility is scheduled for completion in 2025 and will create 2,700 additional job opportunities. It will focus mainly on the production of the copper clip and image sensor packages.
November 2022	**Lam Research extends its presence in advanced packaging with the Semsysco acquisition** Lam Research acquired equipment supplier Semsysco, a provider of wet-processing semiconductor equipment. With this acquisition, Lam gains capabilities in advanced packaging, including leading-edge logic chips and chiplet-based solutions for HPC and AI. Additionally, the company gained an R&D facility in Austria focused on substrates and heterogeneous packaging.
October 2022	**TSMC Launches OIP 3DFabric Alliance** TSMC announced the Open Innovation Platform® (OIP) 3DFabric Alliance, which joins forces with partners such as AMD and AWS to accelerate 3D IC ecosystem innovation and readiness, offering best-in-class solutions for semiconductor design, memory modules, substrate technology, testing, manufacturing, and packaging. TSMC OIP consists of six alliances: the EDA Alliance, IP Alliance, Design Center Alliance (DCA), Value Chain Alliance (VCA), Cloud Alliance, and now the 3DFabric Alliance. Partners of the new 3DFabric Alliance have early access to TSMC's 3DFabric technologies, enabling them to develop and optimize their solutions in parallel with TSMC.

NOTEWORTHY NEWS ON ADVANCED PACKAGING

Investment and Capacity Expansion (3/3)

September 2022	**ASE announces plans to build the world's first 5G SA mmWave NR-DC smart factory with Qualcomm** ASE unveiled plans to build a new 5G mmWave NR-DC SA (New Radio-Dual Connectivity Standalone) smart factory supported by the Industrial Development Bureau and Qualcomm Technologies Inc. The collaboration aims to enable the digital transformation of factory processes by facilitating 5G wireless infrastructure integration, smart heterogeneous equipment integration, and OT security system integration.
September 2022	**EV group expands collaboration with ITRI on heterogeneous integration process development.** EV Group works with Taiwan's Industrial Technology Research Institute (ITRI) to develop advanced heterogeneous integration processes. ITRI has established the *Heterogeneous Integration Chip-let System Package Alliance (Hi-CHIP),* a chiplet ecosystem that includes package design, testing, verification, and pilot production. EVG has provided several of its most advanced wafer bonding and lithography systems for ITRI's state-of-the-art facility.
September 2022	**MediaTek to produce HPC chips using CoWoS in 2023. The company is expanding its supply chain by partnering with Intel Foundry Services (IFS)** MediaTek will reportedly use TSMC's CoWoS packaging technology to produce its new HPC chips, using a heterogeneous integration approach to integrate its HPC chips with HBM. Small volumes should start being shipped by the end of 2022, and mass production will ramp up in 2023. Taiwanese OSATs (ASE and SPIL) could leverage some packaging and assembly outsourcing services. On the other hand, MediaTek is looking to diversify its supply chain and expand its chip production to the U.S. and Europe. Mediatek and IFS announced a strategic partnership to manufacture chips for a range of intelligent edge devices and will begin by using Intel 16 process technology.
September 2022	**SkyWater to expand advanced packaging capacity** SkyWater will leverage a $36.5M funding from the U.S. Department of Commerce to expand its advanced packaging facility operations in Florida to accelerate U.S. domestic packaging capabilities. The funding will be utilized to expand the clean room and purchase tools and machinery. SkyWater is developing WLP, Si Interposer, and hybrid bonding technologies and will support the domestic supply chain including aerospace & defense, automotive, medical, consumer, industrial, and computing end-markets.

NOTEWORTHY NEWS ON ADVANCED PACKAGING

New Packaging Technologies (1/2)

March 2023	JCET provides advanced packaging solutions for 4D millimeter-wave radar to meet the growing demand for autonomous driving technology in the automotive industry. The company offers a complete portfolio of flip-chip chip scale packages and fan-out wafer level packages for high-precision millimeter-wave radar chips, including reliable solutions for System-on-Chip products with integrated Antenna-in-Package. The eWLB packaging solution plays a leading role in the millimeter-wave radar transceiver chip MMIC.
March 2023	ASE has announced the launch of its latest Fan-Out-Package-on-Package (FOPoP) solution, designed to provide exceptional bandwidth advantages for the mobile and networking markets. The FOPoP package reduces electrical path and increases bandwidth density, enabling engine bandwidth expansion up to 6.4 Tbps per unit. The packaging platform is enhanced for increasing complexity and high-performance needs by enabling RDL on both sides of the die for increased integration and functionality. The FOPoP structure provides higher interconnection density and integration through a finer line space RDL, a shorter interconnect length, and a smaller, thinner form factor.
February 2023	JCET Group announced that is supplying advanced packaging HVM solution to several customers for 4D mmWave automotive radar. These solutions include FCCSP and FOWLP (eWLB technology). eWLB is the leading role packaging technology for mmWave radar transceiver chip while FCCSP is the most suitable solution for mmWave System-on-Chip (SOC) products with integrated Antenna in Package (AiP). JCET's 4D mmWave radar packaging solutions are available to meet the customers' L3+ level autonomous driving requirements. JCET has also cooperated with an industry-leading mmWave customer to develop a smaller form factor package with Antenna-on-Mold and double-sided RDL solutions.
February 2023	Adeia announced that Qorvo, a leading global provider of connectivity and power solutions, has licensed its proprietary hybrid bonding technology. According to Qorvo, hybrid bonding introduces new opportunities to optimize the architecture of the RF front-end semiconductor devices and modules to enhance functionality, performance and size of the solutions.
February 2023	Intel has announced the new Intel Xeon W-3400 and Intel Xeon W-2400 desktop workstation processors (codenamed Sapphire Rapids), led by the Intel Xeon w9-3495X, the most powerful desktop workstation processor in the family. With a breakthrough new compute architecture, faster cores and new embedded multi-die interconnect bridge (EMIB) packaging, the Xeon W-3400 and Xeon W-2400 series of processors enable unprecedented scalability for increased performance.

NOTEWORTHY NEWS ON ADVANCED PACKAGING

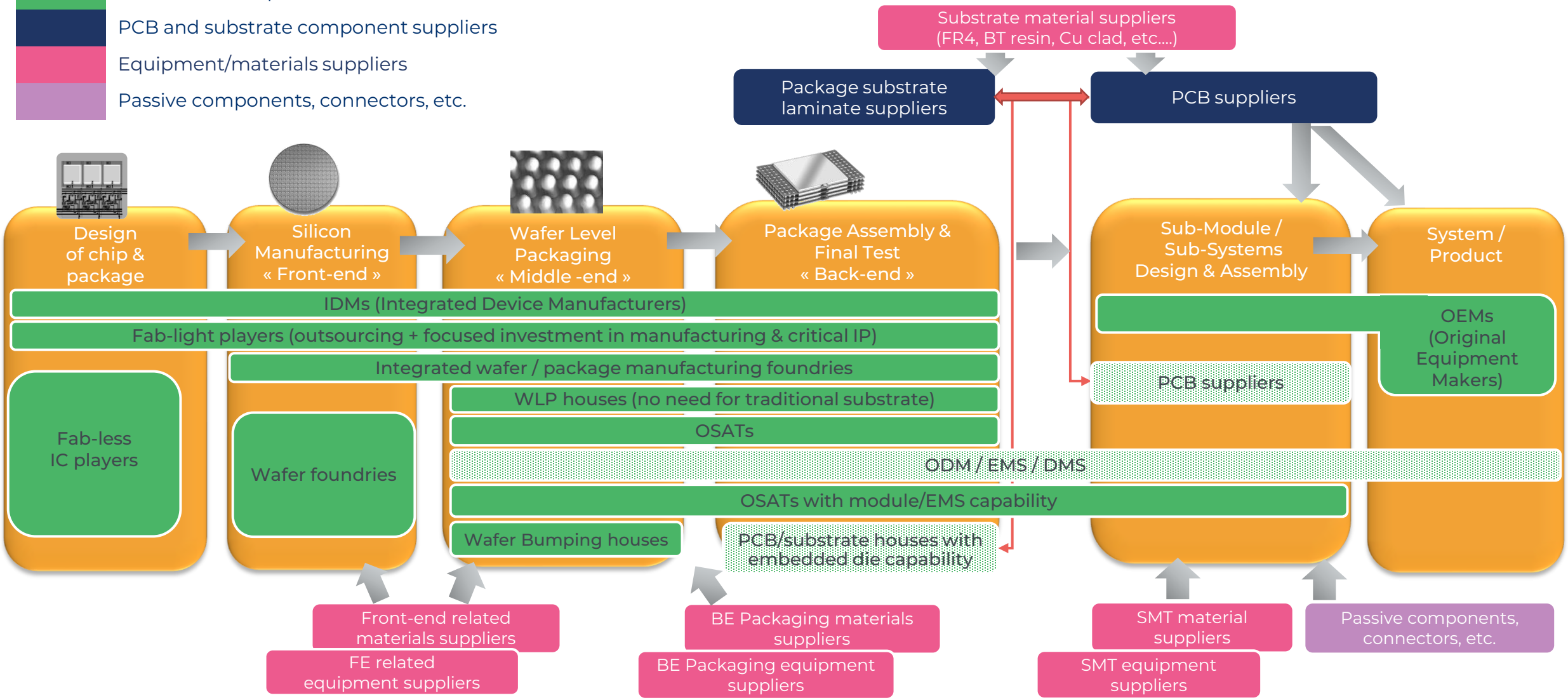
New Packaging Technologies (2/2)

February 2023	SEMCO developed an automotive IC substrate (FCBGA) applicable to ADAS. SEMCO targets electric vehicle market with the aim to become the global no. 1 company in high-end automotive IC substrates. The company applied its microcircuit technology to reduce the circuit width and spacing by 20% and implementing more than 10,000 bumps in a limited space. SEMCO secured product reliability by increasing the IC substrate size to respond to multi-chip packages and improving the bending strength according to the increase in the number of layers.
February 2023	UMC and Cadence have announced that the Cadence 3D-IC reference flow has been certified for UMC's chip stacking technologies, meaning UMC's hybrid bonding solutions are now ready to support the integration across a broad range of technology nodes suitable for edge AI, image processing, and wireless communication applications. Using UMC's 40nm low power (40LP) process as a wafer-on-wafer stacking demonstration, the two companies collaborated to validate key 3D-IC features in this design flow, including system planning, chip and packaging implementation, and system analysis.
January 2023	China-based electronic design automation (EDA) company Empyrean Technology has begun research and development of chiplet-based advanced packaging as well as AI-based design automation. AI-based design automation has become increasingly crucial for chip design, while chiplet-based advanced packaging has been regarded by some as an alternative path forward as US sanctions constrain Chinese chip development at 16/14nm or below.
January 2023	JCET has achieved stable mass production of its XDFOI Chiplet high-density multi-dimensional heterogeneous integration series process, which allows for the shipment of 4nm node multi-chip system integrated packaging products for international customers. The technology enables collaborative design and integration of finished chip products, resulting in a highly integrated heterogeneous package.
October 2022	ASE has announced the industry's first Fan-Out Chip on Substrate Chip First (FOCoS-CF) with encapsulant-separated redistribution layer (RDL) and Chip Last (FOCoS-CL) semiconductor packaging solution, designed to enhance the performance for High-Performance Computing (HPC), under the ASE VIPack™ platform. This chiplet integration technology will allow two or more chips to be reconstituted into a fan-out module and assembled on a substrate, providing greater memory and computing power. The FOCoS-CL technology will particularly improve High Bandwidth Memory (HBM) integration, leading to optimization in power efficiency and space savings. This innovative technology approach will provide a considerable competitive advantage for ASE's customers in meeting stringent miniaturization, bandwidth, latency, and other evolving design and performance requirements.

PLAYERS AND SUPPLY CHAIN

SEMICONDUCTOR SUPPLY CHAIN – WHAT IS CHANGING?

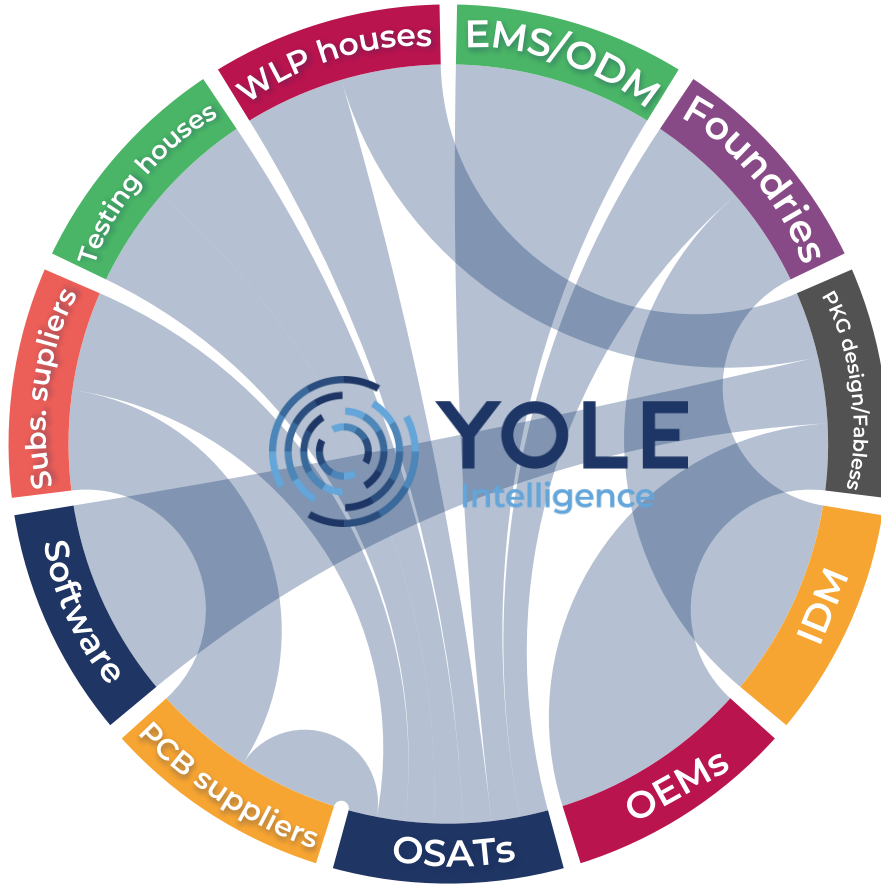
Semiconductor production chain
PCB and substrate component suppliers
Equipment/materials suppliers
Passive components, connectors, etc.



THE SEMICONDUCTOR SUPPLY CHAIN IS CHANGING AT VARIOUS LEVELS

In order to expand the business and explore new areas, players in the semiconductor supply chains are moving to different business models.

Business model	Expansion to	Motivation
Software / services	IC design	• System level integration & customization • Control of supply chain
Foundries	OSATs / Packaging	• System level integration • Provide turnkey solution • Boost foundry business
Substrate / PCB suppliers	OSATs / Packaging	• Minimize substrate business loss due to WLP adoption • Leverage existing infrastructure & experience
EMS/ODMs	OSATs / Packaging	• Move up the value chain • Improve profit margin
OSATs	Testing	• Provide turnkey assembly solutions to customers • Open additional revenue stream
Testing houses	OSATs / Packaging	• Provide turnkey assembly solutions to customers • Open additional revenue stream
IDMs	Foundries	• Leverage Si manufacturing experience to open additional revenue stream • Utilize idle capacity of fab
Substrate suppliers	PCB	• Exploit the recent trends of “substrate-like PCB” adoption • Leverage existing infrastructure & know how



Foundries like TSMC entering fully-fledged into the Advanced Packaging domain have completely changed the game. With $5.3B packaging revenue in 2022, TSMC is already ranked #4 among OSATs. TSMC’s CapEx for 2023 is estimated to be $3.2B to $3.6B for Advanced Packaging and mask-making businesses.

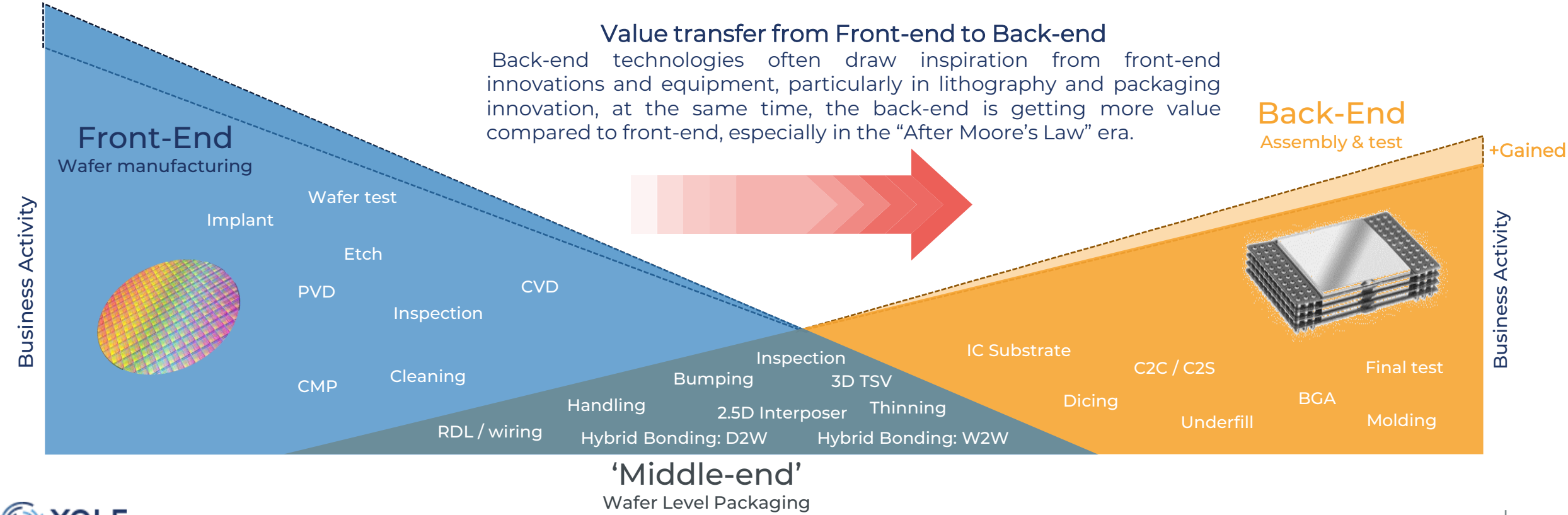
PACKAGING SUPPLY CHAIN ANALYSIS

Wafer-Level-Packages are changing the standard front-end/back-end supply chain

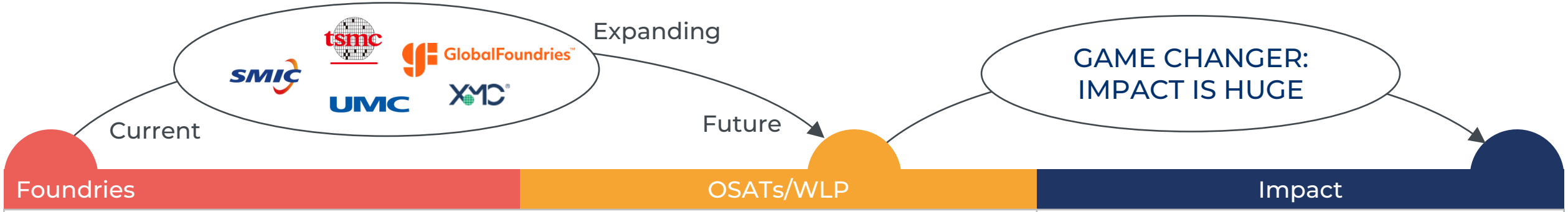
- With packaging at wafer-level, players dedicated to front-end but having wafer equipment are now able to go further along the manufacturing chain. Given their front-end capabilities, foundries and IDMs can play in the high-end part of advanced packaging since they can leverage their front-end capabilities and know-how.
- With the same objective of enlarging their scope, OSATs can go further in their processing steps, since 'packaging' can start earlier in the manufacturing chain, at the wafer-level.
- A 'middle-end' zone between front-end and back-end, where bumping and packaging can be executed at the wafer-level, can be reached by OSATs, WLP Houses, and IDMs, depending on the technology we are speaking about. Processes like TSVs and hybrid bonding are still retrained to foundries and IDM, since although they are considered packaging technologies, they still need front-end capabilities.

Value transfer from Front-end to Back-end

Back-end technologies often draw inspiration from front-end innovations and equipment, particularly in lithography and packaging innovation, at the same time, the back-end is getting more value compared to front-end, especially in the "After Moore's Law" era.

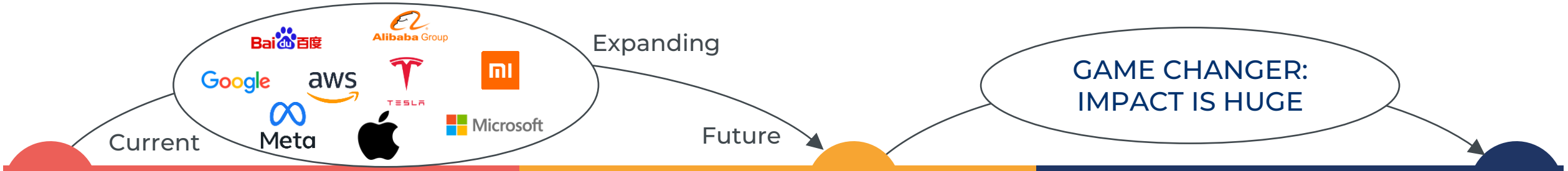


IMPACT OF SEMICONDUCTOR SUPPLY CHAIN CHANGES (1/6)



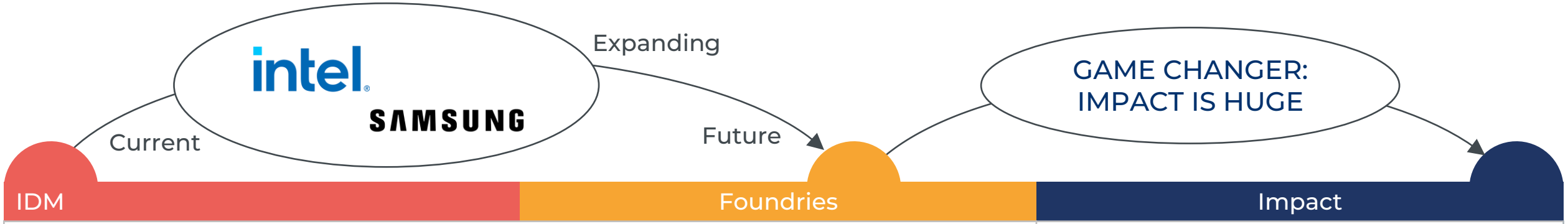
Foundries	OSATs/WLP	Impact
• Foundries such as TSMC expanding into the packaging area have a huge impact on the OSAT business, especially at the high-end. • TSMC has already entered the Advanced Packaging business with high-density fan-out (InFO), 2.5D/3D IC packaging (CoWoS) and SoIC. TSMC is aggressively expanding its high-end packaging portfolio with various InFO variants (InFO-oS, InFO-AiP, InFO-SoW, InFO-LSI), SoIC-CoW, SoIC-WoW, 3D Multi-stack (MUST) system integration technology, 3D MUST-in-MUST (3D-MiM) fan-out package. With its mature InFO product line-up, increased investment in SoIC package infrastructure, and chiplet paradigm shift over the next 2-3 years, TSMC is in a good position to take advantage of the heterogeneous integration revolution. • UMC is a key supplier of Si interposers for 2.5D packaging. Its partnership with Xperi, might be destabilized by the geopolitical tensions, to optimize and commercialize the ZiBond and DBI technologies for semiconductor devices, including image sensors, radio frequency (RF), MEMS, display drivers, touch controllers, SoC, analog, power, and mixed-signal devices. ZiBond & DBI support wafer-to-wafer (W2W) and die-to-wafer (D2W) bonding and 3D interconnect implementations. Furthermore, UMC delivers complete back-end turnkey services through close partnerships with OSATs such as Chipbond in 2021, a packaging specialist in LCD driver assembly and testing. • SMIC got a green light to raise a $2.5B Shanghai IPO. It makes sense for SMIC to invest in the high-end AP activity (3D SoC, 2.5D, hybrid bonding, etc.) and evolve to a system foundry model like TSMC. In the coming days, we expect a rebound activity from SMIC in the AP landscape. • XMC provides 3D IC packaging for image sensors, 3D stacked memory, HBM, and high-performance applications. Its 3DLink™ Technology Platform includes TSV stacking, hybrid bonding, and multi-wafer stacking technologies. XMC is one of the first manufacturers of image sensors using TSV. Hybrid bonding technology has completed R&D and is about to start production. XMC announced its 3DLink™ would be applied in the Xi'an UnilC SeDRAM platform.	For fabless, this supply chain trend provides more assembly / packaging options as well as accessibility to high-end 3D packaging technology For IDMs, more system manufacturers may bring chip design in-house, attracted by the prospect of cutting-edge turnkey services (latest Si node manufacturing technology coupled with Advanced Packaging) OSAT business is being cannibalized by foundries entering the packaging domain, particularly in high-end APUs for mobile by TSMC. Cooperation between foundry and OSAT should be crucial for OSATs to keep their businesses As foundries provide high-end WLP services, end customers will move from substrate-based packaging (e.g., FC BGA/CSP) to fan-out WLP. E.g., Apple adopting TSMC InFO technology seriously hit the Taiwanese substrate suppliers

IMPACT OF SEMICONDUCTOR SUPPLY CHAIN CHANGES (2/6)



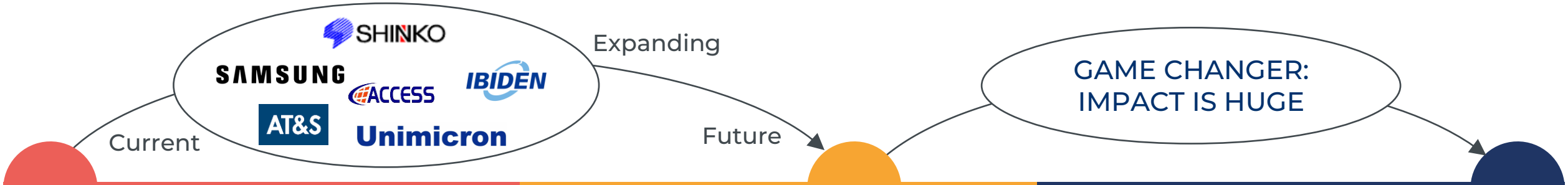
Software / Services / OEMs	IC-packaging design / Fabless	Impact
• Software companies are staffing or acquiring IC companies to develop their own processors. The goal is to design custom-made solutions for its specific products, being able to differentiate from the competition while taking control of its intellectual property. At the same time, companies have started to rely less on Fabless/IC design companies to have more control over the supply chain. • This trend continues today, as Google announced the 2nd-generation Tensor G2, while Meta developed the next gen. of its Big Basin server, called Grand Teton. Also, Baidu recently announced that the 3rd-generation of its Kunlun AI Chip will be mass-produced in 2024. Microsoft might soon release its Athena chip, and Alibaba entered the race with its Hanguang 800 Chip. These companies are strengthening their positions in the supply chain. • Mobile companies like Xiaomi, Apple, and Google started to develop their own smartphone processors, and others like Oppo may do the same in the next few years. Apple moved on from Intel's processors to their own M-series (M2 until now) for iPads and iMacs, and Google will reportedly introduce its self-designed CPUs for Chromebooks. • Automotive OEMs are increasingly involved in the chip-package design or building solid partnerships with IC players (Nvidia with Audi, ZF, automotive industry supplier). After Dojo D1, Tesla is still working on new in-house chip development for autonomous vehicles and recently announced their new FSP chip. Volkswagen Group, signed through its software subsidiary Cariad, a partnership with ST microelectronics to co-design its own chips, while Mercedes signed with Nvidia.		IDMs' business loss is foundries' gain. Software companies & OEMs design chips in-house and give manufacturing business to foundries. OEMs/software companies control the supply chain up to the PCB level. OSATs & substrate /PCB suppliers gain more technical expertise from closer cooperation and deeper insights into industry roadmap & system design. As software companies & OEMs become more independent of fabless and IDM, business impact is negative for fabless and IDM.

IMPACT OF SEMICONDUCTOR SUPPLY CHAIN CHANGES (3/6)



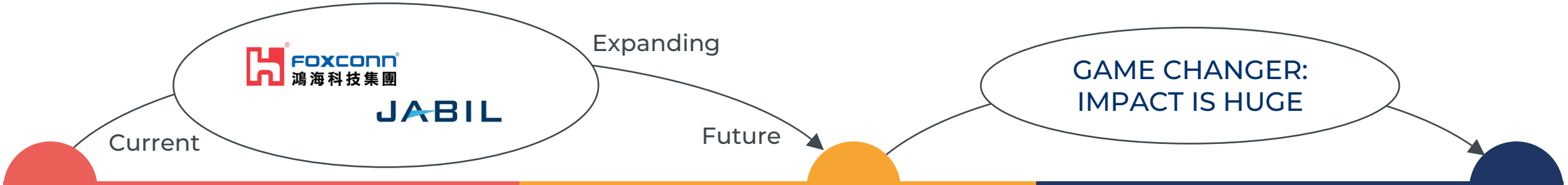
IDM	Foundries	Impact
• IDMs such as Intel moved into the foundry business, IFS (Intel Foundry Services), to leverage their chip manufacturing technological leadership. Key customers recently announced plans to use IFS are Mediatek, ARM, Nvidia, Broadcom, Qualcomm, and Marvell. • Intel's Custom Foundry Business was not successful due to poor responses from customers. Intel struggled with its 10nm production when TSMC had already entered 7nm production. As a fabless customer, the choice was clear: go to TSMC, which has an impeccable track record in the foundry business and is at the forefront of bringing new manufacturing technologies to market. In 2018, Intel announced it would discontinue its Custom Foundry Business, but the US-China trade issues presented an opportunity for Intel to re-enter the foundry business. US tech companies and the government have been trying to reduce the country's dependence on chip factories in Asia for years, underscored by national security concerns, the US-China tariff war, and the Covid-19 pandemic, which disrupted supply chains and logistics around the world. • In 2021, new Intel CEO Pat Gelsinger communicated his vision of "IDM 2.0", a significant evolution of Intel's IDM business model with the establishment of the new Intel Foundry Services (IFS) business unit. Since then, major manufacturing expansion plans have been announced to boost Intel's foundry business. Intel aims to supply its internal business, expand cooperation with third-party foundries, and become a key foundry services provider in the US and Europe. Intel's latest technology roadmap is an aggressive path to catch up and overtake leading foundries such as TSMC and Samsung. • Intel also acquired Altera, Nervana & Mobileye, and Tower amongst others, to bolster their data center offering & to make chips that support new mega trends like AI, autonomous driving / ADAS, 5G, AR/VR, etc.		For Intel, this is a good move, as it will focus on its core business of internally designing & producing chips which has a higher profit margin than foundries. More challenging situation for foundries because specialized IDMs with foundry capability in cutting-edge technology can displace the foundries' top position as manufacturers.

IMPACT OF SEMICONDUCTOR SUPPLY CHAIN CHANGES (4/6)



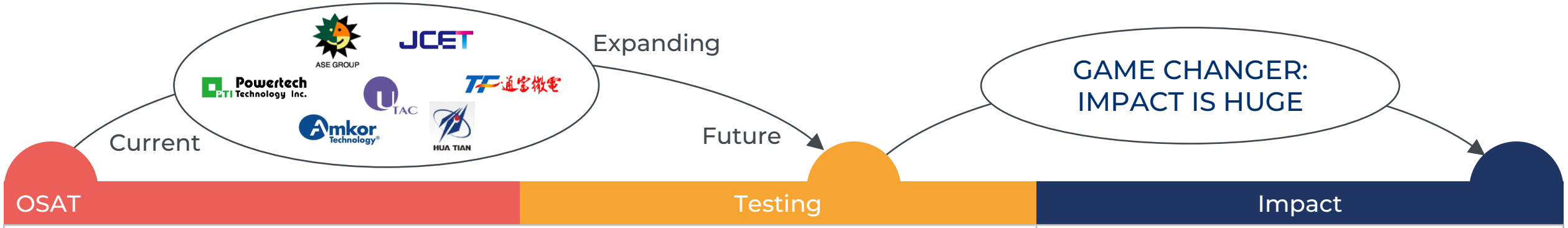
Substrate / PCB	Packaging / Assembly	Impact
• IC substrate and PCB manufacturers, including SEMCO, Unimicron, AT&S, and Shinko, entered the Advanced Packaging arena with panel-level fan-out packages and embedded dies (and passives) in organic substrates, taking advantage of their substrate manufacturing know-how, available panel line and equipment, and thin RDL technology development. • Shinko is already in the packaging business with its MCeP package (licensed to Amkor and others) and is aggressively trying to grow its AP portfolio with 2.1D and 2.3D solutions; SEMCO started FO-PLP packaging with the Galaxy smartwatch (in 2019, Samsung Electronic acquired the PLP production line); AT&S is one of the strong players in embedded-die packaging; Unimicron is aggressively developing fan-out RDL technology and other glass-based Advanced Packaging technologies. Other companies like Ibiden, Simmtech, Access, and Kinsus may also be entering Advanced Packaging. • While embedding passives in PCBs has been underway for years and embedding passives in IC substrates is becoming common, embedding active dies as well as integrated passive devices (IPD) is an emerging market that will grow in the future with a variety of products on order. • Substrate suppliers' decision to enter the packaging business is in response to the accelerated adoption of fan-out packaging, which doesn't require an IC substrate. Its success will depend on customer demand, cost competitiveness, yield, and process maturity.		With Substrate/PCB suppliers' penetration into the assembly business, Substrate/PCB is eating the lunch of OSATs, especially those involved in AP business. No effect

IMPACT OF SEMICONDUCTOR SUPPLY CHAIN CHANGES (5/6)



EMS / ODM	Packaging / Assembly & Foundries	Impact
• EMS companies are developing assembly/packaging capabilities and are expanding into the OSATs' business domain to improve their profit margin. • Foxconn, the #1 EMS company, is entering the foundry business in order to reduce its dependence on Apple, which accounts for half of its annual revenue of NT$4.7 trillion (US$152.65B), as the global smartphone market slows down. It's planning to build a fab in Zhuhai with a total investment of $9B and is supported by China Big Fund and the city government. This is also seen as a strategic geopolitical decision in the wake of worsening US-China ties. Foxconn is to venture into the field of advanced packaging and heterogeneous integration. Besides, Foxconn intends to build a plant in India to reduce the impact of geopolitical tensions. Foxconn acquired ASE's Chinese plants sold to Wise Road Capital. • EMS players such as Foxconn & Jabil are investing in assembly & packaging capabilities to move up the value chain to higher-margin businesses. • Foxconn provides the RF SiP packaging services for Avago's FEM and module assembly services for various OEMs. In July 2021, Foxconn started installing equipment for high-end IC packaging at its chip plant in Qingdao, northeast China. The plant began production in November 2021 and focuses on AP technologies such as fan-out, wafer-level bonding, and 3D stacking, targeting chip solutions for 5G and AI-related device applications. • Jabil acquired Kasalis, a manufacturing system for the active alignment, assembly, and test of compact optoelectronic devices.		Impact is seen on Traditional Packaging OSAT business, but Advanced Packaging remains unaffected

IMPACT OF SEMICONDUCTOR SUPPLY CHAIN CHANGES (6/6)



OSAT	Testing	Impact
• OSATs' expertise in testing is expanding while the traditional pure test players are investing in their assembly and packaging capabilities. • The leading OSATs are aiming to capture the test market segment by increasing their internal capacity or acquiring testing companies. • Test houses like KYEC and Sigurd Microelectronics are adding packaging/assembly capabilities to their service offerings through mergers and acquisitions or by investing in research and development. • KYEC is mainly concentrating on traditional packaging platforms such as BGA, QFN, TSOP, and LGA. • Sigurd acquired Winstek to enhance their wafer-level packaging services. Sigurd also disclosed plans to acquire UTAC Taiwan, another IC assembly and test service company, for NT$4.62 billion ($165 million) in 2021.		Negative impact on pure-play testing business as customers can access turnkey solutions from OSATs. We'll see more investment in testing capability by OSATs. Testing houses offering assembly services will not significantly impact the OSAT business.

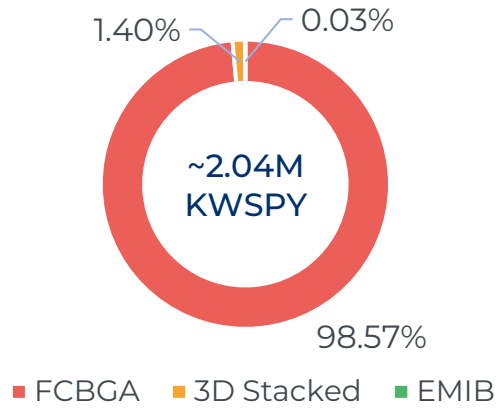
BIG PUSH FROM GIANTS IN AP SEGMENT: INTEL

Intel's IDM 2.0 Advanced Packaging Strategy

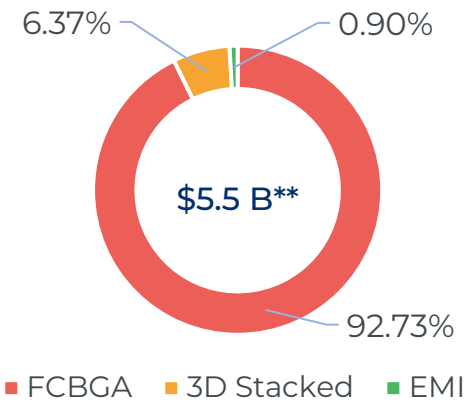
- Intel's recent IDM 2.0 strategy was unveiled in new leadership plans to capitalize on external and internal manufacturing resources with a focus on design wins and increased market share, growing Intel's leadership in the client and data center domains.
- Intel announced a $20B investment in Arizona, creating two additional fabs and possibly looking into expanding in the Munich area soon with a new fab. Intel recently announced that it would discontinue the Lakefield product line by 2022, which was built on the Foveros architecture. However, Intel is adopting Foveros technology for the upcoming Alder Lake product line and beyond.
- Intel announced an investment of $3.5B in hybrid packaging infrastructure in its Rio Rancho, New Mexico facility, where it will start tooling up a new hybrid manufacturing line for advanced die-to-die interconnect with the Foveros (3D stacked) type architecture.
- On top of that, Intel is investing ~$7.1B in expanding its Advanced Packaging capabilities in Penang, Malaysia. The addition of Advanced Packaging capabilities to Intel's operations in Malaysia will strengthen its supporting activities and global service center.
- In 2022, Intel announced a major expansion of its production capacities in Europe with an investment of 80 billion euros over the next decade. The initial 33-billion-euro investment includes plans to build a leading-edge semiconductor fab in Germany, create a new R&D and design hub in France, and invest in R&D, manufacturing, and foundry services in Ireland, Italy, Poland, and Spain.

Intel's estimated revenue from Advanced Packaging is ~$5.5B.

Intel's 2022 wafer production breakdown (estimated)



Intel's 2022 packaging revenue breakdown (estimated)



**Note: Intel revenue is estimated to capture "internal consumption" for packaging services. It is still estimated as if it was in a an out-sourced open market.

BIG PUSH FROM GIANTS IN AP SEGMENT: SAMSUNG

To emerge as a strong competitor and alternative to TSMC

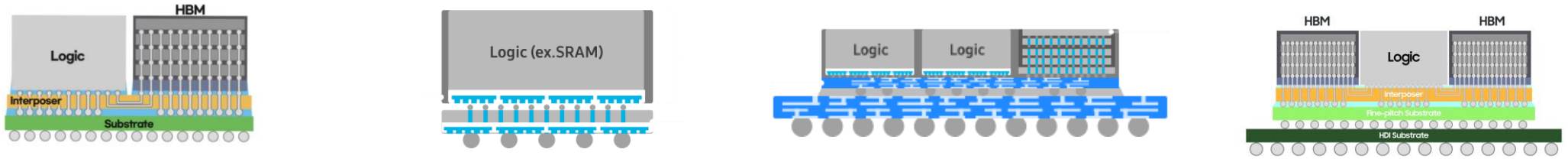
Samsung is aggressively investing in AP technology to boost its foundry business and emerge as a strong alternative to TSMC. Samsung and TSMC are the two foundries remaining engaged in cutting-edge front-end manufacturing, although Intel is trying to catch up by 2024 with an aggressive technology roadmap toward their IFS business. As with its competitors, Samsung Electronics is stepping up its game by strengthening the synergy between semiconductors and packaging.

Samsung Test & System Package division (TSP) at Onyang is developing fan-out and 2.5D/ 3D IC stacked packaging technologies. Meanwhile, to strengthen its efforts to win against the intensifying competition in the semiconductor testing and packaging sector, Samsung has established the Test & Package (TP) Center within the Global Manufacturing & Infrastructure Department of its DX Business Division.

Samsung is a pioneer in the development of 3D TSV stacking technology for HBM memory and one of the few players who have been investing in this technology since the 2000s.

In 2019, Samsung Electronics invested in HD fan-out technology by acquiring the PLP line from SEMCO for ~$650M to compete with TSMC for Apple's APE FE die and packaging business. This is an attempt to expedite the yield and provide more technical breakthroughs for its FE + packaging solution. Currently, Samsung employs its FOPLP solutions for its Galaxy smartwatches and is expected to adopt the same technology for its smartphone APEs in the coming years.

Samsung Electronics AP portfolio includes HD fan-out at both wafer & panel levels, as well as its CUBE packaging technologies.



I-Cube (2.5D Si-Interposer) X-Cube (3DIC Logic Interposer) R-Cube (2.5D RDL Interposer) H-Cube (Hybrid Interposer)

Samsung's CUBE packaging technologies. *Source: Samsung*

Apart from TSMC, Samsung Electronics is the only company with patents related to 3D IC packaging using hybrid bonding. Its hybrid bonding products will probably enter the market between 2024 and 2025.

SUMMARY OF THE TECHNOLOGIES OF KEY PLAYERS

In Production | Developed | In Development

Company	Platform	Generation	Bump Pitch	HVM Intro.	2.5/3D	Platform specificity
intel	EMIB	1st Gen	55µm	2017	2.5D	Si Bridge
		2nd Gen	45µm	2019		
		3rd Gen	36µm	2021		
	Foveros	1st Gen	55µm	2019	3D	Active Interposer & TSV
		2nd Gen	36µm	2023		Active Interposer & TSV
		Omni	25µm	2023		TSV and Cu Column
		Direct	<10µm	2023		Hybrid Bond interconnect
	Co-EMIB			2019	2.5D +3D	EMIB + Foveros
SAMSUNG	I-Cube	I-Cube 2		2018	2.5D	Si Interposer + TSV
		I-Cube 4		2021		
		I-Cube 6		2022	2.5D	
	X-Cube	1st Gen	25µm	2020	3D	Logic Interposer + TSV CoW, WoW
		Future	4µm		3D	D2W
	X/I Cube			2020	2.5D +3D	Integration of I-Cube and X-Cube
	H Cube		35% of conventional pitch	2021	2.5D	RDL Interposer
	R-Cube				2.5D	Low cost 2.5D package Interposer TSV-less

3DFabric	Generation	Bump Pitch	HVM Intro.	2.5/3D	Platform specificity	Company
CoWoS –S	Gen1 to 4		2011 to 2019	2.5D Chip Last	Si interposer	tsmc
	Gen1 5		2021		Si interposer	
CoWoS-R	Co-WoS-R	4µm	2022		Organic interposer	
	Co-WoS-R+	3µm	2023		Organic interposer Hybrid Bond	
CoWoS-L			2023/4		RDL interposer	
InFO	InFO_PoP		2021	2.5D Chip First	HD RDL and TIV	
	InFO_oS	40µm	2019		HD RDL	
	InFO_MS		2019		HBM + Substrate	
	InFo_UHD		2020		Sub micron RDL	
	MUST		2019		Fan-out Multi Stack	
	SoW		2020		Fan-out Si on Wafer	
	AiP		2019		2 RDLs	
	MiM		2019		MiM capacitor between M1 & M2	
	LSI	25µm	2020		With active or passive Si Chip	
SoIC	SOIC4	3µm		3D	Hybrid Bond	
	SOIC5	2µm				

TSMC announced their intention to combine SoIC with CoWoS and InFO to deliver new 3D packaging solutions.

- Intel is active in Advanced Packaging with its EMIB and Foveros technologies.
- TSMC is picking up aggressively with the introduction of InFO and CoWoS technologies with a wide range of customers, including AMD, Apple, Qualcomm, and MediaTek on a number of platforms.
- Samsung is catching up with the introduction of X-Cube, I-Cube, H-Cube, and R-Cube.
- All the players are focusing on mixing and matching chips (chiplets) and new interconnect techniques (TSV and hybrid bond). This accelerates the trend of heterogenous Integration of chiplets.

ANALYSIS OF TSMC VS. INTEL VS. SAMSUNG AP ACTIVITY

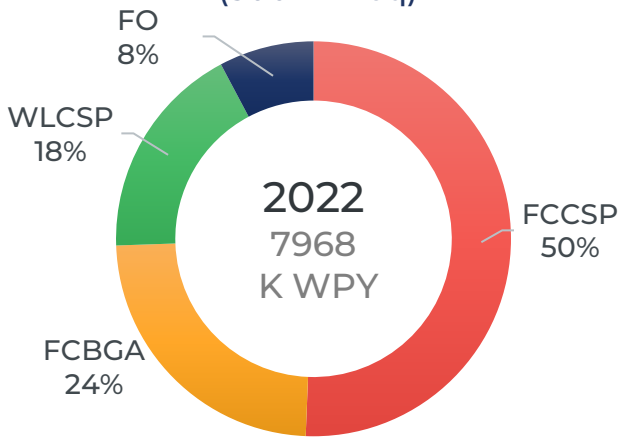
TSMC	Intel	Samsung
• AP technology is key for the system foundry model. • Supports front-end business with turnkey solutions. • Since 2011, when TSMC introduced CoWoS as a Si interposer technology for heterogeneous integration, there have been a series of innovations from InFO (& its multiple versions, InFO-oS, InFO-AiP, etc.) to SoIC to 3D Multi-stack (MUST) system integration technology to 3D MUST-in-MUST (3D-MiM fan-out package) to 3D SoW to low-cost RDL/organic interposer to local silicon interconnect technologies InFO-LSI and CoWoS-L. • AP emerged as a separate business and generated ~$5.3B in revenue in 2022 in back-end & test activities. • SoIC technology development is really pushing the boundary and aims to capture both high-end server, AI, and HPC markets as well as the low-end mobile AP market. • Leading 3D SoC hybrid bonding IP by owning patents describing the hybrid bonding process and 3D die stacking-related patents. • Announced unprecedented ~$3B CapEx investment in 2023 for Advanced Packaging and mask making. • Potential to emerge as #1 OSAT in the future. • Strong collaboration with ASE for packaging outsourcing, assuring enough available capacity to compete with Intel.	• Currently market leader in PC & server business but a serious threat from competitors such as AMD who are using TSMC foundry and clearly ahead in the technology. • In 2021, Intel unveiled its “IDM 2.0” strategy, which includes the establishment of new Intel Foundry Services (IFS) business unit. Intel has an ambitious technology roadmap for the next decade, and AP plays a crucial role. • Heterogeneous integration using AP is the only way to develop and own leading technology to connect chips and chiplets in a package to match the functionality of a monolithic SoC in order to reduce the complexity of manufacturing at cutting-edge nodes. • Investment in AP technology will help Intel to bring the latest node devices to market and maintain a leadership position. • Developed five high-end Advanced Packaging technologies: EMIB, Foveros, Co-EMIB, Foveros Omni, and Direct. • Collaborating with CEA-Leti on advanced chip design for 3D packaging technologies with hybrid bonding. • US tech companies and the government have been trying to reduce the country’s dependence on chip factories in Asia for years, underscored by national security concerns, the US-China tariff war, and the Covid-19 pandemic. Intel plans to become a major foundry provider in the US and Europe and serve the soaring global demand for semiconductor manufacturing. Intel has announced back-end investments in New Mexico, Malaysia, and Italy, a total of almost $3.5B CapEx for AP in 2023.	• >25yrs of packaging experience. Pioneered TSV technology for 3D memory applications. • Aggressively focusing on increasing foundry market share. Currently, TSMC and Samsung are the main leading-edge foundry business players, although Intel is trying to catch up with its IFS business. Great opportunity to gain foundry share. Samsung intends to follow the TSMC system foundry model, and AP is the key. • AP will boost the foundry business and help provide a one-stop turnkey business to meet customer needs. Samsung Electronics is stepping up its game by strengthening the synergy between semiconductors and packaging. • Samsung Electronics invested in HD fan-out technology by acquiring SEMCO’s PLP line in 2019 for ~$650M. • Samsung AP portfolio includes HD fan-out at both wafer & panel levels as well as its CUBE packaging technologies: I-Cube (2.5D Si-Interposer), X-Cube (3DIC Logic Interposer), R-Cube (2.5D RDL Interposer), H-Cube (Hybrid Interposer). • Apart from TSMC, Samsung Electronics is the only company with patents related to 3D IC packaging using hybrid bonding.

ASE : A PURE PLAYER IN FACE OF THE GIANTS

OSAT market leader – What is ASE's investment strategy?

- In 2022, ASE continued to dominate the Advanced Packaging market in revenue. As the leading OSAT, ASE is the strongest player in terms of market share in WLCSP and the second in fan-out, after TSMC.
- ASE announced that in 2022 its CapEx would be either equal to or higher than 2021, at least $2B. This investment, together with the additional resources coming from the disposal of the sites in China, will support ASE's organic growth and be increasingly allocated to Advanced Packaging technologies and less to traditional packaging. ASE's strategy is to ensure enough capacity and rapid response to the strong momentum in automotive, networking, and HPC applications. Also, IDM outsourcing is accelerating, particularly for more advanced products, which is driving ASE's AP business.
- Its investments will also continue the support of ASE's strategic alliance with TSMC, which is outsourcing strongly to ASE. The two companies are not competing but instead supporting each other, with TSMC assuring enough available capacity to avoid competition from Intel, while ASE can remain the leading OSAT.

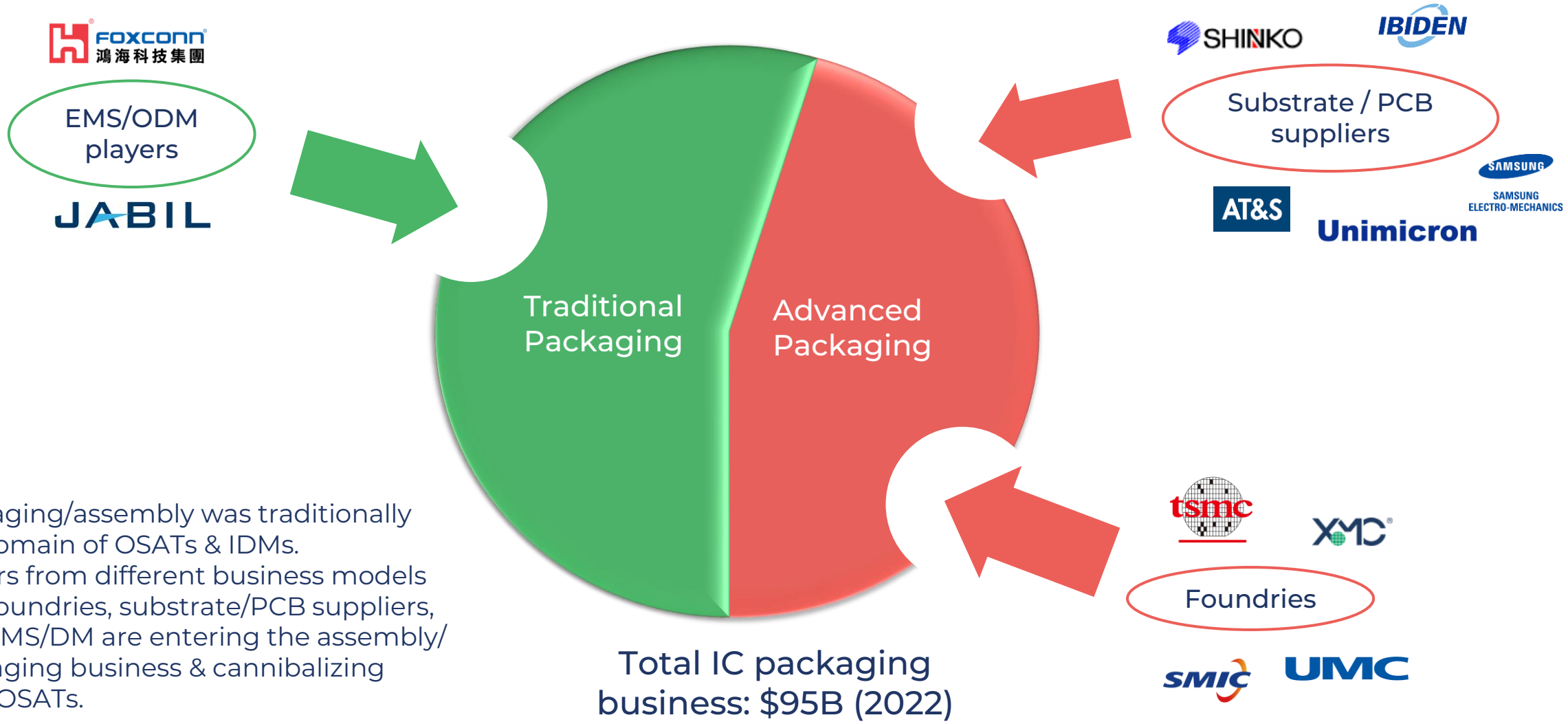
2022 ASE Advanced Packaging wafer Manufacturing breakdown (300mm eq)



VIPack™

- ASE recently announced its new platform named VI Pack, designed to address 3D heterogeneous and chiplet integration trends driven by AI, machine learning, 5G Communications, HPC, IoT, and automotive applications.
- VI Pack comprises six technology pillars leveraging advanced RDL processes, embedded integration, and 2.5D and 3D technologies. The platform was developed by gathering the already existing fan-out technologies in ASE's portfolio and adding new 2.5D/3D solutions, giving the possibility of designing customized products by mixing and matching the different solutions available.

OSATS PACKAGING BUSINESS CANNIBALIZATION TREND

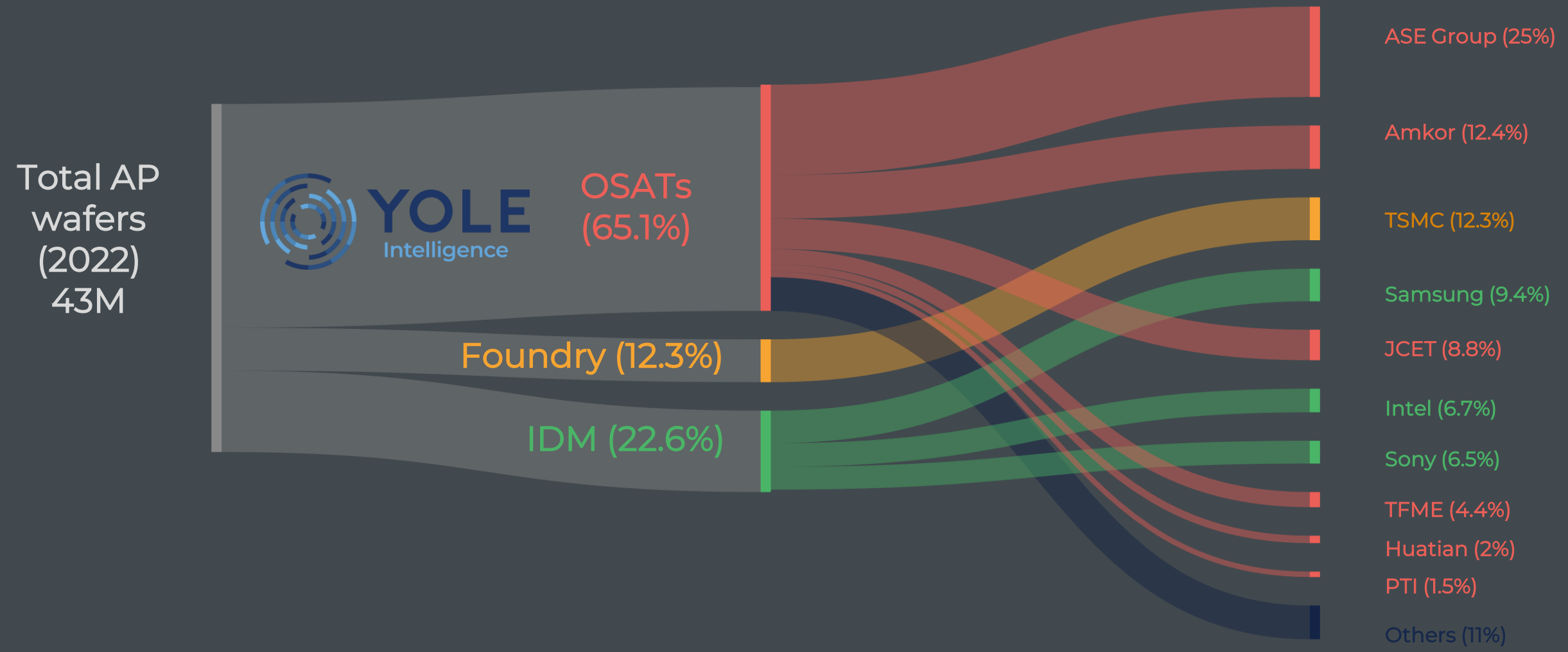


Packaging/assembly was traditionally the domain of OSATs & IDMs.
Players from different business models like Foundries, substrate/PCB suppliers, and EMS/DM are entering the assembly/ packaging business & cannibalizing from OSATs.

Total IC packaging business: $95B (2022)

ADVANCED PACKAGING 2022 WAFERS MANUFACTURERS' MARKET SHARES

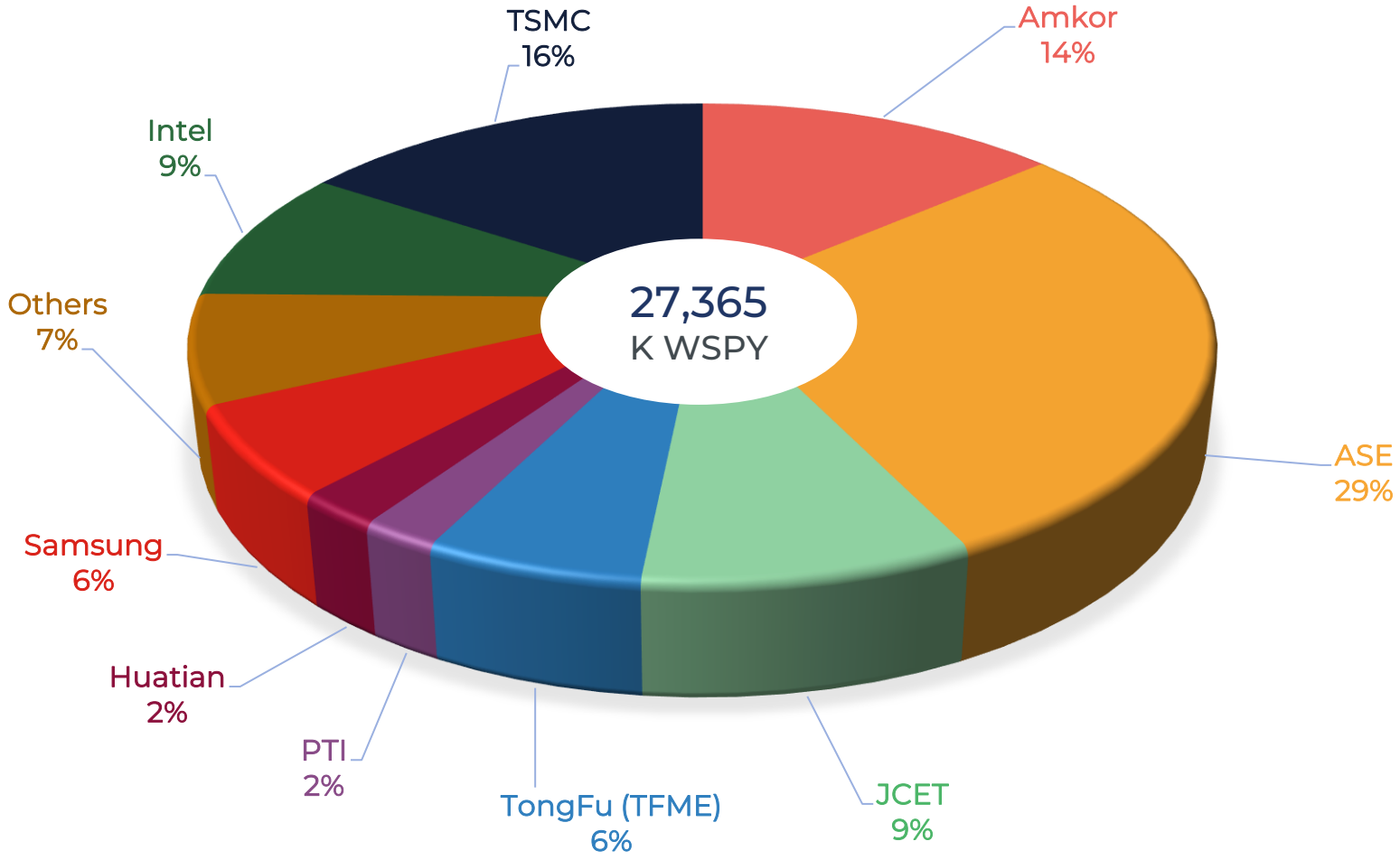
Breakdown by business model



FLIP-CHIP PRODUCTION BY MANUFACTURER

In terms of flip-chip wafer bumping capacity, ASE Group is #1, followed by TSMC and Amkor

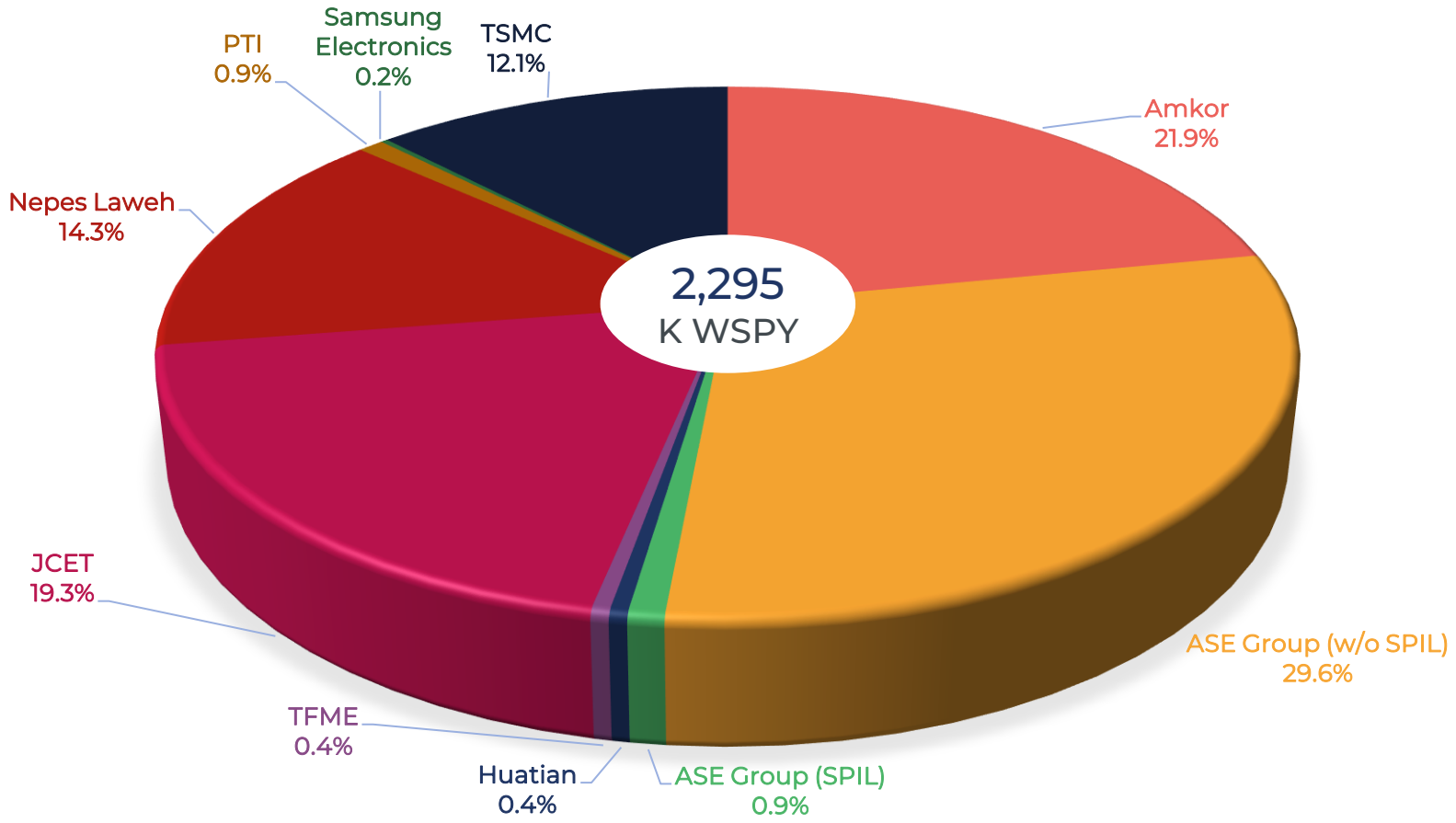
2022 FLIP-CHIP WAFER PRODUCTION BY PLAYER (K WSPY, 300MMEQ)



FAN-OUT PRODUCTION SPLIT BY MANUFACTURER

TSMC leads the market in fan-out wafer production due to the adoption of the InFO platform for mobile APUs, networking, & high-performance applications

2022 FAN-OUT WAFER PRODUCTION BY PLAYER (K WSPY, 300MMEQ)



- Samsung Electronics and PTI are mainly involved in fan-out PLP business.
- Nepes purchased Deca panel fan-out manufacturing facility in Philippines and started mass production end of 2021.

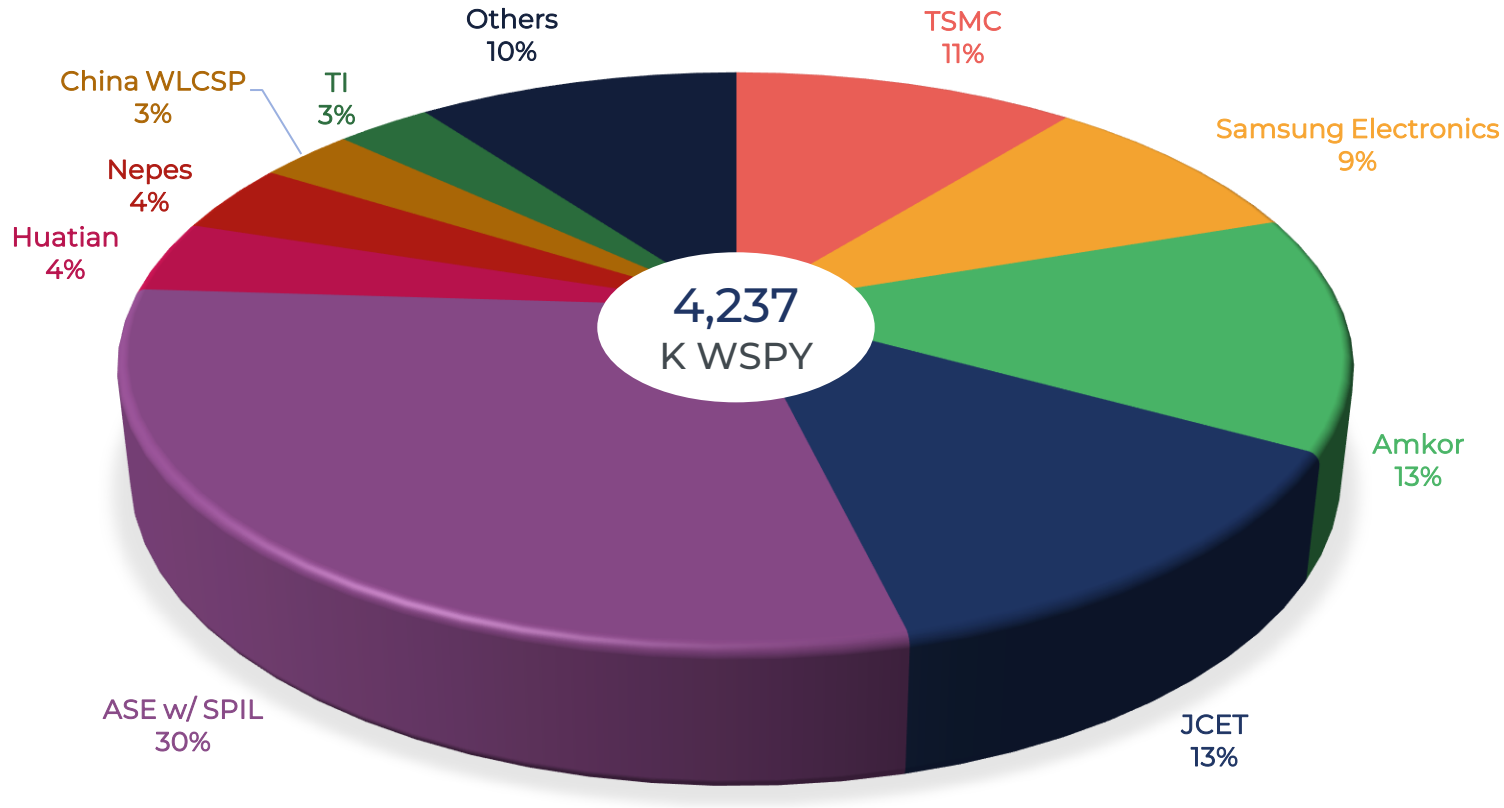
NOTE:

- Fan-out WLP values are entered as total production, not capacity

FAN-IN WAFER PRODUCTION SPLIT BY MANUFACTURER

ASE is the market leader in fan-in WLP production by wafer starts, followed by Amkor and JCET.

2022 FAN-IN WAFER PRODUCTION BY PLAYER (K WSPY, 300MMEQ)

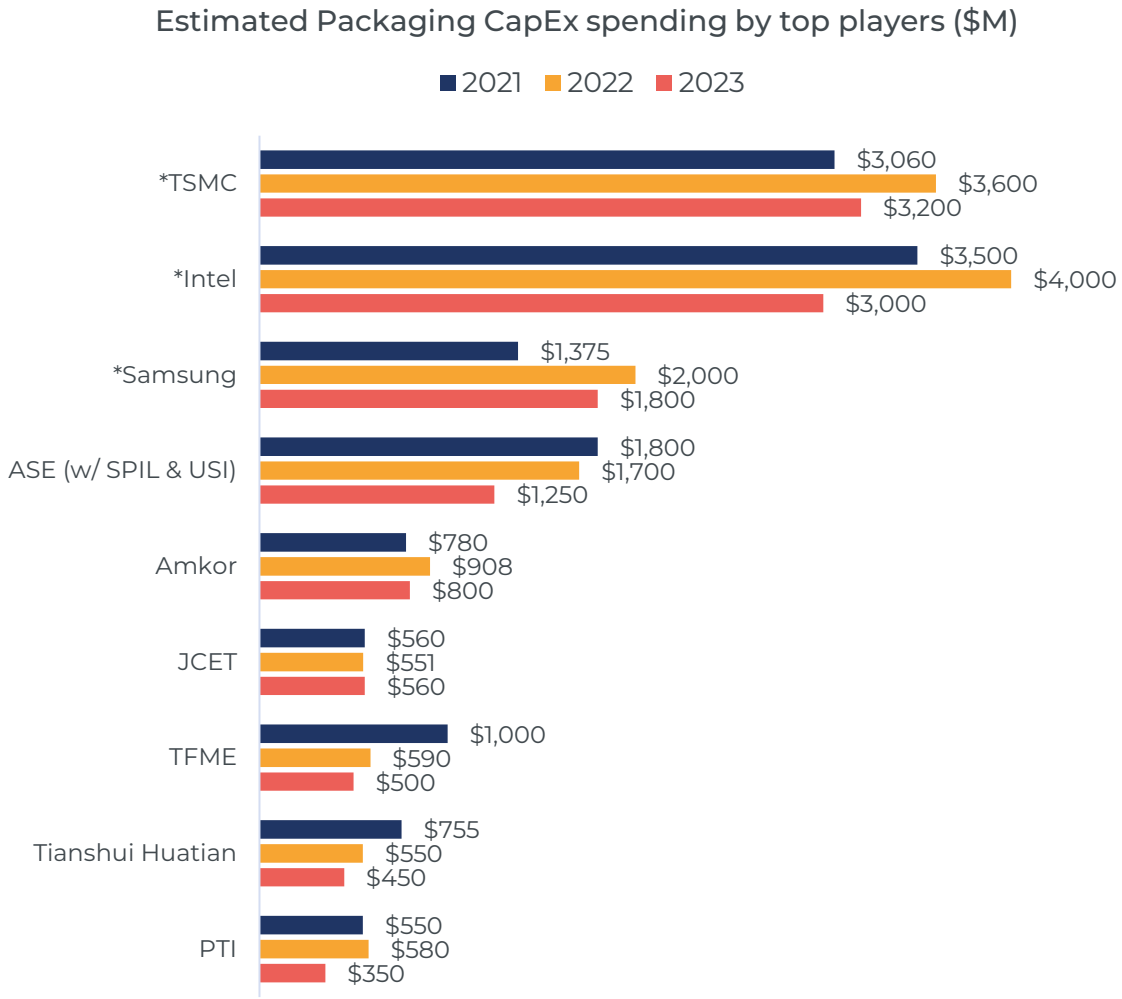


- ASE, along with SPIL, is responsible for one third (~33%) of the fan-in WLCSP production.
- Chinese companies' share of WLCSP production is ~19%, almost one-fifth of the total value.

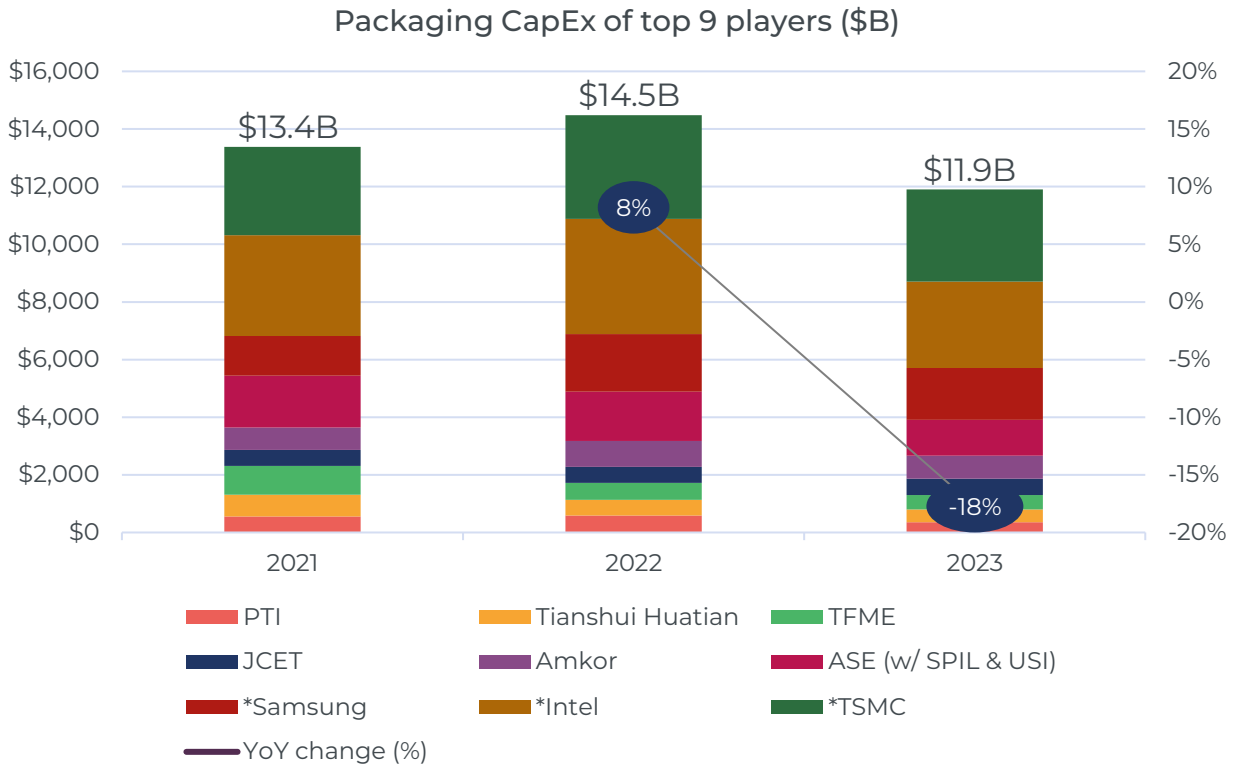
NOTE:

- Fan-in WLP values are entered as total production, not capacity

2021-2023 CAPEX HIGHLIGHTS FOR PACKAGING PLAYERS



*Intel, TSMC, and Samsung's packaging CapEx were estimated based on earnings statements and announcements of investments, since packaging is not their primary business focus. All CapEx data is estimated based on information gathered during **Q2-2023**



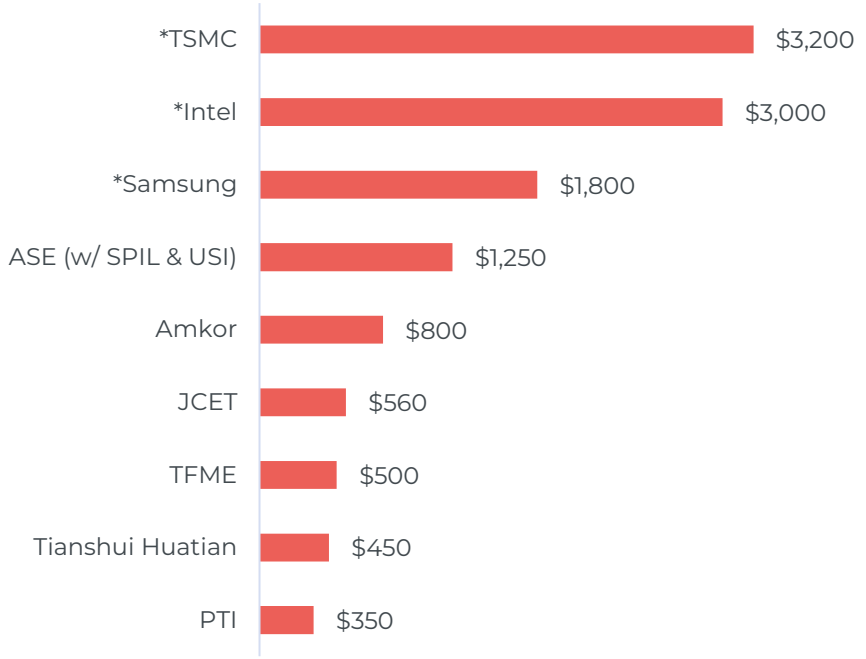
In 2023 the packaging CapEx of the top nine players is expected to reach $11.9B, which is 18% lower than the previous year.

Packaging companies are being cautious about their investments and capacity increases and are decreasing their CapEx for 2023 with decreases from 10% to 40% compared to the previous year. The current macroeconomic situation is causing lower consumer confidence and therefore slowdown in demand, leading to high inventory levels and lower capacity utilization. Hence, packaging suppliers are adjusting the timing of their capacity expansion in response to demand fluctuation.

2023 CAPEX ANALYSIS FOR PACKAGING PLAYERS

- 2022 advanced packaging CapEx (~$14.5B) was about 33% of the total advanced packaging revenue, and this ratio is expected to decrease to 25% in 2023 as top players are reducing the investment in capacity expansion as the chip demand weakens. TSMC and Intel remain the top spenders as they follow a strategy to serve their front-end customers with AP solutions.
- TSMC announced that its 2023 CapEx will decrease to $32 - $36 billion, and about 10% of the total CapEx will be spent on advanced packaging and mask making. We estimate that about $3.2B will be spent on advanced packaging, making TSMC the biggest spender for the year.
- Intel aims to achieve $3 billion in cost reductions in 2023, with a potential yearly savings of up to $10 billion by the end of 2025. In total, these measures could result in a cumulative savings of $23 billion over the course of three years. Regarding packaging investments, Intel announced to be spending $3.5B in its New Mexico plant and about $7.1B in Malaysia during the next years. Intel has also started negotiations with Italy for an advanced packaging plant with an investment of about $5B, but plans are apparently delayed. Based on its announcements, we estimate that in 2023 Intel will spend about $3B (25% less than in 2022), considering that the company is adjusting the timing of capacity expansion in response to near-term changes in demand.
- ASE Group announced that its 2023 CapEx will be a few hundred million lower than the previous year, due to demand slowing down, despite the record-high net profits in 2022. The investments will include new facilities and manufacturing equipment, with more than 50% on packaging operations, which confirms the trends as the same as the previous year. 2022 CapEx totaled $1.7B, of which $918M was used in packaging operations, $574M in testing operations, $154M in EMS operations, and $51M in interconnect materials operations and others. We estimate that in 2023 ASE will spend about $1.25B.
- After its significant investments in 2022 in WLP, flip-chip, advanced SiP, test, and facility expansion, Amkor announced a 12% decrease in CapEx in 2023 to around $800M. Amkor is continuing its factory construction in Vietnam and expects production to begin by the end of 2023. Amkor is currently assessing its investment policies intending to construct a manufacturing facility in the US, although its challenge is to make it financially feasible. In comparison to ASE, Amkor finds itself in a less advantageous strategic position to form a similar alliance with a company like TSMC. Amkor's ideal partners would be Intel in the US or Samsung in Korea, but both companies have chosen to invest independently and have not yet established any strategic alliances with OSATs.

Estimated 2023 Packaging CapEx spending by top players ($M)



*Intel, TSMC and Samsung Advanced Packaging CapEx were estimated based on earnings calls statements and recent announcements of investments, since packaging is not their main business focus.
All CapEx data is estimated based on information gathered during Q2 2023.

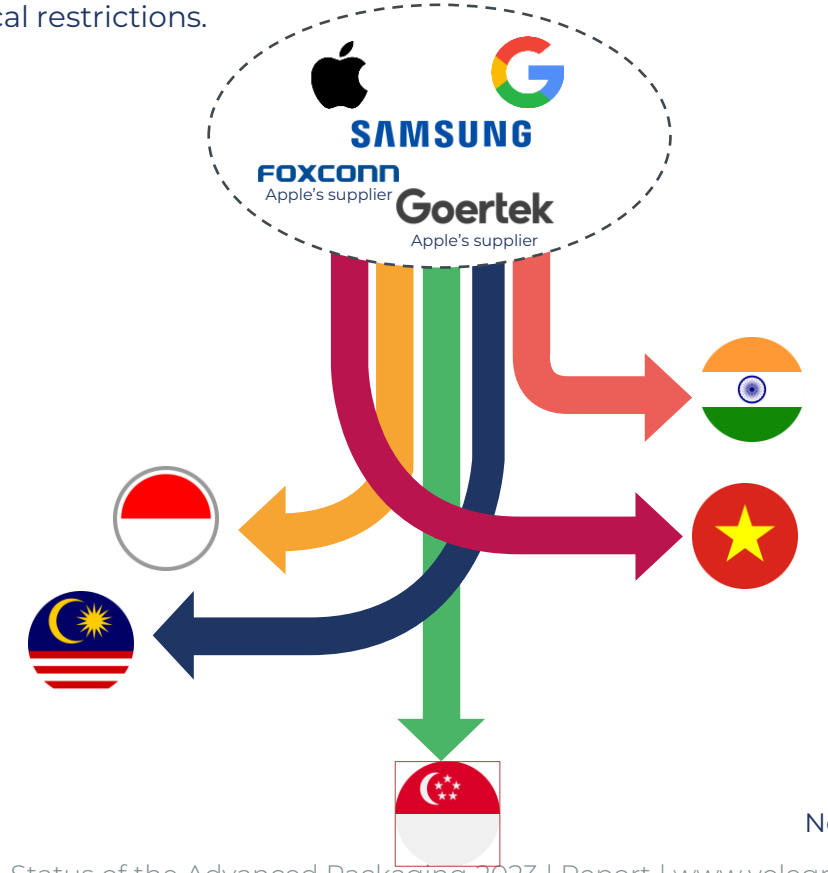
China’s supply chain

RELOCATION OF MANUFACTURING FROM CHINA

A big challenge of supply chain diversification and for China

- The U.S. semiconductor export restrictions on China have prompted companies to explore alternative production bases in Southeast Asia, which is emerging as an attractive location because of its perceived neutrality and lower costs. However, China still holds the lead over regional economies in terms of its competitiveness in chips' production.
- China is facing increasingly urgent challenges as it seeks to ramp up its domestic capacity for high-end chips with the current export controls.
- Leaving China can be complicated due to the interdependence of global supply chains and China's low-cost production leadership.

- Withdrawal from China may entail settling outstanding taxes, debts, and closure taxes, which may come as a surprise to Western companies and may require obtaining permits to leave.
- The decision of relocation should be based on the microeconomics of each company , not just labor costs.
- Some Chinese companies are planning to move out of China to avoid the geopolitical restrictions.



Non-exhaustive list

CHINA'S LOCAL SUPPLY CHAIN

There are Gaps in Many Areas

EDA

HyPerform, ICScape, Empyrean, 芯华章 X-EPIC, XPEEDIC ACCELERATE YOUR IC DESIGN

Fabless

Allwinner Technology, HISILICON, NARI, 紫光展锐 UNISOC, GOODiX, IMICRO 中星微电子, WILLSEMI

IC substrate suppliers

SIMMTECH, SCC 深南电路, AKM MEADVILLE, ACCESS

Foundry/IDM

SMIC, XMC, HHGrace 華虹宏力, HLMC 上海华力, CR MICRO 華潤微电子, asmc 上海先进半导体制造有限公司 Advanced Semiconductor Manufacturing Corporation Limited

OSAT

JCET, JSI, HUA TIAN, TF 通富微電, 沛顿科技 Payton Technology, CR MICRO 華潤微电子, LCSP INNOVATIVE TECHNOLOGIES, CHIPMORE, hitech semiconductor, 宏茂微 UNIMOS, SJSEMI 盛合晶微半导体（江阴）有限公司, ASMeIT, 云天半导体 Sky Semiconductor, ECHINT, 广东省半导体智能装备与系统集成创新中心 广东佛智芯微电子技术研究有限公司, 江苏长电科技股份有限公司, 奕斯伟 YIBU SEMI

EMS

USI, KAIFA, TORTAI TECHNOLOGIES CO.,LTD.

OEM

Lenovo, mi, HUAWEI, ZTE中兴, oppo, MEIZU, BYD, NIO, Baidu 百度

Back-End Equipment

拓荆科技 PIOTECH CO.,LTD, NMC 北方微电子 NORTH MICROELECTRONICS, KINGSEMI 芯源, AMEC, HWATSING 华海清科, Sevenstar, CEC China Electronics Corporation 中國電子股份有限公司, SMEE 上海微电子装备有限公司 SHANGHAI MICRO ELECTRONICS EQUIPMENT CO., LTD., ACM RESEARCH, INC.

Materials

SCC 上荣, 兴森科技 FASTPRINT, 丹邦科技 DANBOND TECHNOLOGY, 晨日科技 Earlysun, 无锡创达电子有限公司 Wuxi Chuangda Electronic Co.,Ltd., SCC 深南电路, AKM MEADVILLE

- China is working on a war footing to develop the local IC supply chain but still has many weak areas: EDA, foundries, equipment, and materials.
- Fabless & OSATs are almost at global levels, mainly focusing on mid-end Advanced Packaging platforms and targeting high-end technologies for the future.

Non-exhaustive list of players

TOP 10 CHINESE OSATS' LOCATIONS

JCET Group
HQ: Jiangsu, China
Other Site:
Jiangyin – Binjiang, China
Jiangyin, Jiangsu, China
Chuzhou, Anhui, China
Suqian, Jiangsu, China
Incheon, Korea
Yishun, Singapore
Tokyo, Japan – (Planning)

Tongfu Microelectronic
HQ: Jiangsu, China
Other Site:
Hefei, China
Suzhou, China
Penang, Malaysia

Chippacking
HQ: Dongguan, China
Other Site:
Shenzhen, China

OSATs concentrated in the Yangtze River Delta represent more than 70% of China OSATs' revenue.

CHINA'S LOCAL SUPPLY CHAIN

There are Gaps in Many Areas

China is self-sufficient in lower-end chips/packages but weak in leading-edge

Considering the expertise lag in Chinese companies in the semiconductor industry, especially in EDA, foundry, memory, equipment, and materials, it is not surprising to note that China's OEMs were also dependent on imports for central processing units and CPU-related chips for computers and servers. Domestic (x)PUs are not as efficient as those produced by Intel, AMD, Nvidia, and ARM because a lot of Chinese production is still at the mid to lower tier. While China has made progress to almost full self-sufficiency in lower-end chips/packages, it continues to be weak in leading-edge design tool services, semiconductor equipment & materials, and hence lower-end multi-core processors and memory devices.

However, China's chip start-ups are venturing into high-end chips to challenge US giants

Chinese venture capital is pouring into developing next-generation microprocessors as Chinese start-ups race to challenge the dominance of US chipmaking giant Nvidia. Lots of investments are happening in new general-purpose graphics processing units (GPGPUs), designed to harness data processing power for artificial intelligence computing. An AI chip maker, Iluvatar CoreX, unveiled China's first GPGPU built on an advanced 7nm node in March 2020. Other players in this area that received significant funding recently are Biren Technology, MetaX Integrated Circuit, and Moore Threads Technology. However, developing the chips to replace Nvidia is not easy as it will take billions of dollars to build up a software ecosystem comparable to Nvidia's. Also, these start-ups need time to meet the standards of big local customers such as Alibaba, Tencent, Baidu, and Huawei. Some of these customers have started in-house chip development.

China is still highly dependent on US technology for high-end semiconductors

With no Chinese companies present among the top global semiconductor companies and with most Chinese activity focused on lower value-added functions and less sophisticated chips, the current tensions and their resulting sanctions have highlighted the continued dependence of Chinese companies on critical foreign suppliers in areas like design software and chip manufacturing. For example, in the case of HiSilicon and SMIC, such critical dependencies have created considerable uncertainty about future developments.

US Fabless losing market share to China/Taiwan Fabless for the Chinese market

Also, partnerships between US and Chinese companies are either affected by uncertainty or have ended. With major Chinese companies such as Lenovo, Oppo, Vivo, and Xiaomi among its key customers, Qualcomm has been working with these Chinese smartphone companies in China's National Development and Reform Commission's (NDRC) 5G project. With the increased tension with the US, however, companies like Qualcomm seeking to gain greater access to China's market will find themselves squeezed between the geopolitical interests of the US and China's own ambitions to achieve greater autonomy in the semiconductor sector. Chinese OEMs like Oppo, Vivo, and Xiaomi will start to source from Qualcomm's rival, Taiwan's MediaTek.

SUMMARY

The supply chain is changing at various levels to adjust to the changing business environment. In order to expand the business and explore new areas, players in semiconductor supply chains are moving to different business models. However, while some have successfully made the change and have had a huge impact across the IC manufacturing chain, others have failed to take off. Different players in the IC supply chain have different motivations to move or expand into new models. The semiconductor supply chain will continue to evolve, and we will see an increased expansion of the business models owing to these different motivations.

Advanced Packaging is moving from a package substrate platform to Silicon. This has allowed giants like TSMC, Intel & Samsung to enter and seriously invest in the AP segment, and these players have emerged as the key innovators in the field. Because of the high resource requirements, innovation in the AP space will continue to be led by these giants instead of OSATs.

- With $5.3B in packaging revenue in 2022, TSMC is already ranked #5 among OSATs. TSMC's CapEx for 2023 is estimated to be $32B to $36B, with about 10% of the CapEx to be spent on the Advanced Packaging and mask-making businesses.
- Samsung is aggressively investing in AP technology to boost its foundry business and emerge as a viable alternative to TSMC. Samsung and TSMC are the two foundries remaining engaged in cutting-edge front-end manufacturing, although Intel is trying to catch up by 2024 with an aggressive technology roadmap for their IFS business.
- In 2021, Intel CEO Pat Gelsinger communicated his vision of "IDM 2.0", a significant evolution of Intel's IDM business model that positions packaging as a crucial component. Intel's FY 2022 estimated revenue from Advanced Packaging is ~$5.5B. Intel will invest around $3.5B in Advanced Packaging in 2023 with several expansion plans in Rio Rancho, New Mexico, and Malaysia; Intel is also targeting Italy as a location for a packaging site.

IC substrate and PCB manufacturers such as SEMCO, Unimicron, AT&S, and Shinko are entering the Advanced Packaging arena with panel-level fan-out packages and embedded die (and passives) in organic substrates in response to the accelerated adoption of fan-out packaging, which does not require IC substrate. This trend will continue.

OSATs are expanding their testing expertise, while traditional pure test players are investing in assembly /packaging capabilities. Top OSATs are investing in IC testing capacity to capture the test market. On the other hand, pure test houses, such as KYEC and Sigurd Microelectronics, are adding packaging/assembly capabilities in their service offering through M&As, or investing in R&D.

Overall, there is a paradigm shift in the packaging/assembly business – traditionally the domain of OSATs & IDMs. Players from different business models, viz. Foundries, Substrate/PCB suppliers, and EMS/DMs are entering assembly /packaging & cannibalizing the OSAT business.

Advanced Packaging Equipment & Material Suppliers

EQUIPMENT & MATERIAL SUPPLIERS FOR FLIP-CHIP MANUFACTURING*

Back grinding and CMP

MATERIALS: slurry
- FujiFIlm
- Fujimi
- Dupont
- CMC Materials
- Showa Denko

EQUIPMENT
- DISCO
- Accretech
- Okamoto

Encapsulant

MATERIALS: Epoxy
- Henkel
- Nagase
- Sumimoto
- Hitachi
- Shin- Etsu

Pick & Place

EQUIPMENT
- Besi
- Hanmi
- Hanwha
- SEMES
- Toray
- Shibaura
- ASM PT
- TDK
- Kulicke&Soffa

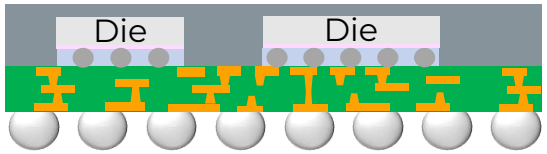
Dielectric: underfill, passivation and photoresists

MATERIALS: Dielectrics
- Merck
- Fujifilm
- JSR
- Asahi Kasei
- Shin-Etsu
- Sumitomo
- Dupont
- AGC
- Toray
- HD Microsystems
- Nippon Kayaku
- TOK

MATERIALS: Underfill
- Henkel
- NAGASE
- SUMIMOTO
- Toray
- Hitachi
- NAMICS

Dicing

EQUIPMENT: mechanical, laser
- DISCO
- Accretech
- ASM PT



Lithography

EQUIPMENT:
- Veeco
- SUSS MicroTec
- ORC
- Nikon
- Canon
- SMEE
- Onto Innovation
- EVG

Test & Inspection

EQUIPMENT:
- Onto Innovation
- Confovis
- Camtek
- CyberOptics
- FormFactor
- Unity SC
- KLA

Metallization: RDL

EQUIPMENT: PVD/PECVD
- KLA / SPTS
- Evatec
- Tango Systems
- ULVAC
- Canon
- AMAT
- NEXX/TEL
- Veeco
- Lam Research
- Shibaura

EQUIPMENT: Plating
- Atotech
- SEMSYSCO
- TEL
- Ebara
- AMAT

*Non-exhaustive list

Non-exhaustive list

EQUIPMENT & MATERIAL SUPPLIERS FOR FAN-IN MANUFACTURING*

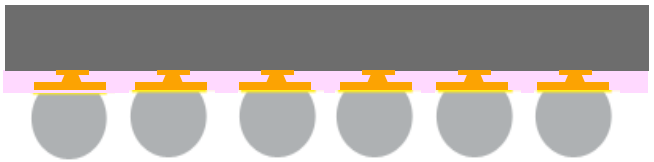
Back grinding and CMP

MATERIALS: slurry
- FujiFIlm
- Fujimi
- Dupont
- CMC Materials
- Showa Denko

EQUIPMENT
- DISCO
- Accretech
- Okamoto

Dicing

EQUIPMENT: mechanical, laser
- DISCO
- Accretech
- ASM PT



Pick & Place

EQUIPMENT
- Besi
- Hanmi
- Hanwha
- SEMES
- Toray
- Shibaura
- ASM PT
- TDK
- Kulicke&Soffa

Dielectric: underfill, passivation and photoresists

MATERIALS: Dielectrics
- Merck
- Fujifilm
- JSR
- Asahi Kasei
- Shin-Etsu
- Sumitomo
- Dupont
- AGC
- Toray
- HD Microsystems
- Nippon Kayaku
- TOK

MATERIALS: Underfill
- Henkel
- NAGASE
- SUMIMOTO
- Toray
- Hitachi
- NAMICS

Lithography

EQUIPMENT:
- Veeco
- USHIO
- SUSS MicroTec
- Nikon
- Canon
- SMEE
- Onto Innovation
- EVG

Test & Inspection

EQUIPMENT:
- Onto Innovation
- Confovis
- Camtek
- CyberOptics
- FormFactor
- Unity SC
- KLA

Metallization: RDL

EQUIPMENT: PVD/PECVD
- KLA / SPTS
- Evatec
- Tango Systems
- ULVAC
- Canon
- AMAT
- NEXX/TEL
- Veeco
- Lam Research
- Shibaura

EQUIPMENT: Plating
- Atotech
- SEMSYSCO
- TEL
- Ebara
- AMAT

Non-exhaustive list

*Non-exhaustive list

EQUIPMENT & MATERIAL SUPPLIERS FOR FAN-OUT MOLD MANUFACTURING*

Mold Compound Encapsulant

MATERIALS: Epoxy Mold Compound
- Nagase
- Henkel
- Sumitomo
- Nitto-Denko
- Hitachi
- Panasonic
- Shin-Etsu

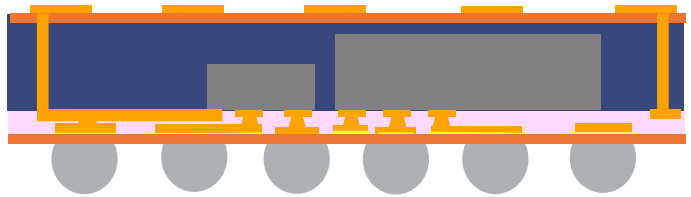
EQUIPMENT: Molding Tool
- ASM
- Towa
- Yamada
- Hanmi
- Besi

Temporary bonding/debonding solution

MATERIALS: Laminated adhesive tapes
- Nitto Denko
- JSR
- Brewer Science
- 3M
- Shin-Etsu
- Wacker
- TOK
- HD Microsystems
- Nissan Chemical

MATERIALS: Glass hard carrier
- Corning
- Schott
- AGC
- NGK
- NEG

EQUIPMENT:
- EVG
- ERS electronic
- SUSS MicroTec
- Tazmo
- TEL
- EO Technics
- Kingyoup Optronic



Dielectric: passivation and photo-resists

MATERIALS: Dielectrics
- Merck
- Fujifilm
- JSR
- Asahi Kasei
- Shin-Etsu
- Sumitomo
- Dupont
- AGC
- Toray
- HD Microsystems
- Nippon Kayaku
- TOK

Lithography

EQUIPMENT:
- Veeco
- SUSS MicroTec
- ORC
- Nikon
- Canon
- SMEE
- Onto Innovation
- EVG

Test & Inspection

EQUIPMENT:
- Onto Innovation
- Camtek
- Unity SC
- Nanometrics
- Xradia
- KLA

*Non-exhaustive list

Pick & Place

EQUIPMENT:
- Besi
- Amicra
- Capcon
- Hanmi
- Toray
- Shibaura
- ASM PT
- Shinkawa
- Kulicke&Soffa

Metallization: RDL, Via

EQUIPMENT: PVD/PECVD
- KLA / SPTS
- Evatec
- Tango Systems
- ULVAC
- Canon
- AMAT
- NEXX/TEL
- Veeco
- Lam Research
- Shibaura

EQUIPMENT: Plating
- Atotech
- SEMSYSCO
- Novellus/TEL
- Ebara
- AMAT

Non-exhaustive list

EQUIPMENT & MATERIAL SUPPLIERS FOR 2.5D/3D MANUFACTURING*

DRIE

MATERIALS: gasses
- AirLiquide
- MERCK
- ADEKA
- STREM
- LINDE

EQUIPMENT: Etcher
- LAM Research
- AMEC
- KLA / SPTS
- AMAT
- Naura

Back grinding and CMP

MATERIALS: slurry
- FujiFIlm
- Fujimi
- Dupont
- CMC Materials
- Showa Denko

EQUIPMENT
- AMAT
- Ebara
- DISCO
- Accretech
- Okamoto

Dicing

EQUIPMENT: mechanical, plasma, laser
- DISCO
- Accretech
- Plasma-Therm
- ASM PT

Lithography

EQUIPMENT for TSV
- Canon
- SMEE
- SUSS MicroTec

Test & Inspection

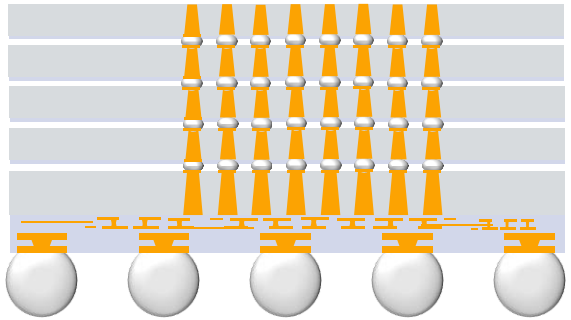
EQUIPMENT:
- Onto Innovation
- Unity SC
- KLA
- AMAT
- TEL
- Camtek

Temporary bonding/debonding solution: Thinning

MATERIALS: adhesive tapes
- Nitto Denko
- Brewer Science
- Shin-Etsu
- HD Microsystems
- Nissan Chemical

MATERIALS: Glass or Silicon
- Corning
- Schott
- AGC
- Global Wafers
- Siltronics
- Sumko

EQUIPMENT:
- EVG
- SUSS MicroTec
- TEL
- TOK



Pick & Place

EQUIPMENT:
- Besi
- Hanmi
- Toray
- Shibaura
- SEMES
- ASM PT
- Shinkawa
- Kulicke&Soffa

Metallization

EQUIPMENT: PVD/PECVD
- KLA / SPTS
- Canon
- AMAT
- TEL
- Lam Research

EQUIPMENT: Plating
- Atotech
- TEL
- Ebara
- AMAT
- Lam Research

Dielectric: passivation and photo-resists

Equipment : Deposition
- SPTS/Orbotech
- AMAT
- LAM Research
- Canon

MATERIALS: Dielectrics
- Merck
- JSR
- Sumitomo
- Dupont
- HD Microsystems
- Nippon Kayaku
- TOK

*Non-exhaustive list

Non-exhaustive list

EQUIPMENT & MATERIAL SUPPLIERS FOR EMBEDDED BRIDGE MANUFACTURING*

Note: there are two components: SI bridge process flow is like 2.5D which can be then embedded in epoxy or IC substrate

Pick & Place

EQUIPMENT
- Besi
- Amicra
- Capcon
- Hanmi
- Toray
- Shibaura
- ASM PT
- Shinkawa
- Kulicke&Soffa

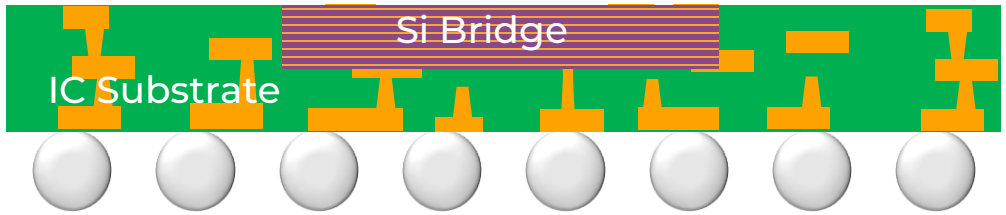
Laser Drill

EQUIPMENT
- KLA/ Orbotech
- EO Technics
- NIDEC
- MICROMAC
- DISCO
- HANMI

Metallization

EQUIPMENT: PVD/PECVD
- KLA / SPTS
- Canon
- AMAT
- TEL
- Lam Research

EQUIPMENT: Plating
- Atotech



Test & Inspection

EQUIPMENT:
- Onto Innovation
- Camtek
- Unity SC
- Nanometrics
- Xradia
- KLA

Lithography

EQUIPMENT:
- Onto Innovation
- ORC
- SCREEN
- Adtec Engineering
- USHIO
- KLA/Orbotech

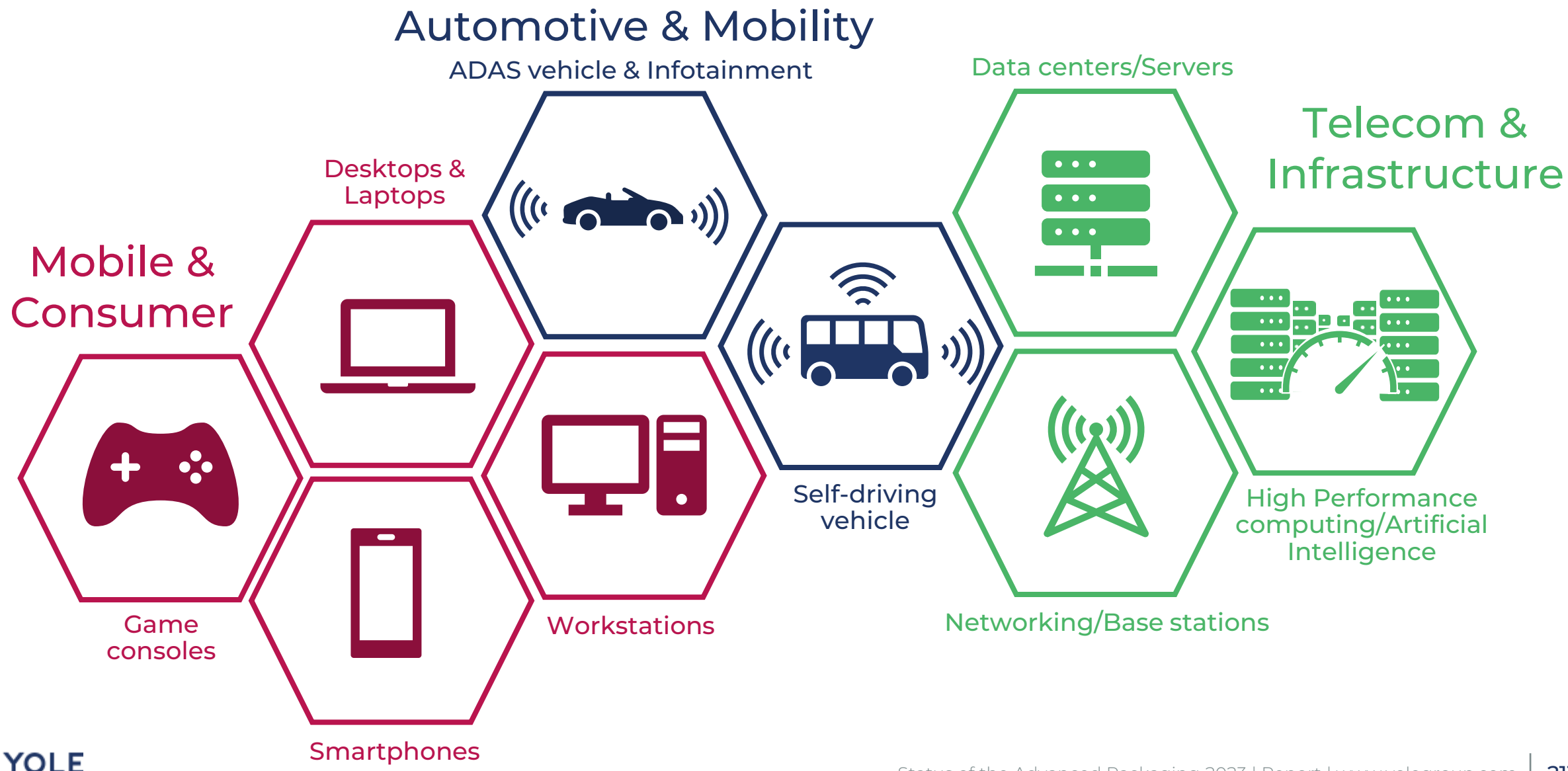
IC Substrate Materials

Core	Prepreg	Buildup	Copper Film	Photo Resist	Solder Resist	Glass Cloth
• Hitachi	• Hitachi	• Ajinomoto	• Nippon Denkai	• Ashai Kasei	• Hitachi	• Ashai Kasei
• Panasonic	• Panasonic	• Duksan	• Mitsui	• Hitachi		• Nittobo
• MGC	• MGC	• Doosan	• Olin Brass	• JSR Micro		• Unitika
• Doosan	• Doosan	• Hitachi		• Fujifilm		

*Non-exhaustive list

Substrate Shortage Issues

FC BGA SUBSTRATE MARKET DRIVERS: KEY APPLICATIONS

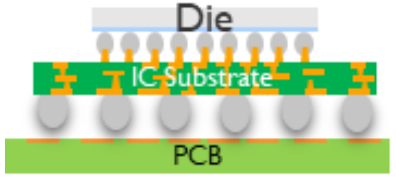


FC BGA SUBSTRATE APPLICATIONS BY PACKAGING PLATFORM

Ajinomoto Build-up Film (ABF)-based FC BGA build-up substrate

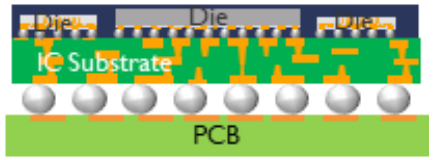
Flip-Chip BGA

Traditional FC BGA package



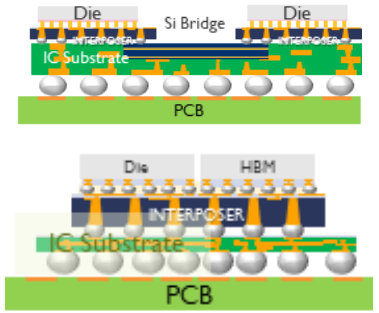
Fan-Out on Substrate

Ultra-High-Density Fan-Out (UHD FO)
e.g., InFO-oS (TSMC), FOCoS (ASE)



2.5D/3D

Si Interposer, Si bridge
e.g., CoWoS (TSMC), EMIB, Foveros (Intel)



FC BGA SUBSTRATE TECHNOLOGY DEVELOPMENT TREND

ABF material has matured and can now support FC BGA requirements. It is undergoing continuous innovation to meet development roadmaps.

Driver	Requirement trends
Heterogeneous integration	Large body/package size (up to 100x100mm^2)
High I/O count	Higher layer count (>20L)
High-density interconnect	Targeting L/S 5/5µm and below to 3/3µm by 2027. FC pitch 60µm and below
Increase bandwidth	High-speed transmission
Increase assembly yield	Lower warpage
More functionalities	Thermal management
Development direction	
New materials with low Dk (<3), Df (<0.004), PID, low surface roughness (<200nm)	
New advanced tools such as sputterers, coaters, steppers, LDI and UV lasers for fine lines, small via/pad registration	
High-stiffness/-toughness materials to manage warpage or overcome SR cracking issues	
Integrated substrate with embedded passive component (R/L/C) for better signal & thermal management	

THE SUBSTRATE SHORTAGE:
A Return To The Supply-Demand Balance in 2023?

Substrate Shortage Reasons

Market demand

- Resurgence of automotive demand by the end of 2020, electric vehicles and autonomous driving trends driving demand for ADAS & infotainment chips, which mainly use FCBGA chips.
- Growth of 5G phones & 5G infrastructure: RF SiPs, AiPs, networking devices.
- Growth of AI, networking, data centers, cloud computing: demand for CPU, GPUs, AI ASICs, FPGAs, DIMMs, etc.

Technological trend

- Heterogeneous integration using various Advanced Packaging technologies such as high-end FC BGA-SiP, 2.5D/3D, fan-out on substrate, chiplets, etc., which require laminate substrate and drive its demand.
- Package size increase: 2.5D interposer up to 100x100mm^2; PC/notebook up to 50x50mm^2, networking & server up to 85x85mm^2, AI/HPC up to 100x100mm^2. Due to package size increase, fewer substrate units are available in one panel.
- Substrate layer increase. Trend in number of layers: PC/notebook 10-12L, networking/server 16-20L, AI/HPC 20-22L.

Supply chain disruption

- Covid-19 lockdowns affected substrate production and supply.
- Increase in equipment lead times.
- Fire in the Unimicron factory.
- There was no serious investment in increasing substrate capacity in the last ten years. Currently, substrate suppliers are investing heavily in capacity expansion to meet the demand.
- Low yield for large body size (>50x50mm^2) and higher layer count (18-20) substrate.

The decreasing demand from the end customers reduced the pressure on the IC substrate market and helped to ease the shortage as most companies have cut/stopped the orders.

The rise of the AI industry is expected to drive long-term growth for ABF substrate.

Factors leading to the end of the substrate shoratge

- New investments to increase the production capacity
- The end of lockdowns started contributing to normalize the supply chain and reduce lead times.

THE SUBSTRATE SHORTAGE

Investing in Capacity Expansion: The Key to Resolving Substrate Shortages

- The IC substrate shortage is mainly due to strong demand from major chipmakers, including Intel, AMD, and Nvidia, for high-end CPUs, GPUs, and 5G networking chips. In addition, the demand for computing devices has exploded driven by AI, HPC, and networking, among others, during the COVID-19 pandemic, which requires FC BGA substrates to package xPU chips. Other factors contributing to the substrate shortage include the increase in package size and the need for increased layer counts. The supply chain constraints related to the Covid-19 pandemic, highly increased inflation, and geopolitical tensions were also impacting material availability negatively.
- Substrate suppliers are investing heavily in capacity expansion to respond to the shortage, but it takes some time until this capacity comes online. In the last two years, end customers started securing the supply of FCBGA substrate through long-term agreements longer than three years and co-investments with substrate suppliers.
- However, some updates are indicating that the ABF substrates shortage is easing as demand weakens from major US CPU/GPU vendors who have sharply slashed orders. Moreover, Ajinomoto may invest in a new manufacturing plant to produce more ABF to contribute to the supply of ABF substrates. LG Innotek plans to boost the production of FC-BGA packages in the second half of this year and become the No. 1 player in the market by increasing its share to 30% or more. While low-end IC substrate shortage seems to be pretty much resolved due to weakness in demand in the mobile and consumer market, there is still demand for high-end IC substrates. Despite headwinds hitting the HPC segment, AI, cloud computing and the automotive markets will remain on a growth trend, and the demand for mainstream FC-BGA packaging is still rosy in the medium and long term.
- In sum, the semiconductor industry is still facing some substrate shortages, which are expected to end or at least further ease shortly. The investment in capacity expansion by substrate suppliers and the entry of new players will help ease the shortage to some extent.

THE LATEST INVESTMENTS BY SUBSTRATE SUPPLIERS (1/2)

Calumet ELECTRONICS	• In May 2022, Calumet announced that they will invest $6.5M to be the first supplier to bring IC substrates to the United States. The demonstration builds using SAP technology are nearly complete. These products represent demand of 1.5 million units from defense contractors and other customers working with 5G, satellite communications, and health care.
Unimicron	• Unimicron's new ABF substrate plant in Yangmei was set to start commercial runs in the second half of 2021 to offer dedicated processing capacity for Intel. Unimicron announced a total capital expenditure budget of about $1.4B for 2022, mostly to support further capacity expansions for ABF substrate production. • In May 2021, the Chinese government approved funds of €70.6 million to relocate the Unimicron manufacturing facility for HDI, SLP and IC substrate to the Kunshan New and High-tech Industrial Development Zone. Production is expected to start in April 2023. • Unimicron Technology and Subtron Technology announced that they will merge at the end of 2022. Subtron is a company specializing in developing and manufacturing 5G SiP substrate. The merger will complement both companies' IC substrate technologies and products and will allow the integration of resources to expand product portfolios.
AT&S	• AT&S announced that was building its first high-end PCB and IC substrate production facility in Southeast Asia, in the Kulim Hi-Tech Park, Kedah, Malaysia. The project involves a total investment of €1.7 billion with commercial operations targeted to start in 2024 and full-capacity production in 2026. Recently, AT&S announced plans to establish an IC substrate institute at a Malaysian university. • AT&S has started the construction of its new research center in Leoben, Austria. AT&S is investing a total of €500 million until 2025 in this new building to serve both research and production.
IBIDEN	• Ibiden announced that it will expand its high-end ABF substrate production capacity. It is investing JP¥180 billion (US$1.66 billion) in the construction of a new building, which is planned to start production in 2023. From 2023 onwards, the company plans to increase the production line capacity even further to meet the demand for IC substrate for high-end applications.
景碩科技	• Kinsus is expected to increase its production capacity for ABF substrate by 30-40% in 2022, and by another 40% in 2023. A total investment of NT$4.485 billion (US$0.15 billion) is expected.
SAMSUNG ELECTRO-MECHANICS	• In late 2021, Samsung Electro-Mechanics announced it would invest US$920 million to build FC-BGA substrate facilities and infrastructure at its plant in Thai Nguyen Province, Vietnam. • In March 2022, the company announced that it will expand its ABF substrate production capacity at its Busan plant, bringing its total investment in the segment to KR₩1.6 trillion (US$1.32 billion). The main targets are high-speed computing applications including CPUs and GPUs.

THE LATEST INVESTMENTS BY SUBSTRATE SUPPLIERS (2/2)

TOPPAN	• In April 2022, Toppan announced the acquisition of Thai packaging manufacturer, Majend Makcs Co., Ltd., a manufacturer and supplier of flexible packaging.
LG Innotek	• LG Innotek is entering the FC BGA market and has announced that it will spend ₩413 billion ($280M)to build a production line. In the future, the company plans to increase its FC BGA investments. Until now, LG Innotek has mainly focused on IC substrate such as FC-CSP and SiP which are mostly used for mobile devices and IoT applications.
NYPCB	• In 2021, Nan Ya PCB announced plans to invest NT$8.4 billion to expand production capacity for ABF substrate at its factory sites in Shulin, Taiwan, and Kunshan, China. The capacity expansion includes three phases of investment: the first and second, in Shulin and Kunshan respectively, will start operations in 2023; the third, taking place in Shulin, will be ready by 2024. • The Taiwanese site will focus on high-end ABF substrate, whereas in China production will be focused on more mature products.
SIMMTECH	• Simmtech announced the opening of a new facility in Penang. It is the company's eighth factory, adding to its existing operations in Korea, China, and Japan. The facility will reportedly produce two million PCBs and 60 million units of substrate per month when it is in full operation.
臻鼎科技集團 Zhen Ding Tech. Group	• Zhen Ding is investing NT$15 billion (US$535.71 million) to set up a new plant in China dedicated to ABF substrate for processing HPC chips. The new fab is slated to start commercial runs in 2023, mainly to serve major chipmakers including AMD, Nvidia and Xilinx. The company has also built a new BT substrate plant in China, at a total cost of NT$8 billion. It will become operational in the fourth quarter of 2022 and will supply substrate for processing of mobile APs and RF modules from MediaTek, Qualcomm and Apple, SiP and AiP substrate, and high-end HDI and SLP for handset applications. • In 2022, Zhen Ding announced plans to invest NT$60 billion in the next four years (NT$15bn per year) for IC substrate expansion.
DAEDUCK	• Around 2020, Daeduck stopped SLP operations due to low profitability. • In 2021, Daeduck announced an investment of KR₩70 billion to expand its production capacity for FC BGA. In 2020, the company had already announced a KR₩90 billion investment. Recently, the company announced that will invest up to KR₩400 billion for FC-BGA expansion by 2022, given the growing demand for FC-BGA, securing four times higher FC-BGA production capacity in 2023 compared to 2021.
SHINKO	• In May 2022, Shinko opened a new plant in Chikuma City, Nagano Prefecture to strengthen its production system for flip-chip substrate.
SCHWEIZER	• In August 2020, Schweizer Electronic AG formed a sales representative agreement with Varikorea Co., Ltd to promote Schweizer's high-tech printed circuit boards and embedding solutions in South Korea.

FINANCIAL ANALYSIS

KEY HIGHLIGHTS OF THE FINANCIAL ANALYSIS

- With $11.95B of revenues (with SPIL and excluding USI), ASE maintained its position as the market leader in 2022.
- As ASE and TSMC reached new heights with record income and capabilities, Taiwan will continue to increase its market share for OSAT, reaching 43% in 2022.

- The overall income generated by OSATs climbed from $28.1B in 2021 to $45.9B in 2022. Nearly 26% of the overall OSAT revenue was produced by ASE (excluding USI revenues), whereas the sum of ASE, Amkor, and JCET was 53% of the entire OSAT revenue.
- The amount spent on OSAT R&D in 2022 increased significantly from $1.31B to $1.58B.
- Total AP CapEx increased to $18B in 2022 from around $16B in 2021.
- In the top 30 OSAT rankings for 2022, SJ Semi was ranked # 18 after being out of the ranking in 2021.
- LB Semicon dropped to #27 in 2022 from #23 in the top 30 OSATs.
- The player ranking in 2022 included 7 Chinese OSATs (Payton, Forehope, TFME, SJ semi, Hitech Semi, Huatian & JCET), two IDMs (Intel and Samsung), and one foundry (TSMC).
- For Intel, TSMC, and Samsung, no estimate was made for packaging-only operations as their R&D, Net Margin and Gross Margin accounted for all of their activities.

- To address the rising need for high-performance computing and artificial intelligence applications, there is an increased focus on advanced packaging technologies, such as 3D integration and heterogeneous integration. Due to its capacity to decrease package size and cost, fan-out wafer-level packaging (FOWLP) is also becoming more and more popular for usage in mobile and Internet of Things (IoT) applications.

KEY FINANCIAL OVERVIEW FOR TOP 30 PLAYERS

Revenue in $M
Financial Ratios in %

Revenue, YoY Growth, R&D, CapEx, Gross Margin, and Net Margin for the top 30 players in 2022.

Rank	Company	BM	Location	Revenue [$M]	Growth [%]	R&D [$M]	Margin [%]	CapEx [$M]	Margin [%]	Gross Profit [$M]	Margin [%]	Net Income [$M]	[%]
1	ASE (With SPIL) ASE (With SPIL & USI)	OSAT	Taiwan	$11,95B $21.8B	17.70%	$481M	3.60%	$2,363M	10.80%	$3,887M	20.10%	$2,020M	17%
2	Amkor	OSAT	US	$7,092M	15.50%	$149M	2.10%	$908M	12.80%	$1,330M	18.80%	$766M	11%
3	Intel	IDM	US	$5,500M	-20%	$18,853M	29.90%	$25,050M	39.70%	$26,866M	42.60%	$8,104M	-60%
4	TSMC	Foundry	Taiwan	$5,313M	42.60%	$5,302M	7.20%	$35,219M	47.80%	$43,862M	59.60%	$33,068M	54%
5	JCET	OSAT	China	$4,895M	10.70%	$190M	2.23%	$589M	11.60%	$834M	17.00%	$469M	10%
6	Samsung	IDM	Korea	$4,000M	8.10%	$19,921M	8.30%	$39,255M	16.40%	$89,094M	37.10%	$43,463M	32%
7	TFME	OSAT	China	$3,107M	35.50%	$192M	5.95%	$1,023M	33.30%	$432M	13.70%	$102M	3%
8	Powertech	OSAT	Taiwan	$2,730M	0%	$79M	2.90%	$607M	22.20%	$565M	20.70%	$283M	10%
9	Huatian	OSAT	China	$1,726M	-1.60%	$103M	6.17%	$780M	45.20%	$283M	16.40%	$109M	6%
10	UTAC	OSAT	Singapore	$1,690M	14.90%	$80M	4.7%	$310M	18.34%	$600M	35.5%	$345M	20.4%
11	King Yuan	OSAT	Taiwan	$1,197M	9.00%	$41M	3.40%	$338M	28.30%	$425M	35.50%	$222M	19%
12	Hana Micro	OSAT	Taiwan	$798M	14.60%	$10M	1.40%	$93M	11.60%	$119M	14.90%	$61M	8%
13	Chipbond	OSAT	Taiwan	$781M	-11.30%	$25M	3.20%	$120M	15.30%	$255M	32.60%	$202M	26%
14	ChipMOS	OSAT	Taiwan	$765M	-14.20%	$37M	4.90%	$153M	20.00%	$160M	20.90%	$110M	14%
15	Sigurd	OSAT	Taiwan	$608M	12.10%	$14M	2.30%	$131M	21.50%	$180M	29.60%	$99M	16%
16	Hitech Semi	OSAT	China	$556M	-2%	$35M	6.3%	$10M	1.8%	$167M	30%	$91M	16,4%
17	SFA Semicon	OSAT	Japan	$555M	9.10%	$2M	0.30%	$43M	7.70%	$63M	11.40%	$34M	6%
18	SJ Semi	OSAT	China	$537M	141%	$7M	1.3%	$65M	12.1%	$85M	15.8%	$47M	8.8%
19	Carsem	OSAT	Malaysia	$526M	2.60%	$12M	2.20%	$94M	17.90%	$90M	17.20%	$53M	10%
20	Greatek	OSAT	Malaysia	$519M	-18.00%	$8M	1.60%	$143M	27.50%	$138M	26.50%	$103M	20%
21	OSE	OSAT	Malaysia	$505M	-2.60%	$11M	2.20%	$36M	7.00%	$82M	16.20%	$47M	9%
22	Ardentec	OSAT	Malaysia	$472M	21.60%	$17M	3.60%	$200M	42.30%	$193M	40.80%	$115M	24%
23	Nepes	OSAT	Korea	$467M	32.90%	$57M	12.20%	$193M	41.30%	$98M	21.10%	$62M	13%
24	Tong Hsing	OSAT	Taiwan	$457M	-11.53%	$12M	2.60%	$109M	23.80%	$163M	35.60%	$73M	16%
25	Payton	OSAT	China	$448M	10.3%	$9M	2%	$111M	24.8%	$74M	16.5%	$58M	12.9%
26	Unisem	OSAT	Taiwan	$406M	13.80%	$2M	0.50%	$136M	33.40%	$76M	18.80%	$88M	22%
27	LB Semicon	OSAT	Korea	$404M	-4%	$3M	0.84%	$192M	31.00%	$72M	17.30%	$32M	8%
28	Formosa	OSAT	Taiwan	$339M	5.00%	$5M	1.60%	$19M	5.70%	$71M	21.00%	$67M	20%
29	Inari	OSAT	Malaysia	$336M	-5.10%	$4M	1.2%	$12M	3.50%	$101M	30.20%	$86M	26%
30	Forehope	OSAT	China	$317M	6.30%	$13M	4.10%	$142M	44.79%	$23M	7.30%	$30M	-36%

(*) NOTES
- Only revenue and CapEx are estimated for packaging activity related to Intel, TSMC, and Samsung.
- ASE & SPIL revenue is separated from USI to provide a clearer picture of OSAT-specific business.

*Estimation

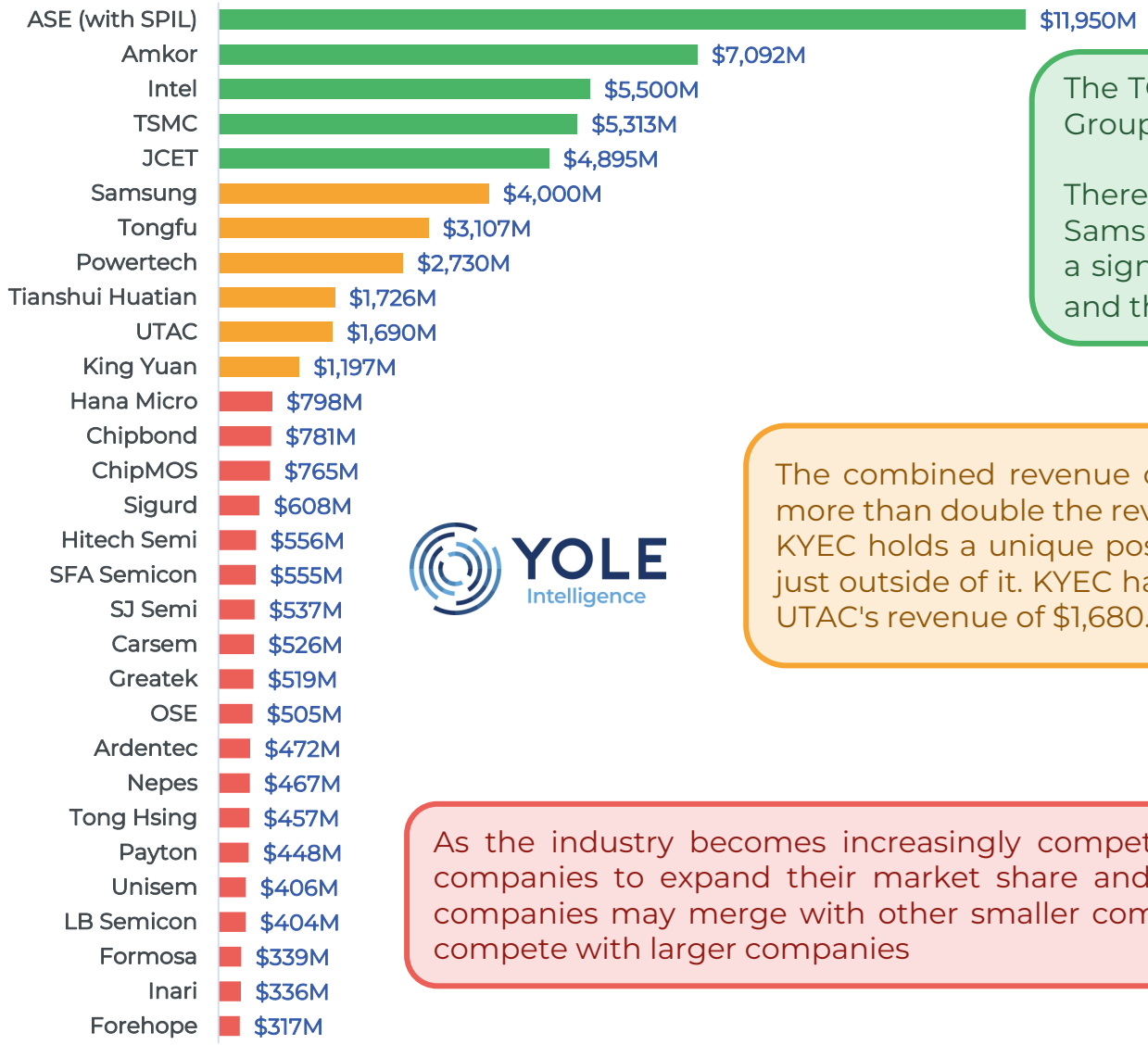
FINANCIAL OVERVIEW FOR TOP 30 PLAYERS

Revenue in 2022

Big players were separated from the rest.

The top 8 players dominate the market in revenue and continue with heavy investment in CapEx and R&D.

TOP 30 players ranking by 2022 revenue [$M]



The TOP 5 players hold a significant market share, with ASE Group (with SPIL) having the highest revenue at $11,950 M.

There is a noticeable drop in revenue from JCET to Samsung and TFME, with a difference of $800M, indicating a significant difference in market share between the TOP 6 and the rest of the companies.

The combined revenue of the TOP 11 companies amounts to $49 B, which is more than double the revenue of the remaining players combined.
KYEC holds a unique position in this group as it is close to the top 10 but falls just outside of it. KYEC has a revenue of $1,200, which is only slightly lower than UTAC's revenue of $1,680.

As the industry becomes increasingly competitive, larger companies may look to acquire smaller companies to expand their market share and gain a competitive advantage. Additionally, smaller companies may merge with other smaller companies to combine resources and expertise to better compete with larger companies

2022 REVENUE GROWTH FOR TOP 30 PLAYERS

Ranking based on YoY Growth (%) 22/21*

SJ Semi registered the biggest % revenue growth – of 141% YoY growth.

In 2022, 9 OSATs showed negative YoY figures.

Among the TOP 10 companies, that recorded a positive YoY growth, there are 9 OSATs and one foundry (TSMC).

2022 has been a more challenging year as more companies registered a negative YoY growth (10 players) compared to 2021 (3 players). The 10 players are OSATs except Intel, an IDM.

"YoY %" is the revenue growth ratio from 2021 to 2022

2022 R&D SPEND OF TOP 30 PLAYERS

Ranking based on R&D [%]*

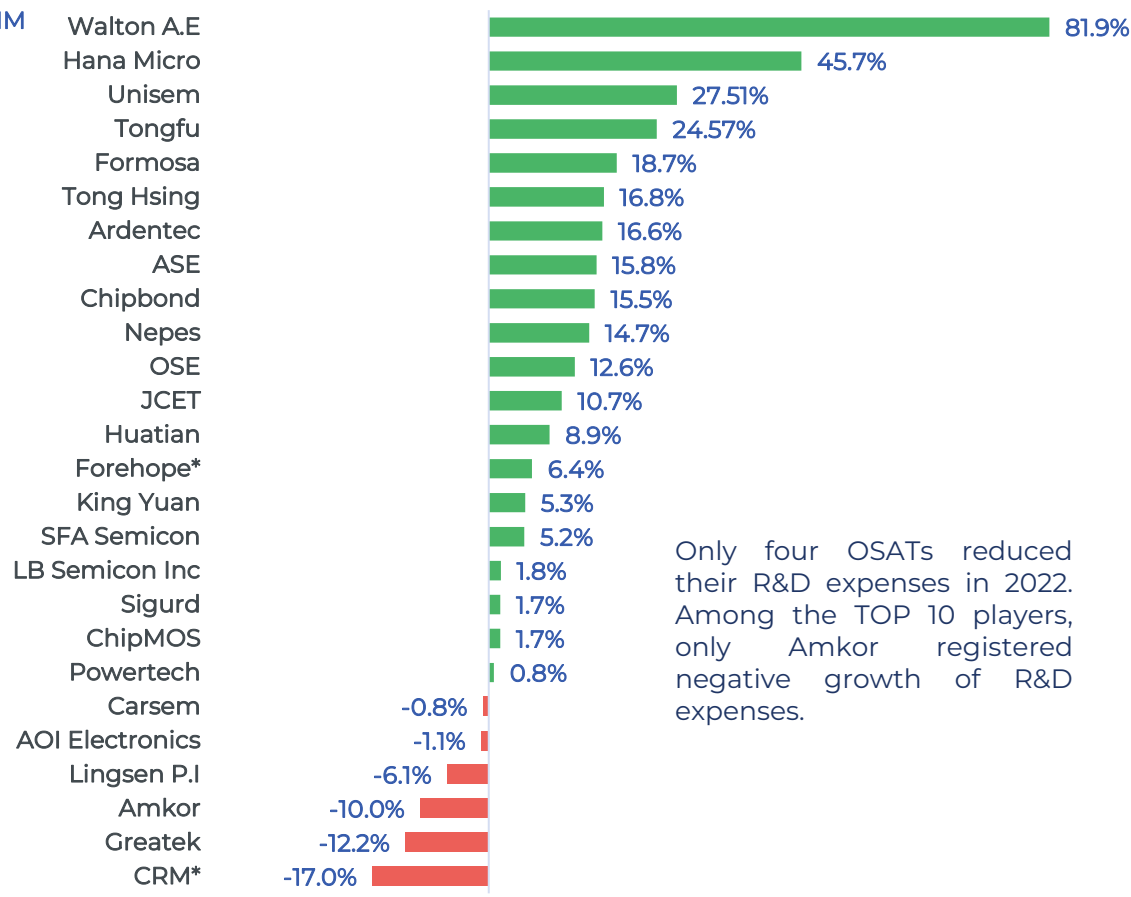
Walton Advanced Engineering had the biggest YoY growth of R&D expense at 81.9%, followed by Hana Micro, TSMC, TFME , and Formosa.

ASE's total R&D spending (with SPIL) was $481M representing 3.6% of its revenue.

2022 R&D expenses ($M) and margin (%)

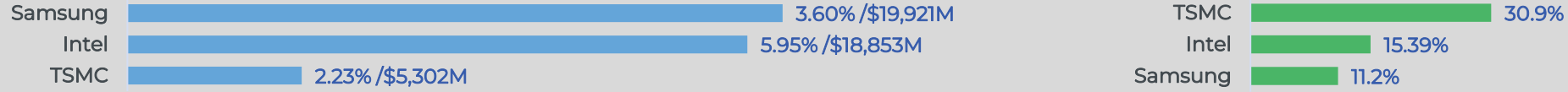
There is an important gap in R&D spend between the top 8 OSATs (>$50M) and the rest of players. ASE is the only player with >$480M spend in R&D. 7 players have R&D spend <$10M. Players with a lower R&D expenditure will not be able to support themselves in the medium and long run. They only have a few options: either increase their R&D spending or prepare for acquisitions.

2022 R&D YoY Growth(%)



Only four OSATs reduced their R&D expenses in 2022. Among the TOP 10 players, only Amkor registered negative growth of R&D expenses.

Foundry and IDMs



* R&D [%] is "R&D to Revenue Ratio" or "R&D/Revenue"

2022 CAPITAL EXPENDITURE OF TOP 30 PLAYERS

Ranking based on CapEx [%]*

Forehope Electronic had significant investments in 2022, with a CapEx of $170M, representing 53% of its revenue, followed by TSMC, Huatian Tehcnology, Nepes, Ardentec.

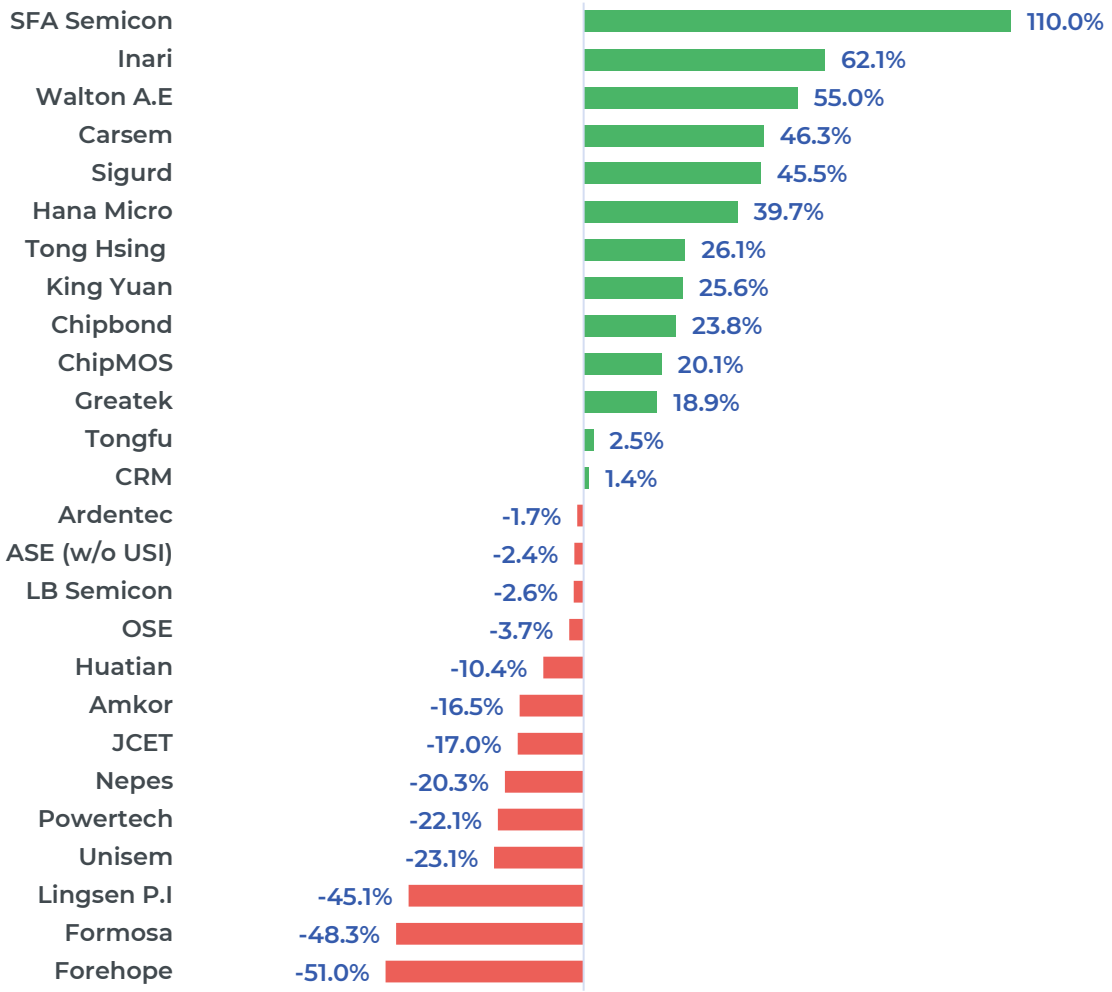
The highest CapEx spend in 2022 comes from Intel, TSMC, ASE, Samsung and TFME.

2022 Capex ($M) and margin (%)

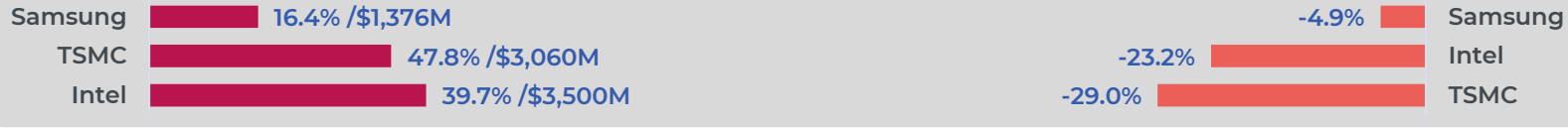
YOLE Intelligence

ASE spent ~US$2.4B CapEx in 2022 (excluding USI). This is more than 2.3 times more than the next biggest OSATs: TFME (~ $1.1B) and Amkor ($908M). 8 Players spent less than $100M CapEx.

2022 CapEx YoY Growth(%)



Foundry and IDMs



YOLE Intelligence

* CapEx [%] is "CapEx to Revenue Ratio" or "CapEx/Revenue"

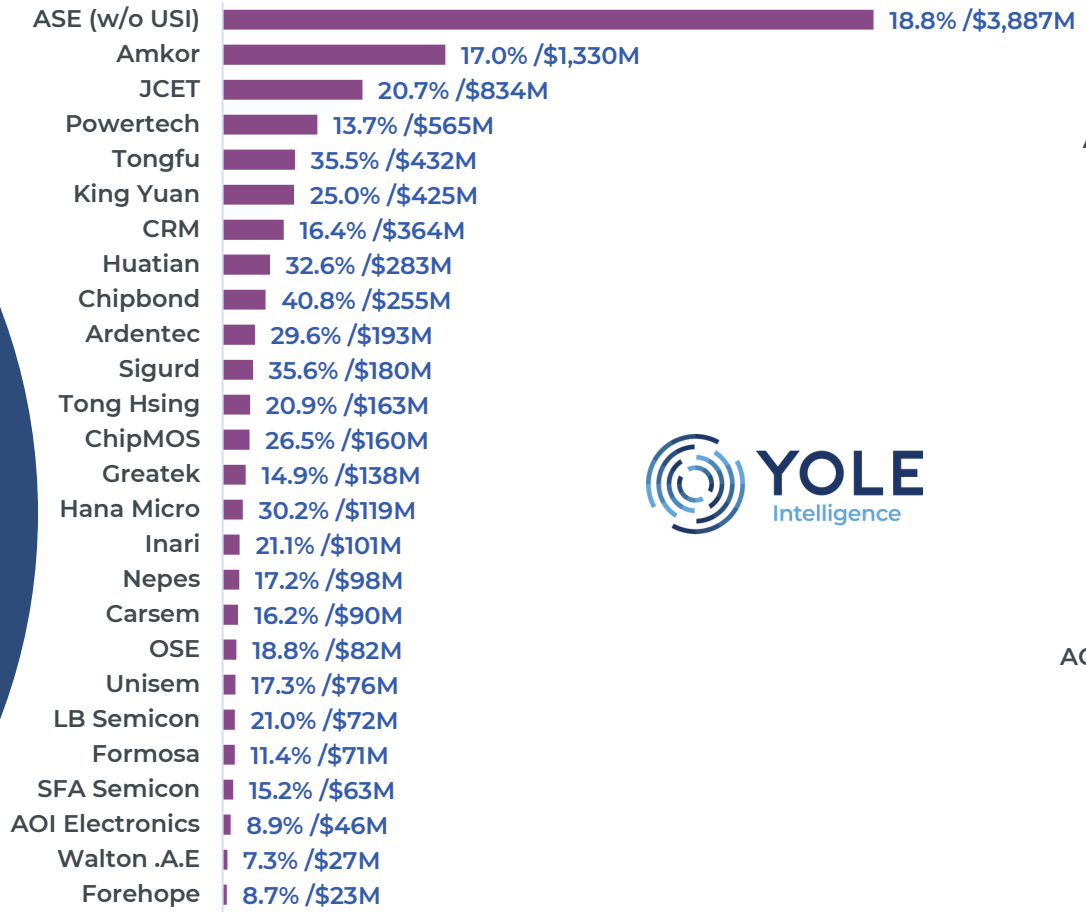
2022 GROSS MARGIN OF TOP 30 PLAYERS

Ranking based on Gross Margin [%]*

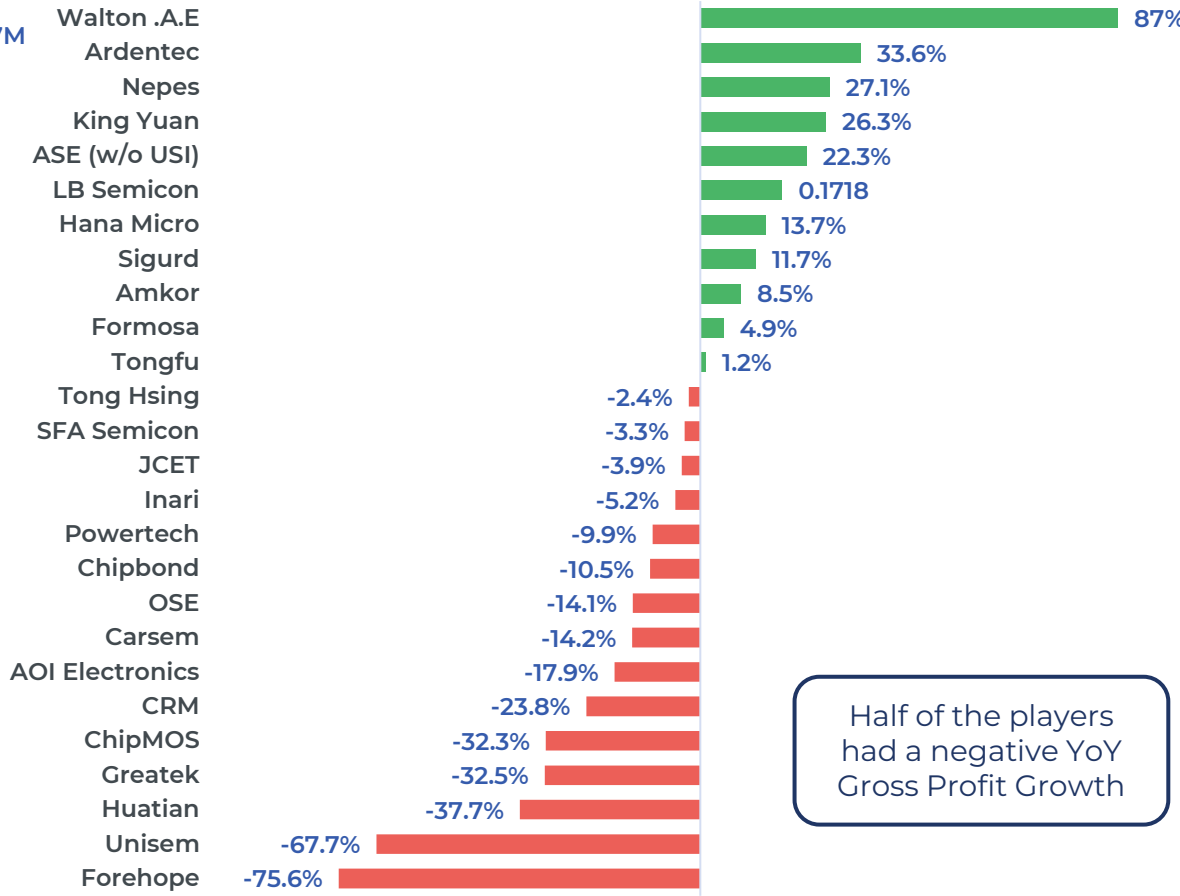
TSMC had the highest gross profit margin at 59.6%, followed by Intel, Ardentec, and Samsung.

Walton Adv. Eng. had by far the highest Gross Margin growth at 87%, followed by Ardentec, Nepes, KYEC, ASE, LB Semicon and Hana Micron

2022 Gross profit ($M) and margin (%)

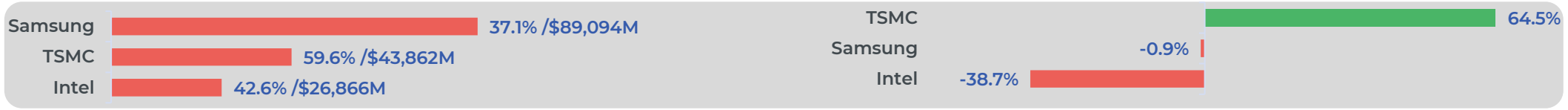


2022 Gross Profit YoY Growth (%)



Half of the players had a negative YoY Gross Profit Growth

Foundry and IDMs

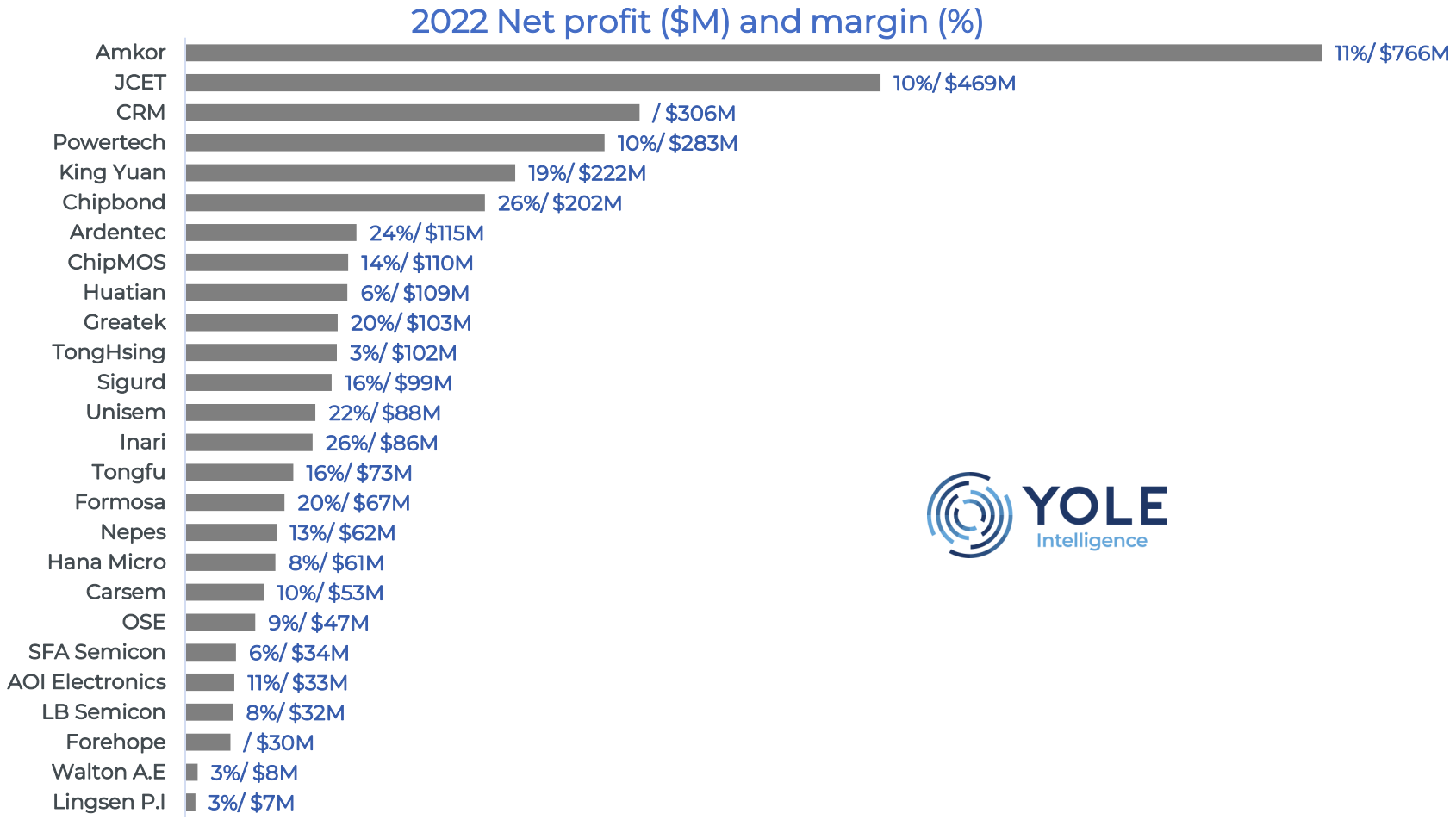


* Gross Margin [%] is "Gross Margin to Revenue Ratio" or "Gross Margin/Revenue"

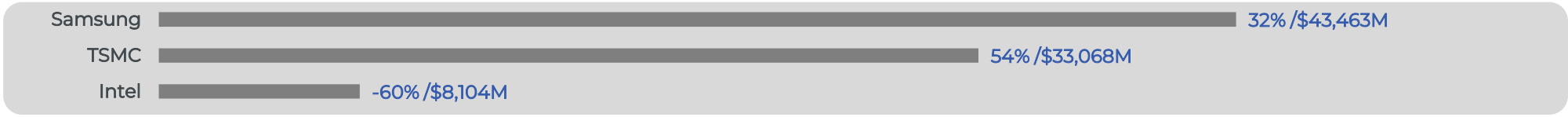
2022 NET INCOME OF TOP 30 PLAYERS

Ranking based on Net Margin [%]*

In 2022, TSMC recorded the highest net margin at 54% net. It is followed by Samsung with 32% and Chipbond and Inari both with 26% net margin.



Foundry and IDMs



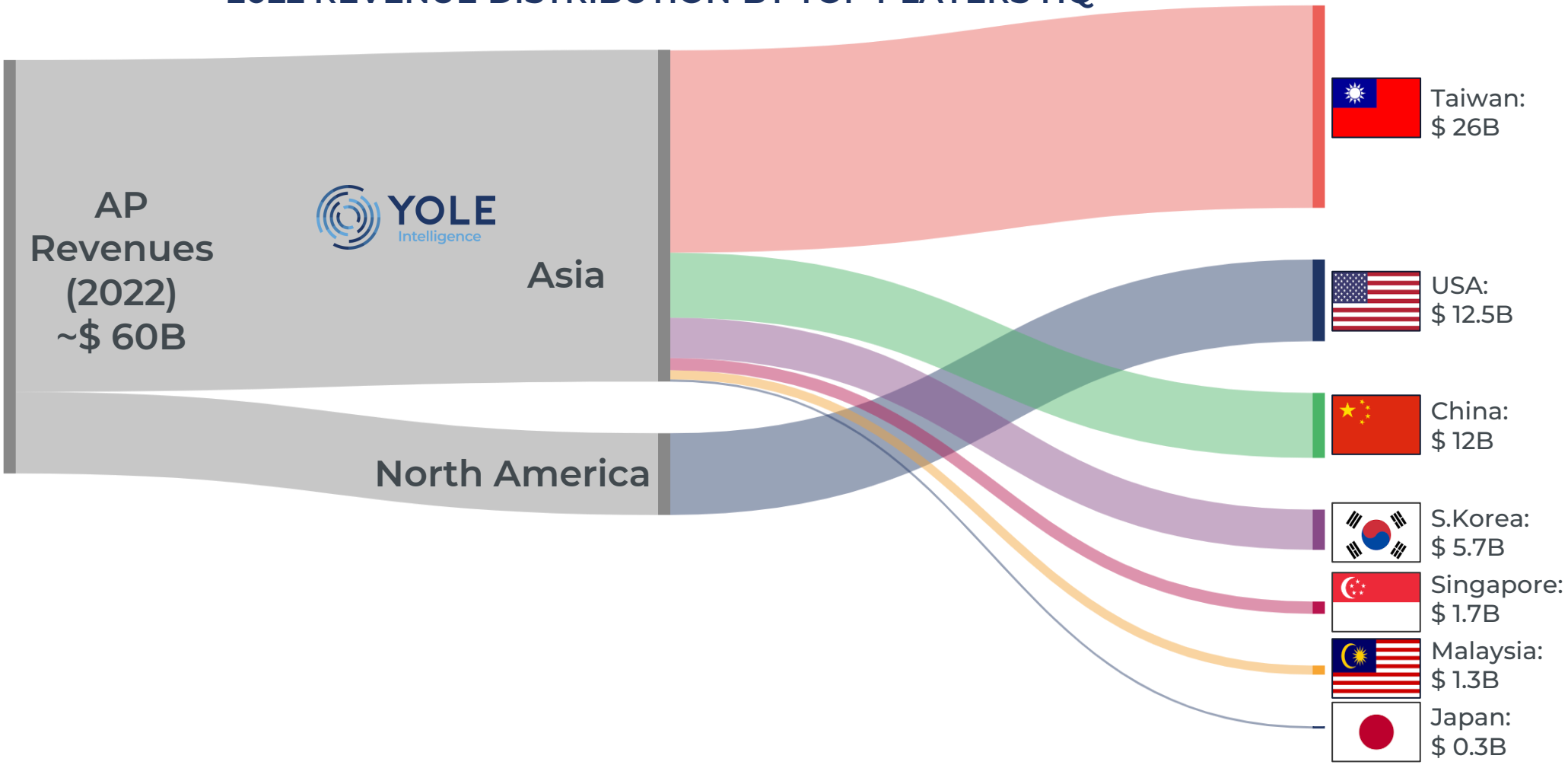
* Net Margin [%] is "Net Margin to Revenue Ratio" or "Net Margin/Revenue"

2022 REVENUE DISTRIBUTION OF TOP 30 PLAYERS

Based on company HQ location (Top 30 players)

Of the Top 30 players, Taiwan-based contributed half of the revenue in 2022, followed by the US. China came third, then South Korea, Singapore, Malaysia, and Japan.

2022 REVENUE DISTRIBUTION BY TOP PLAYERS HQ



TOP 30 PLAYERS (RANKING CHANGES BASED ON REVENUE)

Company	BM	Location	2022 Ranking		2021 Ranking		2020 Ranking
ASE (rev w/SPIL & w/o USI)	OSAT	Taiwan	1		1		1
Amkor	OSAT	US	2		2		2
Intel	IDM	US	3		3		3
TSMC	Foundry	Taiwan	4	1	5		5
JCET Group	OSAT	China	5	-1	4		4
Samsung	IDM	Korea	6		6		6
Tongfu Microelectronics	OSAT	China	7	1	8		8
Powertech Technology	OSAT	Taiwan	8	-1	7		7
Tianshui Huatian Microelectronics	OSAT	China	9		9		9
UTAC	OSAT	Singapore	10		10	1	11
King Yuan Electronics	OSAT	Taiwan	11		11	-1	10
Hana Micron (w/ Hana Materials)	OSAT	Korea	12	6	18	-4	14
Chipbond Technology	OSAT	Taiwan	13		13		13
ChipMOS Technologies	OSAT	Taiwan	14	-2	12		12
Sigurd Microelectronics	OSAT	Taiwan	15		15	4	19
Hitech Semi	OSAT	China	16	1	17		
SFA Semicon	OSAT	Korea	17	2	19	-4	15
SJ Semi	OSAT	China	18	17	35		
Carsem	OSAT	Malaysia	19	1	20		20
Greatek Elec	OSAT	Taiwan	20	-6	14	2	16
Orient Semiconductor Electronics	OSAT	Taiwan	21	-5	16	1	17
Ardentec	OSAT	Taiwan	22		22	3	25
Nepes Corporation	OSAT	Korea	23	5	28	-1	27
Tong Hsing	OSAT	Taiwan	24	-3	21	2	23
Payton	OSAT	China	25	-1	24		
UniSem Berhad	OSAT	Malaysia	26		26		26
LB Semicon Inc	OSAT	Korea	27	-4	23	-2	21
Formosa Advanced Technologies	OSAT	Taiwan	28	-1	27	-3	24
Inari	OSAT	Malaysia	29		29	-1	28
Forehope	OSAT	China	30	1	31	2	33

Kept position

Went up

Went down

In 2022, ASE remained #1 with Amkor #2, and Intel #3, while TSMC became #4.

A highly competitive landscape was observed for the remaining players.

Inari and forehope had the last positions in the TOP 30 ranking

- *No change in the top 10 this year: except ranking switch between TSMC/JCET and TFME/PTI.*
- *Hana Micron passed to the 12th place compared to the 18th last year.*
- *SJ Semi was out of the ranking last year and in 2022, it registered the #18 position.*
- *The rest of the ranking is more dynamic compared to 2021 ranking.*

As the same as 2021, the size drop is becoming bigger & bigger between the TOP 10 and the remaining players. This will lead to potential mergers or acquisitions in the short term, pushed also by the size drop inside the TOP 10 group.

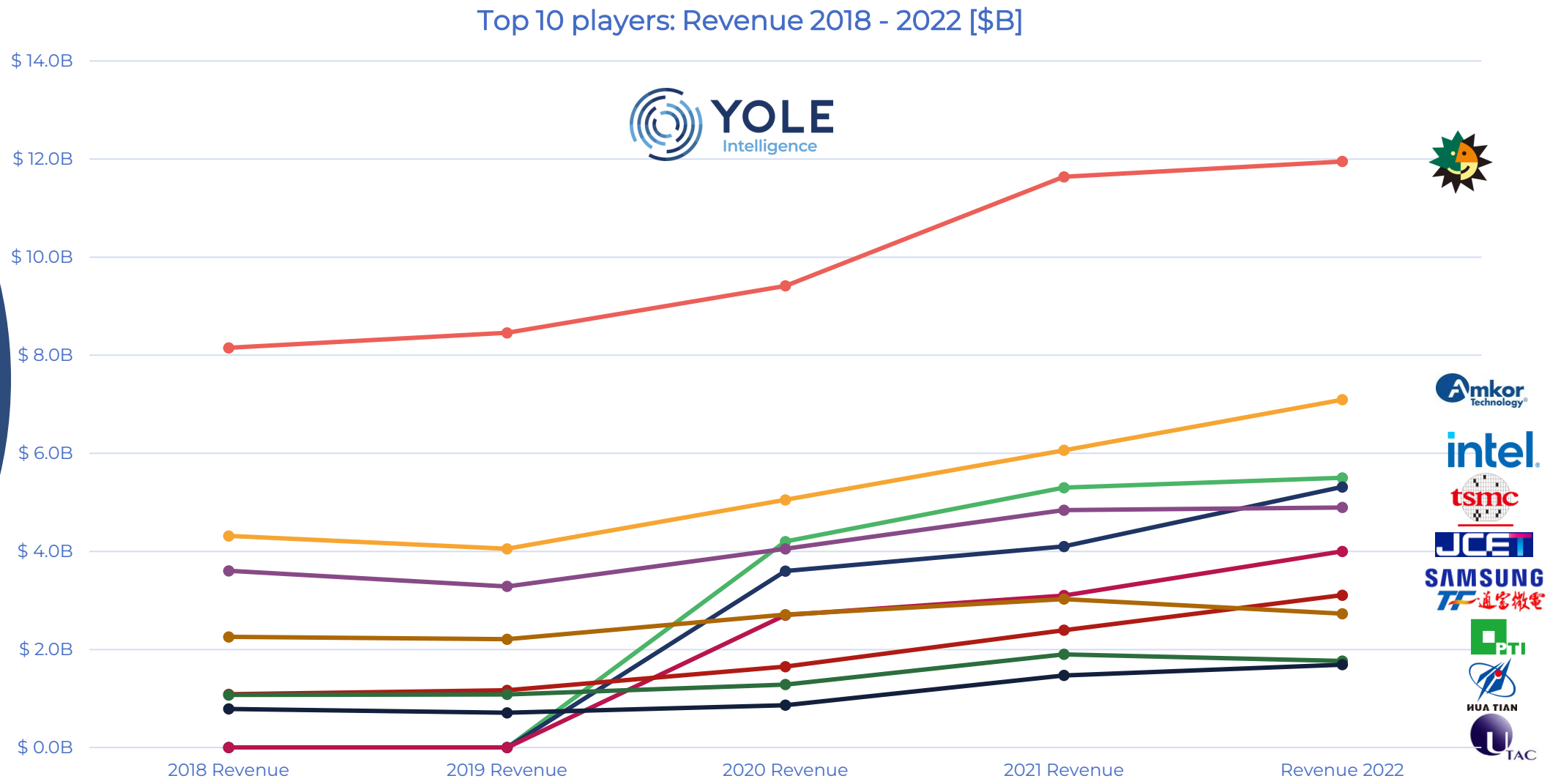
Ranking based on 2022 revenue

TOP 10 PERFORMANCE

By Revenue 2018-2022 (Overlay View)

In 2022, ASE remained top of the leaderboard, followed by Amkor, Intel, TSMC, Intel, and Samsung.

Tongfu passed to the #7 position.

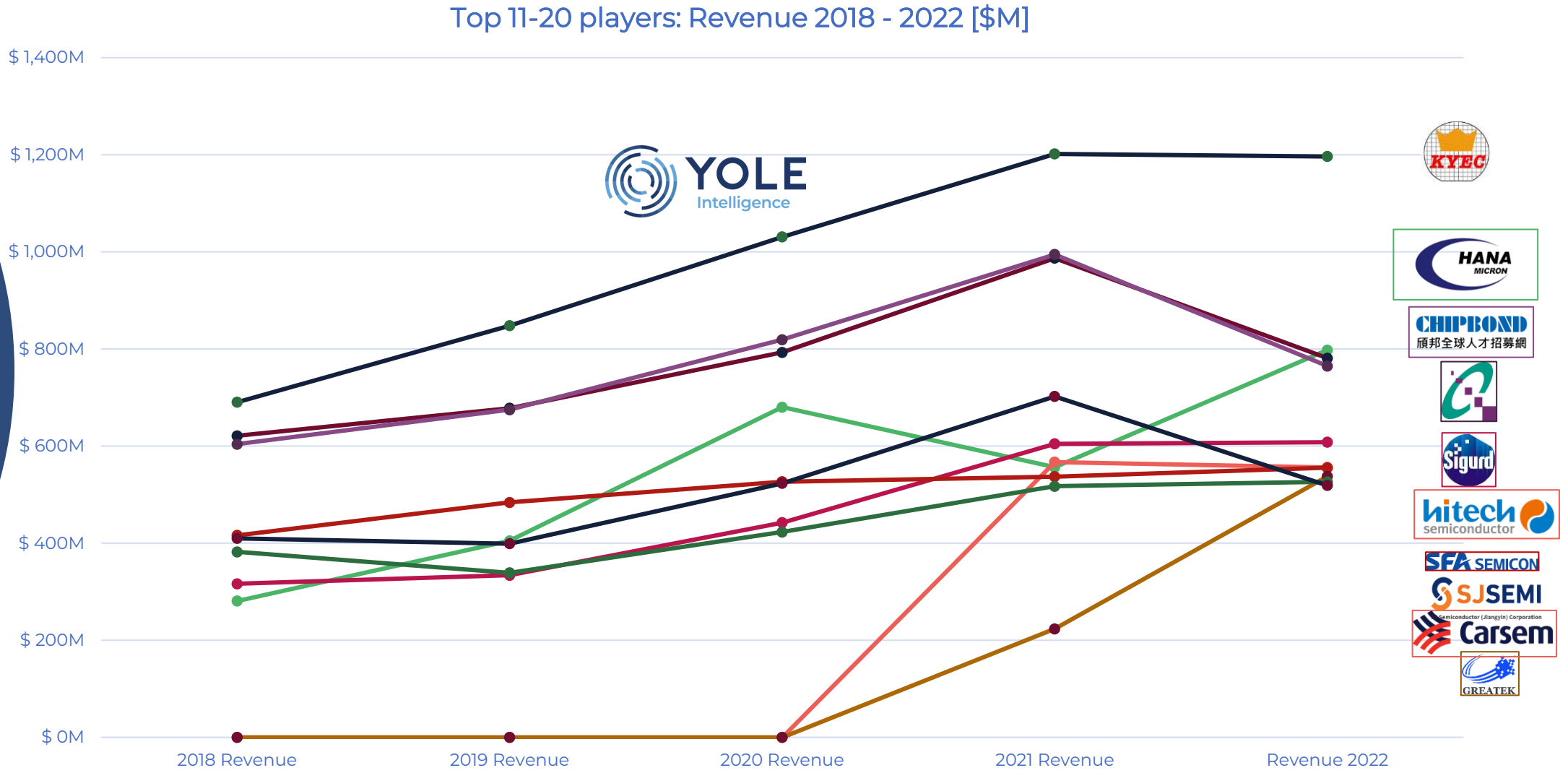


Ranking based on 2022 revenue

TOP 11 TO 20 PERFORMANCE

By Revenue 2013-2022 (Overlay View)

In 2022, KYEC kept its #11 position in player revenue but so close to the TOP 10 while Hana Micron passed to the #12 position.



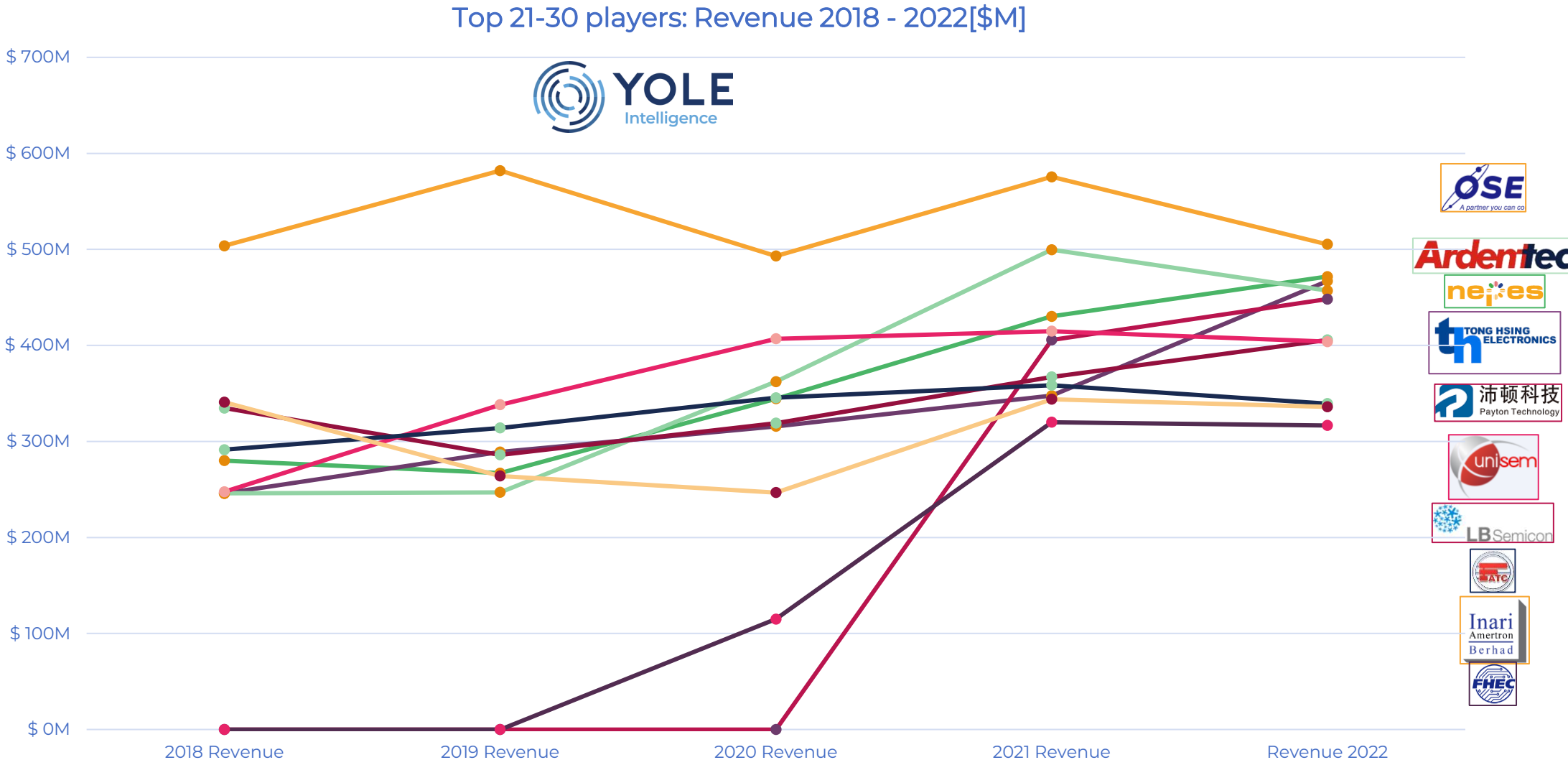
All the players experienced revenue growth in 2021 compared to 2020.

Ranking based on 2022 revenue

TOP 21 TO 30 PLAYERS PERFORMANCE

By Revenue 2013-2022 (Overlay View)

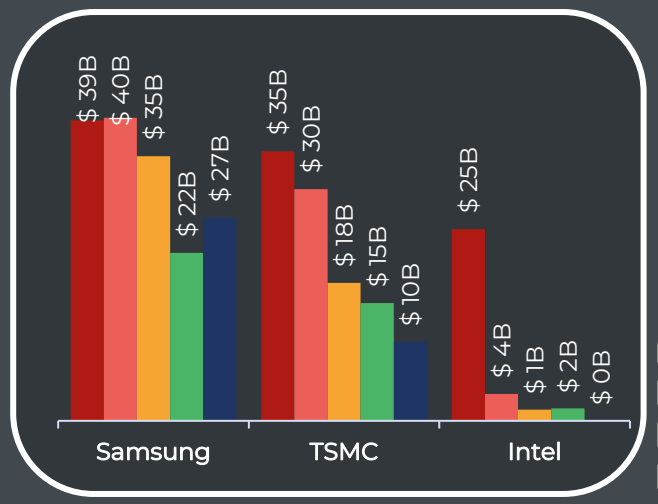
2022 was a dynamic year for most OSATs except for AOI electronics, Inari and LB Semicon.



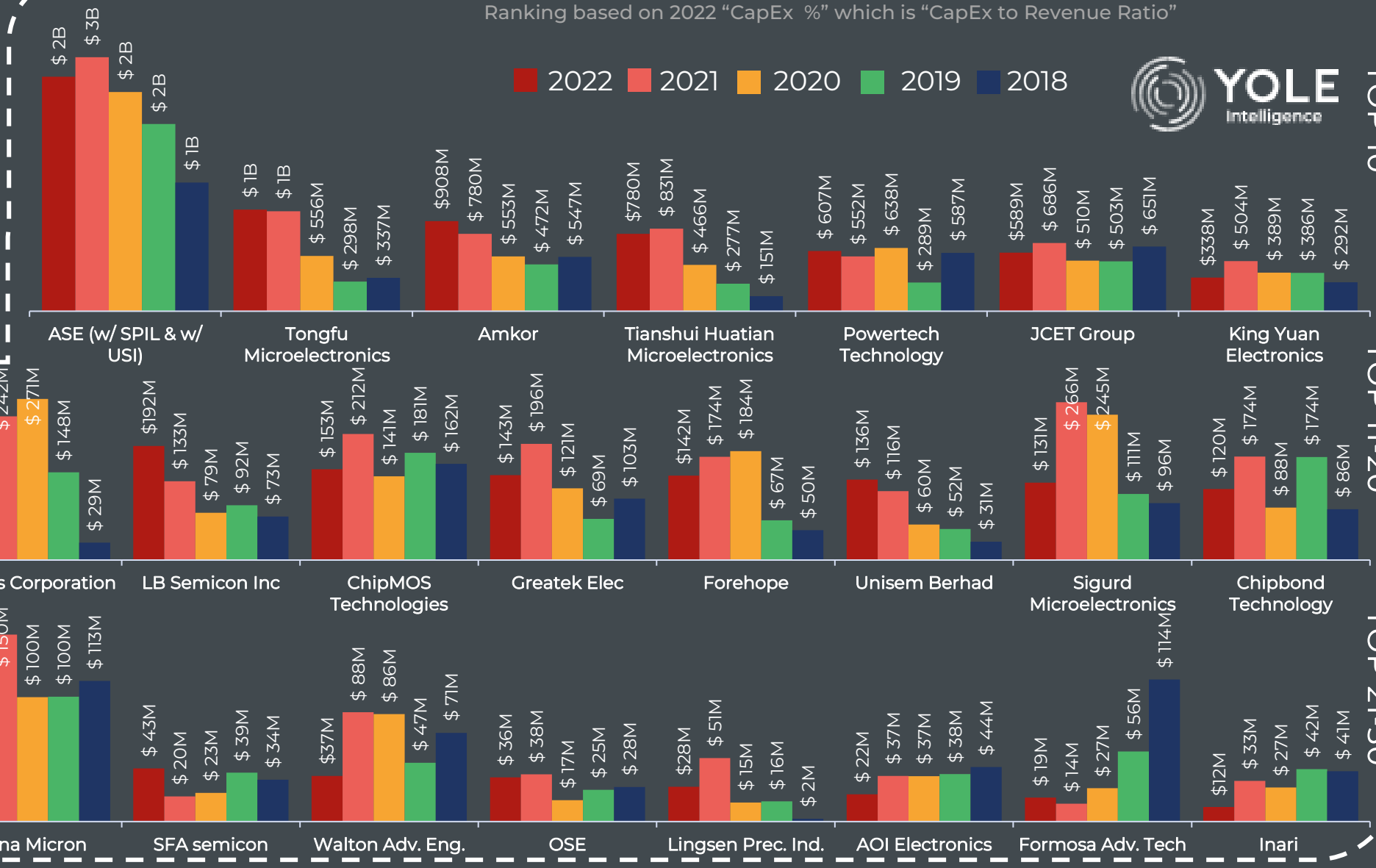
In 2022, more OSATs registered negative YoY growth compared to 2021.

Ranking based on 2022 revenue

TOP 30 PLAYERS: CAPITAL EXPENDITURE (CAPEX) [$M]



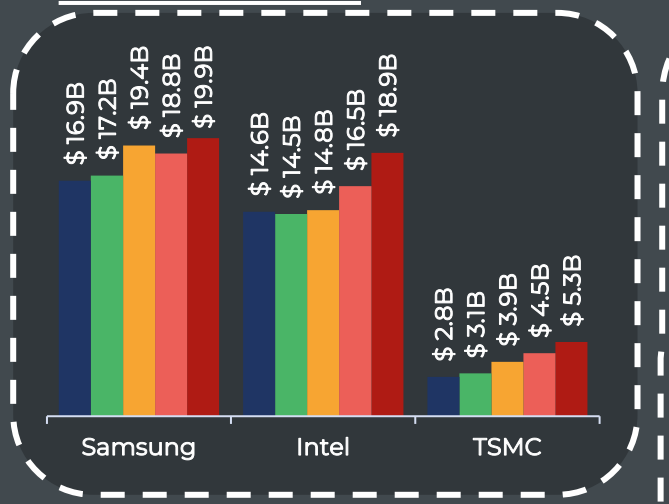
Ranking based on 2022 "CapEx %" which is "CapEx to Revenue Ratio"

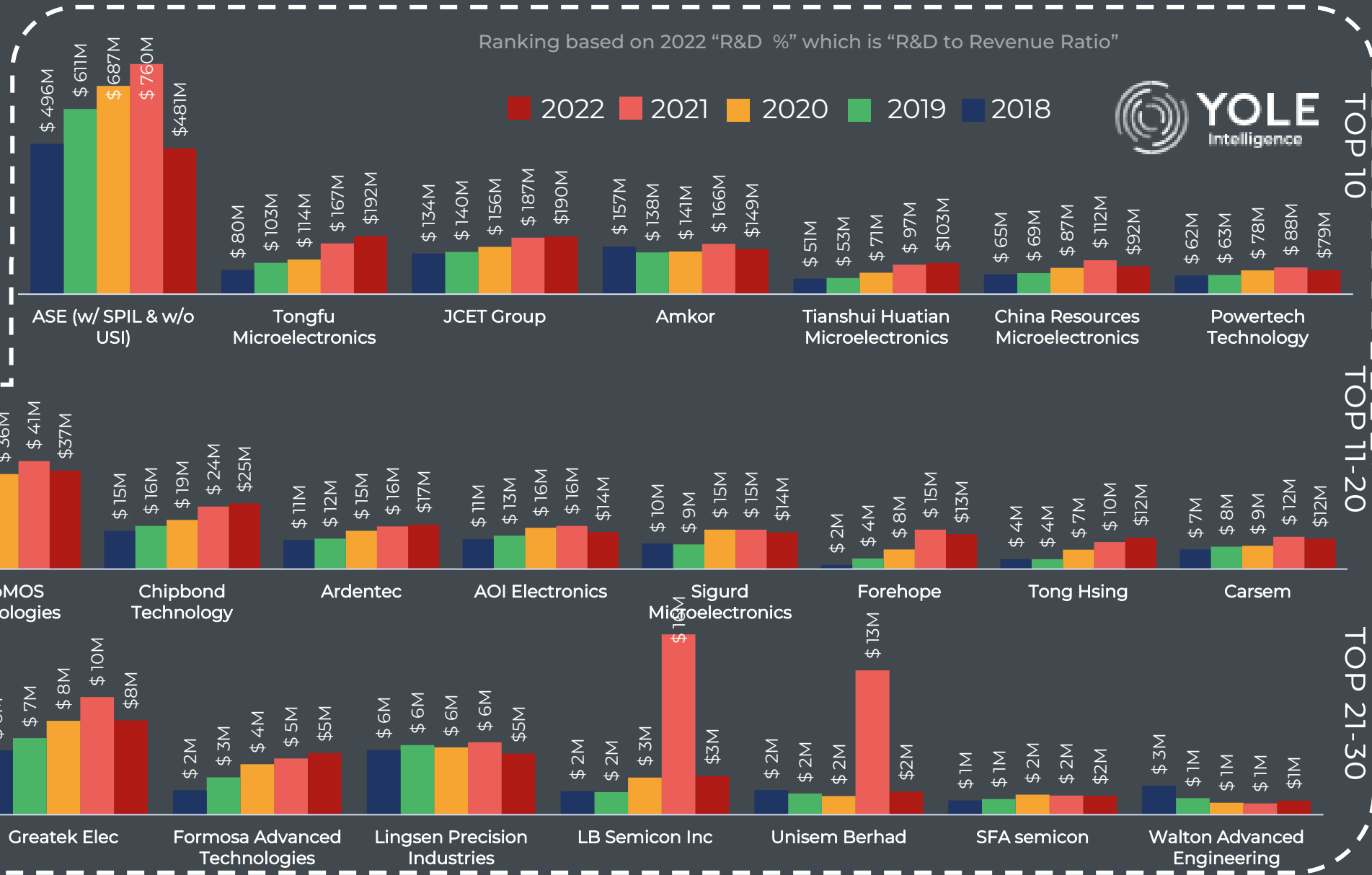


IDM and foundry

OSATs

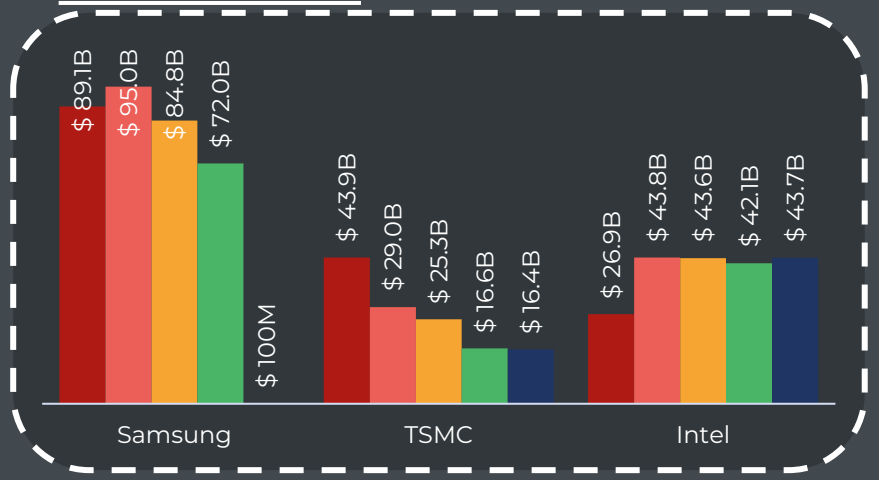
TOP 30 PLAYERS: R&D EXPENDITURE [$M]





IDM and foundry | OSATs

TOP 30 PLAYERS: GROSS MARGIN [$M]



Ranking based on 2022 "Gross Margin %" which is "Gross Margin to Revenue Ratio" or "Gross Margin/Revenue"

The charts are ranked by 2022 Gross Margin % in decreasing order from left (1st) to right (30th).

2022 2021 2020 2019 2018

YOLE Intelligence

TOP 10

ASE (w/ SPIL & w/o USI): $ 4.4B, $ 4.0B, $ 2.8B, $ 2.1B, $ 2.0B
Amkor: $ 1.3B, $ 1.2B, $ 901M, $ 649M, $ 711M
JCET Group: $834M, $ 868M, $ 617M, $ 309M, $ 412M
Powertech Technology: $ 565M, $ 696M, $ 535M, $ 421M, $ 459M
Tongfu Microelectronics: $432M, $ 422M, $ 252M, $ 180M, $ 158M
King Yuan Electronics: $ 425M, $ 374M, $ 283M, $ 233M, $ 178M
China Resources Microelectronics: $364M, $ 486M, $ 285M, $ 184M, $ 225M

TOP 11-20

Tianshui Huatian Microelectronics: $283M, $ 445M, $ 271M, $ 155M, $ 160M
Chipbond Technology: $ 255M, $ 316M, $ 224M, $ 225M, $ 177M
Ardentec: $ 193M, $ 160M, $ 121M, $ 83M, $ 93M
Sigurd Microelectronics: $ 180M, $ 178M, $ 128M, $ 69M, $ 88M
Tong Hsing: $ 163M, $ 167M, $ 103M, $ 53M, $ 62M
ChipMOS Technologies: $ 160M, $ 262M, $ 179M, $ 130M, $ 112M
Greatek Elec: $ 138M, $ 226M, $ 136M, $ 93M, $ 107M
Hana Micron: $119M, $ 131M, $ 88M, $ 76M, $ 86M
Carsem: $ 115M, $ 82M, $ 76M, $ 56M, $ 60M
Inari: $101M, $ 102M, $ 77M, $ 62M, $ 90M

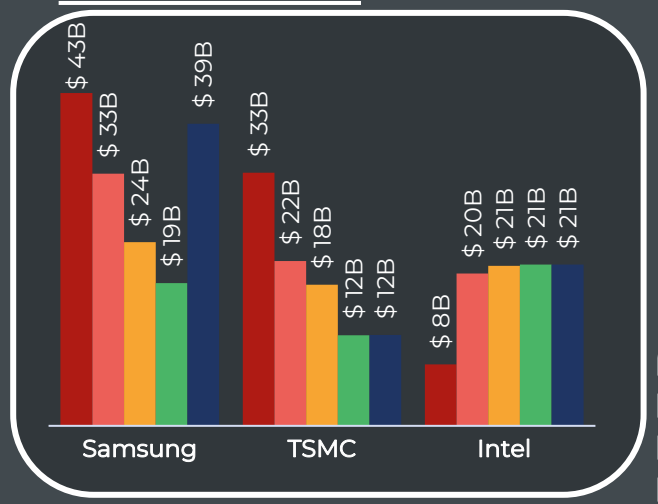
TOP 21-30

Nepes Corporation: $98M, $ 77M, $ 55M, $ 91M, $ 54M
OSE: $ 82M, $ 106M, $ 25M, $ 55M, $ 15M
Unisem Berhad: $ 76M, $ 249M, $ 215M, $ 25M, $ 87M
LB Semicon Inc: $72M, $ 62M, $ 67M, $ 65M, $ 41M
Formosa Advanced Technologies: $71M, $ 75M, $ 67M, $ 55M, $ 55M
AOI Electronics: $ 64M, $ 65M, $ 61M, $ 68M, $ 86M
SFA semicon: $ 63M, $ 69M, $ 47M, $ 43M, $ 42M
Walton Advanced Engineering: $ 27M, $ 16M, $ 7M, $ 29M
Forehope: $23M, $ 103M, $ 23M, $ 8M
Lingsen Precision Industries: $17M, $ 53M, $ 11M, $ 6M

YOLE Intelligence

IDM and foundry | OSATs

TOP 30 PLAYERS: NET MARGIN [$M]

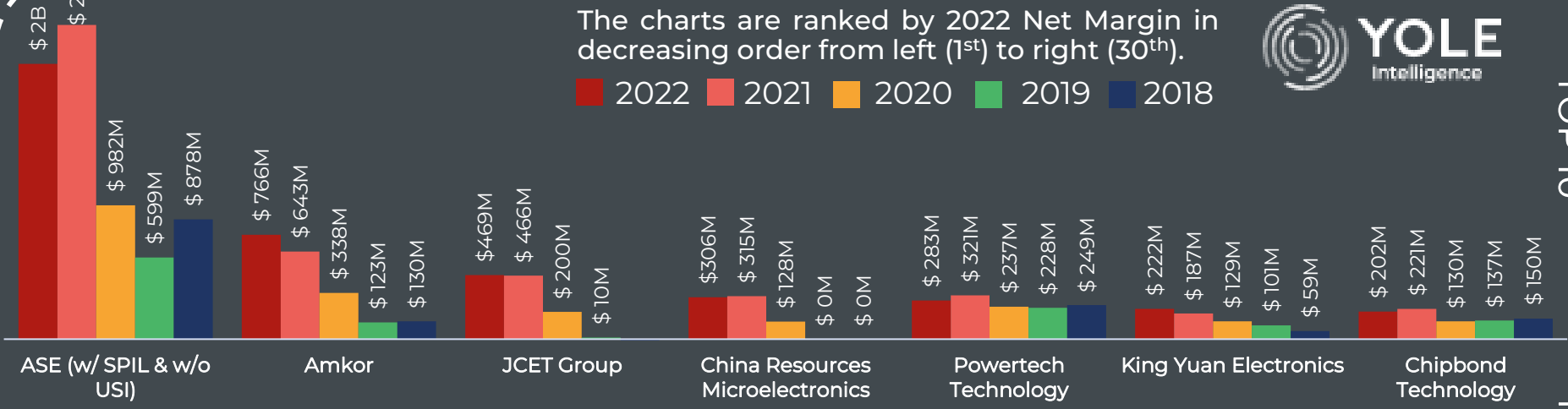


The charts are ranked by 2022 Net Margin in decreasing order from left (1st) to right (30th).

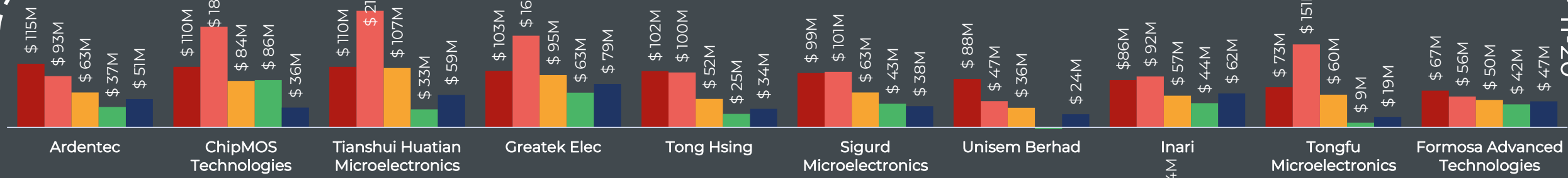
2022 2021 2020 2019 2018

YOLE Intelligence

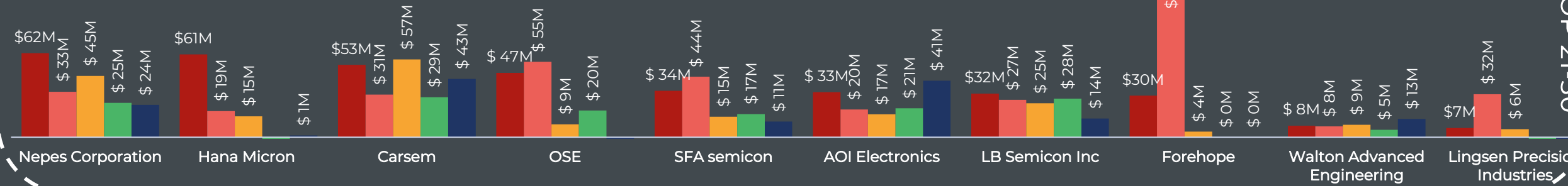
TOP 10



TOP 11-20



TOP 21-30



YOLE Intelligence

IDM and foundry | OSATs

OSAT MARKET ECOSYSTEM

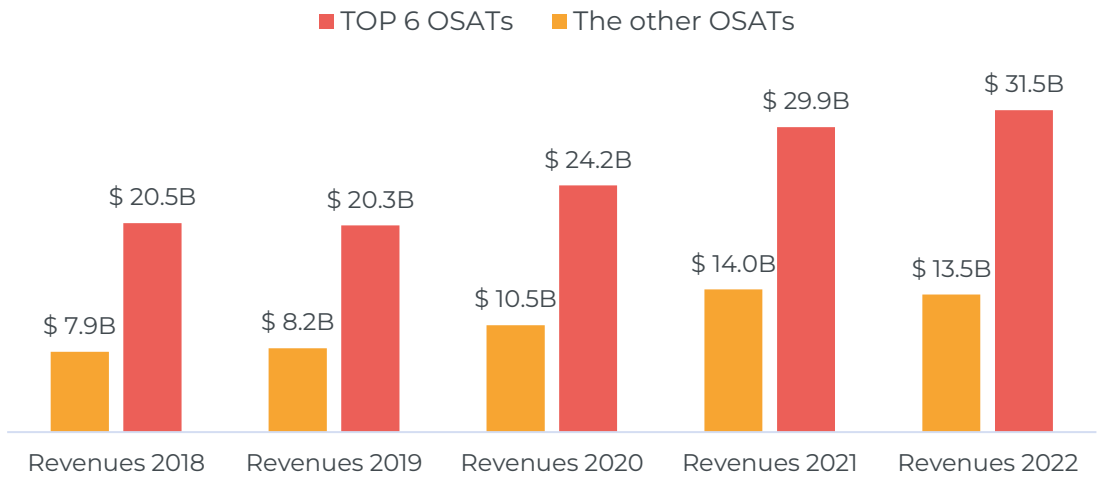
Focus on the TOP 6 OSATs

TOP SIX OSATs

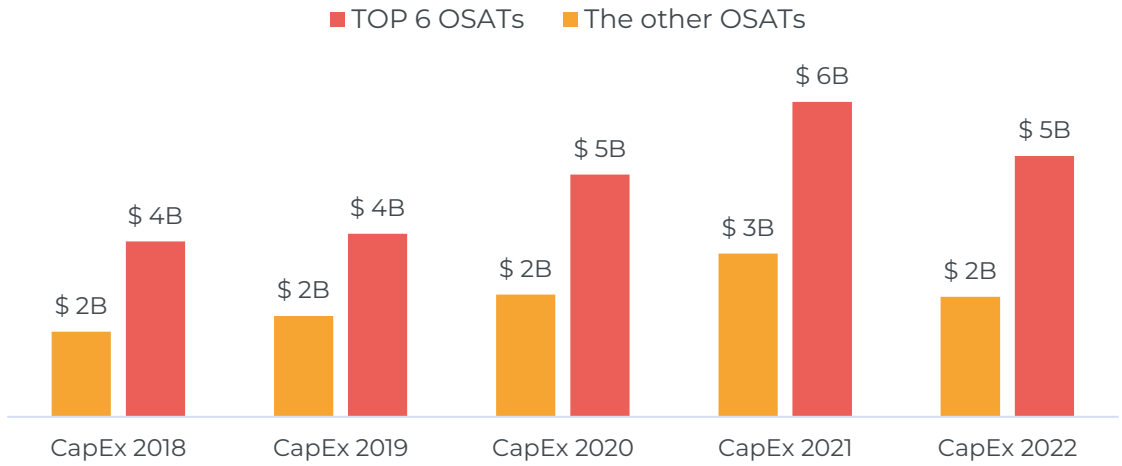
The other OSATs*

- The packaging market is strongly dominated by big players and the top six OSATs have taken 70% of the OSAT market in 2022.
- These are the companies not only investing the most but also investing more in advanced packaging technologies.
- Apart from IDMs and foundries, these are the companies with potential to penetrate the high-end performance packaging segment.
- On one side, the top OSATs hold strong collaborations with IDMs and foundries and as these collaborations get stronger, OSATs will slowing enter the high-end packaging supply chain.
- One another hand, top OSATs are allocating most of their CapEx to develop their own advanced packaging solutions. Hence, we expect their revenues to be increasingly driven by the advanced packaging segment.

Revenue Comparison: TOP 6 OSATs vs. The other OSATs



CapEx Comparison: TOP 6 OSATs vs. The other OSATs



* Non-exhaustive list of OSATs

KEY FINANCIAL SUMMARY

#1 player by different financial parameters

Relative R&D Expenditure (% of revenue)

12% nexes

Relative CapEx (% of revenue)

53% FHEC

*FHEC: Forehope Electronic (China)

Net Margin (%)

54% tsmc

Revenue [$M]

$11 950M (with SPIL)

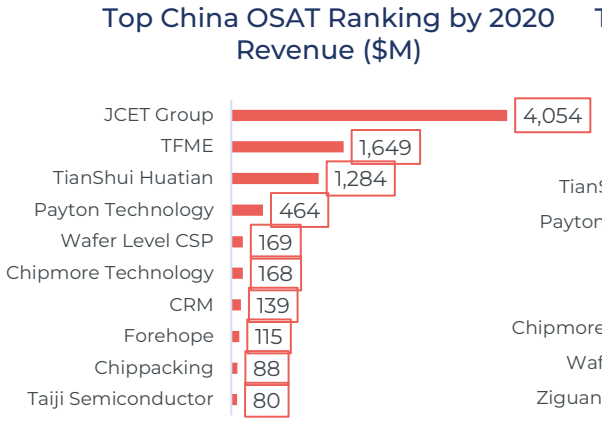
Revenue YoY growth Rate (%)

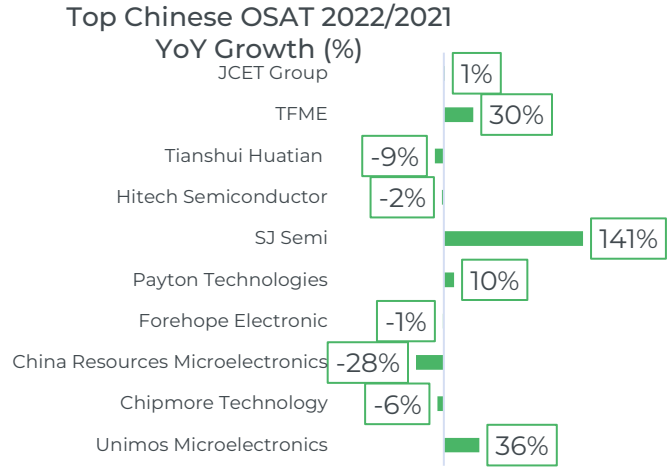
SJSEMI SJ Semiconductor (Jiangyin) Corporation 141%

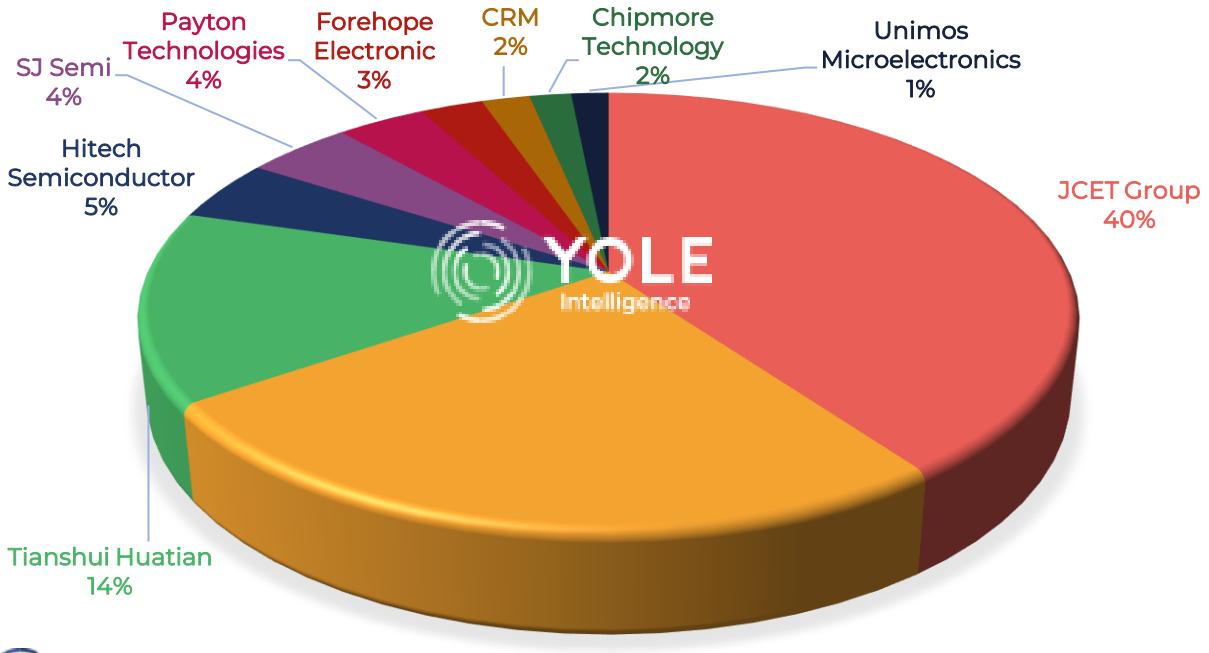
Gross Margin %

tsmc 59.6%

TOP 10 CHINESE OSATS' REVENUES



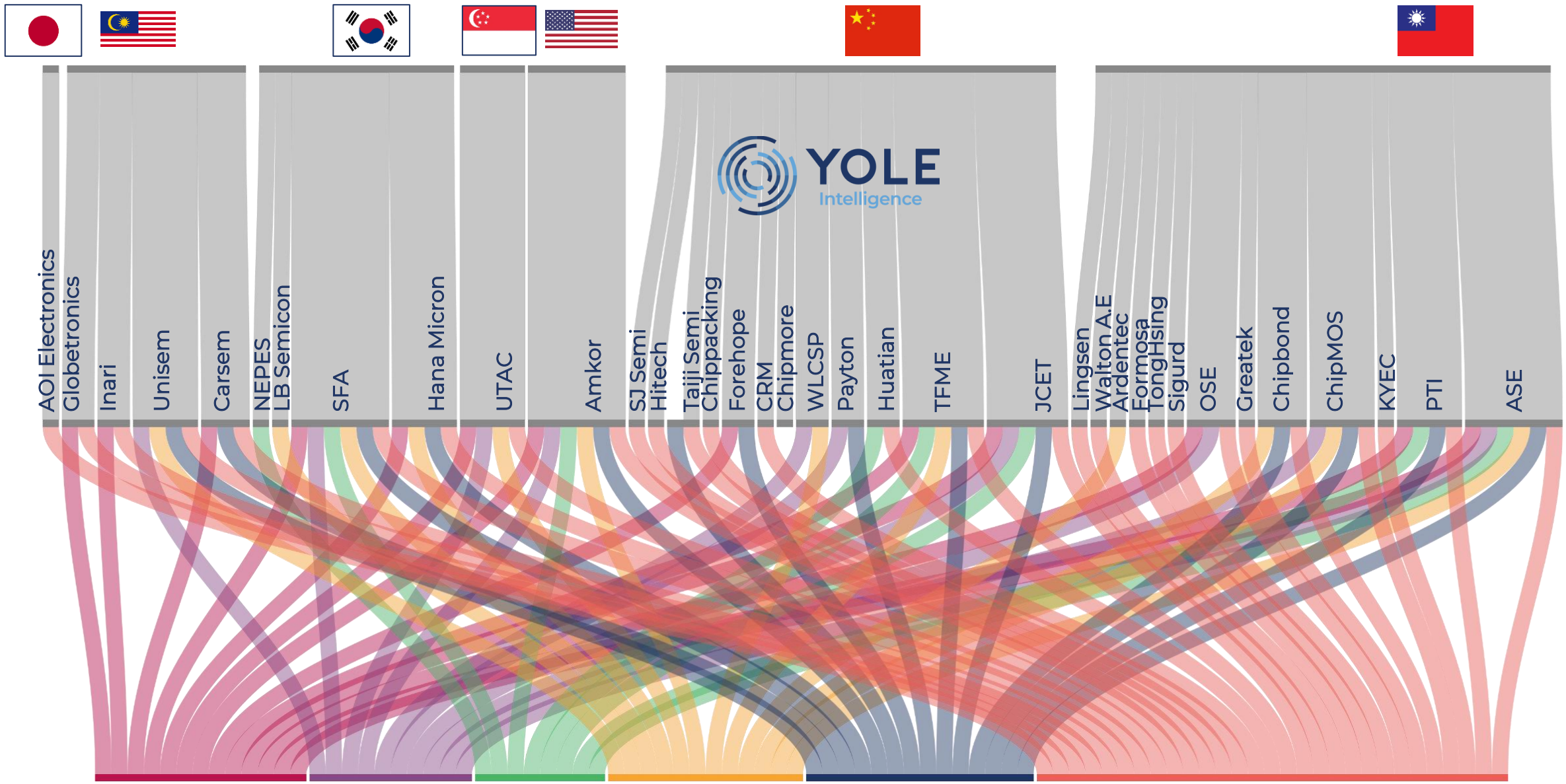




- China's Top 3 OSATs contributed with 79% of China's top 10 OSATs' revenue in 2022 (less than 2021 : 85%).
- China's Top 3 OSATs are in the world's top 10 OSATs (JCET, TFME, and Tianshui Huatian) .
- China's Top 10 OSATs have total revenue of $12B, YoY growth of 8%.
- Most of China's OSATs show significant YoY growth, especially SJ Semi with 141 % growth.
- A total of 8 out of the 10 OSATs are concentrated at the Yangtze River Delta.

TOP CHINESE OSATS' TECHNOLOGIES

GLOBAL'S OSAT OVERVIEW BY PRODUCTS



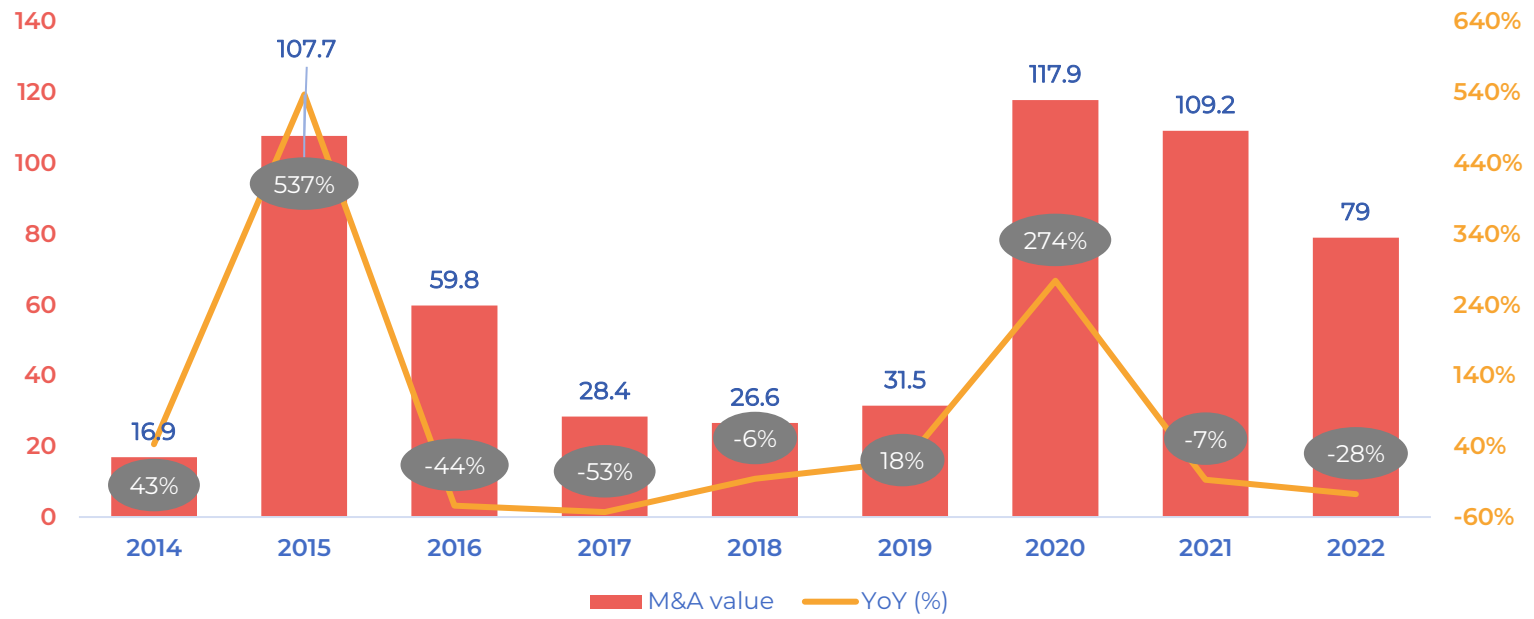
MERGERS & ACQUISITIONS

SEMICONDUCTOR M&A

Semiconductor M&As to the value of $79B were agreed in 2022, 28% lower than in 2021. Semiconductor Packaging M&As were worth ~$7B in 2022, only ~ 8.8% of the total.

Semiconductor M&A value reached almost $79B in 2022. Semiconductor key consolidation drivers included the desire to supplement organic growth, revenue & cost synergies to drive growth, economies of scale given cutting-edge R&D costs, the desire to add complementary products and expand portfolios, and market exposure. Another critical factor was the need to ensure the supply chain amid the current constraints. Of the total semiconductor M&As, Semiconductor Packaging M&A was worth ~$7B in 2022, representing only approximately 8.8% of the total.

Of the ~$7B semiconductor packaging M&A value in 2022, the bulk was from the Atotech acquisition by MKS Instruments, valued at $4.4B.



SELECTED SEMICONDUCTOR PACKAGING M&A IN 2022

MKS Instruments has completed its acquisition of Atotech for $4.4 billion. Atotech provides process chemicals, equipment, software, and services for printed circuit boards, semiconductor IC packaging, and surface finishing. The acquisition will position MKS to accelerate roadmaps for future generations of advanced electronics devices and optimize interconnects	$ 4.4B	mks Atotech
Lam Research has completed the acquisition of SEMSYSCO, a provider of wet processing semiconductor equipment. With the addition of SEMSYSCO, Lam gains capabilities in advanced packaging, ideal for leading-edge logic chips and chiplet-based solutions for high-performance computing (HPC), artificial intelligence (AI), and other data-intensive application	$ 1B	SEMSYSCO
APACT is expanding its semiconductor back-end process business by acquiring ATsemicon's packaging business. The total investment in these mergers and acquisitions is around 200 billion KRW for $153 M, as companies seek to expand their business to system semiconductors following memory semiconductors	$ 153M	ATSEMICON
Nordson Corporation has agreed to acquire CyberOptics, a leading developer and manufacturer of high-precision 3D optical sensing solutions. The acquisition is aimed at strengthening Nordson's Test and Inspection platform and expanding its product offerings in the semiconductor and electronics industries. The all-cash transaction is valued at approximately $380 million.	$ 380M	CYBEROPTICS Technology Leadership. Global Solutions.
DOOSAN TESNA acquired EngiOn, for $780 M, to expand its packaging business area and promote synergy. The acquisition aims to increase DOOSAN TESNA's presence in the high-tech packaging business, which is growing in importance.	$ 780M	EngiOn
Doosan Group acquired Tesna ($353 M) to diversify its business and secure new growth drivers. Tesna specializes in testing non-memory semiconductors, and its acquisition will help Doosan become competitive in AI, VR, AR, big data, 5G, electric vehicles, and autonomous driving.	$ 353M	TESNA

RECENT M&A / INVESTMENTS BY KEY OSATS

Company		Activities
ASE Technology Holding Parent company of ASE Inc. | SPIL | USI	ASE Technology Holding Co., Ltd. Advanced Semiconductor Engineering, Inc. SPIL USI	• ASE is currently qualifying its 300x300mm panel-level fan-out with expected HVM in 2022/2023, with plans to ramp up its production with M-Series products soon. • USI announced a new plant to be set up in Vietnam at a cost of $42 million, which will start commercial production in 2022 to further increase its AiP capacity in line with increased demand for TWS earbuds. • ASE obtained flip-chip packaging orders for Qualcomm's flagship 5G SoC Snapdragon 888 and the X60 5G modem. • ASE announced a new business unit to be set up at its plant in Kaohsiung, southern Taiwan, to handle Sony's automotive CIS orders, which will mainly be fulfilled with its BGA packaging technology. • SPIL's subsidiary Siliconware Electronics (Fujian) was sold to Shenzhen Hiwin System for $142.2 million. 2022-2023 (NEW) • ASE's 2022 total CapEx reached $1.7B, and the company announced that in 2022 the total investment would probably reach the same number as the previous year. For the full year 2022, machinery and equipment CapEx reached $1.7B, with $918M spent on packaging, $574M on testing, and $154M on EMS and US$51 million in interconnect materials operations. • ASE announced expansion plan of its factory site in Malaysia with $300 M investment. It is scheduled to complete in 2025. • ASE will also expand its production capacity in Singapore and South Korea according to customer needs • About 25% of ASE's system and packaging capacity to be moved outside Chinese mainland • SPIL started operating the new Changhua plant (Taiwan) in Jan 2023. • SPIL announced building a new plant at Yunlin County with an investment of $3.3 B. • ASE announced it would complete its Chungli, Taiwan factory site expansion in 3Q24.

RECENT M&A / INVESTMENTS BY KEY OSATS

Company		Activities
JCET Group		• JCET raised $777.4 million in paid-in capital through private placements looking to enhance its presence in the 5G device back-end field by enhancing its SiP, QFN, BGA, and other related technology capabilities. The new funds will also help JCET expand its production capacity and optimize its financial structure. 2022 – 2023 (NEW) • JCET started the construction of a new plant in Jiangyin city (China) with a dedicated investment of $14.5 B. • JSI (JCET Semiconductor Integration, Shaoxing) started small volume production in Q3 2022, with a monthly production capacity of 5K wafers by the end of 2022. JSI plans an annual production capacity of 480K wafers of eWLB and XDFOI products. In January 2023, JCET's XDFOI™ entered mass production • With a total CapEx of $548M in 2022, significant growth of its system-in-package business and FCCSP and FCBGA product lines was achieved. • JCET will open a facility in Tokyo (Japan), covering both sales and operations, as the company is willing to invest heavily in the Japanese market.
Powertech Technology (PTI)		• In 2018, PTI started constructing a new plant at Hsinchu, Northern Taiwan, to focus on FOPLP. An estimated NT$50 billion ($1.63B) will be poured into the new plant, which should be ready for full production by the end of 2022. • Capex $607 M with 10.1 % growth • PTI's CapEx is projected to total $1.6B in five years. Its capacity will be expanded to 50k panels/month once its new plant in northern Taiwan is online by 2021. The new fab will focus on heterogeneous integration. 2022 – 2023 (NEW) • PTI plans to invest 40% less on Capex; around $332.8 M, compared to 2022. • In adaptation with macroeconomic trends, PTI halted capacity expansions. • PTI's Chinese plants returned to full capacity operation state after the China's Covid lockdowns.

RECENT M&A / INVESTMENTS BY KEY OSATS

Company		Activities
Tongfu Microelectronics Formerly known as Nantong Fujitsu		• TFME, through its acquisition of an 85% stake in AMD's Penang, Malaysia, and Suzhou, China facilities, enabled the company to win part of the orders for AMD's new 7nm processors and gained new technologies, packages, and market segments. • TFME to raise up to CNY 4 billion (~US$660M) in private share placements to fund projects, replenish capital and repay bank loans. • Tongfu borrowed $35 million from China Development Bank in February 2020 for work and production resumption after the pandemic and capacity increase. • Tongfu established a CPU and GPU packaging and testing center with a total investment of $94M, allowing it to obtain new customers. Tongfu also announced plans to invest ~$176M in an intelligent packaging and testing center for automotive products. 2022 - 2023 (NEW) • AMD-TF Microelectronics JV announced plans to expand its manufacturing facility in Penang, with nearly RM2 billion (around $445 M) of capital investment, bringing total capacity area to over 2.3 Million square feat. • Tongfu Microelectronics launched a new plant project in Suzhou, China. Flip chip, multi-chip packaging and other advanced packaging and testing technologies will be used to provide integrated packaging and testing solutions for high-performance computing integrated circuits. • The Tongfu Tongke D2 product line project has reportedly begun installing equipment in March 2022, laying the foundation for the construction of high-end packaging product lines. It is expected to achieve mass production in June 2022.
Amkor		• The key growth drivers are 5G deployments, HPC, IoT wearables, and automotive electronics. Also, Amkor Korea (K5) plans to start offering HVM fan-out packages. 2022- 2023 (NEW) • Amkor's Capex was $908.3 M in 2022 and it is expected to drop to $800M in 2023. • Amkor and GlobalFoundries formed a strategic partnership to create first at-scale semiconductor supply chain outside of Asia in Europe. GF will transfer its 300mm Bump and Sort lines from Dresden to Amkor's Portugal operations, enabling a comprehensive EU/US supply chain from semiconductor wafer production to OSAT services. • Amkor is investing $1.6B in a new plant in Bac Ninh, Vietnam. The construction will begin around the first quarter of 2022 and is scheduled to start pilot production in the second half of 2023.

RECENT M&A / INVESTMENTS BY KEY OSATS

Company		Activities
Sigurd Microelectronics		• Sigurd Microelectronics and Winstek Semiconductor both plan to expand production capacity to satisfy the growing demand for 5G-related chips and blockchain ASICs. • Sigurd Microelectronics budgeted $113M of CapEx for 2023 to replace old equipment and expand production capacity to respond to robust demand mainly for 5 G-related chips, automotive sector and power management IC sector. • Sigurd increased its number of testing machines to 1,300 units to meet testing demand for handset SoCs, networking chips, power management ICs, and automotive chips. 2022 – 2023 (NEW) • Sigurd Microelectronics, to keep 2023 capex plans flexible due to client inventory issues • Sigurd Microelectronics approved to invest NT$4bn in smart production lines • In 2021, Sigurd Microelectronics announced plans to wholly acquire fellow IC assembly and test service company UTAC Taiwan for NT$4.62 billion ($165 million).
Nepes		• In February 2020, Nepes built an independent management system by spinning off its fan-out packaging business as a subsidiary, Nepes Laweh. • BNW Investment, IBK's PE arm, and the PE unit of Korea Development Bank (KDB) have completed a transaction to buy new shares and convertible notes issued by Nepes Laweh. Each of the three investors invested 40 billion won in Nepes Laweh, in a deal that valued the entity at 280 billion won. 2022 - 2023 (NEW) • Nepes expands mass production with advanced packaging technologies and introduces next-generation packaging markets using fan-out technology. • Nepes suffers from steep drop-in factory operation rates due to global chip downturn • Nepes' CapEx is estimated at $187M for 2023, and its FO WLP should experience increased growth with the adoption of autonomous driving & IoT platforms in automotive. • In 2021, Nepes moved into volume production of 600 x 600mm^2 fan-out panel-level packaging technology, using Deca's M-Series adaptive patterning technology. Nepes is expected to offer high-density packaging solutions with initial production focused on single and multi-die packages for smartphones. In the future, the target is heterogeneous integration of chiplets using Deca's Gen 2 technology.

RECENT M&A / INVESTMENTS BY KEY OSATS

Company		Activities
ChipMOS		• ChipMOS enjoyed strong demand for testing DRAM and flash memory chips. It has over 500 sets of testing equipment running at nearly 100% capacity. • Based on its NT$15.1 billion investment project approval by the Taiwanese government, ChipMOS will expand its LCD driver IC and memory packaging capacities at its plants in Southern Taiwan Science Park (STSP) and Hsinchu Science Park (HSP) to extend its capacity lead over Chinese peers. • ChipMOS experienced a ramping up of demand for display driver ICs in the second half of 2020, thanks to the launch of new 5G phones and a surge in demand for large-size display applications. 2022 - 2023 (NEW) • Capex $152.9 M • ChipMOS Technologies to invest NT$12.5 billion in Taiwan to expand capacity and presence in the DRAM chip business. Investment will help explore new opportunities in 5G and automotive fields. • ChipMOS will tend to be conservative about its capital spending in 2023, likely reaching about 15% of 2022's total revenue. • The firm has maintained its capacity utilization at a high level due to growing back-end demand for DRAM and NOR flash chips. • ChipMOS Technologies is expanding its production capacity for memory chips by 30-40% to meet strong demand from major memory module makers in Taiwan.
Chipbond		• In 2019, Chipbond put on hold its 5G PA (power amplifier) packaging capacity expansion due mainly to the uncertainties associated with the US trade ban on China's Huawei. • Taiwan-based Chang Wah Electromaterials, a distributor of packaging materials and equipment, will buy a 9.9% stake in Chipbond for $117.27M. • Chipbond is forming an alliance with Orient Semiconductor Electronics to combine their wire bonding capacity and metal bumping capacity to serve vendors of diverse 5G, communication, and power management ICs with better back-end services. 2022 - 2023 (NEW) • Chibond's CapEx was $119.6 M in 2022. • Chipbond is also planning to invest in additional high-end testing equipment, mainly from Advantest, to satisfy the growing demand for OLED DDIs in 2022. • United Microelectronics Corp. (UMC) took a 9% stake in Chipbond Technology Corp. The companies came to this agreement in order to offer their customers added value in the display driver market.

RECENT M&A / INVESTMENTS BY KEY OSATS

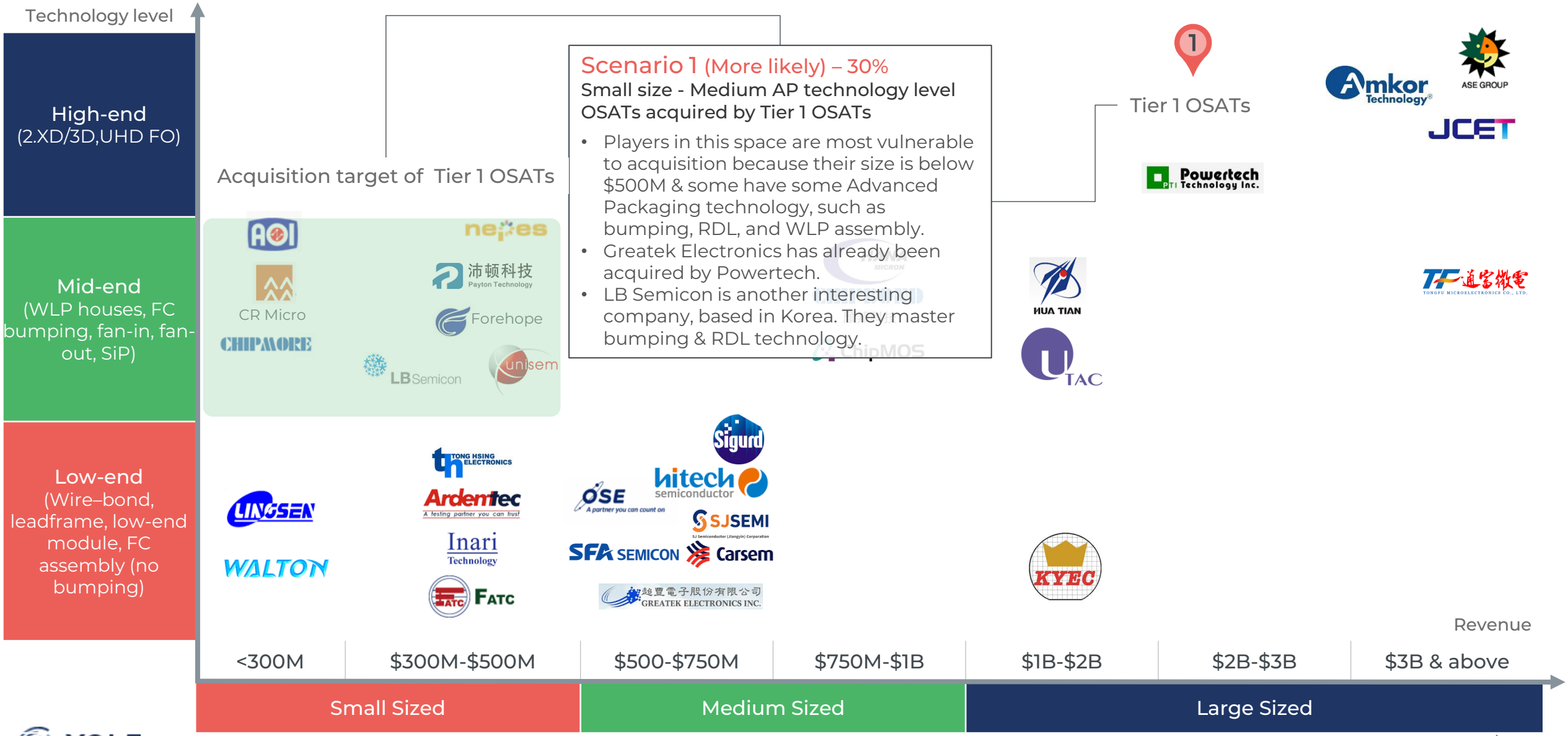
Company		Activities
Ardentec		• Ardentec is expected to reduce CapEx in 2019 due to a more cautious short-term outlook for communication chips due to continued inventory adjustments of mobile SoC, uncertainties created by the US-China trade disputes, and weakening memory chip demand. • Ardentec revealed a NT$1 billion ($31.8M) investment for factory site expansion. The new capacity is designed for advanced wafer-level packaging, and testing for radio-frequency IC and other components for use in emerging applications arising from 5G, AIoT, and automotive electronics. 2022 - 2023 (NEW) • Capex $199.7 M reduced from $217.7M for 2023. • Ardentec doubles capacity with new Singapore plant, highlighting commitment to long-term growth • Ardentec is also investing in new factory site in northern Taiwan, slated for production in 2024 • Ardentec to invest $672.8M in new Taiwan plant, set to expand production capacity by 30%. • Equipment move into the new facility was expected to occur in 2021.
KYEC		• KYEC and Keystone were among the back-end partners of Huawei's HiSilicon and have seen a reduction in orders. However, both enjoyed a ramp-up in demand for 5G and Wi-Fi 6-related chip solutions. • KYEC and Sigurd have both stepped up high-end test equipment purchases to provide more capacity support for MediaTek's mobile chips. 2022 – 2023 (NEW) • KYEC plans to allocate NT$7.05 billion for capex in 2023, down significantly from the previous year, but will make adjustments based on customer demand and market conditions. • Ardentec, to keep 2023 capex plans flexible due to client inventory issues • KYEC plans to invest less in CapEx in 2023 by investing $227M to expand production capacity.

RECENT M&A / INVESTMENTS BY KEY OSATS

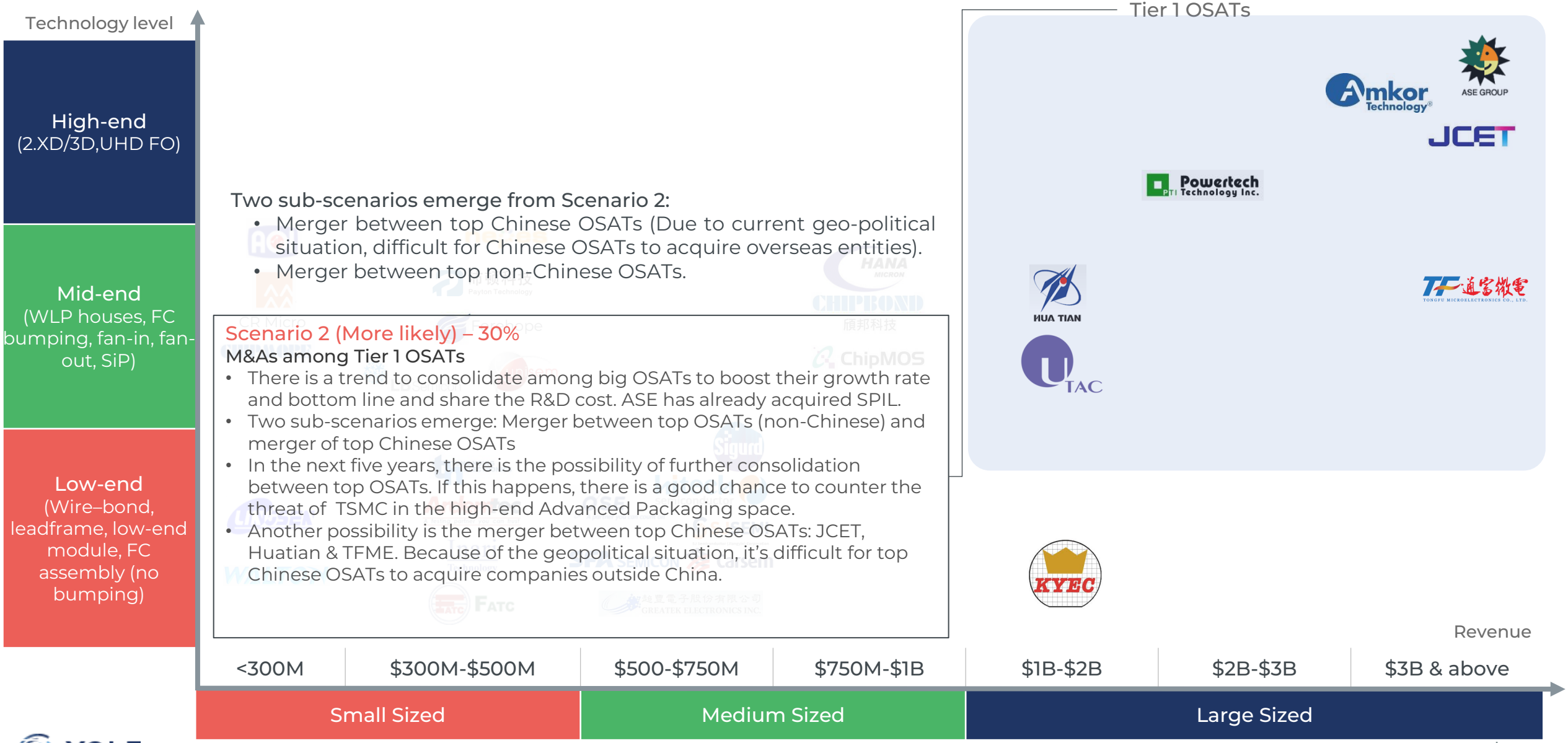
Company		Activities
LB Semiconductor	LB Semicon	• LB Semicon built a new facility starting in September 2020 at its plant in Ansung, worth 58.1 billion won. The new testing facility is designed to handle Samsung's order to test CMOS image sensors and application processors, and it began testing the initial stock of chips in March 2021. This will allow LB Semicon to handle a greater volume of image sensors and APs. 2022 - 2023 (NEW) • YES sold VertaCure XP G2 system to LB Semicon in Korea. The VertaCure system supports wafer-level chip scale packaging (WLCSP) with flexibility for both 200mm and 300mm wafers. • In September 2021, LB Semicon announced an additional investment of 95.5 billion won into non-memory test facilities. • With the construction of its new facility now complete, in 2022, the company is ramping up operations with expected capacity utilization rates of 70%. • LB Semicon expects a healthy 2022, with its test portfolio diversification, capacity expansion, and DDI business growth. • LB Semicon is reportedly planning to enter the FOWLP business in 2023.

M&A SCENARIOS FOR OSATS IN 2023-2028 (1/5)

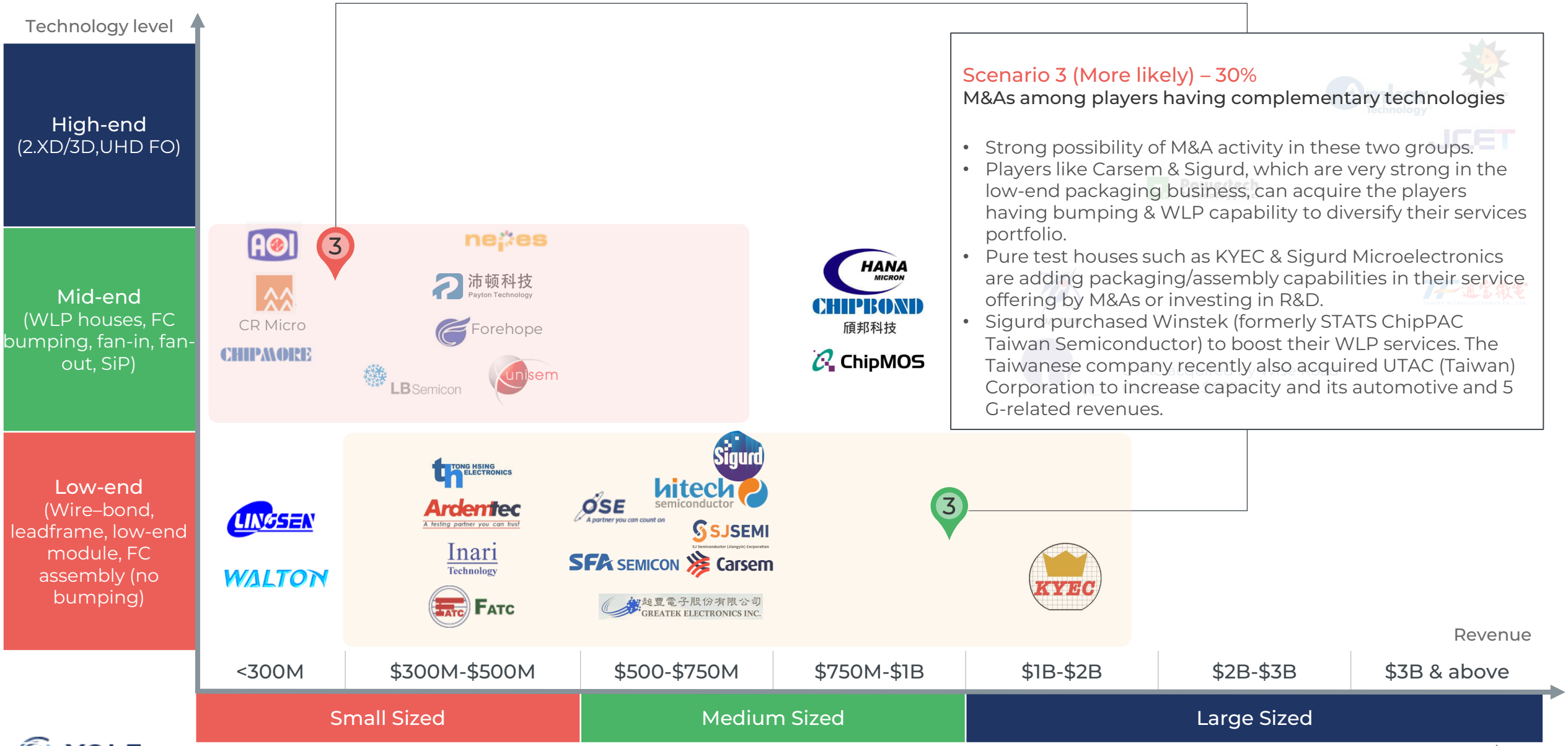
M&A SCENARIOS FOR OSATS IN 2023-2028 (2/5)



M&A SCENARIOS FOR OSATS IN 2023-2028 (3/5)



M&A SCENARIOS FOR OSATS IN 2023-2028 (4/5)

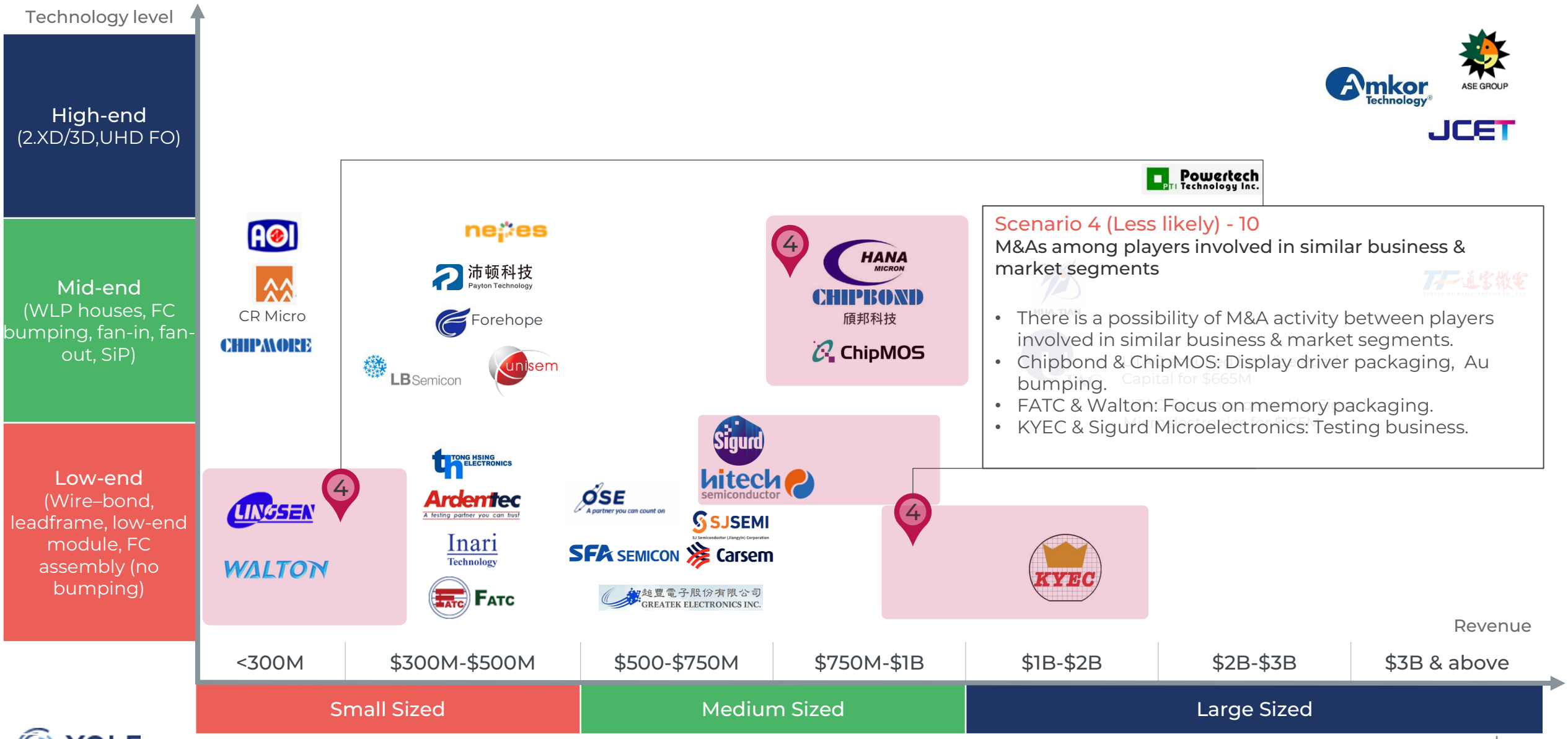


Scenario 3 (More likely) – 30%

M&As among players having complementary technologies

- Strong possibility of M&A activity in these two groups.
- Players like Carsem & Sigurd, which are very strong in the low-end packaging business, can acquire the players having bumping & WLP capability to diversify their services portfolio.
- Pure test houses such as KYEC & Sigurd Microelectronics are adding packaging/assembly capabilities in their service offering by M&As or investing in R&D.
- Sigurd purchased Winstek (formerly STATS ChipPAC Taiwan Semiconductor) to boost their WLP services. The Taiwanese company recently also acquired UTAC (Taiwan) Corporation to increase capacity and its automotive and 5 G-related revenues.

M&A SCENARIOS FOR OSATS IN 2023-2028 (5/5)



OSAT M&A SUMMARY

The semiconductor industry has seen a significant slowdown in M&A activity in 2022, with deal activity dropping by 28% compared to 2021 and 2020. This decline in M&A activity can be attributed to various factors, including geopolitical constraints, changes in packaging trends, and a shift in priorities among corporations.

One major factor contributing to the slowdown in M&A activity in the semiconductor industry is the ongoing geopolitical tensions between the United States and China. The US government's restrictions on technology transfers to Chinese companies and the increasing regulatory scrutiny of foreign investment have made it difficult for Chinese firms to acquire assets in the US semiconductor industry. Additionally, Chinese companies are increasingly looking inward and investing in their domestic semiconductor industry, leading to a decrease in Chinese investment in the global semiconductor market.

Based on their revenue size and technology level, we propose various M&A scenarios among OSATs:

Scenario 1 (More likely)	Scenario 2 (More likely)	Scenario 3 (More likely)	Scenario 4 (Less likely)
Small size - Medium AP technology level OSATs acquired by Tier 1 OSATs	**M&As among Tier 1 OSATs**	**M&As among players having complementary technologies**	**M&As among players involved in similar business & market segments**
• Players in this space are most vulnerable to acquisition because their size is below $500M & some have some Advanced Packaging technology, such as bumping, RDL, and WLP assembly. • Greatek Electronics has already been acquired by Powertech. • LB Semicon is another good company, based in Korea. They have bumping & RDL technology.	• There is a trend to consolidate among big OSATs to boost their growth rate and bottom line and share the R&D cost. ASE has already acquired SPIL. • Two sub-scenarios emerge: Merger between top OSATs (non-Chinese) and merger of top Chinese OSATs • Another possibility is the merger between top Chinese OSATs: JCET, Huatian & TFME. Because of the geopolitical situation, it's difficult for top Chinese OSATs to acquire companies outside China.	• Players like Carsem & Sigurd, which are very strong in the low-end packaging business, can acquire the players having bumping & WLP capability to diversify their services portfolio. • Pure test houses such as KYEC & Sigurd Microelectronics are adding packaging/assembly capabilities in their service offerings by M&As or investing in R&D. • Sigurd purchased Winstek (formerly STATS ChipPAC Taiwan Semiconductor) to boost their WLP services. The Taiwanese company recently also acquired UTAC (Taiwan) Corporation to increase capacity and its automotive and 5 G-related revenues.	• There is a possibility of M&A activity between players involved in similar business & market segments. • Chipbond & ChipMOS: Display driver packaging, Au bumping. • FATC & Walton: Focus is memory packaging. • KYEC & Sigurd Microelectronics: Testing business.

SEMICONDUCTOR M&A SUMMARY

OSAT M&A (Possible Scenario)

Scenario 1	OSAT Tier 1	+	OSAT Small or Medium	Increase the revenue and reduce competition (More likely)
Scenario 2	OSAT Tier 1	+	OSAT Tier 1	Boost growth rate and share R&D cost (More likely)
Scenario 3	OSAT Tech A	+	OSAT Tech B	Strengthen Technology Competency (More likely)
Scenario 4	OSAT Market A	+	OSAT Market A	Strengthen Business and Market Position (More likely)

Semiconductor M&A (Possible Scenario)

Scenario 5	OSAT	+	Substrate House			Secure substrate allocation to meet customer demand
Scenario 6	Foundry/IDM	+	OSAT	+	Substrate House	Secure the main supply chain business for the best turnaround time and cost optimization

* Chip shortage and substrate shortage are critical. Long term strategy with M&A will strengthen a company position in the market.

CONCLUSIONS

CONCLUSION (1/2)

The World Bank projects a minor growth in GDP of **2.7% in 2023**. The semiconductor market is expected to witness a drop of 6% from $594 B in 2022 to $550 B in 2023. In the future, the market will re-adjust and bypass the 2022 revenues.

The current global economic factors, including the world political conflicts and geopolitical crisis, have been causing supply chain disruption since the 2nd half of 2022. Their impact is expected to reach its maximum in 2023, causing economic slowdown, before starting to show recovery signs before the end of the year. Despite all the economic headwinds influencing the semiconductor sector, including lower demand for several consumer electronic end systems, the overall forecast remains strong at the long term, particularly for cutting-edge technology. The semiconductor industry is predicted to decline during 2023, marking it as an uncommon year.

In addition to its importance, the semiconductor industry is gaining a strategic geopolitical role within governments around the globe, which is reflected by the unprecedented investment amounts worldwide, from companies or governments. A total of more than $800B has been announced, in different countries, to secure the domestic semiconductor supply chain from any future disruptions or shortages at the mid and long-terms. The total IC packaging market was **$95B** in 2022. Advanced Packaging (AP) was worth **$44.3B** and is expected to grow at a CAGR2022-2028 of **10%** to **$78B** in 2028. At the same time, the traditional packaging market will grow at a CAGR2022-2028 of **4.15%**, and the total packaging market will grow at a CAGR 2022-2028 of **7.10%**, to **$64.7B** and **$143.3B**, respectively.

In 2022, the AP market represented **47%** of the total IC packaging market. Due to strong momentum in the AP market driven by megatrends, the share of AP in the total semiconductor market is increasing continuously and will reach about 51% of the market by 2025. The highest AP market share belongs to the flip-chip platform (which includes FCBGA and FCCSP), with **51%** of the market in 2022. The **highest revenue** CAGR 2022-2028 is expected from ED (in the laminate substrate), 2.5D/3D, and Flip-chip, at **30%**, **18.7%**, and **9%**, respectively, as high-volume products further penetrate the market.

By segment, Mobile & Consumer constituted **70%** of the total AP market in 2022. It will grow at a **7%** CAGR and constitute **61%** of the AP market by 2028. Telecom & Infrastructure is the **fastest-growing** segment **(~17%)** by revenue and will account for **27%** of the AP market in 2028. Automotive & Transportation will account for **9%**, and other segments, including medical, industrial, and aerospace/defense, will account for **3%** of the market.

In terms of 300mm eq wafers, traditional packaging still dominates with almost **71%** of the total market in 2022. However, AP is continuously increasing its share of wafers, and its market share will increase from **~29%** in 2022 to **37%** in 2028. AP wafer production was **~43M** 12" wafers in 2022, and it is expected to grow at **~ 10%** CAGR $_{2022\text{-}2028}$ to reach **~76M** wafers in 2028. Concerning units, traditional packaging accounts for more than **94%**. Advanced Packaging volumes will increase at **~6%** CAGR2022-2028 to **101B** units in 2028. WLCSP packages will remain dominant.

CONCLUSION (2/2)

In the semiconductor industry, Advanced Packaging is becoming increasingly important due to its ability to enhance the value of semiconductor products and its role as a transistor scaling alternative. This is achieved by adding more functionality, improving performance, and lowering costs. One of the key trends in this area is the adoption of a chiplet approach, which is being propelled by the advancement of heterogeneous integration.

To stay ahead of the game, large IDMs and foundries are turning to heterogeneous integration using Advanced Packaging technology to complement their front-end efforts. This trend has been facilitated by the development of wafer processing tools, such as lithography for RDL interposers used in heterogeneous integration. Industry giants like TSMC, Intel, and Samsung continue to lead the way in Advanced Packaging as a result.

One of the key areas of focus in Advanced Packaging is increasing interconnect density through the use of a 3D packaging platform. Commonly adopted solutions include Cu RDLs and Cu vias as interconnects. The industry is moving towards sub-micron pad pitches, which is driving the introduction of hybrid bonding technology. This allows for metal-metal and oxide-oxide face-to-face stacking with <10 µm bump pitch.

The changing business environment is also having an impact on the supply chain at various levels. As a result, Advanced Packaging is transitioning from a package substrate platform to Silicon, which has enabled companies like TSMC, Intel, and Samsung to make serious investments in the AP segment. These players have emerged as the key innovators in the field.

Seven players, including three IDMs (Intel, Samsung, and Sony), a foundry (TSMC), and the top three global OSATs (ASE, Amkor, JCET), process over 81% of Advanced Packaging wafers. OSATs accounted for 65.1% of the AP wafers in 2022 while Foundry and IDM accounted for 12.3% and 22.6% respectively.

In the last years, top packaging players have invested over one-third of the market value in CapEx. In 2022, Advanced Packaging CapEx reach $18B, which is ~12% higher than the previous year and represents almost 40% of the total Advanced Packaging revenue for the year. In 2023, the CapEx is expected to drop, as the big players are cutting expenses and the overall slowdown of the semiconductor industry.

In 2022, ASE retained its Mega-OSAT position, outranking its peers with $21B revenue as SPIL and USI revenue grew. This shielded ASE from a YoY reduction compared to other OSATs, such as Amkor and JCET (ASE's revenue without USI was about $11.9B in 2022). Total OSAT revenue increased to ~$60B from $43 B in 2021. ASE generated 24% of the total OSAT revenue, and ASE, Amkor, and JCET combined generated 52.4% of total OSAT revenue. OSAT R&D spending in 2022 dropped slightly to $1.57B from $1.96B in 2021. OSAT CapEx spending in 2022 also dropped to $8.7B from approximately $9.74B in 2021. Taiwan continues to be the leader as its share of the OSAT market is the biggest, around 43% in 2022 as more Chinese companies entered the Top 30 ranking. In 2022, the OSATs ranking included 7 Chinese players - Payton, Forehope, TFME, SJ semi, Hitech Semi, Huatian & JCET.

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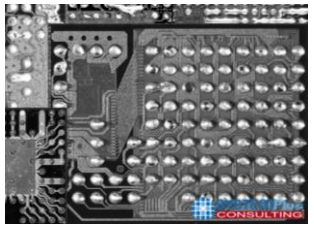
High-End Performance Packaging: 3D/2.5D Integration 2023

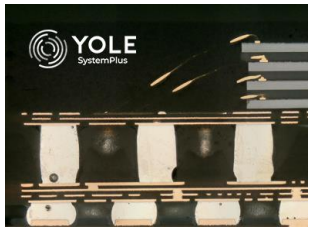
Fan-Out WLP and PLP Applications and Technologies 2023

NVIDIA A100 Ampere GPU

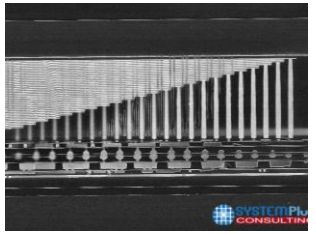


Fan-Out Packaging Processes Comparison 2020

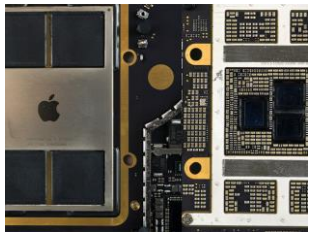
Memory Packaging 2023



Intel Foveros 3D Packaging Technology



YMTC's 3D-NAND Flash Memory



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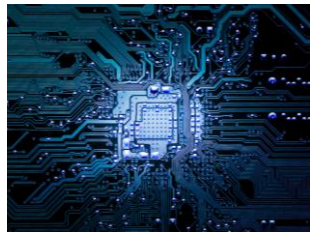
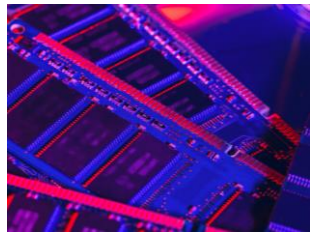


Advanced Packaging Market Monitor



DRAM Market Monitor

NAND Market Monitor

Processor Market Monitor

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- Semiconductor Packaging
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190 custom projects per year

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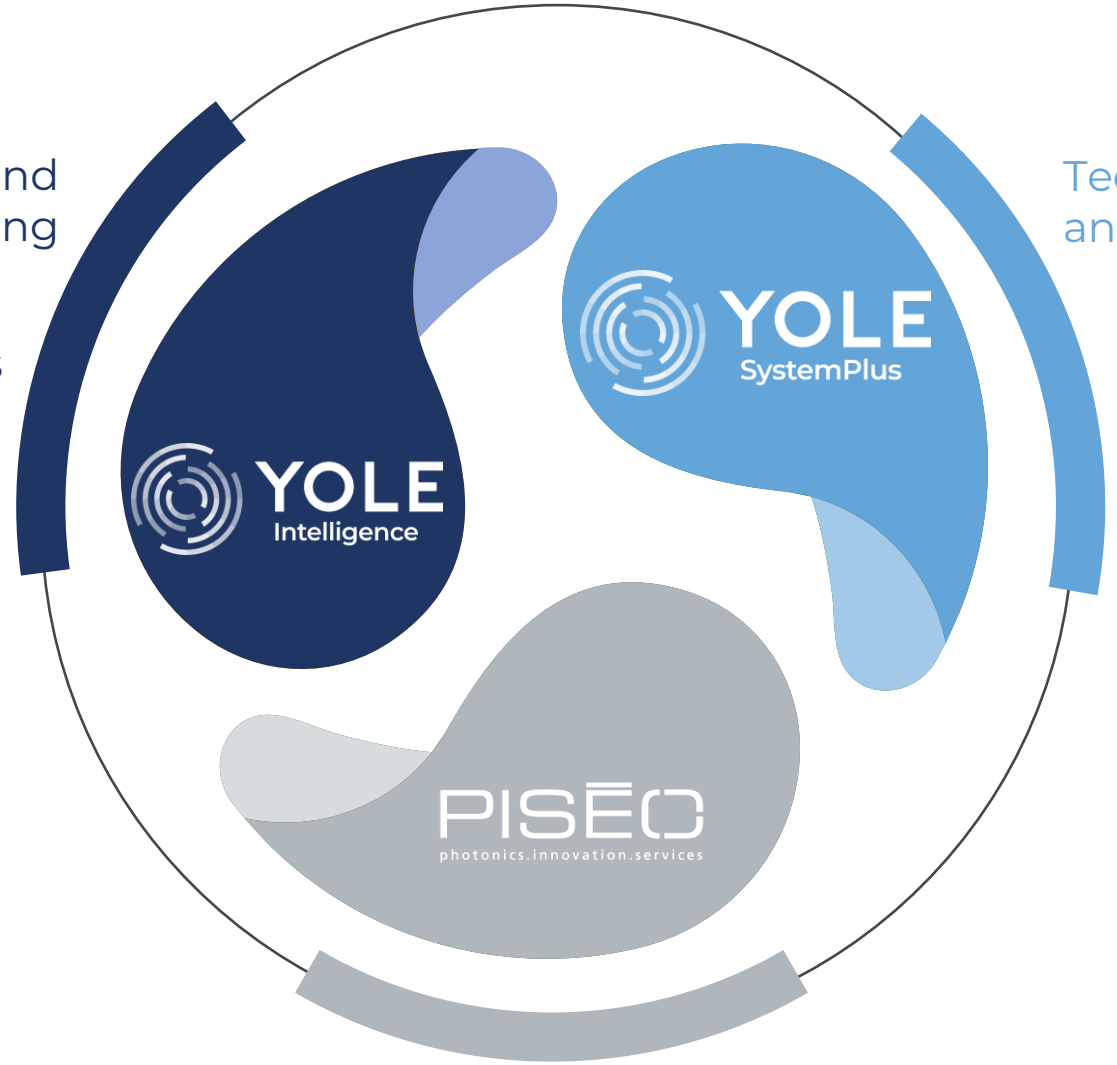

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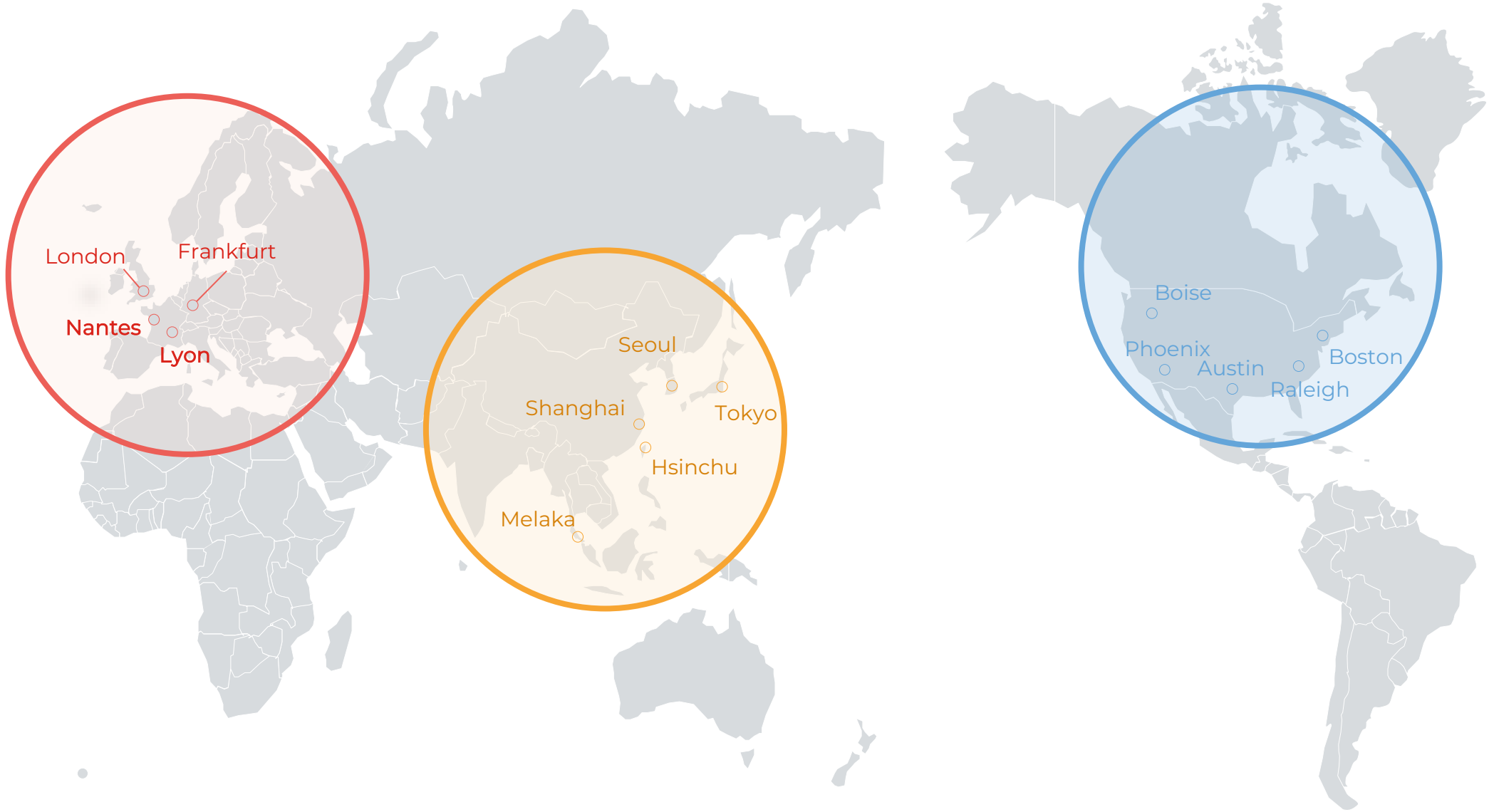

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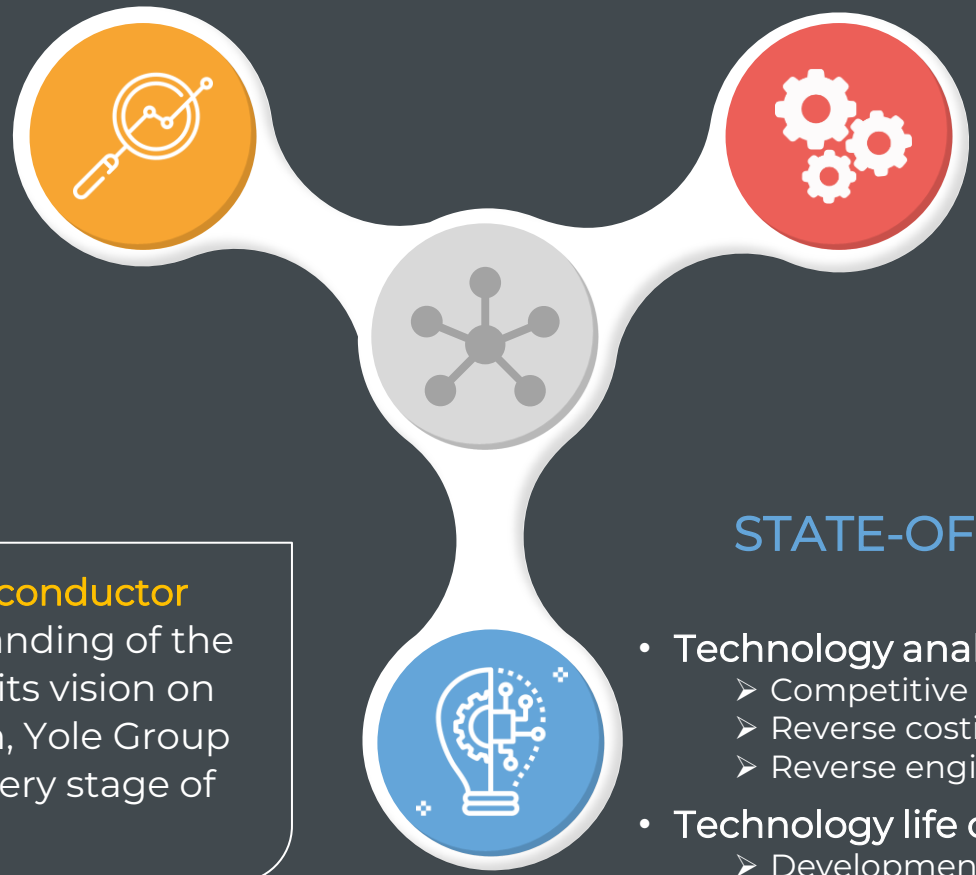

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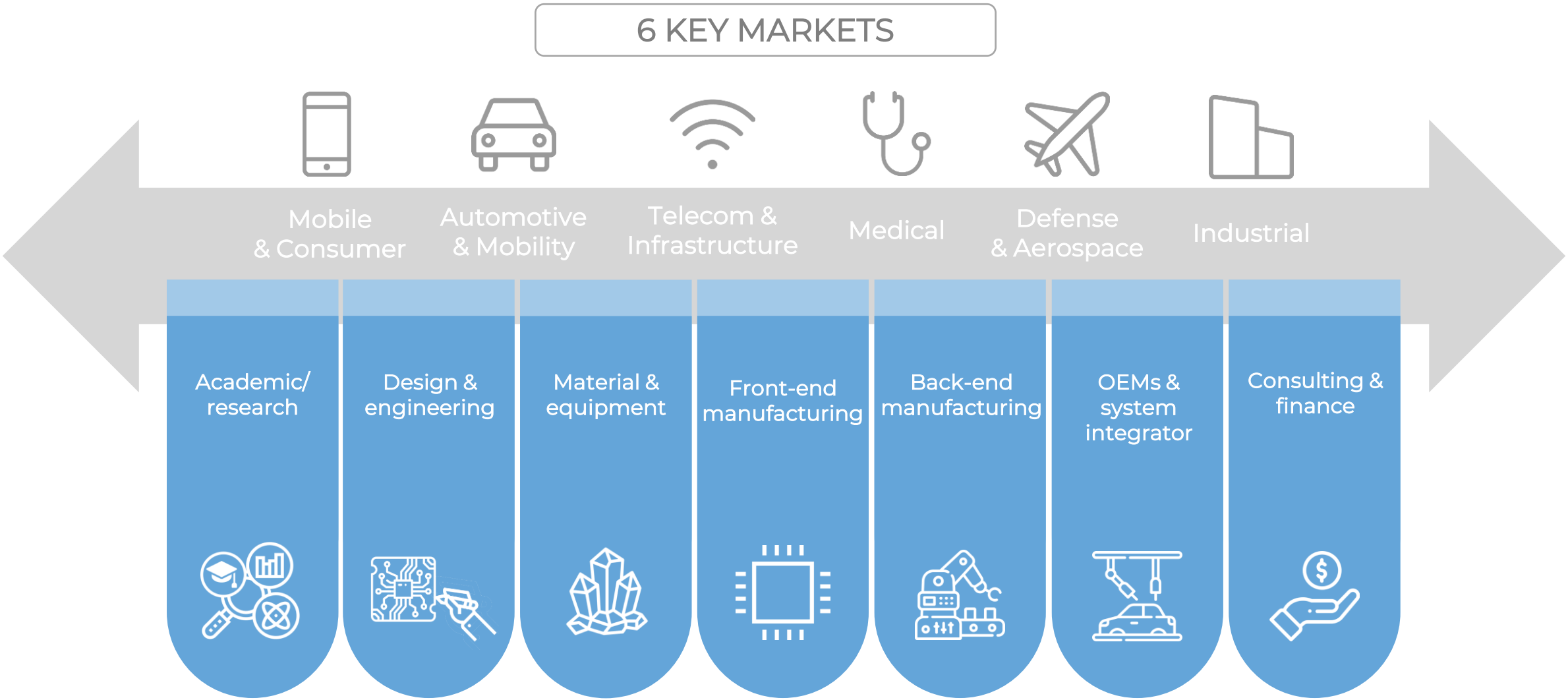

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