TSV-based Stacked Silicon Capacitor with Embedded Package Platform

Kyojin Hwang
S.LSI Business,
Samsung Electronics Co. Ltd.
Hwaseong-si, Korea
kyojin.hwang@samng.com

Jisoo Hwang
S.LSI Business,
Samsung Electronics Co. Ltd.
Hwaseong-si, Korea
js10.hwang@samsung.com

Woobin Jung
S.LSI Business,
Samsung Electronics Co. Ltd.
Hwaseong-si, Korea
woobin.jung@samsung.com

Heeseok Lee
S.LSI Business,
Samsung Electronics Co. Ltd.
Hwaseong-si, Korea
hees.lee@samsung.com

Junso Pak
S.LSI Business,
Samsung Electronics Co. Ltd.
Hwaseong-si, Korea
junso.pak@samsung.com

Junghwa Kim
S.LSI Business,
Samsung Electronics Co. Ltd.
Hwaseong-si, Korea
Junghwas.kim@samsung.com

***Abstract*— In this paper, authors propose a new type of trough silicon via (TSV)-based stacked silicon capacitor (SSC). This SSC is designed by stacking two silicon capacitor wafers, thereby connecting wafers with Cu to Cu bonding. As a result of wafer stack, SSC can have two times of capacitance and lower ESL characteristics when compared with the same size of Conventional Silicon Capacitor (CSC). Furthermore, if we stack n wafers additionally, we will be able to acquire N times of capacitance. In addition, when we adopt this SSC as an embedded capacitor (eCAP) in a cored substrate system on a chip (SoC) package, SSC has the advantage of reducing the distance from bumps to a decoupling capacitor. And we can design two sided bump SSC that allows the area of bottom side of the SSC can be used for power delivery network (PDN) design. Thus, shortcut PDN design through TSV is possible. As a result, the inductance generated in the package is reduced and the Power Integrity (PI) characteristic is improved.**

Through this work, we provide a comparative study of SSC, conventional silicon capacitor, and conventional ceramic capacitor with a cored substrate platform for premium mobile SoC products. Impedance characteristics and voltage drop simulation experimental results are provided in this paper. Through electrical performance simulation analysis, the effect of the new technology in this work on the performance improvement of the SoC package will be demonstrated through performance measurement evaluation finally.

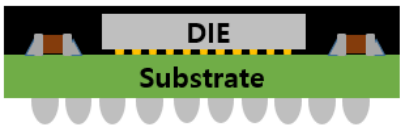
Keywords— Stacked silicon capacitor, TSV silicon capacitor, embedded silicon capacitor

I. Introduction

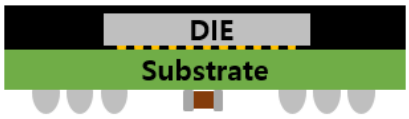
Due to the multifunctionality and high performance of electronic devices. There is a high demand to integrate various intellectual property (IP) to implement additional functions in an system on a chip (SoC). To make this possible, more advanced IP design and packaging technology that does not degrade IP performance is required. It is important to design a robust power delivery network (PDN) to ensure IP performance, and a solution for impedance reduction is required. In order to design an optimized PDN for high-performance SoC, it is necessary to lower the impedance peak of the system PDN by connecting a capacitor with high capacitance and low ESL performance [1]-[7].

To design a stable PDN, the effective way is to connect the decoupling capacitors inside the SoC package. In mobile SoC platform, decoupling capacitors have been applied in various ways such as die side capacitor (DSC) , land side capacitor (LSC) , embedded capacitor (eCAP) as Fig. 1.

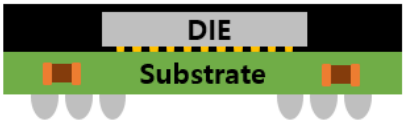
Among them, eCAP is efficient with the shortest power delivery distance between the die bumps and a decoupling capacitor, and is more reliable. So in this paper, simulation was performed by using eCAP to the embedded substrate platform.



DSC (Die side capacitor).



LSC (Land side capacitor).



eCAP (Embedded capacitor).

Fig. 1. DSC versus LSC versus eCAP.

In the mobile SoC package design, low inductance ceramic capacitor (LICC) has been used because it has lower ESL than multilayer ceramic capacitor (MLCC). Furthermore, silicon

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capacitors with lower ESL and better impedance characteristics are being applied [8]-[19].

Multi-Layer Ceramic Capacitor (MLCC).

Low Inductance Ceramic Capacitor (LICC).

Fig. 2. MLCC and LICC.

In this paper, we propose SSC that can improve the performance of the SoC package. We also describe the advantage of the SSC through the comparative electrical simulation results of LICC, CSC, and SSC

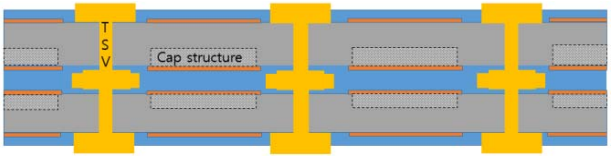
II. TSV-Based Stacked Silicon Capacitor(SSC)

In this chapter, SSC's design concept, advantages, and process of SSC are explained.

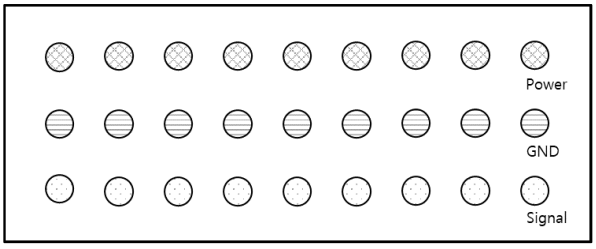
A. Design concept of SSC

SSC is a concept in which the upper and lower bumps are connected to power, ground, and signal lines through Trough Silicon Via (TSV) as described in Fig. 3 [20]. By Cu-to-Cu bonding of the same silicon capacitor wafer, SSC can get twice the capacitance compared to the same size of CSC, and SSC can get a lower ESL value because the number of bumps is doubled.

Conventional Silicon capacitor (CSC).



Vertical View of SSC.



Top and Bottom View of SSC.

Fig. 3. Concept of SSC.

B. Advantage of SSC

- Ultra Low ESL

  LICC has a lower ESL than general MLCC, and the ESL value is about 60 pH. But in case of a CSC with many bumps, the ESL value is lower than ESL value of LICC . CSC's ESL value is below 10 pH.

  Furthermore, for SSC, since the number of bumps are doubled, a lower ESL specification is possible.

- Higher Capacitance

  Since SSC is manufactured by stacking two wafers of CSC, it can acquire twice the capacitance when compared with the same size of CSC. When n wafers are stacked, N times of capacitance is acquired. Therefore, if package does not have any height restriction, SSC can acquire a larger capacitance as same size of CSC.

- Optimized PDN design

  When using a CSC for cored substrate embedded platform, only single sided mounting is available as described in Fig 4. And in this design, it is impossible to directly connect the power and signal at the bottom of the CSC, As there is no direct signal line to the bottom of the CSC, the signal line returns to the outside of the CSC, and thereby increases the length of the signal line.

  However, when SSC is applied, both top and bottom sides can be connected, and PDN shortcut design through SSC's TSV is possible as described in Fig 5. It can improve PDN design optimization and improves PI characteristic.

  Therefore, if a package is designed using SSC, the package design efficiency will be increased.

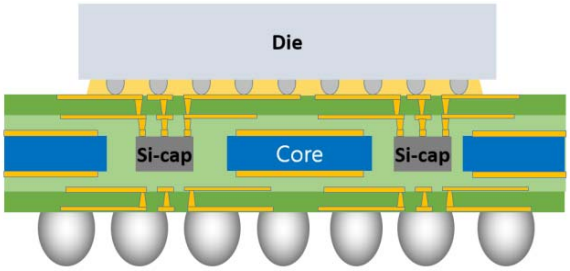


Fig. 4. Embedded Platform with Conventional Silicon Capacitor.

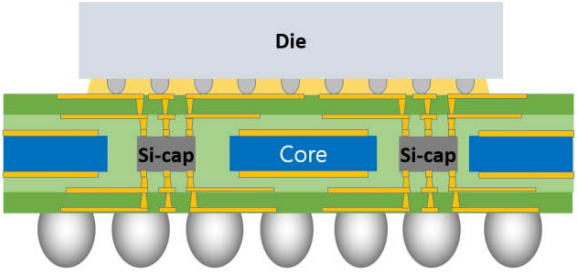


Fig. 5. Embedded Platform with SSC.

C. *Process Flow of SSC*

This chapter explains the manufacturing process concept of SSC.

At first, during fabrication process of wafer, a silicon capacitor wafer including TSV and capacitor structure is fabricated. After manufacturing same silicon capacitor wafers, stack them and connect two wafers with Cu-to Cu bonding. After bonding, grind the upper surface and form Cu bumps. After grinding the upper surface of the wafer, turn the wafer and perform the same process on the other side as in Fig.6's step d3.

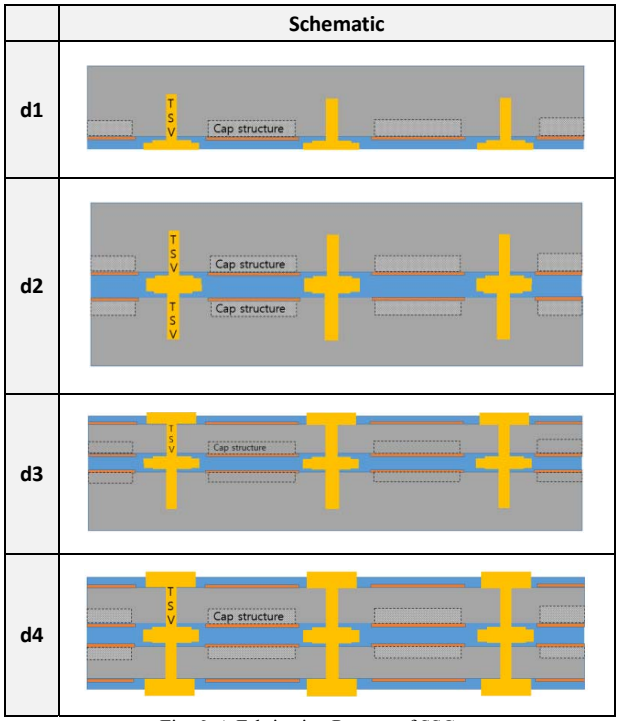


Fig. 6. A Fabrication Process of SSC.

III. Embedding Process Of SSC

This chapter explains how SSCs are mounted on multi-layer substrates and Redistribution Layer (RDL)-based Fan-out Package (FoPKG) as described in Fig. 7 and Fig. 8 [15].

A. *Multilayered Organic Substrate with SSC*

At first, SSC is placed on the temporary carrier, on which the substrate core is also attached before placing discrete capacitor. The substrate core should be perforated. The capacitor, which will be embedded, should be placed in the hole of the substrate core. In step-e2, the perforation of the substrate core with embedded SSC is molded or encapsulated, thereby SSC and the substrate core become mechanically single. Via holes are made on the top sides and bottom sides of electrical terminals in SSC. In general, laser drilling process is used for making via holes. Metal-filled vertical interconnects called by via are fabricated for electrical connection between SSC and metal layers of organic substrate. After fabricating a few more additional metal layers, the substrate will be used for SoC package assembly as described in Step e5. The multi-layered organic substrate is employed to make SoC package, whose PDN has multiple SSCs.

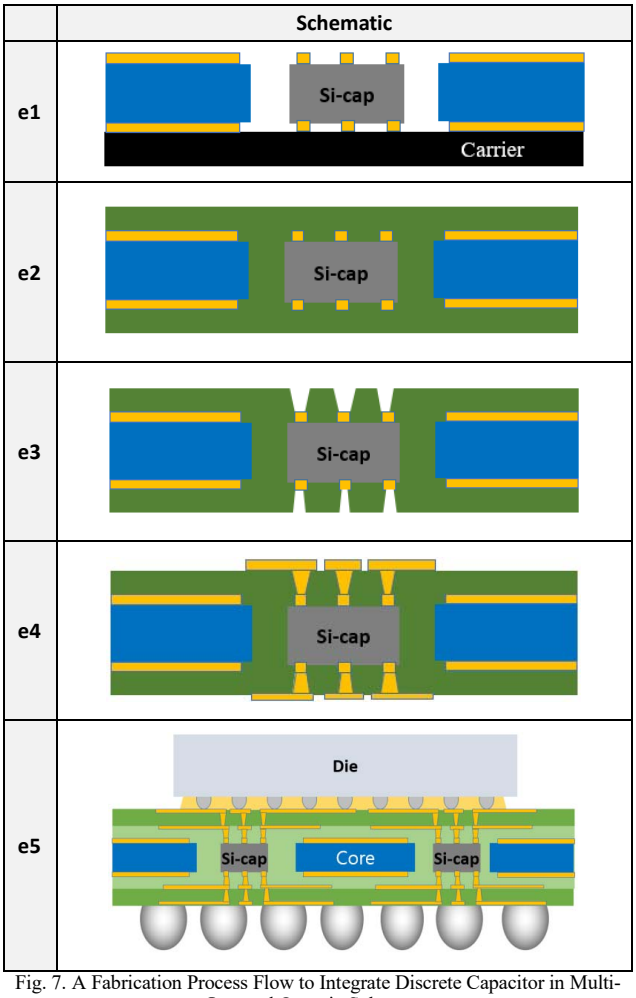


Fig. 7. A Fabrication Process Flow to Integrate Discrete Capacitor in Multi-Layered Organic Substrate.

B. *RDL based FoPKG with SSC*

At first, after SSCs and die are placed on the temporary carrier, the hole of the substrate core is molded, thereby mechanically making the SSCs, die, and the substrate core as a single entity. A dielectric layer is coated on the bottom surface of the molded substrate including SSCs and die. The via holes are drilled on the terminals of SSCs and die to expose the metallic surface of those. The first layer of F-RDL including vias to electrically connect SSC is fabricated. When multiple layers are required, the F-RDL fabrication process shown in step-f4 can be repeated to add more metal layers. After completing F-RDL process, the top side of metallic terminals of SSC is exposed. B-RDL is fabricated, which is almost same to step-f4 and step-f5. Additional package or die can be placed over the Fo-PKG made from step-f1 through step-f7.

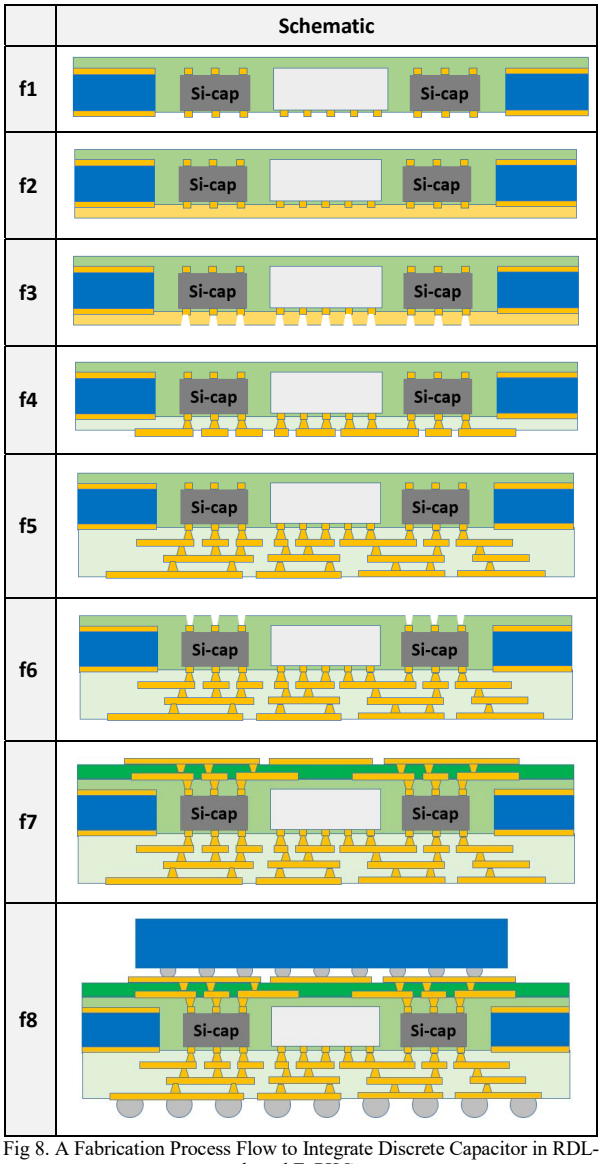


Fig 8. A Fabrication Process Flow to Integrate Discrete Capacitor in RDL-based FoPKG.

IV. Simulation

In this section, the simulation verification was performed by applying the capacitor for each case such as without a capacitor, LICC, CSC, and SSC. Each capacitor was simulated by applying 1 point at a CPU location of premium smartphone SoC. Table I describes the specifications of each capacitor.

TABLE I. Capacitor Specification.

	size(mm)	capacitance
LICC 1pcs	0.5x1.0	220nF
CSC	0.5x1.26	250nF
SSC	0.5x1.26	500nF

A. Impedance Simulation

Impedance behavior of PDN for CPU of a premium smartphone SoC had been simulated. The simulation test performed without a capacitor showed the largest impedance value graph.

In the simulation test performed with a LICC, the peak impedance value could be reduced by more than 30%. But when CSC with better ESL characteristics was applied, the graph improved even more than 50%. Finally, when SSC was applied, we can get the most stable impedance graph as described in Fig. 9.

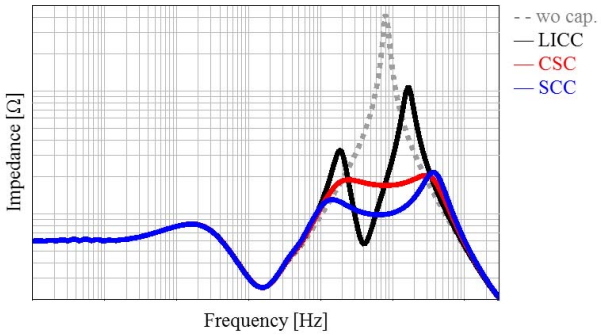


Fig. 9. Impedance Graph by Frequency for each Capacitor Case.

B. Voltage Drop Simulation

The voltage drop simulation was also analyzed for each capacitor case. This experiment also showed a similar trend to the impedance experiment. Without a capacitor, LICC, CSC, SSC trend to reduce voltage drop in the sequence of without a capacitor, LICC, CSC, and SSC.

The voltage drop experiment was conducted in two driving scenarios in the actual premium SoC package, and Fig. 10 is a graph showing how much improvement in voltage drop improvement was achieved in each LICC, CSC, and SSC compared to the case without a capacitor.

As shown as Fig. 10 graph, the effect of CSC was better than that of LICC, and the voltage drop improvement of SSC was improved than that of CSC.

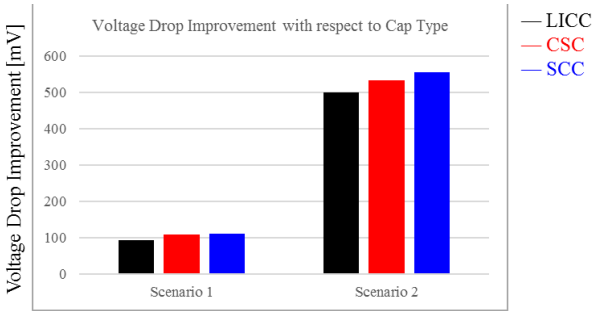


Fig. 10. Voltage Drop Improvement Graph with Respect to Capacitor Type.

Fig. 11 illustrates the voltage drop simulation result graph of each capacitor. In this graph, SSC case is the most stable.

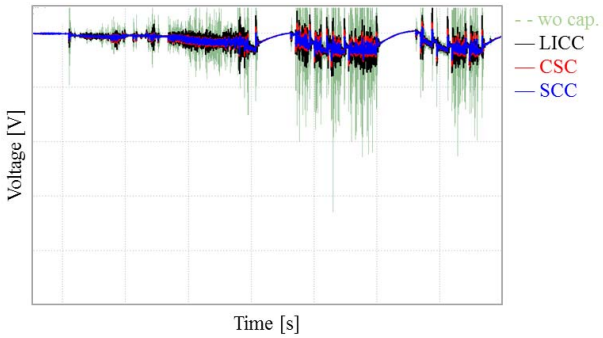


Fig. 11. Voltage Drop Simulation Result of each Capacitor Type. It is difficult to open the x and y-axis values of the graph as confidentiol information.

V. Conclusion & Future Work

With this work, authors presents a new type of SSC. Impedance and voltage drop characteristic are improved by using SSC and also verified through simulations.

Further, authors plan to experiment interconnection by applying SSC to 3D IC or 2.5D package case. N stacked silicon capacitor design for SoC platform will also be experimented.

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