Highly Scalable Vertical Bypass RRAM (VB-RRAM) for 3D V-NAND Memory

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Abstract: We firstly demonstrate highly scalable interface type RRAM based 3D V-NAND memory with WO_x resistivity switching (RS) layer and IGZO selector transistor (Tr). 3D vertical interface type RRAM integrated with IGZO Tr (VB-RRAM), utilizing bypass reading between Tr and RS layer, exhibits low voltage operation (< 5 V), multi-bit (4 bit) capability, and high uniformity of the RS layer while improving the limitations of on/off ratio. Furthermore, with scaling the channel length down to 30 nm, we achieved fast switching speed (~ 50 us), stable endurance (> 10^7 cycles), and low switching energy consumption (5 fJ). Finally, critical V-NAND issues like read disturbance and interface layer were also evaluated.

Introduction: Charge based flash memory faces challenges of scaling such as threshold voltage variability, high operating voltages, and limited endurance [1]. Therefore, non-charge based PCRAM and FeFET for the V-NAND applications have been studied for the alternatives [2,3]. However, they still have obstacles of high-density memory integration due to only single-bit operation, and scalability issues (Table 1). Vertical RRAM has been suggested as a solution for high-density memory owing to the stable endurance, scalability, and low operation voltage [4]. However, in vertical RRAM, there are still drawbacks such as high cost, complex fabrication, and degraded performance [5].

In this study, we introduce the 3D vertical interface type RRAM utilizing bypass reading (VB-RRAM) for V-NAND with a WO_x resistivity switching (RS) layer and IGZO selector transistor (Tr). By scaling the channel length, VB-RRAM shows the excellent memory characteristics such as fast switching speed, stable endurance, and significant reduction of energy consumption. Finally, we demonstrate that our VB-RRAM can be a promising candidate for V-NAND memory applications.

Bypass reading and V-NAND operation: In VB-RRAM, bypass reading between the RS and Tr layer is essential for the V-NAND operation. By controlling the oxygen vacancy (V_o) concentration in the RS layer, we can modulate the resistance of RS layer. This makes a current path through the RS layer when its resistance in the 'on' state is lower than Tr (Fig. 1). Therefore, bypass reading can occur in the V-NAND structure.

For the demonstration of bypass reading between the RS and Tr layer, we integrated the WO_x RS with IGZO Tr in planar structure (Fig. 2(a)). We realized memory characteristics and bypass reading from the IGZO Tr to the WO_x RS depending on each resistance (Fig. 2(b)). Furthermore, the RS layer's analog switching property enabled a multi-bit (> 4 bit) operation with various RS states, achieving an 8 V memory window (MW: Tr V_{th} (-2.5 V) ~ RS V_{reset} (-11 V)) (Fig. 2(c)). To verify the non-volatile characteristics of RS layer, we measured the failure time ($t_{failure}$) with various fail ratio (5 ~ 25 %) depending on the temperature and extracted the activation energy (E_a ~ 0.43 eV) through the Arrhenius plot (Fig. 2(d)) [6]. Based on the E_a, we can obtain 1 year retention at 25 % fail ratio. These results show that our VB-RRAM can be utilized for the high-density memory.

Integration with V-NAND structure: In VB-RRAM, read disturbance should be considered since gate bias affects both the RS and Tr layers as shown in Fig. 3(a). To evaluate the read disturbance issue, we applied V_{pass} on (V_{on}) and V_{pass} off (V_{off}) pulses, which turn on the Tr and turn off the Tr, respectively (Fig. 3(b)). During a 1000 s stress of V_{on} pulse at 0.5 V and V_{off} pulses at -2.5 V, Tr is almost no degradation (blue line) and only 2 % state loss of RS states occurs while the Tr is turned off (red line) (Fig. 3(c)). This result indicates that V_{pass} bias at unselected gate does not significantly affect the RS state, enabling disturbance-free V-NAND operation.

Furthermore, we fabricated 3D vertical VB-RRAM to confirm the feasibility of the V-NAND memory (Fig. 4). For the Tr's selector operation in VB-RRAM, high on current (I_{on}) (~ 10 uA) was observed in vertical IGZO Tr (Fig. 5(a)). It was also found that the thickness of insulating layer plays a crucial role in the I_{on} in IGZO Tr. According to the Fig. 5(b), we utilized the 50 nm SiO_2 insulating layer in base structure considering I_{on}.

Memory characteristics of VB-RRAM: Within the V-NAND structure, we maintained stable memory characteristics at low voltage (< 5 V) through the bypass reading (Fig. 6(a)). We confirmed the bypass reading by observing the transfer curve depending on the RS states. Fig. 6(b) shows that RS states maintain each state and VB-RRAM operates through the bypass reading between the RS and Tr. Furthermore, we achieved high on/off ratio (> 10^5) in VB-RRAM owing to the extremely low off current of IGZO Tr (Fig. 6(c)). This allows us to improve the typically low on/off ratio in conventional RS layers.

Moreover, in VB-RRAM, the memory characteristics are enhanced by scaling the channel length (30 nm) compared to the long channel device (Fig. 7(a)). This result can be related to the interface capacitance (C_{int}) within the gate stack of the VB-RRAM (Fig. 7(b)). As the channel length decreases, C_{int} decreased and the required charge for the program can be reduced [7]. Therefore, the pulse width for 1 V MW is reduced and we can achieve the fast switching speed of 50 us at 30 nm channel length (Fig. 8(a)). Accordingly, we also obtained the low switching energy consumption (~ 5 fJ), which can be further reduced by scaling the channel width (Fig. 8(b)). In addition, VB-RRAM has excellent endurance characteristics (> 10^7 cycles), which is advantageous for V-NAND memory (Fig. 9).

Interface layer issue in VB-RRAM: During programming and erasing, an interface layer (IL) can be formed between the Tr and RS layer due to oxygen migration (Fig. 10(a)). Unlike the planar bypass RRAM, the current path is formed through the IL between RS and Tr layer, which can be an interface resistance (R_{int}) during the bypass reading in VB-RRAM (Fig. 10(b)). This can lead to negative issues like degraded I_{on} and inaccurate reading of RS states because of the voltage drop across the R_{int}. By comparing the I_{on} between planar bypass RRAM and VB-RRAM (Fig. 11(a)), we confirmed that IL is formed as a 100 kΩ R_{int}, which degrades the I_{on} in VB-RRAM (Fig. 11(b)).

To achieve the lower R_{int}, density functional theory (DFT) calculations are employed to understand the physical origin of IL. Our study identifies that IL is originated from the difference in defect formation energy (DFE) of V_o between the Tr and RS layer (Fig. 12). We also confirm that DFE in RS layer increases as oxygen deficiency of WO_x increases. As a result, the oxygens shift from the Tr layer to the RS layer, leading to increase in IL thickness when the V_o in the RS increases during programming. Therefore, to minimize the IL formation, the difference in DFE should be reduced. To reduce the difference in DFE, doping materials that has high DFE such as F, Sn, and Mg can be a solution by increasing the DFE of IGZO Tr [10,11]. Therefore, by doping method, we can suppress the IL formation and reduce the R_{int} for the high I_{on} in VB-RRAM.

Conclusion: We demonstrated a 3D interface type RRAM based V-NAND memory for the high-density memory. Our device exhibits excellent memory characteristics compared to previously V-NAND type memory (Table 2). Based on these results, VB-RRAM can be a promising candidate for replacing the charge-based flash memory in V-NAND applications.

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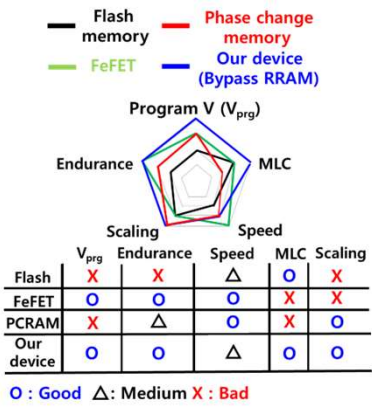
Reference: [1] J. Jang, et al., *VLSI*, 2009. [2] S. Morita, et al., *VLSI*, 2011. [3] F. Mo, et al., *VLSI*, 2019. [4] Q. Luo et al., *IEDM,* 2015. [5] I. Baek et al., *IEDM,* 2011. [6] C. Lee et al., *IEDM,* 2022. [7] J. Lee et al., *Advanced Electronic Materials*, 2022. [8] W. Choi et al., *ACS Appl. Electron Mater*, 2023. [9] M. Kim, et al., *Sci. Adv,* 2021. [10] H. Kawai et al., *IEDM*, 2020. [11] J. Wu et al., *VLSI*, 2021.



	V_{prg}	Endurance	Speed	MLC	Scaling
Flash	X	X	△	O	X
FeFET	O	O	O	X	X
PCRAM	X	△	O	X	O
Our device	O	O	△	O	O

O : Good △: Medium X : Bad

Table 1. Comparison of memory characteristics among flash memory, FeFET, PCRAM, and bypass RRAM (Our device). Our device shows the feasibility of high-density memory.

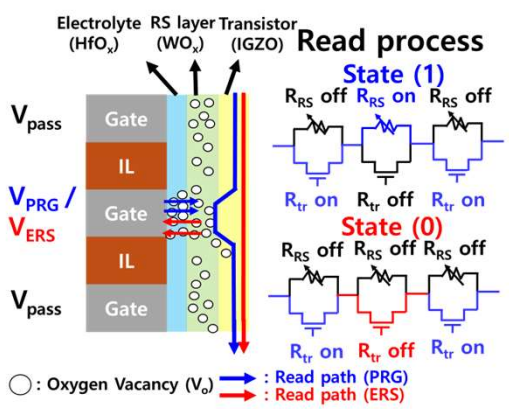


Fig. 1 Schematic and circuit diagram of proposed bypass RRAM in V-NAND structure. V-NAND operation can be obtained through the bypass reading between the WO_x resistivity switching (RS) layer and IGZO transistor (Tr).

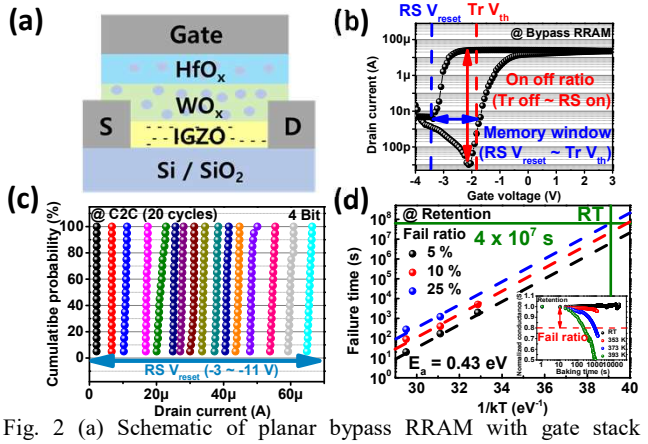


Fig. 2 (a) Schematic of planar bypass RRAM with gate stack ($W/HfO_x/WO_x$/IGZO). (b) Transfer curve through the bypass reading between the Tr and RS layer depending on each state. (c) Multi-bit operation owing to the analog state of RS layer. (d) $t_{failure}$ with various fail ratio (5 ~ 25 %) based on the E_a (0.43 eV).

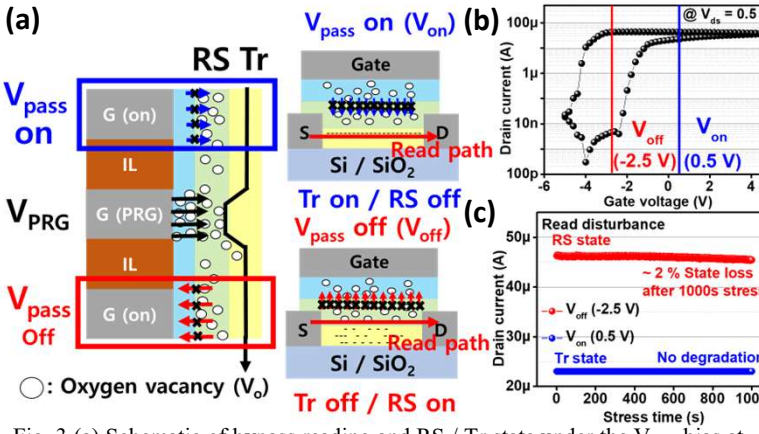


Fig. 3 (a) Schematic of bypass reading and RS / Tr state under the V_{pass} bias at unselected gate. RS state should not be affected by V_{pass} bias. (b) V_{pass} on (V_{on}) and V_{pass} off (V_{off}) bias at transfer curve in the bypass RRAM. (c) RS and Tr states under 1000 seconds stress time of the V_{on} (0.5 V) and V_{off} (-2.5 V) pulses. RS and Tr maintain each states under 1000 seconds stress time.

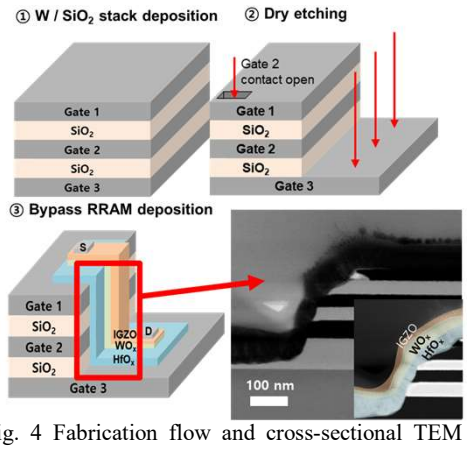


Fig. 4 Fabrication flow and cross-sectional TEM image of the VB-RRAM. All gate stacks are well deposited at the side wall of the base structure (W / SiO_2 / W / SiO_2 / W). Channel length and width of switching region are 30 nm / 20 um, respectively.

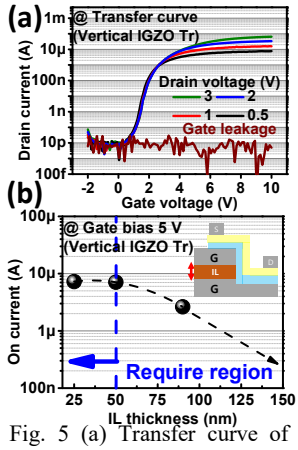


Fig. 5 (a) Transfer curve of vertical IGZO Tr for selector operation. (b) I_{on} of IGZO Tr depending on the SiO_2 layer (insulating layer) thickness.

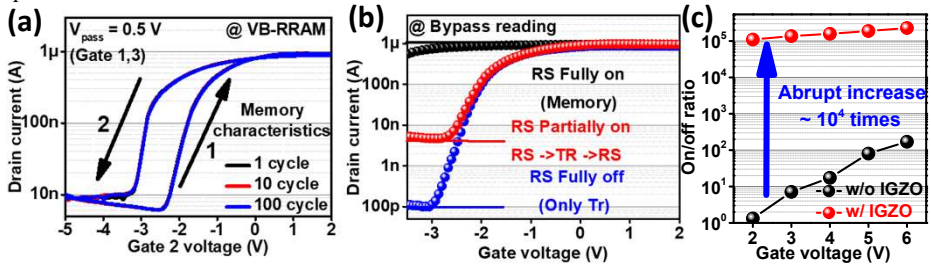


Fig. 6 (a) Transfer curves of VB-RRAM under V_{pass} = 0.5 V at unselected gate. Stable memory operation was obtained during DC 100 cycles. (b) Bypass reading between the RS and Tr layer depending on RS states. (c) Comparison of on/off ratio between the device with IGZO and without IGZO. High on/off ratio (> 10^5) can be obtained through the extremely low off current of IGZO Tr.

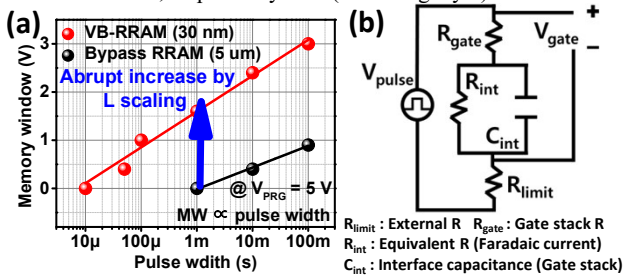


Fig. 7 (a) MW of the VB-RRAM (30 nm) and planar bypass RRAM (5 um) depending on the pulse width. (b) Equivalent circuit of the gate stack in VB-RRAM.

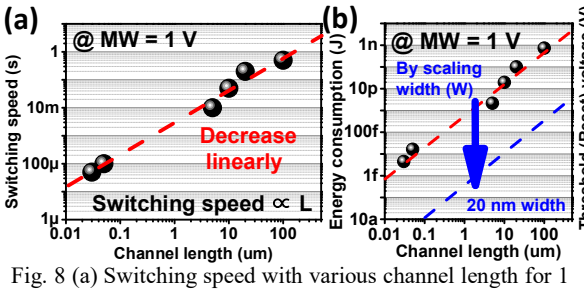


Fig. 8 (a) Switching speed with various channel length for 1 V MW. (b) Energy consumption for 1 V MW depending on the channel length. Energy consumption can be decreased abruptly with scaling the channel width.

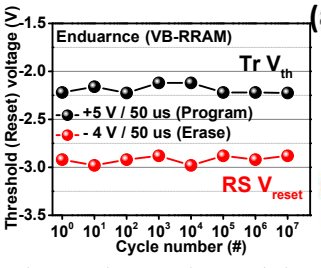


Fig. 9 Endurance characteristics of VB-RRAM for 10^7 cycles using V_{PRG} (5 V / 50 us) and V_{ERS} (- 4 V / 50 us).

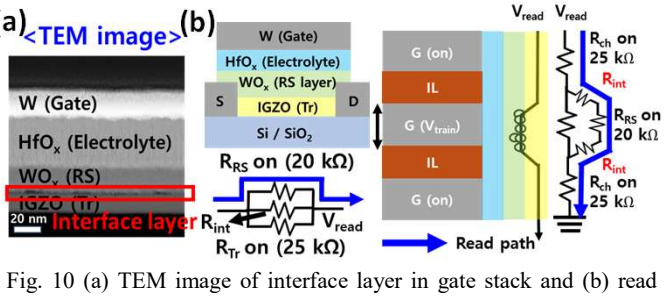


Fig. 10 (a) TEM image of interface layer in gate stack and (b) read path during the bypass reading in planar bypass RRAM and VB-RRAM. During bypass reading at VB-RRAM, I_{on} is critically affected by the R_{int}.

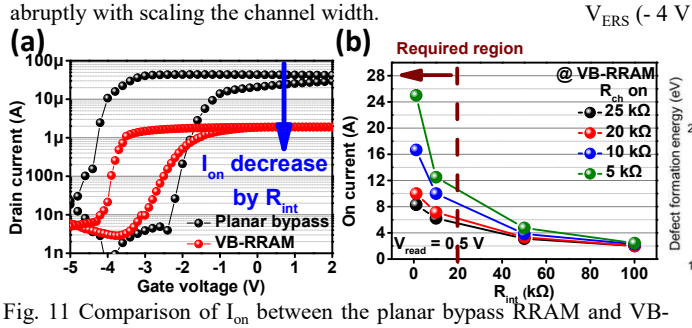


Fig. 11 Comparison of I_{on} between the planar bypass RRAM and VB-RRAM. In VB-RRAM, I_{on} is degraded by the R_{int}. (b) I_{on} with various R_{int} and R_{ch} on. R_{int} should be reduced for high I_{on} and accurate reading of RS layer.

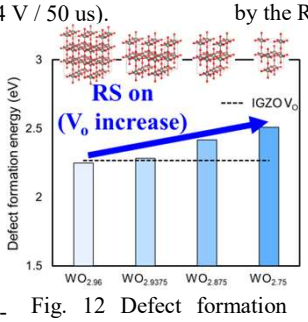


Fig. 12 Defect formation energy (DFE) of V_o in the IGZO Tr and WO_x(x = 2.96 - 2.75) RS layers.

	[1]	[2]	[8]	[9]	Our work
Mechanism	Charge trap	Phase change	Phase change	Polarization	Electrochemical reaction
V_{prog}	20 V	10 V	20 V	3 V	< 5 V
Speed	100 us	-	0.6 us	1 us	50 us
On/off (MW)	10^5 (5.6 V)	10	100	10^4 (2.5 V)	10^6 (~ 8 V)
Endurance	10^4	10^6	10^5	10^8	10^7
MLC	> 4 bit	1 bit	1 bit	2 bit	> 4 bit

Table 2. Comparison of various memory parameters in other emerging memories. These results show that our device can be a promising candidate for the V-NAND memory.