Highly Scalable Vertical Bypass RRAM (VB-RRAM) for 3D V-NAND Memory

Geonhui Han[1], Youngdong Kim[1], Jaeseon Kim[1], Dongmin Kim[1], Yoori Seo[1], Chuljun Lee[1], Jinmyung Choi[2], Jinwoo Lee[2], Dongho Ahn[2], Sechung Oh[2], Donghwa Lee[2], and Hyunsang Hwang[1]

[1] Department of Material Science and Engineering, Pohang University of Science and Technology (POSTECH), Republic of Korea
[2] Advanced Process Development Team 2, Samsung Electronics, Republic of Korea

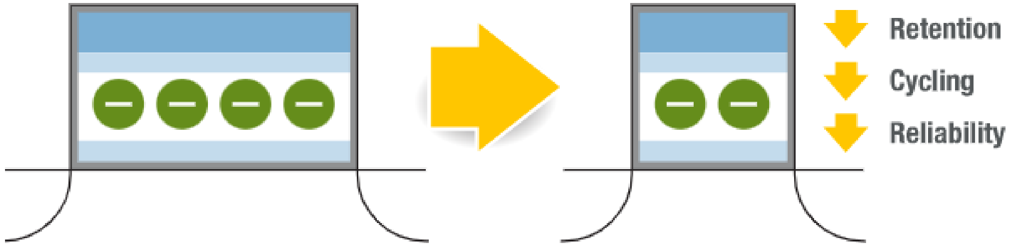
Outline

- Introduction
- Feasibility of bypass reading in planar structure
- Vertical integration for V-NAND operation
- Memory characteristics of the VB-RRAM
- Interface resistance (R_{int}) issue in the VB-RRAM
- Conclusion

High scalability of the RRAM for V-NAND

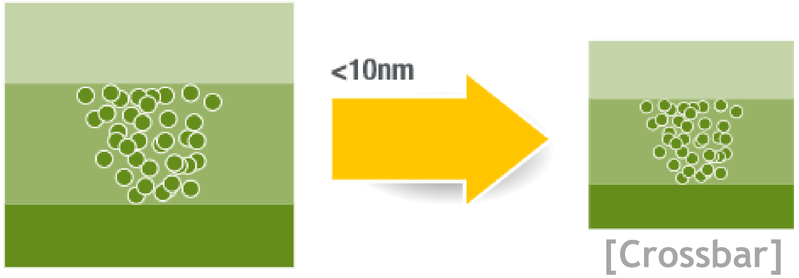
✓ Charge based Flash memory

scaling > less electrons > performance degrade

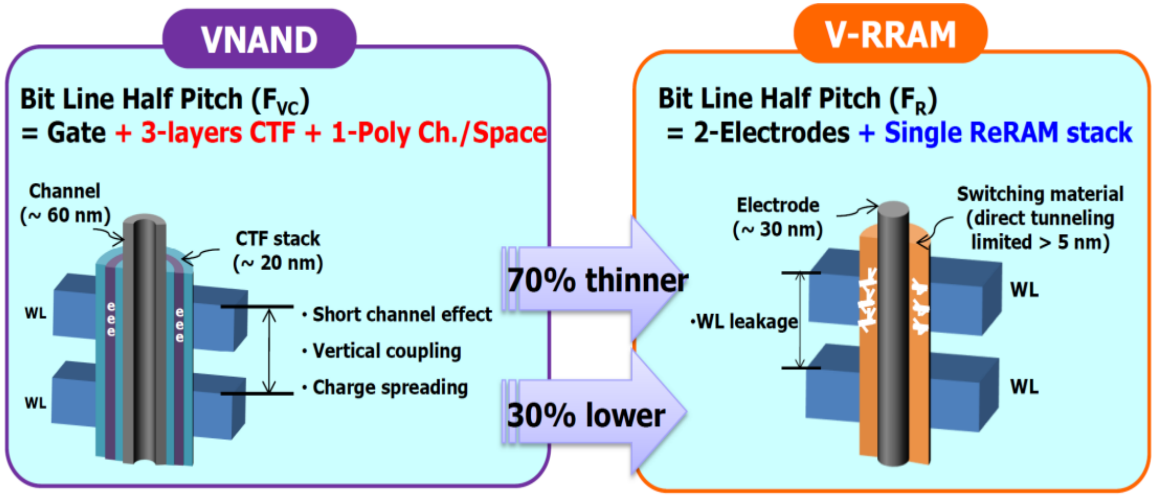


✓ Non-charge based RRAM

scaling > same nanofilament > better performance



[Crossbar]



[LETI memory workshop 2012]

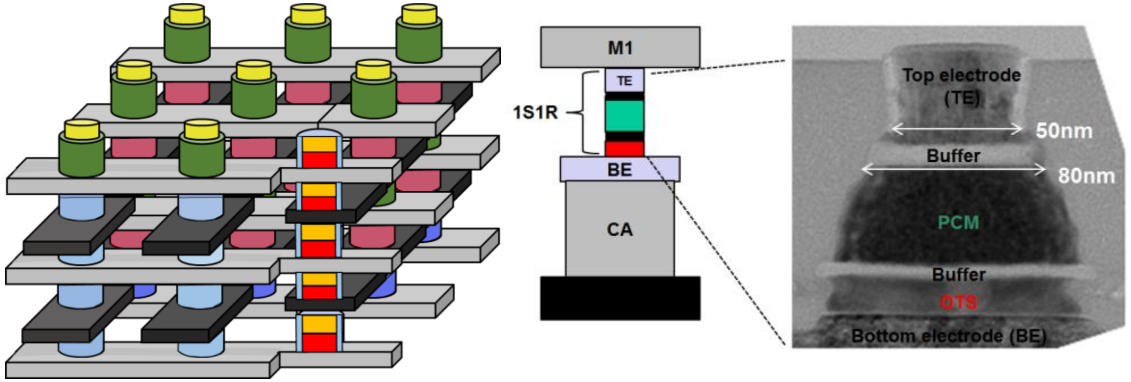
	Flash	RRAM
Cell area	$<4F^2$ if 3D	$<4F^2$ if 3D
Multi-bit	3	3
Scalability	< 20 nm	< 10 nm
Voltage	> 10 V	< 3 V
speed	~ 10us	< 10 ns
Energy/bit	~ 100pJ	~ 0.1 pJ
endurance	10^5	10^6 ~ 10^{12}
Retention	> 10 years	> 10 years

✓ RRAM is gaining interest as a potential alternative to flash memory

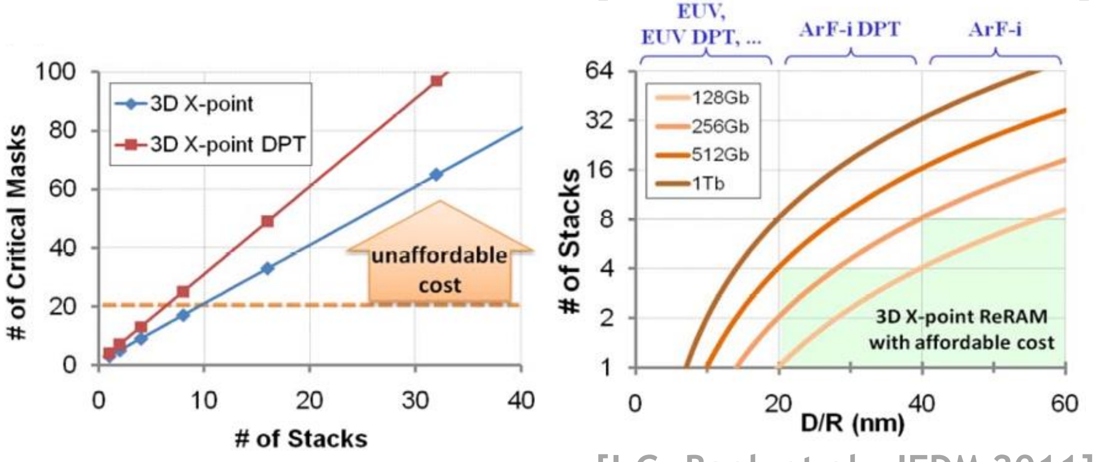
✓ RRAM : High scalability, low voltage, stable endurance, and low power consumption

Limitation of conventional 3D vertical RRAM

✓ Cross-point array (3D X-RRAM)



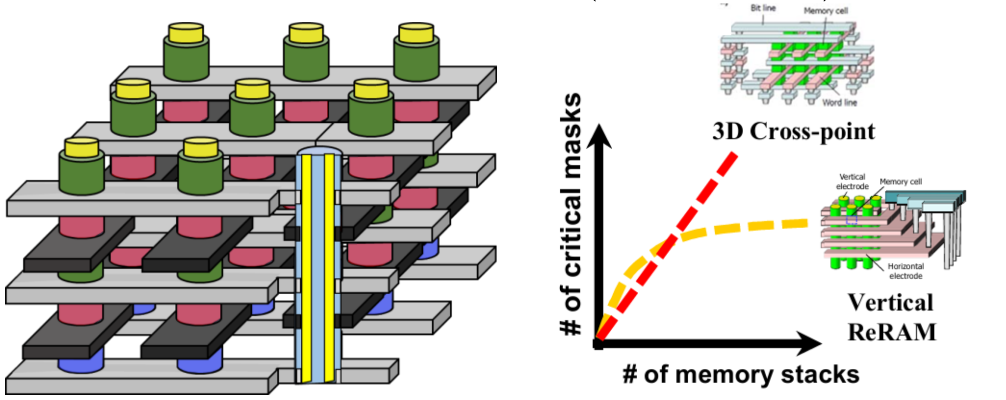
[C. W. Yeh et al., VLSI 2018]



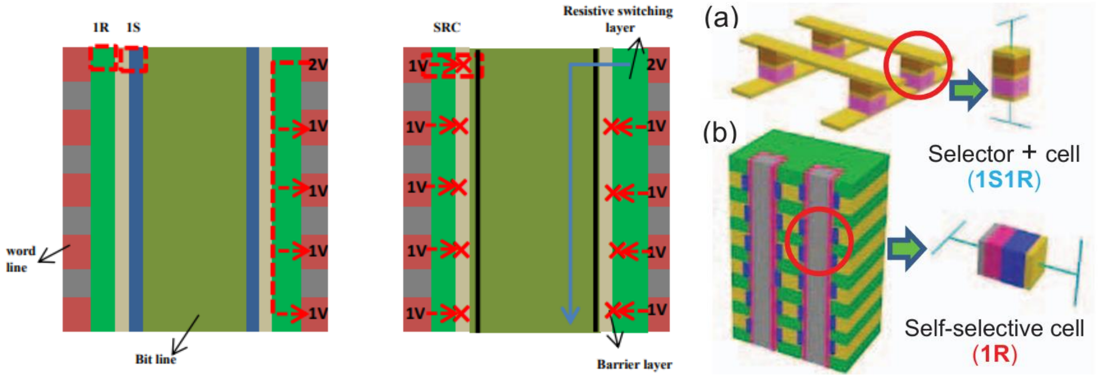
[I.G. Baek et al., IEDM 2011]

Good performance but high costs
(Complex fabrication / process)

✓ Vertical RRAM (V-RRAM)



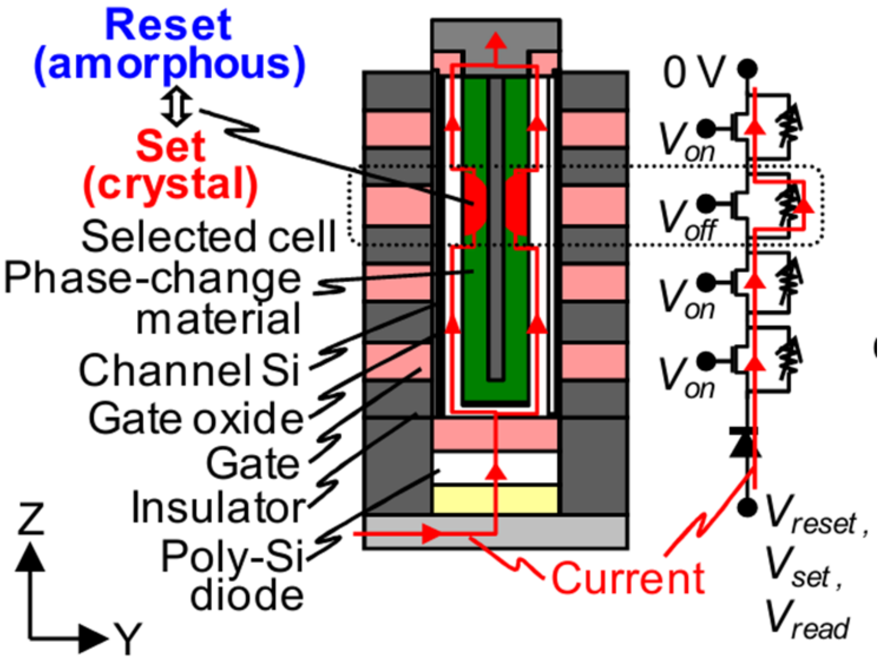
[I.G. Baek et al., IEDM 2012]

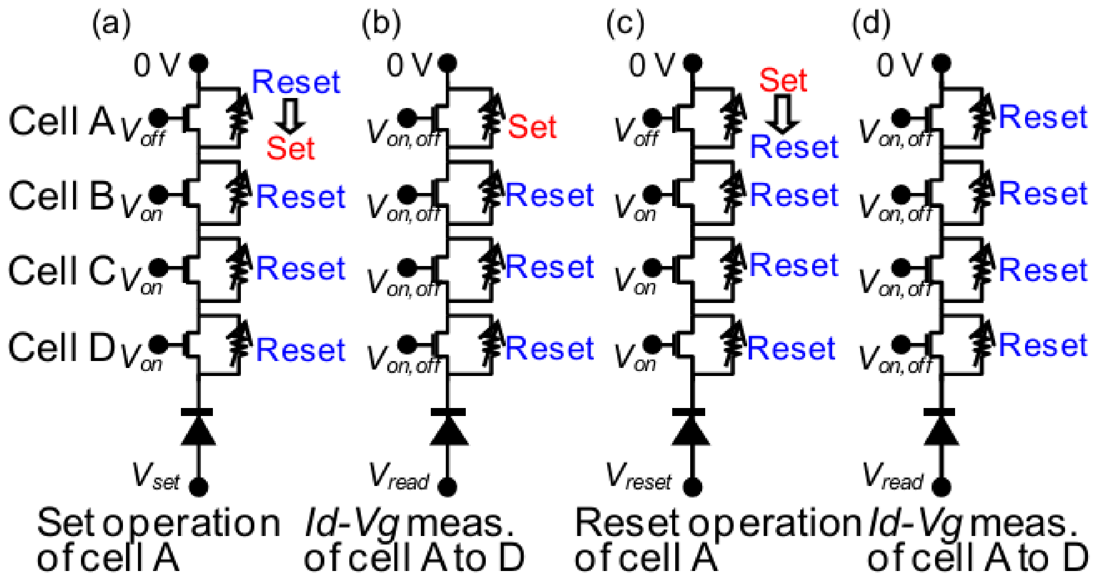


[Q. Luo et al., IEDM 2015]

Low costs but poor performance
(Requirements of selector integration)

V-NAND compatible structure (bypass memory)

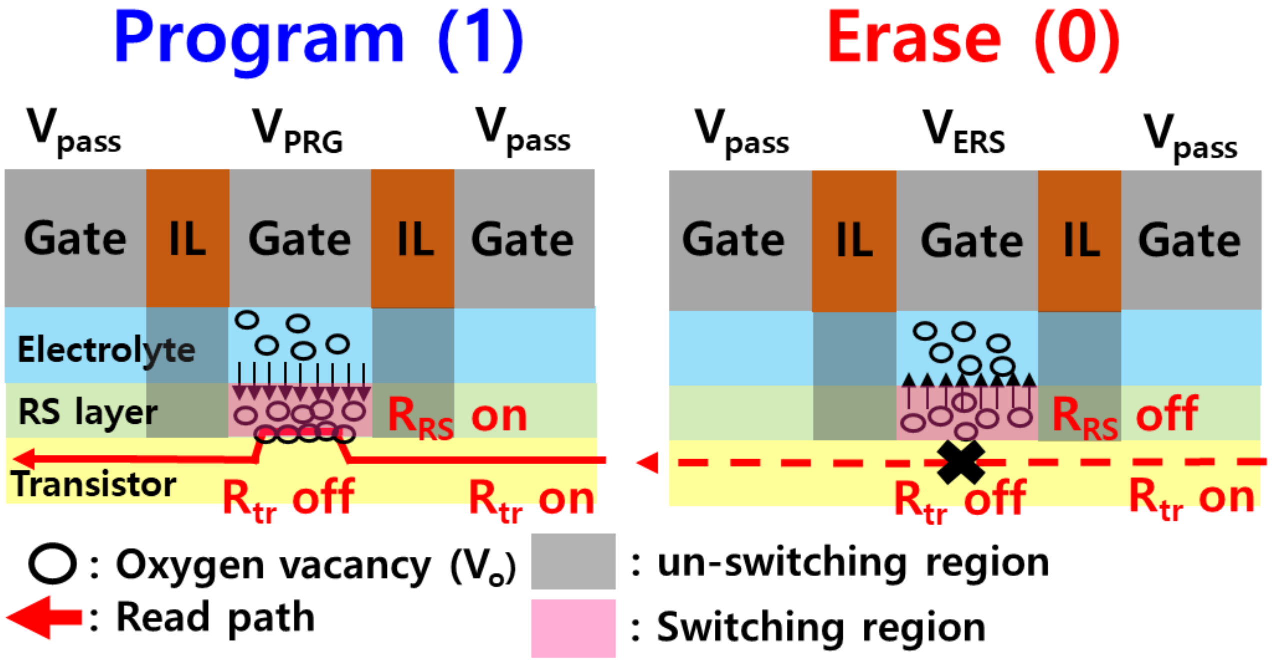


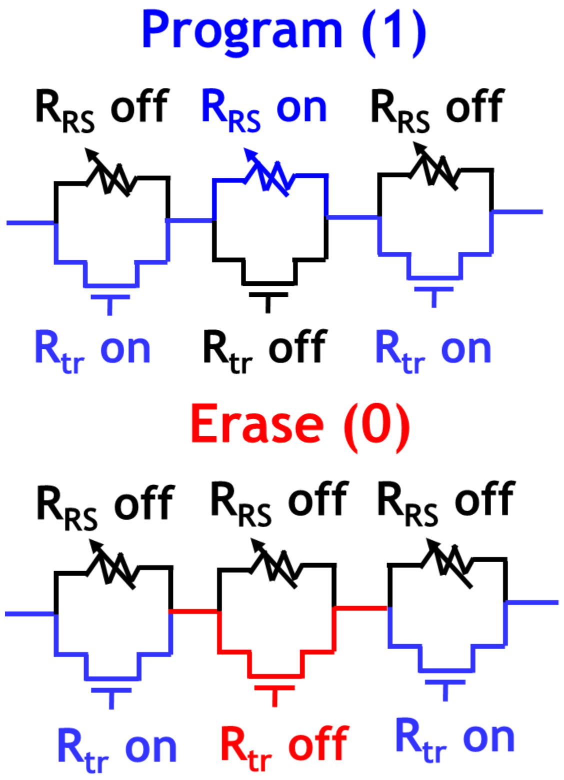


[M. Kinoshita et al., VLSI 2012]

- ✓ Bypass memory can be a promising candidate for the V-NAND memory
- ✓ Bypass memory utilizes the switching layer as memory and transistor as selector
- ✓ Excellent memory characteristics & low costs can be achieved in bypass memory

Concept of V-NAND compatible bypass RRAM

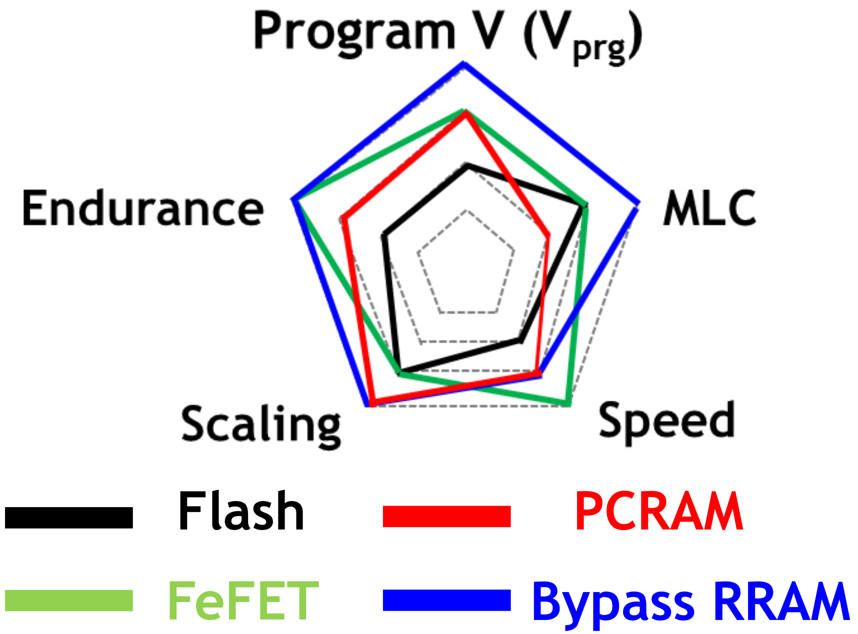




* RS layer : Resistive switching layer

- ✓ For the first time, we proposed bypass RRAM using interface switching RRAM
- ✓ Bypass RRAM operates through bypass reading between the RS and Tr layer
- ✓ RS states can be varied depending on the V_o concentration by PRG / ERS voltage

Advantages of the bypass RRAM for V-NAND



	V_{prg}	Endurance	Speed	MLC	Scalability
Flash	X	X	X	O	Δ
FeFET	Δ	O	O	X	X
PCRAM	X	Δ	O	X	O
Bypass RRAM	O	O	Δ	O	O

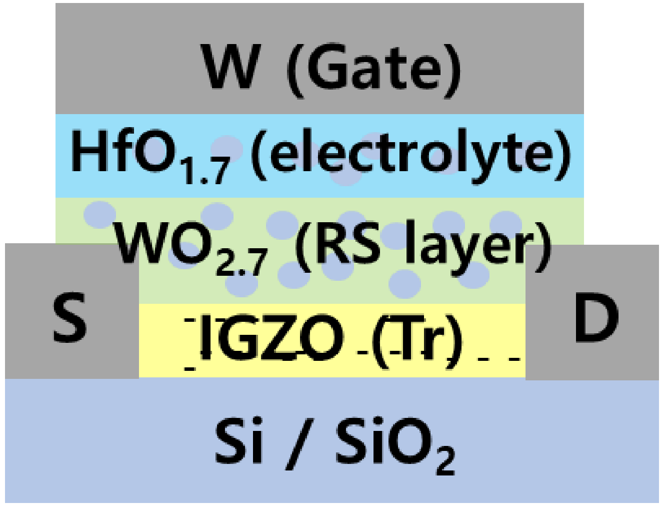
O : Good Δ: Medium X : Bad

- ✓ Bypass RRAM holds potential as a promising candidate for NVM applications.
- ✓ Compared to other memory, bypass RRAM has high scalability and MLC operation

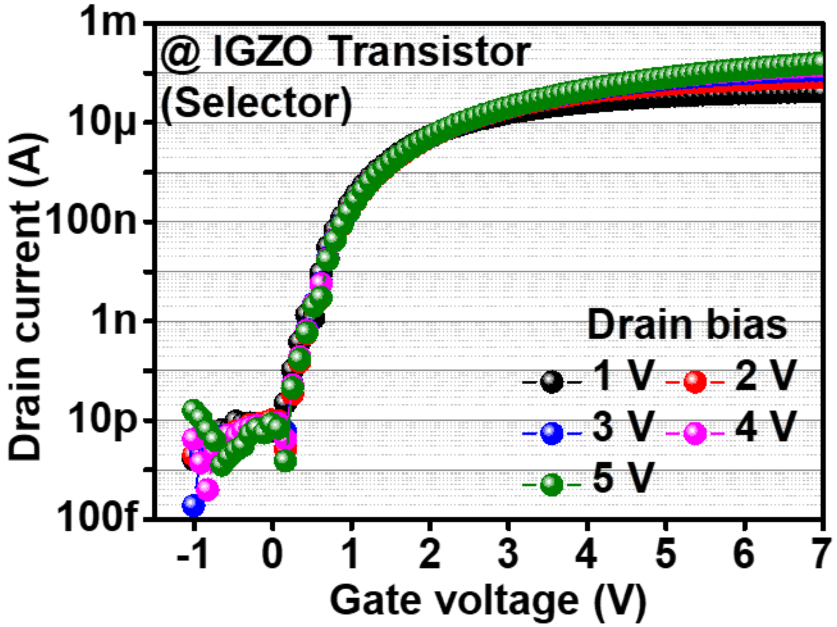
Outline

- Introduction
- **Feasibility of bypass reading in planar structure**
- Vertical integration for V-NAND operation
- Memory characteristics of the VB-RRAM
- Interface resistance (R_{int}) issue in the VB-RRAM
- Conclusion

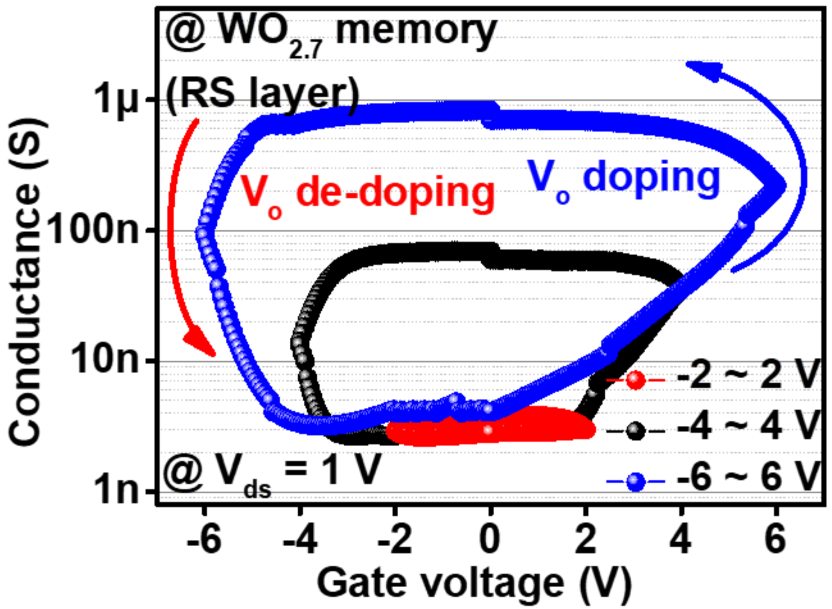
Fabrication of bypass RRAM in planar structure



IGZO Transistor



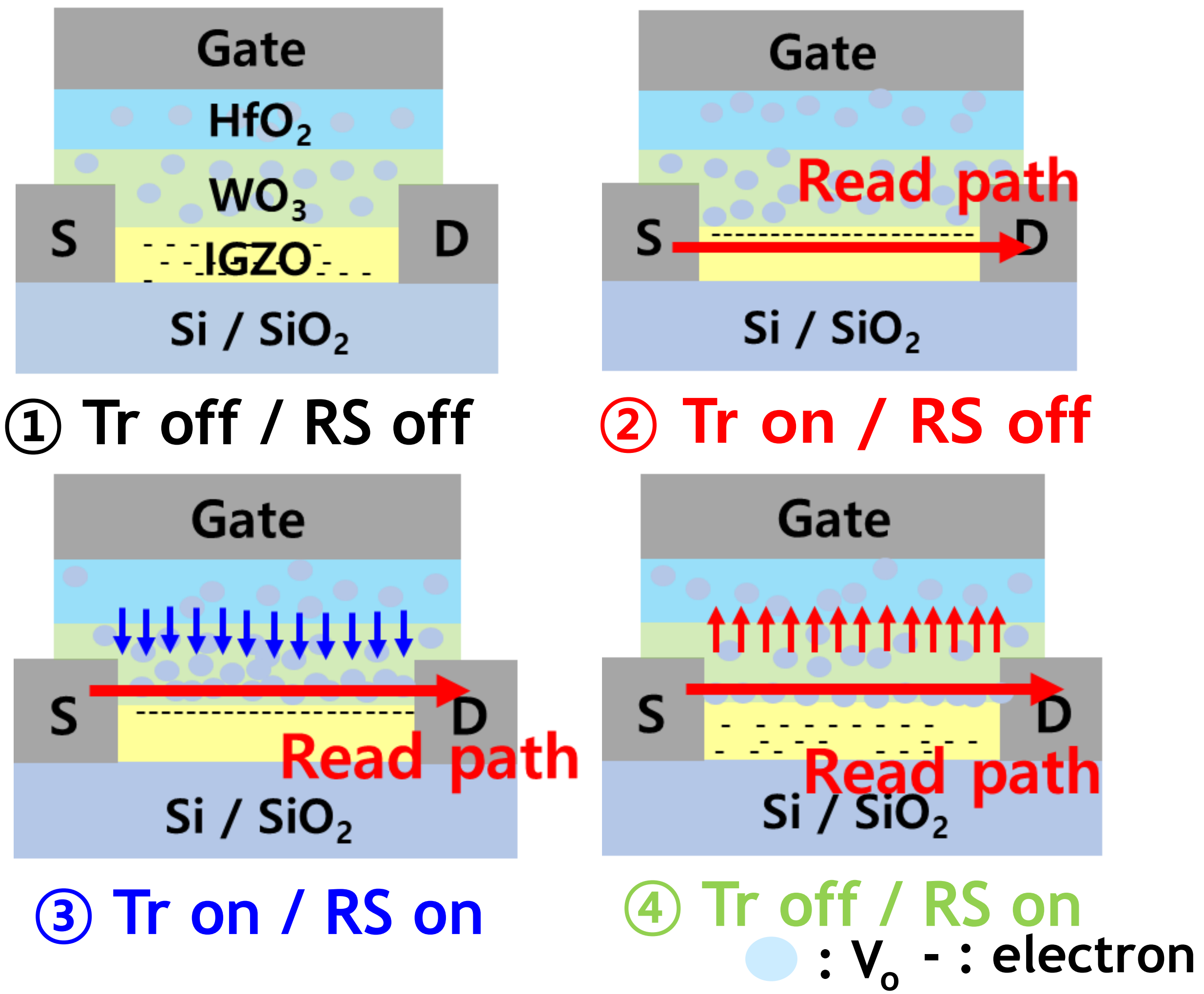
$WO_{2.7}$ RS layer

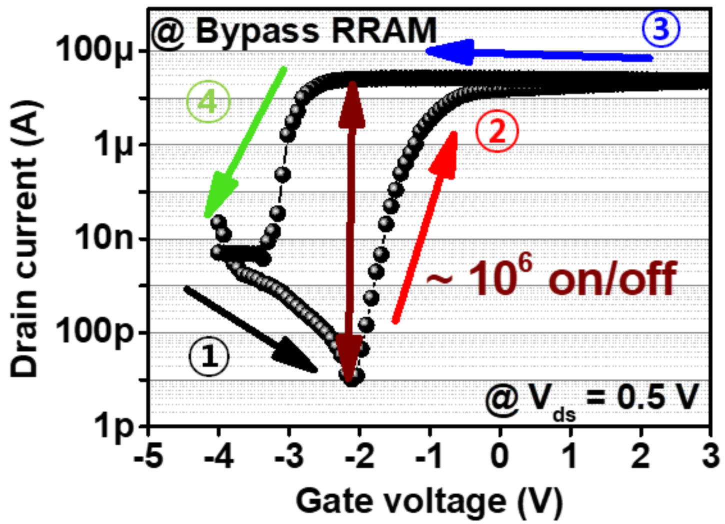


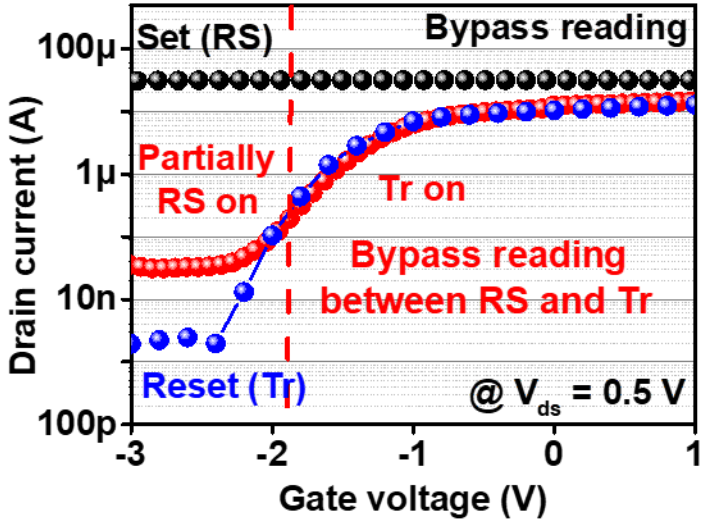
Requirement :R_{Tr} on < R_{RS} on < R_{RS} off < R_{Tr} off

- ✓ Selector : IGZO based Tr layer for high on/off ratio (10^4 ~ 10^{11} Ω)
- ✓ Memory : $WO_{2.7}$ based RS layer for multi-bit operation (> 4 bit)
- ✓ We integrated the $WO_{2.7}$ RS layer (memory) to the IGZO Tr (selector) for bypass RRAM

Feasibility of bypass reading in planar structure

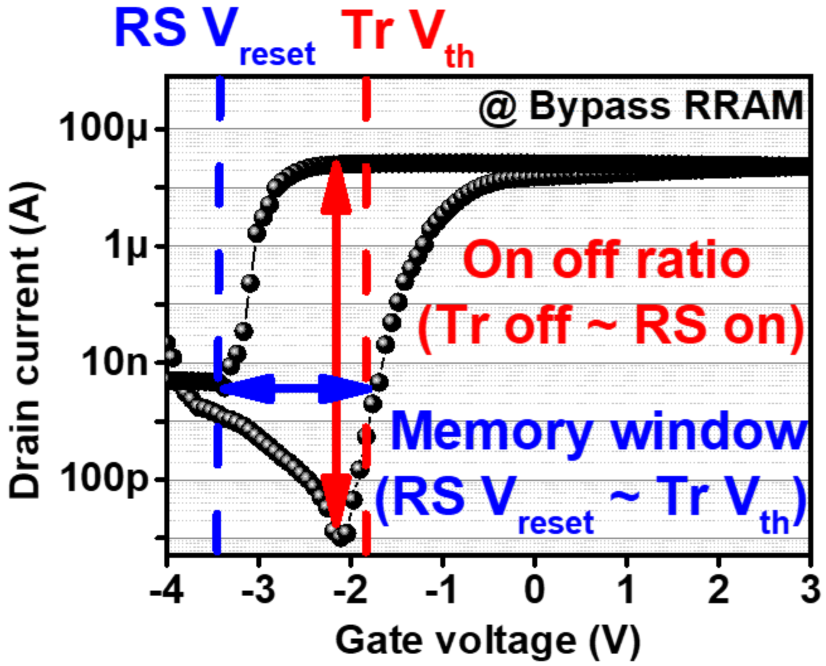


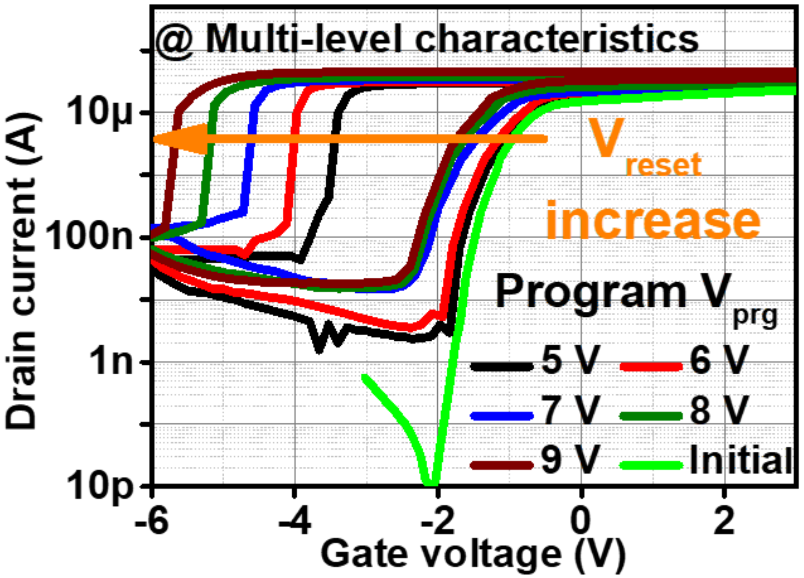


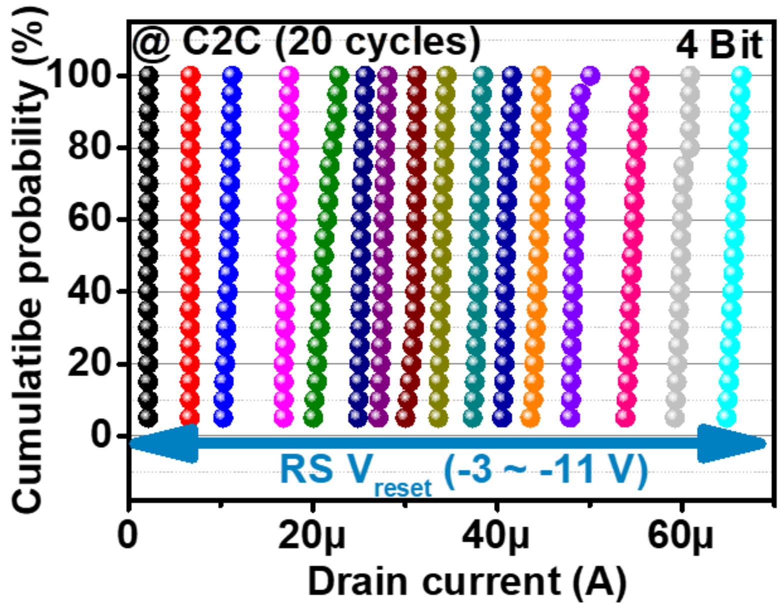


✓ We confirmed the bypass reading depending on RS states in the bypass RRAM

MLC in bypass RRAM for high-density memory

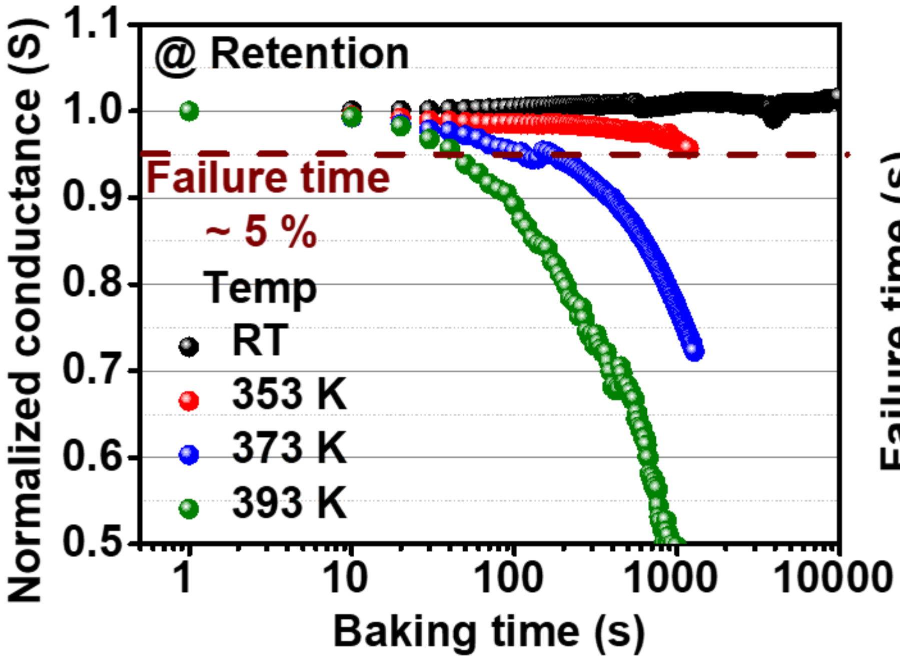


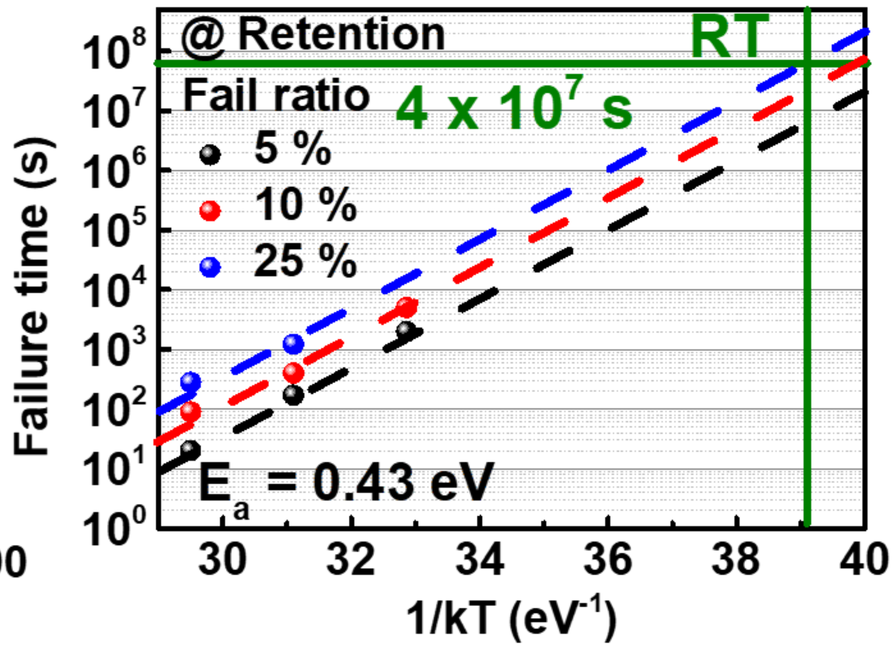




- ✓ Memory window (MW) : RS V_{reset} ~ Tr V_{th}
- ✓ Analog switching of RS layer induce the MLC operation
- ✓ We achieved the 8 V MW and 4-bit operation for high-density memory

Retention characteristics of the bypass RRAM





Arrhenius equation : $t_{failure} \propto e^{\frac{E_a}{K_b T}}$

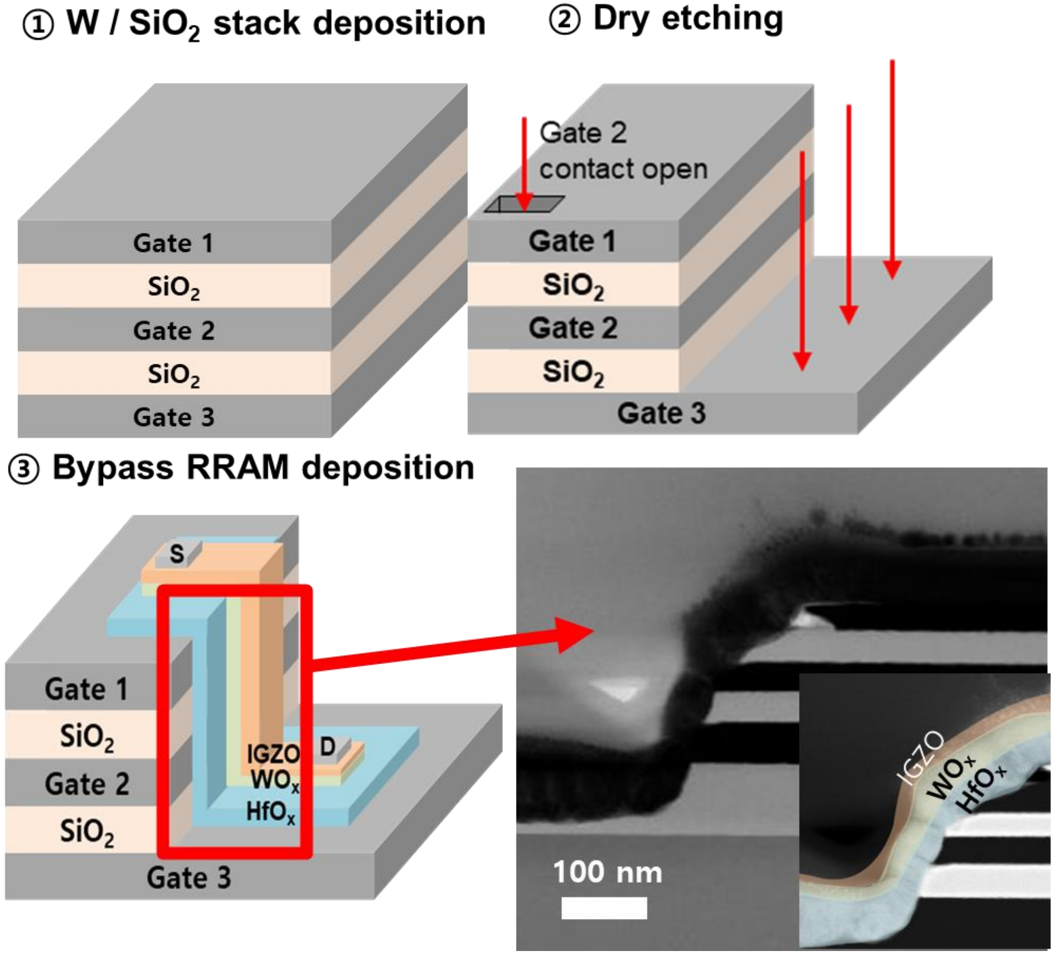
K_b : boltzman constant
T : Temperature
E_a : activation E

- ✓ We evaluated the failure time (retention) at various temperature
- ✓ We obtained the 1-year retention at 25 % fail ratio by extracted E_a (0.43 eV)
- ✓ Retention can be improved by increasing E_a through the diffusion barrier

Outline

- Introduction
- Feasibility of bypass reading in planar structure
- Vertical integration for V-NAND operation
- Memory characteristics of the VB-RRAM
- Interface resistance (R_{int}) issue in the VB-RRAM
- Conclusion

Fabrication flow of the VB-RRAM



Base structure deposition
(W / SiO_2 / W (30 nm) / SiO_2 / W)

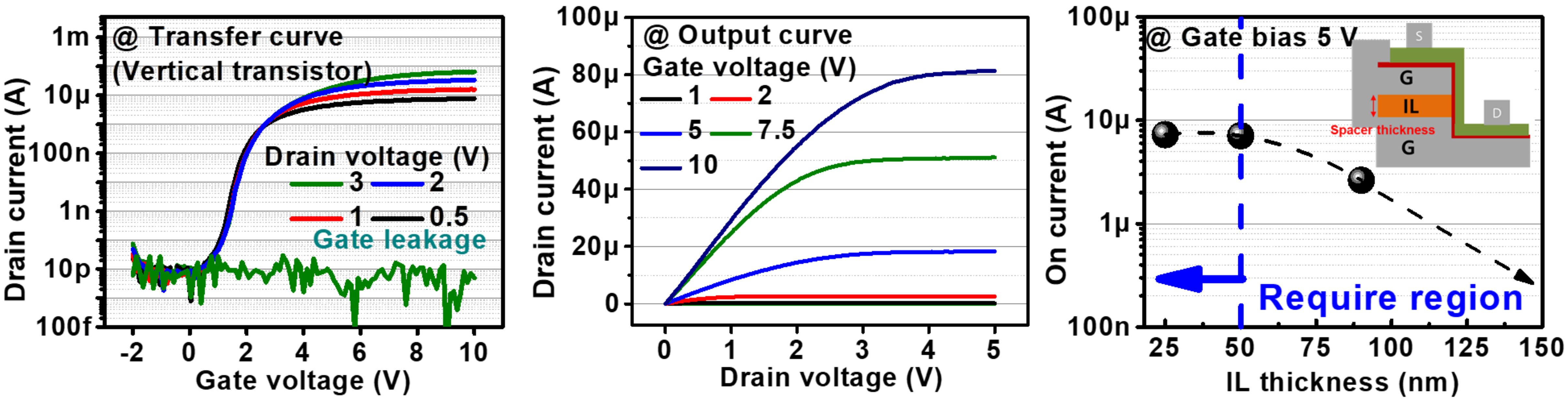
Dry etching for contact area

Gate stack deposition
($HfO_{1.7}$ / $WO_{2.7}$ (RS) / IGZO (Tr))

Annealing at 300 ℃ for 1hour
(N_2 atmosphere)

- ✓ We integrated the bypass RRAM to the vertical structure for V-NAND operation
- ✓ We utilized the 30 nm W (switching area) and 50 nm SiO_2 (IL layer) for the VB-RRAM

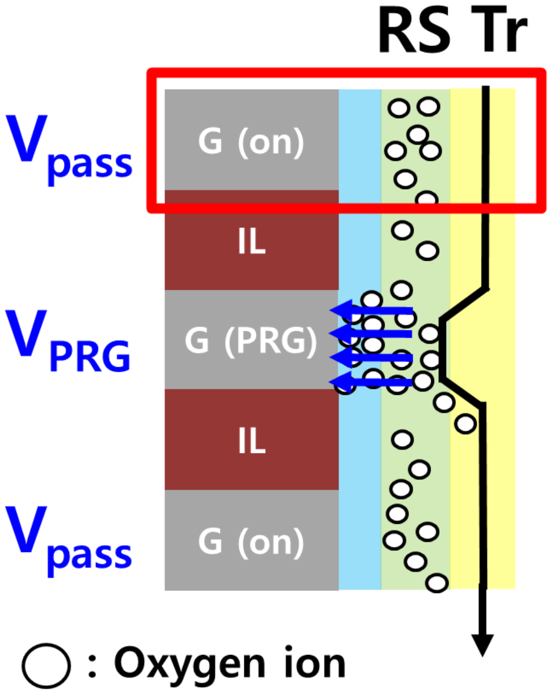
Optimization of IL thickness for VB-RRAM

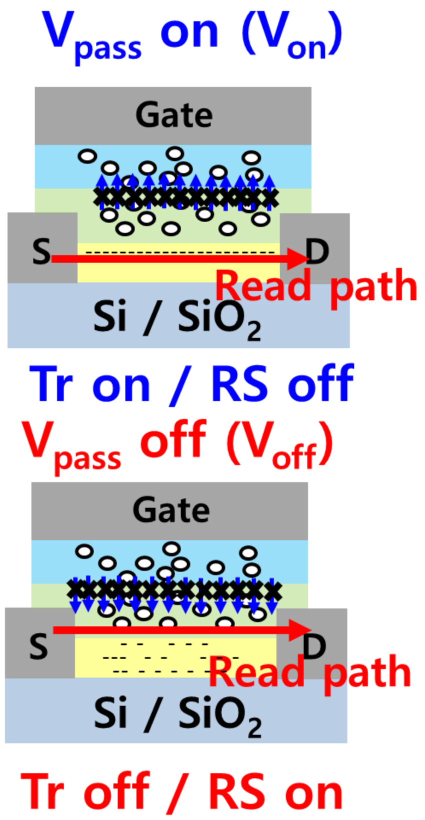


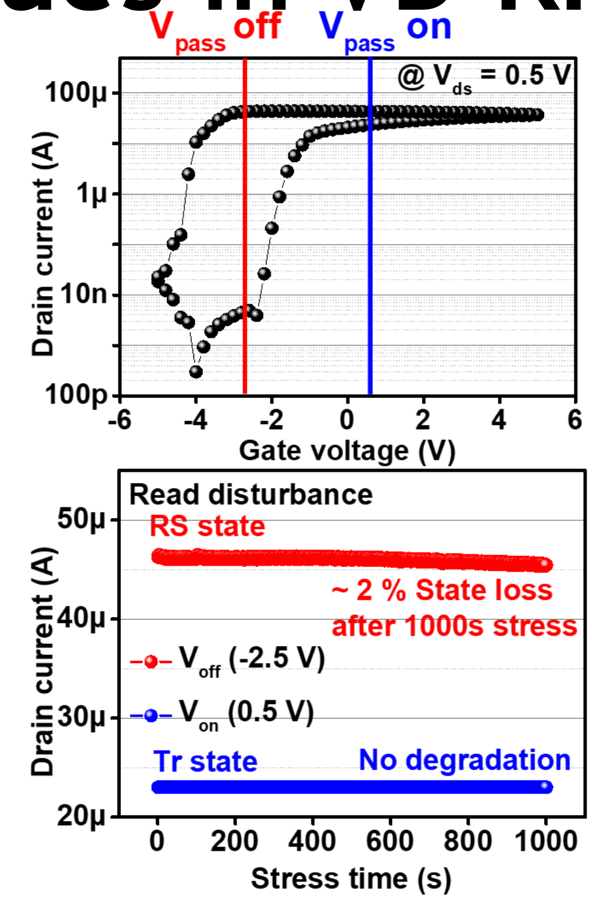
* IL : Isolation layer

- ✓ Without IL, we obtained high I_{on} (> 10 uA) in vertical IGZO transistor
- ✓ If the IL is too thick (> 50 nm), I_{on} of transistor decreases abruptly
- ✓ IL thickness should be below the 50 nm for the high I_{on} of the transistor

Read disturbance issues in VB-RRAM







✓ In VB-RRAM, read disturbance should be considered (unselected cell)

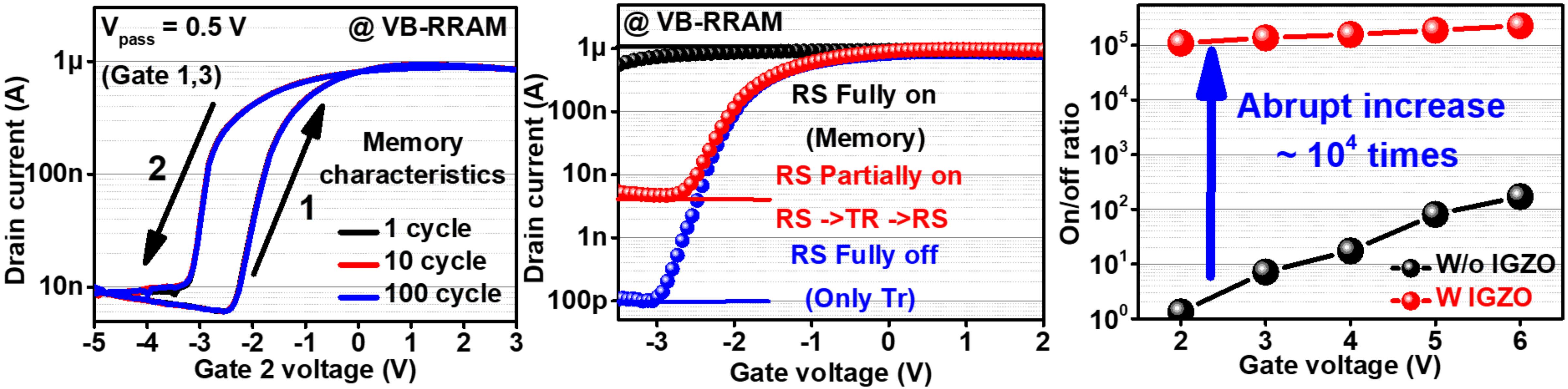
✓ We applied V_{pass} on (0.5 V) and V_{pass} off (-2.5 V) during 1000s stress

✓ Only 2 % state loss of RS states occurs while the Tr is tuned off

Outline

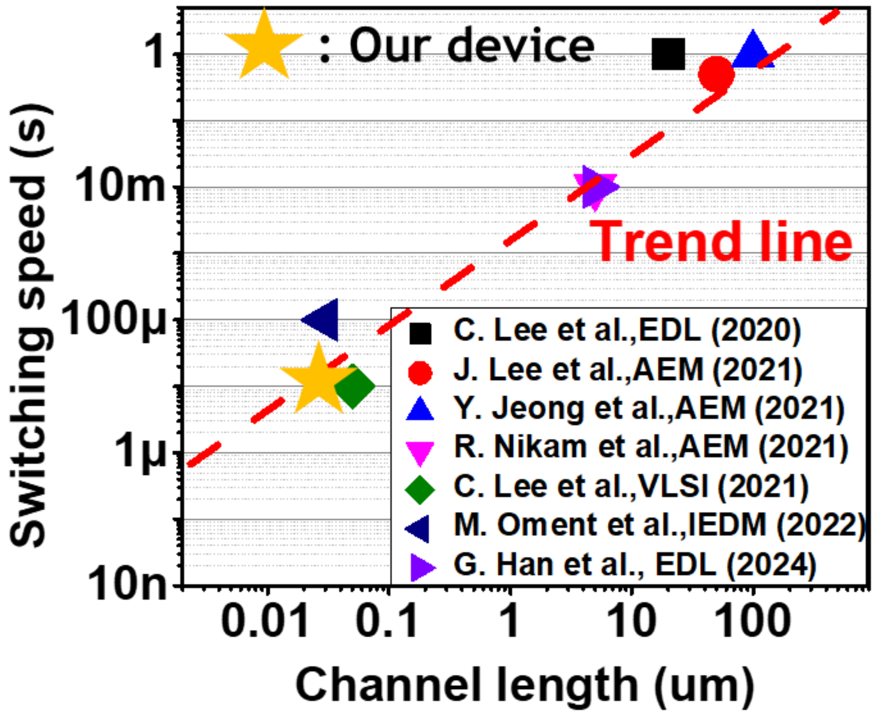
- Introduction
- Feasibility of bypass reading in planar structure
- Vertical integration for V-NAND operation
- **Memory characteristics of the VB-RRAM**
- Interface resistance (R_{int}) issue in the VB-RRAM
- Conclusion

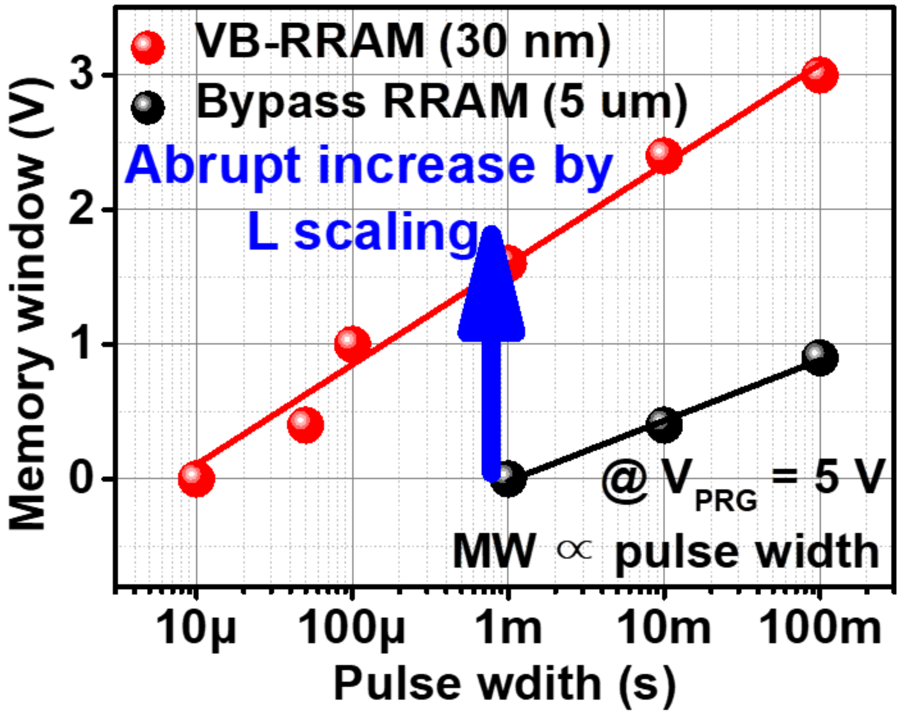
Memory characteristics of the VB-RRAM (1)



- ✓ VB-RRAM also shows the counter-clockwise hysteresis (memory characteristics)
- ✓ We demonstrated the bypass reading in VB-RRAM depending on the RS states
- ✓ On/off ratio (> 10^5) increase abruptly owing to the low off current of IGZO Tr

Improved switching speed by area scaling



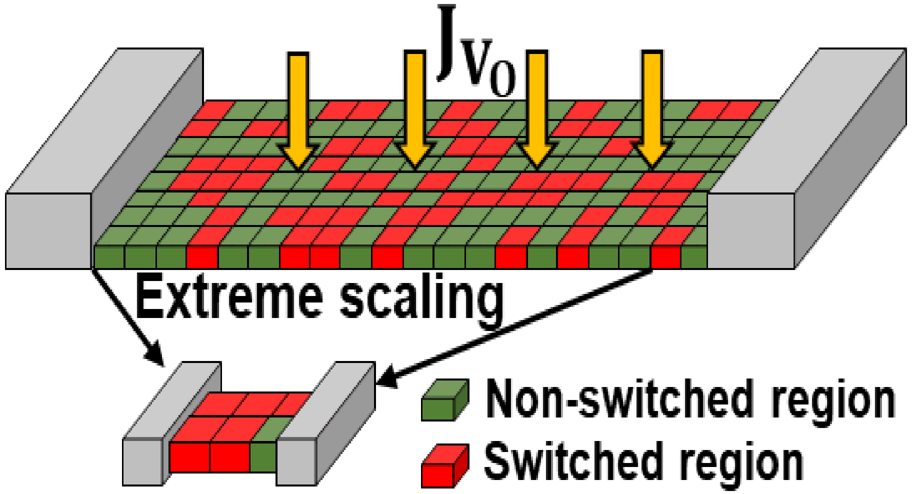


* ECRAM : Electrochemical RAM

- ✓ In conventional, Ion based ECRAM has area dependence of switching speed
- ✓ As channel length decreases, MW and switching speed are improved in VB-RRAM

Origin of area dependence in VB-RRAM

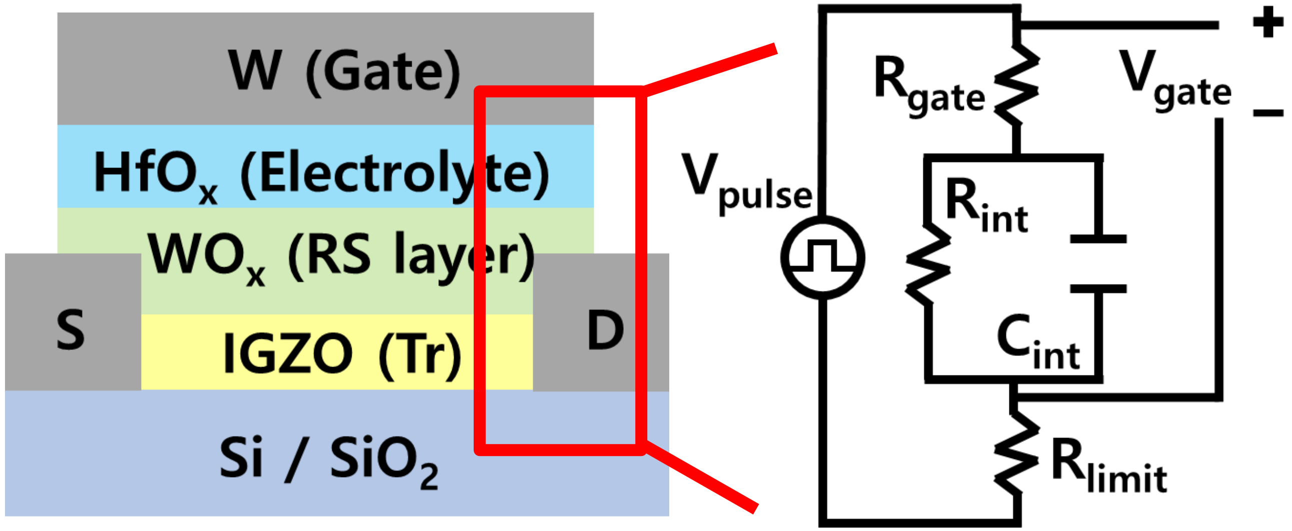
✓ Non-uniform ion injection



$$j_{ion} = 2cizieavoe^{-Ea/kbT}\sinh\left(\frac{z_i eaE}{k_b T}\right)$$

a = Jump distance
C_i = Concentration
v_o = Jump frequency
E_a = Activation E
K_b = Boltzman constant
T = Temperature

✓ Interface cap issues in VB-RRAM



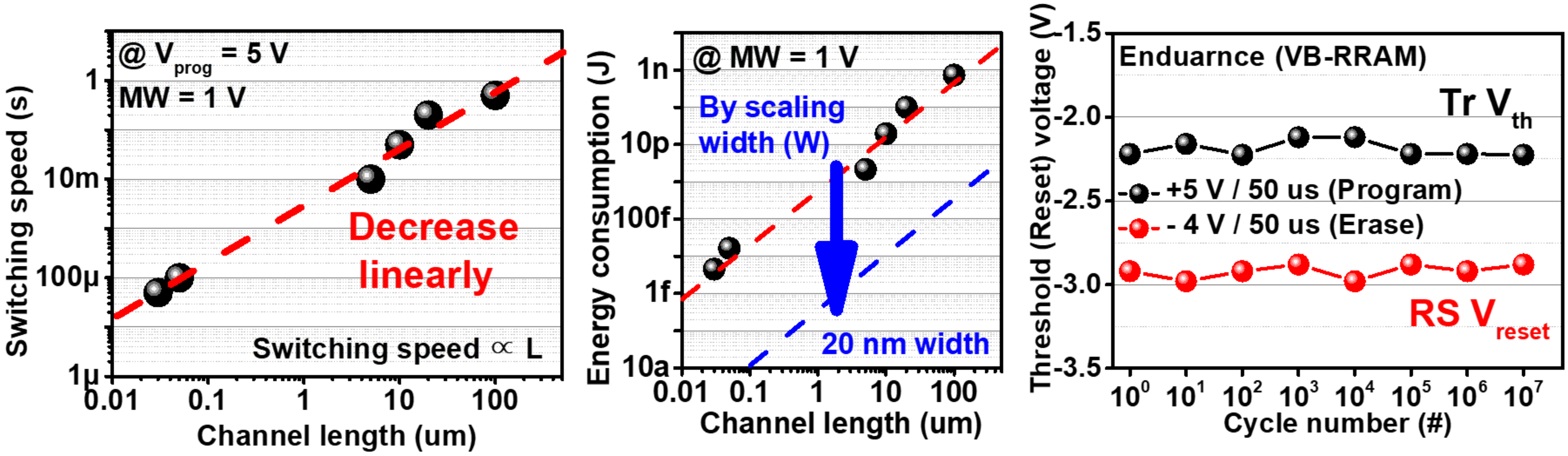
$$t_{switch} \propto R_{limit} * C_{int} \quad (C_{int} \propto A)$$

R_{gate} : Resistance of gate stack
R_{int} : Resistance of interface in gate stack
C_{int} : Interface capacitance in gate stack
R_{limit} : External resistance

✓ As the channel length decreases, probability of uniform ion injection increases

✓ Also, C_{int} can be reason of the slow switching speed in the um channel length

Memory characteristics of the VB-RRAM (2)



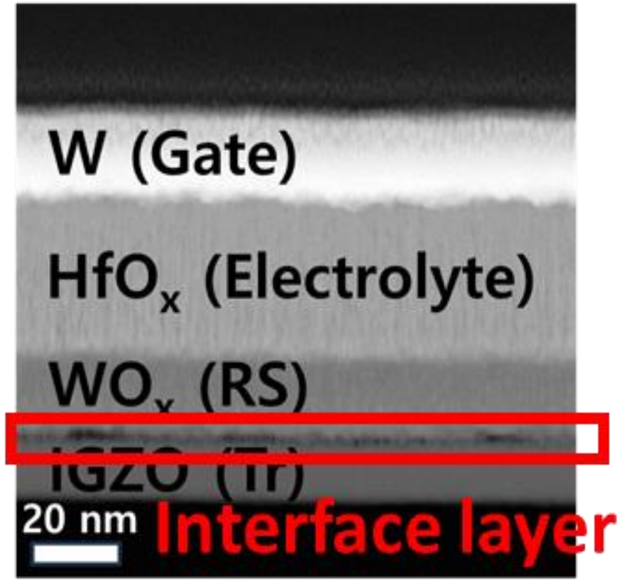
- ✓ VB-RRAM achieved 1 V MW with 50 us pulse width (30 nm channel length)
- ✓ Low power consumption (~5 fJ) was also obtained in VB-RRAM
- ✓ With 50 us pulse width, VB-RRAM has excellent endurance (> 10^7 cycles) for V-NAND

Outline

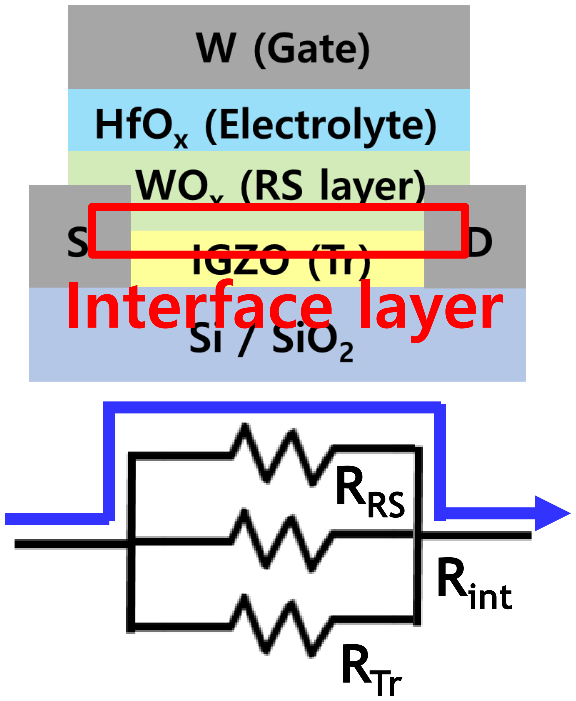
- Introduction
- Feasibility of bypass reading in planar structure
- Vertical integration for V-NAND operation
- Memory characteristics of the VB-RRAM
- **Interface resistance (R_{int}) issue in the VB-RRAM**
- Conclusion

Interface resistance issues (R_{int}) in the VB-RRAM

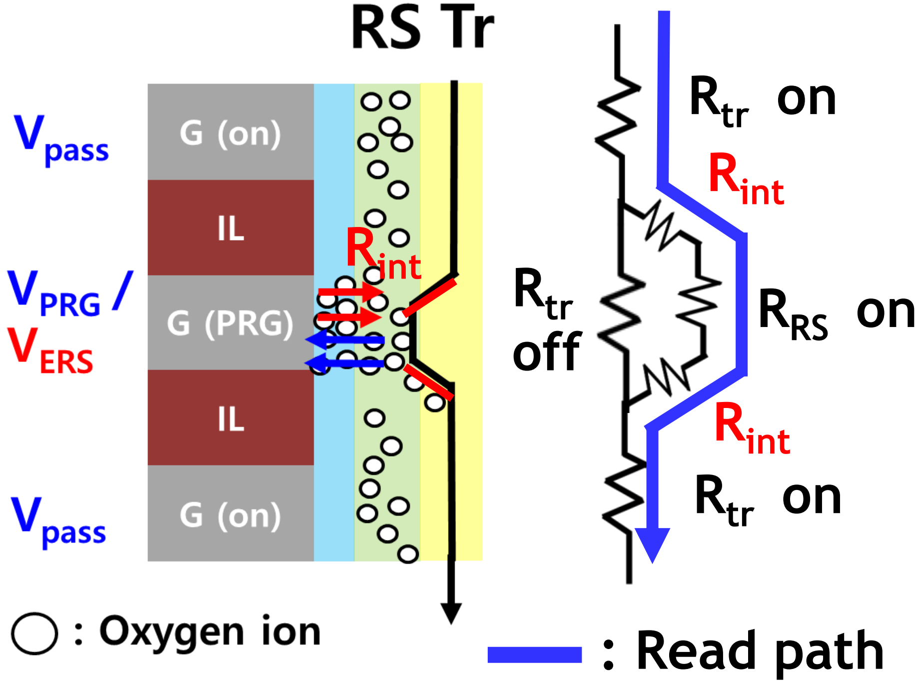
<TEM image>



Planar Bypass RRAM



Vertical Bypass RRAM

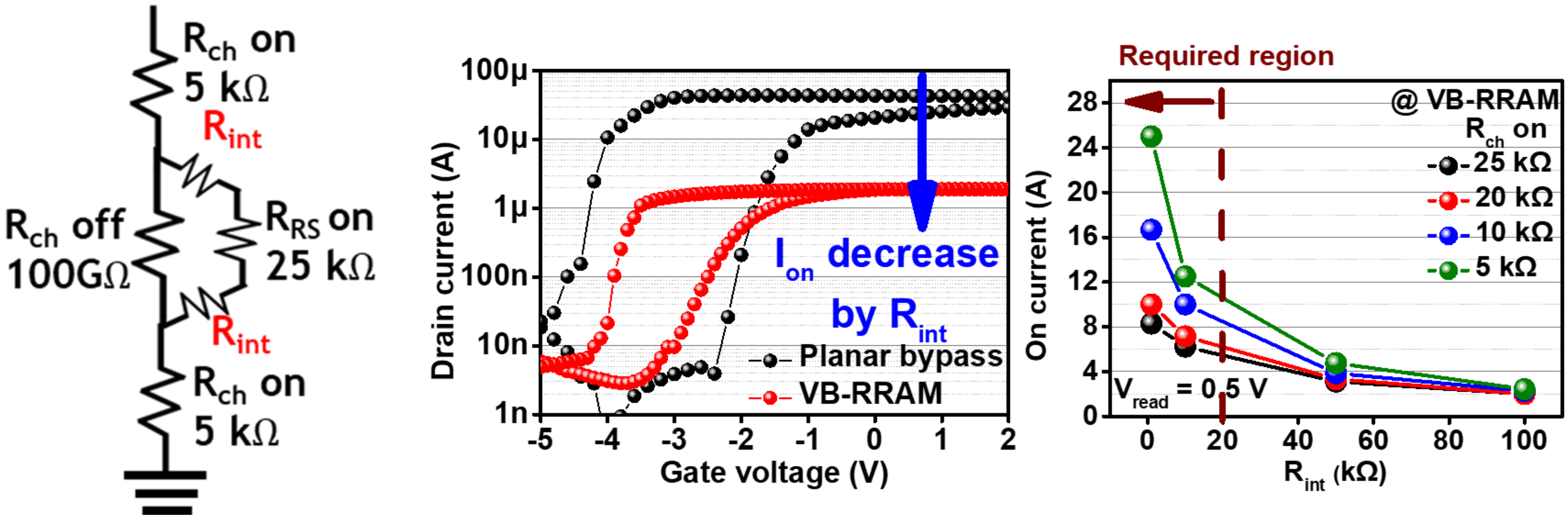


Requirements : 2 R_{tr} on +2 R_{int} < R_{RS} on

* R_{int} = Resistance of the interface layer

- ✓ Compared to the planar structure, interface layer (IL) issues occurred in VB-RRAM
- ✓ During the bypass reading, resistance of IL (R_{int}) can disturb the RS reading

Interface resistance issues (R_{int}) in the VB-RRAM



- ✓ I_{on} is decreased at VB-RRAM compared to planar bypass RRAM due to R_{int}
- ✓ We extracted the R_{int} as 100 kΩ by I_{on} of the VB-RRAM
- ✓ R_{int} should be reduced below the 20 kΩ (R_{RS} on) for accurate reading of RS states

Origin of the interface layer in VB-RRAM

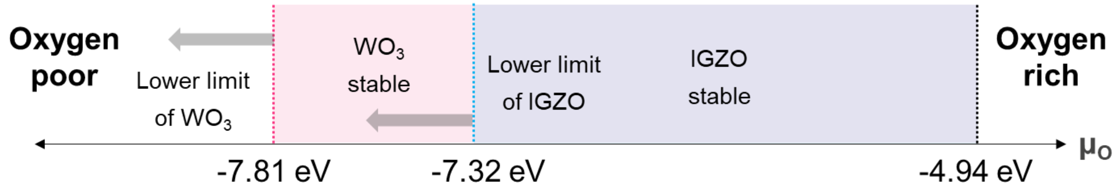
WO_3 μ_O calculation

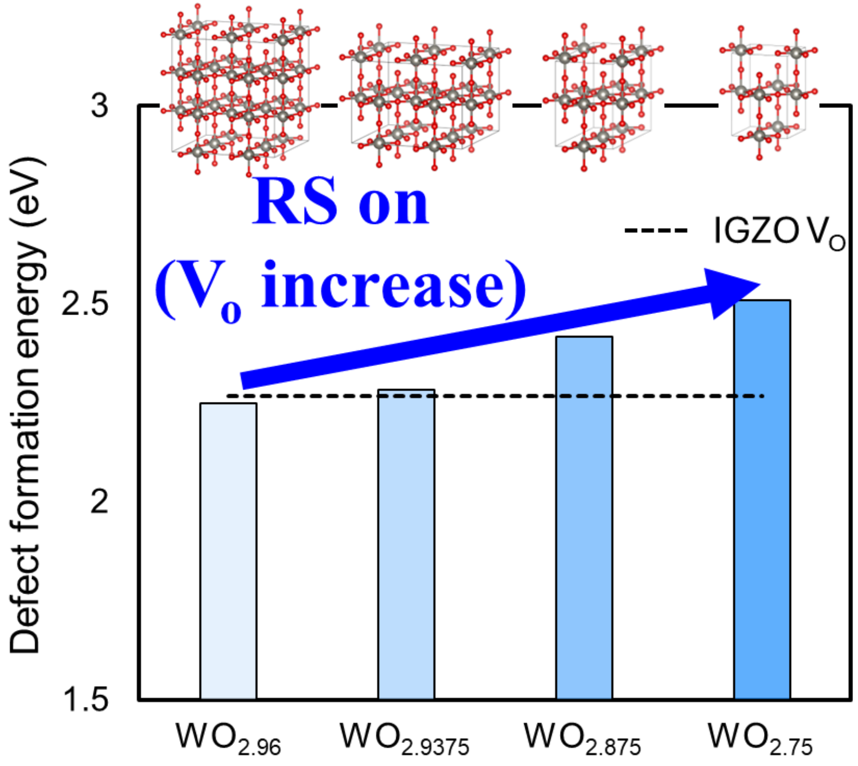
$$\left.\begin{array}{l} Oxygen\ gas \rightarrow E_O < -4.94\ eV \\ \frac{1}{3}(E_{WO_3} - E_W) = -7.77\ eV < E_O \end{array}\right\} WO_3\ \mu_O \rightarrow -7.77\ eV < \mu_O < -4.94\ eV$$

IGZO μ_O calculation

$$\left.\begin{array}{l} E_{InGaZn_2O_5} - (E_{In_2O_3} + E_{ZnO} + E_{ZnGa_2O_4}) < 0.37\ eV \\ E_{ZnO} - E_{Zn} = -7.82\ eV < E_O \\ 1/4\left(E_{ZnGa_2O_4} - E_{Zn} - 2E_{Ga}\right) = -8.14\ eV < E_O \\ 1/3\left(E_{In_2O_3} - 2E_{In}\right) = -7.69\ eV < E_O \end{array}\right\} -7.32\ eV < E_O$$

$$Oxygen\ gas \rightarrow E_O < -4.94\ eV \longrightarrow IGZO\ \mu_O \rightarrow -7.32\ eV < \mu_O < -4.94\ eV$$





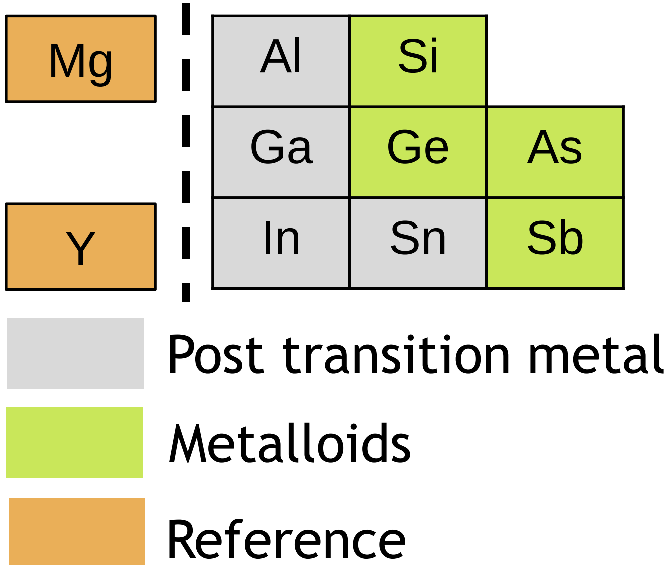
* **DFE** = Defect formation energy

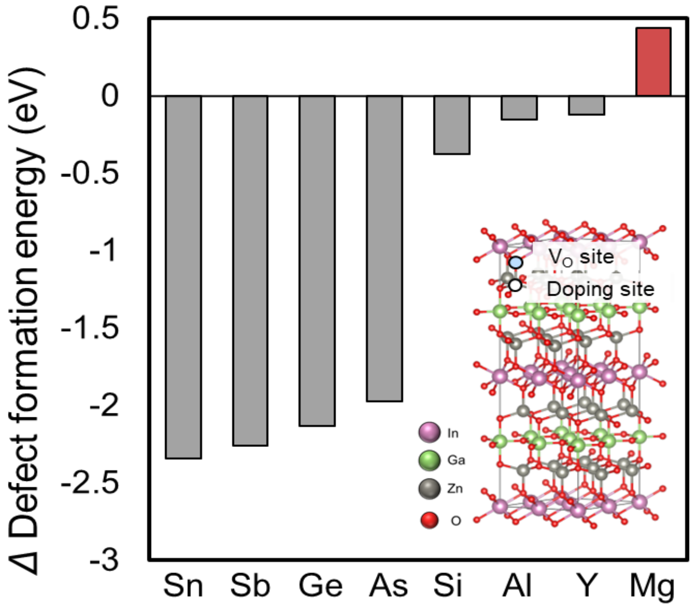
* μ_o = Chemical potential

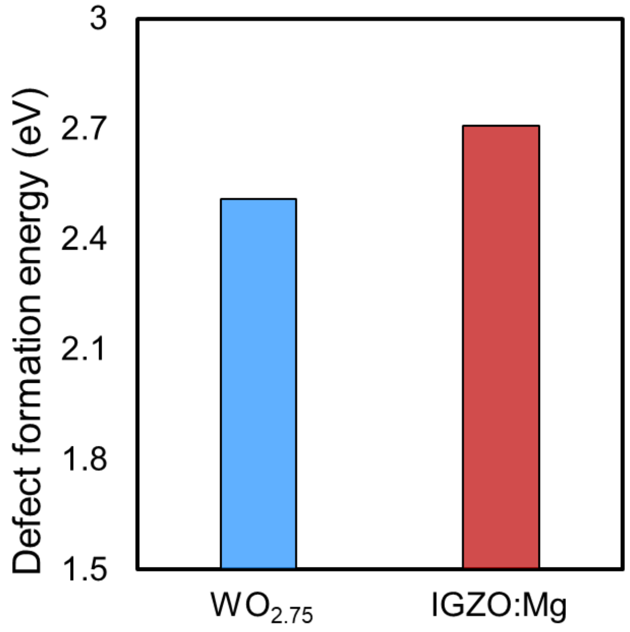
- ✓ Difference of μ_o and DFE can induce the interface layer (IL) between tr and RS layer
- ✓ WO_3 layer is more stable than IGZO transistor based on μ_o and DFE
- ✓ After integration, WO_y IL can be formed between RS and Tr layer

Mg:IGZO based transistor for low R_{int}

Various dopants for IGZO







- ✓ Among various dopants, Mg can be a promising candidate for reducing the IL
- ✓ Difference of DFE between $WO_{2.7}$ and Mg doped IGZO is only 0.2 eV
- ✓ R_{int} can be decreased by Mg doping to the IGZO transistor by reduced IL issue

Outline

- Introduction
- Feasibility of bypass reading in planar structure
- Vertical integration for V-NAND operation
- Memory characteristics of the VB-RRAM
- Interface resistance (R_{int}) issue in the VB-RRAM
- **Conclusion**

Comparison table of V-NAND type memory

	Flash [1]	PCRAM [2]	PCRAM [3]	FeFET [4]	Our work
Mechanism	Charge trap	Phase change	Phase change	Polarization	Electrochemical reaction
V_{prog}	20 V	10 V	20 V	3 V	< 5 V
Speed	100 us	-	0.6 us	1 us	50 us
On/off (MW)	10^5 (5.6 V)	10	100	10^4 (2.5 V)	10^6 (> 5 V)
Endurance	10^4	10^6	10^5	10^8	10^7
MLC	> 4 bit	1 bit	1 bit	2 bit	> 4 bit

- ✓ High scalability (~ 30 nm)
- ✓ Low voltage operation (< 5 V)
- ✓ Reasonable speed (~ 50 us)
- ✓ High on/off ratio (> 10^6)
- ✓ Stable endurance (> 10^7)
- ✓ MLC operation (> 4 bit)

[1] J. Jang, et al., *VLSI* (2009)
[2] S. Morita et al., *VLSI* (2011)
[3] W. Choi et al., *ACS Appl. Mater* (2023)
[4] M. Kim et al., *Sci. Adv* (2021)

- ✓ We demonstrated the feasibility of interface switching RRAM-based V-NAND
- ✓ VB-RRAM shows the excellent memory characteristics compared to other memories

Summary

- **Excellent memory characteristics of the bypass RRAM**

- Bypass reading between the RS and Tr depending on the resistance (R_{tr} on < R_{RS} on < R_{RS} off < R_{tr} off)
- Low voltage (< 5 V), Stable endurance (> 10^7 cycles), reasonable speed (~ 50 us)
- High scalability (~ 30 nm) and 4-bit operation for high-density memory

- **V-NAND integration issues**

- Isolation layer should be below the 50 nm for high I_{on} (> 10 uA)
- Almost no read disturbance issues (~ 2 % state loss)

- **Remain issues in VB-RRAM**

- R_{int} between RS and Tr should be reduced for accurate reading of RS states ($2\ R_{tr} + 2\ R_{int} < R_{RS}$ on)
- Mg: IGZO can be a promising candidate for the low R_{int} with WO_3 based RS layer

Thank you for your attention

Acknowledgement: This work was supported by the Samsung Electronics Co., LTD (IO211115-09118-01)