Low Latency Wide IO DRAM Specification

Date: 2022/05/03

Revision History

Revision	Date	Description
0.0	05/03/2022	First version for target specification

Contents

1. General Description 5
1.1. Key Feature List 5
1.2. Comparison between LPDDR4X and LPDDR5 6
1.3. Command Set 6
2. Die Outline 8
2.1. Block Diagram 8
2.2. Die Floor Plan 8
2.3. Bump Map 9
2.4. Pad Layout Requirements 9
2.5. Alignment Mark, Scribe Lane and Seal Ring Requirements 10
3. Pad Definition and Description 12
3.1. Pin Definition 12
4. Functional Description 14
4.1. State Diagram 14
4.2. Multi-Channel and Slice Operation 14
4.3. Power-up, Initialization, Power-off Procedures 15
4.4. Half DQ Mode 15
4.5. Mode Register Assignment Table 15
4.6. Detailed Mode Register Settings 16
4.6.1. MR0 Register information – TBD 16
4.6.2. MR1 Register information – Read Preamble 16
4.6.3. MR2 Register information – RL/WL Offset, Early CS 16
4.6.4. MR3 Register information – STU, Operating Speed, tRCW offset 17
4.6.5. MR4 Register information – Refresh rate, TUF 17
4.6.6. MR5 Register information – Manufacturer ID 18
4.6.7. MR6 Register information – Revision ID 1 18
4.6.8. MR7 Register information – Revision ID 2 18
4.6.9. MR8 Register information – Type, Density, IO width. 18
4.6.10. MR9 Register information – Vendor Specific Test Mode 19
4.6.11. MR10 Register information – ZQ Calibration code 19
4.6.12. MR11 Register information – DS, PPR-Ch, PPRE, CBT, RPT, Write leveling 19
4.6.13. MR12 Register information – Vref CA setting 19
4.6.14. MR14 Register information – Vref DQ setting 20
4.6.15. MR15 Register information – DQS Oscillator count start 21
4.6.16. MR16 Register information – DQS Oscillator count stop 21
4.6.17. MR17 Register information – DQS interval timer setting 21
4.6.18. MR18 Register information – DQS Oscillator count LSB 22
4.6.19. MR19 Register information – DQS Oscillator count MSB (Same as LPDDR4) 22
4.6.20. MR24 Register information – MAC Value (# of Active Counter for Row hammer) 22
4.6.21. MR47 Register information – PPR Resource 22
5. Command Definition and AC Timing 24
5.1. Command Truth Table 24
5.2. Read 25

5.2.1. Read Post-amble to Pre-amble Merge Behavior 26
5.3. Write 26
5.3.1. Write Post-amble to Pre-amble Merge Behavior 27
5.3.2. Masked Writes and ECC 27
5.4. Mode Register Read 28
5.5. Mode Register Write 29
5.6. Refresh 29
5.6.1. Row Hammer Mitigation 30
5.6.1.1. Sub-bank Based Special Row Hammer Refresh Command 30
5.6.1.2. Bank Based Special Row Hammer Refresh Command 30
5.7. Power Down Entry and Exit 30
5.8. Self Refresh Entry and Exit 31
5.9. Early CS Mode Option 31
5.10. Input Clock Frequency Change 32
5.11. Training and Calibration Requirements 32
5.11.1. ZQ Calibration 32
5.11.2. CBT (Command Bus Training) 33
5.11.3. Write Leveling 34
5.11.4. Read/Write DQ training 34
5.11.5. Write training Voltage/Temp variation compensation with DQS oscillator 36
5.12. Timing Parameters 37
5.13. Command to Command Timing Rules 38
6. Absolute Maximum DC Rating 39
7. AC and DC Operating Condition 40
7.1. Supply Voltage Requirements 40
7.2. Temperature Requirements 40
7.3. Signaling Requirements 40
7.4. ESD and Latch-up Requirements 41
8. IDD Specification Parameters 43
8.1. Low Latency Wide IO IDD Definitions 43
8.2. IDD spec table 43
9. Testability and Repair Requirements 46
9.1. Boundary Scan 46
9.2. Direct Access 47
9.3. Lane Repair 48
9.3.1. Lane Repair Procedure 49
9.4. Post Package Repair (PPR) 49
9.4.1. PPR procedure 49
9.5. Production Test 50

1. General Description

1.1. Key Feature List

- Total capacity: 256MB
- Total peak bandwidth: 128GB/sec (x512)
- Four independent channels per die
- Two data slices per channel
  - Dedicated DQ pins per data slice
  - Shared command pins among data slices in same channel
  - Both command and data running at DDR data rate of 2Gbps
  - Different data slices may execute overlapping Read or Write commands
- Eight banks per data slice:
  - Page size: 1KB
  - Prefetch size: 64B every 4tCK
  - Supports 64B, 128B, and 256B data bursts on the fly
- Refresh:
  - Auto refresh is per data slice only. All banks in a given data slice are refreshed with one refresh command
  - Self-refresh is per channel
  - Optimized refresh scheme supported
- Closed-page operation without any explicit activate/precharge commands
- On-die ECC support w/ 16B data sectors and one-bit correct scheme
- Masked-Write support with 16B minimum granularity (no internal RMW for ECC)
- Small memory tiles compared to commodity DRAM
- Early CS mode option to improve idle power

1.2. Comparison between LPDDR4X and LPDDR5

Table 1.1. Comparison between LPDDR4X and LPDDR5

	Items	LPDDR4X	LPDDR5	Low Latency Wide IO DRAM
Feature	CLK scheme	Differential (CLK/CLKB)	Differential (CLK/CLKB)	Differential (CLK/CLKB)
	Data scheme	DDR Single ended, Bi-Directional	DDR Single ended, Bi-Directional	DDR Single ended, Bi-Directional
	DQS scheme	Differential (DQS/DQSB) Bi-Directional	Support RDQS Differential(RDQS/RDQSB) Bi-Directional	Differential (DQS/DQSB) Bi-Directional
	ADD / CMD scheme	SDR	DDR	DDR
	Operation Policy (Opened page / Clopsed page)	Support both	Support both	Support closed page only
	I/O Interface	LVSTL_0.6V	LVSTL_0.5V	LVSTL_0.6V
	Burst Length	16, 32 (OTF)	16, 32 (OTF)	8, 16, 32 (OTF)
	Burst Type	Sequential	Sequential	Sequential
	# of Bank per Ch.	8	8 or 16B or 4B/4BG	16 (8bank per data slice)
	Organization per Ch.	x8, x16	x8, x16	x64, x128 (x32, x64 per data slice)
	Data Mask	Support (Masked Write)	Support (Masked Write)	Support (Masked Write)
	Refresh mode	Auto / Self Refresh	Auto / Self Refresh	Auto / Self Refresh
	DBI	Support	Support	N/A
	Speed bin [Mbps]	3200/3733/4266	5500/6400	2000
	tRC	63ns (tRC, Act to Act delay)	63ns (tRC, Act to Act delay)	32ns (tRCW, ACT-WR-PRE-ACT)
Special Function	ZQ Calibration	Support	Support	Support
	Write Leveling	Support	Support	Support
Power Supply	VDD1 [V]	1.70 ~ 1.95	1.70 ~ 1.95	1.70 ~ 1.95
	VDD2/2H [V]	1.06 ~ 1.17	1.01 ~ 1.12	0.97 ~ 1.07
	VDD2L [V]	N/A	0.87 ~ 0.97	N/A
	VDDQ [V]	0.57 ~ 0.65	0.47 ~ 0.55	0.57 ~ 0.65

1.3. Command Set

Command set resembles LPDDR style command definition. A key exception is that no activation or precharge commands are used. They will be implicit within Read and Write commands (closed page memory operation only). All configuration and test mode settings are handled via MRW (Mode Register Write) and MRR (Mode Register Read). Table 1.2 shows a list of all valid Low Latency Wide IO commands.

Table 1.2. Command List

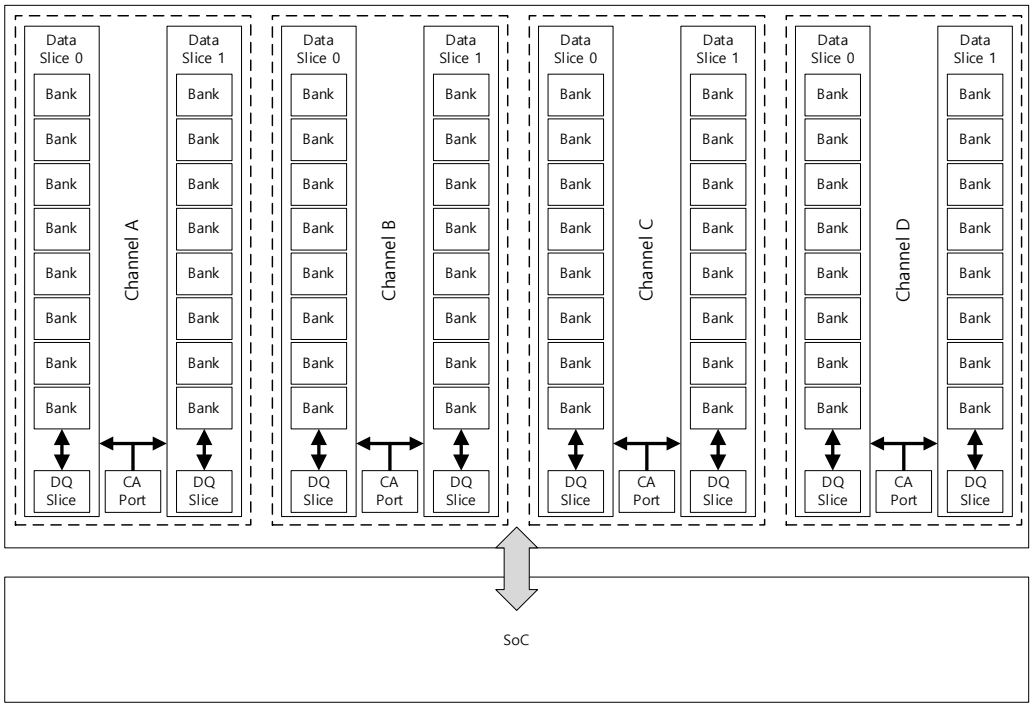
Command	Description
Read	Active page; Reads 64B/128B/256B on the fly; Precharges page
Write	Active page; Writes 64B/128B/256B on the fly; Precharges page Same command supports both masked writes
Refresh	Refreshes all banks in a given data slice (no per bank refresh supported)
MRW	Writes a given Mode Register
MRR	Reads a given Mode Register
SREF Entry	Enters channel into self-refresh state
PD Entry	Enters channel into power-down state

PD or SREF Exit	Exits channel from either SREF or PD state
NOP	Explicit NOP command

2. Die Outline

2.1. Block Diagram

Figure 2.1. Conceptual Block Diagram



2.2. Die Floor Plan

Figure 2.2 shows the outline of Low Latency Wide IO die and arrangement of channels, slices, and banks. Overall physical dimensions of Low Latency Wide IO die shall comply with width and height as specified in this figure. Die width and height are defined by seal ring stepping distance. Bump area for Low Latency Wide IO to SoC connections has a shoreline of 4.402mm and is located at the bottom center of the die.

Figure 2.2. Low Latency Wide IO Die Floor Plan with Bumps Facing Up

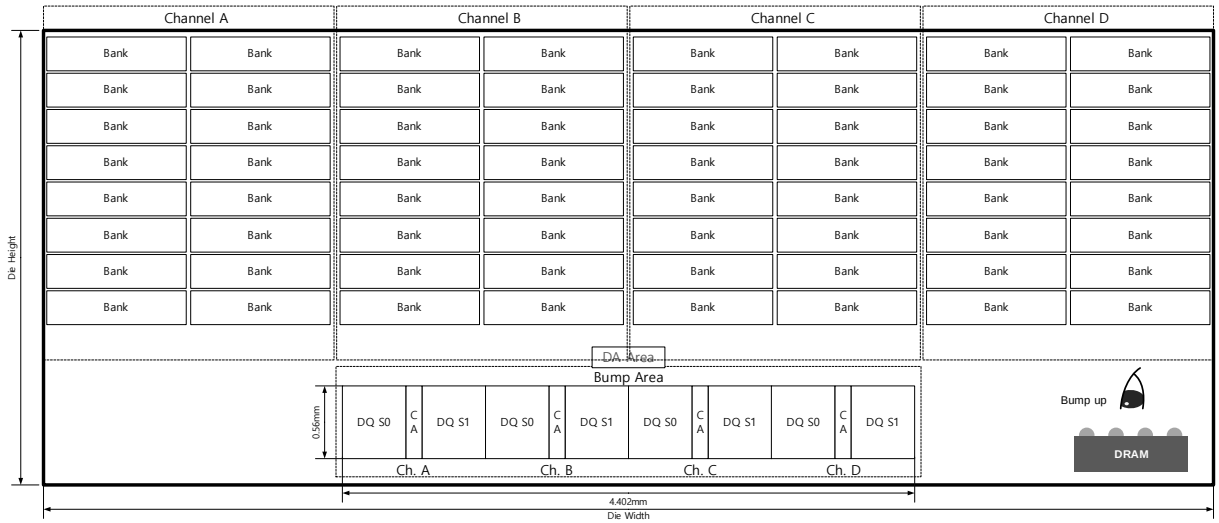


Figure 2.3. Low Latency Wide IO Power Bump Regions with Bumps Facing Up

TBD

2.3. Bump Map

Figure 2.4 shows the physical requirement for the bump area. Bumps shall have vertical pitch of 40um and a horizontal pitch of 62um and follow the bump to signal assignments as specified in this figure. Additional testing pins that contain boundary scan and direct access are shown in Figure 2.5. Bump coordinates for all Low Latency Wide IO bumps are listed in Appendix A. No additional bumps permitted unless listed. Bump coordinates are hard requirements with the exception of power and ground groups as defined in Figure 2.3.

Figure 2.4. Bump map for Low Latency Wide IO Channel0 with bumps facing up

	Channel 0																	
	Pseudo Channel S0								CA		Pseudo Channel S1							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1
B	0_S0_DQ7	0_S0_DQ8	0_S0_DQ23	0_S0_DQ24	0_S0_DQ39	0_S0_DQ40	0_S0_DQ55	0_S0_DQ56	0_CA0	0_CA1	0_S1_DQ7	0_S1_DQ8	0_S1_DQ23	0_S1_DQ24	0_S1_DQ39	0_S1_DQ40	0_S1_DQ55	0_S1_DQ56
C	0_S0_DQ6	0_S0_DQ9	0_S0_DQ22	0_S0_DQ25	0_S0_DQ38	0_S0_DQ41	0_S0_DQ54	0_S0_DQ57	0_CA2	0_CA3	0_S1_DQ6	0_S1_DQ9	0_S1_DQ22	0_S1_DQ25	0_S1_DQ38	0_S1_DQ41	0_S1_DQ54	0_S1_DQ57
D	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ
E	0_S0_DQ5	0_S0_DQ10	0_S0_DQ21	0_S0_DQ26	0_S0_DQ37	0_S0_DQ42	0_S0_DQ53	0_S0_DQ58	0_CS	0_CA8	0_S1_DQ5	0_S1_DQ10	0_S1_DQ21	0_S1_DQ26	0_S1_DQ37	0_S1_DQ42	0_S1_DQ53	0_S1_DQ58
F	0_S0_DQ4	0_S0_DQ11	0_S0_DQ20	0_S0_DQ27	0_S0_DQ36	0_S0_DQ43	0_S0_DQ52	0_S0_DQ59	VDD2	0_CA11	0_S1_DQ4	0_S1_DQ11	0_S1_DQ20	0_S1_DQ27	0_S1_DQ36	0_S1_DQ43	0_S1_DQ52	0_S1_DQ59
G	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2	NP	NP	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2
H	0_S0_DQ3	0_S0_DQS_c	0_S0_DQ19	0_S0_DQ28	0_S0_DQ35	0_S0_DQS_c	0_S0_DQ51	0_S0_DQ60	0_CK_C	0_CA10	0_S1_DQ3	0_S1_DQS_c	0_S1_DQ19	0_S1_DQ28	0_S1_DQ35	0_S1_DQS_c	0_S1_DQ51	0_S1_DQ60
J	0_S0_DQ2	0_S0_DQS_t	0_S0_DQ18	0_S0_DQ29	0_S0_DQ34	0_S0_DQS_t	0_S0_DQ50	0_S0_DQ61	0_CK_T	0_CA9	0_S1_DQ2	0_S1_DQS_t	0_S1_DQ18	0_S1_DQ29	0_S1_DQ34	0_S1_DQS_t	0_S1_DQ50	0_S1_DQ61
K	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS
L	0_S0_DQ1	0_S0_DQ12	0_S0_DQ17	0_S0_DQ30	0_S0_DQ33	0_S0_DQ44	0_S0_DQ49	0_S0_DQ62	VDD2	0_CKE	0_S1_DQ1	0_S1_DQ12	0_S1_DQ17	0_S1_DQ30	0_S1_DQ33	0_S1_DQ44	0_S1_DQ49	0_S1_DQ62
M	0_S0_DQ0	0_S0_DQ13	0_S0_DQ16	0_S0_DQ31	0_S0_DQ32	0_S0_DQ45	0_S0_DQ48	0_S0_DQ63	0_CA7	0_CA5	0_S1_DQ0	0_S1_DQ13	0_S1_DQ16	0_S1_DQ31	0_S1_DQ32	0_S1_DQ45	0_S1_DQ48	0_S1_DQ63
N	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDDQ	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2
P	0_S0_DQ14	NP	0_S0_DQ15	0_S0_DM	0_S0_DQ46	NP	0_S0_DQ47	NP	0_CA6	0_CA4	0_S1_DQ14	NP	0_S1_DQ15	0_S1_DM	0_S1_DQ46	NP	0_S1_DQ47	NP
R	VSS	VDDQ	0_S0_R0_E	0_S0_R0_O	VSS	VDDQ	0_S0_R1_E	0_S0_R1_O	NP	NP	VSS	VDDQ	0_S1_R0_E	0_S1_R0_O	VSS	VDDQ	0_S1_R1_E	0_S1_R1_O
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Figure 2.5. Bump map for Low Latency Wide IO Direct Access (DA) Port

TBD (Around 50pcs pin will be placed)

2.4. Pad Layout Requirements

All pad designs shall follow the same basic cell structure, an example of which is shown in Figure 2.6. PIQ layer shall always cover AP sidewall. AP CD for regular pads is a recommended value only. Proper sizing of AP CD inline with the hard requirement for PIQ CD shall be ensured.

For wafer level probing, dedicated probe pads are required with its own separate pad design. The sizing of these pads is decided by vendor requirements and the CD in table xx is provided for reference. Minimum spacing between AP, seal ring, probe pad are illustrated in Figure 2.6 and listed in Table 2.1.

Figure 2.6. Pad Rules

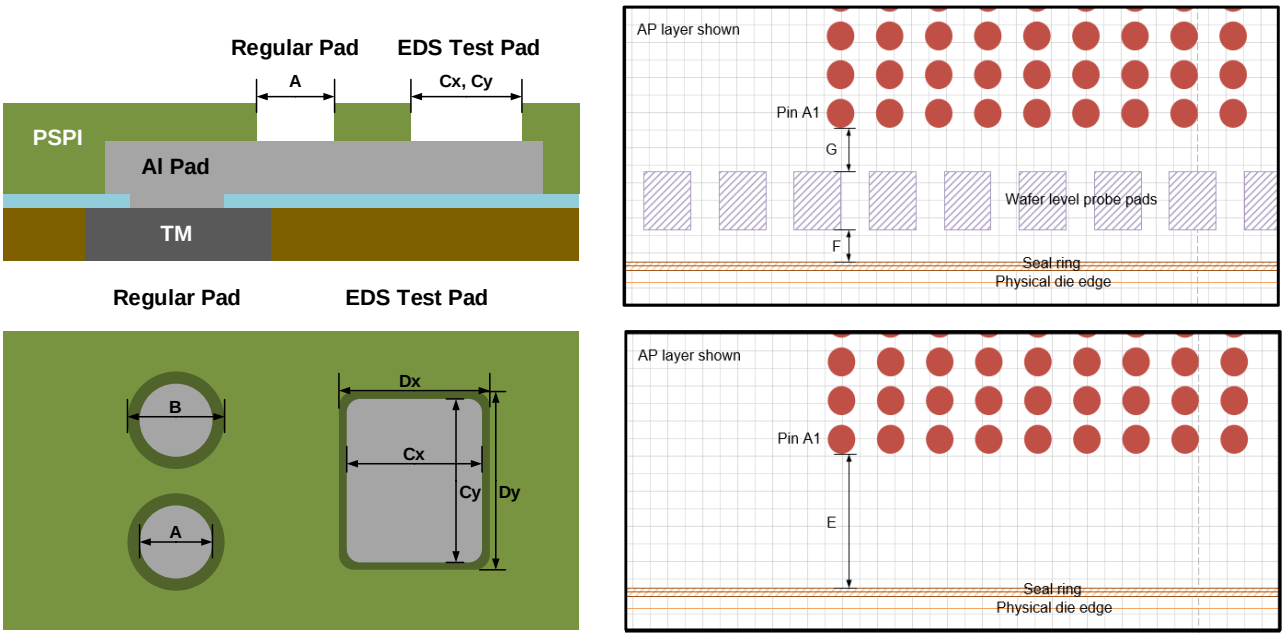


Table 2.1. AP Pad Requirements

No	Description	Label	Rule	Comments
1	Circular shape of PIQ (polymer) opening is required			
2	PIQ CD (Regular pad)	A	= 17um	Hard requirement
3	AP CD (Regular pad)	B	= 28um	Recommendation
4	PIQ CD (Dedicated probe pad)	Cx / Cy	= 50um x 60um	Vendor requirement
5	AP CD (Dedicated probe pad)	Dx / Dy	=56um x 66um	Vendor requirement
6	All PIQ openings on die must be included in mcm design file			
7	Pads dedicated for probing must be identified in mcm design file			
8	AP spacing to seal ring	E	>= 55um	
9	Probe pad spacing to seal ring (AP layer)	F	>= 20um	
10	Bump PIQ edge spacing to probe pad PIQ edge	G	>= 36um	

2.5. Alignment Mark, Scribe Lane and Seal Ring Requirements

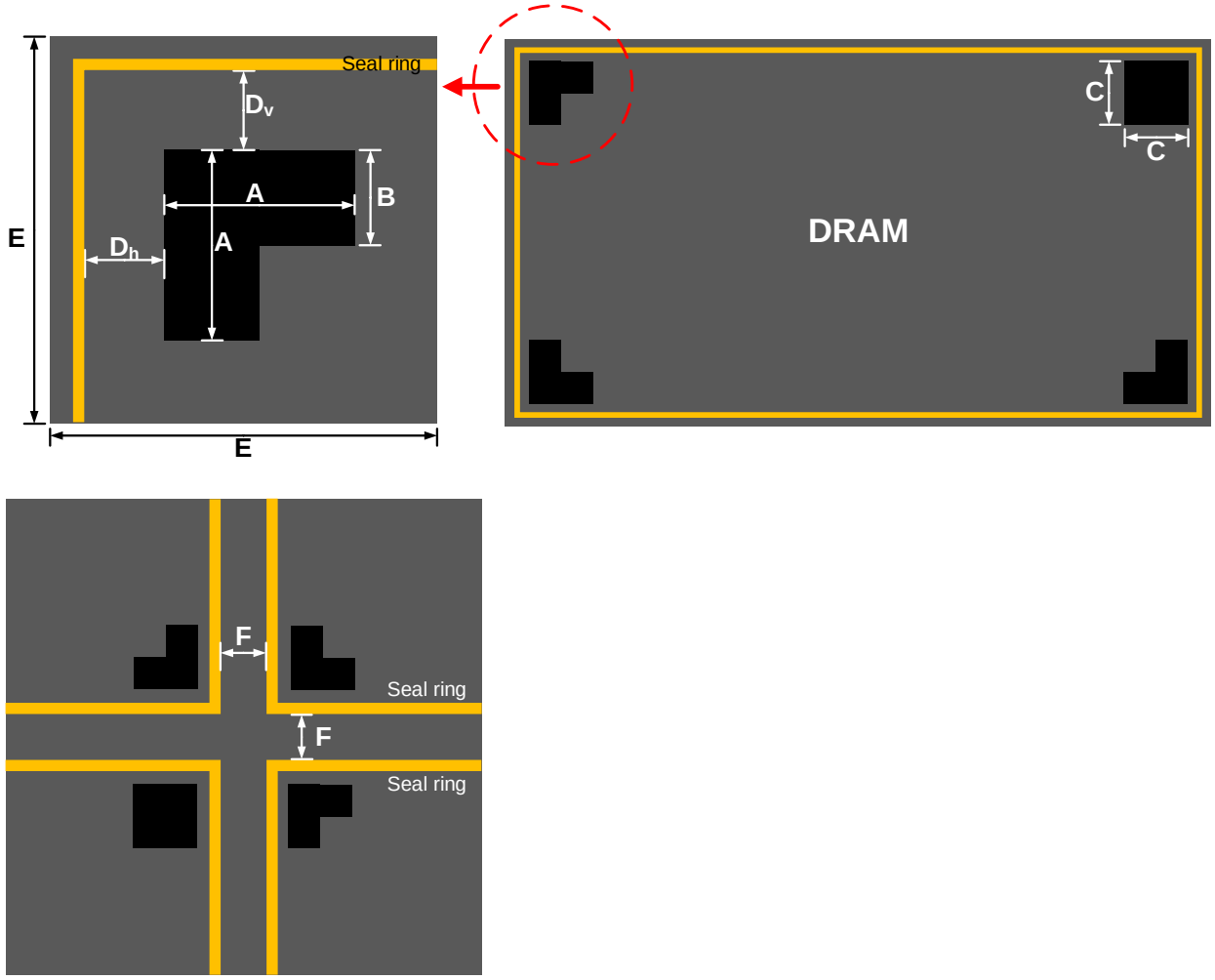
Recommended alignment mark reference design is provided in Figure 2.7.

Table 2.2. Scribe and Alignment Mark Rules

No	Description	Label	Rule
1	L-Shaped alignment marks on 3 die corners and square mark on the last corner		
2	L-Shaped alignment mark dimension A	A	= 62 um
3	L-Shaped alignment mark dimension B	B	= 30um
4	Rectangle alignment mark dimension	C	= 62um

5	Alignment mark to seal ring distance	D_v D_h	= 43um vertical, = 49um horizontal
6	Routing forbidden zone for L-shaped alignment mark (all layers)	E	= 80um
7	Scribe lane width (from seal ring to seal ring)	F	>= 70um (TBD)

Figure 2.7. Scribe Lane and Alignment Mark Rules



3. Pad Definition and Description

3.1. Pin Definition

Low Latency Wide IO die has a total of 684 signal pins. There are four groups of 162 pins per each channel as detailed in Table 3.1.

Table 3.1. Signal pins per each channel

Port	Pin Name	Type	Description	Count	Nominal Signaling Levels
Command	CK_t, CK_c	Input	Differential Clock	2	VSS - VDDQ
	CKE	Input	Clock Enable, SDR signal	1	VSS - VDD2
	CS	Input	Chip Select, SDR signal	1	VSS - VDDQ
	CA [11:0]	Input	Command/Address inputs, DDR signal	12	VSS - VDDQ
Data Slice 0	DQ_S0 [63:0]	IO	Bidirectional DDR data input/output pins. BL=8, 16, 32 for 64B, 128B, 256B accesses respectively.	64	VSS - VDDQ
	DQS_S0_t [1:0] DQS_S0_c [1:0]	IO	Bidirectional differential DQ Strobes. One pair of differential strobes per every 32 DQ's.	4	VSS - VDDQ
	DM_S0	IO	Data Mask Input. DDR. No DBI supported. DM pin shall be in DQS_S0_t/c[0] domain.	1	VSS - VDDQ
	RDQE_S0 [1:0] RDQO_S0 [1:0]	IO	Redundant DQ's. One pair of even/odd redundant DQ's per each DQS domain.	4	VSS - VDDQ
Data Slice 1	DQ_S1 [63:0]	IO	Bidirectional DDR data input/output pins. BL=8, 16, 32 for 64B, 128B, 256B accesses respectively.	64	VSS - VDDQ
	DQS_S1_t [1:0] DQS_S1_c [1:0]	IO	Bidirectional differential DQ Strobes. One pair of differential strobes per every 32 DQ's.	4	VSS - VDDQ
	DM_S1	IO	Data Mask Input. DDR. No DBI supported. DM pin shall be in DQS_S1_t/c[0] domain.	1	VSS - VDDQ
	RDQE_S1 [1:0] RDQO_S1 [1:0]	IO	Redundant DQ's. One pair of even/odd redundant DQ's per each DQS domain.	4	VSS - VDDQ
Total signal count per channel : 162					

There are 36 signal pins shared among all four channels as detailed in Table 3.2.

Table 3.2. Signal pins shared among channels

Pin Name	Type	Description	Count	Nominal Signaling Levels
Reset_n	Input	RESET: When asserted LOW, the RESET_n signal resets all channels of the die	1	VSS - VDD2
ZQ	Reference	Calibration Reference: Used to calibrate the output drive strength. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor.	1	Analog
SEN [1:0]	Input	Boundary Scan Enable: When SEN[0] is enabled, only boundary scan operations is available through all channels. SEN[0] must be routed directly to external package I/O pads to allow un-buffered access to these signals.	2	VSS - VDD2
SSH	Input	Boundary Scan Shift: There is one SSH provided to channels. SSH must be routed directly to external package I/O pads to allow un-buffered access to these signals.	1	VSS - VDD2

SDI	Input	Boundary Scan Serial Data In: There is one SDI provided to input the boundary scan data. SDI must be routed directly to external package I/O pads to allow un-buffered access to these signals.	1	VSS - VDDQ
SCK	Input	Boundary Scan Clock: There is one SCK provided to all channels. SCK must be routed directly to external package I/O pads to allow un-buffered access to these signals.	1	VSS - VDDQ
SDO	Output	Boundary Scan output: There is one SDO to check serialized output data. SDO must be routed directly to external package I/O pads to allow un-buffered access to these signals.	1	VSS - VDDQ
DAEN_DA Reset_n_DA CKE_DA	Input	Direct Access: These I/O pins provide digital direct access to internal DRAM core signals for test/debug purposes. DA pins must be routed directly to external package I/O pads to allow un-buffered access to these signals. When DAEN input is High and DA port is enabled, all non-DA signal pins are in high-Z and must be ignored including Reset_n. When DAEN is Low, All other DA pins must be in high-Z and ignored.	3	VSS - VDD2
CA_DA[11:0] CK_t/c_DA CS_DA[3:0] DQS_t/c_DA DQ_DA[3:0] DM_DA	IO		TBD	VSS - VDDQ
Total signal count (excluding power/GND): 36				

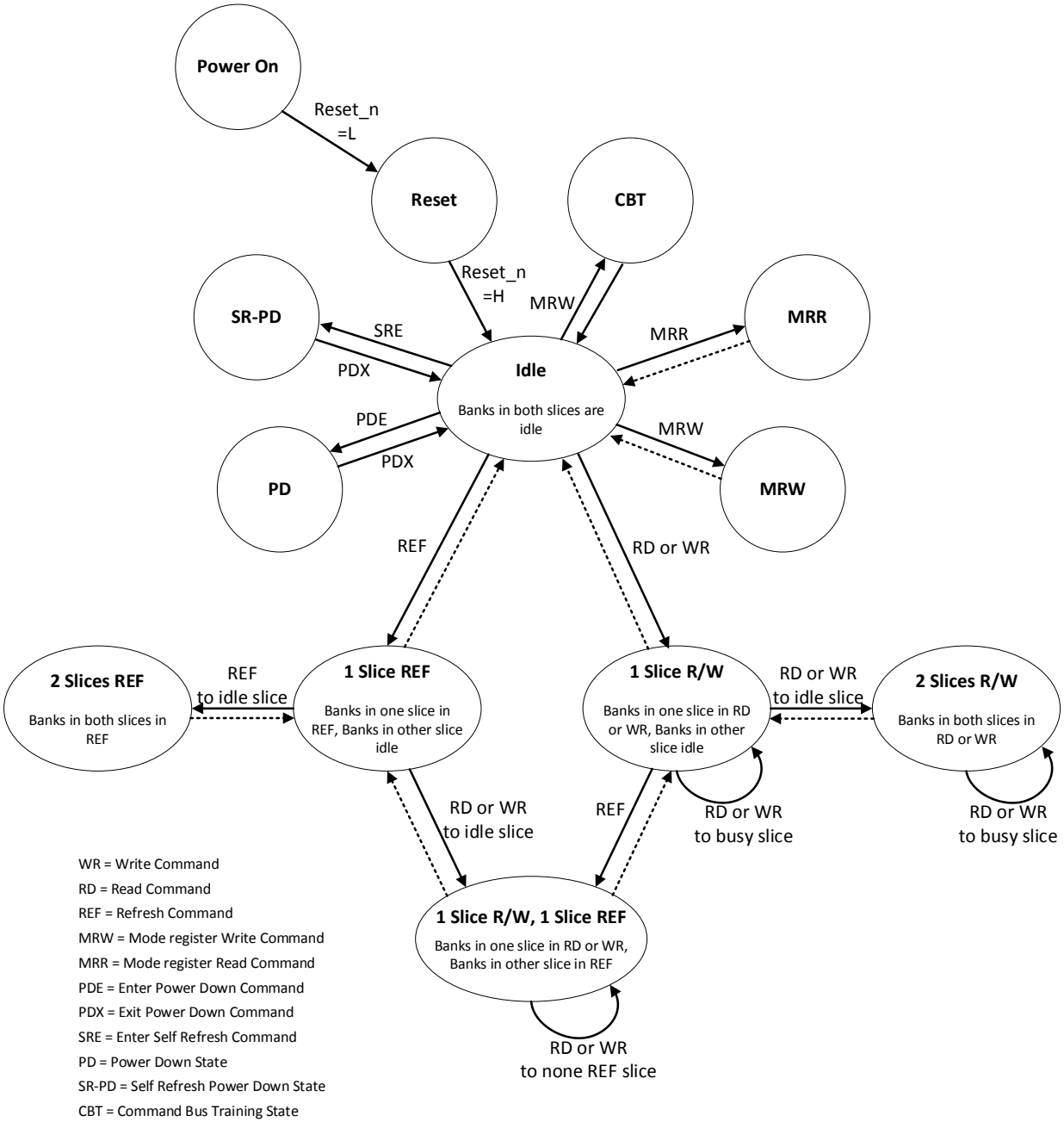
Table 3.3. Power and ground pins shared among channels (Target)

Pin Name	Type	Description	Count
VDD1	Power	Power supplies	18
VDD2	Power		119
VDDQ	Power		128
VSS	GND	Ground and IO Ground	225
Total power/GND pin count : 490			

4. Functional Description

4.1. State Diagram

Figure 4.1. Low Latency Wide IO State Diagram for Each Channel

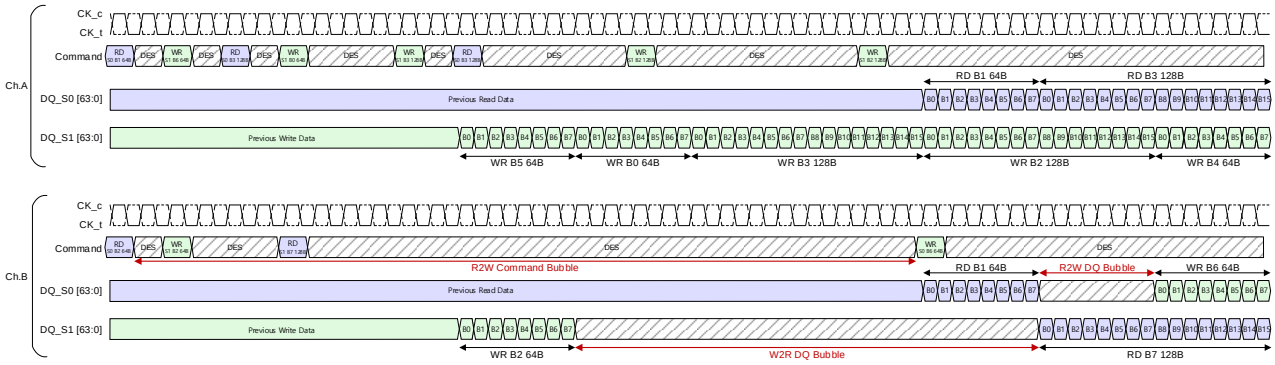


4.2. Multi-Channel and Slice Operation

Figure 4.2 shows an example timing diagram for how two data slices in two channels can operate. Each command requires one cycle and commands to different slices in the same channel can be issued every other cycle. Although not strictly required, a round robin approach can be used to issue a new transaction to the same data slice every four clock cycles as shown. In this example, Channel A data slice 0 performs a sequence of gapless read transactions of varying burst lengths (64B and 128B). Concurrently, channel A data slice 1 performs a sequence of gapless write transactions of varying burst lengths. Channel B slice

0 in this example switches from performing read transactions to performing write transactions. Such a read to write turn results in a “R2W command bubble” in command sequence and a “R2W DQ bubble” as shown. Channel B data slice 1 in this example performs a write to read turn switching from write transactions to read transactions. Such a write to read turn results in a “W2R DQ bubble” on channel B slice 1 DQ bus as shown. More detailed timing diagrams and timing specifications are described in Section Chapter 5, Command Definition and AC Timing.

Figure 4.2. Example of multi-channel and multi-slice operation



4.3. Power-up, Initialization, Power-off Procedures

Low Latency Wide IO power-up, initialization, and power-off procedures shall follow the same exact requirements as LPDDR4, which are specified in Section 3.3 of JEDEC document JESD209-4A.

4.4. Half DQ Mode

TBD

4.5. Mode Register Assignment Table

Table 4.1. Mode Register Assignments

MR # MA[5:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
00, 0x00	R	RFU							
01, 0x01	W	RFU							RD-PRE
02, 0x02	W	Early CS		WL offset			RL offset		
03, 0x03	W	RFU			Operating Speed			tRCW offset	
04, 0x04	R	TUF	RFU				Refresh rate		
05, 0x05	R	Manufacture ID							
06, 0x06	R	Revision ID 1							
07, 0x07	R	Revision ID 2							
08, 0x08	R	IO width		Density				Type	
09, 0x09	W	Vendor Specific Test Mode							
10, 0x0A	W	ZQ Cal start : 0xFF, ZQ Cal Latch : 0xBB, ZQ Reset : 0xC3							

11, 0x0B	W	WR Leveling	RPT	CBT	PPRE	LRE	RFU	Driver Strength
12, 0x0C	R/W	RFU		Vref (CA)				
13, 0x0D	N/A	RFU						
14, 0x0E	R/W	RFU		Vref (DQ)				
15, 0x0F	W	DQS OSC Count Start						
16, 0x10	W	DQS OSC Count Stop						
17, 0x11	W	DQS OSC Interval Timer Run Time Setting						
18, 0x12	R	DQS OSC Count - LSB						
19, 0x13	R	DQS OSC Count - MSB						
20:23	N/A	RFU						
24, 0x18	R	RFU			ARHM - MAC Value			RFU
25:37	N/A	RFU						
38:46	N/A	Do Not Use						
47, 0x2F	R	PPR Resource						

4.6. Detailed Mode Register Settings

4.6.1. MR0 Register information – TBD

TBD

4.6.2. MR1 Register information – Read Preamble

Table 4.2. MR1 Register information – Read Preamble

Function	Register Type	Operand	Data	Notes
RD-PRE (Read Preamble Type)	W	OP[0]	0b0: Read Preamble = 1 tCK static + 1 tCK toggle (Default) 0b1: Read Preamble = 2 tCK toggle	1

Notes:

1. For Read operations this bit must be set to select between a "static" pre-amble and a mixed Preamble.

4.6.3. MR2 Register information – RL/WL Offset, Early CS

Table 4.3. MR2 Register information – RL/WL Offset, Early CS Mode

Function	Register Type	Operand	Data	Notes
RL and MRR_RL offset at 2Gbps	W	OP[2:0]	0b000: Reserved 0b001: RL offset = 0 (Default) 0b010: RL offset = +1 0b011: RL offset = +2 0b100: RL offset = +4	1,2
WL offset at 2Gbps		OP[5:3]	0b000: Reserved 0b001: WL offset = 0 (Default) 0b010: WL offset = +1 0b011: WL offset = +2 0b100: WL offset = +3	1,2

Early CS		OP[7:6]	0b00: Disable Early CS (Default) 0b01: Enable Early CS – 4tCK ahead 0b10: Enable Early CS – TBD tCK ahead 0b11: Reserved	

Notes:

1. MRR_RL, RL and WL offset specified in MR2 OP[2:0] and OP[5:3] are only available to apply at the full speed (2Gbps). For other operating speeds (1Gbps, 100Mbps), only the default value applies regardless of offset setting.

2. RL and WL can be modified with the setting of MR2 OP[2:0] and OP[5:3]. For example, if MR2 OP[2:0] = 0b100 and MR2 OP[5:3] = 0b010, RL and WL will be set to 28 and 9, respectively. (RL is 28 = 26 + 2, WL is 9 = 9 + 0)

4.6.4. MR3 Register information – STU, Operating Speed, tRCW offset

Table 4.4. MR3 Register information – STU, Operating Speed, tRCW offset

Function	Register Type	Operand	Data	Notes
tRCW offset enable	W	OP[1:0]	0b00: tRCW = 28ns + BL/2 (Default) 0b01: tRCW = 28ns + BL/2 + 8ns All Others : Reserved	2
Operating Speed		OP[4:2]	0b000: <100Mbps, WL = 2, RL = 8 (Default) 0b001: 1Gbps, WL = 4, RL = 14 0b010: 2Gbps, WL = 9, RL = 26 All Others : Reserved	1

Notes:

1. When OP[4:2] = 0b000, Low Latency Wide IO only allows to operate below 100Mbps. It is required to modify MR3 setting to proper state prior to operate the other speeds. For example, set MR3 OP[4:2]=0b010 prior to operate Low Latency Wide IO with 2Gbps.

2. MR for tRCW offset is an optional feature to make sure the core write operation at the cold temperature. Offset value must be <=8ns and the temperature range for which OP[1:0]=0b01 is required must be < 0C.

4.6.5. MR4 Register information – Refresh rate, TUF

Table 4.5. MR4 Register information – Refresh rate, TUF

Function	Register Type	Operand	Data	Notes
Refresh Rate	R	OP[2:0]	0b000: DRAM Low temperature operating limit exceeded 0b001: 4x refresh, Below 0'C 0b010: 4x refresh, Above 0'C 0b011: 2x refresh 0b100: 1x refresh 0b101: 0.5x refresh 0b110: 0.25x refresh 0b111: DRAM High temperature operating limit exceeded	1,2,3,4, 7,8
TUF (Temperature Update Flag)		OP[7]	0b0: No change in OP[2:0] since last MR4 read (default) 0b1: Change in OP[2:0] since last MR4 read	5,6,7

Notes:

1. The refresh rate for each MR4 OP[2:0] setting applies to tREFI and tREFW. OP[2:0]=0b100 corresponds to a device temperature of 85 °C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2:0]=0b101 or higher, the device temperature is greater than 85 °C.

2. At higher temperatures (>85 °C), no AC timing de-rating shall be required.

3. DRAM vendor may or may not report all of the possible settings over the operating temperature range

of the device. The vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.

4. The device may not operate properly when OP[2:0]=0b000 or 0b111.

5. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. Once MR4 OP[2:0] is read, OP[7] will be reset to '0'.

6. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence(Te).

7. See the section on “temperature Sensor” for information on the recommended frequency of reading MR4.

8. When MR4 OP[2:0]=0b001, Low Latency Wide IO controller can enable tRCW offset feature when necessary by setting MR3 OP[1:0]=0b01.

4.6.6. MR5 Register information – Manufacturer ID

Table 4.6. MR5 Register information – Manufacturer ID

Function	Register Type	Operand	Data	Notes
Manufacturer ID	R	OP[7:0}	0b00000001 : Samsung	

4.6.7. MR6 Register information – Revision ID 1

Table 4.7. MR6 Register information – Revision ID 1

Function	Register Type	Operand	Data	Notes
Revision ID 1	R	OP[7:0]	0b00001000 : I-version	1

Notes:

1. MR6 is vendor specific.

4.6.8. MR7 Register information – Revision ID 2

Table 4.8. MR7 Register information – Revision ID 2

Function	Register Type	Operand	Data	Notes
Revision ID 2	R	OP[7:0]	0b00000000 : A-version	1

Notes:

1. MR7 is vendor specific.

4.6.9. MR8 Register information – Type, Density, IO width.

Table 4.9. MR8 Register information – Type, Density, IO width

Function	Register Type	Operand	Data	Notes
Type	R	OP[1:0]	0b00: Low Latency Wide IO 4ch, SDRAM All Others : Reserved	
Density		OP[5:2]	0b000: 2Gb (per die) All Others : Reserved	
IO width		OP[7:6]	0b000: x128 (per channel) 0b001: x64 (per channel) All Others : Reserved	

4.6.10. MR9 Register information – Vendor Specific Test Mode

TBD

4.6.11. MR10 Register information – ZQ Calibration code

Table 4.10. MR10 Register information – ZQ Calibration code

Function	Register Type	Operand	Data	Notes
ZQ Calibration Code	W	OP[7:0]	0xFF: ZQ Calibration Start 0xBB: ZQ Latch 0xC3: ZQ Reset All Others : Reserved	1,2,3,4

Notes:

1. Host processor shall not write MR10 with “Reserved” values.
2. Low Latency Wide IO devices shall ignore calibration command when a “Reserved” value is written into MR10.
3. If ZQ is connected to VDDQ through RZQ, the ZQ calibration Start MRW Command is supported. If ZQ is connected to VSSQ, the device may operate with the calibration command, but ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

4.6.12. MR11 Register information – DS, PPR-Ch, PPRE, CBT, RPT, Write leveling

Table 4.11. MR11 Register information – DS, PPR-Ch, PPRE, CBT, RPT, Write leveling

Function	Register Type	Operand	Data	Notes
DS (Driver Strength)	W	OP[1:0]	0b00: RFU 0b01: RZQ / 2 : 120ohm 0b10: RZQ / 3 : 80ohm – (Default) 0b11: Reserved	1
LRE (Lane Repair Entry)		OP[3]	0b0: Normal Operation (Default) 0b1: Lane Repair Mode	
PPRE (PPR Entry)		OP[4]	0b0: Normal Operation (Default) 0b1: PPR Mode	
CBT Command Bus Training		OP[5]	0b0: Disabled (Default) 0b1: Enabled	
RPT Read Preamble Training		OP[6]	0b0: Disabled (Default) 0b1: Enabled	
WR Leveling		OP[7]	0b0: Disabled (Default) 0b1: Enabled	2

Notes:

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=0b1), Low Latency Wide IO device remains in the MRW state until another MRW command clears the bit (OP[7]=0b0). No other commands are allowed until the Write Leveling Enable bit is cleared.

4.6.13. MR12 Register information – Vref CA setting

Low Latency Wide IO shall support independent Vref CA generator for each channel so that channels can be independently trained. The Vref settling time to +/- 1% accuracy shall be less than 1us for >5-step

change and less than 200ns for 1-step change.

Table 4.12. MR12 Register information – Vref CA setting

Operand	Vref Values (% of VDDQ)							
OP[5:0]	0b 000000	16%	0b 10000	32%	0b 100000	48%	0b 110000	64%
	0b 000001	17%	0b 10001	33%	0b 100001	49%	0b 110001	65%
	0b 000010	18%	0b 10010	34%	0b 100010	50%	0b 110010	66%
	0b 000011	19%	0b 10011	35%	0b 100011	51%	0b 110011	67%
	0b 000100	20%	0b 10100	36%	0b 100100	52%	0b 110100	68%
	0b 000101	21%	0b 10101	37%	0b 100101	53%	0b 110101	69%
	0b 000110	22%	0b 10110	38%	0b 100110	54%	0b 110110	70%
	0b 000111	23%	0b 10111	39%	0b 100111	55%	0b 110111	71%
	0b 001000	24%	0b 11000	40%	0b 101000	56%	0b 111000	72%
	0b 001001	25%	0b 11001	41%	0b 101001	57%	0b 111001	73%
	0b 001010	26%	0b 11010	42%	0b 101010	58%	All Others Reserved	
	0b 001011	27%	0b 11011	43%	0b 101011	59%		
	0b 001100	28%	0b 11100	44%	0b 101100	60%		
	0b 001101	29%	0b 11101	45%	0b 101101	61%		
	0b 001110	30%	0b 11110	46%	0b 101110	62%		
	0b 001111	31%	0b 11111	47%	0b 101111	63%		

4.6.14. MR14 Register information – Vref DQ setting

Low Latency Wide IO shall support independent Vref DQ generator for each channel so that channels can be independently trained. The Vref settling time to +/- 1% accuracy shall be less than 1us for >5-step change and less than 200ns for 1-step change.

Operand	Vref Values (% of VDDQ)							
OP[5:0]	0b 000000	16%	0b 10000	32%	0b 100000	48%	0b 110000	64%
	0b 000001	17%	0b 10001	33%	0b 100001	49%	0b 110001	65%
	0b 000010	18%	0b 10010	34%	0b 100010	50%	0b 110010	66%
	0b 000011	19%	0b 10011	35%	0b 100011	51%	0b 110011	67%
	0b 000100	20%	0b 10100	36%	0b 100100	52%	0b 110100	68%
	0b 000101	21%	0b 10101	37%	0b 100101	53%	0b 110101	69%
	0b 000110	22%	0b 10110	38%	0b 100110	54%	0b 110110	70%
	0b 000111	23%	0b 10111	39%	0b 100111	55%	0b 110111	71%
	0b 001000	24%	0b 11000	40%	0b 101000	56%	0b 111000	72%
	0b 001001	25%	0b 11001	41%	0b 101001	57%	0b 111001	73%
	0b 001010	26%	0b 11010	42%	0b 101010	58%	All Others Reserved	
	0b 001011	27%	0b 11011	43%	0b 101011	59%		
	0b 001100	28%	0b 11100	44%	0b 101100	60%		
	0b 001101	29%	0b 11101	45%	0b 101101	61%		
	0b 001110	30%	0b 11110	46%	0b 101110	62%		

	0b 001111	31%	0b 11111	47%	0b 101111	63%	

4.6.15. MR15 Register information – DQS Oscillator count start

Table 4.13. MR15 Register information – DQS Oscillator count start

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count Start	W	OP[7:0]	0x01 DQS Oscillator Count Start	1

Notes:

1. Once MR15 is accessed by host, DQS oscillator counter starts to operate. Other than issuing DQS Oscillator Count Stop command or reaching automatic counter stop by MR17, DQS oscillator keeps running to count the DQS clocks.

4.6.16. MR16 Register information – DQS Oscillator count stop

Table 4.14. MR16 Register information – DQS Oscillator count stop

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count Stop	W	OP[7:0]	0x01 DQS Oscillator Count Stop	1,2

Notes

1. DQS Oscillator Count Start MRW command (MR15) shall be issued prior to issue DQS Oscillator Count Stop MRW command (MR16).
2. Once MR16 is accessed by host, DQS oscillator counter stops to operate. Other than issuing DQS Oscillator Count Stop command or reaching automatic counter stop by MR17, DQS oscillator keeps running to count the DQS clocks.

4.6.17. MR17 Register information – DQS interval timer setting

Table 4.15. MR17 Register information – DQS interval timer setting

Function	Register Type	Operand	Data	Notes
DQS interval time run time	W	OP[7:0]	0b00000000: DQS interval timer stop via MR16 (default) 0b00000001: DQS interval timer stop automatically at 16th clocks after timer start 0b00000010: DQS interval timer stop automatically at 32th clocks after timer start 0b00000011: DQS interval timer stop automatically at 48h clocks after timer start 0b00000100: DQS interval timer stop automatically at 64th clocks after timer start ----------Thru---------- 0b00111111: DQS interval timer stop automatically at (63*16)th clocks after timer start 0b01XXXXXX: DQS interval timer stop automatically at 2048th clocks after timer start 0b10XXXXXX: DQS interval timer stop automatically at 4096th clocks after timer start 0b11XXXXXX: DQS interval timer stop automatically at 8192th clocks after timer start	1,2

Notes:

1. MRW DQS OSC Count Stop command with MR16 stops DQS interval timer in case of MR17 OP[7:0]

= 00000000B.

2. MRW DQS OSC Count Stop command with MR16 is illegal with non-zero values in MR17 OP[7:0].

4.6.18. MR18 Register information – DQS Oscillator count LSB

Table 4.16. MR18 Register information – DQS Oscillator count LSB

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	R	OP[7:0]	0-255 LSB DRAM DQS Oscillator Count	1,2,3

Notes:

1. MR18 reports the LSB bits of the DRAM DQS oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A MRW DQS OSC Count Stop command (MR16) could be issued to reset the contents of MR18/MR19.

4.6.19. MR19 Register information – DQS Oscillator count MSB (Same as LPDDR4)

Table 4.17. MR19 Register information – DQS Oscillator count MSB

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	R	OP[7:0]	0-255 MSB DRAM DQS Oscillator Count	1,2,3

Notes:

1. MR19 reports the MSB bits of the DRAM DQS oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A MRW DQS OSC Count Stop command (MR16) could be issued to reset the contents of MR18/MR19.

4.6.20. MR24 Register information – MAC Value (# of Active Counter for Row hammer)

Table 4.18. MR24 Register information – MAC Value (# of Active Counter for Row hammer)

Function	Register Type	Operand	Data	Notes
MAC Value	R	OP[4:2]	TBD	

4.6.21. MR47 Register information – PPR Resource

MR 47 is a read-only register. Each OP code indicates availability of one of eight PPR resources for the channel of Low Latency Wide IO. Each channel has its own separate MR 47. 0b0 indicates that corresponding PPR resource is not available and 0b1 indicates that PPR resource is available. Mapping the eight PPR resources to banks/slices within channel are as follows:

Table 4.19. MR47 Register information – PPR Resource

MR	Register Type	OP[0]	OP[1]	OP[2]	OP[3]	OP[4]	OP[5]	OP[6]	OP[7]

MR47	R	Slice 0 Banks 0,1	Slice 0 Banks 2,3	Slice 0 Banks 4,5	Slice 0 Banks 6,7	Slice 1 Banks 0,1	Slice 1 Banks 2,3	Slice 1 Banks 4,5	Slice 1 Banks 6,7

5. Command Definition and AC Timing

5.1. Command Truth Table

Table 5.1 defines the command truth table for each Low Latency Wide IO channel. Each command takes one clock cycle. CA pins are DDR and are specified at both rising and falling edge of each CK_t transition. The following notes apply to this table:

- Cells with X represent don't care values. Cells with V indicate valid logic high or low level is OK
- DS specifies the data slice address within channel
- BA0, BA1, and BA2 specify the bank address in a given data slice
- R0 to R10 specify the page (row) address in a given bank
- C0 to C3 specify the column address for a 64B data segment
- BL0 and BL1 specify on the fly burst length as defined in Table 5.2

Table 5.1. Command Truth Table

Command	CK_t	SDR Command Pins			DDR Command Pins											
		CKE		CS	CA[0]	CA[1]	CA[2]	CA[3]	CA[4]	CA[5]	CA[6]	CA[7]	CA[8]	CA[9]	CA[10]	CA[11]
		@CK (N-1)	@ CK (N)													
Read	R	H	H	H	H	H	BL0	BL1	C0	C1	C2	C3	DS	BA0	BA1	BA2
	F			X	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	
Write	R	H	H	H	L	H	BL0	BL1	C0	C1	C2	C3	DS	BA0	BA1	BA2
	F			X	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	
Refresh	R	H	H	H	H	L	H	L	L	V			DS	V		
	F			X	V											
Refresh_S	R	H	H	H	H	L	H	H	V				DS	V		
	F			X	V											
MRW	R	H	H	H	H	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7
	F			X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V			
MRR	R	H	H	H	H	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7
	F			X	V											
NOP	R	H	H	H	L	L	L	L	V							
	F			X	V											
SREF Entry	R	H	H	H	H	L	H	L	H	V						
	F	X		X	V											
PD Entry	R	H	L	L	X											
	F	X		X	X											
SREF/PD Exit	R	L	H	L	X											
	F	X		X	X											
DeSelet (DES)	R	H	H	L	V											
	F			X	V											

Table 5.2 shows the truth table for how burst length bits (BL0, BL1) and column address bits (C0, C1, C2, C3) shall define the burst length and burst order. C0 shall be used to determine which 64B data segment is burst in or our first for 128B and 256B Read and Write commands. C1 is don't care for 256B Read and Write commands.

Table 5.2. Burst Length and Burst Order Options Truth Table

	Burst Length Bits		Column Address Bits				Resulting Burst Order			
	BL1	BL0	C0	C1	C2	C3	1st BL8	2nd BL8	3rd BL8	4th BL8
64B (BL=8)	L	X	Select 1 of 16 64B data segments				1st 64B	NA		
128B (BL=16)	H	L	L	Select 1 of 8 128B data segments			1st 64B	2nd 64B	NA	
			H				2nd 64B	1st 64B		
256B (BL=32)	H	H	L	X	Select 1 of 4 256B data segments		1st 64B	2nd 64B	3rd 64B	4th 64B
			H				2nd 64B	1st 64B	4th 64B	3rd 64B

5.2. Read

Read command replaces the common sequence of activate, read, precharge commands of LPDDR memory. Three different burst lengths of 8, 16, and 32 corresponding to 64B, 128B, and 256B data accesses can be specified on the fly with the Read command. Figure 5.1 and Figure 5.2 show timing diagrams for a single Read and gapless back to back Read operations in the same data slice. Figure 5.3 shows minimum time from a Read command to a Write command in the same slice. Read timing parameters RL, tDQSCK, tRPRE, tDQSQ, and tRPST are defined in Table 5.7.

Figure 5.1. 64B Read command timing diagram

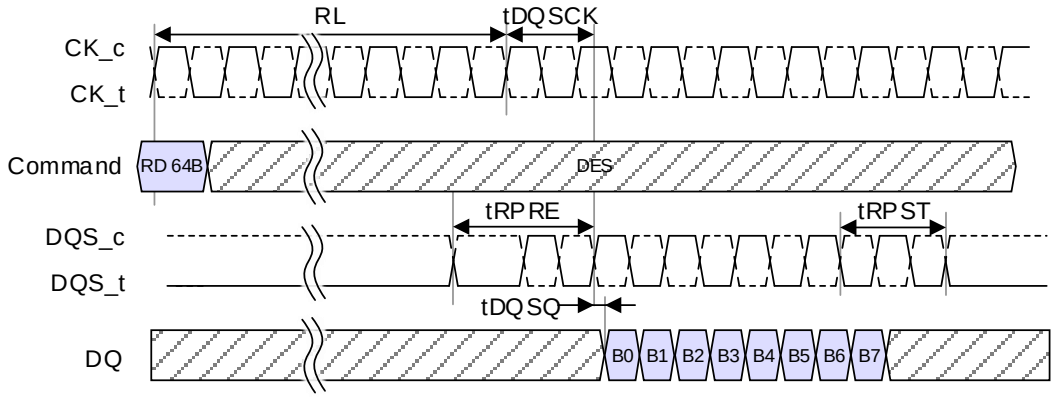


Figure 5.2. Gapless back to bank 64B Reads to different banks in same slice

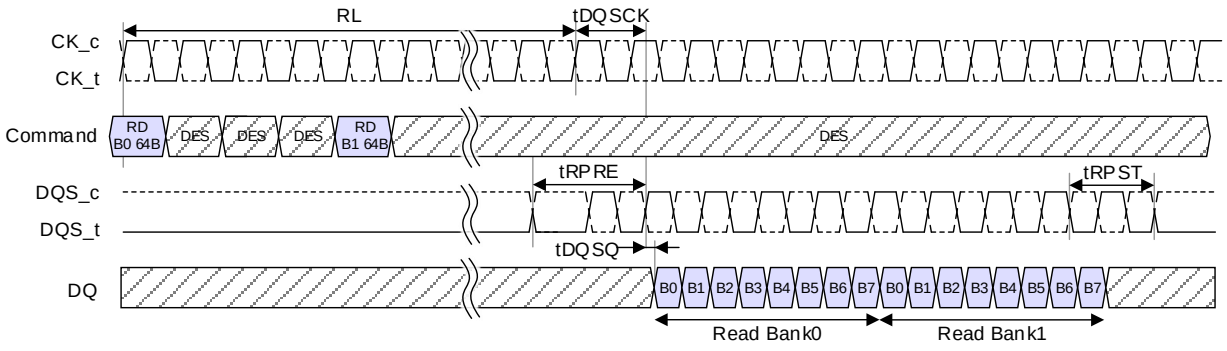
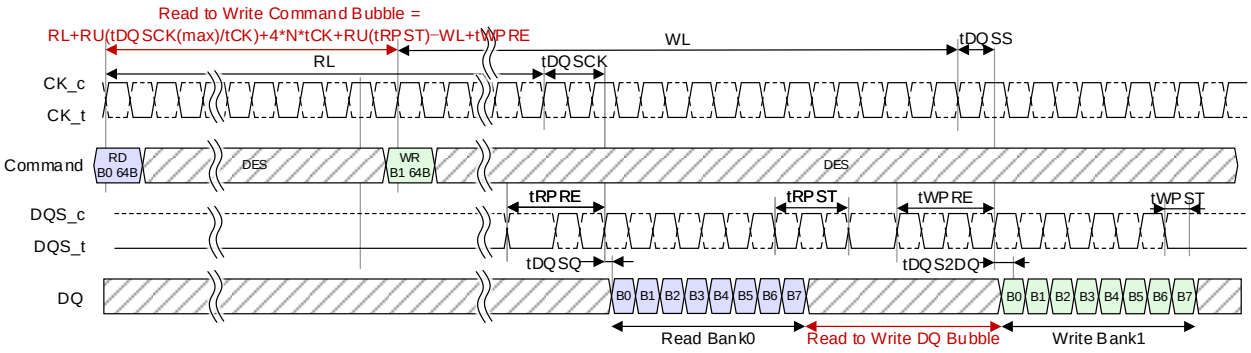


Figure 5.3. 64B Read followed by a 64B Write to different banks in same slice



5.2.1. Read Post-amble to Pre-amble Merge Behavior

When subsequent Read commands to a data slice are more than 4*N*tCK (burst-length of first Read command) apart and post-amble of first Read overlaps pre-amble of second Read, DQS signals shall follow the post-amble waveform for the duration of the post-amble to pre-amble overlap and then switch to the remaining waveform of pre-amble for the remainder of the tRPRE. This situation happens when second Read command is (4N+1)*tCK or (4N+2)*tCK or (4N+3)*tCK after the first Read command.

Both DQ and DQS signals during read shall transition from high-Z to low-Z state only at the onset of DQS Read pre-amble until the end of DQS Read post-amble.

5.3. Write

Write command replaces the common sequence of activate, write, precharge commands of LPDDR memory. Three different burst lengths of 8, 16, and 32 corresponding to 64B, 128B, and 256B data accesses can be specified on the fly with the Write command. Figure 5.4 and Figure 5.5 show timing diagrams for a single Write and gapless back to back Write operations in the same data slice. Figure 5.6 shows minimum time from a Write command to a Read command in the same slice. Write timing parameters WL, tDQSS, tWPRE, tDQS2DQ, and tWPST are defined in Table 5.7.

Figure 5.4. 64B Write timing diagram

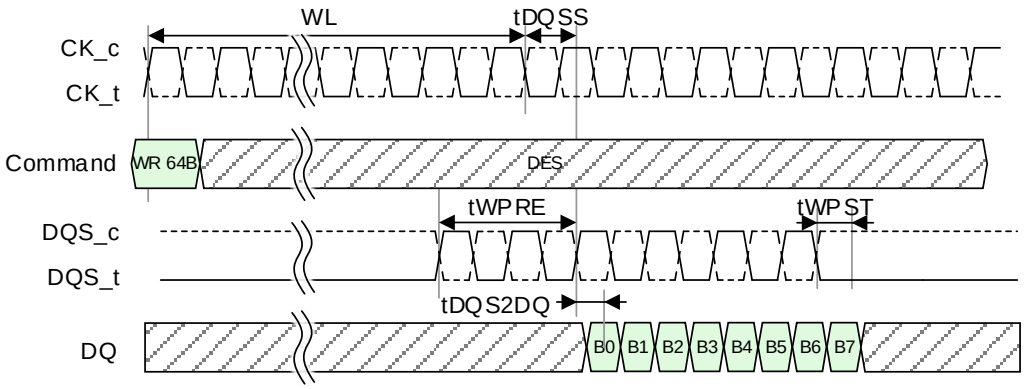


Figure 5.5. Gapless back to bank 64B Writes to different banks in same slice

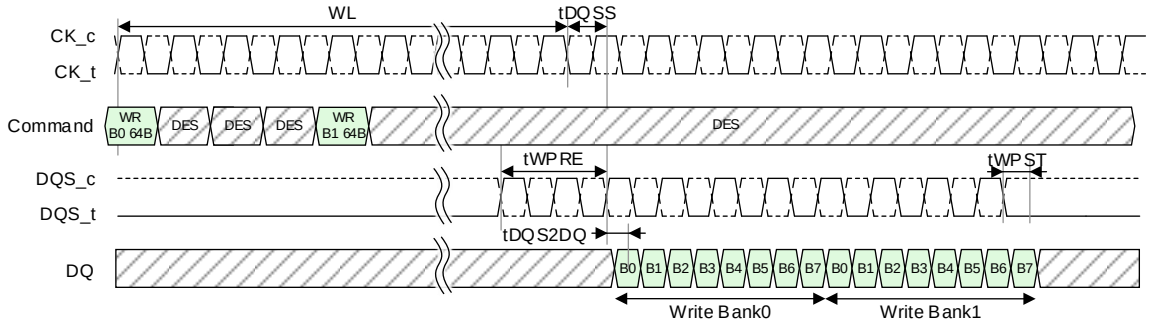
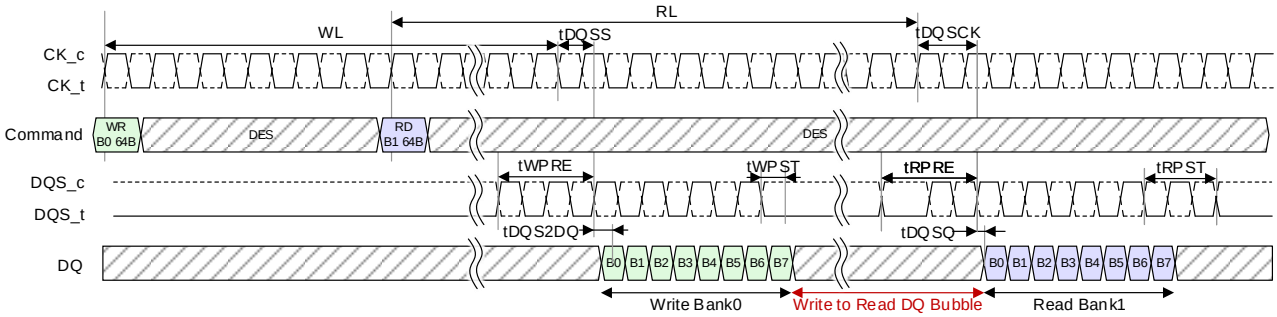


Figure 5.6. 64B Write followed by a 64B Read to different banks in same slice



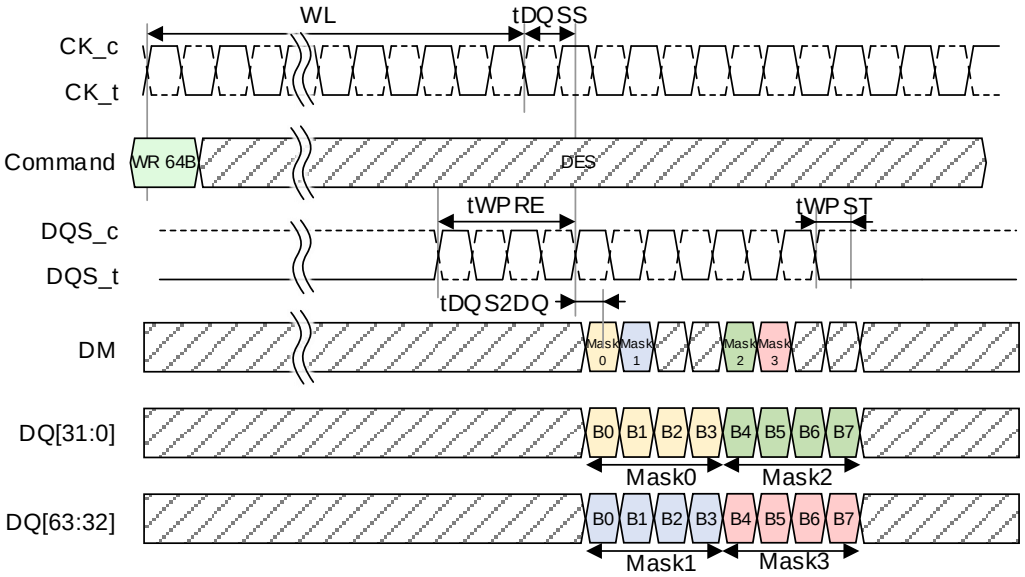
5.3.1. Write Post-amble to Pre-amble Merge Behavior

When subsequent Write commands to a data slice are more than 4*N*tCK (burst-length of first Write command) apart and post-amble of first Write overlaps pre-amble of second Write, DQS signals shall follow the post-amble waveform for the duration of the post-amble to pre-amble overlap and then switch to the remaining waveform of pre-amble for the remainder of the tWPRE. This situation happens when second Write command is (4N+2)*tCK after the first Write command. Please note that Write to write command distance of (4N+1)*tCK is illegal.

5.3.2. Masked Writes and ECC

Masked writes shall have the same command and same timing requirements as normal writes except for use of DM pin to specify write data to be masked. In Low Latency Wide IO, due to small banks, ECC codec logic is placed once per each data slice and shared among all eight banks. Data mask segments shall have 16B granularity and match the granularity of the Low Latency Wide IO internal ECC data segments so that no internal read-modify-write operation is needed to support masked writes. Figure 5.7 shows the mapping of data mask bits sent on DM pin and the 16B data segment that will be masked as a result. In every burst length of 8, there are only four valid mask bits as shown with other four bits being ignored.

Figure 5.7. Mapping of DM mask bits to 16B data segments in a masked write operation



5.4. Mode Register Read

The Mode Register Read (MRR) command is used to read configuration and status data from Low Latency Wide IO channel. The mode register address operands (MA[5:0]) allow the user to select one of 64 registers. The 8-bit mode register content OP[7:0] is burst out of DQ_S0[8] of data slice 0 according to the timing shown in Figure 5.8. DQS in slice 0 is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length of 8. MRR operation shall not be interrupted. tMRR timing parameter is defined in Table 5.7. Other timing parameters shown for MRR shall match normal Read timings.

Figure 5.8. Mode Register Read (MRR) timing diagram

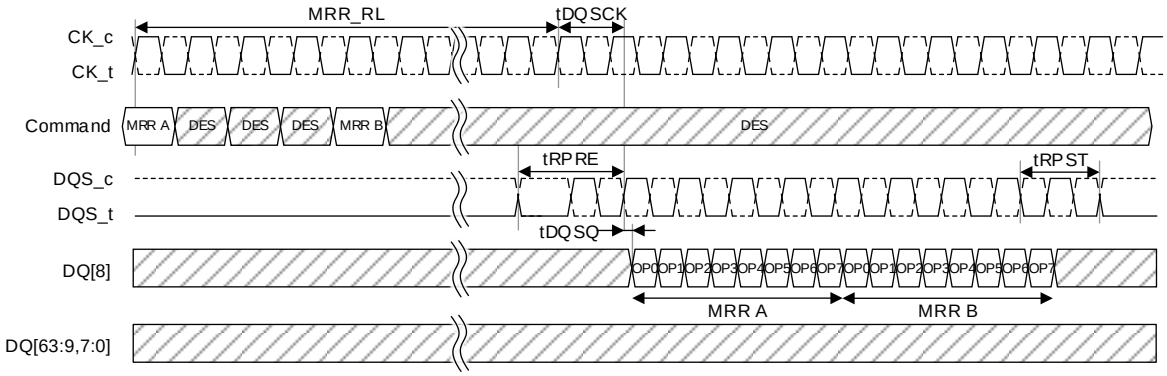


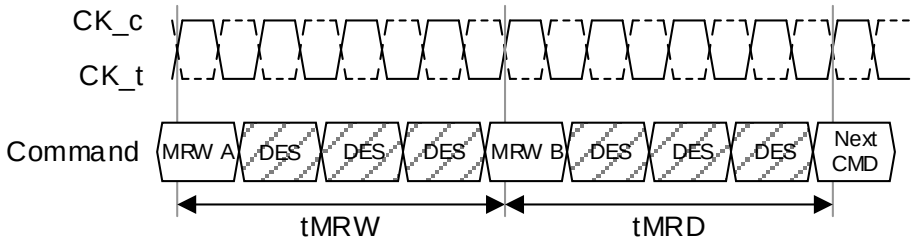
Table 5.3. Mapping of MRR read data to DQ

Pin Name	BL0	BL1	BL2	BL3	BL4	BL5	BL6	BL7
DQ_S0[8]	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ_S0[63:9,7:0] DQ_S1[63:0]	V							

5.5. Mode Register Write

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The mode register address and the data written to the mode registers are contained in MRW command as specified in Table 5.1. The MRW command period is defined by tMRW. After an MRW command, a time period of tMRD must pass before any other command can be issued. Mode register Writes to read-only registers have no impact on the functionality of the device. MRW timing parameters tMRW and tMRD are defined in Table 5.7.

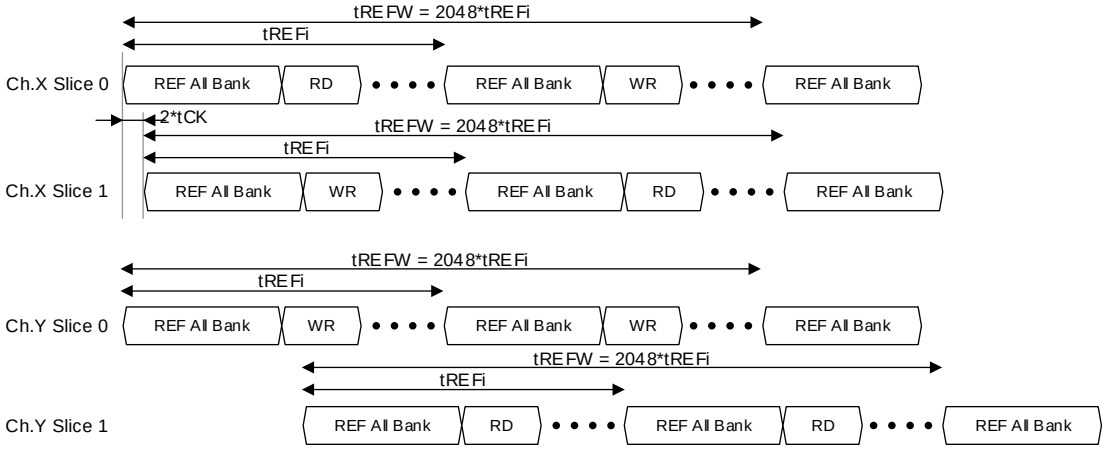
Figure 5.9. Mode Register Write (MRW) timing diagram



5.6. Refresh

Refresh command in Low Latency Wide IO only supports all-bank refresh for the banks in the same slice. Each data slice shall receive a refresh command every tREFI. Refresh command intervals cannot be pulled-in or pushed out by more than one tREFI period. A total of 2048 Refresh commands must be issued to every Low Latency Wide IO data slice every tREFW period. Figure 5.10 shows an example of how refresh operations may be mixed and overlapped among multiple data slices and channels. Refresh timing parameters tRFC, tREFI, tREFW are defined in Table 5.7.

Figure 5.10. Example Refresh operation timing diagram in two slices and two different channels



Low Latency Wide IO shall support JEDEC “Optimized Refresh” feature. Optimized Refresh requires that Low Latency Wide IO controller shall record the amount of time that has passed since the last refresh command for each data slice prior to entering self-refresh state. After exiting self-refresh state, Low Latency Wide IO controller shall wait for the remaining amount of time to complete refresh interval (tREFI) before issuing another refresh command to a data slice. Similarly, Low Latency Wide IO shall retain the amount of time that has expired in the current self-refresh interval prior to exiting self-refresh state, so that a remaining amount of time may expire after re-entering self-refresh state prior to performing a first self-refresh operation. Low Latency Wide IO controller shall keep track of Optimized refresh requirements for each channel separately (one timer per channel). Low Latency Wide IO device only needs to track

Optimized refresh requirements on a per channel basis.

5.6.1. Row Hammer Mitigation

There shall be no limitation on the number of read/write accesses to an Low Latency Wide IO page due to “row hammer” limitations in Low Latency Wide IO. To ensure “row hammer free” operation, Low Latency Wide IO controller will support the following two features. One of the two features can be enabled by Low Latency Wide IO controller:

5.6.1.1. Sub-bank Based Special Row Hammer Refresh Command

When enabled, Low Latency Wide IO controller will keep count of number of Read and Write accesses (one activate per access) issued to each of four sub-banks in a given bank in a given data slice (32 counters per data slice). If the number of accesses in any given sub-bank reaches a threshold as specified by MR24 OP[4:2], a special row hammer refresh command, Refresh_S, is issued to the corresponding data slice. The four sub-banks within each Low Latency Wide IO bank are separated by the two most-significant page address bits (R10 and R9) in Read and Write command. No other command can be issued to the same data slice for tRFC_SR duration after a Refresh_S command. Once Refresh_S command is issued to a given data slice, all 32 counters for that data slice are reset by Low Latency Wide IO controller.

5.6.1.2. Bank Based Special Row Hammer Refresh Command

When enabled, Low Latency Wide IO controller will keep count of number of Read and Write accesses (one activate per access) issued to each bank in a given data slice (8 counters per data slice). If the number of accesses in any given bank reaches a threshold as specified by MR24 OP[4:2], a special row hammer refresh command, Refresh_S, is issued to the corresponding data slice. No other command can be issued to the same data slice for tRFC_SR duration after a Refresh_S command. Once Refresh_S command is issued to a given data slice, all 8 counters for that data slice are reset by Low Latency Wide IO controller.

5.7. Power Down Entry and Exit

Power-down is asynchronously entered when CKE is driven LOW. CKE can only go low after both data slices in the channel have completed any on-going operation and are in idle state. Table 2.6 shows the earliest time power down entry can happen following any given command.

Entering power-down deactivates the input and output buffers, excluding CKE and Reset_n. After CKE goes low, clock inputs and CS input must stay valid for a time period defined by tCKELCK. Beyond this point clock and CS are also don’t care. CKE LOW will result in deactivation of all input receivers except Reset_n and CKE after tCKELCK has expired. CKE LOW interval cannot be shorter than tCKE time period.

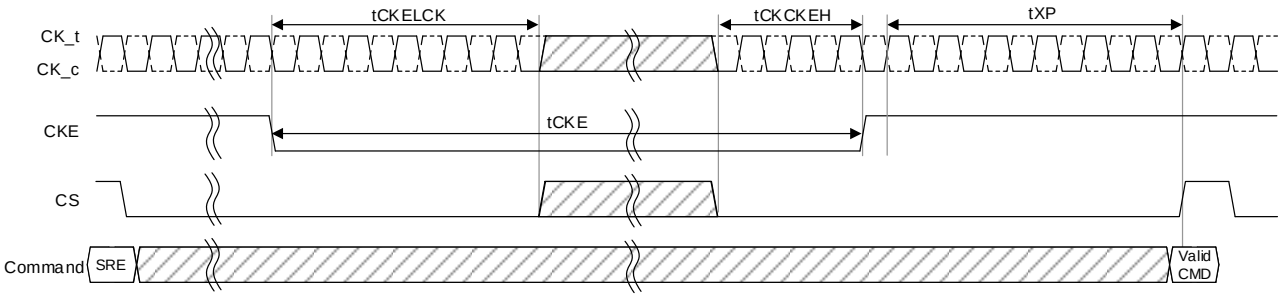
VDDQ can be turned off during power-down after tCKELCK is satisfied. Prior to exiting power-down, VDDQ must be within its minimum/ maximum operating range.

No self-refresh operations are performed in power-down. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH interval cannot be shorter than tCKE time period. A valid, executable command can be applied after time period tXP after CKE goes HIGH.

Table 5.7 defines the power down timing parameters tCKELCK, tCKCKEH, tXP, and tCKE.

Figure 5.11. Power down entry and exit timing diagram



5.8. Self Refresh Entry and Exit

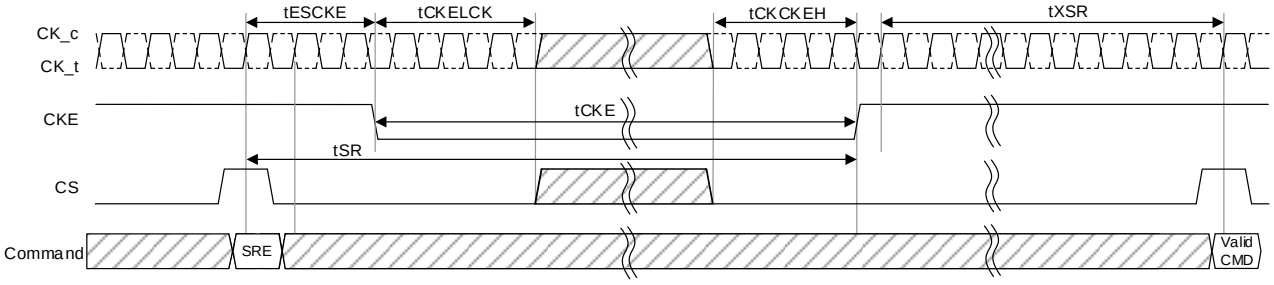
The self refresh command can be used to retain data without external refresh command. The device has a built-in timer to accommodate self refresh operation. The self refresh can only be entered when both data slices in the channel are in idle state. Unlike LPDDR definition of self refresh, in Low Latency Wide IO self refresh state is always a self refresh combined with power down state.

Low Latency Wide IO die will manage self refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperatures.

For proper self refresh operation, power supply pins (VDD1, VDD2) must be at valid levels. However, VDDQ may be turned off during self refresh after tCKELCK is satisfied. Prior to exiting Self-Refresh, VDDQ must be within specified limits. The minimum time that the SDRAM must remain in self refresh mode is tSR. Self refresh timing parameters are defined in Table 5.7.

There is no need to issue extra refresh commands upon exiting self refresh state since Low Latency Wide IO supports Optimized refresh as described in refresh section of this specification.

Figure 5.12. Self refresh entry and exit timing diagram



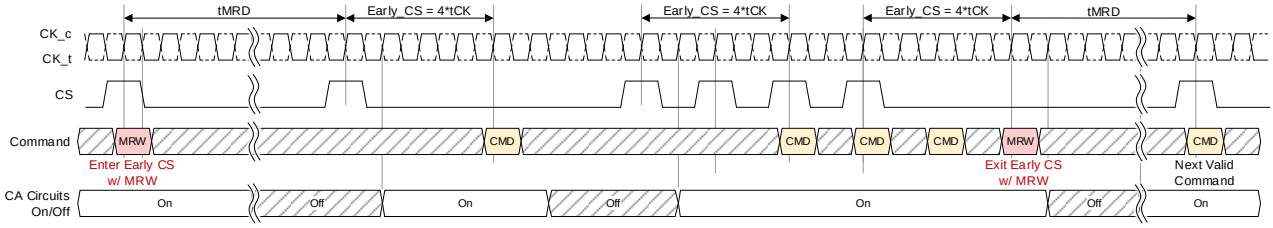
5.9. Early CS Mode Option

Unlike conventional DDR DRAM, Low Latency Wide IO uses a closed-page operation in which precise relationship between RAS and CAS events in known and single Read or Write commands triggers the whole sequence of events. Therefore, clock gating approach on Low Latency Wide IO design can be optimized to only turn on/off various circuits and clocks during the precise time they are needed to save power.

To further improve the possibility of power saving during idle time, Low Latency Wide IO shall support an early CS mode option. In this mode, CS signal associated with a command can be submitted a known number of clocks (e.g. 4*tCK) in advance of the actual command itself. The number of clocks by which CS precedes command shall be programmable by mode registers. When in early CS mode, all circuits

and clocks associated with receiving commands are clock gated or turned off except for CS, CKE and clock receivers themselves. Upon arrival of CS, the command receiver circuits and clocks are turned on to receive the new command and they will be turned off soon after the command is received, unless another CS is asserted for a subsequent command. Figure 5.13 shows an example of early CS mode.

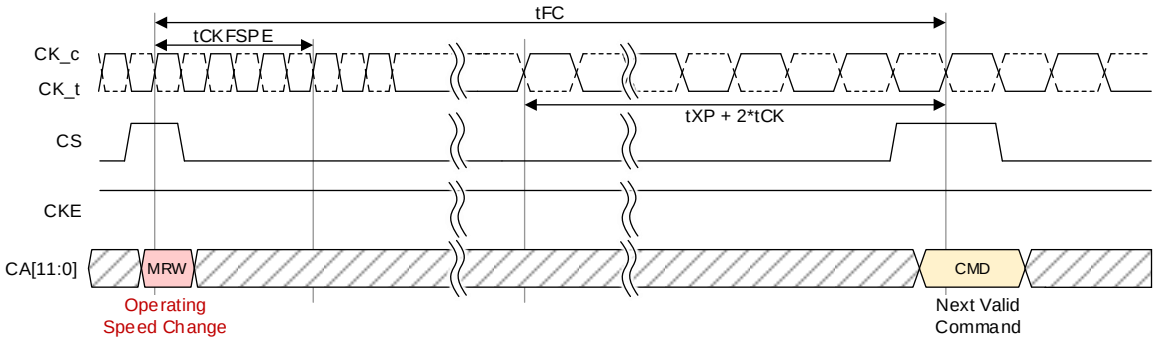
Figure 5.13. Example Early CS Mode with 4*tCK latency between CS and its command



5.10. Input Clock Frequency Change

Input clock frequency change must follow the requirements shown in Figure 5.14 timing diagram. All data slices in the channel are in idle state without any pending operation prior to frequency change MRW command. CKE must be held high and CS must be held low throughout frequency change interval. There are no VRCG requirements as IO has only one setting. RL, MRR_RL, and WL timing parameters automatically switch to their corresponding values at the new operating speed.

Figure 5.14. Input Clock Frequency Change Timing Diagram



5.11. Training and Calibration Requirements

Apart from background ZQ calibration that is periodic, all other training or calibration in Low Latency Wide IO shall be non-periodic and only be performed once after cold boot.

5.11.1. ZQ Calibration

Calibration of the output driver impedance across process, temperature, and voltage occurs in the background of device operation and no ZQ calibration initiation command to be issued to DRAM. There will be one ZQ resistor connected to MLB per one Low Latency Wide IO device (4 channels). Each channel's controller issues ZQCal Start/Latch command independently to the other channels while keeping tZQCal/tZQLat parameter. Low Latency Wide IO shall use only one channel's(Channel 1) ZQCal Start command to initiate internal calibration process and ignore other three channels'(Channel 0, 2, 3) ZQCal command to reduce calibration arbitration complexity coming from 4 channel calibration with one ZQ resistor. Upon receiving ZQCal Latch command, the channel updates the output driver impedance with the most recent calibrated value. A ZQCal Latch Command may be issued anytime outside of power-down after all DQ bus operations have completed.

Figure 5.15. ZQ Cal Timing

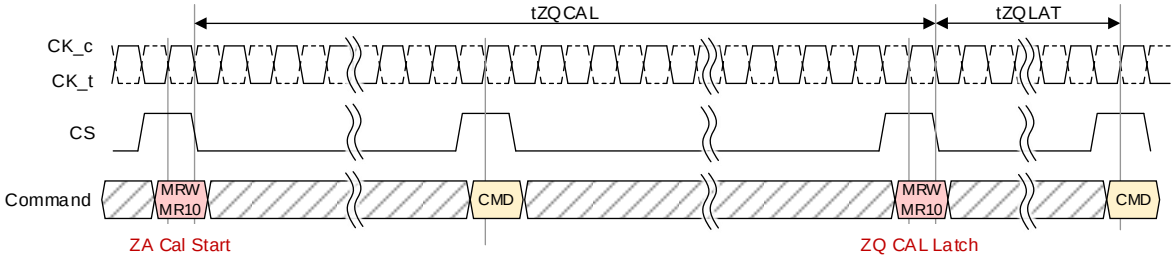


Table 5.4. ZQ Cal Timing Parameters

Timing Parameter	Description	Value	Units	Min/ Max
tZQCAL	ZQ Calibration Time	TBD	us	Min
tZQLAT	ZQ Calibration Latch Time	TBD	ns	Min
tZQRESET	ZQ Calibration Reset Time	TBD	ns	Min

5.11.2. CBT (Command Bus Training)

Low Latency Wide IO shall provide an internal VREF(ca) that defaults to a level suitable for un-terminated, low-frequency operation (~50Mhz), but the VREF(ca) will be trained to achieve suitable receiver voltage margin for unterminated, high-frequency operation. The training methodology described here centers the internal VREF(ca) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training methodology described here uses a minimum of external commands to enter, train, and exit the Command Bus Training methodology.

CBT procedure:

1. Issue MRW command to enter Command Bus Training mode. (MR11 OP[5]='1b)
2. Drive CKE= "Low" tMRD after Command Bus Training Mode MRW
3. After driving CKE to Low, Valid temporary Vref setting values (MR12 OP codes) are transmitted to Low Latency Wide IO through S0 DQ[17:16,13:12,1:0] (refer to Table 5.5 for VREF to DQ mapping) along with at least two consecutive DQS toggles. Low Latency Wide IO may or may not capture the first rising/falling edge of DQS_t/c due to an unstable first rising edge. Low Latency Wide IO updates internal VREFca setting of MR12 temporarily.
4. Once DRAM valid pattern is captured with CS toggle, DQs send it back to host (refer to Table 5.5 for CA to DQ mapping)
5. If it is required to change Vref CA setting, host repeats step #3 & #4
6. If it doesn't require to change Vref CA setting, host repeats step #4 with updated patterns
7. Exit training, issue MRW commands to exit Command Bus Training mode.
8. Vref value should be returned to its default setting after exiting CBT mode
9. Training values will be written to Low Latency Wide IO using MR12 MRW before starting normal operation

Table 5.5. VREFCA OP code to DQ mapping

CA Pin	OP5	OP4	OP3	OP2	OP1	OP0
Rising	S0 DQ17	S0 DQ16	S0 DQ13	S0 DQ12	S0 DQ1	S0 DQ0

Table 5.6. CA pin to DQ Out Mapping

CA Pin	CA11	CA10	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Rising	S0 DQ58	S0 DQ56	S0 DQ54	S0 DQ52	S0 DQ42	S0 DQ40	S0 DQ38	S0 DQ36	S0 DQ24	S0 DQ22	S0 DQ6	S0 DQ4
Falling	S0 DQ59	S0 DQ57	S0 DQ55	S0 DQ53	S0 DQ43	S0 DQ41	S0 DQ39	S0 DQ37	S0 DQ25	S0 DQ23	S0 DQ7	S0 DQ5

5.11.3. Write Leveling

Low Latency Wide IO samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair. Only DQ[8] and DQ[40] of each data slice (DQ[8] for DQS_t/c[0] and DQ[40] for DQS_t/c[1]) carry the training feedback to the controller. Low Latency Wide IO enters into write-leveling mode when mode register MR11-OP[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only DESELECT commands are allowed, or a MRW command to exit the write-leveling operation. Clock stop during write-leveling, similar to LPDDR4X, shall be allowed. Upon completion of the write-leveling operation, Low Latency Wide IO exits from write-leveling mode when MR11-OP[7] is reset LOW. Write Leveling should be performed before Write Training (DQS2DQ Training).

Write Leveling Procedure:

1. Enter into Write-leveling mode by setting MR11-OP[7]=1,
2. Once entered into Write-leveling mode, DQS_t must be driven LOW and DQS_c HIGH.
3. Wait for a time tWLMRD (=min 40tck) before providing the first DQS signal input.
4. DRAM may or may not capture first rising edge of DQS_t due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal during Write Training Mode. The captured clock level by each DQS edges are overwritten at any time and the DRAM provides asynchronous feedback on a DQ bit after time tWLO(=max 20ns).
5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings.
6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established.
7. Exit from Write-leveling mode by setting MR11-OP[7]=0.

5.11.4. Read/Write DQ training

As there is no read/write FIFO function available in Low Latency Wide IO, the controller will not perform periodic read/write training. Instead, one time read/write training will be performed by writing/reading predefined training data to/from memory array after power up.

When using a DRAM array for RD/WR DQ training, refresh-command is not required when the assigned row address is accessed (RD/WR) within tREFW to guarantee written data.

Read DQ Training Procedure:

1. Change DRAM frequency to 50Mhz and set mode register “operation speed” MR3 OP[4:2] to low speed
2. Low Latency Wide IO internal VREF(ca) and VREF(dq) level will be set to power-up default level suitable for low speed operation.
3. Controller issues Write command with predefined training pattern.
   A. DM input should stay at “low” to avoid write data masking
4. Set mode register “operation speed” MR4 OP[4:2] to high speed and then Change DRAM frequency to high speed (1Ghz)
5. Issue VREF(dq) MRW14 OP[5:0] to set internal VREF(dq) level. Vref (ca) shall be set to a level suitable for high speed operation.
6. Controller reads the training pattern stored in the array in Step #3
7. Repeat Step#6 until the optimal read data capturing delay is obtained
   A. If training time exceeds 8ms, refresh command needs to be issued to retain the written data

Write DQ Training Procedure:

1. Set mode register “operation speed” MR3 OP[4:2] to high speed and then Change DRAM frequency to high speed (1Ghz)
2. Issue VREF(dq) MRW14 OP[5:0] to set internal VREF(dq) level
3. Write predefined training pattern to memory array with tDQS2DQ delay
   A. DM input should stay at “low” to avoid write data masking
4. Controller reads the written training pattern from memory array.
5. Repeat step #3~#4 until the optimal DQ delay is obtained
6. Repeat Step #2~#5 until the optimal VREF(dq) is obtained.
7. Set the optimal VREF(dq) value through MRW14 OP[5:0]

Write DM Training Procedure:

1. Set mode register “operation speed” MR3 OP[4:2] to high speed and then change DRAM frequency to high speed (1Ghz)
2. Set optimal VREF(dq) value obtained by Write DQ training
3. Write predefined training pattern without DM(DM set to “low”) to the memory array with the optimal tDQS2DQ delay obtained by Write DQ training
4. Write predefined training pattern along with DM to memory array with tDQS2DQ delay. The data that will be masked with DM has to be different in value than the data that has already been written to the memory array.
5. Controller reads the written training pattern from memory array. (DM mask needs to be considered during the read)

   Repeat step #3~#4 until optimal tDQS2DQ delay is obtained

5.11.5. Write training Voltage/Temp variation compensation with DQS oscillator

There is no periodic read/write training but to compensate for the VT drift of tDQS2DQ delay after cold boot, the controller may read the DQS oscillator count value periodically using MR15/16 or 17/18/19 and adjust the tDQS2DQ delay based on that. DQS oscillator count value update starts by accessing MR15 and stops either by accessing MR16 explicitly when MR17 OP[7:0] is set to 8'h00 or after certain clock cycles from start specified by MR17 OP[7:0]. The updated DQS oscillator count value can be read using MR18 (LSB) and MR19 (MSB).

tDQS2DQ compensation procedure:

1. Controller reads out DQS oscillator count value right after write timing training is completed and store it as "DQSosc_cold"
2. During read/write operations, the controller periodically reads out DQS oscillator counter value (="DQSosc_current") and if the value has been drifted from "DQSosc_cold" then controller's tDQS2DQ delay is adjusted by the drift ratio.

Example:

DQSosc_cold = 300, DQSosc_current=280

tDQS2DQ delay found during cold boot training = 400ps

Adjusted tDQS2DQ delay = 400ps * 280/300 = 373ps

5.12. Timing Parameters

Table 5.7. Timing Parameters

Timing Parameter	Description	2Gbps	1Gbps	0.1Gbps	Units	Min/ Max
tCK	Command Clock Period	1	2	20	ns	Min
tRCR	64B*N Read command (N=1, 2, or 4 for on-the-fly burst length of 64B, 128B, or 256B) spacing to any other Read/Write command to the same bank	24 + 4*N			tCK	Min
tRCW	64B*N Write command (N=1, 2, or 4 for on-the-fly burst length of 64B, 128B, or 256B) spacing to any other Read/Write command to the same bank	28 + 4*N			tCK	Min
RL	Read Command to Read Data Burst Start	TBD	TBD	TBD	tCK	Min
WL	Write Command to Write Data Burst Start	9	4	2	tCK	Min
tDQSCK_Max	Maximum clock to Read DQS delay	TBD			ns	Max
tDQSCK_Min	Minimum clock to Read DQS delay	TBD			ns	Min
tDQS2DQ_Max	Maximum Write DQS to DQ delay	TBD			ps	Max
tDQS2DQ_Min	Minimum Write DQS to DQ delay	TBD			ps	Min
tDQSS_Min	Minimum Write DQS to Clock skew	TBD			tCK	Min
tDQSS_Max	Maximum Write DQS to Clock skew	TBD			tCK	Max
tRPRE	Read DQS Preamble, 1 static + 1 toggle *Mode register option to elect 2 toggle*	TBD			tCK	Min
tRPST	Read DQS Post-amble, toggle	TBD			tCK	Min
tWPRE	Write DQS Preamble, toggle	TBD			tCK	Min
tWPST	Write DQS Post-amble, toggle	TBD			tCK	Min
tRFC	Per data slice all-bank Refresh cycle time	80			ns	Min
tRFC_SR	Row Hammer Command all-bank Special Refresh cycle time	130			ns	Min
tREFI	Per data slice all-bank Refresh command interval at 85C	15.6			us	Min
tREFW	Refresh interval back to same memory page	2048 * tREFI			-	Max
tCKE	Minimum CKE high or CKE low pulse width	TBD			-	Min
tCKELCK	Minimum time from CKE low to valid clock	TBD			-	Min
tCKCKEH	Minimum time from valid clock and CS start to CKE high	TBD			-	Min
tXP	Power down exit to next valid command	TBD			-	Min
tXSR	Self refresh exit to next valid command	TBD			-	Min
tSR	Self refresh entry to exit	TBD			-	Min
tMRW	MRW to MRW	TBD			-	Min
tMRD	Mode register set delay	TBD			-	Min
tMRR	MRR to MRR	TBD			tCK	Min
MRR_RL	Read latency for MRR	TBD	TBD	TBD	tCK	Min
tMRRI	Additional time after tXP expired to MRR command	TBD			ns	Min
tFC	Frequency Change MRW command to next valid command	TBD			ns	Min
tCKFSPE	Valid clocks required post Frequency Change MRW	TBD			-	Min
tESCKE_Min	Minimum delay from self-refresh entry command to CKE low	TBD			-	Min
tESCKE_Max	Minimum delay from self-refresh entry command to CKE low	TBD			-	Max
tOSCO	Delay from DQS oscillator MRW stop to mode register read out	TBD			-	Min

5.13. Command to Command Timing Rules

Table 5.8 show timing rules for all allowed command to command sequences. Any command to command sequence not listed in this table is not allowed.

Table 5.8. Command to command timing restrictions

Current Command	Next Command	Timing Rule	Min. Value @2Gbps
64B*N Read (N=1, 2, or 4 for 64B, 128B, or 256B bursts respectively)	Any Read same bank, Refresh same slice, or MRR	tRCR	TBD
	Any Write in same bank	Max(tRCR, RL + RU(tDQSCK_max/tCK) *tCK+ 4*N*tCK + RU(tRPST/tCK)*tCK+ tWPRE – WL)	TBD
	Any Read to different bank in same slice	4*N*tCK	TBD
	Any Write to different bank in same slice	RL + RU(tDQSCK_max/tCK)*tCK+ 4*N*tCK + RU(tRPST/tCK)*tCK+ tWPRE –WL	TBD
	Any Read, Write, or Refresh in different slice	2*tCK	TBD
	MRW, PDE, or SRE	RL + RU(tDQSCK_max/tCK)*tCK+ 4*N*tCK +RU(tRPST/tCK)*tCK+2	TBD
64B*N Write (N=1, 2, or 4 for 64B, 128B, or 256B bursts respectively)	Any Read or Write same bank, or Refresh same slice	tRCW	TBD
	Any Read to different bank in same slice	4*N*tCK	TBD
	Any Write to different bank in same slice	4*N*tCK (4*N+1)*tCK is forbidden[1]	TBD
	Any Read, Write, or Refresh in different slice	2*tCK	TBD
	MRR, MRW, PDE, or SRE	tRCW	TBD
Refresh	Read, Write, or Refresh in same slice	tRFC or tRFC_SR	TBD
	Read or Write in different slice	2*tCK	TBD
	Refresh in different slice	2*tCK	TBD
	MRR, MRW, SRE, PDE, or PDX	tRFC or tRFC_SR	TBD
MRR	MRR, Read any slice	tMRR	TBD
	Refresh any slice	tRCR	TBD
	Write any slice	MRR_RL + RU(tDQSCK_max/tCK)*tCK + 4*tCK + RU(tRPST/tCK)*tCK- WL+tWPRE	TBD
	MRW, PDE, or SRE	MRR_RL + RU(tDQSCK_max/tCK)*tCK + 4*tCK + 4*tCK	TBD
MRW	Read, Write, Refresh any slice, or MRR	tMRD	TBD
	MRR, PDE, or SRE	tMRD	TBD
	MRW	tMRW	TBD
Power Down Entry	Power Down Exit	tCKE	TBD
Self-refresh Entry	Self-refresh Exit (Same command as power down exit)	tCKE	TBD
Power Down Exit	MRW, Read, Write, Refresh, PDE, SRE any slice	tXP	TBD
	MRR	tXP + tMMRI	TBD
Self-refresh Exit	Any other command in any slice	tXSR	TBD
NOP Command	Any other command in same channel	1*tCK	TBD
Any command	NOP Command	1*tCK	TBD

[1](4N+1)*tCK is illegal for write to write to the same slice

6. Absolute Maximum DC Rating

Low Latency Wide IO absolute maximum DC ratings shall be the same as LPDDR4, which are specified in Section 5 of JEDEC document JESD209-4A.

7. AC and DC Operating Condition

7.1. Supply Voltage Requirements

Voltage supply requirements measured at bump and inclusive of all noise from DC to 100MHz.

Table 7.1. DC supply requirements

Parameter	Description	Min	Typ	Max	Unit
VDD1	Memory Core Supply 1[1]	1.70	1.80	1.95	V
VDD2	Memory Core Supply 2	0.97	1.00	1.07	V
VDDQ	I/O Supply	0.57	0.60	0.67	V

[1]VdIVW and TdIVW limits described elsewhere in this document include 60mV peak to peak noise at bump from DC to 100MHz

7.2. Temperature Requirements

Table 7.2. Operating temperature range

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-25		85	°C

7.3. Signaling Requirements

Table 7.3. DQ signaling Requirements defined at bump

Parameter	Value	Notes
Max Data Rate (Gbps)	2	
DQS/CK	Differential	
VDDQ [mV]	600	
Voltage Swing [mV]	0 - VDDQ	
Cio [pF]	< 0.3	
Zpu @VDDQ/2	80, or 120	
Zpd @VDDQ/2	80, or 120	
Zpu/Zpd @VDDQ/2 Variation post calibration	+/- 10%	
Zpu/Zpd @VDDQ/2 Variation between ZQ calibration	+/- TBD%	
ODT	no	
DQ 20% - 80% rise slew rate [mV/ps]	TBD	driver w/ 0.2pF Cload only
DQ 20% - 80% fall slew rate [mV/ps]	TBD	
rise/fall mismatch (%)	< 10	
VDDQ PSIJ for DQ rise [ps/mV]	< 0.1	
VDDQ PSIJ for DQ fall [ps/mV]	< 0.1	
VDDQ Cdie [pF/bit]	>= 20	
VDDQ Rdie [Ω/bit]	0.1 - 2	

Table 7.4. DQ write timing requirements

Parameter	Value	Notes
vDIVW [mV]	+/- 100	Rx mask voltage p-p total
tDIVW (%UI)	25	Rx timing window total at Vref voltage levels
tDIVW2 (%UI)	12	Rx timing window total at vDIVW voltage levels (hexagon mask)
tDQS2DQ, min/max	TBD	DQ to DQS offset
tDQS2DQ_temp	TBD ps/°C	DQ to DQS offset temperature variation
tDQS2DQ_volt	TBD ps/mV	DQ to DQS offset voltage variation
tDQ2DQ_Write [ps]	50	DQ to DQ max timing offset during Write
Rx sensitivity variation within one channel	need feedback	vref shared per channel

Table 7.5. DQ read timing requirements

Parameter	Value	Notes
tDQSQ [ps]	TBD	Max DQS_P,DQS_N to DQ Skew
tQW (%UI)	75	DQ triggered by DQS, clock pattern, including VDD2 noise impact
tDQSCK_temp	TBD ps/°C	tDQSCK slope vs. temperature
tDQSCK_volt	TBD ps/mV	tDQSCK slope vs. voltage
tDQ2DQ_Read	80 ps	DQ to DQ max timing skew during Read

Table 7.6. CA timing requirements

Parameter	Value	Notes
vCIVW [mV]	+/- 100	Rx mask voltage p-p total
tCIVW (%UI)	30	Rx timing window total at Vref voltage levels
tCIVW2 (%UI)	15	Rx timing window total at vCIVW voltage levels

Table 7.7. Clock timing requirements

Parameter	Value	Notes
tCH(abs)	43% - 57%	Absolute clock HIGH pulse width
tCL(abs)	43% - 57%	Absolute clock LOW pulse width
tJIT [ps]	+/- 80	Clock period jitter

7.4. ESD and Latch-up Requirements

A minimum ESD protection shall be supported for all Low Latency Wide IO bumps, as listed in Table 7.8. Pins that are balled out such as direct access, boundary scan, must support higher ESD specifications. External pins must also meet Latch-up requirements.

Table 7.8. ESD and Latch-up Specification

Parameter	Value	Notes
Die to Die Pins HBM	NA	
Die to Die pins CDM	TBD	Meet worst case V or I specification
External Pins HBM	TBD	
External Pins CDM	TBD	
External Pins LU IO current injection	TBD	
External Pins LU over-voltage	TBD	

8. IDD Specification Parameters

8.1. Low Latency Wide IO IDD Definitions

Table 8.1. IDD Power Component Definitions

Parameter	Description	Unit
IDD2PS	Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW;CS is LOW;All banks are idle; CA bus inputs are stable; Data bus inputs are stable	mW
IDD2N	Idle non power-down standby current: CKE is HIGH; Clock togglingCS is LOW;All banks are idle;CA bus inputs are stable; Data bus inputs are stable	mW
IDDR1X	Operating 64B burst READ current: CS is LOW between valid commands; gapless access interleaving across all slices in the channel;64B data;50% data change each burst transfer	mW
IDDR2X	Operating 128B burst READ current: CS is LOW between valid commands; gapless access interleaving across all slices in the channel;128B data;50% data change each burst transfer	mW
IDDR4X	Operating 256B burst READ current: CS is LOW between valid commands; gapless access interleaving across all slices in the channel;256B data;50% data change each burst transfer	mW
IDDW1X	Operating 64B burst WRITE current: CS is LOW between valid commands; gapless access interleaving across all slices in the channel; 64B data;50% data change each burst transfer	mW
IDDW2X	Operating 128B burst WRITE current: CS is LOW between valid commands; gapless access interleaving across all slices in the channel; 128B data;50% data change each burst transfer	mW
IDDW4X	Operating 256B burst WRITE current: CS is LOW between valid commands; gapless access interleaving across all slices in the channel; 256B data;50% data change each burst transfer	mW
IDD5AB	All-Bank(=Per Slice) REFRESH Average current: CKE is HIGH between valid commands;tRC = tREFI/data_slices_per_channel; CA bus inputs are stable;Data bus inputs are stable;	mW
IDD6	Self refresh current: CK_t=LOW, CK_c=HIGH;CKE is LOW;CA bus inputs are stable;Data bus inputs are stable; Maximum 1x Self-Refresh Rate;	mW

8.2. IDD spec table

Table 8.2. IDD Specification for 2Gb Low Latency Wide IO DRAM x512

Symbol		Power supply	2000Mbps	Unit
IDD2PS	$IDD2PS_1$	VDD1	TBD	mA
	$IDD2PS_2$	VDD2	TBD	mA
	$IDD2PS_Q$	VDDQ	TBD	mA
IDD2N	$IDD2N_1$	VDD1	TBD	mA
	$IDD2N_2$	VDD2	TBD	mA
	$IDD2N_Q$	VDDQ	TBD	mA
IDDR1X	$IDDR1X_1$	VDD1	TBD	mA
	$IDDR1X_2$	VDD2	TBD	mA

	$IDDR1X_Q$	VDDQ	TBD	mA
IDDR2X	$IDDR2X_1$	VDD1	TBD	mA
	$IDDR2X_2$	VDD2	TBD	mA
	$IDDR2X_Q$	VDDQ	TBD	mA
IDDR4X	$IDDR4X_1$	VDD1	TBD	mA
	$IDDR4X_2$	VDD2	TBD	mA
	$IDDR4X_Q$	VDDQ	TBD	mA
IDDW1X	$IDDW1X_1$	VDD1	TBD	mA
	$IDDW1X_2$	VDD2	TBD	mA
	$IDDW1X_Q$	VDDQ	TBD	mA
IDDW2X	$IDDW2X_1$	VDD1	TBD	mA
	$IDDW2X_2$	VDD2	TBD	mA
	$IDDW2X_Q$	VDDQ	TBD	mA
IDDW4X	$IDDW4X_1$	VDD1	TBD	mA
	$IDDW4X_2$	VDD2	TBD	mA
	$IDDW4X_Q$	VDDQ	TBD	mA
IDD5AB	$IDD5AB_1$	VDD1	TBD	mA
	$IDD5AB_2$	VDD2	TBD	mA
	$IDD5AB_Q$	VDDQ	TBD	mA
IDD6	$IDD6_1$	VDD1	TBD	mA
	$IDD6_2$	VDD2	TBD	mA
	$IDD6_Q$	VDDQ	TBD	mA

Table 8.3. . IDD Specification for 2Gb Low Latency Wide IO DRAM x256

Symbol		Power supply	2000Mbps	Unit
IDD2PS	$IDD2PS_1$	VDD1	TBD	mA
	$IDD2PS_2$	VDD2	TBD	mA
	$IDD2PS_Q$	VDDQ	TBD	mA
IDD2N	$IDD2N_1$	VDD1	TBD	mA
	$IDD2N_2$	VDD2	TBD	mA
	$IDD2N_Q$	VDDQ	TBD	mA
IDDR1X	$IDDR1X_1$	VDD1	TBD	mA
	$IDDR1X_2$	VDD2	TBD	mA
	$IDDR1X_Q$	VDDQ	TBD	mA
IDDR2X	$IDDR2X_1$	VDD1	TBD	mA
	$IDDR2X_2$	VDD2	TBD	mA
	$IDDR2X_Q$	VDDQ	TBD	mA
IDDR4X	$IDDR4X_1$	VDD1	TBD	mA
	$IDDR4X_2$	VDD2	TBD	mA

	$IDDR4X_Q$	VDDQ	TBD	mA
IDDW1X	$IDDW1X_1$	VDD1	TBD	mA
	$IDDW1X_2$	VDD2	TBD	mA
	$IDDW1X_Q$	VDDQ	TBD	mA
IDDW2X	$IDDW2X_1$	VDD1	TBD	mA
	$IDDW2X_2$	VDD2	TBD	mA
	$IDDW2X_Q$	VDDQ	TBD	mA
IDDW4X	$IDDW4X_1$	VDD1	TBD	mA
	$IDDW4X_2$	VDD2	TBD	mA
	$IDDW4X_Q$	VDDQ	TBD	mA
IDD5AB	$IDD5AB_1$	VDD1	TBD	mA
	$IDD5AB_2$	VDD2	TBD	mA
	$IDD5AB_Q$	VDDQ	TBD	mA
IDD6	$IDD6_1$	VDD1	TBD	mA
	$IDD6_2$	VDD2	TBD	mA
	$IDD6_Q$	VDDQ	TBD	mA

9. Testability and Repair Requirements

9.1. Boundary Scan

Low Latency Wide IO die supports boundary scan. Boundary scan is used for:

- Continuity testing between SOC and Low Latency Wide IO;
- DC defects (open, shorts) in IO structures.

For the command bus, SOC TX to Low Latency Wide IO RX is covered. For the DQ slices, SOC TX to Low Latency Wide IO RX and Low Latency Wide IO TX to SOC RX are covered. This is illustrated in Figure 9.1 and Figure 9.2. The exact sequence for boundary scan chain pin order is specified in TBD.

Figure 9.1. SoC to DRAM

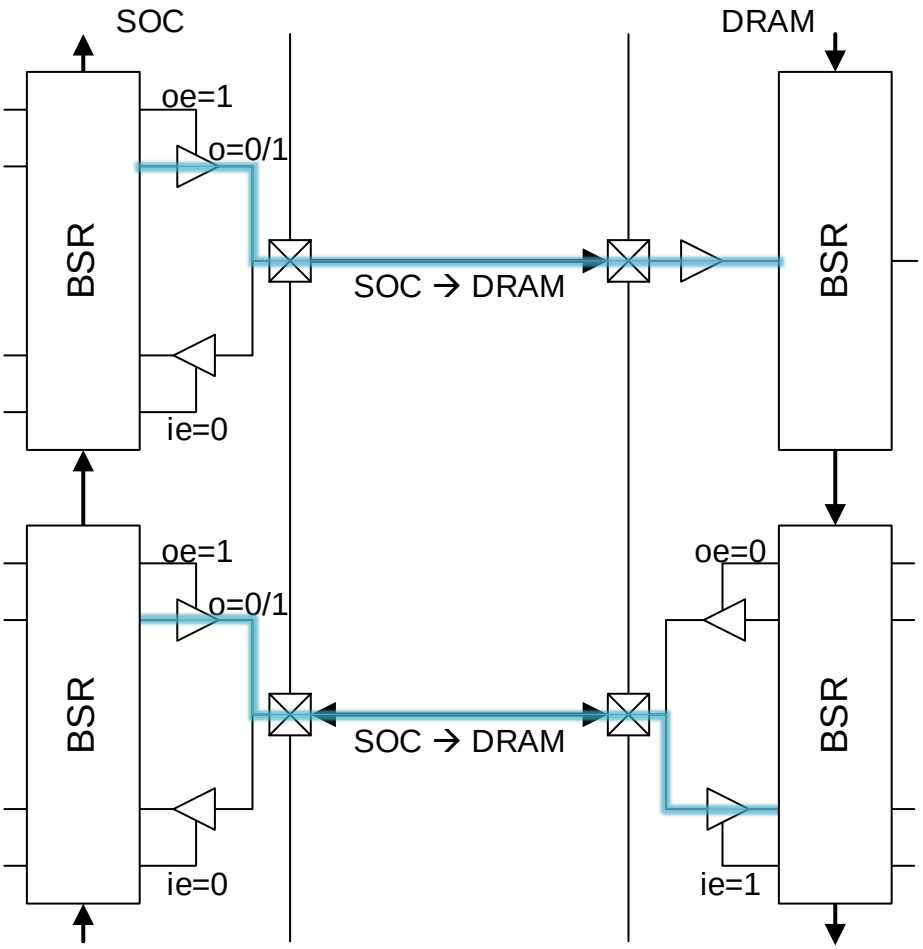
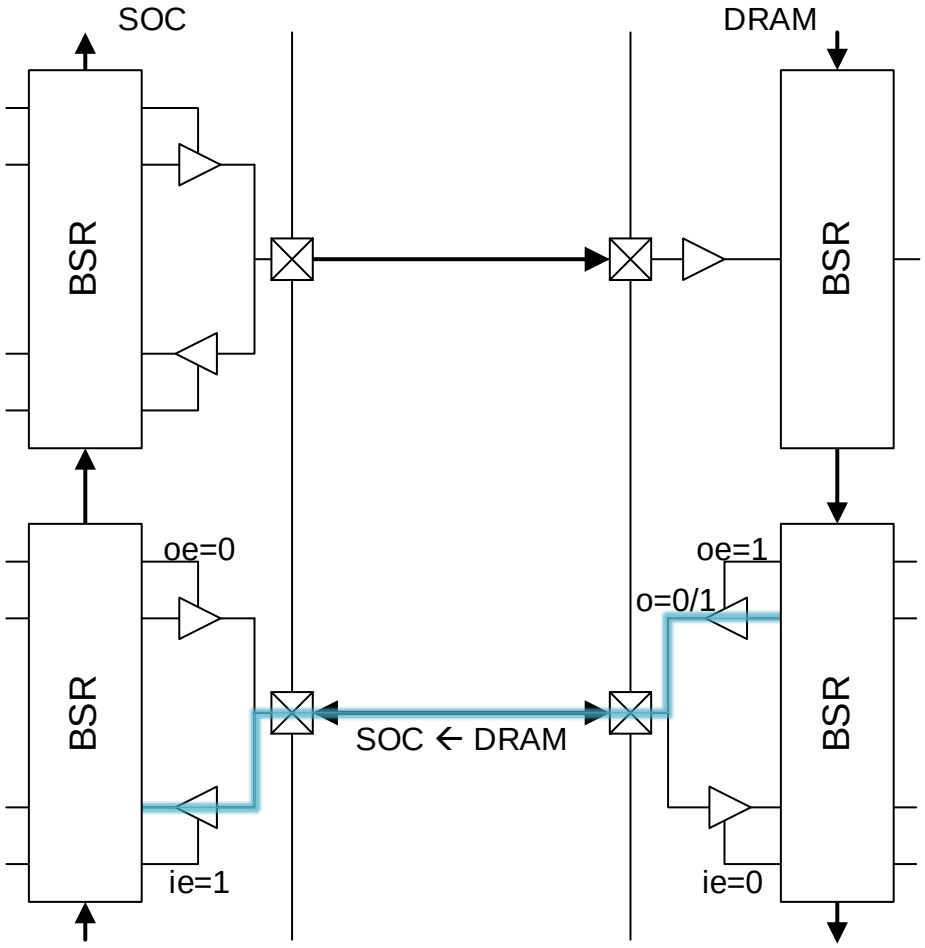


Figure 9.2. DRAM to SoC



In case of Low Latency Wide IO to SOC, SOC will ignore invalid CA capture in the data stream during shift out operation.

All Boundary Scan pins shall be routed to package BGA balls..

Table 9.1. Boundary Scan Pin Description

Pin Name	Type	Description	Operation
SEN [0]	Input	Boundary Scan Enable	0b: Normal Operation 1b: Boundary Scan Mode
SEN [1]	Input	SoC to Low Latency Wide IO direction	0b: SoC to Low Latency Wide IO 1b: Low Latency Wide IO to SoC
SSH	Input	Boundary Scan Shift	0b: Serial Data In 1b: Parallel Data In
SCK	Input	Boundary Scan Clock	Clock
SDI	Input	Boundary Scan Input	Serial Data Pattern Input
SDO	Output	Boundary Scan Output	Serial Data Pattern Output

9.2. Direct Access

- DA (Direct Access) pins should be connected to the bottom BGA balls.
- DA pins will be utilized for Low Latency Wide IO debugging on the chip set level and FA on ATE level.

- There shall be an eFuse option added to Low Latency Wide IO die to permanently disable Direct Access pins and PPR at the conclusion of production level test. This option does not disable boundary scan pins and functionality.
- While DA port is active, the main interface to Low Latency Wide IO including command port and data slices shall be disabled and ignored as their pins may have any invalid state (including reset_n pin).

9.3. Lane Repair

LOW LATENCY WIDE IO shall support lane repair scheme to repair failed IO during production test.

- Only DA pins are used during lane repair operation.
- Lane repair capability is two repairable IOs per each DQS domain for each data slice where each repairable IO is limited to 16 group A IOs and 16 group B IOs
- The grouping and repair shift order for each group within a data slice is specified in Table 9.2. Each row specifies one redundancy group for which one faulty DQ can be replaced. The redundant DQ is in the 1st column for each group in this table. To replace a faulty DQ in a group, all the DQs to the left of the faulty DQ in the same row of this table will shift by one column to the left and assume the functionality of the DQ they replaced. For example, if physical DQ11 is faulty, in redundancy group row 0B, physical R0O, DQ30, …, DQ6, DQ4 assume the functionality of logical DQ30, DQ28, …, DQ4, DQ11 respectively. Faulty DQ (physical DQ11 in this example) shall be left floating and in a high-Z state by both Low Latency Wide IO device and SoC after lane repair. The DQs to the right of the faulty DQ (physical DQ20, …, DQ2 in this example) are left unchanged after lane repair.

Table 9.2. Redundant IO Grouping and Order per Data Slice

	Physical DQ Order for Redundancy Shift															
Redundant Group Per Data Slice	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th	17th
1A DQS Domain 1 Group A	R1E	DQ46	DQ47	DQ49	DQ44	DQ33	DQ35	DQ51	DQ53	DQ42	DQ37	DQ39	DQ55	DQ57	DQ59	DQ61	DQ63
1B DQS Domain 1 Group B	R1O	DQ62	DQ60	DQ58	DQ56	DQ54	DQ41	DQ40	DQ38	DQ36	DQ43	DQ52	DQ50	DQ48	DQ45	DQ32	DQ34
0A DQS Domain 0 Group A	R0E	DQ14	DQ15	DQ17	DQ12	DQ1	DQ3	DQ19	DQ21	DQ10	DQ5	DQ7	DQ23	DQ25	DQ27	DQ29	DQ31
0B DQS Domain 0 Group B	R0O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2

- To prevent unintended entry to the lane repair operation, Low Latency Wide IO requires a guard key protection prior to the entry of lane repair mode.
- Lane repair mode cannot be executed independently per channel. Channel 3 serves as a master where lane repair information for all of the channels are sent
- The faulty IOs that are repaired shall be left floating or in high-impedance (hi-Z) state by both Low Latency Wide IO device and SoC.
- Same exact redundancy grouping and shift order applies to all data slices
- Boundary scan sequence in ??? shall not be affected by lane repair and pre-repair order shall stay in effect.

9.3.1. Lane Repair Procedure

1. Put Low Latency Wide IO in idle state with all banks in all four channels
2. Issue the guard key using DA pins (refer to vendor data sheet)
3. Enable lane repair mode with MR11 OP[3]=1 on channel 3
4. Issue guard key II, which also includes the lane repair information
5. Wait tPGM and exit lane repair by setting MR11 OP[3]=0 on channel 3
6. Wait tPGMST and assert RESET_n and follow the reset and initialization procedure specified in Section 4.3, “Power-up, Initialization, Power-off Procedures”

9.4. Post Package Repair (PPR)

LOW LATENCY WIDE IO SDRAM shall support PPR for failed row repair during production test.

- Recommended PPR capability for Low Latency Wide IO is at least 1 Row per 2 banks.
- Resource can be read by MR47 (refer to Table 9.1 for resource mapping) from each channel.
- To prevent unintended PPR entry, Low Latency Wide IO requires a Guard Key protection prior to the entry of PPR mode.
- Since Low Latency Wide IO doesn’t have explicit ACTIVE/PRECHARGE commands, which are needed for the PPR procedure, separate PPR purpose ACTIVE/PRECHARGE commands have to be defined.

9.4.1. PPR procedure

1. Put Low Latency Wide IO in Idle state with all banks precharged in all four channels.
2. Issue the guard key
3. Enter PPR mode by setting MR11 OP[4]=1.
4. In PPR mode, Low Latency Wide IO operates in open page mode and PPR purpose ACTIVE/PRECHARE command becomes valid.
5. Issue PPR purpose ACTIVE command to a channel along with the bank and failed row address.
6. Wait tPGM(=1s) and then issue PPR purpose PRECHARGE command.
7. Wait tPGM_Exit and exit PPR mode by setting MR11 OP[4]=0 and wait tPGMPST.
8. Assert RESET_n and follow the reset and initialization procedure specified in Section4.3, ″Power-up, Initialization, Power-off Procedures”
9. Repeat #2-#8 to repair another address in another bank or channel.

Table 9.3. Special-purpose PPR Commands

Command	CK_t	SDR Command Pins			DDR Command Pins											
		CKE		CS	CA[0]	CA[1]	CA[2]	CA[3]	CA[4]	CA[5]	CA[6]	CA[7]	CA[8]	CA[9]	CA[10]	CA[11]
		@CK (N-1)	@ CK (N)													

Activate	R	H	H	H	L	L	H	H					DS	BA0	BA1	BA2
	F				R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	
Precharge	R	H	H	H	L	L	H	L				AB	DS	BA0	BA1	BA2
	F															

9.5. Production Test

1. Boundary scan

- Open/Short tests.
- IO repair by using the DA mode.

2. Low Latency Wide IO array test at-speed with all the DQs thru IBIST

- As shown in Pad Layout Requirements, probing the regular pads are limited. DRAM vendor will use the dedicated probe pads to guarantee the DRAM cells at slow speed. IBIST is engine will test the DRAM cells at speed utilizing all 512 IOs.
- IBIST is a Built-In Self Test engine that located in SOC.
- Row repair if there is a defect from at-speed DRAM array test.
- Row repair shall be done by the IBIST engine issuing the PPR procedure

List of Figures

Figure 2.1. Conceptual Block Diagram

Figure 2.2. Low Latency Wide IO Die Floor Plan with Bumps Facing Up

Figure 2.3. Low Latency Wide IO Power Bump Regions with Bumps Facing Up

Figure 2.4. Bump map for Low Latency Wide IO Channel0 with bumps facing up

Figure 2.5. Bump map for Low Latency Wide IO Direct Access (DA) Port

Figure 2.6. Pad Rules

Figure 2.7. Scribe Lane and Alignment Mark Rules

Figure 4.1. Low Latency Wide IO State Diagram for Each Channel

Figure 4.2. Example of multi-channel and multi-slice operation

Figure 5.1. 64B Read command timing diagram

Figure 5.2. Gapless back to bank 64B Reads to different banks in same slice

Figure 5.3. 64B Read followed by a 64B Write to different banks in same slice

Figure 5.4. 64B Write timing diagram

Figure 5.5. Gapless back to bank 64B Writes to different banks in same slice

Figure 5.6. 64B Write followed by a 64B Read to different banks in same slice

Figure 5.7. Mapping of DM mask bits to 16B data segments in a masked write operation

Figure 5.8. Mode Register Read (MRR) timing diagram

Figure 5.9. Mode Register Write (MRW) timing diagram

Figure 5.10. Example Refresh operation timing diagram in two slices and two different channels

Figure 5.11. Power down entry and exit timing diagram

Figure 5.12. Self refresh entry and exit timing diagram

Figure 5.13. Example Early CS Mode with 4*tCK latency between CS and its command

Figure 5.14. Input Clock Frequency Change Timing Diagram

Figure 5.15. ZQ Cal Timing

Figure 9.1. SoC to DRAM

Figure 9.2. DRAM to SoC

List of Tables

Table 1.1. Comparison between LPDDR4X and LPDDR5

Table 1.2. Command List

Table 2.1. AP Pad Requirements

Table 2.2. Scribe and Alignment Mark Rules

Table 3.1. Signal pins per each channel

Table 3.2. Signal pins shared among channels

Table 3.3. Power and ground pins shared among channels (Target)

Table 4.1. Mode Register Assignments

Table 4.2. MR1 Register information – Read Preamble

Table 4.3. MR2 Register information – RL/WL Offset, Early CS Mode

Table 4.4. MR3 Register information – STU, Operating Speed, tRCW offset

Table 4.5. MR4 Register information – Refresh rate, TUF

Table 4.6. MR5 Register information – Manufacturer ID

Table 4.7. MR6 Register information – Revision ID 1

Table 4.8. MR7 Register information – Revision ID 2

Table 4.9. MR8 Register information – Type, Density, IO width

Table 4.10. MR10 Register information – ZQ Calibration code

Table 4.11. MR11 Register information – DS, PPR-Ch, PPRE, CBT, RPT, Write leveling

Table 4.12. MR12 Register information – Vref CA setting

Table 4.13. MR15 Register information – DQS Oscillator count start

Table 4.14. MR16 Register information – DQS Oscillator count stop

Table 4.15. MR17 Register information – DQS interval timer setting

Table 4.16. MR18 Register information – DQS Oscillator count LSB

Table 4.17. MR19 Register information – DQS Oscillator count MSB

Table 4.18. MR24 Register information – MAC Value (# of Active Counter for Row hammer)

Table 4.19. MR47 Register information – PPR Resource

Table 5.1. Command Truth Table

Table 5.2. Burst Length and Burst Order Options Truth Table

Table 5.3. Mapping of MRR read data to DQ

Table 5.4. ZQ Cal Timing Parameters

Table 5.5. VREFCA OP code to DQ mapping

Table 5.6. CA pin to DQ Out Mapping

Table 5.7. Timing Parameters

Table 5.8. Command to command timing restrictions

Table 7.1. DC supply requirements

Table 7.2. Operating temperature range

Table 7.3. DQ signaling Requirements defined at bump

Table 7.4. DQ write timing requirements

Table 7.5. DQ read timing requirements

Table 7.6. CA timing requirements

Table 7.7. Clock timing requirements

Table 7.8. ESD and Latch-up Specification

Table 8.1. IDD Power Component Definitions

Table 8.2. IDD Specification for 2Gb Low Latency Wide IO DRAM x512

Table 8.3. . IDD Specification for 2Gb Low Latency Wide IO DRAM x256

Table 9.1. Boundary Scan Pin Description

Table 9.2. Redundant IO Grouping and Order per Data Slice

Table 9.3. Special-purpose PPR Commands