# RF modelling and characterization of TSVs and inductive links of hybrid bonded devices

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*Abstract* — Wafer-to-wafer hybrid bonding allows for the integration of different semiconductor materials and the creation of complex 3D structures, resulting in higher device density and reduced interconnect parasitic. This paper focuses on the RF performance of the interconnect in hybrid bonded devices. Specifically, we study noise coupling between 5/5µm TSVs, as well as inductive links between different metal layers and their applications for both wireless communication and non-invasive wafer testing. The study combines experimental measurements with calibrated HFSS models up to 67 GHz. ESD tests have also been conducted on hybrid-bonded inductor loops for reliability evaluations.

***Keywords—Hybrid bonding, TSVs, inductive coupling, non-contact probing***

## I. INTRODUCTION

Amongst most different processing approaches for heterogenous integration, hybrid bonding technology has emerged as an excellent option for the integration of different semiconductor materials and the creation of complex 3D structures, leading to higher device densities and reduced interconnect parasitic for high-end applications, such as high-performance computing (HPC), artificial intelligence (AI), servers, or data centers.

By nature, systems featuring hybrid bonded types of interconnections will require high-density TSVs to embed metal pads, ideally in an array format to maintain the density for connections to additional layers. Thus, it is important to investigate the noise coupling introduced by the TSVs and develop mitigation techniques for interconnection architectures with unprecedented density. By contrast, the coupling can also be favorable in some cases and be used for applications. For example, the inductive link with the bonded wafer can enable chip-to-chip vertical communication and non-invasive wafer testing.

In the first part of this paper, the mechanism of TSV-introduced noise coupling is discussed. To mimic the coupling from a 5/5µm signal TSV array to a second signal TSV array in a real case scenario, test structures including the signal TSV array have been designed and measured for a hybrid bonding configuration. The noise coupling level introduced by the 5/5µm TSVs has then been compared to that for 5/50µm TSVs with and without noise mitigation.

In the second part, the inductive coupling between the different metal layers of hybrid bonded devices and their applications have been investigated. For each combination, the S-parameters of three test structures were measured and analyzed. In addition, calibrated HFSS models based on the S-parameter measurements were developed. The excellent agreement between simulated and measured data validates our HFSS model. We demonstrate that the complex RF field distributions that arise in-between the wafers can be accurately represented by the HFSS model. This approach allows for a complete analysis of the inductive coupling mechanisms between bonded wafers and for a study of the impact of different parameters.

Moreover, for hybrid bonding, the bonding and alignment between two wafers must avoid detrimental impacts by impurities, defects, or measurement traces on the bonding surface, since this can be detrimental to the bonding quality. Consequently, there is a strong need for non-invasive *"known good* die" (KGD) *wafer testing.* With one inductor loop integrated inside the probe head and another inductor loop in the bonded wafer, the inductive link concept can enable such non-contact wafer testing.

Furthermore, ESD tests are also conducted on these hybrid-bonded inductor loops for reliability evaluations. The results indicate that all these inductor loops can meet the required 500V HBM ESD specification. However, an unexpected ESD failure spot located at the TSV structures has been observed in a particular inductor loop under specific ESD stress conditions. More details will be shown in section VI.

## II. HYBRID BONDING TECHNOLOGY DESCRIPTION

Amongst several processing options for 3-D SoC applications, hybrid bonding technology by directly joining

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BEOL layers from two substrates has emerged as a favorable option for high density interconnect applications. All devices can be processed on a 300 mm wafer-level integration platform. A hybrid bonding layer using SiCN as the bonding interface dielectric is introduced on top of a full processed wafer. An optimized Cu PAD chemical mechanical polishing (CMP) process according to the scaled Cu pad dimension and low thermal budget requirements for the targeted 3D applications is critical in hybrid bonding. Recent breakthroughs in wafer-to-wafer bonding techniques, alignment methods, and equipment have enabled significant progress in W2W HB scaling for the development of next-generation electronic devices with enhanced performance and functionality.

In our test vehicle [1], top and bottom wafers are both processed with three metal levels (M1, Via, and PAD). The key process flow is shown in Fig. 1. To enable wafer probing, the measurement pads are realized on the backside of the top wafer with a METPASS layer, connected to M1T through 5 µm high TSVs. Fig. 2 shows a TEM image of 400 nm long daisy chains to evaluate the Cu-to-Cu connectivity between top and bottom wafers.

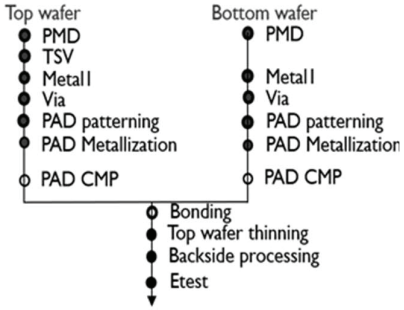


**Fig. 1:** Key process flow of wafer-to-wafer bonding.

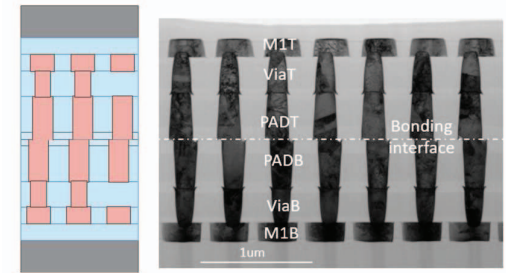


**Fig. 2:** Schematic and TEM image of 400 nm long daisy chains. Top and bottom PAD CD = 226 nm.

## III. TSV NOISE COUPLING AND MITIGATION IN HYBRID BONDING

### *A. TSV introduced noise coupling mechanism in a 3DIC*

In high-speed high-frequency applications, TSVs can interfere with the operation of neighboring devices and circuits through the TSV oxide liner and the conductive Si substrate, which can cause signal integrity problems and circuit malfunctioning. Therefore, it is essential to characterize and understand the noise coupling introduced by the TSVs. The general TSV noise coupling mechanism is shown in Fig. 3. At low frequencies, the TSV oxide capacitance dominates the noise coupling, which is frequency dependent with a slope of 20 dB per decade. By contrast, at intermediate frequencies, the Si substrate resistance is the dominant contributor to noise coupling, which leads to a region where noise coupling is independent of frequency. At high frequencies, the coupling path is dominated by the Si substrate capacitance and becomes once more frequency dependent with a 20 dB per decade slope in this region. The transition frequencies from low to intermediate and to high frequency depend on various factors, such as TSV dimensions, liner thickness, TSV pitch, and Si substrate resistivity.

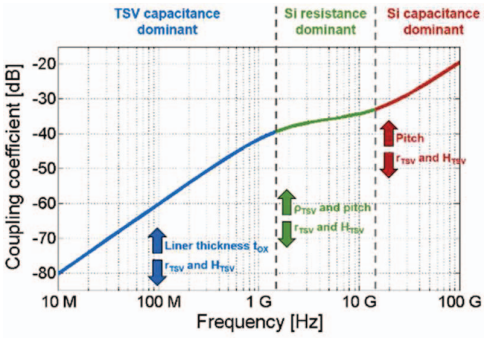


**Fig. 3:** General frequency behavior of TSV noise coupling and associated mechanisms.

Based on the noise coupling mechanism, the impact of the TSV dimensions on electromagnetic (EM) coupling can be understood and mitigation techniques can be assessed. Increasing the oxide liner thickness is only efficient at low frequency. By contrast, increasing the Si resistivity can improve the EM noise coupling immunity in the intermediate frequency range. Increasing the TSV pitch can reduce the noise coupling both at low and intermediate frequency, whereas decreasing the TSV radius and height leads to reduced noise coupling over the entire frequency range [2,3,4,5].

### *B. 5/5 µm TSV induced noise coupling test strucutres in hybrid bonded devices*

To mimic a real case scenario, our TSV test structures consist of a two-port grounded coplanar waveguide (GCPW) interdigital capacitance-like device, as depicted in Fig. 4. The TSV diameter and height are both 5 µm.

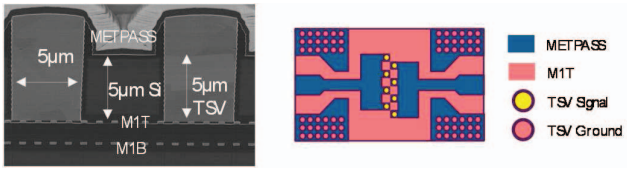


**Fig. 4:** TSV noise coupling test structure: side view (left) and top view (right) for four signal TSVs.

A signal TSV is connected at the end of each finger on the METPASS layer. The structure measures the coupling of the signal TSVs from the left port to the corresponding TSVs at the right port. The M1T ground plane is perforated at the

location of the signal TSV to isolate it from the ground. Probing pads consists of GSG 100 µm pitch 50 Ω CPW-like pads. The M1T ground plane is connected to the grounds of the GSG probing pad through two sets of TSV arrays with a total array resistance of less than 2 mΩ.

### C. *Measured noise coupling level vs. numbers of signal TSVs*

The three test structures with two, four, and six signal TSVs at each side, respectively, are depicted in Fig. 5. The measured S-parameters show that the noise coupling level is proportional to the number of signals TSVs; owing to the small dimensions of the 5/5 µm TSVs, the noise coupling is less than -30 dB at 67 GHz even for an array of six TSVs at each side and can thus be neglected.

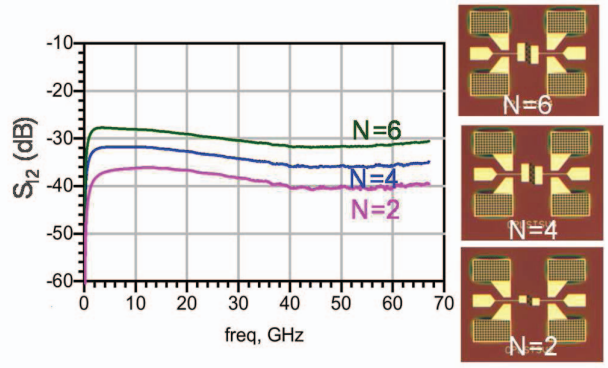


**Fig. 5:** Measured noise coupling level *vs.* the numbers of 5/5 µm TSVs at each side of the text structure.

### D. *Impact of TSV dimension on noise coupling level: 5/5 µm TSVs vs. 5/50 µm TSVs*

With respect to standard 5/50 µm TSVs, the 5/5 µm TSVs in our hybrid bonded wafer induces much lower noise coupling, as shown by the RF measurements in Fig. 6. For the test structures with four signal TSVs at each side, the 5/5 µm TSVs introduce less than -30 dB noise coupling up to 67 GHz. By contrast, 5/50 µm TSVs lead to much higher noise coupling of up to -12 dB for the same number of TSVs. Hence:

- TSV scaling helps to reduce the insertion loss and the noise coupling in dense vertical interconnects in hybrid bonding: 5/5 µm TSVs induce about 15 to 20 dB less noise coupling than 5/50 µm TSVs.
- Using noise mitigation techniques, such as grounded TSVs around signal TSVs, the noise coupling level of 5/50 µm TSVs can be strongly reduced, especially for frequencies above 40 GHz. Nonetheless, the noise coupling remains still higher than for same structures with 5/5 µm TSV even without noise mitigation.

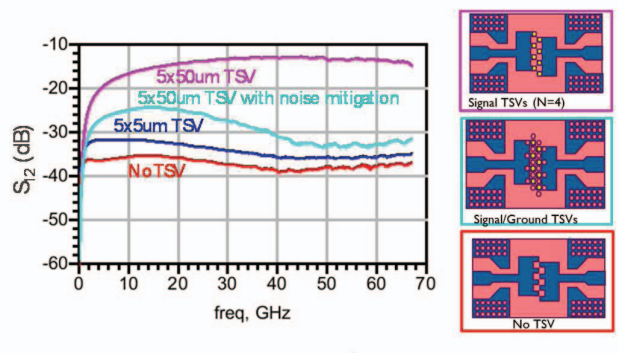


**Fig. 6:** Measured noise coupling level: 5/5 µm TSVs *vs.* 5/50 µm TSVs.

## IV. INDUCTIVE COUPLING CHARACTERIZATION AND ITS APPLICATIONS

Besides the unwanted TSV noise coupling, which can degrade the circuit performance, there is also desired inductive coupling [5,6] in hybrid bonded devices, which can be used for inter-chip data communication or non-contact sensing/probing for non-invasive wafer testing, as shown in Fig. 7.

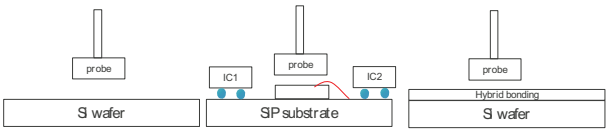


**Fig. 7:** Non-contact sensing/probing for wafer testing

### A. *Inductive link characterization and HFSS model validation for hybrid bonding*

Four types of inductive links between different metal layers have been studied in this test vehicle (see Fig. 8):

- METPASS to M1T
- M1T to M1B
- METPASS to M1B without floating M1T loop
- METPASS to M1B with floating M1T loop in between

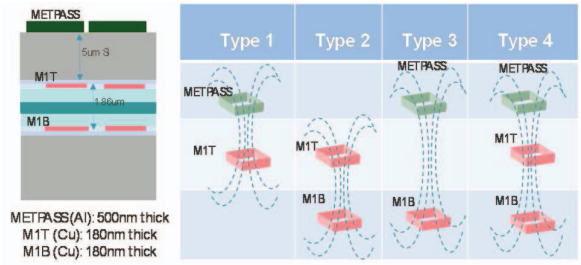


**Fig. 8:** Different inductive coupling types in hybrid bonding

Each type of inductive link is studied using two test structures with different loop overlap widths, 75 µm and 100 µm, and complemented by a test structure without inductive coupling (W = 0 µm) as a reference (Fig. 9). The microscopy image in Fig. 9 only shows the inductor loop in METPASS layer, the loop below in M1T is invisible.

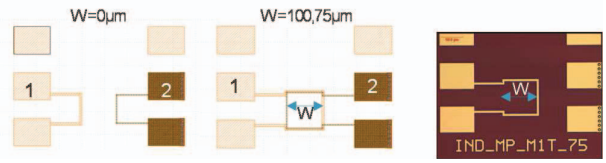


**Fig. 9:** Inductive coupling test structure layout (left); microscopy image (right).

Fig. 10 illustrates the measured inductive link between two types of structures: METPASS/M1T and M1T/M1B. Both show rather similar behavior: the coupling level is quite low below 1 GHz but increases with frequency, which indicates that the transmit signal needs high frequency spectral content to go pass through coupled inductors. Larger loops with 100 µm width leads to larger inductances, which in turn leads to higher inductive coupling in the linear region.

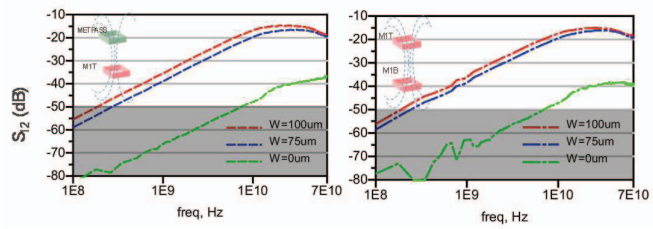


**Fig. 10:** Inductive coupling measurements: METPASS/M1T *vs.* M1B/M1T.

To mimic a real case scenario, one floating inductor loop of M1T has been inserted between METPASS and M1B. The measured inductive coupling between METPASS/M1B both with and without the floating inductor loop in M1T is compared in Fig. 11. Inserting a floating loop between the METPASS and M1B layer has minor impact in the lower frequency range, but at 25 GHz, the coupling level is reduced by about 4 dB. Moreover, we can observe that the HFSS simulation result (red solid line) shows good agreement with measurements for METPASS/M1B ($W$ = 100 µm), which validates our HFSS model.

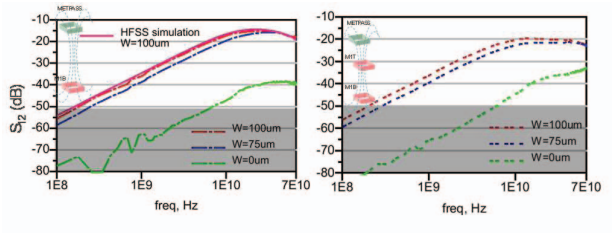


**Fig. 11:** Inductive coupling between METPASS/M1T with (left) and without (right) a floating MIT loop.

For all four types of inductive coupling, frequency regions with both linear as well as nonlinear inductive coupling have been observed. The bandwidth of the inductive channel is defined by the cut-off frequency between the linear and non-linear regime, which is determined by the self-resonance $f_{SR}$. In the linear region, larger inductance values led to higher inductive coupling. Above the linear region, increasing the inductor dimension or its inductance value becomes ineffective. To further increase the operation frequency, the bandwidth of the inductive channel needs to be increased by decreasing the self-inductance value. However, decreasing the self-inductance also decreased the inductive coupling in the linear region. Thus trade-offs must be made depending on the targeted application frequency.

### *B. Non-contact sensing/probing for wafer testing: feasibility check by HFSS modelling*

With growing complexity and density of devices, wafer testing is facing increasing challenges such as smaller pad size, increased pad density, increased signal input/output (I/O) frequencies, longer test times, or mechanical reliability of low-k dielectric materials. However, the probe card contact and alignment are restricting the progress towards smaller, faster, and more economical integrated circuits. Wireless non-contact probing techniques can alleviate all these constraints and allow for significant improvements in both the economics and the functional performance of the devices. In addition to the traditional wafer probing performed at the end of the fabrication process, wireless testing can also be implemented earlier in the manufacturing value chain, providing important feedback during the production process without leaving the measurement trace in the bonding surface.

Based on our validated HFSS model, we have transferred the top inductor loop into the probe head to mimic the non-contact wafer testing. As shown in Fig. 12, the distance between the wafers and non-contact probe head is varied from 10 µm to 30 µm to detect signals and defectivities. Based on the HFSS simulation results in Fig. 12, we can see that

- non-contact probing can detect the wireless signal through air and Si substrate.
- increasing the distance between the probe and the device reduces the inductive coupling.
- larger inductor loop sizes (W) lead to higher inductive coupling in the linear region (Fig. 13).
- defects in the inductor loop/connectivity lead to negligible inductive link signals. Hence, "open device/defect" situations can be detected (Fig. 12).

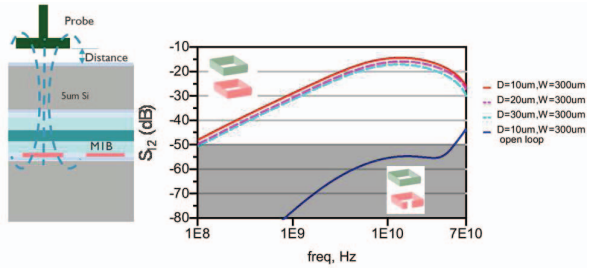


**Fig. 12:** Non-contact probing: impact of distance between probe head and device.

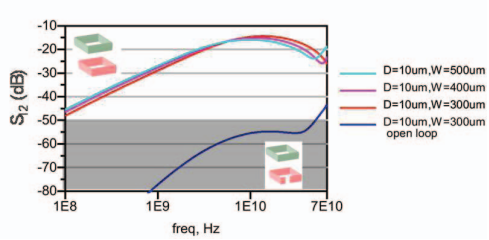


**Fig. 13:** Non-contact probing: impact of inductor loop size and connectivity

## V. Human-Body-Model ESD Analysis

For reliability evaluations, ESD tests have also been conducted based on hybrid-bonded inductor loops. A Hanwa HED-W5000M Human-Body-Model ESD Tester has been used to mimic real-time ESD events and measure the ESD robustness of these inductor loops. The inductor loops have been classified into two groups: lateral groups and vertical groups. Fig. 14 illustrates these three inductor loops. For lateral groups, a single inductor loop is tested for its ESD robustness, indicating that the lower impedance conducting path mainly involves a single inductor. The measurement results represent the maximum failure current of the single inductor. On the other hand, for hybrid-bonded devices, ESD events could occur in the vertical direction, involving at least two inductors. Therefore, in vertical loops, the ESD robustness of two inductor loops has been tested simultaneously. Its ESD robustness suggests large maximum failure voltage of the dielectric layers between the two inductor loops. Fig. 15 (a) and (b) depict the transient HBM ESD current waveform and the devices' I-V curve for the lateral loop. The M1B lateral inductor loop can sustain about 500 mA HBM ESD current. Fig. 16 depicts the HBM voltage waveform for the vertical loop. Table I and II summarize the ESD robustness results for these two groups.

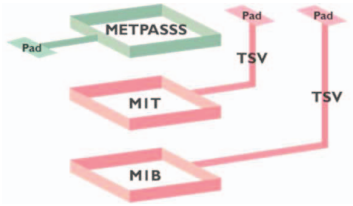


**Fig. 14:** Illustration of the studied inductor loops.

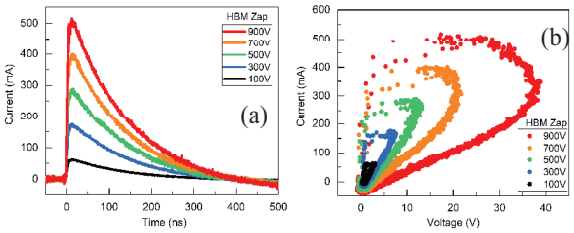


**Fig. 15:** (a) HBM transient current waveform (b) HBM I-V for a M1B lateral inductor loop with 900 V ESD robustness.

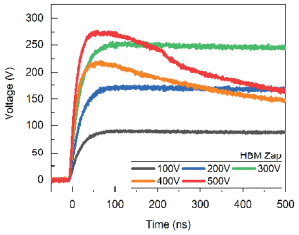


**Fig. 16:** HBM transient current waveform for a M1T-M1B vertical inductor loop with 400 V ESD robustness.

TABLE I. HBM ESD test results for lateral loops.

| Lateral loop / Loop size | HBM ESD robustness (V) | | |
|---|---|---|---|
| | METPASS | M1T | M1B |
| 75*75 ($um^2$) | 3700 | 900 | 900 |
| 100*100 ($um^2$) | | | |

TABLE II. HBM ESD test results for vertical loops.

| Vertical loop / Loop size | HBM ESD robustness (V) | | | |
|---|---|---|---|---|
| | MP_M1T | MP_M1B | MP/M1T_M1B | M1T_M1B |
| 75*75 ($um^2$) | 700 | 600 | **400** | **300** |
| 100*100 ($um^2$) | 500 | | | **400** |

**Note: MP = METPASS**

It should be noted that, for the lateral loops, three inductor loops pass the 500 V HBM tests, and METPASS metal even exhibit ESD robustness up to 3700 V. There is no significant variation between the 75×75 $\mu m^2$ and 100 × 100 $\mu m^2$ loop sizes. The lower ESD robustness of the lateral loops in M1T and M1B can be attributed to the higher impedance of inductor metals compared with the METPASS metal. Furthermore, for inductor loops measured in the vertical direction, the ESD robustness obviously declines to 300 V.

## VI. Failure Analysis

In the previous section, the inductor loops consisting of M1T and M1B exhibit the lowest ESD robustness in both lateral loop and vertical loop conditions. An unexpected ESD failure spot located at the TVS structures has been observed in the particular inductor loop under a special ESD stress condition. To pinpoint the failure location, a failure analysis is further conducted.

### *A. Failure points in lateral loops*

Fig. 17 shows top-view optical images of M1T and M1B test structures along lateral loops after ESD failure. It can be noticed that the failure occurs due to the burnout of the inductor metal. Since the failure points are located at the edge of the inductor metal wires, we hypothesize that the heat generated during the ESD event resulted in the melting of the inductor metal, causing the failure.

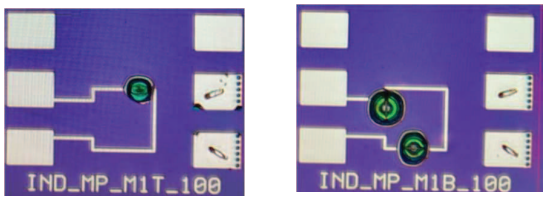


**Fig. 17:** Top-view optical images of (a) M1T and (b) M1B loops after ESD failure stresses.

### *B. Failure points in vertical loops*

For vertical loops, no obvious failure points have been observed after ESD failure. Thus, we further utilize the non-destructive hot spot detection method to determine the failure points. Fig. 18 shows the hot spot images for the M1T-M1B vertical loop configuration. It can clearly be seen that hot spots appear in the region of the probing pads, indicating the location of the 5/5 µm TSV underneath, whereas the central inductor metal remained undamaged. Therefore, we conclude that the ESD failure for inductor loops in hybrid-bonded wafer takes place at the region of TSV channels.

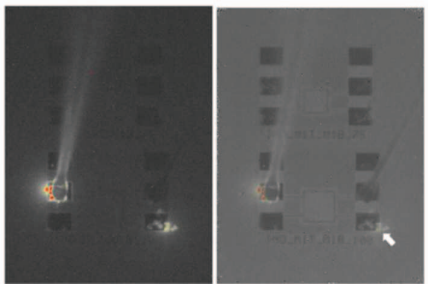

**Fig. 18:** Hot spot images in M1T-M1B vertical metal loops after ESD failure stresses.

## VII. CONCLUSIONS

We have demonstrated that hybrid wafer bonding enables higher device density and reduces the interconnect parasitic for high speed and high frequencies. Scaled TSVs in hybrid bonding improve the RF performance and reduce the noise coupling among the dense vertical interconnects. Moreover, inductive links in hybrid bonded wafers can be used for wireless communication to transmit high-frequency signals. Furthermore, noninvasive wafer testing using inductive links has been demonstrated by HFSS simulations. ESD effects have also been investigated for different inductor loops. The results indicate all inductor loops can meet the required 500 V HBM ESD specification.

## ACKNOWLEDGMENT

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