INTEL INVENTION DISCLOSURE

ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

Disclosure#110164

11/25/2013 (WW48)

Inventors

Inventor Name	WWID	Badge Type	Site Code	Resident Country	Email
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Organization/Division(s)

Intel Corporation - NAND MEMORY DIV
Intel Corporation - NVM SOLUTIONS DIVISION

Disclosure Details

Disclosure Title:

SXP POR Differential Sense Architecture & Reference Generation Scheme

Key words to describe the technology area of the invention:

AMPLIFIER, ARCHITECTURE, REFERENCE, SENSE

What technology/product/process (code name) does your invention relate to (be specific if you can)?

SXP/S15A/S15B POR Sense Architecture

Specify any keywords that describe the technology area of the invention: (Characters "(" and ")" and words such as "and", "or" and "to" should not be used and will be removed.) Please do not use acronyms.

AMPLIFIER, ARCHITECTURE, REFERENCE, SENSE

Under which of the following classifications does this invention predominantly fall?

Products: Inventions embodied in products other than high volume architecture. Encompasses test systems & design/debug tools that, although used to make Intel products, would themselves be low volume.

Is the core of your invention directed to:

Micro Architecture

Was the substantive portion of the invention made outside the United States?

No

If yes, specify the country where the substantive portion of the invention was made.

NOT APPLICABLE

Does this disclosure relate to a special harvesting project?

Phase Change Memory with Switch (PCMS)

If a description of your invention has been (or is planned to be) published outside of Intel, was the manuscript submitted for pre-publication approval through the Author Incentive Program?

No

If a description of your invention has been (or is planned to be) published outside of Intel, identify the publication.

NOT APPLICALBLE

If a description of your invention has been (or is planned to be) published outside of Intel, identify the date published. Once you have submitted your disclosure, please contact the committee chair via email if this date is less than three months from now.

If your invention has been sold or used internally or externally, or there are plans for sale or use of the invention internally or externally, what is the first date it was or will be used or sold by Intel or others? Once you have submitted your disclosure, please contact the committee chair via em

If the subject matter of this disclosure has been disclosed or plans to be disclosed to any standard setting organization (JEDEC, IEEE, etc), provide the name of the organization.

If the subject matter of this disclosure has been disclosed or plans to be disclosed to any standard setting organization (JEDEC, IEEE, etc), provide the date when it was disclosed. Once you have submitted your disclosure, please contact the committee chair via email if this date is less than three

Does your idea improve resilience of Intel products to malicious attack?

No

If the invention is embodied in a semiconductor device, what is the actual or anticipated date of tapeout?

9/14/2012

If the invention is Software, specify the actual or anticipated date of any beta tests or other distribution outside Intel?

If the invention was conceived or constructed in collaboration with anyone other than an Intel employee or as part of a project involving entities other than Intel (e.g. government (US or EU under FP7 or otherwise), companies, universities or consortia), provide the name of the individual or entity.

Is the invention related to any other invention disclosure that you have recently submitted? If so, please give the Title, Inventors and if possible, the assigned disclosure #.

1st. inventor	2nd. inventor	3rd. inventor	4th. inventor
A. Name (Last, First):			
Srinivasan, Balaji	Rivers, Doyle	Kau, Derchang	Goldman, Matthew
B. Personnel number (Intel WWID, if Intel employee)			
10598748			
C. What percentage share of the invention at the time of submission do you hold? Please specify whole numbers only and the total for all inventors must add up to 100%. If not specified below, the default is an equal percentage share for all inventors.			
%	%	%	%
D. In what country did you reside when the invention was created?			
USA	USA	USA	SA
E. At the time of the invention: Were you on a long- or short-term assignment to another legal entity?			
○ YES ◉ NO	○ YES ◉ NO	○ YES ◉ NO	○ YES ◉ NO
F. Occupation / Position / Title within the company: (e.g. design engineer)			
Analog Engineer			
G. Was the invention developed in (select one only) *a. your direct work field?* *b. different field of work at your employer?* *c. other area which does not relate to your employer?*			
◉ a ○ b ○ c	○ a ○ b ○ c	○ a ○ b ○ c	◉ a ○ b ○ c
H. Was the invention developed in response to a request from your employer to solve a particular problem?			
◉ YES ○ NO	○ YES ○ NO	○ YES ○ NO	◉ YES ○ NO

5th. inventor	6th. inventor	7th. inventor	8th. inventor

A. Name (Last, First):

B. Personnel number (Intel WWID, if Intel employee)

C. What percentage share of the invention at the time of submission do you hold? Please specify whole numbers only and the total for all inventors must add up to 100%. If not specified below, the default is an equal percentage share for all inventors.

%	%	%	%

D. In what country did you reside when the invention was created?

E. At the time of the invention: Were you on a long- or short-term assignment to another legal entity?

○ YES ○ NO	○ YES ○ NO	○ YES ○ NO	○ YES ○ NO

F. Occupation / Position / Title within the company: (e.g. design engineer)

G. Was the invention developed in

a. your direct work field?

b. different field of work at your employer?

(select one only)

c. other area which does not relate to your employer?

○ a ○ b ○ c	○ a ○ b ○ c	○ a ○ b ○ c	○ a ○ b ○ c

H. Was the invention developed in response to a request from your employer to solve a particular problem?

○ YES ○ NO	○ YES ○ NO	○ YES ○ NO	○ YES ○ NO

9th. inventor	10th. inventor	11th. inventor	12th. inventor

A. Name (Last, First):

B. Personnel number (Intel WWID, if Intel employee)

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H. Was the invention developed in response to a request from your employer to solve a particular problem?

○ YES ○ NO	○ YES ○ NO	○ YES ○ NO	○ YES ○ NO

Please provide a description of the invention and include the following information:

1. Describe your invention:

   What problem(s) does your invention solve? Briefly describe the problem you are addressing and previous solution(s), if any:

- SXP Sense reference Architecture provides a Low Die/Energy, Noise Immune solution to the problem of Resolving the question of State of the cell (0/1) being read from the array.

2. Your Idea – Provide a high-level summary of your idea that includes a figure or flowchart. Be sure to note differences between your idea and the previous solutions and to note what advantages your idea provides. Please break down the high-level summary of your idea into 3 portions as indicated by the 3 questions 2a, 2b, and 2c below:

   a. What is the basic principle? Please explain in just a few sentences (do not provide results or use cases here).

This architecture provides a apparatus to determine the State of the SXP cell being read, at low energy/diesize impact at high speed. This compares the signal (charge) against a locally generated reference to determine if this is in the 1 or 0 state. This is then level shifted & restored to a logic level before being shipped to the periphery of the memory.

The architecture provides a differential path to make it robust & immune to noise.

It also generates the reference voltage local by switched capacitors & locally available supplies to avoid expensive analog reference grids.

   b. How is your invention better than the known solutions (answer can include results, applications, or use cases)?

New Sense architecture for new SXP cell.

   c. Provide a more detailed description of your invention, highlighting what is new (please include block diagrams, process flow diagrams, etc., and limit the text to no more than 3 pages).

- Float Read (current BKM)
  - Charge word line to vdm_wl voltage
  - Float word line by de-selecting local word line driver
  - Ramp up bit line to vdm_bl voltage
  - Ramp down bit line voltage

- Select local word line driver to charge share word line with hnreg node

Issue : How do you sense the Small charge created by the Cell snap event.

- Above leaves a residual charge on the LWL, which is then transferred to the SA, using proposed architecture & enable SA.
- Need for reference that is immune to noise & easy to generate without an analog voltage grid.
- Level shift the negative signal to full restored logic level with low energy impact & at high speed.
- Works with1T/2T Decode schemes

- SXP Sense reference Architecture provides a Low Die/Energy, Noise Immune solution to the problem of Resolving the question of State of the cell (0/1) being read from the array.
  - Noise immune differential sense scheme.
  - Local reference generation, no expensive analog signal grids
  - Low energy-High speed level shifting 2 stage differential sense amplifier.
  - Works with 1T & 2T Decode schemes.

SXPSenseSchemeand reference scheme.pp

Details in power point enclosed

3. Which of our competitors are likely to use your idea or something similar?

4. How would we be able to determine if someone outside of Intel was using your idea (e.g. from visual inspection, from the product literature, from reverse engineering)?

5. Is this idea related to work performed in a Stand Development Organization (SDO) or Special Interest Group (SIG)? ○ YES ○ NO

If YES, please answer the following (a, b, c):

a. Identify the SDO or SIG involved:

b. Is this IDF prepared in anticipation of being part of an Intel proposal or submission for this SDO/SIG? ○ YES ○ NO ○ NOT SURE

If YES:

I. Identify the date of first disclosure to a party outside of Intel and outside of a confidentiality agreement (actual or anticipated):

II. Provide the name of the person(s) driving Intel's efforts for this SDO/SIG that have been made aware of this idea, if any:

c. Is there an implementation of this idea which might not be covered by a standard requirement?

6. To the best of your knowledge, identify any other pertinent information related to your idea.

7. Describe any aspects of your idea relating to unusual results or unusual function of the components/techniques in the idea, or check the box below:

☐ The unique combination of components/techniques in this idea provides an improvement over previously known structures and techniques:

8. What is the value of your idea to Intel (how will it be used by Intel or a competitor)?