Global Standards for the Microelectronics Industry

Expanding Reach: LPDDR's Enhanced Performance and Power Efficiency in Memory Solutions

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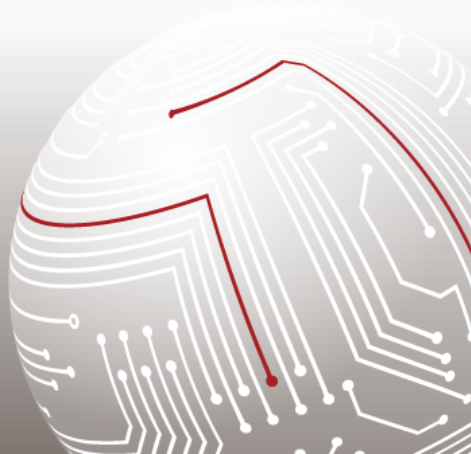
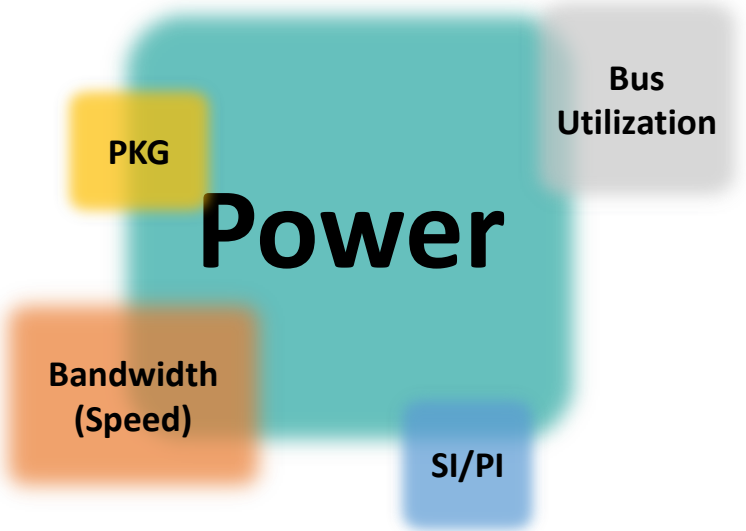


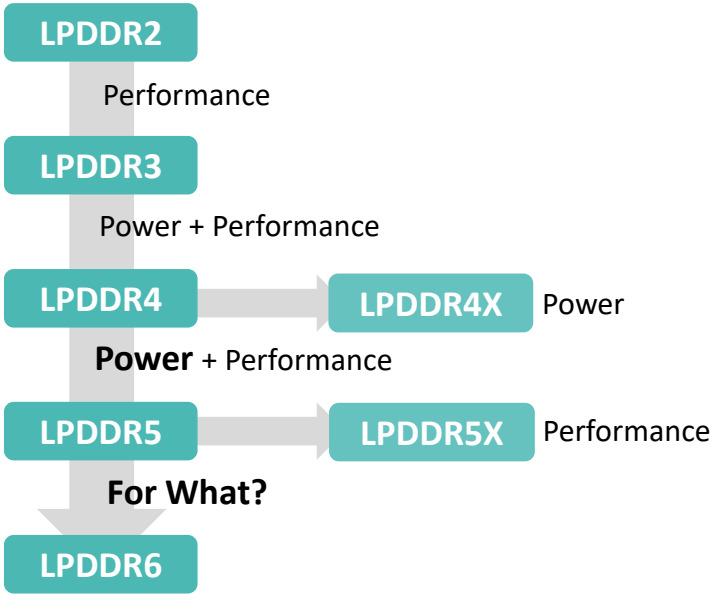
Mobile/Client/AI Computing Forum

Paradigm Shift in LPDDR

What has been required for LPDDRx?

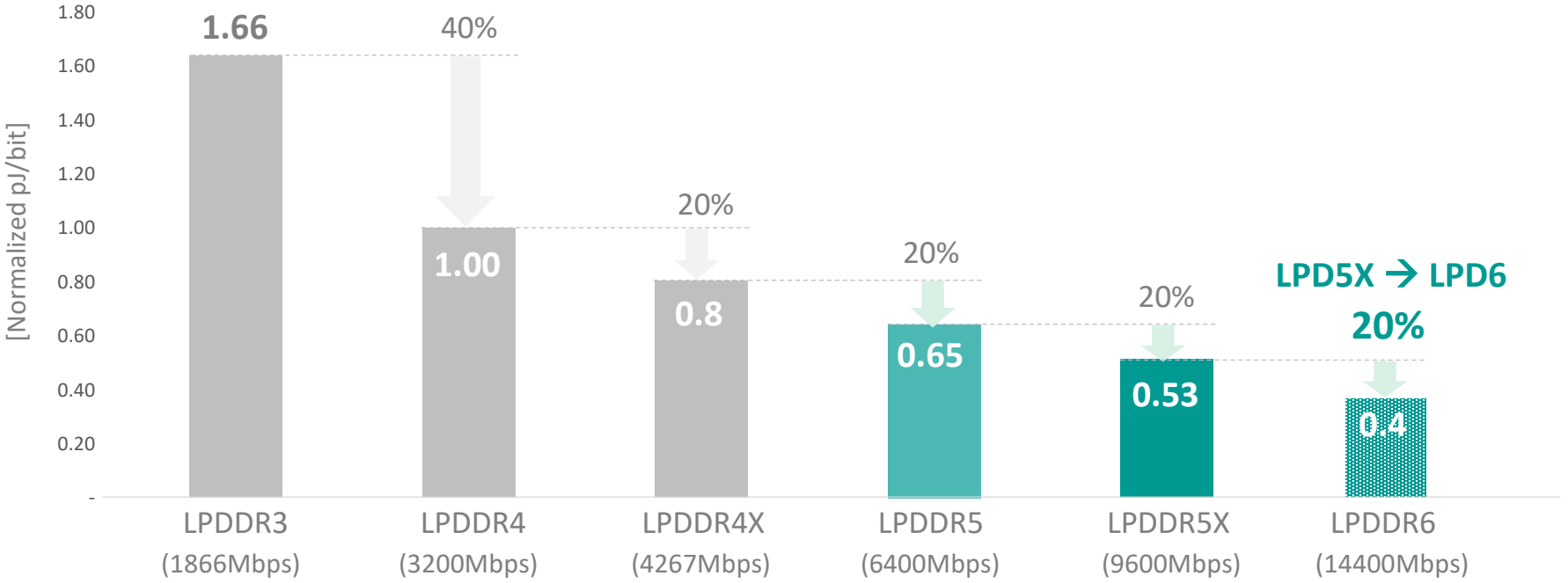


Priority of Each Generation



Power Limitation

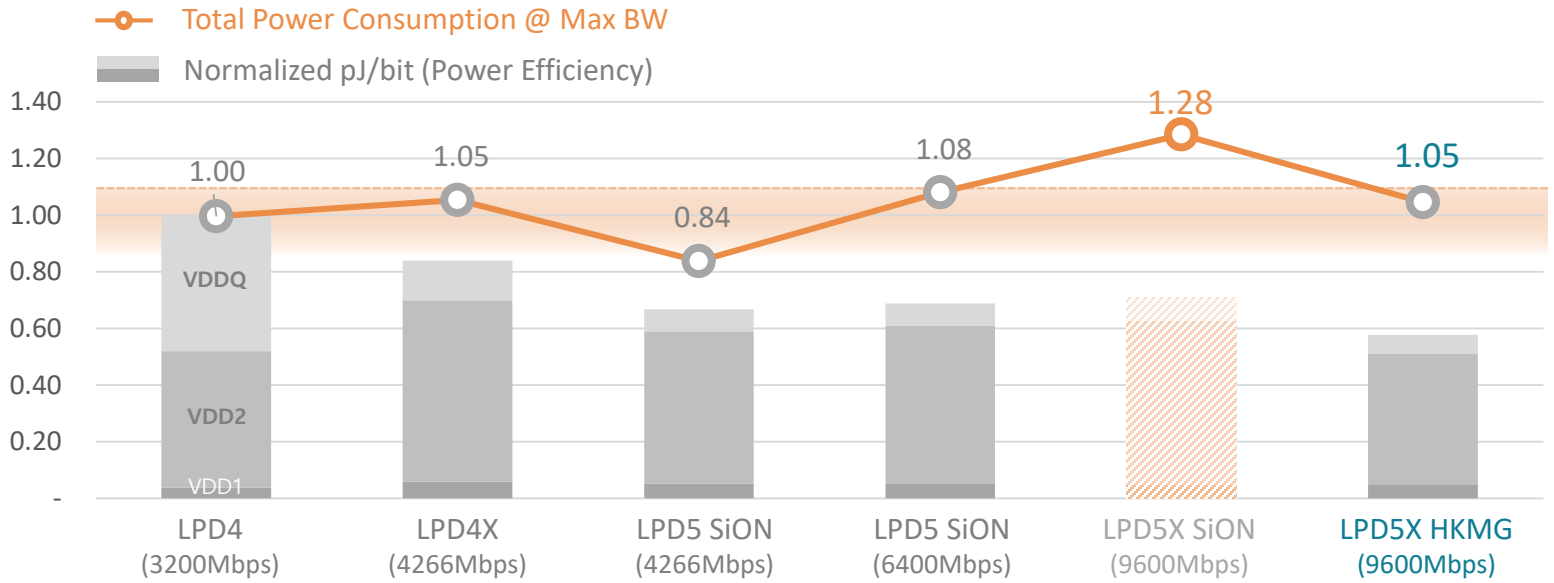
Targeting 20~40% improvement in power efficiency in every generation



* Normalized with LPD4 Power consumption

It is Due to Thermal Budget

Power efficiency needs to be improved to run at higher speeds within same amount of thermal budget



Features Adopted in LPD5 to Save Power

- Voltage Reduction
  - VDD2 : 1.10V (LPD4) → 1.05V (LPD5) • All IDD
  - VDDQ : 0.60V (LPD4) → 0.50V (LPD5) • IDD4R
- DVFS (Dynamic Voltage Frequency Scaling)
  - DVFSC : separated VDD2L (0.9V) for low speeds (up to 3200Mbps) • IDD0/2N/3N + IDD4R/4W
  - DVFSQ : Dynamic scaling between 0.5V and 0.3V (up to 3200Mbps) • IDD4R
- Low Clock Speed
  - LPDDR5 : 800Mhz Clock for 6400Mbps data rate
    400Mhz(or 200Mhz) Clock for 3200Mbps data rate • IDD0/2N/3N + IDD4R/4W
  - LPDDR4 : 1600Mhz Clock for 3200Mbps data rate
- CIO Improvement : 0.9pF (LPD4) → 0.65pF (LPD5) • IDD4R/4W

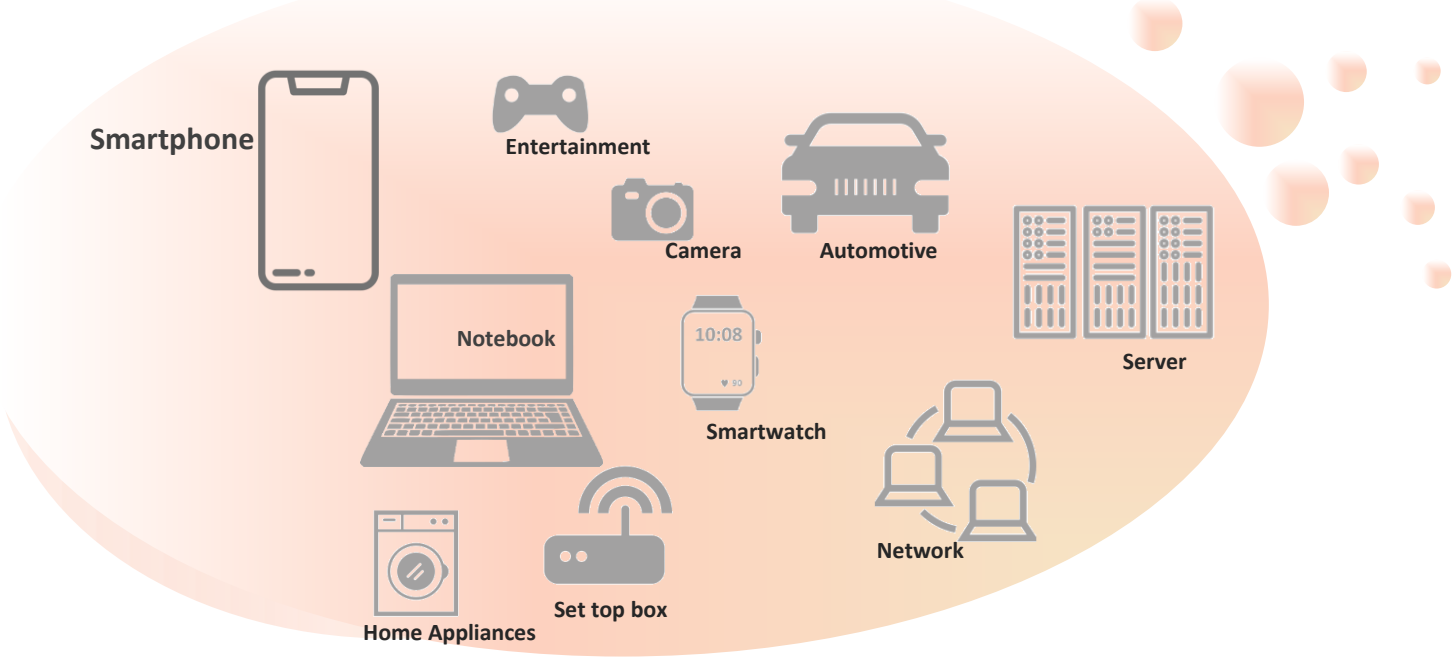
Beyond LPDDR5: What's Next?

- Still power efficiency is the first priority in mobile space
  - Features in LPDDR5 were not attractive enough to gain traction initially
- DRAM vendors adopt more advanced process technology (SiON → HKMG)
  - with a new advanced process, around 25% additional power reduction possible
- Novel process & voltage reduction already adopted in LPD5X
- Now… What's next?

  ➔ There's no free lunch, so we have to define the clear direction.

Expanding Scope of LPDDR Application

The application scope LPDDR continues to expand with its strengths



Different Set of Priorities for Each Application

Each application requests improvements to LPDDR with its own set of priorities

	Cost	Power	Density	BW/Speed	RAS	Longevity
Mobile	◎	◎	△	○	△	△
PC Client	◎	◎	△	○	△	△
Server	○	○	◎	◎	◎	○
Automotive	○	○	△	◎	◎	◎
Graphics	◎	○	△	○	△	○
Consumer	◎	○	△	○	△	◎

Various Requirements Cannot be Consolidated

- All industries do not want the **increased cost of LPDDR**
  - However, at the same time, they do not want to **forego their own priorities**
- JEDEC only provides one vote for each company – fair system
  - Who would abandon their priority for others?

Losing the Direction

- The only way to cover everything is to define “SUPER” Memory which means “SUPER Expensive” Memory
- This CANNOT be the solution and direction for future LPDDR
  - The Avengers are a group of heroes, not superheroes with all abilities
- Despite the various requirements, we have to keep in mind what makes LPDDR attractive in the first place: **LOW POWER**

The Priority Must Still be Power Efficiency

- "A nation that forgets its past has no future" by Winston S. Churchill
  - A Memory that neglects its heritage has no future?
- The fundamental advantages of LPDDR must be 'Power Efficiency'
  - The criterion that all industries pay attention to is 'Power'

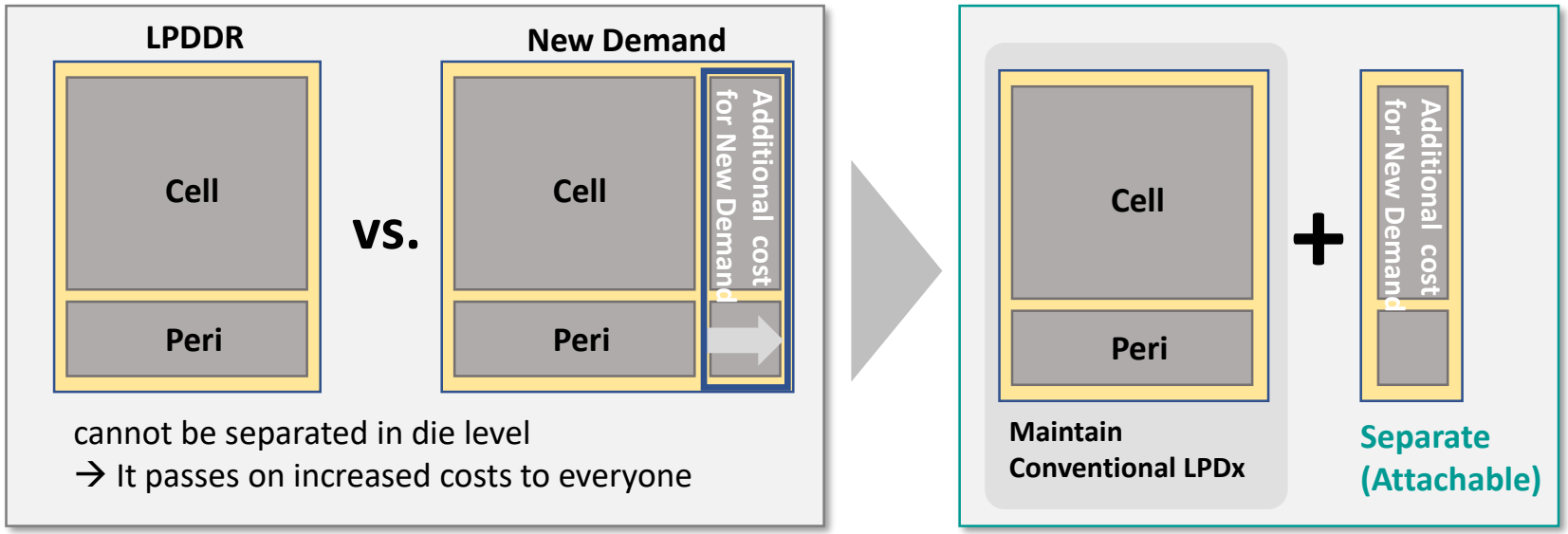
	Mobile	PC Client	Server	Auto	Graphic	Consumer
Power Efficiency	◎	◎	○	○	○	○

How to Support Other Requirements

- Can we waive other requirements? Probably not...
  - RAS
  - Density
  - Bandwidth (Speed)
- But those features would be expensive to support, so that…
  - Cost vs. New Requirement
- Is there anyone willing to pay for features they will not use?

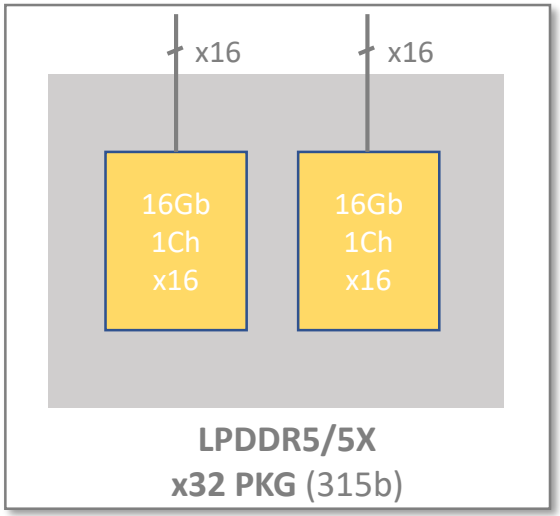
Suggestion

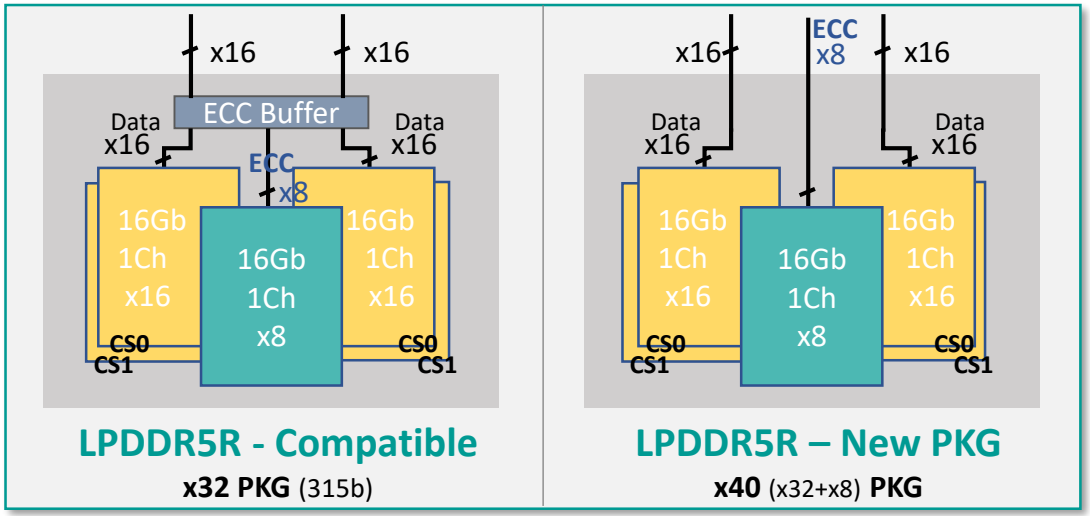
The fundamentals of LPDx shall not be jeopardized by new requirements → a form of scalability required to meet new requirements without giving up LPDx fundamentals



RAS

Solve the requirement in PKG level → Provide additional die for ECC bits enhancing RAS features (LPDDR5R)





Bandwidth

Flexible to increase the number of channels in PKG level → with 6CH & 8CH PKG users can enjoy higher bandwidth

[2 CH - JEDEC]

2ch

- 297b uMCP
- 315b discrete

[4 CH - JEDEC]

4ch

- 496b PoP
- 441b discrete
- 563b discrete

[6/8 CH Solution]

2Ch or 4Ch

4ch

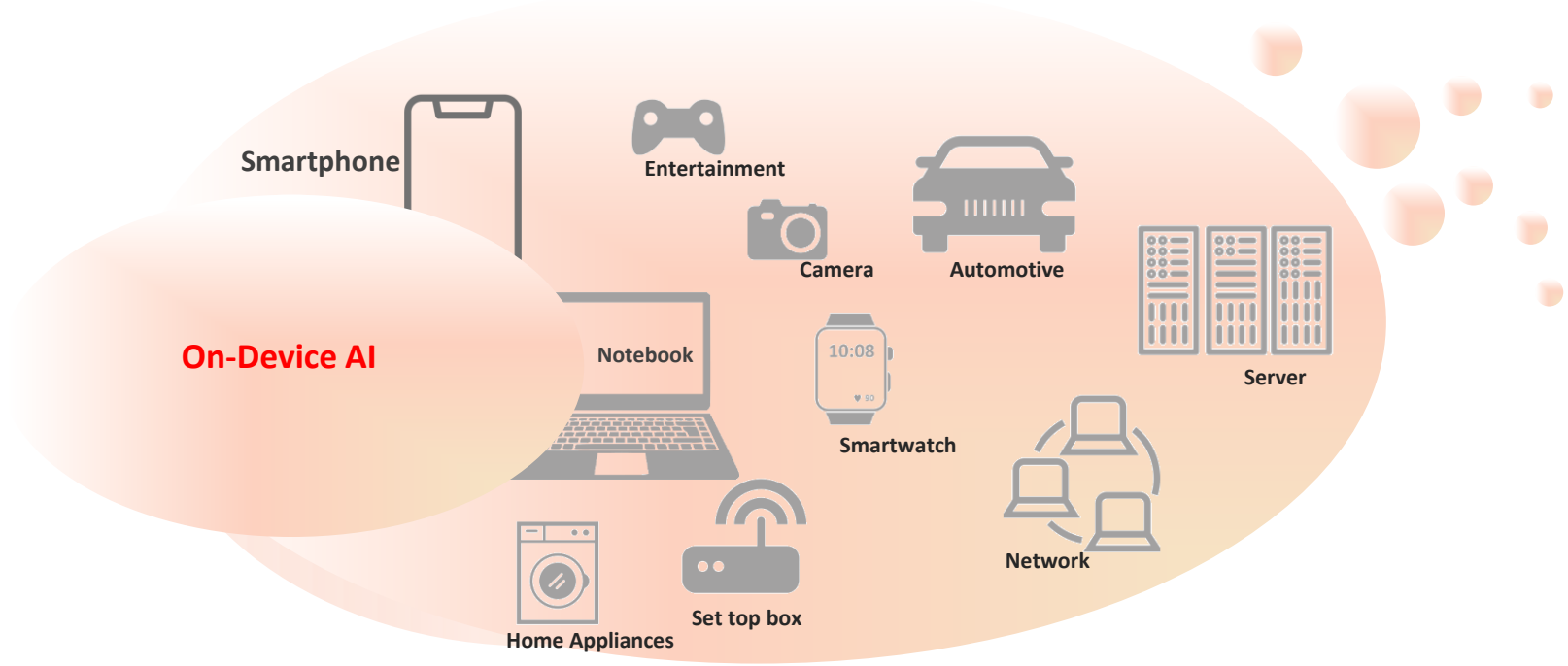
- 496b PoP
- 441b discrete
- 563b discrete

6/8CH

- New PKG

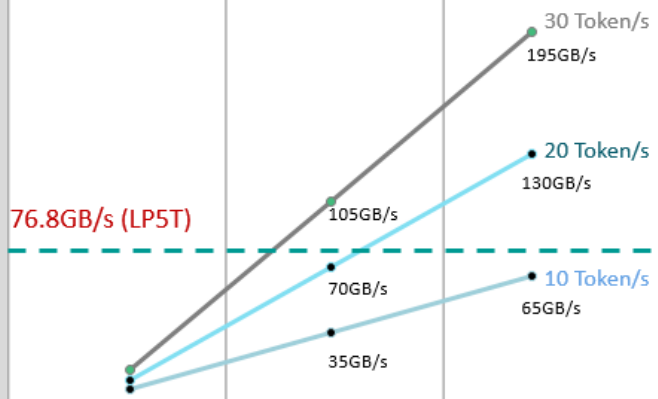
Another requirement of LPDDR Application

On-Device AI is an another hot topic in overall industry.



Memory Requirement for On-device AI

	2023	2024	2025	2026	2027	2028
On-device AI Application	Summarize Translate Speech Recognition		AI Assistant	Artificial General Intelligence?		
Model Para. (Memory Cap.)	1B (0.5GB)	7B (3.5GB)	13B (6.5GB)	over 13B?		
Memory bandwidth for decoding	(Theoretically calculated based on INT4)			**Questions** • Do real systems require Theoretical memory Capacity and Bandwidth? • What Model, Token/s, Precision are required for each Application? • Is LPDDR6 enough for after 2026 for the AI application? • When will Multi-modal based AI services be introduced and prevail the market?		



LPDDR6 and Beyond

- Not only do we provide diverse solutions to the industry, but also JEDEC has prepared LPDDR6 specification to move forward and to meet future requirements
- LPDDR is one of the best candidates to meet industries needs, and we have to see if it can cater to the specific needs of different applications while maintaining core value of LOW POWER.