JEDEC STANDARD

LPDDR5/5X Serial Presence Detect (SPD) Contents

JESD406-5

Document Release 1.0

Section	Version
Base section	1.0
Solder down annex	1.0
CAMM annex	1.0

June 2024

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2024
3103 10th Street North
Suite 240S
Arlington, VA 22201

PRICE: Contact JEDEC

Printed in the U.S.A.

For information, contact:

JEDEC Solid State Technology Association
3103 10th Street North
Suite 240S
Arlington, VA 22201
https://www.jedec.org/contact

This page intentionally left blank

LPDDR5/5X SERIAL PRESENCE DETECT (SPD) CONTENTS

Contents

Page

1 Introduction 1

2 History 2

3 SPD Architecture 3

4 Overlay Schema 4

4.1 Solder Down Overlay Schema 4

4.2 CAMM2 Overlay Schema 4

5 Parsing the SPD 5

6 SPD Revision Progression 7

7 Address Map 8

8 Details of Each Byte 11

8.1 Blocks 0 and 1: General Configuration Section: Bytes 0~127 (0x000~0x07F) 11

Annex Format — Blocks 3~6, 8~9, and 10~15 29

Blocks 3~6: Module-Specific Section: Bytes 192~447 (0x0C0~0x1BF) 29

Blocks 8~9: Module Supplier's Data: Bytes 512~639 (0x200~0x27F) 29

Blocks 10~15: End User Programmable: Bytes 640~1023 (0x280~0x3FF) 29

Annex A.0 — Common SPD Bytes for All Module Types (Bytes 192~447, 0x0C0~0x1BF) 30

Annex A.1 — Module Specific Bytes for Solder Down (Bytes 192~447, 0x0C0~0x1BF) ... 39

Annex A.8 — Module Specific Bytes for Compression Attached Memory Module Types (Bytes 192~447, 0x0C0~0x1BF) 40

Blocks 8~9 — Manufacturing Information: (Bytes 512~639, 0x200~0x27F) 42

Blocks 10~15 — End User Programmable: Bytes 640~1023 (0x280~0x3FF) 45

LPDDR5/5X SERIAL PRESENCE DETECT (SPD) CONTENTS

Contents (cont'd)

List of Figures

Page

Figure 1 — 16 GB LPDDR5/5X CAMM2 Dual Channel 1Rx16 37

List of Tables

Page

Table 1 — LPDDR5/5X Module SPD Address Map 3
Table 2 — Solder Down Overlay Schema 4
Table 3 — CAMM2 Overlay Schema 4
Table 4 — Some Relevant SPD Bytes for Parsing 5
Table 5 — Hypothetical SPD Revision Progression 7
Table 6 — SPD Address Map for all LPDDR5/5X Modules 8
Table 7 — ASCII Decode Matrix for SPDs 10
Table 8 — General Configuration Section: Bytes 0~127 (0x000~0x07F) 11
Table 9 — SPD Bytes Common to All Module Types 30

Serial Presence Detect (SPD) for LPDDR5/5X SDRAM Modules

(From JEDEC Board Ballot JCB-24-17, formulated under the cognizance of the JC-45 committee on DRAM Modules, item number 2291.04A).

LPDDR5/5X SPD, Document Release 1.0

Base SPD, Revision 1.0
Soldered Down Annex, Revision 1.0
CAMM2 Annex, Revision 1.0

1 Introduction / Scope

This publication describes the serial presence detect (SPD) values for all LPDDR5/5X memory modules. In this context, “modules” applies to memory modules like traditional Dual In-line Memory Modules (DIMMs) or solder-down motherboard applications. The SPD data provides critical information about all modules on the memory channel and is intended to be use by the system's BIOS in order to properly initialize and optimize the system memory channels. The storage capacity of the SPD non-volatile memory is limited, so a number of techniques are employed to optimize the use of these bytes, including overlays and run length limited coding.

All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

Timing parameters in the SPD represent the operation of the module including all DRAMs and are valid from t_{CKAVG}min to t_{CKAVG}max (see SPD bytes 18, 19, 124, and 125).

To allow for maximum flexibility as devices evolve, SPD fields described in this document may support device configuration and timing options that are not included in the JEDEC LPDDR5/5X SDRAM standard (JESD209-5). Please refer to DRAM supplier data sheets or JESD209-5 to determine the compatibility of components.

2 History

Computer main memory buses have traditionally been defined by the generation of memory attached to the bus, e.g., EDO, SDRAM, DDR1, etc. The bus interface protocol and characteristics have largely been defined by the memory type. Clock frequency, CAS latencies, refresh recovery times and similar parameters defined the timing of signals between memory controller and the memory, and parameters such as number of ranks installed and device widths allowed system software to determine the memory capacity and similar high level characteristics of each module.

Over time, the memory bus has been extended to include additional features for application specific requirements. Registered DIMMs, for example, increased total capacity by buffering the loading of the address bus signals, allowing more DRAM to be installed. Similarly, Load Reduced DIMMs buffered the data bus as well, allowing even more ranks of memory to be supported.

As each new extension to the function of the memory bus was introduced, system software combined knowledge of those extensions with information programmed into the non-volatile memory in the SPD to determine how to use and optimize the new features. Using the RDIMM as an example, systems understood than an additional clock of latency needed to be added to the DRAM latency to accommodate propagation delay through the register.

3 SPD Architecture

The SPD contents architecture must support the many variations of module types while remaining efficient. A system of overlay information selected through the use of “key bytes”, or selectors for the type of information to load has been implemented. The following LPDDR5/5X module SPD address map describes where the individual lookup table entries will be held in the serial non-volatile memory.

Consistent with the definition of LPDDR5/5X generation SPD devices (SPD5118) which have 16 individual write protection blocks of 64 bytes in length each, the SPD contents are aligned with these blocks as follows:

Table 1 — LPDDR5/5X Module SPD Address Map

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration, DRAM, and Module Parameters
1	64~127	0x040~0x07F	Base Configuration, DRAM, and Module Parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See annex A.0 for details
	240~255	0x0F0~0x0FF	Standard Module Parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard Module Parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard Module Parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard Module Parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FD	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for SPD bytes 0~509
8	512~575	0x200~0x23F	Manufacturing information
9	576~639	0x240~0x27F	Manufacturing information
10	640~703	0x280~0x2BF	End User Programmable
11	704~767	0x2C0~0x2FF	End User Programmable
12	768~831	0x300~0x33F	End User Programmable
13	832~895	0x340~0x37F	End User Programmable
14	896~959	0x380~0x3BF	End User Programmable
15	960~1023	0x3C0~0x3FF	End User Programmable

Operating parameters for the different module types are defined in the following Annexes and will reside in the appropriate address ranges of the SPD address map depending on the module type. Please see Overlay Schema for further details.

- Annex A.0: Common SPD Bytes for All Module Types
- Annex A.1: Solder down memory applications
- Annex A.2 through A.7: Reserved
- Annex A.8: CAMM2

4 Overlay Schema

The following Schema exemplify the manner in which the base configuration information along with the Annexes are to be overlaid onto the appropriate address spaces in order to provide a complete definition of the module.

4.1 Solder Down Overlay Schema

Key Byte 3 contains any of the following values:

- 0x0B, Solder Down

Table 2 — Solder Down Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration and DRAM Parameters
1	64~127	0x040~0x07F	Base Configuration and DRAM Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.1: Solder Down
4	256~319	0x100~0x13F	Insert Annex A.1: Solder Down
5	320~383	0x140~0x17F	Insert Annex A.1: Solder Down
6	384~447	0x180~0x1BF	Insert Annex A.1: Solder Down
7~15	448~1023	0x1C0~0x3FF	...

4.2 CAMM2 Overlay Schema

Key Byte 2 contains value 0x13 (LPDDR5) or 0x15 (LPDDR5X)

Key Byte 3 contains any of the following values:

- 0x08, CAMM2

Table 3 — CAMM2 Overlay Schema

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration, DRAM, and Module Parameters
1	64~127	0x040~0x07F	Base Configuration, DRAM, and Module Parameters
2	128~191	0x080~0x0BF	...
3	192~239	0x0C0~0x0EF	Insert Annex A.0: Common
	240~255	0x0F0~0x0FF	Insert Annex A.8: CAMM2 Memory Module Types
4	256~319	0x100~0x13F	Insert Annex A.8: CAMM2 Memory Module Types
5	320~383	0x140~0x17F	Insert Annex A.8: CAMM2 Memory Module Types
6	384~447	0x180~0x1BF	Insert Annex A.8: CAMM2 Memory Module Types
7~15	448~1023	0x1C0~0x3FF	...

5 Parsing the SPD

Table 4 — Some Relevant SPD Bytes for Parsing

SPD Byte(s)	Definition
1	SPD revision for the base section of the SPD
2	DRAM interface type presented or emulated
3	Memory module interface type
0~125	Base configuration, DRAM, and Module parameters
192	SPD revision for the module specific annex
192~239	Common module parameters
240~445	Module specific parameters
510~511	CRC for bytes 0~509

The system BIOS will acquire information from the SPD in order to properly configure the system's memory controller. It is assumed the BIOS will parse the SPD data in the order listed below.

Step 1: Parse Byte 1 - Verify the SPD contents.

The first step is to verify the validity of the contents of the SPD. Calculate and verify that the 16-bit cyclic redundancy check (CRC) for bytes 0~509 matches the CRC stored in bytes 510~511.

Step 2: Parse Byte 2 - Verify the installed DRAM type is supported.

The first step in parsing the SPD is to verify that the DRAM type installed is supported by looking at DRAM device type byte 2. While it is usually not possible to physically plug in the wrong memory type, for example a DDR3 module size or key location should prevent insertion into a DDR5 system, there are cases where byte 2 is used to prevent accidental use of an incompatible memory type.

Step 3: Parse Byte 1 - Verify SPD compatibility. See Section 6 - SPD Revision Progression

The SPD revision byte 1 "encoding" nibble may be used to force legacy systems to reject newer modules. This would typically only occur if a critical error were found in SPD encoding that would require a "fix". In this case, as in the case of an unsupported DRAM type, system initialization must be halted immediately.

The SPD revision stored in Byte 1 applies to all information for the module, including base information and module specific information. Each SPD revision exactly defines how many bytes are valid in all other SPD blocks. The number of supported bytes (or bits) may increase from one SPD revision to another within each block as indicated by the "additions" nibble of the SPD revision. For example, an SPD revision 1.3 has more bytes or bits defined than SPD revision 1.2.

This progression of SPD contents is important for the BIOS to DIMM compatibility model. An older system may have a BIOS that only understands SPD revision 1.2 encoding, so if a module is installed that contains revision 1.3 information, the system can accurately interpret all of the historical revision 1.2 information retained in the module that is the subset of the revision 1.3 specification. Similarly, if a module with SPD revision 1.1 information is installed, that same BIOS can interpret all information that was current at the time that SPD 1.1 was defined. Therefore, BIOSes must maintain a knowledge of the active information for each historical SPD revision in order to support older modules.

5 Parsing the SPD (cont'd)

New in the LPDDR5/5X SPD contents definition is a separate revision byte for sections of the contents. For example, the revision byte 1 covers only the base configuration information blocks, bytes 0 to 127. There is a separate revision byte for other sections such as the standard module parameters in bytes 192-447. The same scheme of contents and additions nibbles is used in each of these sections to allow forward and backward compatibility. Having separate revision levels in various sections of the SPD contents allows those sections to change independently.

Step 4: Parse Byte 3 - Determine module type and appropriate overlays.

Key byte 3 for module type determines the subsequent use of overlay information. Byte 3 defines the host to module interface style: unbuffered, registered, load reduced, differential, or hybrid. Standard module types are defined in Annexes A.x.

Step 5: Parse Bytes 0~127 - Make base configuration settings to memory interface based on these bytes.

All module types are required to read and interpret this block of data to set up the DRAM type, maximum operating frequency, the number of row, column, bank bits, write recovery time, etc. While these bytes primarily describe the timing of the DRAMs, timing represents the capabilities of the module and it may be necessary to downgrade the timing based on other factors including layout or support components on the module, such as registers.

Step 6: Parse Byte 192 - Module-specific annex SPD revision.

This byte determines the encoding level and additions level of the module specific bytes of the SPD. Separating the base section of the SPD and module specific section prevents unnecessary churn; for example, if the CAMM annex changes, the SPD for soldered down need not change.

Step 7: Parse Bytes 193~447 - Configure standard module memory interface.

These bytes will be referenced and used by the system as needed based on the Standard module type that was determined after Byte 3 was parsed as indicated in Step 2. Bytes 192~239 are common byte definitions for all module types as defined in Annex A.0. Bytes 240~447 are coded differently for each standard module type as defined in Annex A.x.

6 SPD Revision Progression

SPD Contents sections have a revision code for that section of the specification. This allows each section to evolve over time independently as much as possible. For example a system may need to parse one revision level for the Base Configuration section (bytes 0~127) and a different revision level for the Standard Module Parameters section (bytes 192-447).

Hypothetical SPD Revision Progression Showing Revision Relationships		
Section	**Bytes**	**Revision Byte**
Base Configuration, SDRAM, and Module Parameters	0~127	1
Standard Module Parameters	192~447	192

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

A hypothetical progression is shown to illustrate the relationship between feature updates, typographical error corrections, specification revisions, and dates. In order to reduce the number of module requalifications, policy is to issue SPD releases once per year, typically in June (publication to the JEDEC public site typically takes an additional 3 months from committee approval).

Table 5 — Hypothetical SPD Revision Progression

Year	Description	Document	Release Date	SPD Byte 1	SPD Byte 192	
				Base	Soldered Down	CAMM2
0	Initial SPD document release	JESD406-5	June 2024	1.0	1.0	1.0
0	Typographical fixes	JESD406-5	September 2024	1.0	1.0	1.0
0	Typographical fixes	JESD406-5	December 2024	1.0	1.0	1.0
1	Additions to base, CAMM2	JESD405-5A	June 2025	1.1	1.0	1.1
1	Typographical fixes	JESD405-5A	September 2025	1.1	1.0	1.1
1	Typographical fixes	JESD405-5A	March 2026	1.1	1.0	1.1
2	Additions to base, Soldered Down	JESD405-5B	June 2026	1.2	1.1	1.1
3	Additions to base	JESD405-5C	June 2026	1.3	1.1	1.1
3	Typographical fixes	JESD405-5C	March 2027	1.3	1.1	1.1

7 Address Map

Table 6 is the SPD address map for all LPDDR5/5X modules. It describes where the individual lookup table entries will be held in the serial non-volatile memory. Consistent with the definition of LPDDR5/5X generation SPD devices which have 16 individual write protection blocks of 64 bytes in length each, the SPD contents are aligned with these blocks as follows:

Table 6 — SPD Address Map for all LPDDR5/5X Modules

Block	Range		Description
0	0~63	0x000~0x03F	Base Configuration, DRAM, and Module Parameters
1	64~127	0x040~0x07F	Base Configuration, DRAM, and Module Parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See Annex A.0 for details
	240~255	0x0F0~0x0FF	Standard Module Parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard Module Parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard Module Parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard Module Parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FD	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for bytes 0~509
8	512~575	0x200~0x23F	Manufacturing Information
9	576~639	0x240~0x27F	Manufacturing Information
10	640~703	0x280~0x2BF	End User Programmable
11	704~767	0x2C0~0x2FF	End User Programmable
12	768~831	0x300~0x33F	End User Programmable
13	832~895	0x340~0x37F	End User Programmable
14	896~959	0x380~0x3BF	End User Programmable
15	960~1023	0x3C0~0x3FF	End User Programmable

After programming the SPD contents, suppliers of JEDEC compliant modules must set the write protect bits for SPD device blocks 0 through 8. See the SPD5118 Device Specification for details on the block protect command protocol.

Blocks 0~1: Base Configuration, DRAM, and Module Parameters

These blocks define the parameters for LPDDR5/5X SDRAMs and limited parameters for the modules. Limited module information is being retained in blocks 0~1 to reduce enable greater firmware reuse for systems utilizing LPDDR3 and LPDDR4 SPD standard byte definitions prior to the creation of this LPDDR5/5X standard.

Block 2: Reserved for Future Use

Blocks 3~6: Module Specific Parameters

Bytes 192~447 (0x0C0~0x1BF). Parameters in this block are specific to the module type as selected by the contents of SPD Key Byte 3 bits 3~0. Refer to the appropriate annex for detailed byte descriptions.

7 Address Map (cont'd)

Block 7: Reserved for future use

Bytes 448~509 are reserved and must be programmed as 0.

Byte 510 (0x1FE): Cyclical Redundancy Code (CRC) for SPD Bytes 0~509, Least Significant Byte
Byte 511 (0x1FF): Cyclical Redundancy Code (CRC) for SPD Bytes 0~509, Most Significant Byte

This two-byte field contains the calculated CRC for bytes 0~509 (0x000~0x1FD) in the SPD. The following algorithm and data structures (shown in C) are to be followed in calculating and checking the code.

```
int Crc16 (char *ptr, int count)
{
   int crc, i;

   crc = 0;
   while (--count >= 0) {
      crc = crc ^ (int)*ptr++ << 8;
      for (i = 0; i < 8; ++i)
         if (crc & 0x8000)
            crc = crc << 1 ^ 0x1021;
         else
            crc = crc << 1;
   }
   return (crc & 0xFFFF);
}

char spdBytes[] = { SPD_byte_0, SPD_byte_1, ..., SPD_byte_N-1 };
int data16;

data16 = Crc16 (spdBytes, sizeof(spdBytes));
SPD_byte_510 = (char) (data16 & 0xFF);
SPD_byte_511 = (char) (data16 >> 8);
```

Blocks 8~9: Manufacturing Information

Bytes 512~639 (0x200~0x27F). The following table details the location of each byte in this block.

Byte Number		Function Described	Notes
512	0x200	Module Manufacturer's ID Code, First Byte	1
513	0x201	Module Manufacturer's ID Code, Second Byte	1
514	0x202	Module Manufacturing Location	1
515~516	0x203~0x204	Module Manufacturing Date	1
517~520	0x205~0x208	Module Serial Number	1
521~550	0x209~0x226	Module Part Number	1
551	0x227	Module Revision Code	
552	0x228	DRAM Manufacturer's ID Code, First Byte	1
553	0x229	DRAM Manufacturer's ID Code, Second Byte	1
554	0x22A	DRAM Stepping	
555~639	0x22B~0x27F	Module Manufacturer's Specific Data	
NOTE 1 Required byte			

Blocks 10~15: End User Programmable

Bytes 640~1023 (0x280~0x3FF). Bytes in these blocks are reserved for use by end users. Module manufacturers should not assert write protect on blocks 10~15 unless requested to do so by customers.

ASCII Decode Matrix for SPDs

Table 7 is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

Table 7 — ASCII Decode Matrix for SPDs

First Hex Digit in Pair	Second Hex Digit in Pair															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	Blank Space								(	)				- Dash	. Period	
3	0	1	2	3	4	5	6	7	8	9						
4		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z					_ Under-score
6		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z					

Examples:

0x20 = Blank Space
0x34 = '4'
0x41 = 'A'

SPD Bytes 521~550	
Manufacturer's PN	**Coded in ASCII**
13M32734BCD-260Y	31334D33323733344243442D323630592020

8 Details of Each Byte

8.1 Blocks 0 and 1: General Configuration Section: Bytes 0~127 (0x000~0x07F)

This section defines parameters common to all modules with LPDDR5 or LPDDR5X SDRAM as the media type and provides “key bytes” to allow overlay of module specific information. These bytes are defined when Key Byte 2 contains 19 (0x13) for LPDDR5 SDRAM or 21 (0x15) for LPDDR5X SDRAM.

Table 8 — General Configuration Section: Bytes 0~127 (0x000~0x07F)

Byte Number		LPDDR5/5X Function Defined	Notes
0	0x000	Number of Bytes in SPD Device and Beta Level	
1	0x001	SPD Revision for Base Configuration Parameters	
2	0x002	Key Byte / Host Bus Command Protocol Type	
3	0x003	Key Byte / Module Type	
4	0x004	SDRAM Density and Banks	1
5	0x005	SDRAM Addressing	1
6	0x006	SDRAM Package Type	1
7	0x007	Reserved - Must be coded as 0x00	
8	0x008	Reserved - Must be coded as 0x00	
9	0x009	Optional SDRAM Features	1
10	0x00A	Reserved - Must be coded as 0x00	
11	0x00B	Reserved - Must be coded as 0x00	
12	0x00C	Module Organization	1
13	0x00D	Bus Width	
14	0x00E	Reserved - Must be coded as 0x00	
15	0x00F	Reserved - Must be coded as 0x00	
16	0x010	Signal Loading	1
17	0x011	Timebases	
18	0x012	Minimum Cycle Time (t_{CKAVG}min), MTB	1
19	0x013	Maximum Cycle Time (t_{CKAVG}max), MTB	1
20	0x014	Reserved - Must be coded as 0x00	
21	0x015	Reserved - Must be coded as 0x00	
22	0x016	Reserved - Must be coded as 0x00	
23	0x017	Reserved - Must be coded as 0x00	
24	0x018	Minimum CAS Latency Time (t_{AA}min), MTB	1
25	0x019	Reserved - Must be coded as 0x00	1
26	0x01A	Minimum RAS to CAS Delay Time (t_{RCD}min), MTB	1
27	0x01B	All Banks Minimum Row Precharge Delay Time (t_{RPab}min), MTB	1
28	0x01C	Per Bank Minimum Row Precharge Delay Time (t_{RPpb}min), MTB	1
29	0x01D	All Banks Minimum Refresh Recovery Delay Time (t_{RFCab}min), MTB, LSB	1

Table 8 — General Configuration Section: Bytes 0~127 (0x000~0x07F) (cont'd)

Byte Number		LPDDR5/5X Function Defined	Notes
30	0x01E	All Banks Minimum Refresh Recovery Delay Time (t_{RFCab}min), MTB, MSB	1
31	0x01F	Per Bank Minimum Refresh Recovery Delay Time (t_{RFCpb}min), MTB, LSB	1
32	0x020	Per Bank Minimum Refresh Recovery Delay Time (t_{RFCpb}min), MTB, MSB	1
33~119	0x021~0x077	Reserved - Must be coded as 0x00	
120	0x078	Per Bank Minimum Row Precharge Delay Time (t_{RPpb}min), FTB	1
121	0x079	All Banks Minimum Row Precharge Delay Time (t_{RPab}min), FTB	1
122	0x07A	Minimum RAS to CAS Delay Time (t_{RCD}min), FTB	1
123	0x07B	Minimum CAS Latency Time (t_{AA}min), FTB	1
124	0x07C	Maximum Cycle Time (t_{CKAVG}max), FTB	1
125	0x07D	Minimum Cycle Time (t_{CKAVG}min), FTB	1
126~127	0x07E~0x07F	Reserved -- must be coded as 0x00	
NOTE 1 From LPDDR5/5X SDRAM data sheet.			

(LPDDR5/5X): Number of Bytes in SPD Device and Beta Level Byte 0 (0x000)

Bits 6~4 define the total size of the serial memory used to hold the Serial Presence Detect data. Bits 7,3~0 define the Beta Level of the SPD encoding.

Number of Bytes in SPD Device		
Bit 7	**Bits 6~4**	**Bits 3~0**
Beta Level 4	**SPD Bytes Total**	**Beta Level 3~0**
See bits 3~0	000: Undefined 001: 256 010: 512 011: 1024 (e.g., SPD5118) 100: 2048 (e.g., ESPD5216) All others reserved	Bits 7, 3~0: Beta Level Values 0 to 31
NOTE The 5-bit Beta Level field (bit 7 and bits 3~0) is the incremental documentation release level to track changes between major external publications of the SPD Contents specification, typically done once per year. This value shall be reset to 00000 upon each external release and will be visible only to JEDEC members between releases. The Beta Level applies to all sections of the document, including DRAM and module annex sections.		

(LPDDR5/5X): SPD Revision for Base Configuration Parameters Byte 1 (0x001)

This byte defines the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. Software should examine the upper nibble (Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

(LPDDR5/5X): SPD Revision for Base Configuration Parameters Byte 1 (0x001) (cont'd)

SPD Revision for Base Configuration Parameters										
Production Status	**SPD Revision**	**Encoding Level**				**Additions Level**				**Hex**
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	
Pre-production	Revision 0.0	0	0	0	0	0	0	0	0	00
	Revision 0.1	0	0	0	0	0	0	0	1	01
	...	.	.	.	.	.	.	.	.	.
	Revision 0.9	0	0	0	0	1	0	0	1	09
Production	Revision 1.0	0	0	0	1	0	0	0	0	10
	Revision 1.1	0	0	0	1	0	0	0	1	11
	...	.	.	.	.	.	.	.	.	...
Undefined	Undefined	1	1	1	1	1	1	1	1	FF

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

Revisions for each module specific overlay are coded in the same format so that each module type can evolve over time independent of the base configuration parameters section.

The Beta Level (SPD byte 0, bits 7,3~0) may also be used to decode changes made since the last external publication of the SPD Contents.

(LPDDR5/5X): Key Byte / Host Bus Command Protocol Type Byte 2 (0x002)

This byte is the key byte used by the system BIOS to determine how to interpret all other bytes in the SPD EEPROM. The BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. This command protocol is often based on the interface parameters for a specific memory device such as a DDR5 SDRAM, however may also be a general media interface protocol such as DDR5 NVDIMM-P. Protocol extensions such as the use of registers or data buffers must be documented in Byte 3, the Module Type byte, and such differences comprehended and accounted for by the system and memory controller. Some non-DRAM solutions called “Hybrid” use an extension of a DRAM bus protocol, such as NVDIMM-N, and use the code for the emulated DRAM protocol in this byte, such as DDR4 SDRAM.

Key Byte / Host Bus Command Protocol Type		
Line #	**Hex**	**SDRAM / Module Type Corresponding to Key Byte**
0	00	Reserved
1	01	Fast Page Mode
2	02	EDO
3	03	Pipelined Nibble
4	04	SDRAM
5	05	ROM
6	06	DDR SGRAM
7	07	DDR SDRAM
8	08	DDR2 SDRAM
9	09	DDR2 SDRAM FB-DIMM
10	0A	DDR2 SDRAM FB-DIMM PROBE
11	0B	DDR3 SDRAM
12	0C	DDR4 SDRAM
13	0D	Reserved
14	0E	DDR4E SDRAM
15	0F	LPDDR3 SDRAM
16	10	LPDDR4 SDRAM
17	11	LPDDR4X SDRAM
18	12	DDR5 SDRAM
19	13	LPDDR5 SDRAM
20	14	DDR5 NVDIMM-P
21	15	LPDDR5X SDRAM
-	-	-
253	FD	Reserved
254	FE	Reserved
255	FF	Reserved

(LPDDR5/5X): Key Byte / Module Type
Byte 3 (0x003)

This byte is a Key Byte used to index the module specific section of the SPD from bytes 512~639. Byte 3 bits 3~0 identifies the SDRAM memory module type, and bits 7~4 define hybrid memory extensions.

Some modules may have no base memory, but will have only a secondary memory type. For example, a Flash-only memory module. These are classified as “hybrid” for the purposes of interpreting the SPD. Where base memory parameters apply to this class of hybrid module, these will be documented with those bytes in the base section.

LPDDR5/5X Key Byte / Module Type		
Bit 7	**Bits 6~4**	**Bits 3~0**
Hybrid	**Hybrid Media**	**Base Module Type**
0: Not hybrid (Module is DRAM only) 1: Hybrid module (See bits 6~4 for hybrid type)	000: Not hybrid 001: NVDIMM-N Hybrid 010: NVDIMM-P Hybrid All other codes reserved	0000: Reserved 0001: RDIMM 0010: UDIMM 0011: SODIMM 0100: LRDIMM 0101: CUDIMM 0110: CSODIMM 0111: MRDIMM 1000: CAMM2 1001: Reserved 1010: DDIMM 1011: Solder down 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

Base Module Type Definitions:
Solder down: Direct attachment to memory controller
RDIMM: Registered Dual In-Line Memory Module
UDIMM: Unbuffered Dual In-Line Memory Module
SODIMM: Unbuffered Small Outline Dual In-Line Memory Module
LRDIMM: Load Reduced Dual In-Line Memory Module
MRDIMM: Multiplexed Rank Dual In-Line Memory Module
DDIMM: Differential Dual In-Line Memory Module
CUDIMM: Clocked Unbuffered Outline Dual In-Line Memory Module
CSODIMM: Clocked Small Outline Dual In-Line Memory Module
CAMM2: Compression Attached Memory Module

Hybrid Memory Type Definitions:
NVDIMM-N: Non-Volatile Dual In-Line Memory Module, Hybrid module with a DDR5 SDRAM interface with one or more non-DRAM components for data storage
NVDIMM-P: Non-Volatile Dual In-Line Memory Module, Hybrid module with a DDR5 NVDIMM-P interface with one or more non-DRAM components for data storage

Examples:

0x01: RDIMM, no bybrid memory present
0x91: RDIMM, NVDIMM-N hybrid memory present
0x94: LRDIMM, NVDIMM-N hybrid memory present
0x0B: Soldered down memory, no hybrid memory present
0x08: CAMM2, no hybrid memory present

(LPDDR5/5X): SDRAM Density and Banks Byte 4 (0x004)

This byte defines the total density of each LPDDR SDRAM and the number of internal banks and bank groups into which the memory array is divided. The bank and bank group values reflected in byte 4 should align with the bank architecture associated with the maximum data rate for the LPDDR SDRAM per the JESD209-5 standard.

LPDDR5/5X SDRAM Density and Banks		
Bits 7~6	**Bits 5~4**	**Bits 3~0**
Bank Group Bits	**Bank Address Bits**	**Total SDRAM capacity, per die, in Gigabits**
00: No bank groups 01: 2 Bank groups 10: 4 Bank groups 11: Reserved	00: 4 Banks 01: 8 Banks 10: 16 Banks All others reserved	0000: Reserved 0001: Reserved 0010: 1 Gb 0011: 2 Gb 0100: 4 Gb 0101: 8 Gb 0110: 16 Gb 0111: 32 Gb 1000: 12 Gb 1001: 24 Gb 1010: 3 Gb 1011: 6 Gb All others reserved

(LPDDR5/5X): SDRAM Addressing Byte 5 (0x005)

This byte defines the row and column addressing in each SDRAM device. Bits 2~0 reflect the bank/bank group address bits in addition to the column address bits. These values comes from the LPDDR5 SDRAM data sheet.

LPDDR5/5X SDRAM Addressing		
Bits 7~6	**Bits 5~3**	**Bits 2~0**
Reserved	**Row Address Bits**	**Bank/Bank Group Address Bits + Column Address Bits**
Reserved; must be coded as 00	000: 12 rows 001: 13 rows 010: 14 rows 011: 15 rows 100: 16 rows 101: 17 rows 110: 18 rows All others reserved	000: 3 bank address bits; 6 columns 001: 4 bank/bank group address bits; 6 columns All others reserved

(LPDDR5/5X): SDRAM Package Type
Byte 6 (0x006)

This byte defines the type of SDRAM device(s) on the module. These values comes from the LPDDR5 SDRAM data sheet. Note: Bits 3~1 are defined by dividing the Total Package DQs by the DRAM Die Data Width.

LPDDR5/5X SDRAM Package Type			
Bit 7	**Bit 6~4**	**Bit 3~1**	**Bit 0**
SDRAM Package Type	**Die per SDRAM Package**	**Total Pkg DQs Divided by DRAM Die Data Width**	**Signal Loading Index[2]**
0: Monolithic DRAM Device 1: Non-Monolithic Device[1]	000: 1 die 001: 2 die 010: 3 die 011: 4 die 100: 5 die 101: 6 die 110: 16 die 111: 8 die	000: 1 001: 16 010: 2 011: Reserved 100: 4 101: Reserved 110: 8 111: Reserved	0: Not specified 1: Byte 16 Signal Loading Matrix 1
NOTE 1 This includes dual die, quad die, multi-die, or physically stacked devices - anything outside the standard monolithic device NOTE 2 Index into LPDDR5/5X byte 16 for signal loading. Monolithic devices (bit 7 = 0) should code bit 0 as 0.			

Examples:

Package Description	SDRAM Package Type	Die per SDRAM Package	Total Pkg DQs Divided by DRAM Die Data Width	Signal Loading Index
315b, 1 Rank, x16, 2 Die	1: Non-Monolithic	001: 2 die	010: 2	1: Matrix 1
315b, 2 Rank, x16, 4 Die	1: Non-Monolithic	011: 4 die	010: 2	1: Matrix 1
315b, 2 Rank, x8, 8 Die	1: Non-Monolithic	111: 8 die	100: 4	1: Matrix 1
315b, 4 Rank, x8, 16 Die	1: Non-Monolithic	110: 16 die	100: 4	1: Matrix 1

(LPDDR5/5X): Reserved
Byte 7 (0x007)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Reserved
Byte 8 (0x008)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Optional SDRAM Features
Byte 9 (0x009)

This byte defines optional SDRAM features. These values comes from the LPDDR5 SDRAM data sheet.

LPDDR5/5X Optional SDRAM Features		
Bits 7~6	**Bit 5**	**Bit 4~0**
Post Package Repair (PPR)	**Soft PPR**	**Reserved**
00: PPR not supported 01: PPR supported 10: Reserved 11: Reserved	0: Soft PPR not supported 1: Soft PPR supported	Reserved; must be coded as 00000

(LPDDR5/5X): Reserved
Byte 10 (0x00A)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Reserved
Byte 11 (0x00B)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Module Organization
Byte 12 (0x00C)

This byte defines the organization of the SDRAM module. Bits 2~0 encode the die data width of the SDRAM devices. Bits 5~3 encode the number of package ranks per sub-channel. These values come from the LPDDR5 SDRAM data sheet.

LPDDR5/5X Module Organization			
Bits 7	**Bit 6**	**Bit 5~3**	**Bits 2~0**
Reserved	**Byte Mode Identification**	**Package Ranks Per Sub-Channel**	**DRAM Die Data Width**
Reserved; must be coded as 0	0: Standard Device 1: Byte Mode Device	000: 1 Package Rank 001: 2 Package Ranks 010: 3 Package Ranks 011: 4 Package Ranks All others reserved	000: 4 bits 001: 8 bits 010: 16 bits 011: 32 bits All others reserved

“Package Ranks Per Sub-Channel” refers to the number of common chip select signals across the data width of the sub-channel such that assertion of each chip select enables a number of DRAM devices equivalent to the width of the sub-channel.

The LPDDR5/5x standard includes a byte mode feature allowing half of the I/O’s to be shared with another die, forming a single x16 channel. This function allows for doubling the capacity of the package without adding more loading on the DQ lines.

(LPDDR5/5X): System Sub-Channel Bus Width Byte 13 (0x00D)

This byte defines the bus width of the system sub-channel, in bits. E.g., Sub-channels for CAMM2 with LPDDR5/5X CAMM2s are defined as being 16 bits. Four 16-bit sub-channels form a single 64-bit channel.

LPDDR5/5X System Sub-Channel Bus Width	
Bit 7~3	**Bits 2~0**
Reserved	**System Sub-Channel Bus Width, in bits**
Reserved; must be coded as 00000	000: Reserved 001: 16 bits 010: 32 bits All others reserved

(LPDDR5/5X): Reserved Byte 14 (0x00E)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Reserved Byte 15 (0x00F)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Signal Loading Byte 16 (0x010)

This byte defines the number of loads placed on significant groups of signals within a sub-channel of the memory solution. The signal groups are data/strobe/mask, command/address/clock, and chip select. This byte is indexed from LPDDR5/5x SPD byte 6, bit 0.

LPDDR5/5X Signal Loading Matrix 1 (LPDDR5/5X Byte 6, Bit 0 = 1)		
Bits 7~6	**Bits 5~3**	**Bits 2~0**
Data/Strobe/Mask Loading	**Command/Address/Clock Loading**	**Chip Select Loading**
00: 1 load 01: 2 loads 10: 4 loads 11: Reserved All others reserved	000: 1 load 001: 2 loads 010: 4 loads 011: 8 loads All others reserved	000: 1 load 001: 2 loads 010: 4 loads 011: 8 loads All others reserved

(LPDDR5/5X): Signal Loading, Byte 16 (0x010) (cont'd)

Examples:

Package Desc.	Data/Strobe/Mask Loading	Command/Address/Clock Loading	Chip Select Loading
315b, 1 Rank, x16	00: 1 load	000: 1 load	000: 1 load
315b, 2 Rank, x16	01: 2 loads	001: 2 loads	000: 1 load
315b, 2 Rank, x8	01: 2 loads	010: 4 loads	001: 2 loads
315b, 4 Rank, x8	10: 4 loads	011: 8 loads	001: 2 loads

(LPDDR5/5X): Timebases
Byte 17 (0x011)

This byte defines a value in picoseconds that represents the fundamental timebase for fine grain and medium grain timing calculations. These values are used as a multiplier for formulating subsequent timing parameters.

LPDDR5/5X Timebases		
Bits 7~4	**Bits 3~2**	**Bits 1~0**
Reserved	**Medium Timebase (MTB)**	**Fine Timebase (FTB)**
Reserved; Must be coded as 0000	00: 125 ps All others reserved	00: 1 ps All others reserved

Relating the MTB and FTB

When a timing value tXX cannot be expressed by an integer number of MTB units, the SPD must be encoded using both the MTB and FTM. The Fine Offsets are encoded using a two's complement value which, when multipled byt the FTB yields a positive or a negative correction factor. Typically, for safety and for legacy compatibility, the MTB portion is rounded UP and the FTB correction is a negative value. The general algorithm for programming SPD values is:

```
Temp_val = tXX / MTB                          //Calculate as a real number
Remainder = Temp_val modulo 1                 // Determine if integer # MTBs
Fine_Correction = 1 - Remainder               // If needed, what correction
if(Remainder == 0) then                       // Integer # MTBs?
        tXX(MTB) = Temp_Val                   // Convert to integer
        tXX(FTB) = 0                          // No correction needed
else
        tXX(MTB) = ceiling(Temp_val)          // Round up for safety in legacy systems
        tXX(FTB) = Fine_correction * MTB/FTB  // Correction is negative offset
endif
```

To recalculate the value of tXX from the SPD values, a general formula BIOSes may use is:

```
tXX = tXX(MTB) * MTB + tXX(FTB) * FTB
```

(LPDDR5/5X): Timebases, Byte 17 (0x011) (cont'd)

Example:

t_{CKAVG}min SPD Calculations Using MTB and FTB			
Speed Bin	**t_{CKAVG}min Value Decimal**	**SPD byte 18 Decimal (Hexadecimal)**	**SPD byte 125 Decimal (Hexadecimal)**
LPDDR5-6400	1.071 ns	9 (0x09)	-54 (0xCA)
	=	(9 * 0.125) + (-54 * 0.001)	
NOTE Examples assume MTB of 0.125 ns and FTB of 0.001 ns			

Timing parameters using both MTB and FTB are:

Parameter	MTB Byte(s)	FTB Byte
t_{CKAVG}min	18 (0x012)	125 (0x07D)
t_{CKAVG}max	19 (0x013)	124 (0x07C)
t_{AA}min	24 (0x018)	123 (0x07B)
t_{RCD}min	25 (0x019)	122 (0x07A)
t_{RP}min	26 (0x01A)	121 (0x079)
t_{RC}min	27, 29 (0x01B, 0x01D)	120 (0x078)

The encoding of two's complement fine timebase offsets:

Coding		Value (Dec)	Value (Hex)	FTB Timebase
Bit 7	**Bits 6~0**			**1 ps**
0	1111111	+127	7F	+127 ps
0	1111110	+126	7E	+126 ps
...	...	...	...	
0	0000001	+1	01	+1 ps
0	0000000	0	00	0
1	1111111	-1	FF	-1 ps
1	1111110	-2	FE	-2 ps
...	...	...	...	
1	0000000	-128	80	-128 ps

Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66.. MHz mathematically yields a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the SPD establishes a minimum granularity for timing parameters of 1 ps.

Clock periods such as t_{CKAVG}min are defined to 1ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.

(LPDDR5/5X): Minimum Cycle Time (t_{CKAVG}min), MTB Byte 18 (0x012)

This byte defines the minimum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM. These values comes from the LPDDR5 SDRAM data sheets.

LPDDR5/5X Minimum Cycle Time (t_{CKAVG}min) MTB Units
Bits 7~0
Values defined from 1 to 255 0x00: Reserved

If t_{CKAVG}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{CKAVG}min (SPD byte 125) used for correction to get the actual value.

Examples:

t_{CKAVG}min (MTB units)		MTB (ns)	t_{CKAVG}min Offset (FTB units)[1]		FTB (ns)	t_{CKAVG}min Result (ns)	Use
10	0x0A	0.125	0	0	0.001	1.25	LPDDR5-6400 (800 MHz clock)
9	0x09	0.125	-58	0xC6	0.001	1.067	LPDDR5X-7500 (937.5 MHz clock)
8	0x08	0.125	-62	0xC2	0.001	0.937	LPDDR5X-8533 (1066.5 MHz clock)
7	0x07	0.125	-42	0xD6	0.001	0.833	LPDDR5X-9600 (1200 MHz clock)
NOTE 1 See SPD byte 125.							

(LPDDR5/5X): Maximum Cycle Time (t_{CKAVG}max), MTB Byte 19 (0x013)

This byte defines the maximum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM. These values comes from the LPDDR5 SDRAM data sheets.

LPDDR5/5X Maximum Cycle Time (t_{CKAVG}max) MTB Units
Bits 7~0
Values defined from 1 to 255 0x00: Reserved

If t_{CKAVG}max cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{CKAVG}max (SPD byte 124) used for correction to get the actual value.

NOTE: JESD209-5 specifies t_{CKAVG}max as 200 ns for all LPDDR5/5X speed bins. Byte 19 should be programmed with the maximum possible value of 0xFF.

(LPDDR5/5X): Reserved
Byte 20 (0x014)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Reserved
Byte 21 (0x015)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Reserved
Byte 22 (0x016)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Reserved
Byte 23 (0x017)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Minimum CAS Latency Time (t_{AA}min), MTB
Byte 24 (0x018)

This byte defines the minimum CAS Latency in medium timebase (MTB) units. These values comes from the LPDDR5 SDRAM data sheet.

LPDDR5/5X Minimum CAS Latency Time (t_{AA}min) MTB Units
Bits 7~0
Values defined from 1 to 255 0x00: Reserved

If t_{AA}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{AA}min (SPD byte 123) used for correction to get the actual value.

Examples:

t_{AA}min (MTB units)		MTB (ns)	t_{AA}min Offset (FTB units)[1]		FTB (ns)	t_{AA}min Result (ns)	Use
170	0xAA	0.125	0	0	0.001	21.25	LPDDR5/5X RL = 17,
NOTE 1 See SPD byte 123 NOTE 2 Refer to device data sheet for downbin support details.							

(LPDDR5/5X): Reserved
Byte 25 (0x019)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Minimum RAS to CAS Delay Time (t_{RCD}min), MTB
Byte 26 (0x01A)

This byte defines the minimum RAS to CAS Delay Time in medium timebase (MTB) units. This value comes from the LPDDR5 SDRAM data sheet.

LPDDR5/5X Minimum RAS to CAS Delay Time (t_{RCD}min) MTB Units
Bits 7~0
Values defined from 1 to 255 0x00: Reserved

If t_{RCD}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RCD}min (SPD byte 122) used for correction to get the actual value.

Examples:

t_{RCD}min (MTB units)		MTB (ns)	t_{RCD}min Offset (FTB units)[1]		FTB (ns)	t_{RCD}min Result (ns)	Use
144	0x90	0.125	0	0	0.001	18 ns	LPDDR5: BG Mode, DVFSC & Write Link ECC Disabled
144	0x90	0.125	0	0	0.001	18 ns	LPDDR5X: BG Mode, DVFSC & Write Link ECC Disabled, ACT-2 to Read command
NOTE 1 See SPD byte 122 NOTE 2 Refer to device data sheet for downbin support details.							

(LPDDR5/5X): All Banks Minimum Row Precharge Delay Time (t_{RPab}min), MTB
Byte 27 (0x01B)

This byte defines the All Banks Minimum Row Precharge Delay Time in medium timebase (MTB) units. This value comes from the LPDDR5 SDRAM data sheet.

LPDDR5/5X All Banks Minimum Row Precharge Delay Time (t_{RPab}min) MTB Units
Bits 7~0
Values defined from 1 to 255 0x00: Reserved

If t_{RPab}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RPab}min (SPD byte 121) used for correction to get the actual value.

(LPDDR5/5X): All Banks Minimum Row Precharge Delay Time (t_{RPab}min), MTB Byte 27 (0x01B) (cont'd)

Example:

t_{RPapb}min (MTB units)		MTB (ns)	t_{RPab}min Offset (FTB units)[1]		FTB (ns)	t_{RPab}min Result (ns)	Use
168	0xA8	0.125	0	0	0.001	21	LPDDR5/5X
NOTE 1 See SPD byte 121 NOTE 2 Device supports downbinning in lower frequency applications; see supplier data sheet							

(LPDDR5/5X): Per Bank Minimum Row Precharge Delay Time (t_{RPpb}min), MTB Byte 28 (0x01C)

This byte defines the Per Bank Minimum Row Precharge Delay Time in medium timebase (MTB) units. This value comes from the LPDDR5 SDRAM data sheet.

LPDDR5/5X Per Bank Minimum Row Precharge Delay Time (t_{RPpb}min) MTB Units
Bits 7~0
Values defined from 1 to 255 0x00: Reserved

If t_{RPpb}min cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for t_{RPpb}min (SPD byte 120) used for correction to get the actual value.

Example:

t_{RPpb}min (MTB units)		MTB (ns)	t_{RPpb}min Offset (FTB units)[1]		FTB (ns)	t_{RPpb}min Result (ns)	Use
144	0x90	0.125	0	0	0.001	18	LPDDR5/5X
NOTE 1 See SPD byte 120 NOTE 2 Device supports downbinning in lower frequency applications; see supplier data sheet							

(LPDDR5/5X): All Banks Minimum Refresh Recovery Delay Time (t_{RFCab}min), MTB Byte 29 (0x01D), LSB Byte 30 (0x01E), MSB

This byte defines the All Banks Minimum Refresh Recovery Delay Time in medium timebase (MTB) units. This value comes from the LPDDR5 SDRAM data sheet.

LPDDR5/5X All Banks Minimum Refresh Recovery Delay Time (t_{RFCab}min) MTB Units	
Byte 31	Byte 30
Bits 15~8	Bits 7~0
Values defined from 1 to 65535	

(LPDDR5/5X): All Banks Minimum Refresh Recovery Delay Time (t_{RFCab}min), MTB Byte 29 (0x01D), LSB, Byte 30 (0x01E), MSB (cont'd)

Examples:

t_{RFCab}min (MTB units)		MTB (ns)	t_{RFCab}min Result (ns)	Use
1680	0x0690	0.125	210	8 Gb LPDDR5/5X SDRAM BG or 16B Mode
2240	0x08C0	0.125	280	12 Gb LPDDR5/5X SDRAM BG or 16B Mode
2240	0x08C0	0.125	280	16 Gb LPDDR5/5X SDRAM BG or 16B Mode
3040	0x0BE0	0.125	380	24 Gb LPDDR5/5X SDRAM BG or 16B Mode
3040	0x0BE0	0.125	380	32 Gb LPDDR5/5X SDRAM BG or 16B Mode

(LPDDR5/5X): Per Bank Minimum Refresh Recovery Delay Time (t_{RFCpb}min), MTB Byte 31 (0x01F), LSB Byte 32 (0x020), MSB

This byte defines the Per Bank Minimum Refresh Recovery Delay Time in medium timebase (MTB) units. This value comes from the LPDDR5 SDRAM data sheet.

LPDDR5/5X Per Bank Minimum Refresh Recovery Delay Time (t_{RFCpb}min) MTB Units	
Byte 31	**Byte 30**
Bits 15~8	**Bits 7~0**
Values defined from 1 to 65535	

Examples:

t_{RFCpb}min (MTB units)		MTB (ns)	t_{RFCpb}min Result (ns)	Use
960	0x03C0	0.125	120	8 Gb LPDDR5/5X SDRAM BG or 16B Mode
1120	0x0460	0.125	140	12 Gb LPDDR5/5X SDRAM BG or 16B Mode
1120	0x0460	0.125	140	16 Gb LPDDR5/5X SDRAM BG or 16B Mode
1520	0x05F0	0.125	190	24 Gb LPDDR5/5X SDRAM BG or 16B Mode
1520	0x05F0	0.125	190	32 Gb LPDDR5/5X SDRAM BG or 16B Mode

(LPDDR5/5X): Reserved Bytes 33~119 (0x021~0x077)

Reserved. Must be coded as 0x00.

(LPDDR5/5X): Per Bank Minimum Row Precharge Delay Time (t_{RPpb}min), FTB Byte 120 (0x078)

This byte modifies the calculation of SPD Byte 28 (MTB units) with a fine correction using FTB units. The value of t_{RPpb}min comes from the LPDDR5 SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 28. For Two's Complement encoding, see **Relating the MTB and FTB.**

(LPDDR5/5X): All Banks Minimum Row Precharge Delay Time (t_{RPab}min), FTB Byte 121 (0x079)

This byte modifies the calculation of SPD Byte 27 (MTB units) with a fine correction using FTB units. The value of t_{RPab}min comes from the LPDDR5 SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 27. For Two's Complement encoding, see **Relating the MTB and FTB.**

(LPDDR5/5X): Minimum RAS to CAS Delay Time (t_{RCD}min), FTB Byte 122 (0x07A)

This byte modifies the calculation of SPD Byte 26 (MTB units) with a fine correction using FTB units. The value of t_{RCD}min comes from the LPDDR5 SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 26. For Two's Complement encoding, see **Relating the MTB and FTB.**

(LPDDR5/5X): Minimum CAS Latency Time (t_{AA}min), FTB Byte 123 (0x07B)

This byte modifies the calculation of SPD Byte 24 (MTB units) with a fine correction using FTB units. The value of t_{AA}min comes from the LPDDR5 SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 24. For Two's Complement encoding, see **Relating the MTB and FTB.**

(LPDDR5/5X): Maximum Cycle Time (t_{CKAVG}max), FTB Byte 124 (0x07C)

This byte modifies the calculation of SPD Byte 19 (MTB units) with a fine correction using FTB units. The value of t_{CKAVG}max comes from the LPDDR5 SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Note: JESD209-5 specifies t_{CKAVG}max as 200 ns for all LPDDR5/5X speed bins. Byte 124 should be programmed with the maximum possible value of 0x7F.

(LPDDR5/5X): Minimum Cycle Time (t_{CKAVG}min), FTB Byte 125 (0x07D)

This byte modifies the calculation of SPD Byte 18 (MTB units) with a fine correction using FTB units. The value of t_{CKAVG}min comes from the LPDDR5 SDRAM data sheet. This value is a two's complement multiplier for FTB units, ranging from +127 to -128.

Examples: See SPD byte 18. For Two's Complement encoding, see **Relating the MTB and FTB.**

(LPDDR5/5X): Reserved Byte 126 (0x07E) Byte 127 (0x07F)

Reserved. Must be coded as 0x00.

Annex Format — Blocks 3~6, 8~9, and 10~15

Blocks 3~6: Module-Specific Section: Bytes 192~447 (0x0C0~0x1BF)

This section contains SPD bytes which are specific to families DDR5 module families. Module Type Key Byte 3 is used as an index for the encoding of bytes 192~447. The content of bytes 192~447 are described in multiple annexes, one for each memory module family. These bytes are write protected.

Blocks 8~9: Module Supplier's Data: Bytes 512~639 (0x200~0x27F)

These blocks of the SPD contain information specific to the memory module assembly including module manufacturer ID, manufacturing location, and module part number.

Blocks 10~15: End User Programmable: Bytes 640~1023 (0x280~0x3FF)

These blocks of the SPD are not write protected so that end users may program any values into these bytes during system runtime or for system management.

Annex A.0 — Common SPD Bytes for All Module Types (Bytes 192~447, 0x0C0~0x1BF)

This section describes SPD bytes that are common to all module types. Some bytes, as indicated in the table, are documented in separate annexes for each module type:

- A.1: Solder Down
- A.2 through A7: Reserved
- A.8: CAMM2

Table 9 — SPD Bytes Common to All Module Types

Byte Number		Function Described
192	0x0C0	SPD Revision for SPD bytes 192~447
193	0x0C1	Hashing Sequence
194	0x0C2	SPD Manufacturer ID Code, First Byte
195	0x0C3	SPD Manufacturer ID Code, Second Byte
196	0x0C4	SPD Device Type
197	0x0C5	SPD Device Revision Number
198	0x0C6	PMIC 0 Manufacturer ID Code, First Byte
199	0x0C7	PMIC 0 Manufacturer ID Code, Second Byte
200	0x0C8	PMIC 0 Device Type
201	0x0C9	PMIC 0 Revision Number
202	0x0CA	PMIC 1 Manufacturer ID Code, First Byte
203	0x0CB	PMIC 1 Manufacturer ID Code, Second Byte
204	0x0CC	PMIC 1 Device Type
205	0x0CD	PMIC 1 Revision Number
206	0x0CE	PMIC 2 Manufacturer ID Code, First Byte
207	0x0CF	PMIC 2 Manufacturer ID Code, Second Byte
208	0x0D0	PMIC 2 Device Type
209	0x0D1	PMIC 2 Revision Number
210	0x0D2	Thermal Sensor Manufacturer ID Code, First Byte
211	0x0D3	Thermal Sensor Manufacturer ID Code, Second Byte
212	0x0D4	Thermal Sensor Device Type
213	0x0D5	Thermal Sensor Revision Number
214~229	0x0D6~0x0E5	Reserved
230	0x0E6	Module Nominal Height
231	0x0E7	Module Maximum Thickness
232	0x0E8	Reference Raw Card Used
233	0x0E9	DIMM Attributes
234	0x0EA	Module Organization
235	0x0EB	Memory Channel Bus Width
236~239	0x0EC~0x0EF	Reserved
240~447	0x0F0~0x1BF	Module Type Specific Information. These SPD bytes are unique to each module type. See the appropriate annex for the module.

(Common): SPD Revision for Module Information Byte 192 (0x0C0)

This byte defines the SPD revision for bytes 192~447. See SPD byte 1 for details.

(Common): Hashing Sequence Byte 193 (0x0C1)

This byte defines the sequence of device serial numbers used in the hashing of an attribute certificate for the authentication of a memory solution. See JESD316-5 Enhanced Serial Presence Detect Device Specification for details. If authentication is not supported, code as 0x00.

Hashing Sequence	
Bits 7~3	**Bits 2~0**
Reserved	**Serial Number Hashing Sequence**
Reserved; must be coded as 00000	000 = No authentication 001 = Algorithm 1 ESPDs DRAMs PMICs RCDs/MRCDs/CKDs TSs DBs/MDBs All other codes reserved

(Common): Module Device Information Bytes 194~213 (0x0C2~0x0D5)

This table lists the SPD byte addresses for the key components on this assembly.

Module Generic Device Information								
Device	**Manufacturer ID Code, First Byte**		**Manufacturer ID Code, Second Byte**		**Device Type**		**Device Revision**	
	Dec	**Hex**	**Dec**	**Hex**	**Dec**	**Hex**	**Dec**	**Hex**
SPD	194	0x0C2	195	0x0C3	196	0x0C4	197	0x0C5
PMIC 0	198	0x0C6	199	0x0C7	200	0x0C8	201	0x0C9
PMIC 1	202	0x0CA	203	0x0CB	204	0x0CC	205	0x0CD
PMIC 2	206	0x0CE	207	0x0CF	208	0x0D0	209	0x0D1
Thermal Sensors (TS)	210	0x0D2	211	0x0D3	212	0x0D4	213	0x0D5
NOTES: SPD = Serial Presence Detect PMIC = Power Management Integrated Circuit								

(Common): Module Device Information, Bytes 194~213 (0x0C2~0x0D5) (cont'd)

Manufacturer ID Code: Per JEP106. See SPD bytes 512~513 for an example.

Device types:

Device Types				
	Bit 7	**Bit 6**	**Bits 5 ~ 4**	**Bits 3 ~ 0**
Device	**Devices Installed**		**Reserved**	**Device Type**
SPD	0 = Not installed 1 = Installed	Reserved; must be coded as 0	Reserved. Must be coded as 00	0000: SPD5118 (see JESD300-5) 0001: ESPD5216 (see JESD316-5) All other codes reserved
PMIC 0	0 = Not installed 1 = Installed			0000: PMIC5000 (see JESD301-1) 0001: PMIC5010 (see JESD301-1) 0010: PMIC5100 (see JESD301-2) 0011: PMIC5020 (see JESD301-4) 0100: PMIC5120 (see JESD301-6) 0101: PMIC5200 (see JESD301-3) 0110: PMIC5030 (see JESD301-5) All other codes reserved
PMIC 1	0 = Not installed 1 = Installed			
PMIC 2	0 = Not installed 1 = Installed			
Thermal Sensors	0 = TS0 Not installed 1 = TS0 Installed	0 = TS1 Not installed 1 = TS1 Installed		0000: TS5111 (see JESD302-1) 0001: TS5110 (see JESD302-1) 0010: TS5211 (see JESD302-1A) 0011: TS5210 (see JESD302-1A) All other codes reserved

Device revision: This byte is coded as a major revision in bits 7~4 and minor revision in bits 3~0, each nibble expressed in BCD. For example, device stepping 3.2 would be coded as 0x32.

(Common): Reserved
Bytes 214~229 (0x0D6~0x0E5)

(Common): Module Nominal Height
Byte 230 (0x0E6)

This byte defines the nominal height (A dimension) in millimeters of the fully assembled module including heat spreaders or other added components. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions; e.g., MO-357 defines the LPDDR5/LPDDR5X CAMM2 as being 34.00 mm in height.

Module Nominal Height	
Bits 7~5	**Bits 4~0**
Reserved	**Module Nominal Height max, in mm (baseline height = 15 mm)**
Reserved; must be coded as 000	00000 = height ≤ 15 00001 = 15 < height ≤ 16 00010 = 16 < height ≤ 17 00011 = 17 < height ≤ 18 00100 = 18 < height ≤ 19 … 01010 = 24 < height ≤ 25 01011 = 25 < height ≤ 26 … 01111 = 29 < height ≤ 30 10000 = 30 < height ≤ 31 10001 = 31 < height ≤ 32 … 11111 = 45 < height

Example:

Nominal Module Height, mm	Coding, bits 4 ~ 0 Binary	Meaning, mm
34.00 (MO-357: LPDDR5/5X CAMM2)	10011	33 < height ≤ 34

(Common): Module Maximum Thickness
Byte 231 (0x0E7)

This byte defines the maximum thickness in millimeters of the fully assembled module including heat spreaders or other added components above the module circuit board surface, rounding up to the next integer. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

Module Maximum Thickness	
Bits 7 ~ 4	**Bits 3 ~ 0**
Module Maximum Thickness max, Back, in mm (Baseline Thickness = 1 mm)	**Module Maximum Thickness max, Front, in mm (Baseline Thickness = 1 mm)**
0000 = thickness ≤ 1 0001 = 1 < thickness ≤ 2 0010 = 2 < thickness ≤ 3 0011 = 3 < thickness ≤ 4 ... 1110 = 14 < thickness ≤ 15 1111 = 15 < thickness	0000 = thickness ≤ 1 0001 = 1 < thickness ≤ 2 0010 = 2 < thickness ≤ 3 0011 = 3 < thickness ≤ 4 ... 1110 = 14 < thickness ≤ 15 1111 = 15 < thickness

(Common): Reference Raw Card Used
Byte 232 (0x0E8)

This byte indicates which JEDEC reference design raw card was used as the basis for the module assembly, if any. Special reference raw card indicator, ZZ, is used when no JEDEC standard raw card reference design was used as the basis for the module design. Pre-production modules should be encoded as revision 0 in bits 7~5.

Reference Raw Card Used	
Bit 7~5	**Bits 4~0**
Design Revision	**Reference Design**
000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3 100 = Revision 4 101 = Revision 5 110 = Revision 6 111 = Reserved	00000 = A 00001 = B 00010 = C 00011 = D 00100 = E 00101 = F 00110 = G 00111 = H 01000 = J 01001 = K 01010 = L 01011 = M 01100 = N 01101 = P 01110 = R 01111 = T 10000 = U 10001 = V 10010 = W 10011 = Y 10100 = AA 10101 = AB 10110 = AC 10111 = AD 11000 = AE 11001 = AF 11010 = AG 11011 = AH 11100 = AJ 11101 = AK 11110 = Reserved 11111 = ZZ (No reference used)
NOTE 11111111 = ZZ (no JEDEC reference raw card design used)	

(Common): DIMM Attributes
Byte 233 (0x0E9)

This byte indicates the number of rows of DRAM packages (monolithic or 3D stacked) parallel to edge connector (independent of DRAM orientation) on each side of the printed circuit board, and whether the assembly is covered in a heat spreader. The temperature range applies to the SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs are at the minimum and maximum values.

Note: CAMM2 with LPDDR5/5X components will contain 1 row of DRAMs on the module.

DIMM Attributes			
Bits 7~4	**Bit 3**	**Bit 2**	**Bits 1~0**
Operating Temperature Range[1]	**Reserved**	**Heat Spreader**	**# of rows of DRAMs on Module**
0000 = A1T (-40 to +125 °C) 0001 = A2T (-40 to +105 °C) 0010 = A3T (-40 to +85 °C) 0011 = IT (-40 to +95 °C) 0100 = ST (-25 to +85 °C) 0101 = ET (-25 to +105 °C) 0110 = RT (0 to +45 °C) 0111 = NT (0 to +85 °C) 1000 = XT (0 to +95 °C)[2] All other codings reserved	Reserved; must be coded as 0	0 = Not installed 1 = Installed	00 = Undefined 01 = 1 row 10 = 2 rows 11 = 4 rows
NOTE 1 See JESD402-1 for details NOTE 2 Typical DDR5 SDRAM thermal specification is XT, 0 to +95 °C, code 1000 in bits 7~4			

(Common): Module Organization
Byte 234 (0x0EA)

This byte describes the organization of the SDRAM module. Bits 5~3 encode the number of package ranks on the module. Bit 6 describes whether the assembly has the same SDRAM density on all ranks or has different SDRAM densities on even and odd ranks.

Module Organization			
Bit 7	**Bit 6**	**Bits 5~3**	**Bits 2~0**
Reserved	**Rank Mix**	**Number of Package Ranks per Sub-Channel**	**Reserved**
Reserved; must be coded as 0	0 = Symmetrical 1 = Asymmetrical	Bit [5, 4, 3] : 000 = 1 Package Rank 001 = 2 Package Ranks 010 = 3 Package Ranks 011 = 4 Package Ranks 100 = 5 Package Ranks 101 = 6 Package Ranks 110 = 7 Package Ranks 111 = 8 Package Ranks	Reserved; must be coded as 000

(Common): Module Organization, Byte 234 (0x0EA) (cont'd)

"Package Ranks Per Sub-Channel" refers to the number of common chip select signals across the data width of the sub-channel such that assertion of each chip select enables a number of DRAM devices equivalent to the width of the sub-channel.

"Channel" refers to the data interface at the DIMM edge connector, and "Sub-channel" refers to the interface to the separate SDRAMs. For example, LPDDR5/5X CAMM2s consist of two 64-bit wide channels, each consisting of four 16-bit sub-channels for a total of eight sub-channels.

(Common): Memory Channel Bus Width Byte 235 (0x0EB)

This byte describes the width of the SDRAM memory bus on the module. Bits 2~0 encode the primary bus width. Bits 4~3 encode the bus extensions such as parity or ECC. Bits 7~5 define the number of channels on each module. Though a CAMM2 (compression attached memory module) is not technically a DIMM (dual in-line memory module), for the purposes of documentation a CAMM2 will be treated as a DIMM.

Memory Channel Bus Width		
Bits 7~5	**Bits 4~3**	**Bits 2~0**
Number of Sub-Channels per DIMM	**Bus width extension per Sub-Channel, in bits**	**Primary bus width per Sub-Channel, in bits**
Bit [7, 6, 5] : 000 = 1 sub-channel 001 = 2 sub-channels 010 = 4 sub-channels 011 = 8 sub-channels All others reserved	Bit [4, 3] : 00 = 0 bits (no extension) 01 = 4 bits 10 = 8 bits All others reserved	Bit [2, 1, 0] : 000 = 8 bits 001 = 16 bits 010 = 32 bits 011 = 64 bits All others reserved

Examples:

Number of Sub-Channels Per DIMM	Bus Width Extension Per Sub-Channel	Primary Bus Width per Sub-Channel	Byte 235 Coding	Total Data Width per DIMM	Standard Usage
2	0	32	001 00 010	64	SODIMM, UDIMM
2	4	32	001 01 010	72	ECC SODIMM, ECC UDIMM
2	8	32	001 10 010	80	EC8 RDIMM, LRDIMM, NVDIMM, MRDIMM
2	4	32	001 01 010	72	EC4 RDIMM
4	0	32	010 00 010	128	Dual-channel DDR CAMM2
8	0	16	011 00 001	128	Eight sub-channel LPDDR CAMM2

Calculating LPDDR5/5X CAMM2 Module DRAM Capacity

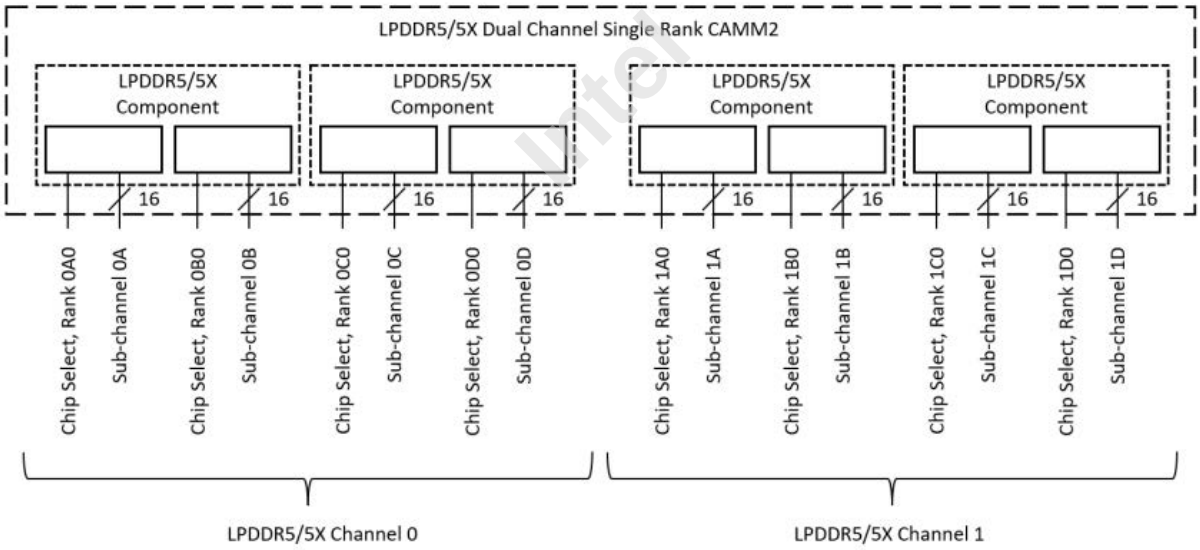
The total memory capacity of the DRAM on a DIMM may be calculated from SPD values. The following table details the SPD bytes needed for the calculation.

Package Ranks per Sub-Channel	SDRAM Density per Die	SDRAM Die Data Width	Primary Bus Width per Sub-Channel	Number of Sub-Channels per DIMM
SPD byte 234 Bits 5~3	SPD byte 4 Bits 3~0	SPD byte 12 Bits 2~0	SPD byte 235 Bits 2~0	SPD byte 235 Bits 7~5

To calculate the total capacity in bytes for a symmetric module, the following math applies:

Capacity in bytes =
Number of sub-channels per DIMM *
Primary bus width per sub-channel / SDRAM Die Data Width *
SDRAM density per die / 8 *
Package ranks per sub-channel

Example: 16 GB LPDDR5/5X CAMM2 Dual Channel 1Rx16



Number of sub-channels per DIMM (CAMM2): 8
Primary bus width per sub-channel: 16
SDRAM Die Data Width: 16
SDRAM density per die: 16 Gb
Package ranks per sub-channel: 1

Figure 1 — 16 GB LPDDR5/5X CAMM2 Dual Channel 1Rx16

(Common): Reserved
Bytes 236~239 (0x0EC~0EF)

Reserved -- must be coded as 0x00

(Common): Module Type Specific Information
Bytes 240~447 (0x0F0~0x1BF)

These bytes are specific to each module type. See the appropriate annex for definition.

Annex A.1 — Module Specific Bytes for Solder Down (Bytes 192~447, 0x0C0~0x1BF)

Revision 1.0: Byte 192 coded as 0x10

This section defines the encoding of SPD bytes 192~447 when Memory Technology Key Byte 2 contains the value 0x12 and Module Type Key Byte 3 contains any of the following:

- 0xHB, Solder Down
- where H refers to the hybrid memory architecture, if any present

See Annex A.0 for common SPD bytes 192~239 (0x0C0~0EF).

Module Specific SPD Bytes for Solder Down Memory		
Byte Number		Function Described
240~447	0x0F0~0x1BF	Reserved

Bytes 240~447 (0x0F8~0x1BF) (Solder Down):

Reserved -- must be coded as 0x00.

Annex A.8 — Module Specific Bytes for Compression Attached Memory Module Types (Bytes 192~447, 0x0C0~0x1BF)

Revision 1.0: byte 192 coded as 0x10

This section defines the encoding of SPD bytes 192~447 when Memory Technology Key Byte 2 contains the value 0x12, 0x13, or 0x15 and Module Type Key Byte 3 contains any of the following:

- 0x08, CAMM2

See Annex A.0 for common SPD bytes 192~239 (0x0C0~0EF).

Module Specific SPD Bytes for Compression Attached Memory Module Types		
Byte Number		Function Described
240	0x0F0	Clock Driver 0 Manufacturer ID Code, First Byte
241	0x0F1	Clock Driver 0 Manufacturer ID Code, Second Byte
242	0x0F2	Clock Driver 0 Device Type
243	0x0F3	Clock Driver 0 Revision Number
244	0x0F0	Clock Driver 1 Manufacturer ID Code, First Byte
245	0x0F1	Clock Driver 1 Manufacturer ID Code, Second Byte
246	0x0F2	Clock Driver 1 Device Type
247	0x0F3	Clock Driver 1 Revision Number
248~447	0x0F4~0x1BF	Reserved

(CAMM2): Module Specific Device Information Bytes 240~243 (0x0F0~0x0F3)

This table lists the SPD byte addresses for the key components on this assembly.

Module Specific Device Information								
Device	Manufacturer ID Code, First Byte		Manufacturer ID Code, Second Byte		Device Type		Device Revision	
	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex
Clock Driver (CK) 0	240	0x0F0	241	0x0F1	242	0x0F2	243	0x0F3
Clock Driver (CK) 1	244	0x0F4	245	0x0F5	246	0x0F6	247	0x0F7

(CAMM2): Module Specific Device Information, Bytes 240~243 (0x0F0~0x0F3) (cont'd)

Manufacturer ID Code: Per JEP106. See SPD bytes 512~513 for an example.
Device types:

Module Specific Device Types				
	Bit 7	**Bit 6**	**Bits 5 ~ 4**	**Bits 3 ~ 0**
Device	**Devices Installed**		**Reserved**	**Device Type**
Clock Driver (CK)	0 = Not installed 1 = Installed	Reserved; must be coded as 0	Reserved. Must be coded as 00	0000: DDR5CK01 (see JESD82-531) All other codes reserved

Device revision: This byte is coded as a major revision in bits 7~4 and minor revision in bits 3~0, each nibble expressed in BCD. For example, device stepping 3.2 would be coded as 0x32.

(CAMM2): Reserved
Bytes 248~447 (0x0F8~0x1BF)

Reserved -- must be coded as 0x00.

Blocks 8~9 — Manufacturing Information: (Bytes 512~639, 0x200~0x27F)

Byte 512 (0x200): Module Manufacturer ID Code, First Byte
Byte 513 (0x201): Module Manufacturer ID Code, Second Byte

This two-byte field indicates the manufacturer of the module, and shall be encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte 513, Bits 7~0	Byte 512, Bit 7	Byte 512, Bits 6~0
Last non-zero byte, Module Manufacturer	**Odd Parity for Byte 512, bits 6~0**	**Number of continuation codes, Module Manufacturer**
See JEP-106		See JEP-106

Examples:

Company	JEP-106		# continuation codes	SPD	
	Bank	Code		Byte 512	Byte 513
Fujitsu	1	04	0	0x80	0x04
US Modular	5	A8	4	0x04	0xA8

Byte 514 (0x202): Module Manufacturing Location

The module manufacturer shall include an identifier that uniquely defines the manufacturing location of the memory module. While the SPD specification will not attempt to present a decode table for manufacturing sites, the individual manufacturer must keep track of manufacturing location and its appropriate decode represented in this byte.

Bytes 515~516 (0x203~0x204): Module Manufacturing Date

The module manufacturer shall include a date code for the module. The JEDEC definitions for bytes 515 and 516 are year and week respectively. These bytes must be represented in Binary Coded Decimal (BCD). For example, week 47 in year 2014 would be coded as 0x14 (0001 0100) in byte 515 and 0x47 (0100 0111) in byte 516.

Bytes 517~520 (0x205~0x208): Module Serial Number

The supplier shall include a unique serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

One method of achieving this is by assigning a byte in the field from 517~520 as a tester ID byte and using the remaining bytes as a sequential serial number. Bytes 512~520 will then result in a nine-byte unique module identifier. Note that part number is not included in this identifier: the supplier may not give the same value for Bytes 517~520 to more than one DIMM even if the DIMMs have different part numbers.

Bytes 521~550 (0x209~0x226): Module Part Number

The manufacturer's part number shall be included and is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (0x20).

Byte 551 (0x227): Module Revision Code

This refers to the module revision code. While the SPD specification will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte. This revision code refers to the manufacturer's assembly revision level and may be different than the raw card revision in SPD byte 232.

Byte 552 (0x228): DRAM Manufacturer ID Code, First Byte
Byte 553 (0x229): DRAM Manufacturer ID Code, Second Byte

This two-byte field indicates the manufacturer of the DRAM on the module, and shall be encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte 553, Bits 7~0	Byte 552, Bit 7	Byte 552, Bits 6~0
Last non-zero byte, DRAM Manufacturer	**Odd Parity for Byte 552, bits 6~0**	**Number of continuation codes, DRAM Manufacturer**
See JEP-106		See JEP-106

Example: See bytes 512~513 for example manufacturer codes.

Byte 554 (0x22A): DRAM Stepping

This byte defines the vendor die revision level (often called the "stepping") of the DRAMs on the module. This byte is optional. For modules without DRAM stepping information, this byte should be programmed to 0xFF. For DRAM suppliers who use a single letter ("A", "B", etc.) for the stepping indicator, the coding shall be the uppercase ASCII code for that letter.

Bits 7~0
DRAM Stepping
Programmed in straight Hex format - no conversion needed. 00 - Valid 01 - Valid .. FE - Valid FF - Undefined (No Stepping Number Provided)

Byte 554 (0x22A): DRAM Stepping (cont'd)

Examples:

Code	Meaning
0x00	Stepping 0
0x01	Stepping 1
0x31	Stepping 3.1
0xA3	Stepping A3
0xB1	Stepping B1
0x41	Stepping A
0x4A	Stepping J
0xFF	Stepping information not provided

Bytes 555~639 (0x22B~27F): Manufacturer's Specific Data

The module manufacturer may include any additional information desired into the module within these locations.

Blocks 10~15 — End User Programmable: Bytes 640~1023 (0x280~0x3FF)

These blocks of the SPD are not write protected so that end users may program any values into these bytes during system runtime or for system management.

This page intentionally left blank

Standard Improvement Form **JEDEC Standard JESD406-5**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 10th Street North
Suite 240S
Arlington, VA 22201

Email: angies@jedec.org

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____