

Keynote 1

Accelerator Clusters: The New Supercomputer

Bill Dally

Chief Scientist and SVP Research, NVIDIA

Bio

Bill Dally joined NVIDIA in January 2009 as chief scientist, after spending 12 years at Stanford University, where he was chairman of the computer science department. Dally and his Stanford team developed the system architecture, network architecture, signaling, routing and synchronization technology that is found in most large parallel computers today. Dally was previously at the Massachusetts Institute of Technology from 1986 to 1997, where he and his team built the J-Machine and the M-Machine, experimental parallel computer systems that pioneered the separation of mechanism from programming models and demonstrated very low overhead synchronization and communication mechanisms. From 1983 to 1986, he was at California Institute of Technology (CalTech), where he designed the MOSSIM Simulation Engine and the Torus Routing chip, which pioneered “wormhole” routing and virtual-channel flow control. He is a member of the National Academy of Engineering, a Fellow of the American Academy of Arts & Sciences, a Fellow of the IEEE and the ACM, and has received the ACM Eckert-Mauchly Award, the IEEE Seymour Cray Award, and the ACM Maurice Wilkes award. He has published over 250 papers, holds over 120 issued patents, and is an author of four textbooks. Dally received a bachelor's degree in Electrical Engineering from Virginia Tech, a master's in Electrical Engineering from Stanford University and a Ph.D. in Computer Science from CalTech. He was a cofounder of Velio Communications and Stream Processors.

Keynote 2

Industry Trends in High Performance Networking

Robert Hormuth
Corporate Vice President, AMD

Abstract

Modern workloads are redefining the needs and requirements for efficient networks. Perhaps this is nowhere as obvious as the recent advances and investments in Artificial Intelligence and Machine Learning (AI/ML). Intelligent network endpoints, such as SmartNICs, are showing incredible promise for building very powerful and intelligent networks based on Ethernet. In turn, this has profound impacts on data flow and acceleration in these demanding use cases.

Bio

Robert Hormuth is Corporate Vice President, Architecture and Strategy of the Data Center Solutions Group at AMD. Robert has 35 years in the computer industry, joining AMD in 2020 after 13 years with Dell, 8 years with Intel and 11 years at National Instruments.

At AMD Robert is charged with creating a long-term system level vision for DSG and identify the technical requirements/implications to the DSG portfolio.

Robert's experience includes IO peripheral designs, x86 system design, BIOS, firmware, application software, and FPGA/ASIC design.

Robert has a B.S. in Electrical and Computer Engineering from The University of Texas at Austin and currently holds 30+ patents.

Keynote 3

Ultra-high density photonic interconnect and circuit switching up to the wafer-level with Passage

Nick Harris

Founder and CEO, Lightmatter

Abstract

Co-packaged optics (CPO) is increasingly viewed as the path forward for supercomputing and AI scale-out. However, optical fibers used in CPO solutions are large, low-density, high-cost, and expensive to route and manage. Scale-out with CPO is only part of a larger networking picture including packet switches (which are reaching physical density limits). Circuit switching with photonics is beginning to be used in large-scale machine learning applications and represents a path towards petabit per second switching. Lightmatter's Passage technology combines CPO, circuit switching, high-density photonic waveguides, and advanced 3D packaging to enable next-generation products that break through the memory wall, latency bounds, and more.

Bio

Nick Harris is the CEO and co-founder of Lightmatter, where his team is leading the evolution of computing, reducing its impact on our planet, and enabling the next great leaps in human progress through silicon photonics. Prior to founding Lightmatter, Nick was an Intelligence Community Postdoctoral Fellow and National Science Foundation Fellow at MIT, where he received his PhD in Electrical Engineering and Computer Science. Nick has authored 67 academic articles and 13 patents, and his doctoral thesis was titled "Programmable nanophotonics for quantum information processing and artificial intelligence." Nick was previously an R&D engineer working on DRAM and NAND circuits and device physics at Micron Technologies.