Cost Effective and Technically Competitive Nova Lake 8nm PCH

Negotiated $235M in value, enabled platform compatibility

Cost
NRE, IP cost coverage
Switching cost payment
30% lower die cost

Capability
Supplier Design service
Intel/3rd party IP porting
IP customization

$235M
NRE/price reduction value through ‘24-’28

Capacity
Supply assurance
Flexible supply/ purchase commitment terms

Cooperation
Engineering collaboration excellence
Roadmap based engagement

Enabling multiple generations of desktop CPU to market

YEAR	2024	2025	2026	2027
Leading Client Platform	Arrow Lake	Panther Lake	Nova Lake	Razor Lake
PCH	MTL-PCH (14nm)		NVL-PCH (8nm)	

Supporting CCG’s architectural evolution

Platform compatibility and PCIe5 upgrade across 3 CPU generations at the total lowest cost.

Reuse of external 14nm process to enable NVL product with minimal platform cost.

Team Acknowledgement:
EMS, TEG, DEG, FTE, CCG

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GEMS SHOULD PRICE MODELS

Authors: Jelena Culic-Viskota, Sandeep Kumar, Beilei Zhu
Kousik Ganesan, Ana Phillips, Daniela Stickel, Max Wu, Srini Moola

Fab-to-Finish Cost-Efficiency Unleashed: Counters Competition and Bolsters Intel's Market Position

Relationship
Trust and collaboration with Intel Products & Intel Foundry

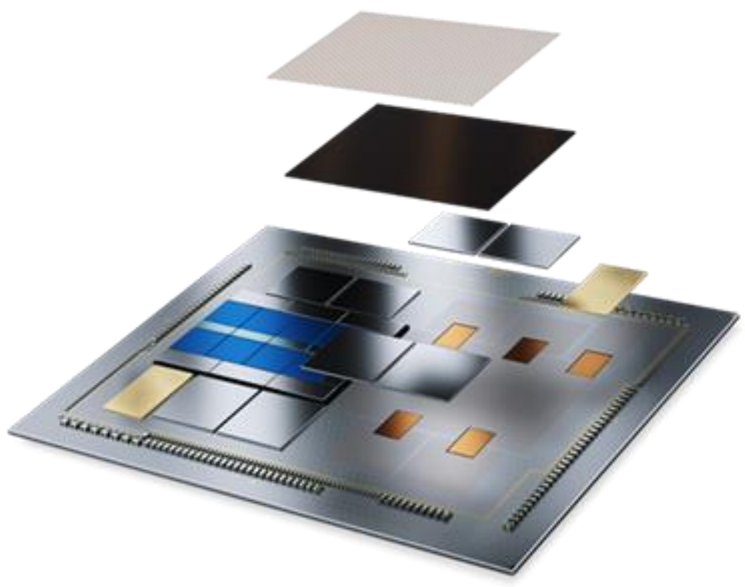
Intelligence
Validated bottoms up analysis

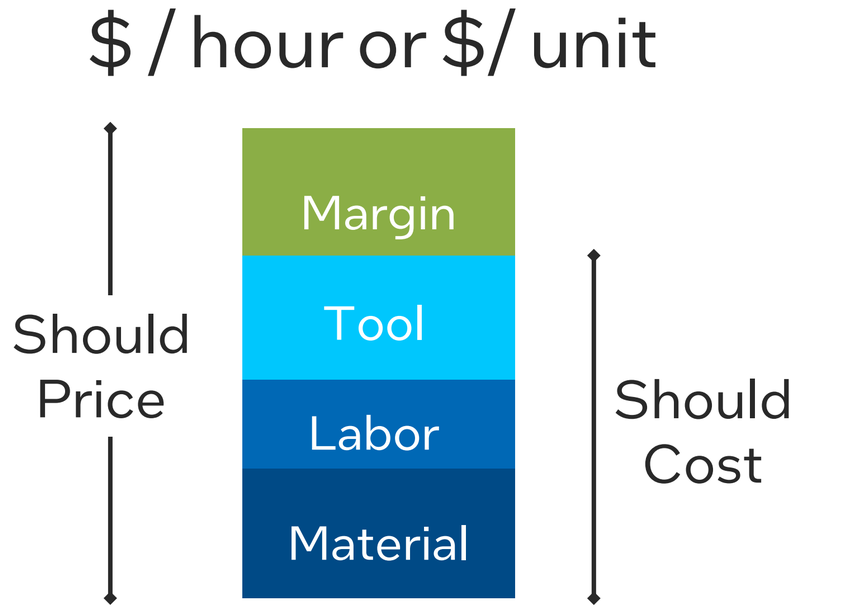
>$1B
CCG PnL Impact

Model
Cover Packaging, Sort and Test insertions

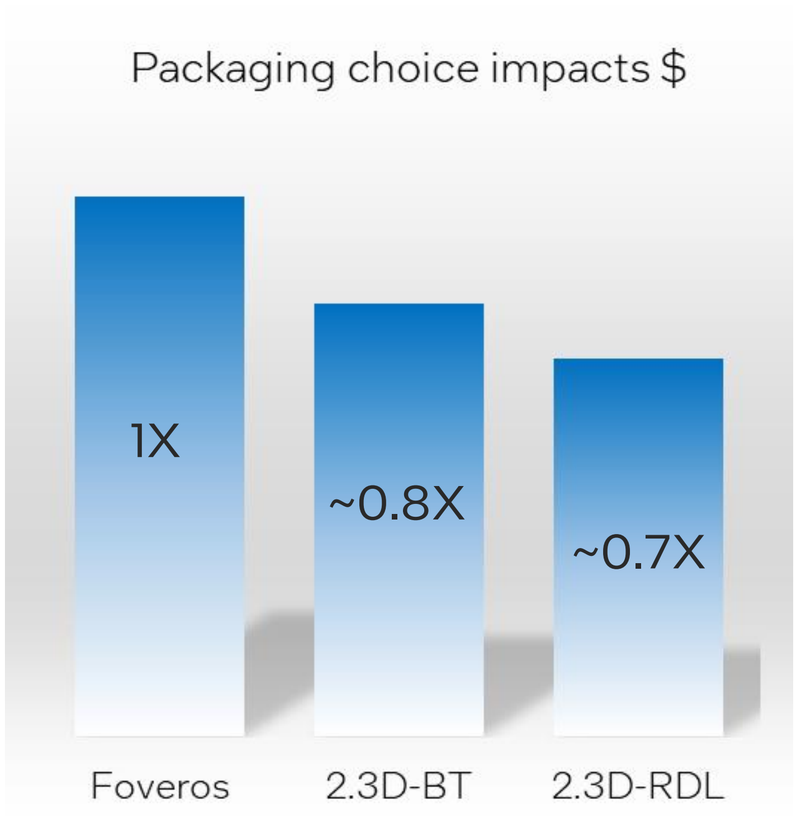
Influence
Drive pricing negotiation & Benchmarking

Methodology:





Bump and Assembly Should Price Model Report



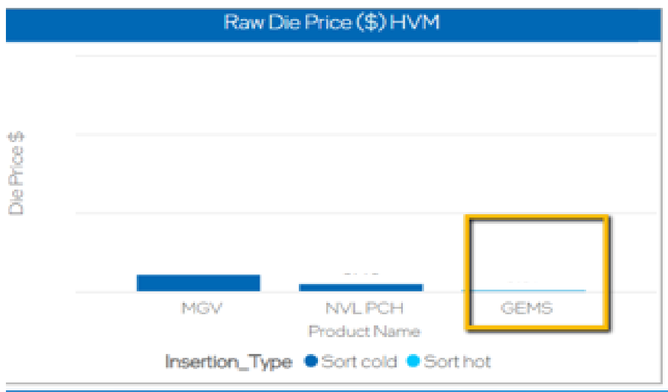
GOTO/GEMS-SPM

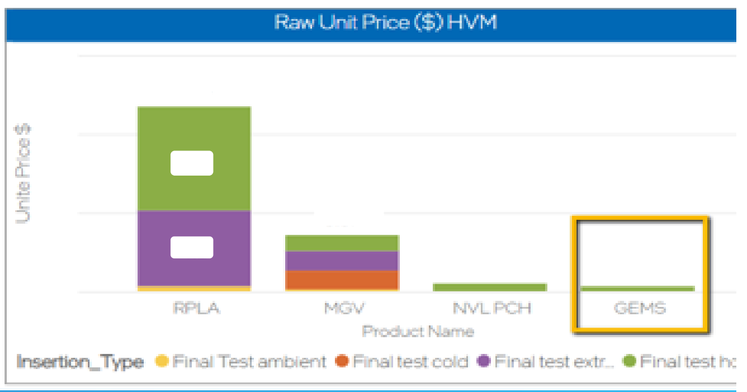
Sort and Test Should Price Model Report

Model Pricing

Product Name	Insertion Type	Raw Die $ EOL	Raw Die $ PRQ	Raw Unit $ EOL	Raw Unit $ PRQ	Sort ETT at EOL (sec)	Sort ETT at PRQ (sec)	FT ETT at EOL (sec)	FT ETT at PRQ (sec)
GEMS	Final test hot							30.00	35.00
GEMS	Sort cold					9.00	10.00		
GEMS	Sort hot					9.00	10.00		
MGV	Final Test ambient							10.00	10.00
MGV	Final test cold							75.00	75.00
MGV	Final test extreme cold							75.00	75.00
MGV	Final test hot							75.00	75.00
MGV	Sort cold					75.00	75.00		
NVL PCH	Final test hot							46.00	46.00
NVL PCH	Sort cold					42.00	42.00		

Price information hidden for security compliance





GOTO/STSPM

Azure Cloud Centralized and On-demand Analytics with Self-service Power BI

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Beilei Zhu | Jelena Culic-viskota | Daniela Stickel | Max Wu | Kousik Ganesan

Product Package Development for IDM 2.0

Enable Intel Products with Worldwide Assembly Capability and Capacity

Comprehensive product applications

Cost effectiveness

Full Portfolio of packaging solutions for IDM 2.0

Complex supply chain management

Extensive Si foundry integration

Packaging Product NPI Portfolio and Summary

CCD	CCG	WCS	NCNG	MBE	Altera	SPPD	VTG

5 Product Architectures

5 Si Foundry 10 Si nodes

8 OSAT Factories

5 Substrate Suppliers

5 Component & Memory Suppliers

22 Products

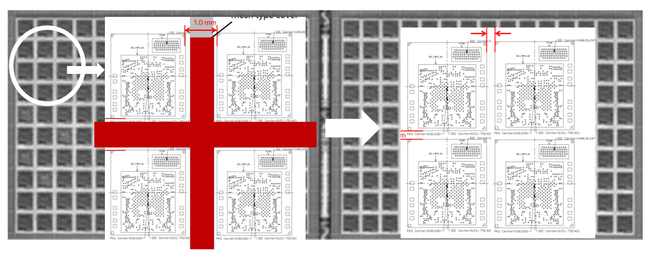
Packaging Product Development Highlights

Resilient supply chain for:

- Increase the IF flexibility: qualified first PCH (MTL/ARL PCH) w/ two OSATs .
- Enable Intel Product w/OSAT: Huddle Bay to meet cost/time req as the first Intel 16 product.

Competitive product cost:

$6M lifetime saving and ahead of time for FmP2 & WhP2 by increasing strip density.



Effective Strategy & Methodology:

- Streamline key deliverables & roadmap
- Create automatic NPI dashboards for GEMS/BUs with email/message time reduction of 15%.

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Optane's Stylish Exit

Maximize profitability through excess liability management and innovative revenue sources

Contact Authors

Excess Liabilities
Demand Generation
Scrap, Cleanup

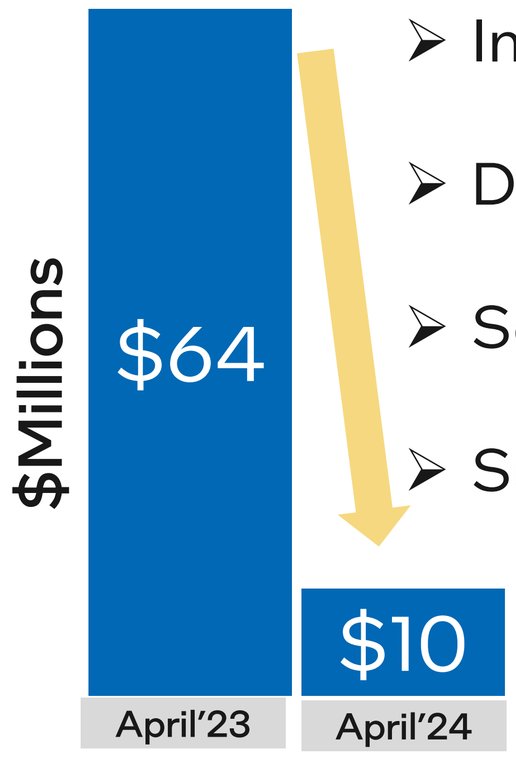
Retail Channels
Amazon
Newegg

Enhanced Profitability

Cost Mgt.
Spending Discipline
Capital Reuse & Resale

Intel Benefit
Re-purpose Excess Drives to Intel Network

IOG Excess Material Liabilities



- Inventory Management
- Demand Variability
- Scrap Avoidance
- Supplier Negotiations

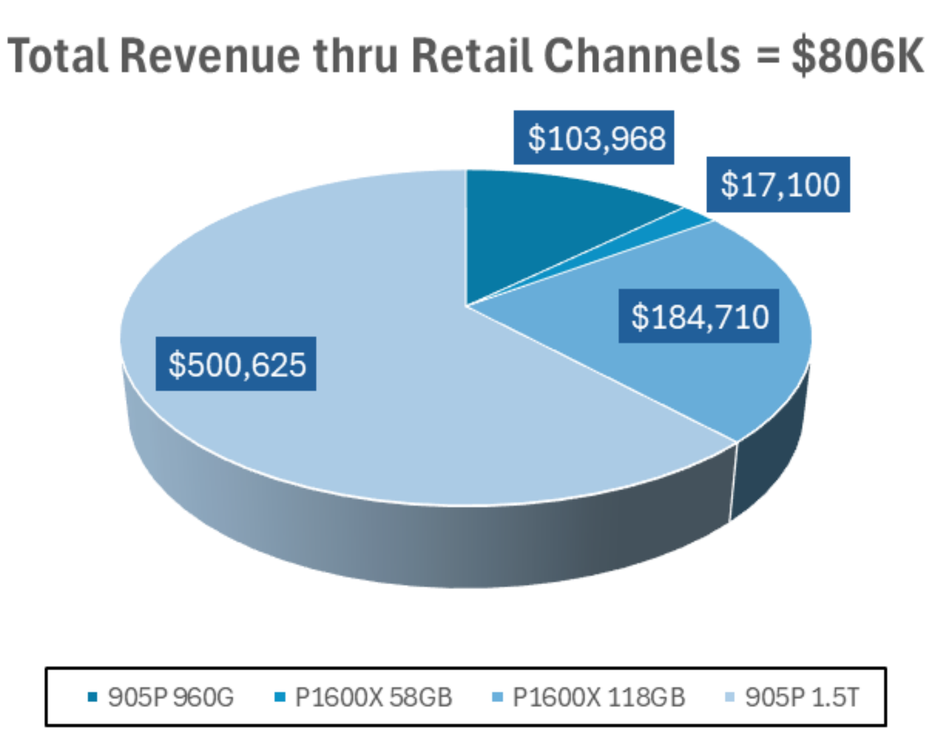
Cost Management Benefits to Intel

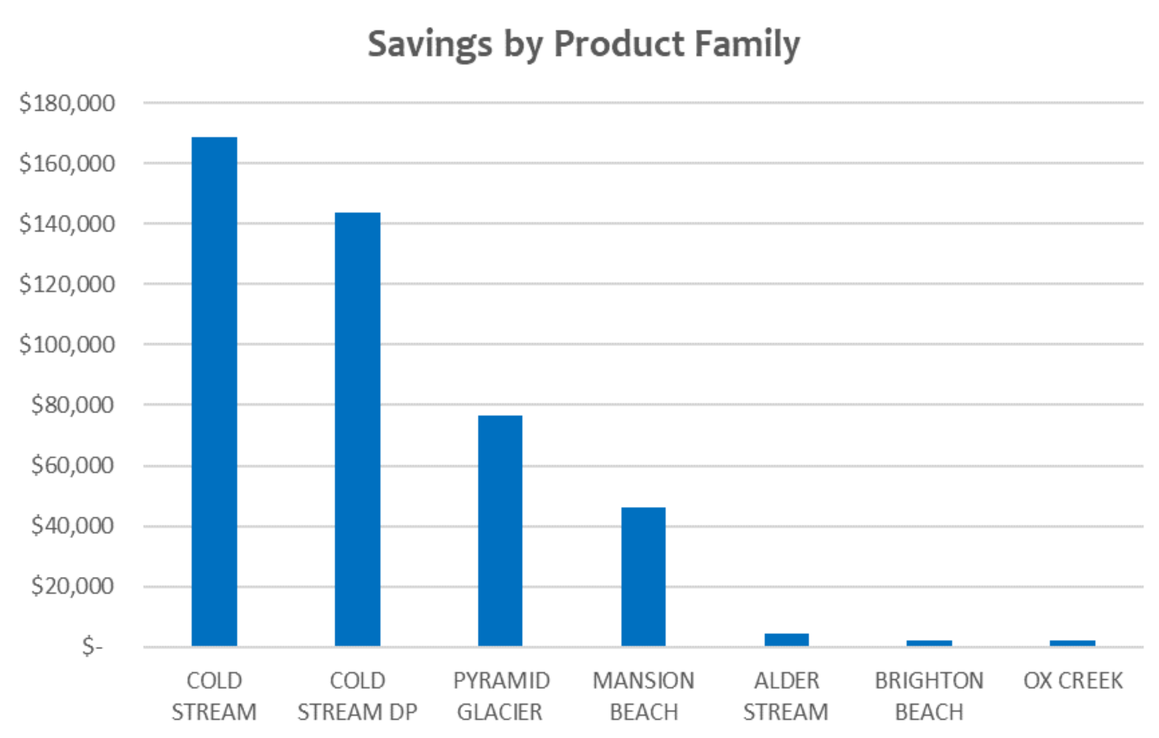
- Operating Margin Task Force
- Supplier tier pricing & negotiations
- Asset reuse and resale - >$25M cash impact to Intel

Revenue & Cost Avoidance

$806K revenue thru sales of excess client drives to Amazon and Newegg

Saved Intel **$444K** by using Intel Network to re-purpose excess drives





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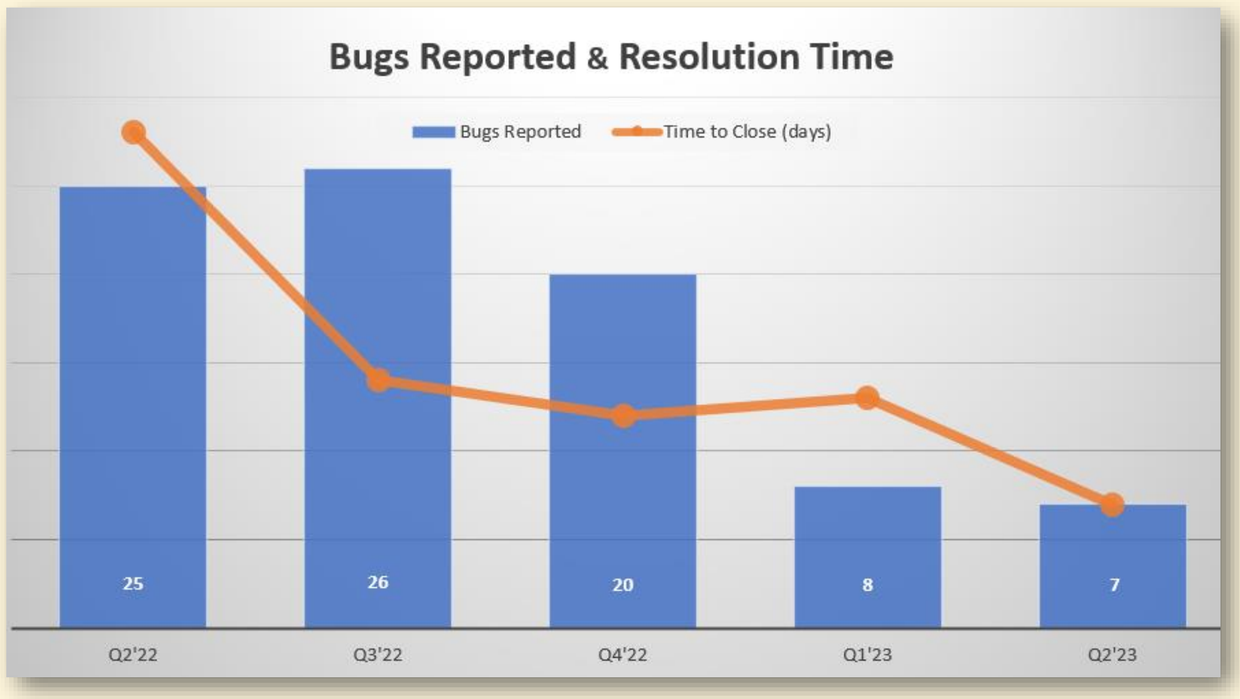
Linda Cheng | linda.cheng@intel.com

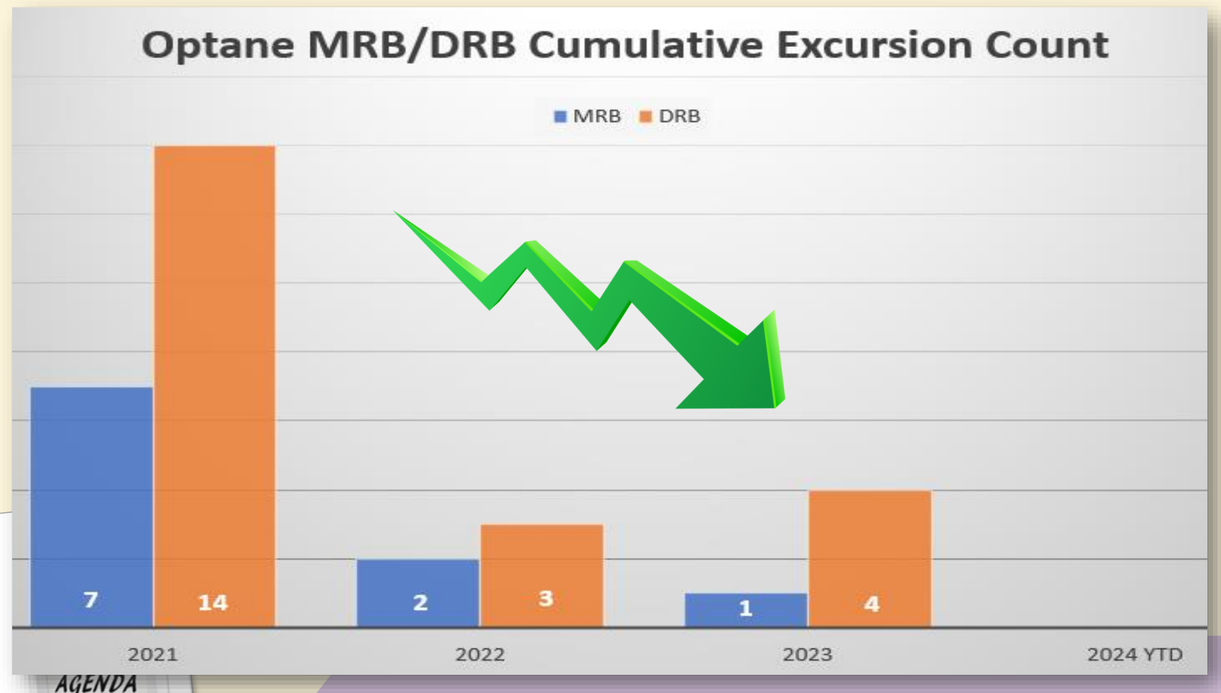
read me!

Quality First, Success Always

Impactful outcomes through a dedicated quality mindset:

- Faster response time to bug sightings & quicker implementation of new features via high coding practices in SCIPIO Supply/Demand solver overhaul.
- Reduce excursions by 75% in 2022 & 2023; 2024 YTD has 0 MRB/DRB.
- Cut down excursion closure time by 40% in 2023.
- Boost 2023 EES quality score by 15% (2024 EES results on Circuit in July).





Optane Quality Culture Refresh Class is designed to enhance understanding of Intel's commitment to quality, supported by Optane Quality Newsletter that promotes a quality mindset at work.

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Volatility and The Outsourcing Paradox

External Manufacturing Can Actually Help Intel Foundry's Bottom Line

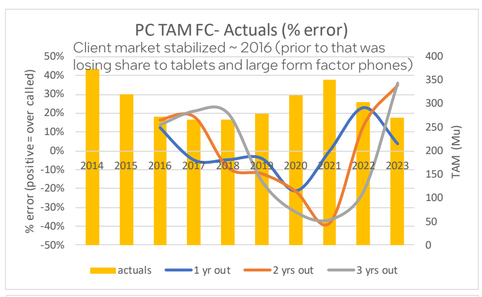
GEMS thought leadership directly helps Intel Foundry

- ~$700M of capital decisions in Q1'24 were informed by GEMS analysis
  - Volatility-based guardrails for capital pull-in/push-out are being implemented in Q2'24 LRP
- Additional projects underway to explore dual-drive opportunities to flex demand in/out to help optimize Intel Foundry internal loading while minimizing capex

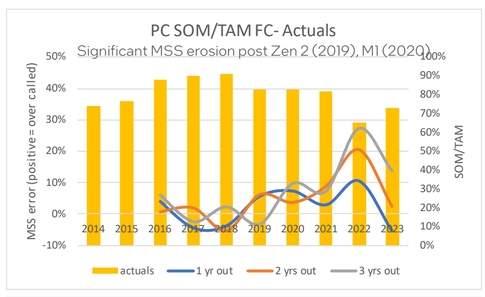
Predicting market/product demand can be challenging

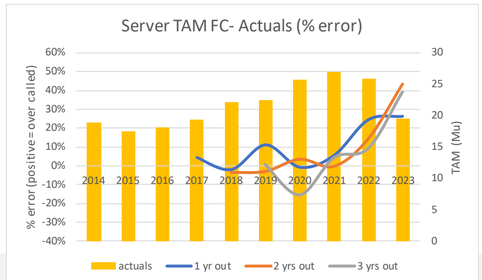
Demand Forecast Volatility

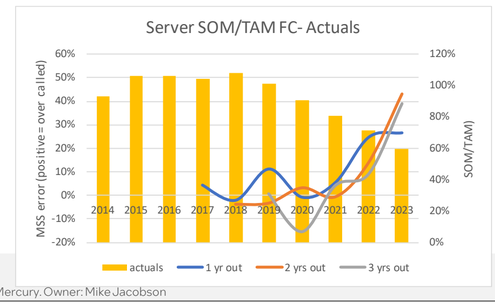
"Bullwhip Effect" for PC TAM



SOM/TAM impacted by MSS shifts







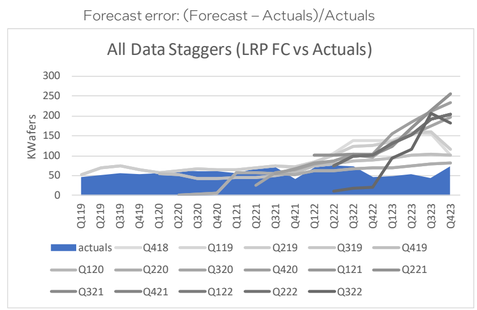
Sources: MS&F, CPC data: LRP forecasts starting 2011, TAM forecasts for years 2016+ only. 2014/15 PC data from Mercury. Owner: Mike Jacobson

And more challenging to predict wafer demand (which adds risk to capacity planning)

Forecast Variability

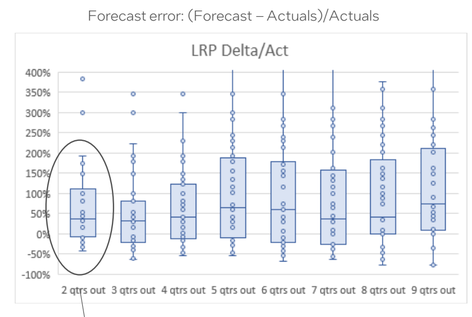
Data from Data for 5/7/16/28nm nodes across all external suppliers

Forecast error: (Forecast – Actuals)/Actuals

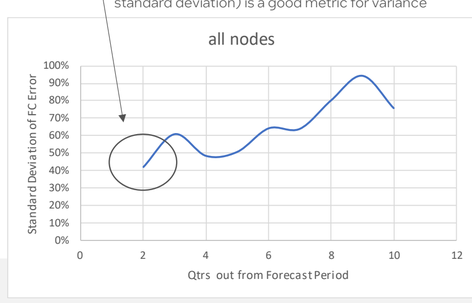


We see > 50% forecast variability for wafers

Forecast error: (Forecast – Actuals)/Actuals



Root Mean Square Error (RMSE, similar to standard deviation) is a good metric for variance

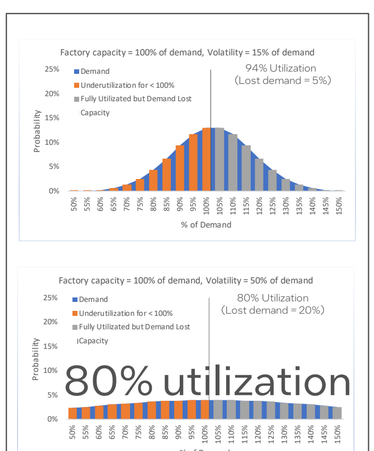


Sources: LRP Demand Q4'18 - Q3'22

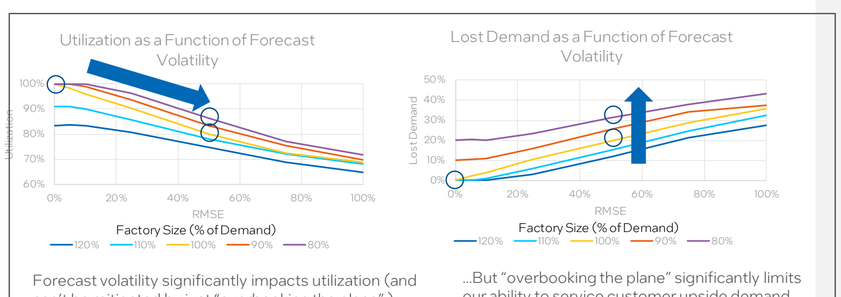
Leads to underutilization and/or lost demand upside

We have seen 50+% volatility within capacity lead time

Looking to develop sourcing strategy that maintains high internal loading by shifting volatility risk to external ("volatility insurance")



Volatility significantly "flattens" demand probability plot…Leads to lower utilization and more potential lost demand upside



Forecast volatility significantly impacts utilization (and can't be mitigated by just "overbooking the plane")

…But "overbooking the plane" significantly limits our ability to service customer upside demand…

…and can significantly impact customer goodwill

Some Sources of Volatility
- Schedule Changes
- Yield Entitlement
- Market Forecast/TAM
- Market Share Forecast (product competitiveness)
- Product mix shifts (product competitiveness)
- Customer/Product Portfolio
- Sourcing Decisions/Relationship Dynamics

"IFS helps IDM and IDM helps IFS"
–Pat @ Investor Day 2022

But Intel Foundry external customers will make forecasts more volatile (initially)

GEMS analysis based on normal demand distribution. RMSE = root mean square forecast error (volatility as a % of demand). Owner: Mike Jacobson

And can't be mitigated completely by changing factory size (relative to demand)

The size of the problem*:

- Multiple Billion $ of capex and underutilization is at risk from volatility on each new node

A robust external corridor allows:

1. Development of a "smart" sourcing strategy to help the reduce the risk to internal loadings
2. BU access to best available external process (equal to or greater than competition)
3. Access to additional capacity to help cover extreme demand upside cases

Good results but partial success so far:

Volatility analysis used in partnership with FMSC Strategic Planning to inform Intel Foundry Capacity strategy in 2024

…full benefit requires Cooperation from Intel Products, Intel Foundry, and Intel Corp. to develop comprehensive end-to-end capacity strategy

- using industry benchmarks and published capacity plans

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PRF Volatility Dashboard

Using data and transparency to reduce cost and improve supply of external wafers

Forecast volatility leads to…

Forecast Volatility

Inventory

Cash

Expedite Fees

Buy-ahead risk

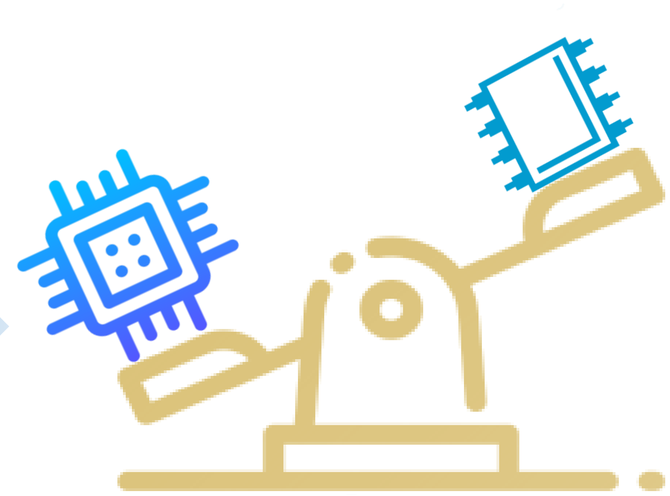
Supplier distrust

But by reducing volatility, we can…

Safely reduce safety stock

Stabilize supply → Stabilize BU impact

Avoid expedite fees/premiums



Optimized Inventory

Supplier Trust

And also…

Improve

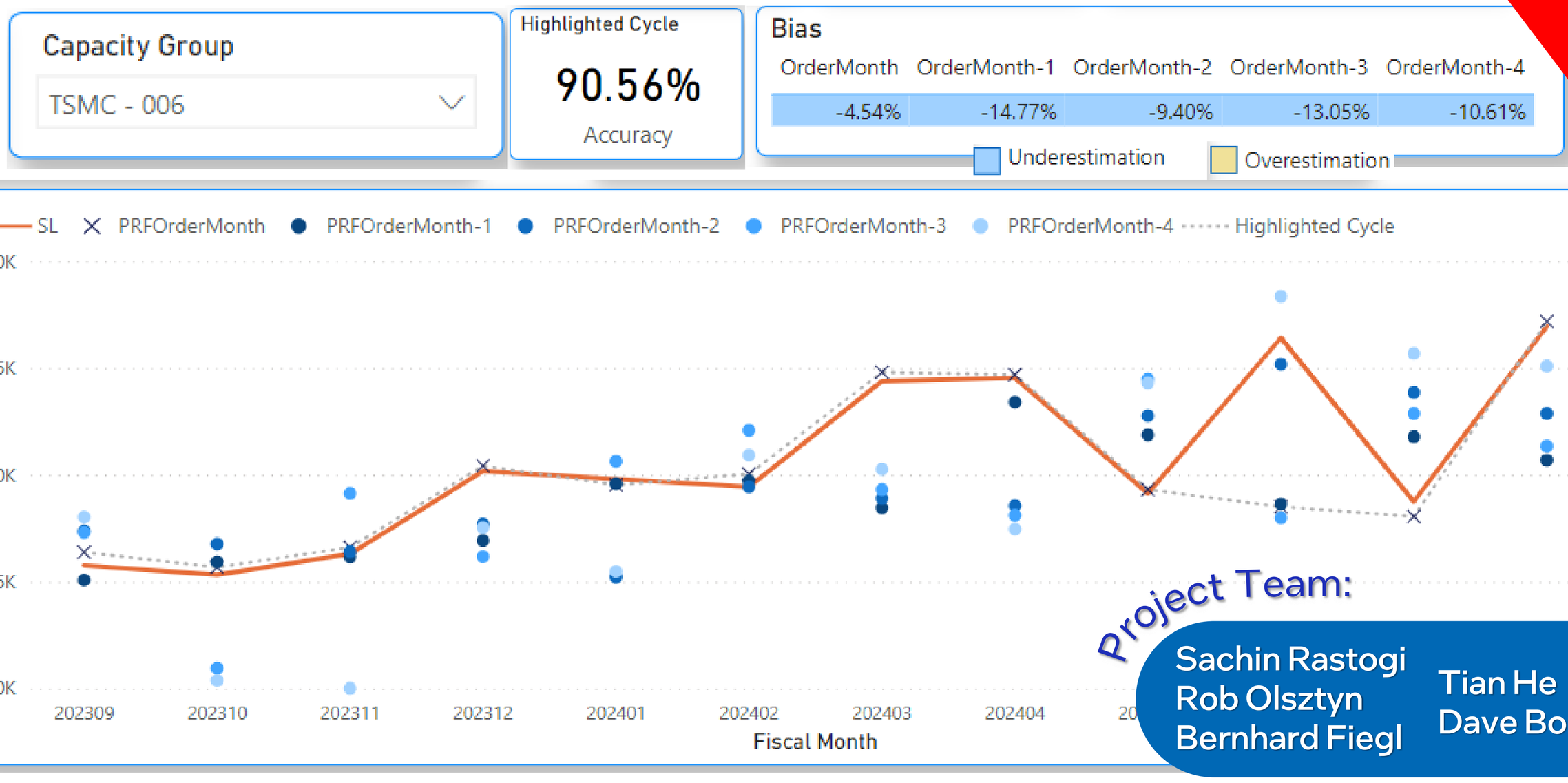
Trust

Negotiating Position

Reputation

Avoid

Supplier Forecast Judgment



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Rob Olsztyn
Bernhard Fiegl
Tian He
Dave Bonner

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Foundry Business Model Python Refactor

Foundry Business Model is a Top-Down End-to-End Profit and Loss Simulation of a Foundry

Anticipate Price Developments
Help BUs/IFS

Set Reference Prices
Support FSM

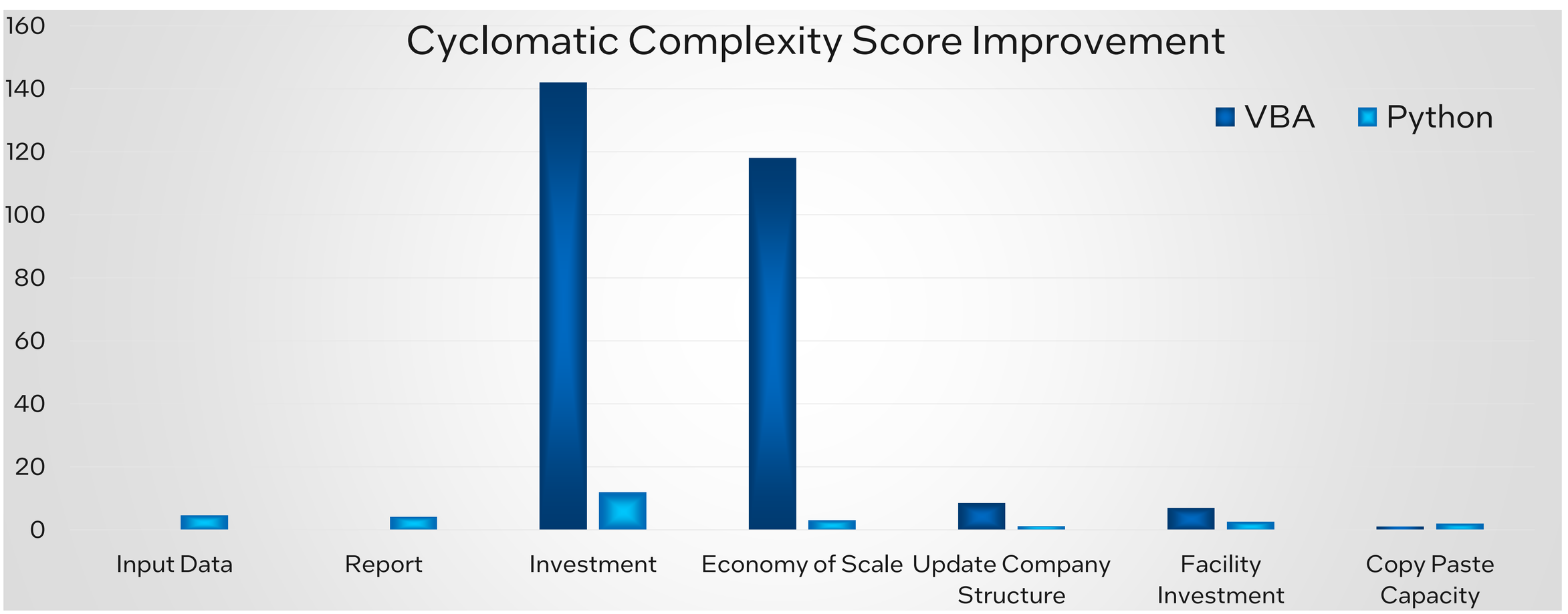
Assess Production Expenses
Aid TD/MSO

±5% Delta Compared to Actual PnL

Major Improvements

Microsoft® Excel VBA → python

Maintainability	Reduced Cyclomatic Complexity by 90%
Flexibility	Modular Code Simplifies Feature Addition
Stability	Corrected 7 Hidden Issues
Speed	91% Time Reduction



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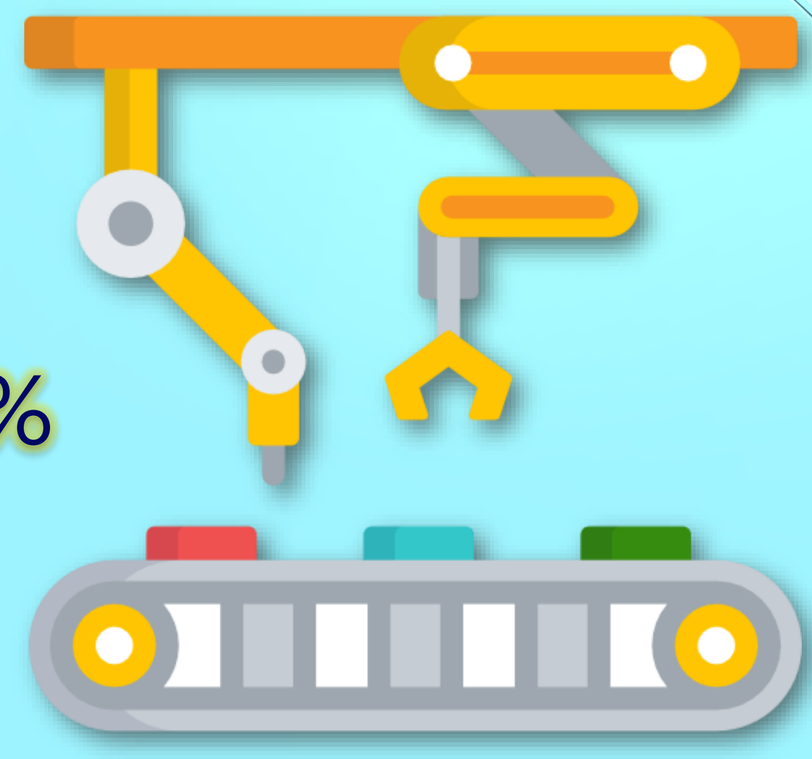
Contact us

Manufacturing Disciplines Ensure Product Yields

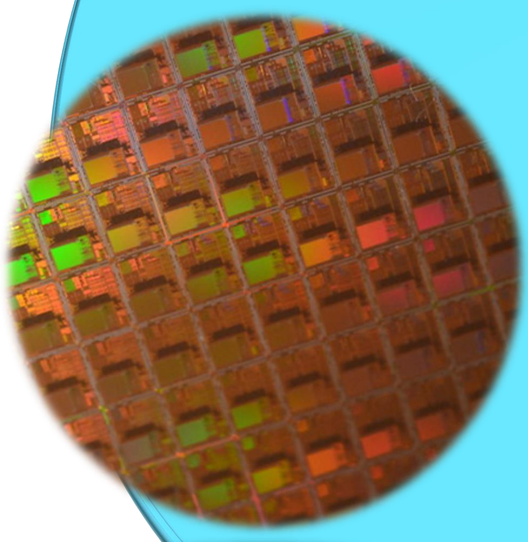
DFM, Design for Manufacture

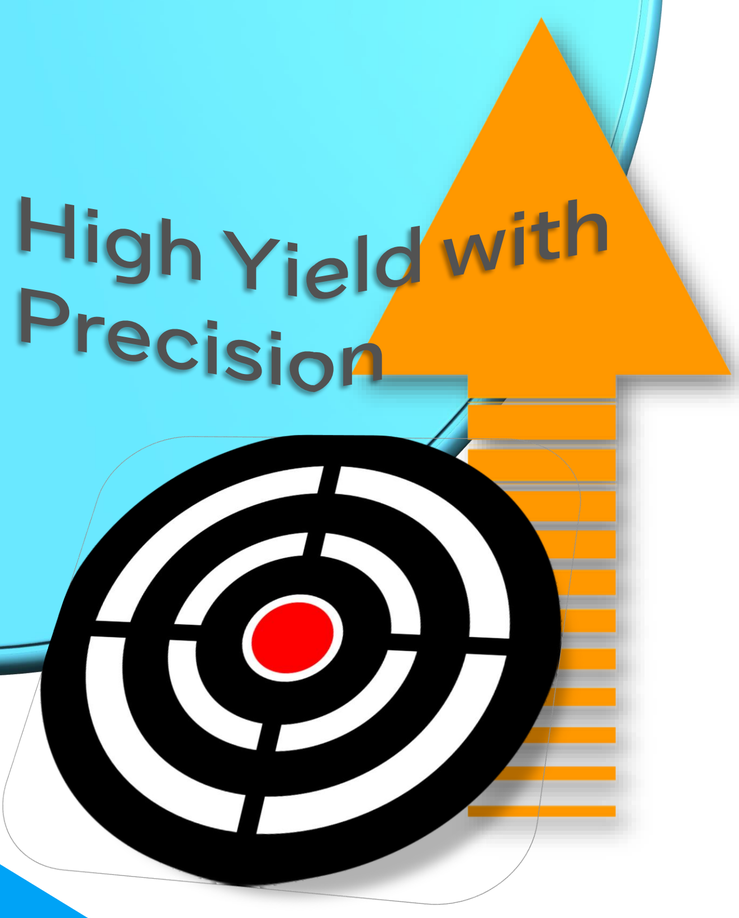
PMEM SMT Yield 99.73%



DFA, Design for Assembly Assy

PMEM Assembly Yield 99.94%





DFT, Design for Test

PMEM >99% 1st Pass Yield

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AI-Powered Manufacturing

Revolutionizing High Volume Manufacturing for Superior Yield Outcomes!

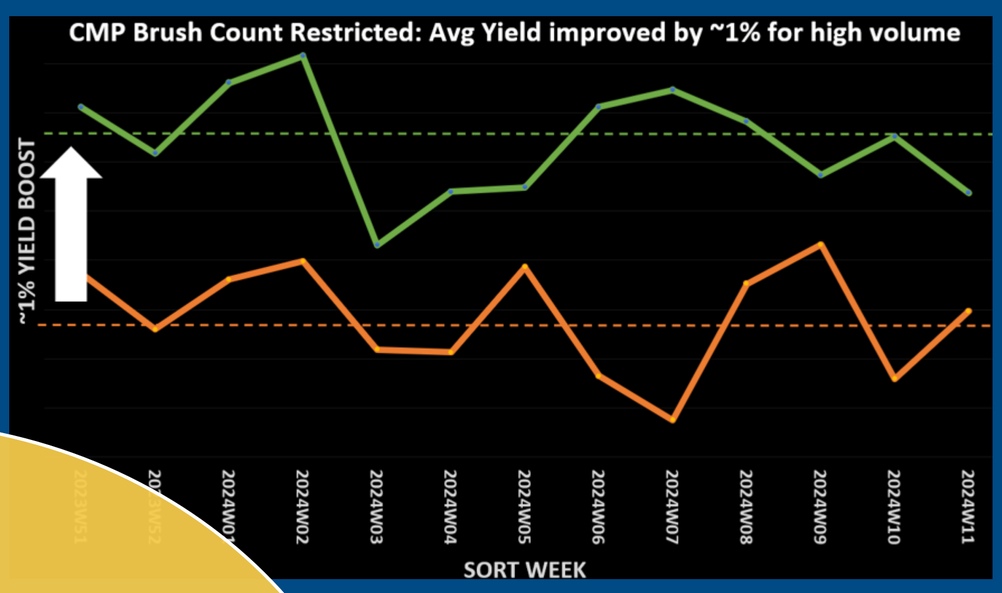
AI based EWS

AI- Early Warning System

Wafer Pattern Recognition
AI/machine learning model used into External Manufacturing HVM product flow for detecting yield defects.
Annual cost reduction of

$4M

~1% Yield Improvement
~$2M Cost Saving



14nm CMP Brush Count Restriction Success Story

Influence Multi Products

ADPS(HVM) & MTPS(NPI)

One Intel

ONE INTEL

Strong Collaboration between Intel's Cross function Departments:
AI Solutions Group & External Manufacturing EMP

Artificial Intelligence-based Wafer Auto Crash flow identified yield loss correlating to Chemical Mechanical Polishing (CMP) brush lifetime resulting into ~1% yield gain and minimum of $2M in cost saving

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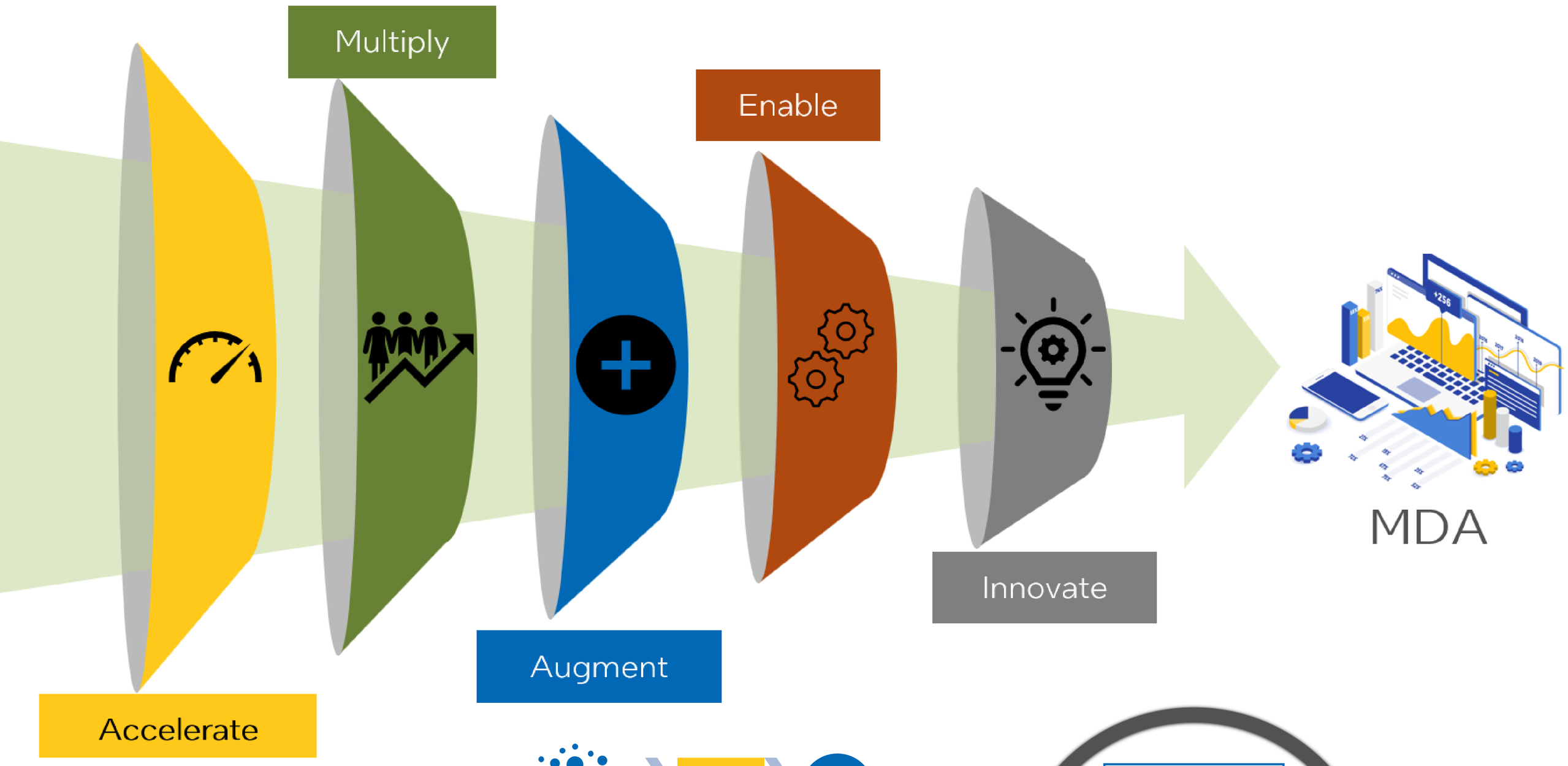
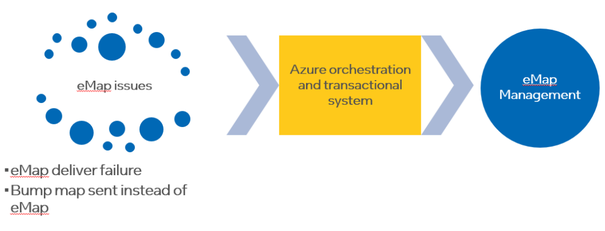
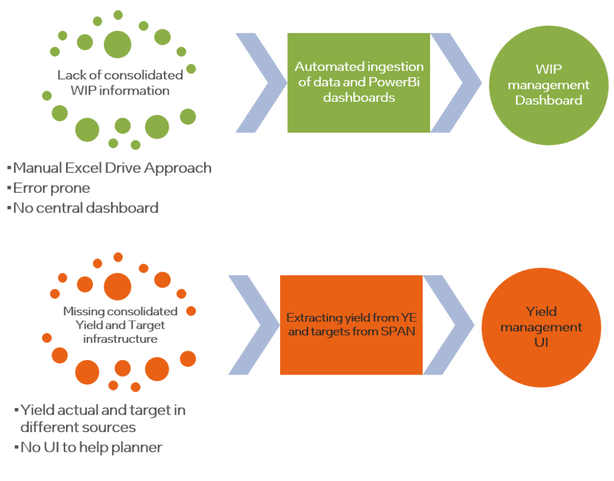
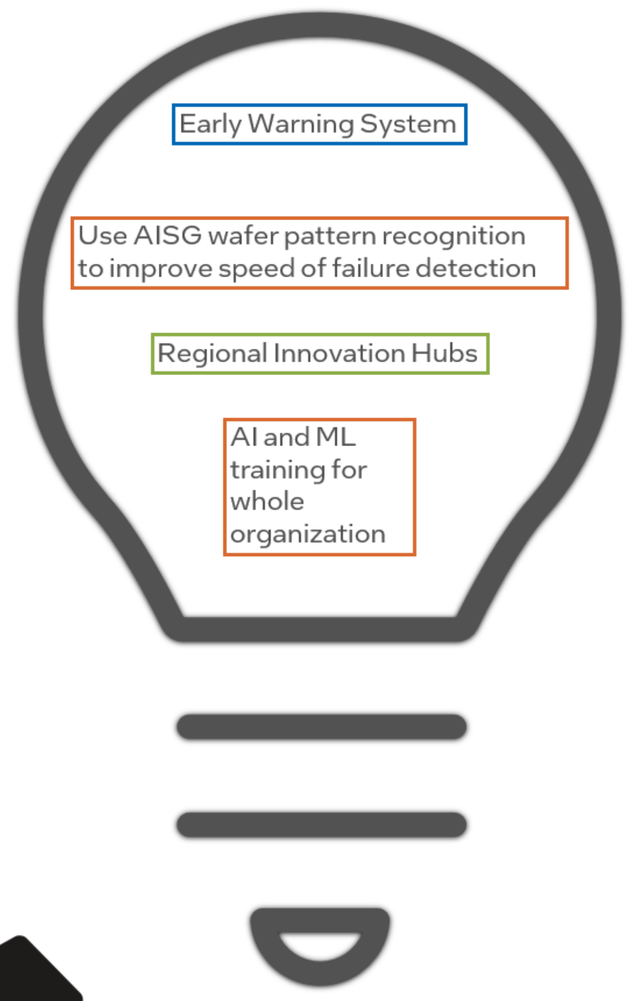
Needle in high volume manufacturing…

Enabling automation and fast external manufacturing data and KPI access.









Supported by various people from:

EMSP
EMSP OE
EMP->FM, APM, TM, MQE
FTE
EMS
Q&R

Core Team

Jeevan Kumar - DE
Arnab Chakraborty - DE
JitendraX - DE
AnkitX - DE
AravanithX - DE
Sharon Yu - DS
Yuanbo Wang – DS
Adrian Crisan

Extended Team

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Ben Sala - Optane

Rock Ke - FTE

Bernhard Fiegl – EMSP OE
Sachin Rastogi - EMSP
Jun Sung Kang – EMSP OE
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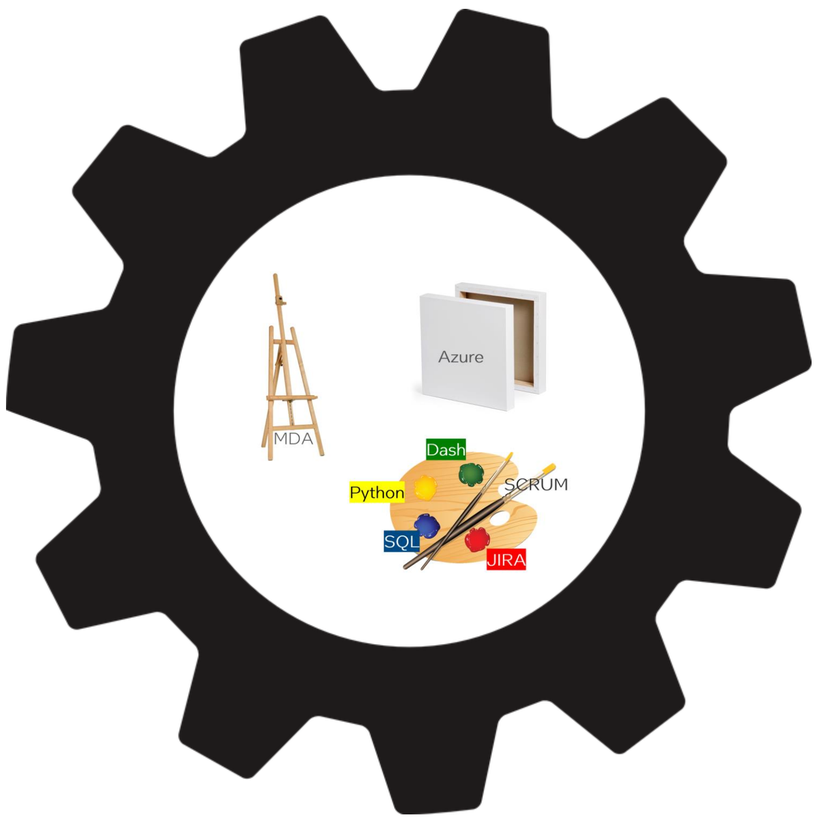

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Efficient Diagnosis / FIFA for RCA in MTL Products

More than 1.6K wafer impacted – Impacted yield ~0.6% below the Q1'24 goal

Problem
Process defect / excursion has impacted
1.6k wafers affecting ~0.6% yield

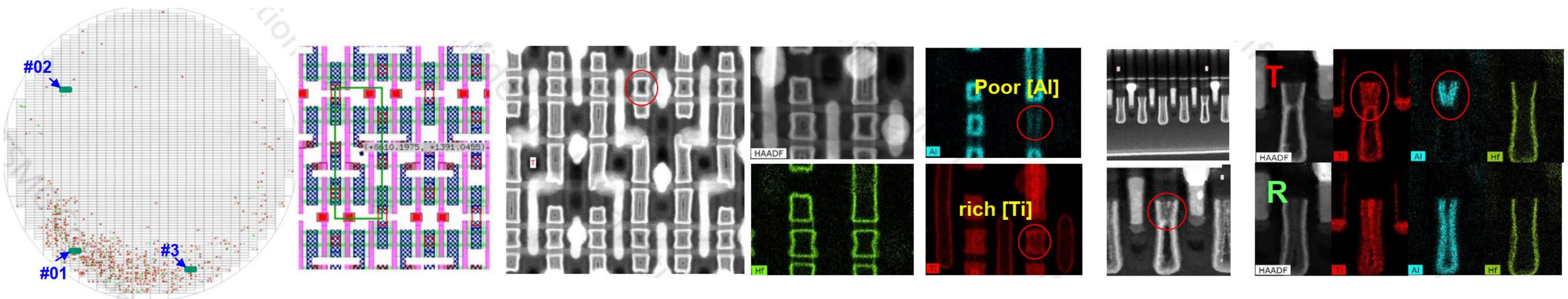
FIFA
Diagnosis / further FA delayering / TEM/EDX analysis confirmation

More than $6M savings

Root Cause
pWF remaining cannot be detected from KLA (in-line)
Cell-aware/chain diagnosis are demonstrated

CIP
Several Foundry CIP in place
3rd party FIFA vendor
Tool procedure improvement

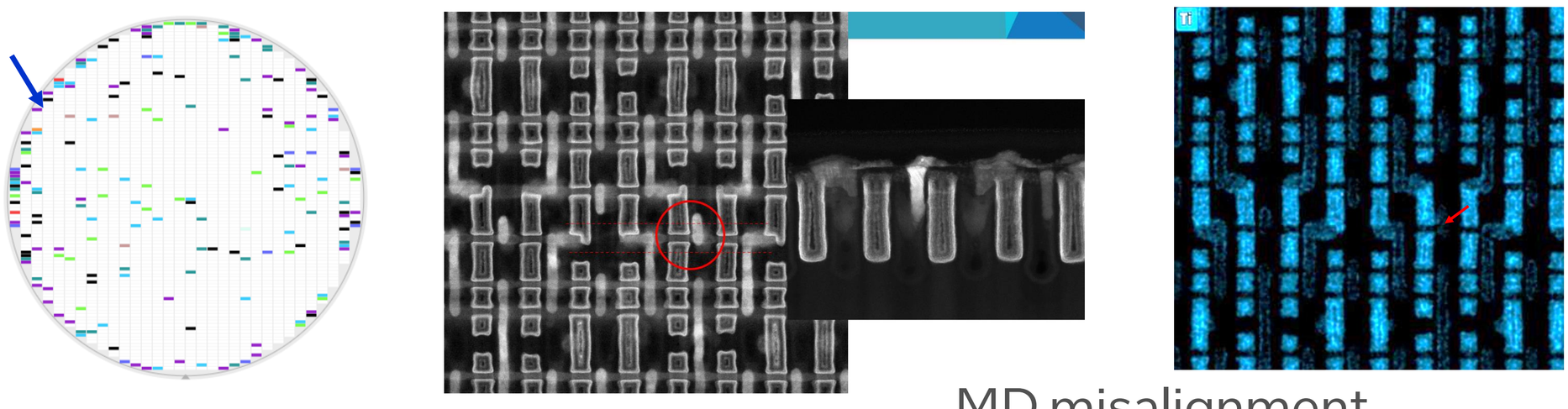
Case: I – Bin 21



pWF remaining

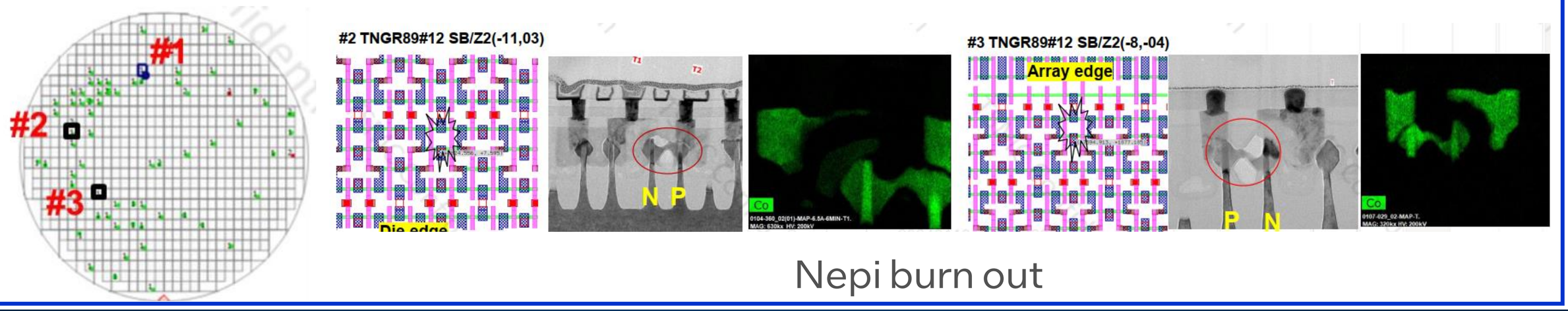
Other Cases Supported for Yield Improvement:

Case: II – Bin 8



MD misalignment

Case: III – Bin 26



Nepi burn out

Global External Manufacturing and Sourcing Poster Pop-Up 2024
Parkash Palanisamy | prakash.palanisamy@intel.com

Find Sensitive Layout Patterns

Find layout patterns that cause systematic defects in High-Volume Manufacturing Production

Rich Data
based on 50K wafers per every week

Realtime Analytic
with Volume-Diagnostic

Time-to-develop
by utilizing EDA engine

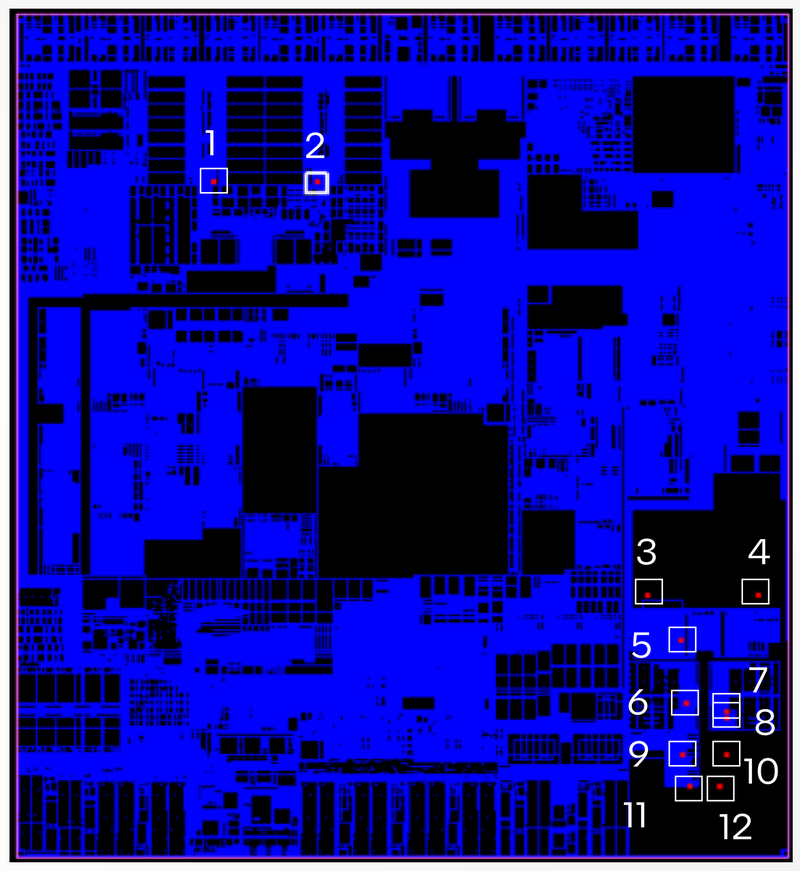
Sustainable
with layout pattern catalog database

Pattern Capture

Capture & Matching Result (Hits/ Matches)

ID#1 pattern has been repeated 12 times in entire chip layout

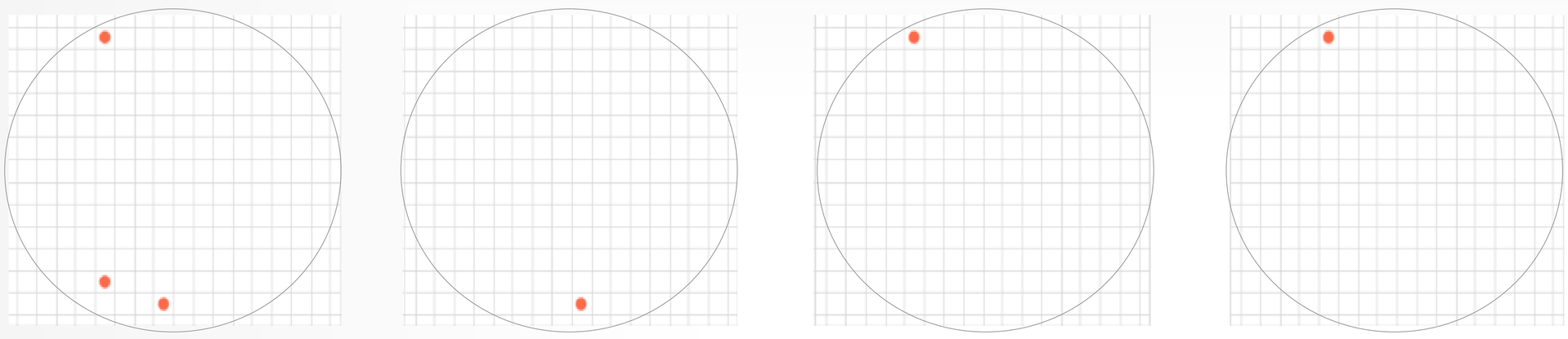
ID	Fault Type	Layers	Pattern Image	Hits	Matches
#1	Open-1	M_{N+1} V_N M_N		1	12
#2	Open-0	M_N V_{N-1} M_{N-1}		1	642
#3	Bridge -both	M_{N+3} V_{N+2} M_{N+2}		1	507
#4	Open -both	M_{N+6} V_{N+5} M_{N+5}		6	131,704,20



Pattern Analysis

Analysis Results

Certain net with ID#1 has been checked 6 times in different fail Dies (L/W/D)

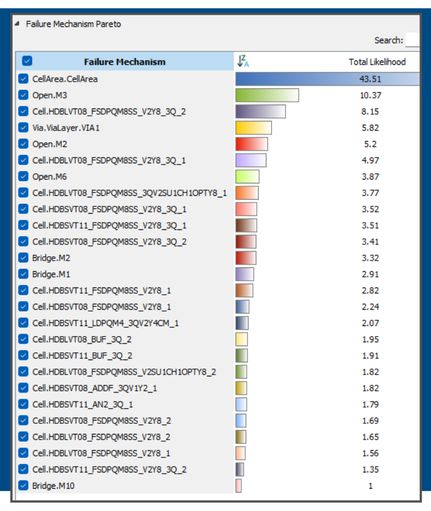


Lot A-Wafer4 | Lot B-Wafer22 | Lot C-Wafer11 | Lot C-Wafer17

Global External Manufacturing and Sourcing Poster Pop-Up 2024
Giyoung Yang giyoung.yang@intel.com
Lay Hoon Loh | Jianjun Cheng | Eric Hao Guan

Cell-Aware Diagnostics

A Technique to Refine the Failure Analysis Candidate Selection


Failure Mechanism Pareto

Search:

Failure Mechanism	Total Likelihood
CellArea.CellArea	43.51
Open.M3	10.37
Cell.HDBLVT08_FSDPQM8SS_V2Y8_3Q_2	8.15
Via.ViaLayer.VIA1	5.82
Open.M2	5.2
Cell.HDBLVT08_FSDPQM8SS_V2Y8_3Q_1	4.97
Open.M6	3.87
Cell.HDBLVT08_FSDPQM8SS_3QV2SU1CH1OPTY8_1	3.77
Cell.HDBSVT08_FSDPQM8SS_V2Y8_3Q_1	3.52
Cell.HDBSVT11_FSDPQM8SS_V2Y8_3Q_1	3.51
Cell.HDBSVT08_FSDPQM8SS_V2Y8_3Q_2	3.41
Bridge.M2	3.32
Bridge.M1	2.91
Cell.HDBSVT11_FSDPQM8SS_V2Y8_1	2.82
Cell.HDBSVT08_FSDPQM8SS_V2Y8_1	2.24
Cell.HDBSVT11_LDPQM4_3QV2Y4CM_1	2.07
Cell.HDBLVT08_BUF_3Q_2	1.95
Cell.HDBSVT11_BUF_3Q_2	1.91
Cell.HDBLVT08_FSDPQM8SS_V2SU1CH1OPTY8_2	1.82
Cell.HDBSVT08_ADDF_3QV1Y2_1	1.82
Cell.HDBSVT11_AN2_3Q_1	1.79
Cell.HDBSVT08_FSDPQM8SS_V2Y8_2	1.69
Cell.HDBLVT08_FSDPQM8SS_V2Y8_2	1.65
Cell.HDBLVT08_FSDPQM8SS_V2Y8_1	1.56
Cell.HDBSVT11_FSDPQM8SS_V2Y8_3Q_2	1.35
Bridge.M10	1

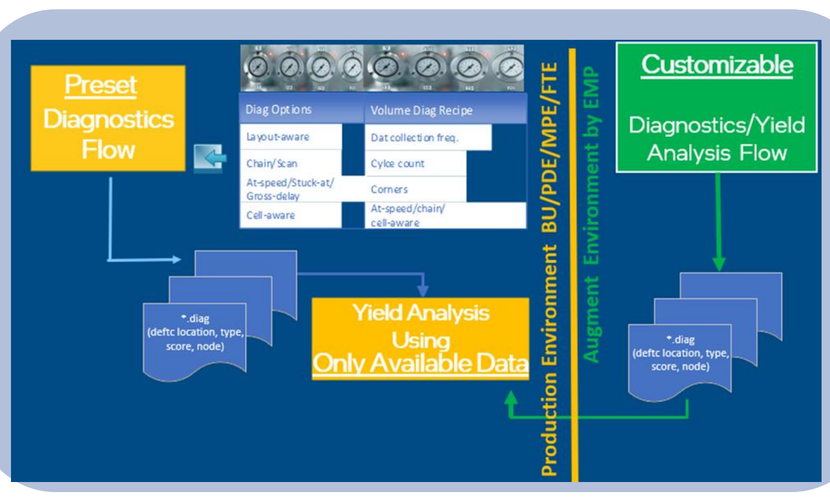
Motivation

- Cell faults can be one of the significant failure mechanisms
- Cell-aware diagnostics can enhance Physical Failure Analysis (PFA) candidate selection by pinpointing faults within specific cell locations.
- Suspect area can be reduced to 10%-1% of the cells' area

Component of Spice Netlist @Standard cell library			UDFM Need	ATPG UDFM	DFM-Aware UDFM
Parasitic	Res	X/Y	O	O	O
		BBox	O	X	O
	Cap	X/Y	O	O	O
		BBox	O	X	O
Device	MOSFET	X/Y	O	X	O

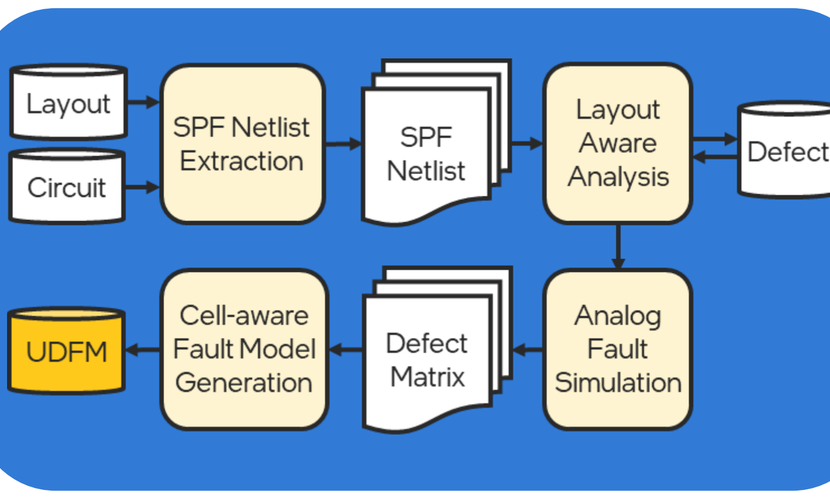
Challenges

- The absence of cell-aware patterns
- Unavailability of cell-aware diagnostics flow during production
- Unavailability of the DFM –Aware User Defined Fault Model (UDFM) library (N6)



Solutions

- Developed the augmented diagnostics flow that operates offline as needed
- Used the existing production Stuck-at patterns and failure logs for the cell-aware diagnostics
- Developed and validated the DFM-Aware UDFM library (N6)
- Validated the effectiveness of cell-aware diagnostics with a few PFAs



Results

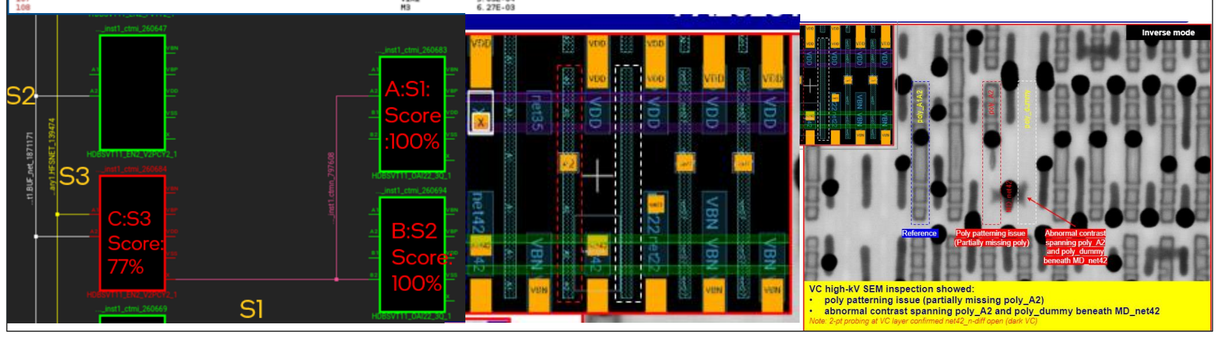
- Library creation methodology is being disseminated to the relevant Intel teams
- Ready to deploy for HVM of new designs with advanced nodes (N6 and N3B)
- Can analyze logic failures within standard cells

Deployed on 2 designs (N6) – Two successful PFA are shown below

DG2-256

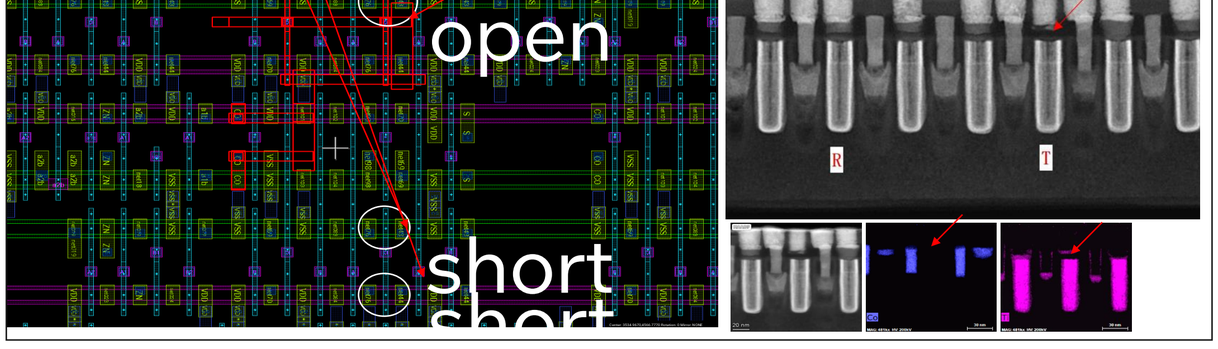
Augment::ed Flow showed cell fault

Match with PFA result



MTL-SOCMC0

Diagnosis report: /nfs/pdx/disks/emp05/lohlayho/MTL/SOCMC0/mtlsocm_thunderball/BBOutput_IC342Y8303__132110.W116/SOCN/MTSC0_IC3



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Saghir A Shaikh saghir.shaikh@intel.com

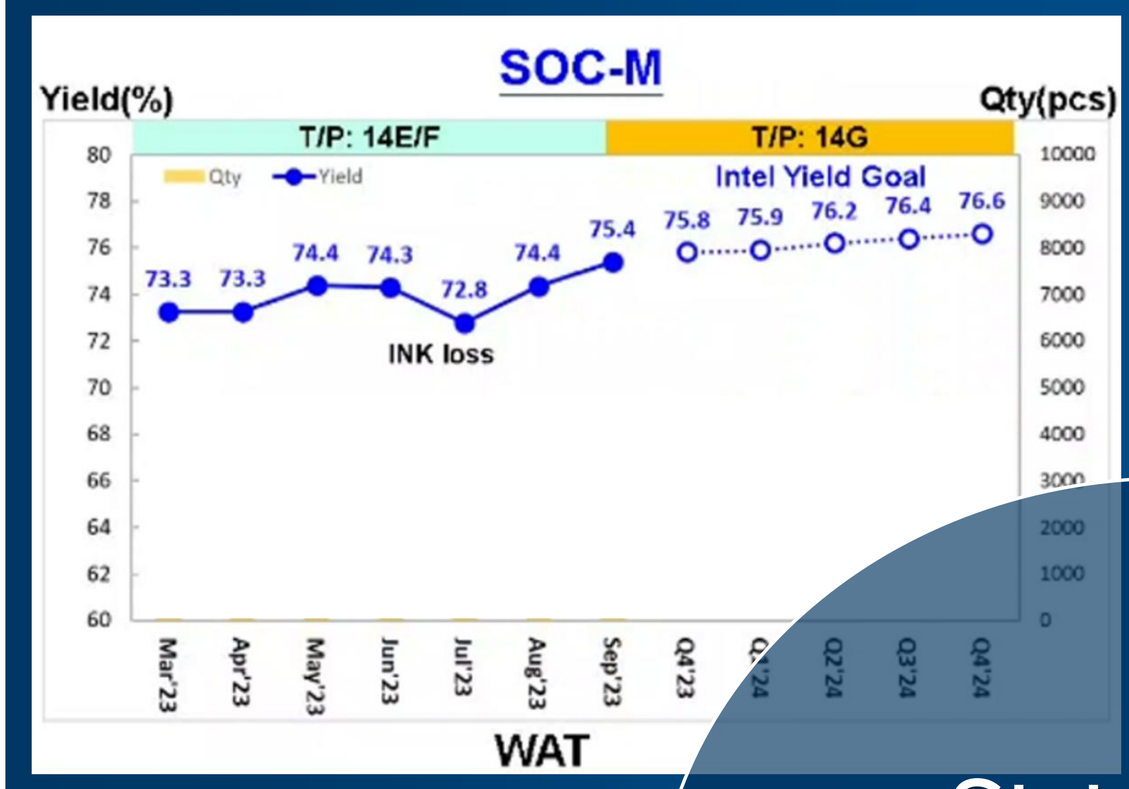
Lay Hoon | Giyoung Yang | Parkash Palanisamy | Jim Lee

Advanced Yield Management

Developed a High Efficiency Yield Management System

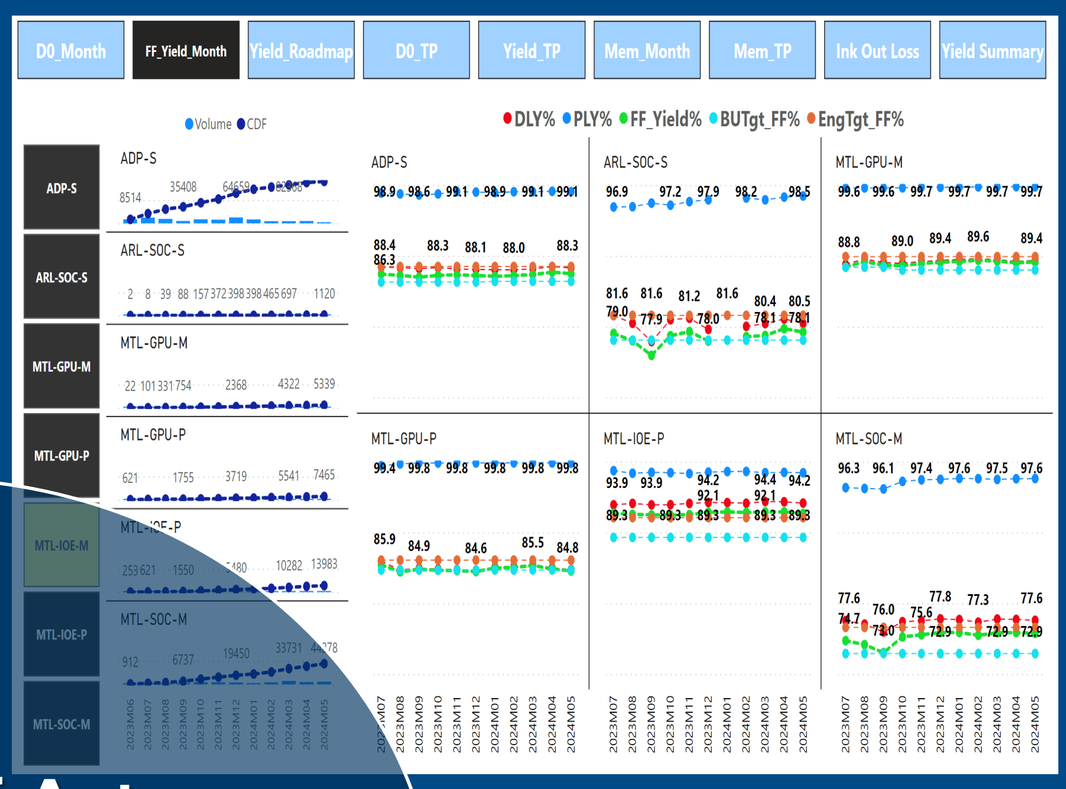
Yield Roadmap

Define Roadmap with Foundry

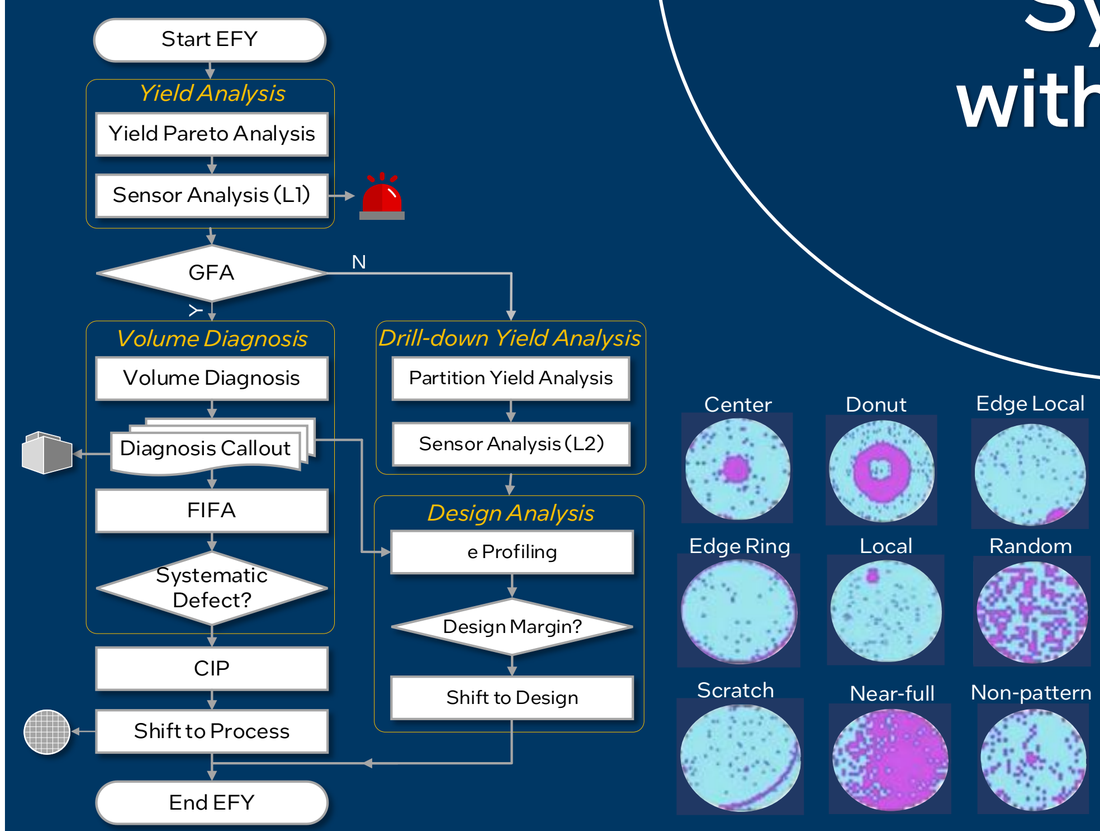


Yield Management

Leverage YE/S.DA and PBI DB

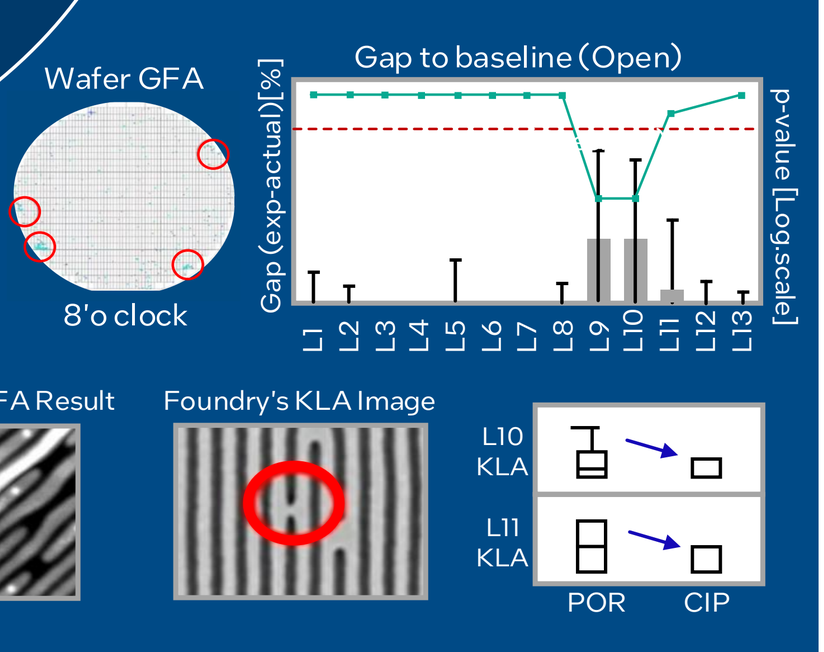


State of Art Yield Management System within EMP



Systems and Tools

Yield Partition, Sensitive Layout Pattern (SLP) , AI WPR, FIFA app



Diagnostics

State of art Layout/Cell Aware, AVD/FMA trending, Call out + SLP

Integrated an efficient HVM yield management system in EMP with start of art tools and metrologies. Contribute to savings in $$ Millions Annually

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Eric Guan | eric.guan@intel.com

Scan Yield Loss debug

MTL SoC South Scan Yield Loss of +1% ⇔ +2% is debugged by utilizing Yield to design marginality timing closure feedback loop. Preventing future products Yield Loss (save $$) via co-developed TFM improvement

Sort Yield Segregation

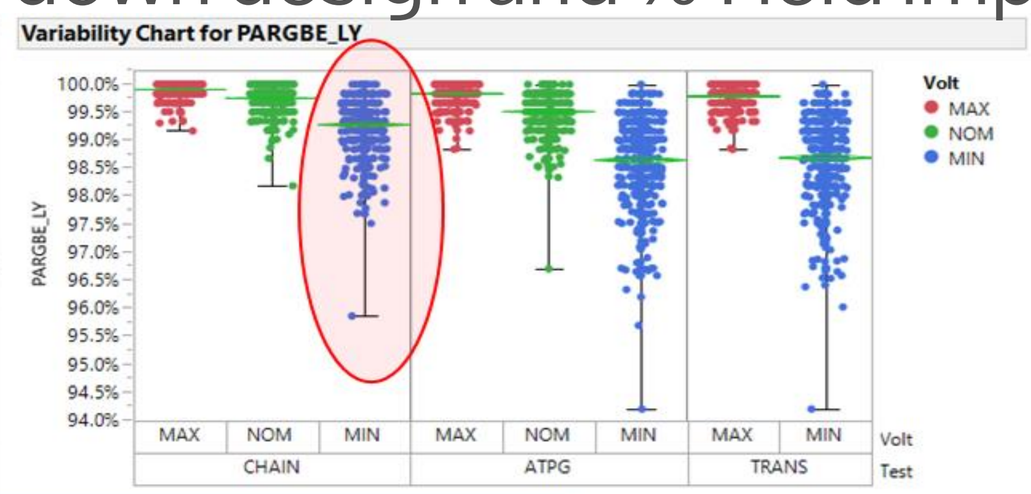
Scan Yield ↑

Design Profiling

Scan Yield loss Diagnostics

Design signoff : IR drop aware STA

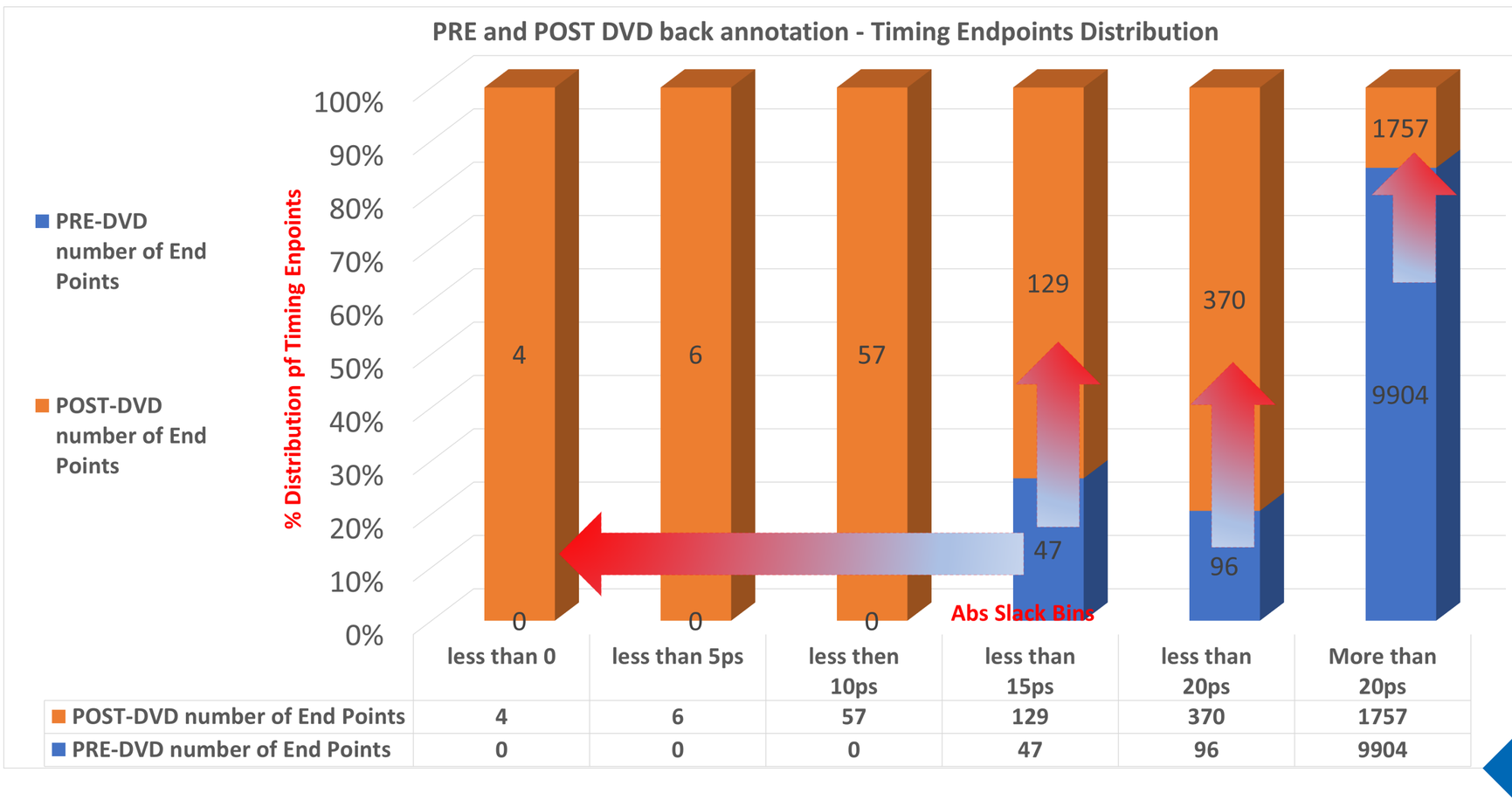
Scan Mode Yield segregation to narrow down design and %Yield impact



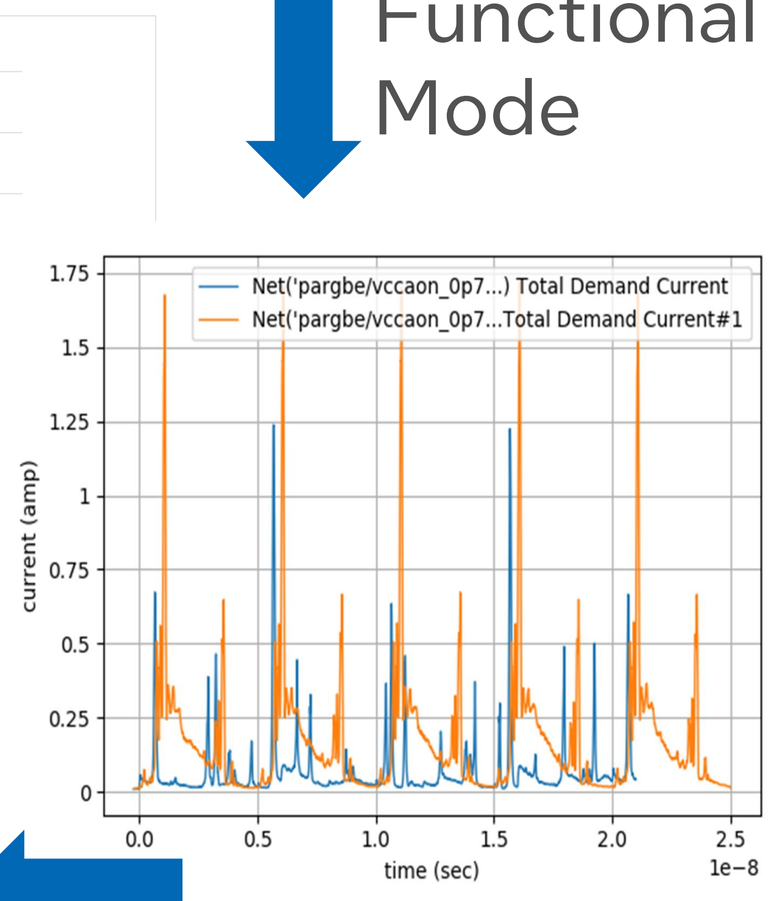
C0 Corner Lot C302Y020, Program Rev 14C

SORT_WAFER		501	502	503	505	507	509	511
Device_Skew		TT	TT	FF	FF	FS	SF	SS
SubPartition		PARGBE						
CHAIN	MAX	100.00%	100.00%	100.00%	100.00%	99.84%	100.00%	100.00%
	NOM	100.00%	99.84%	100.00%	100.00%	99.68%	99.51%	89.35%
	MIN	99.27%	98.99%	100.00%	100.00%	97.91%	98.19%	84.69%

Scan Mode IR drop >> Functional Mode



	less than 0	less than 5ps	less then 10ps	less than 15ps	less than 20ps	More than 20ps
POST-DVD number of End Points	4	6	57	129	370	1757
PRE-DVD number of End Points	0	0	0	47	96	9904



IR drop Induced VDD droop increases hold timing slack and fails

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Sidharth Rastogi | sidharth.rastogi@intel.com

Generative AI: Revolutionizing Intel

How Generative AI Fuels Productivity, Sparks Innovation, and Enhances Decision-Making Through Tangible Success Stories

Development
25% time-saving for software developers

Documentation
20% increase in productivity

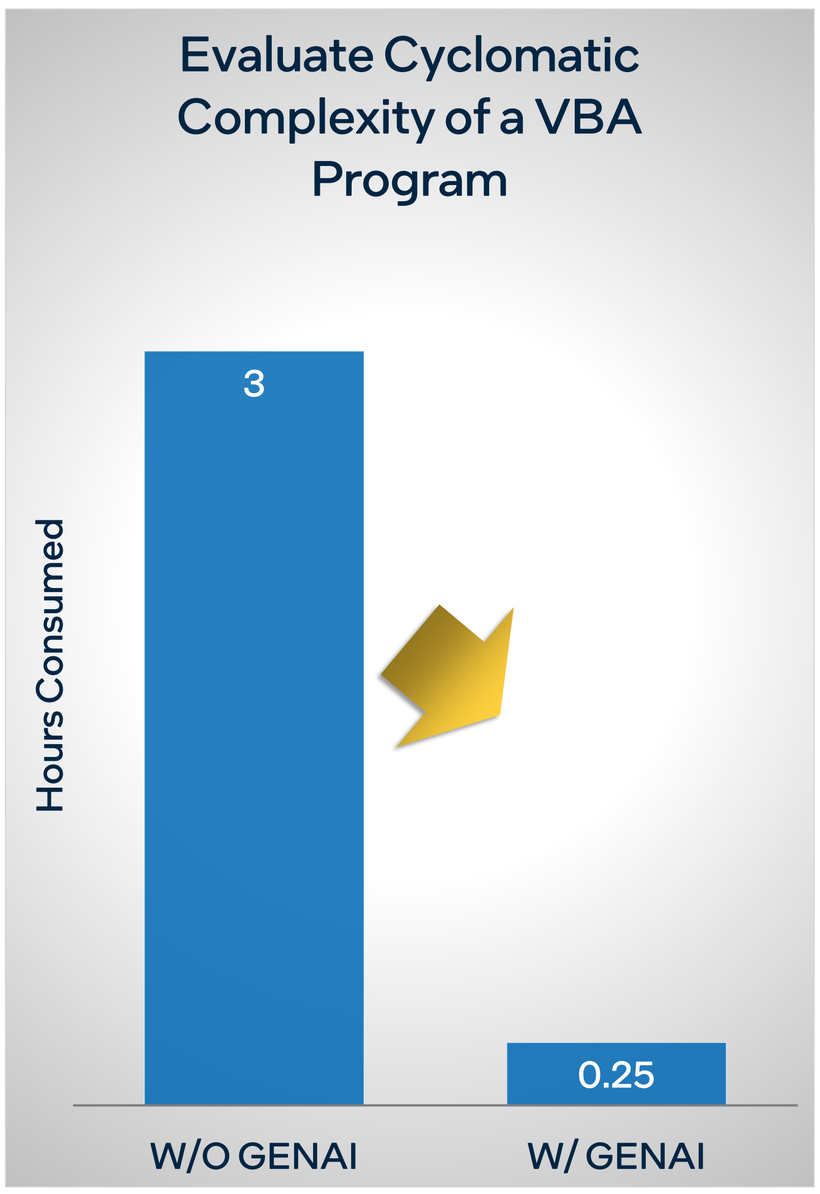
Accelerating Excellence

Innovation
15% enhancement on creative output

Communication
10% reduction in miscommunication

Improvements on different use cases

0~5%	5~10%	10~20%	>20%
Data Analytics	OKR	Creative Thinking	Coding/Debugging
Calculation	Email Coach	Job Description	Proof of Concepts
Reasoning	Data Visualization	Translation	Content Creation
Prediction	Experiments Design	Meeting Minutes	Automated Documentation



Balancing Advantages and Considerations

Advantages

- Increased Productivity
- Enhanced Creativity
- Streamlined Processes
- Improved Communication

Considerations

- Data Security
- Accuracy Risks
- Ethical Use
- Responsible Implementation

The Future of Gen AI in GEMS

- AGS based GEMS RAG Chatbot – Pilot 4Q24
- Exploring more use cases to increase productivity and efficiency
- Inspiring Gen AI insights in weekly open forum

Contact Author

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Tian He | tian.he@intel.com

14nm PCH
Total Management of Supplier Excursion

Si reliability detected, root-cause identified, customer recall prevented, materials screened, scrapped and replaced at $0 to Intel

Data Driven
AI detection, DOEs,
Screening Development
Scrap Decision

$18M Value in 2024

One Intel Team
GEMS Engineering
Q&R, Production
Foundry Account Team
Logistics & Planning

Supplier Partnersh
Fab root-cause
Containment & Prevention
Compensation
Build ahead

Execution
Tests, Shipment Mgmt
Materials Disposition
Replacement & Credit

Supplier Fab Excursion

Total Impacted
13,644 wafers (~8Mu)

~7 Weeks of Wafer Supply
(Shortage Avoided by Build Ahead)

Shipped to Intel
12,279 wafers (7Mu)

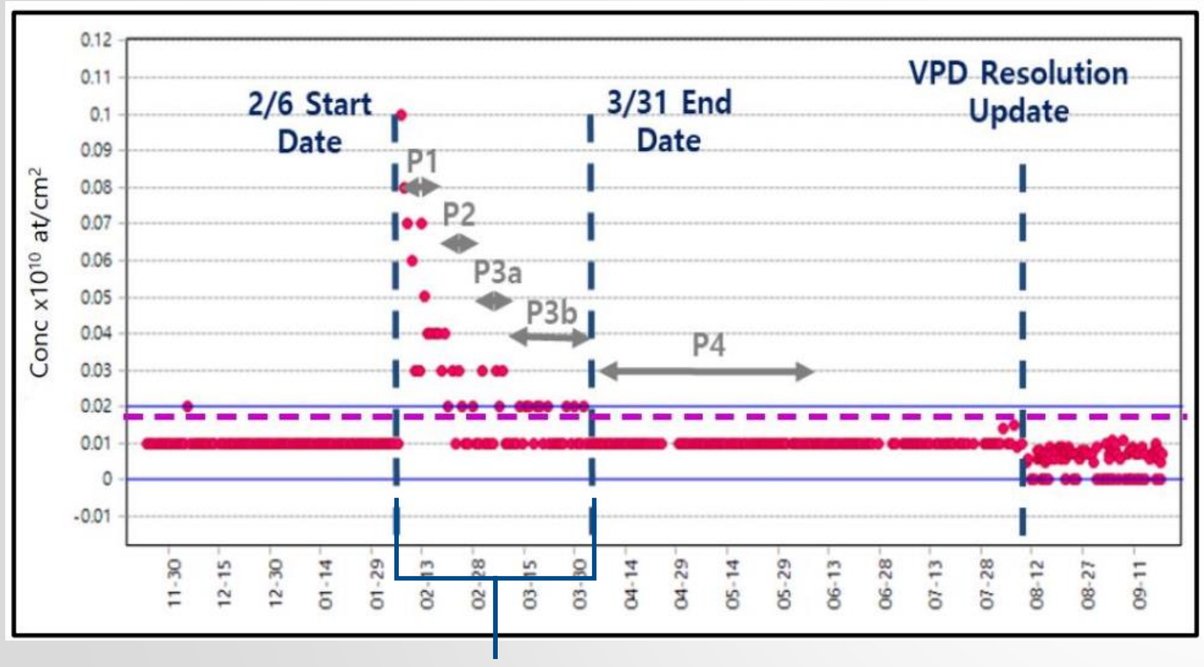
Scrapped at Supplier
1,365 wafers (~1Mu)

Released
7127 wafers
(4Mu)

Scrapped at Intel
5152 wafers
(3Mu)

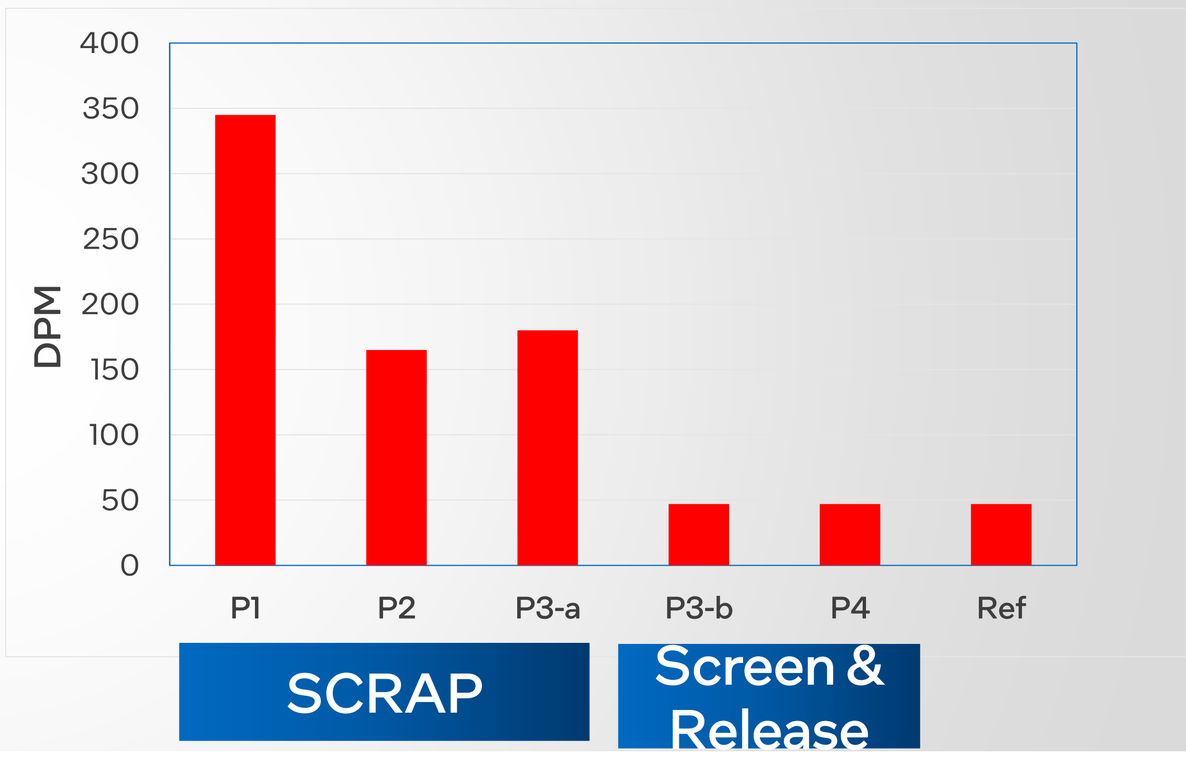
~ $670M Potential Recall Avoided
(Intel Reputation Protected)
$18M Si Compensated

Metal Excursion, Supplier Tool



Trace Metal Excursion

Risk Groups & Decision



Team Acknowledgement: EMP, QnR, EMS

Yonah Cho | yonah.cho@intel.com

Time to Yield Acceleration

On-Site Wafer Sort Enabling 2Q Pulled-in & 5% Fmax Push

Wafer Sort @ TSMC

- >$10M wafers + CPU grade testers ($15 million) free of cost
- Physical Failure Analysis done by TSMC

Industry Standard V93K Test

- Access to best foundry talent
- Leverage Advantest Eco-System

2-3x TAT Improvement

>$10M Free Wafers

~2Q Yield Pull-in

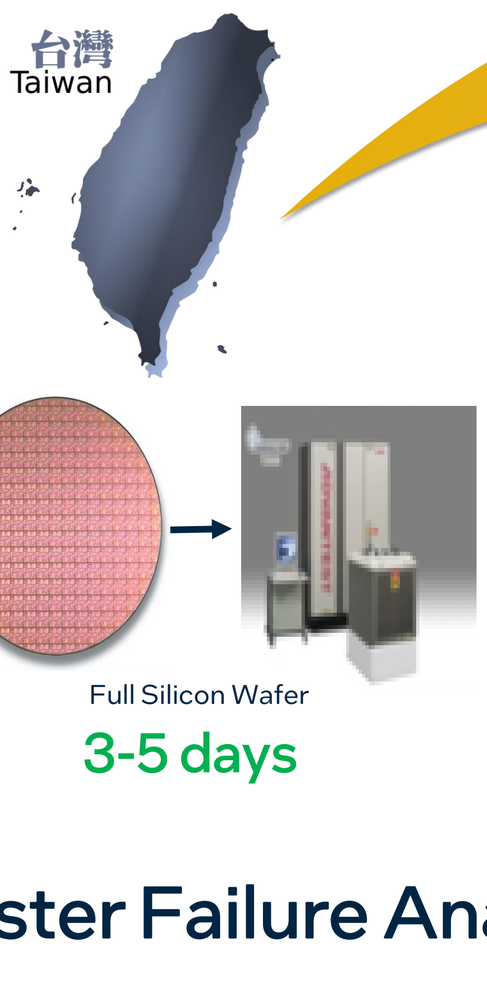
Fast CIP & Yield Feedback

- Shorten yield learning cycle
- 5% Improved FMAX
- Quick TAT for ARL HPC drive

ARL NPI Impact

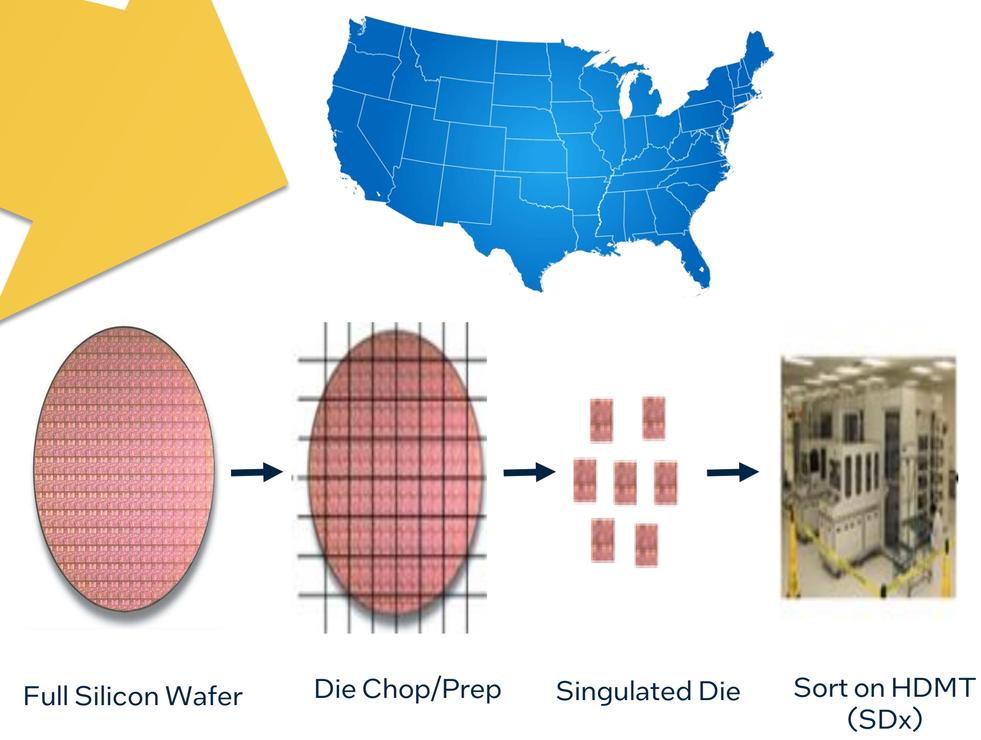
- Earlier Sort PO (3 days)
- Atom bug identified; lead to quick A1
- CIP data 1 week before SDS

2-3X Turnaround Time Reduction



3-5 days

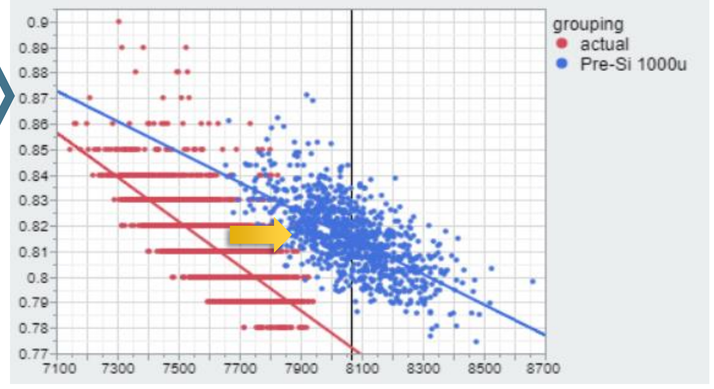
vs.



7-14 days

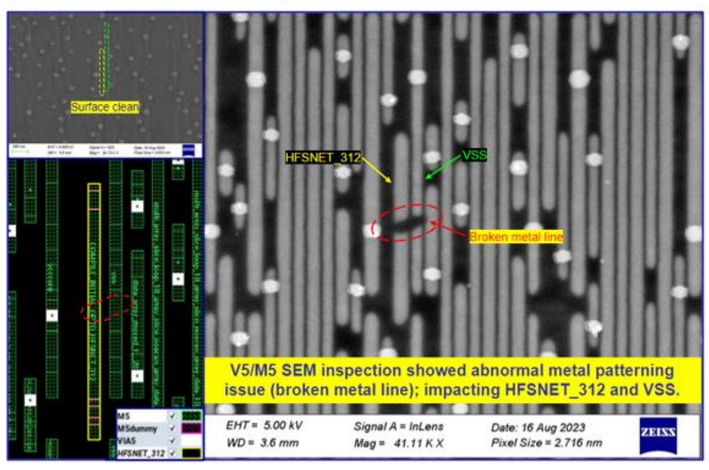
Faster Failure Analysis (FA) , Yield Debug and Performance Improvement

Driving Devices to Target

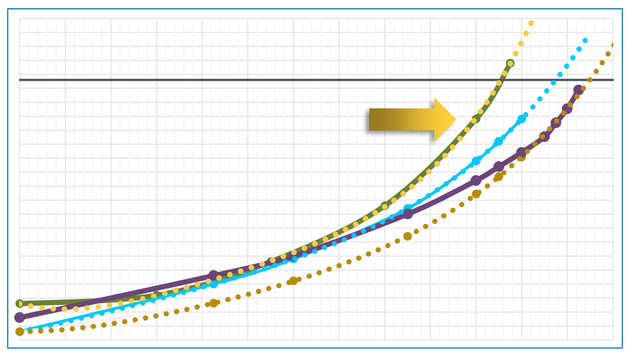


Improving Product Yield

Scan/X-9Y-6 : M5 pattern fail



Pushing Product Fmax



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N3B Yield Improvement

N3B ARL S816 A2 DTCO to improve yield by >10%
Timely resolution enabled healthy ARL B0 production Silicon

Problem

- A2 Si showed ~ 23% yield loss from Bin4+Bin19
- 10% loss higher than projection

FIFA

- FIFA challenging for Bin4/Bin19
- Leverage Scan and DC for fast FA TPT

A2 Yield increased by

>10%

hitting 678 RISO

~2Q Yield Pull-in

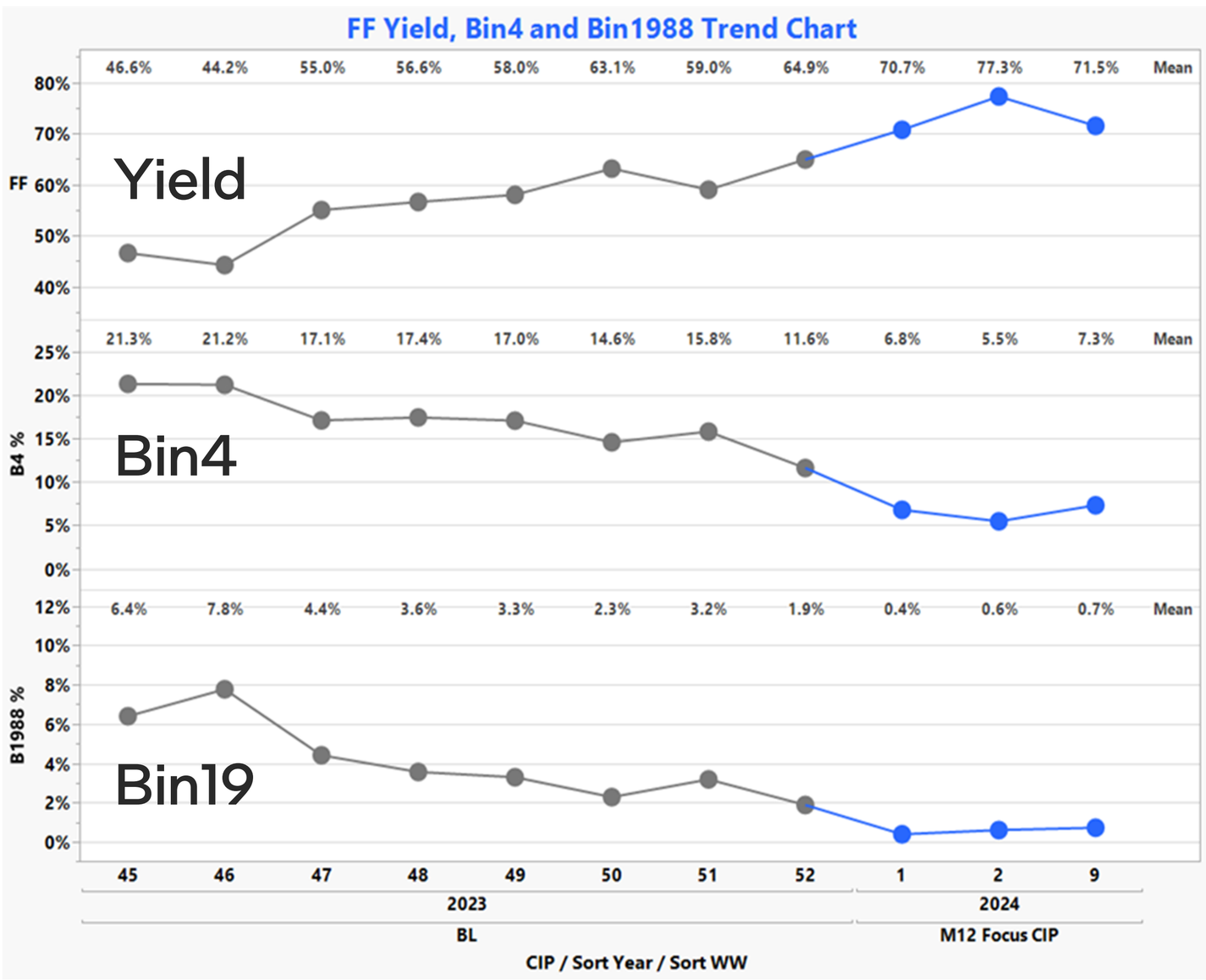
Root Cause

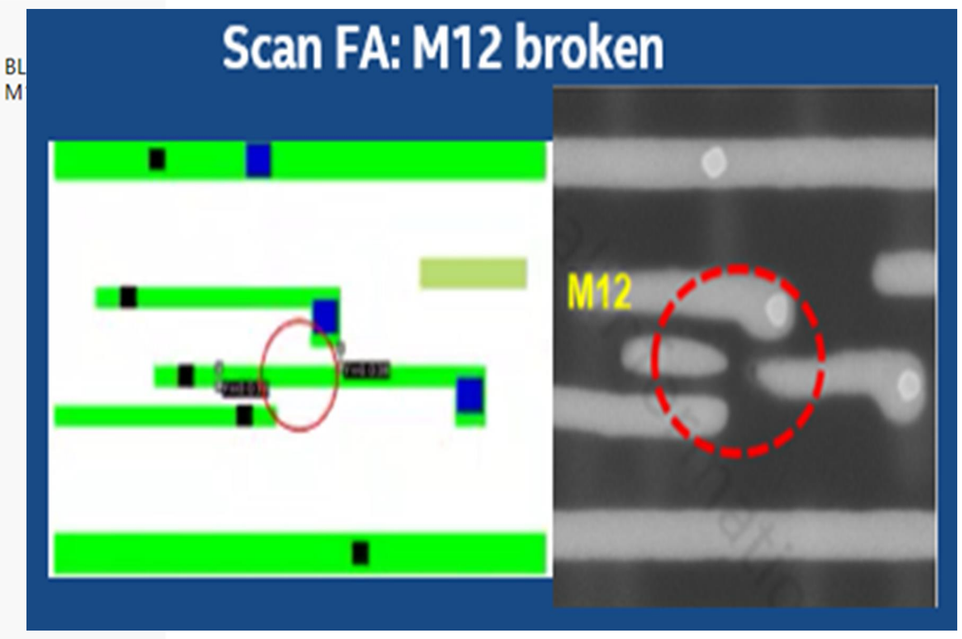
M12 broken due to interaction of

- M11 low density
- M12 unique layout
- Litho process

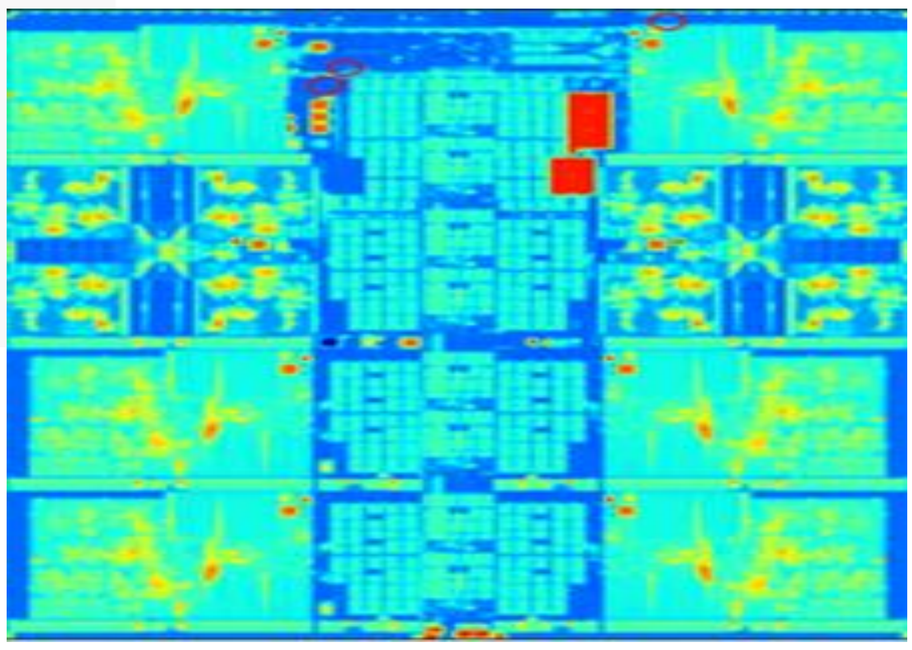
DTCO

- ARL unique M12 Litho focus optimization
- Tailor process for design





M11 Density Map



- Baseline
- M12 focus CIP

Global External Manufacturing and Sourcing Poster Pop-Up 2024
James Guan | james.guan@intel.com

Meteor Lake- flawless 5 Tiles execution to PRQ

Total $176M cost savings /$158M cost avoidance GEMS contributed to production since 2023

Disaggregated architecture

N6 SOC/IOE , N5 GPU and intel 4 CPU assembled together by Foveros.

Process improvement

Total >70 CIPs to improve PnP, beating yield target.

Enabled:

N6 SOC, IOE & N5 GPU and beat yield & DPM target

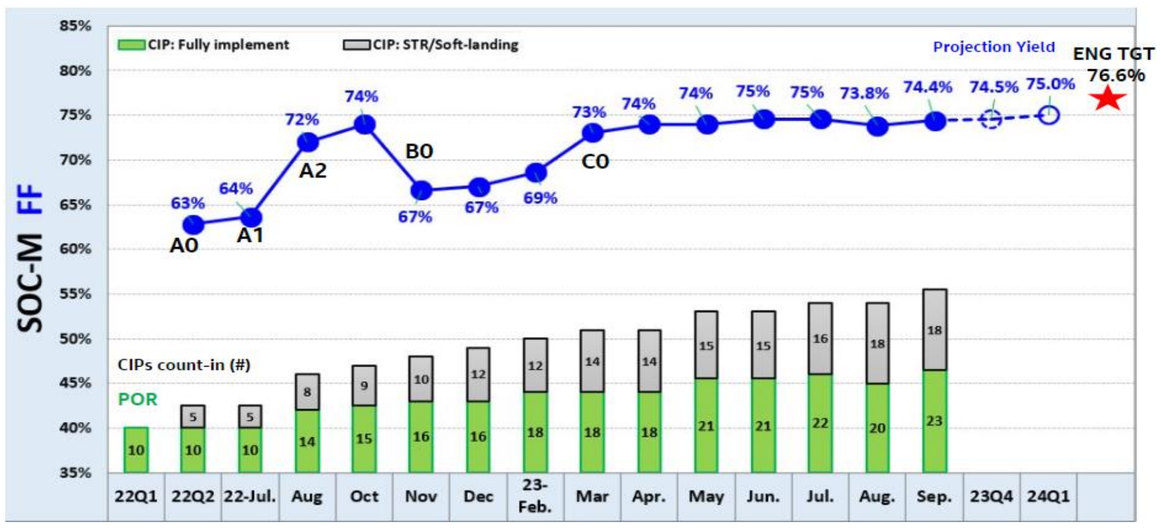
FA/Yield Learning

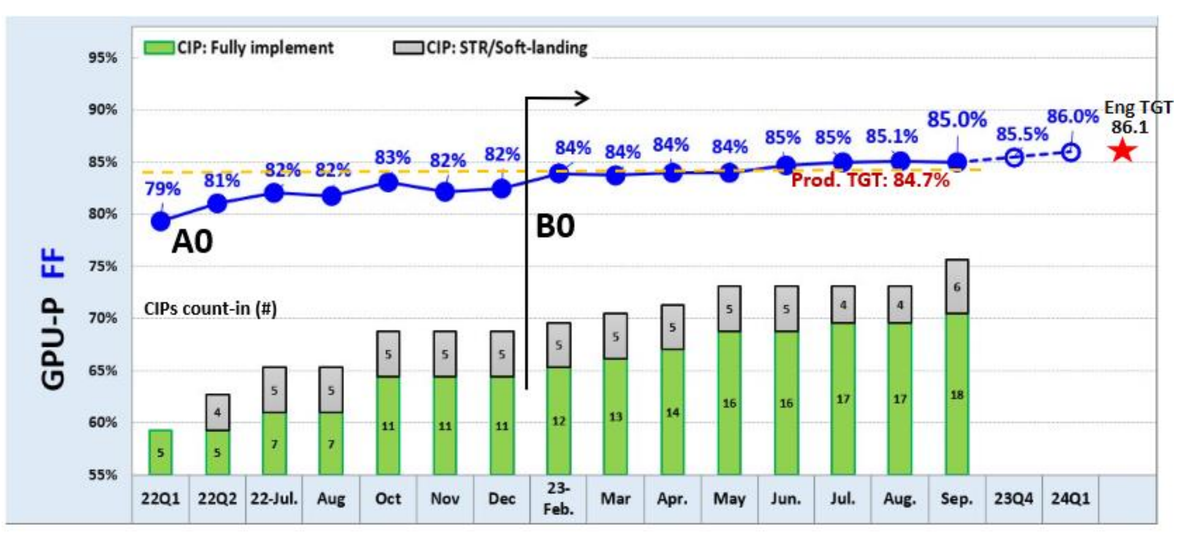
FA for systematic defect reduction and led to effective process CIP.

DPM < 400

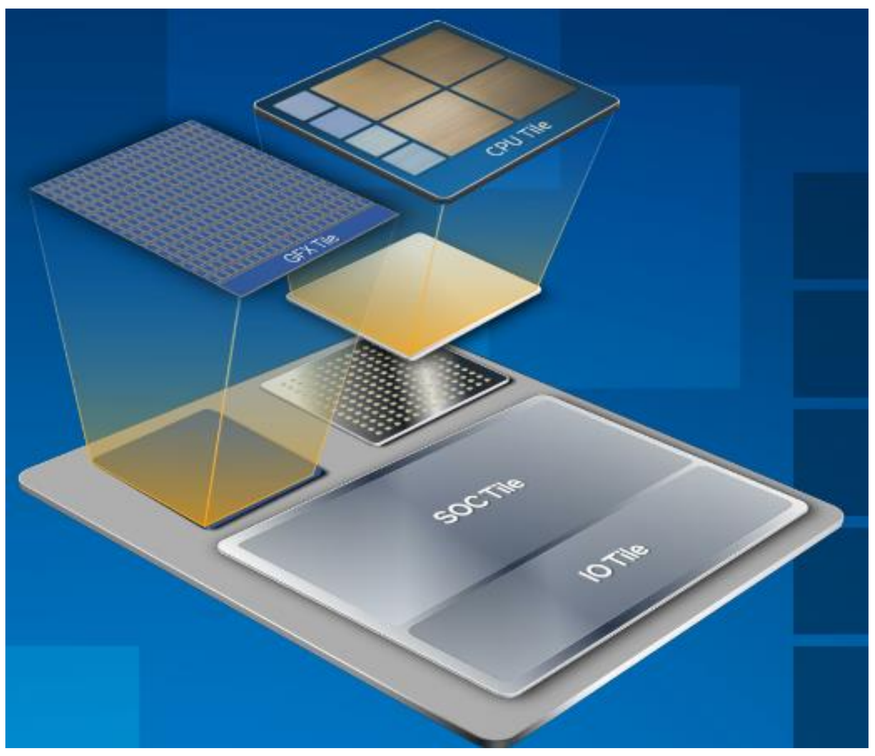
20 proactive CIPs to reduce BEOL voids enabling bake removal.

N6/N5 yield trend with CIP implemented

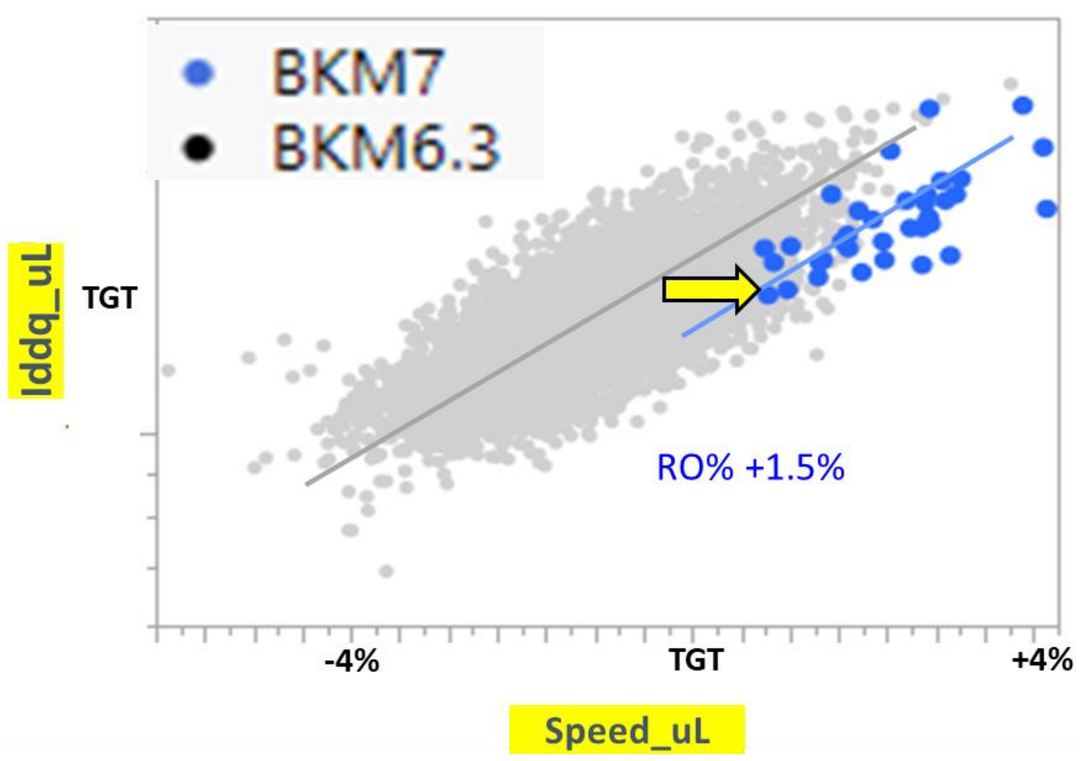




Meteor lake CPU architecture



TSMC N5 GPU speed boost



Global External Manufacturing and Sourcing Poster Pop-Up 2024

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Initiating, Driving, & Executing ½ Node Performance on TSMC N3B through Post Si Tuning with Iso-Design

Aggressive Targets

Set up clear perf targets beating PDK1.0

Development Partner

Work with TSMC for
> 10 device CIPs
executing in < 3 qtr

102% Speed at 0.8X Pre-Si Pwr Tgt

Acceleration

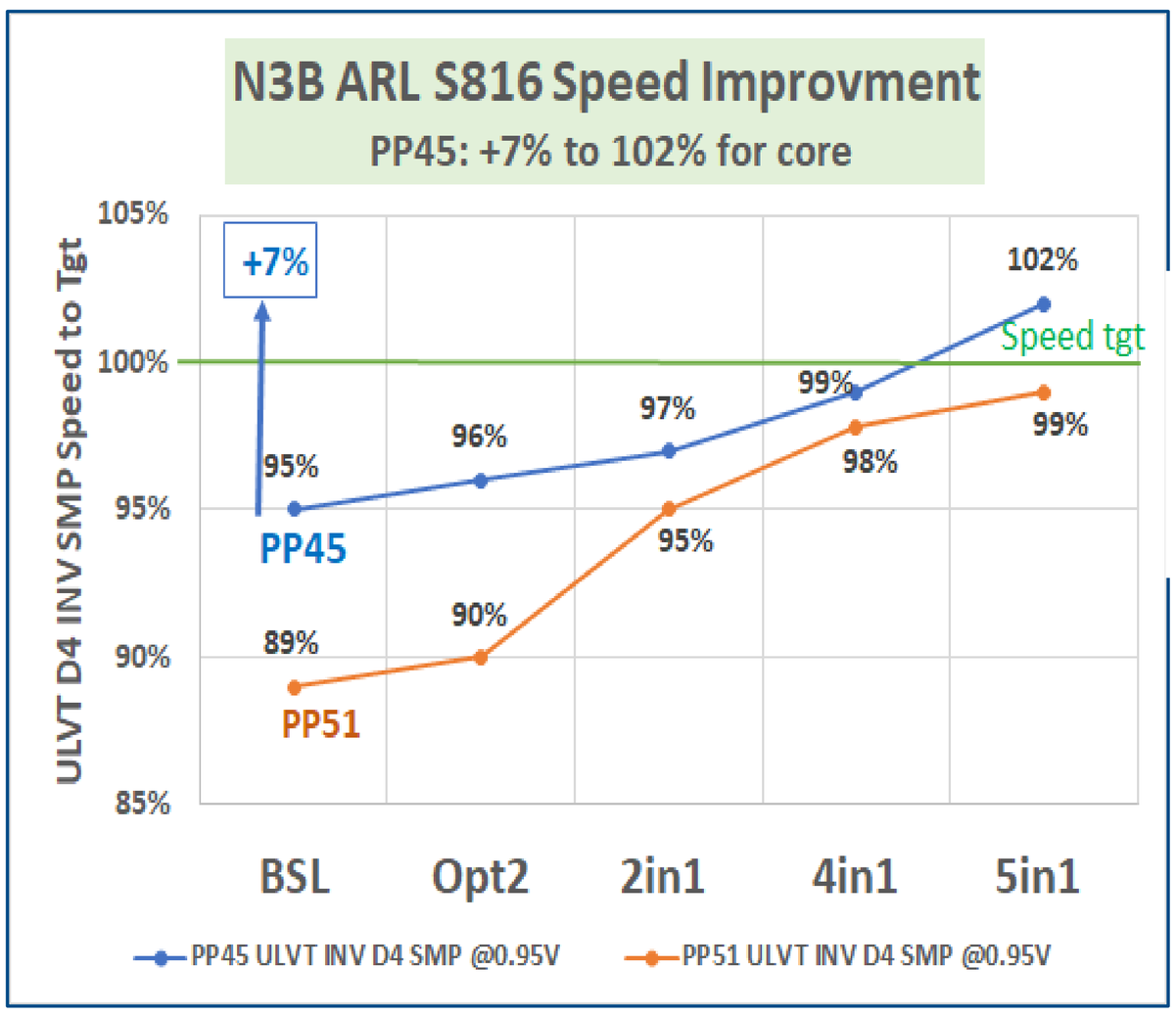
Drive left shift w/
V93K & MPE for
Perf data collection with 2X TPT

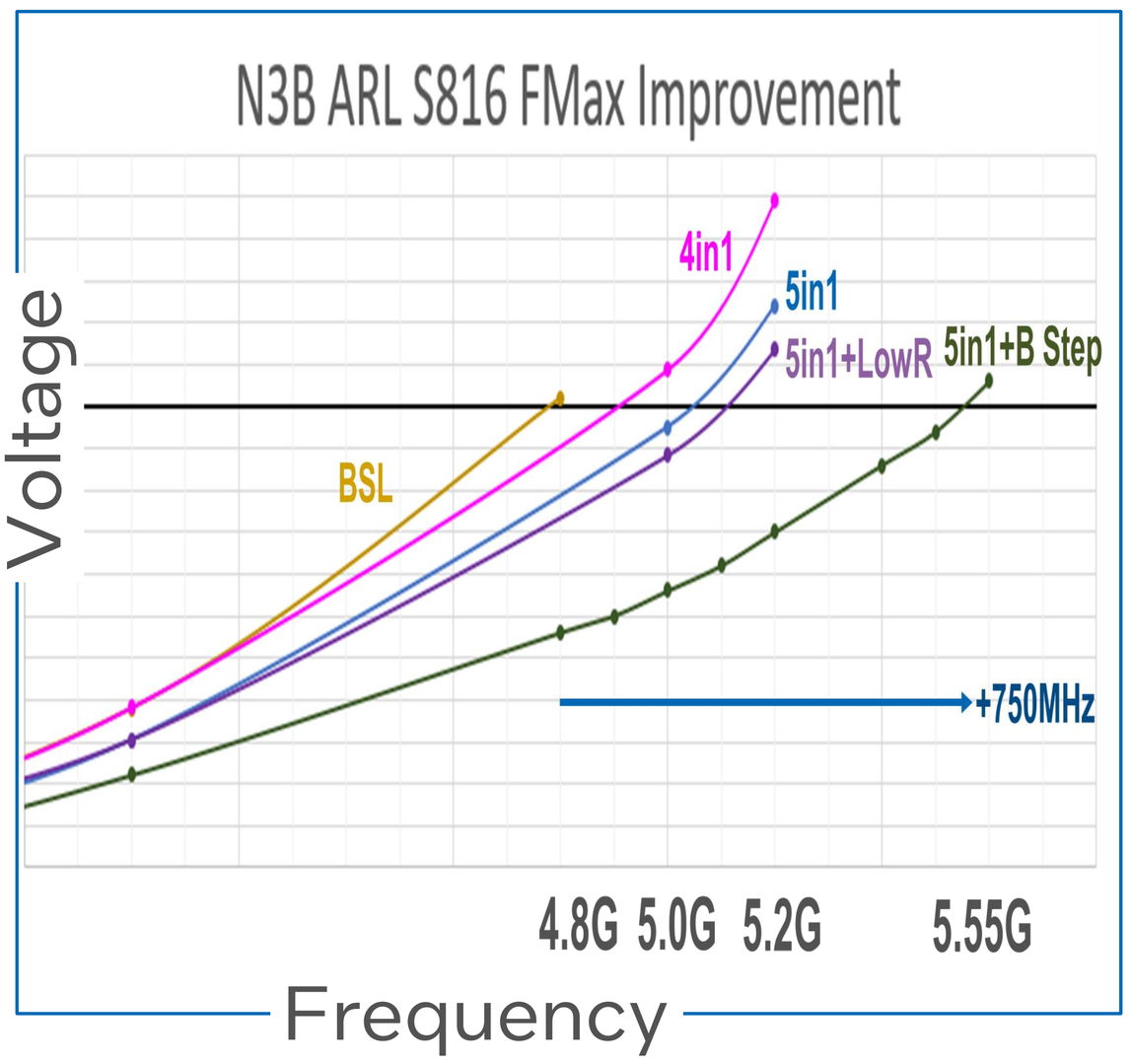
Joint Ratification

Finalize Proc POR
w/ CCG, MPE, DEG

Risk /Decision Matrix

CIP Gorup	TSMC RO % ULVT P45/51	TSMC RO Poff ULVT P45/51	Core (5G) Vmin MLC 1.09V	Total SICC vs tgt	ARR Ring Vmin (0.8G) LLCDATA	Cdyn LNC /SKT 0.95V (% tgt)	Yield (FF+DF) (CIP/ BSL)	TSMC Rel risk	Go/no go to B0
Starting BSL (A0/A1)	89% / 84%	1.0X / 0.7X	1.09	0.5X	0.62	102%/ 82%	82%		
Opt1+ Opt2 (A2 BSL)	91% / 87%	1.1X / 0.8X	1.07	0.5x	0.60	110%/83%	74.8% (81F) 76.4% (81G)		
2-in1	91% / 91%	1.0X / 1.2X	1.06	0.8X	0.58	TP issue/84%	74%/82%		
4-in-1	94% / 94%	1.2X / 1.4X	1.01	0.8X	0.59	111%/84%	71%/81%		
5-in-1	98% / 96%	1.5X / 1.3X	<1	0.8X	0.60	111%/84%	85%/78%		GO WW4723





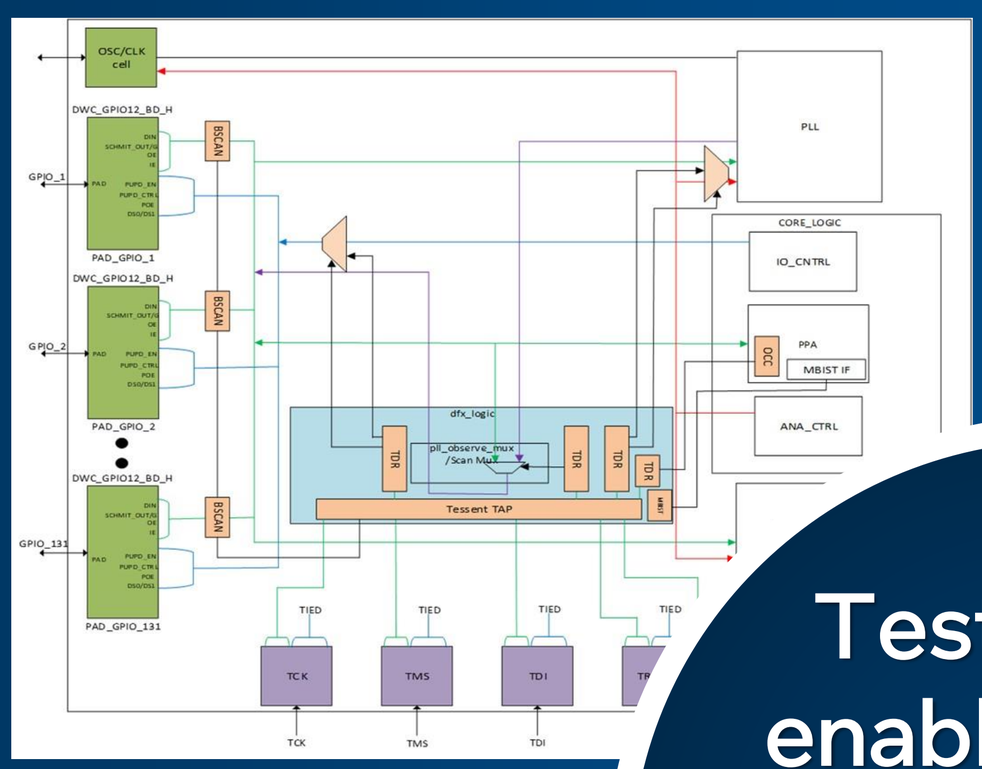
Global External Manufacturing and Sourcing Poster Pop-Up 2024
Li Ling | li.ling@intel.com

FTE FTiP: External Technology Pathfinding

Bringing Technology to Intel Products

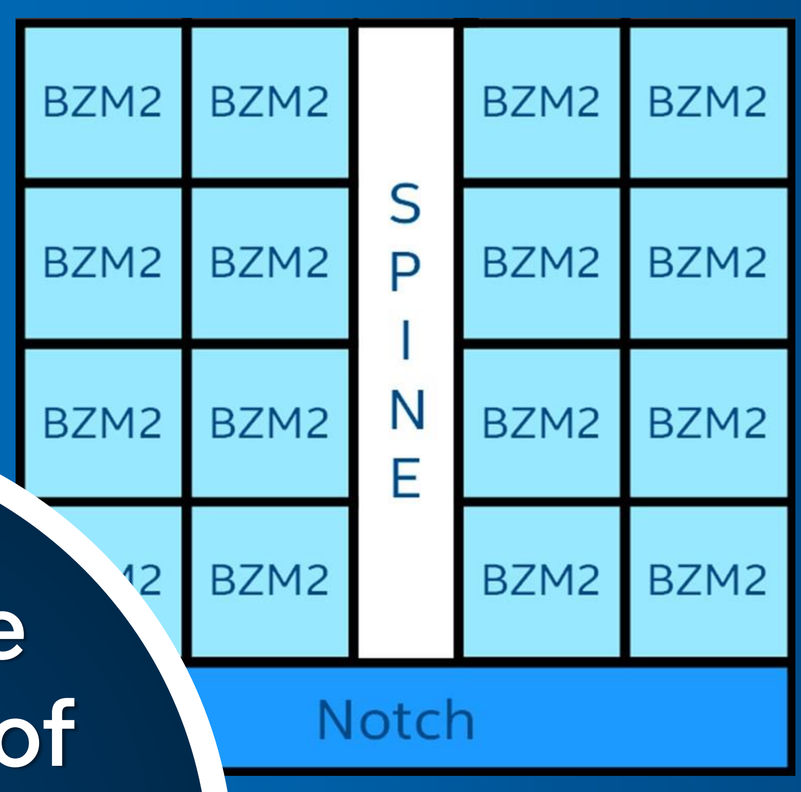
First Creek

PPA / yield verification.

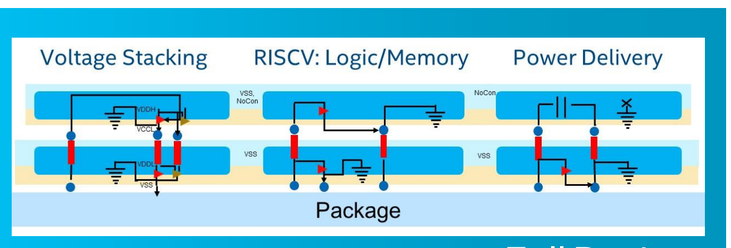


Second Creek

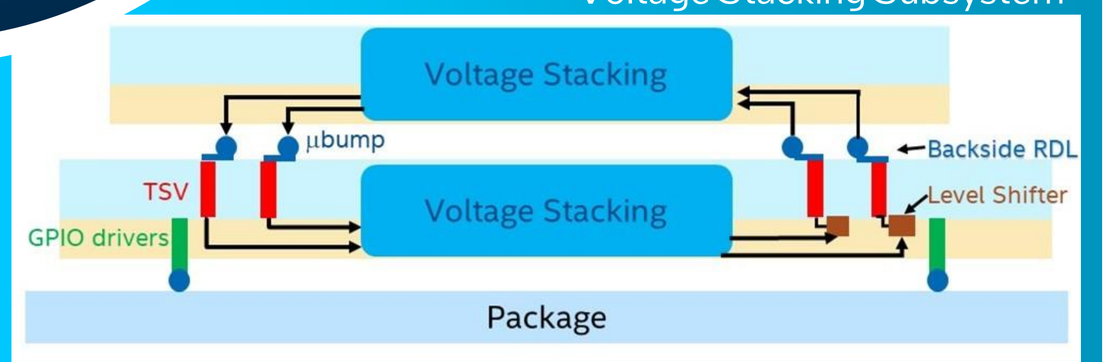
Low Vdd performance / yield validation.

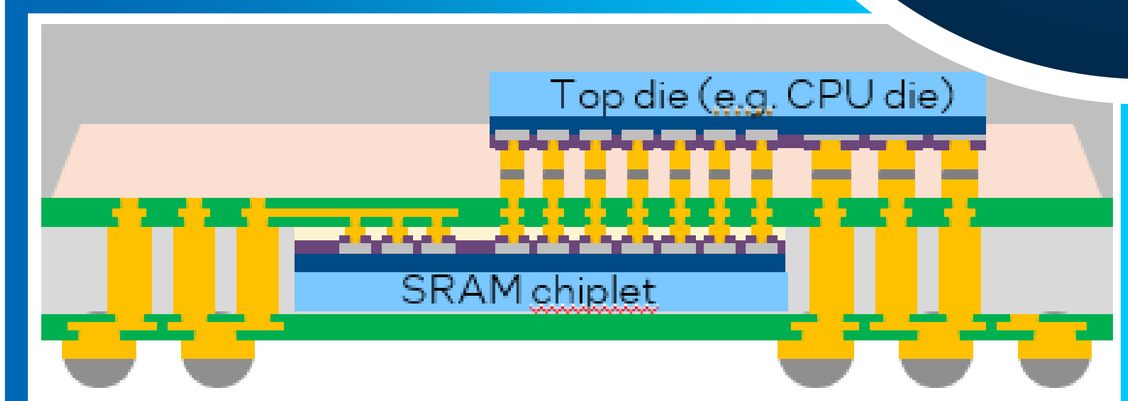


Test vehicle enablement of external ecosystem Si and packaging technology.



Full Design





Muddy Creek

Low-cost memory disaggregation through new packaging options.

Tower Creek

µbump 3DIC: voltage stacking, logic / memory disaggregation, and power delivery noise reduction.

Enabling external Si and packaging technology through Proof-of-Concept test vehicle design / test / optimization in support of Intel's roadmap.

Global External Manufacturing and Sourcing Poster Pop-Up 2024

Per Sverdrup | per.g.sverdrup@intel.com

3D vertical integration of modular memory chiplets

Achieving low-cost 3D vertical integration of SRAM memory chiplets

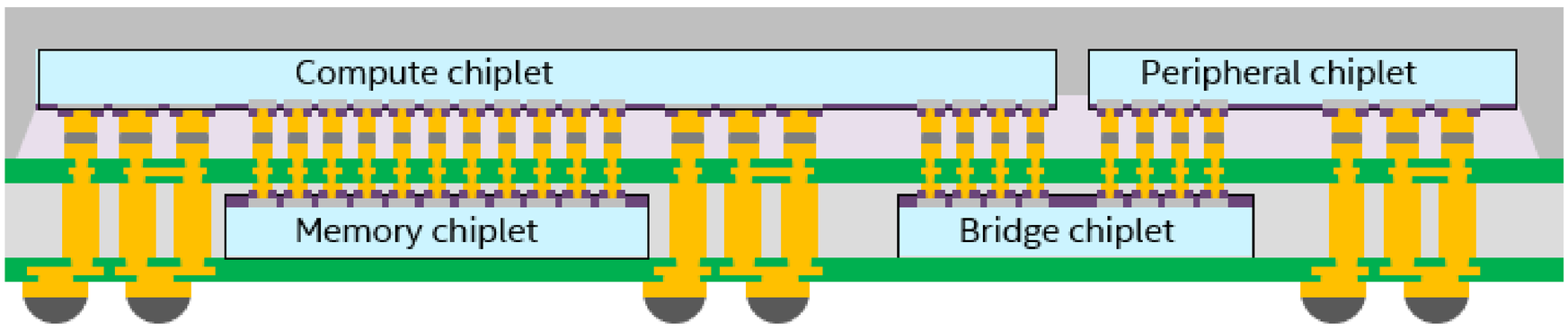
Modular
Reusable, Scalable

3D integration of Memory Chiplets

High Bandwidth
102 GB/s die-to-die
x512 lanes (64B)

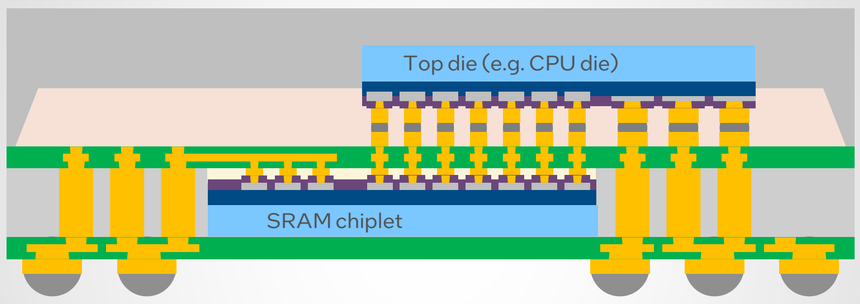
Low Energy
<0.3pJ/bit at 1.6GT/s

Low Latency
<5ns Read/Write latency



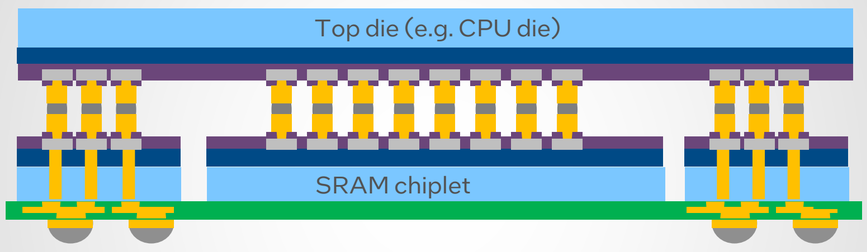
Leverage supply chain to enable new capabilities

Muddy Creek Test Vehicle



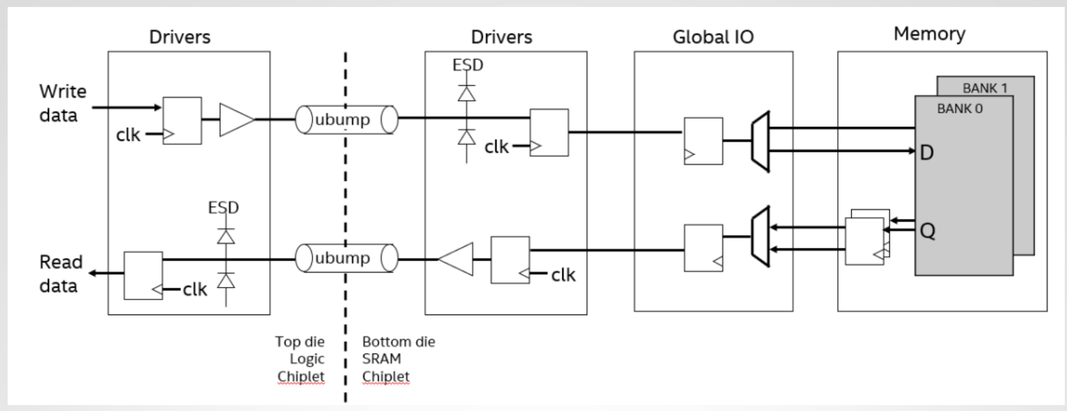
SRAM chiplet integration
as embedded bridge
w/ 25um ubump pitch

Cool Creek Test Vehicle

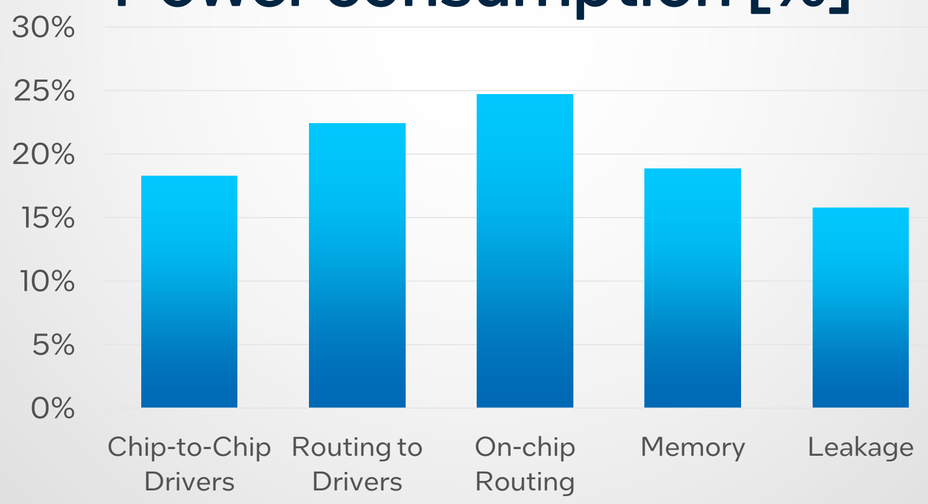


SRAM chiplet integration
as direct attach CoW
w/ 15um ubump pitch

Die-to-die Channel



Power consumption [%]



Enable low-power, low-latency and high bandwidth interface between dies

Global External Manufacturing and Sourcing Poster Pop-Up 2024
Dany-Sebastien Ly-Gagnon | dany-sebastien.ly-gagnon@intel.com

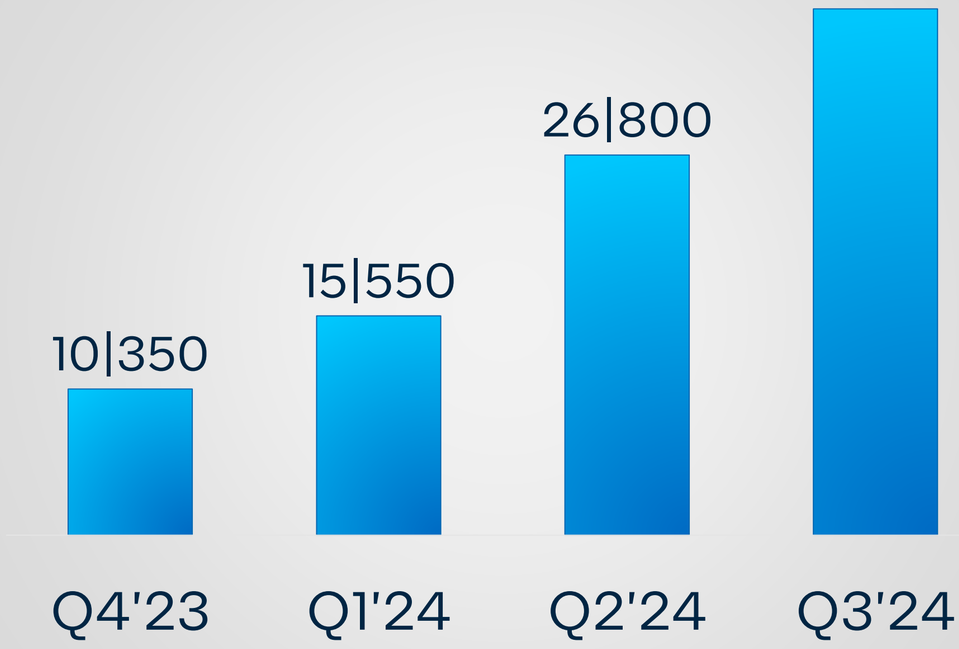
Ext Mfg Order Report

Aligning historic Actuals/SL/CP stitch to data from SDA horizon. Result of collaboration between FOP SC, DCP, FOPO, DSPA, FOP OE & IT.

AS-IS Gaps

OWNERS	Person owned reports
PROCESS	Manual, Time, Unsound Logic
SYSTEM	Partial data, Non-traceable

Active User | Total View



* with projected New Users

Productivity
> 15hr/wk savings

Standardization
Single Align Source

450hrs
savings to-date

Data Integrity
Enterprise tools

Scalability
Data lake
Decision Science analytics

Work Week | Fiscal Month | Fiscal Quarter | 2022 | 2023 | 2024 | Snapshot Date: 4/6/2024

PlnOrgCd	Stage	Solve Group	Item Group	Sub Capacity Grp	Die Name	Design Name		202204	202205	202206	202207	202208	202209	202210
CCD	ASSEMBLY	Burnside Bridge	ASSEMBLY-BBR8040-FC-CSP2F-105		BURNSIDE BRIDGE	BBR8040	SL				0	2,323,422	1,713,653	4,086,381
							CP				0	2,323,422	1,713,653	4,086,381
							Act				298,415	2,083,465	2,658,773	4,499,505
	BUMP	Burnside Bridge	BUMP-BBR8040-N/A-		BURNSIDE BRIDGE	BBR8040	SL	2,068	2,132	2,357	1,197	2,015	1,194	1,817
							CP	2,018	2,182	2,030	1,524	1,816	1,393	1,616
							Act	2,283	1,947	2,156	1,594	1,586	1,391	2,069
	FAB	Burnside Bridge	FAB-C28	HPC/Non-UTM	BURNSIDE BRIDGE	BBR8040	SL	0	0	0	0	0	0	0
							CP	2,222	1,468	1,551	1,925	1,525	782	3,277
							Act	2,339	1,348	1,457	2,121	1,370	720	3,336
	FINISHED GOOD	Burnside Bridge	TEST-BBR8010-FC-CSP2F-105		BURNSIDE BRIDGE	BBR8010	SL				69,000	228,000	984,000	633,000
							CP				0	297,000	1,107,000	633,000
							Act				0	459,000	822,000	633,000
			TEST-BBR8040-FC-CSP2F-105		BURNSIDE BRIDGE	BBR8040	SL				513,000	2,354,000	5,257,567	2,187,998
							CP				83,520	2,195,480	5,879,670	2,187,998
							Act				83,520	3,041,254	5,170,793	3,645,480

Snapshot Date	PlnOrgCd	Stage	Solve Group	Item Group	Sub Capacity Group
4/6/2024	All	All	Burnside Bridge	All	All

Die Name	Design Name	Item ID	Lasor Code	Supplier	Fiscal Month	Tech Node
All	All	All	All	All	All	All

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Global External Manufacturing and Sourcing Poster Pop-Up 2024

Terry Eng Keong Koh | terry.eng.keong.koh@intel.com

Product PHD (Predictive & Holistic Digital Strategy)

Authors: Marta Teixeira, Beilei Zhu , Virginia Pulmano

Strategic Analytics Unleashed:
Revolutionizing GEMS Strategic Planning and Spending

0-5 yrs. Evergreen Forecast

- Pioneer **Unification of 3 Planning horizons** (SDA/MRP/LRP) **Reporting** for Comprehensive Product and Supplier Analytics
- External Manufacturing **One Stop Shop** for Biz Units, Supplier Management and Planning Teams
- **Near real-time reporting capabilities** for about **1/7 of Intel's LRP COS**

>4K hours Saved per Year

- Report output time **from 4-5 weeks to less than 1 week**
- Publication of datasets time reduction **from 24 to 1.5 hours**
- **Increased focus** on **Value-add, Strategic** work

Azure Cloud Centralized Analytics

- **Safeguarded** Azure Cloud Infrastructure
- **On Demand** end –to –end Analytics
- **Dynamic** Data Source with Versioning and "**What If**" Scenarios
- Strengthened **Self-Service BI** Process
- Embarking on an **AI** Odyssey to Uncover **Strategic Insights**!

0% Data Manipulation

- **Data load automation** of >3.5k data entries and over 50k attributes
- **Improved data protection** by elimination of decentralized data sources highly susceptible to data breaches
- **Automated Volume and Pricing Data Feed** reduced Financial reporting time from 8 business days to ~1 hour

100% Employee & Stakeholder Satisfaction

- **Data Quality, Reliability and Readiness** has continuously improved stakeholder satisfaction cycle over cycle
- **Improved Work-Life balance -** no more working extra-hours or weekends with noticeable stress reduction

Global External Manufacturing and Sourcing Poster Pop-Up 2024
Marta Teixeira marta.teixeira@intel.com
Beilei Zhu | Virginia Pulmano

N3B Best-in-Class CPU Yield

Exceeding 6% product yield target before PRQ

Great Collaboration with MPE Sort/Yield

- Established workflow to ensure content bring up with reasonable stability

Successful Collaboration with TSMC

- >$10M FOC ENG wafers for yield learning
- Fast PFA TPT support

product yield target achieved

>$100M Cost savings

Meet EOL Targets

FIFA Acceleration

- ARR Raster/SCN SPOFI enabled < 5 wks from first Si at sort
- 100+ PFA samples done at Intel PFA labs in PNG/Oregon/IDC and TSMC

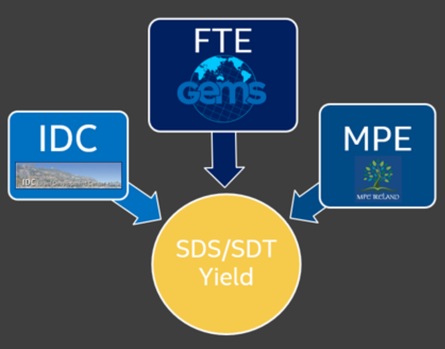
Fulfill ES2 Upside Demand

- 2X more LNL design wins
- Increase Intel true AI PC MSS in 2024

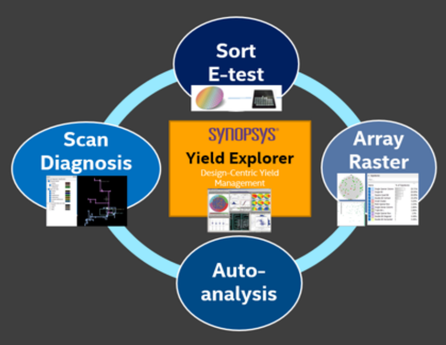
Relentless Yield Enhancement with Highest Quality Standard

Improving SDS Yield Steadily over Entire NPI Cycle

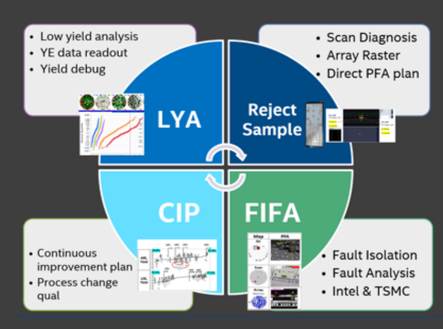
SDS/SDT Collaboration

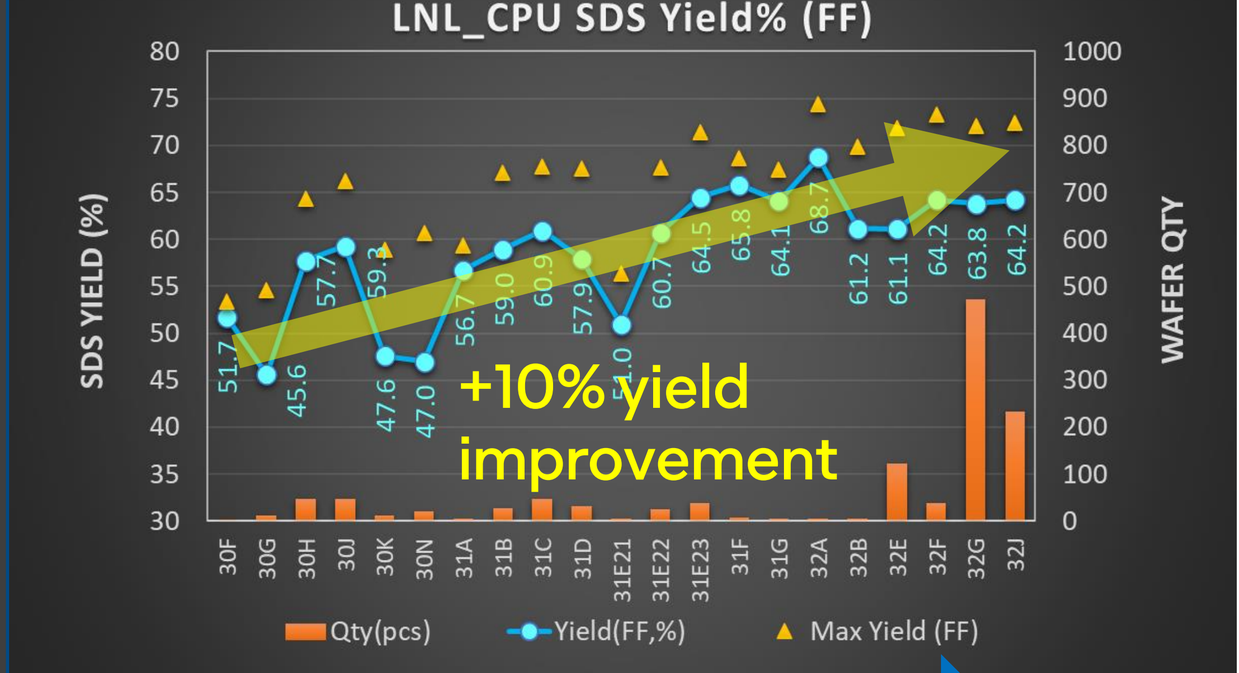


YE Data Integration



Yield Debug Feedback-loop





100+ yield debug FA performed

Increasing Test Coverage

Global External Manufacturing and Sourcing Poster Pop-Up 2024

Hsiang J. Huang | hsiang.j.huang@intel.com

Quality Mindset 1st
Zero Defect Zero Excursion

Quality as Top Priority in meeting Primary Customer's Expectation
Strong Partnership with our External Supplier as One INTEL
Influence Value of Quality Mindset First
Avoid Supply Chain Impact & Cost Saving

Excursion Reduction (Prevention) Program

Plan
- Line of Defense
- Risk Based Thinking
- Mindset & Competency
- Supply Chain Shared Learning

Do
- Systemic Defense
- Early Warning System
- Equipment Management
- Best Known Method
- Supplier Quality Assessment

Check
- Leading indices (Line stability)
- Lagging indices (Quality)

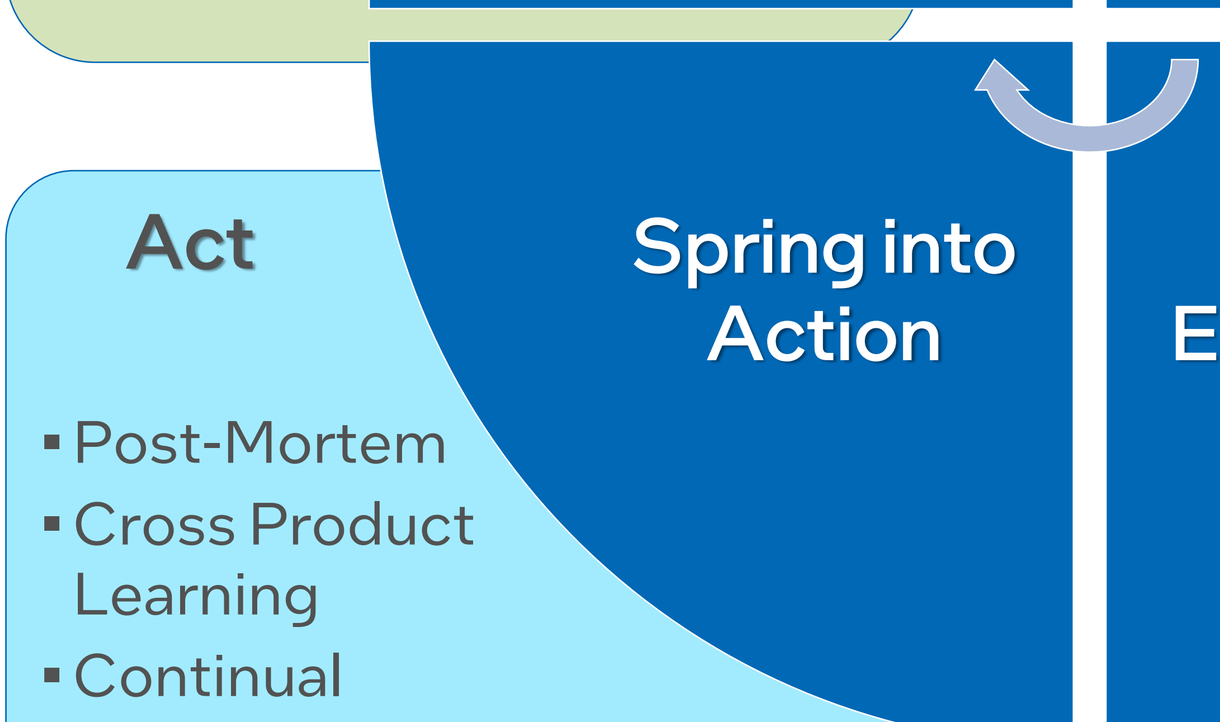
Act
- Post-Mortem
- Cross Product Learning
- Continual Improvement

Safeguard Strategy

Excellence Drive

Spring into Action

Impact Evaluation



Quality performance of a Foundry Supplier

Partnering with Our Suppliers makes Total Quality Defense

Never have to say Sorry to your Customer

Global External Manufacturing and Sourcing Poster Pop-Up 2024
June Chua |hweengoh.chua@intel.com

Torrid CT for 2.5D Assembly

Cost-Effective Solution for Accelerated Si Debug
with 1W TaT for Assembly

Shorter Time-to-Debug
Accelerate Si FA/FI

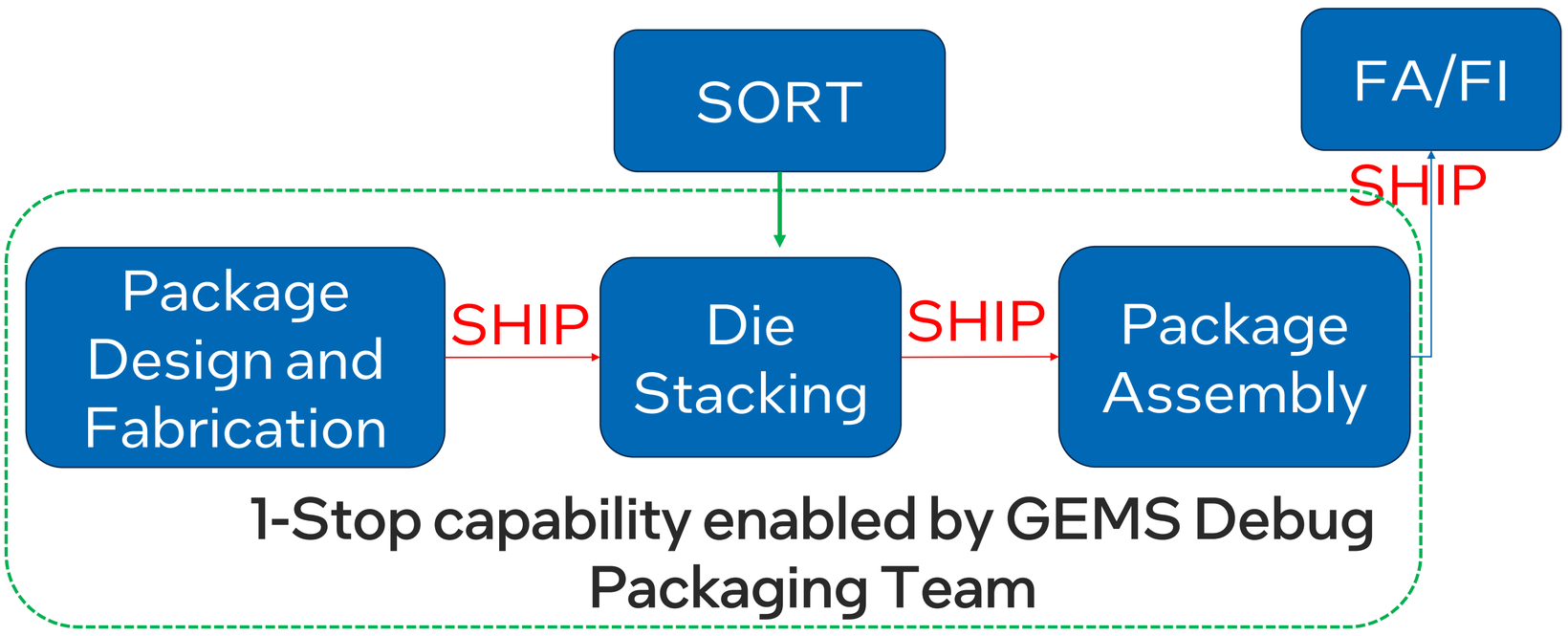
1Q to 1W Assembly Cycle Time

Low Cost
30% Cost Reduction
Fully GEMS Owned

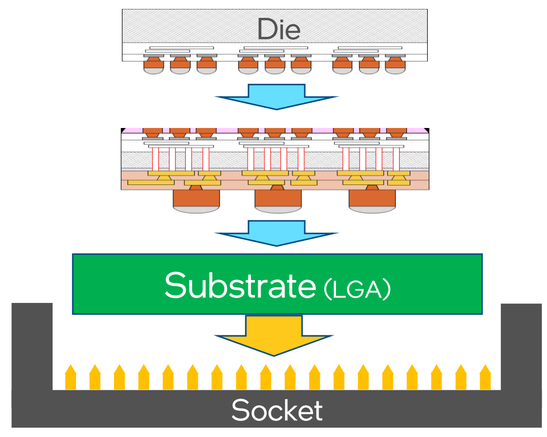
1W TaT for 2.5D Si Assembly
Innovative pre-assembly

Simplified Flow
1-Stop Shop for Design-Assembly-Fabrication

Simplified flow in GEMS Package Debug Assembly



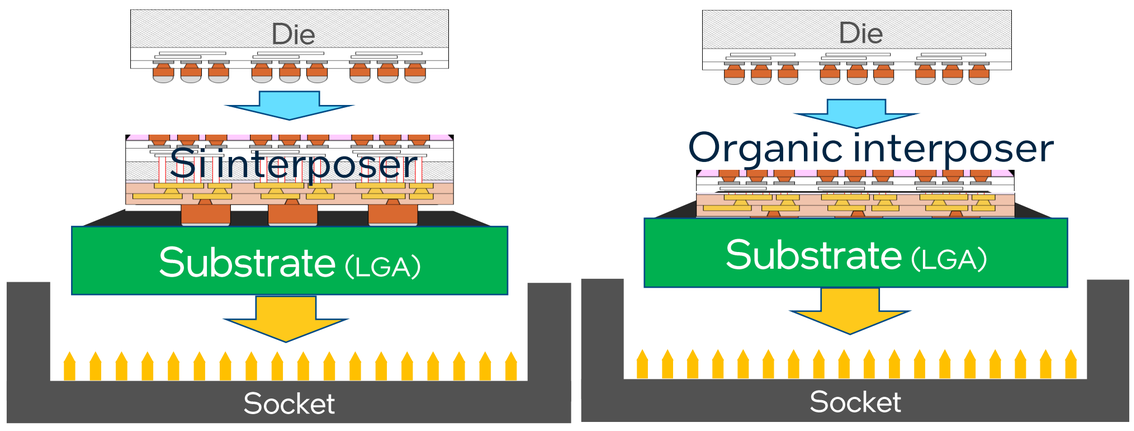
Internal POR Assembly



3 months for Assembly

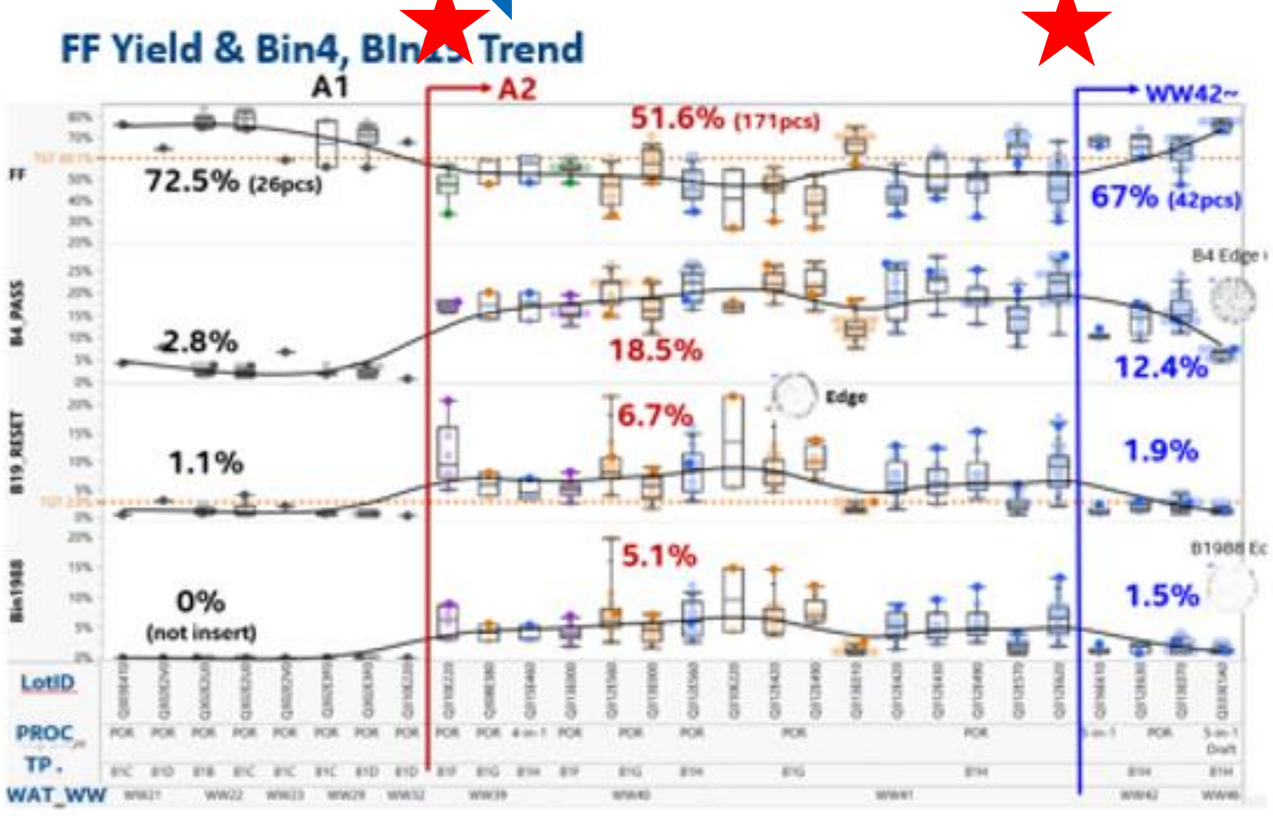
vs.

GEMS Capability



1 week for Assembly

12 week gain in Yield Improvement TaT



Global External Manufacturing and Sourcing Poster Pop-Up 2024
Vasudev Ganesh | vasudev.ganesh@intel.com

High velocity OSAT Cycle Time

35% CT reduction for production volume

Partnership
Collaboration
Negotiation with OSAT

Intelligence
Data driven approach
Benchmarking

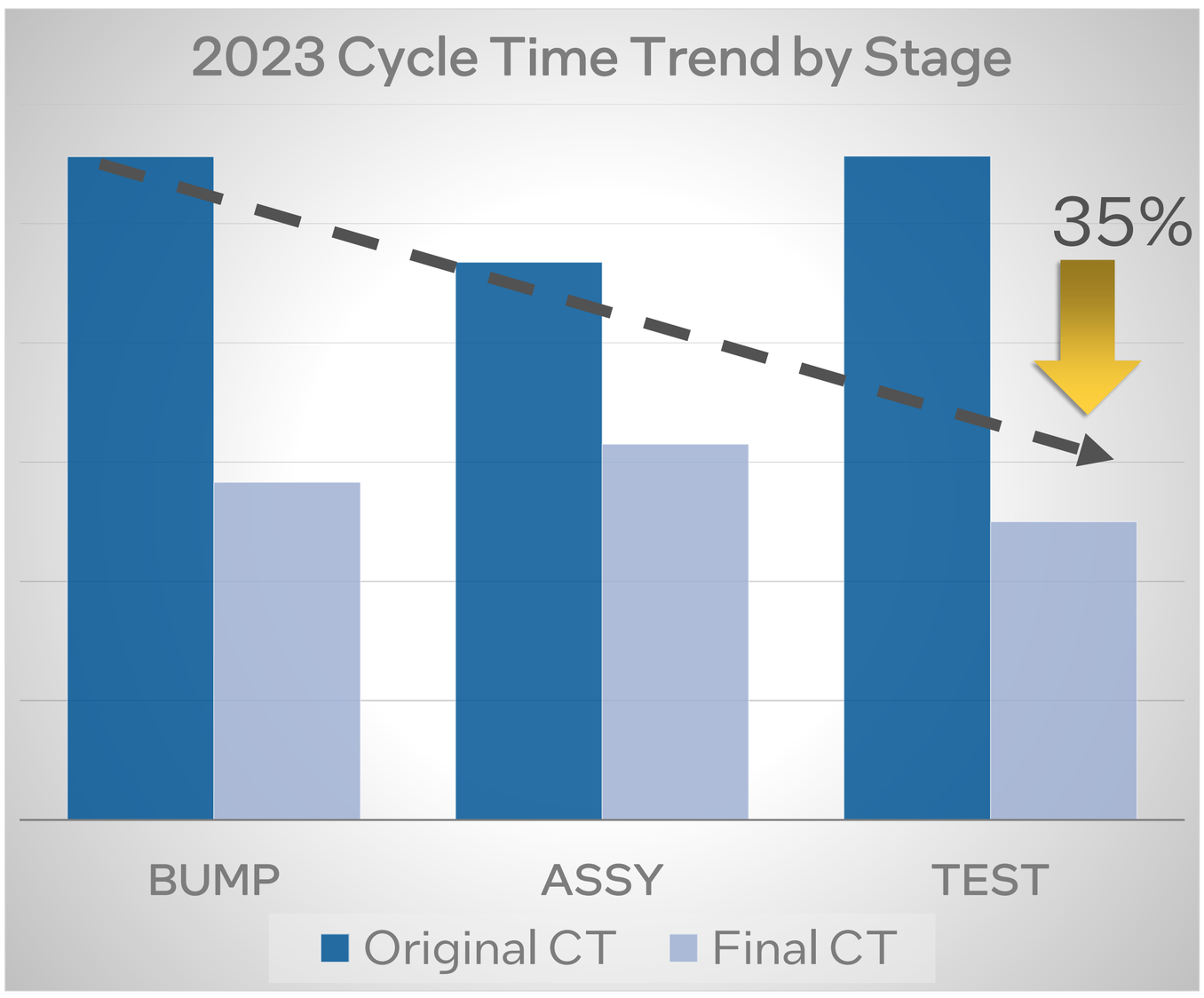
$7M
Positive cash flow

Capacity
Supply improvement
Enhanced supply flexibility

Execution
Disciplined monitoring
Continuous improvement

Optimizing end-to-end CT across manufacturing stages by 1-2 weeks

Products	OSAT CT improvement
Thunderbolt	From 34 to 25 days
WIFI	From 27 to 18 days



Established systemized approach for application to other products and technologies, e.g MTL-PCH

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Yen Mei Ng | yen.mei.ng@intel.com

MTL HVM Achievements

Developed a promising system for foundry management and test stability

Foundry Management
Inline & Tool correlation

Early Warning System
E-test, Yield, Bins, Para & Diagnosis

$8M
Pull-in Value in 2024

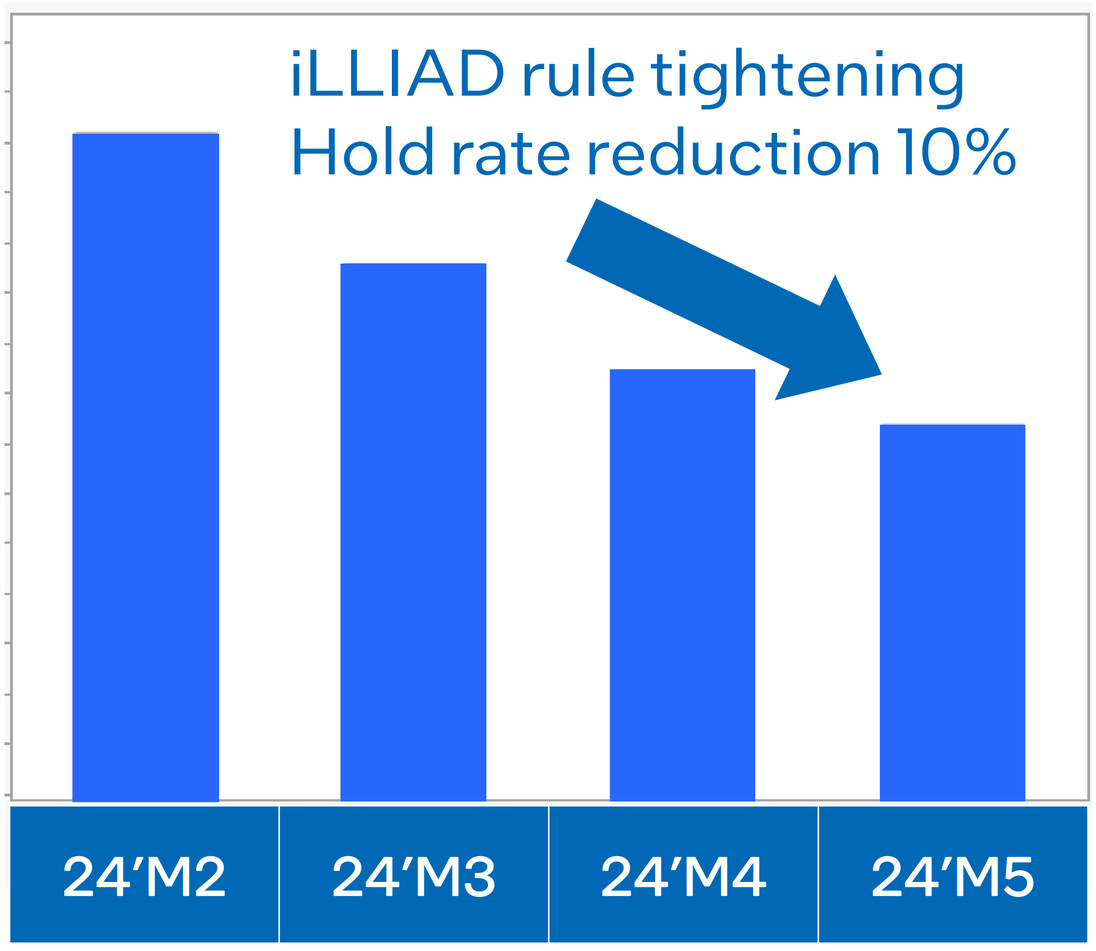
Task Force
Test stability & foundry excursion management

Implement CIP
Risk assessment, Yield evaluation

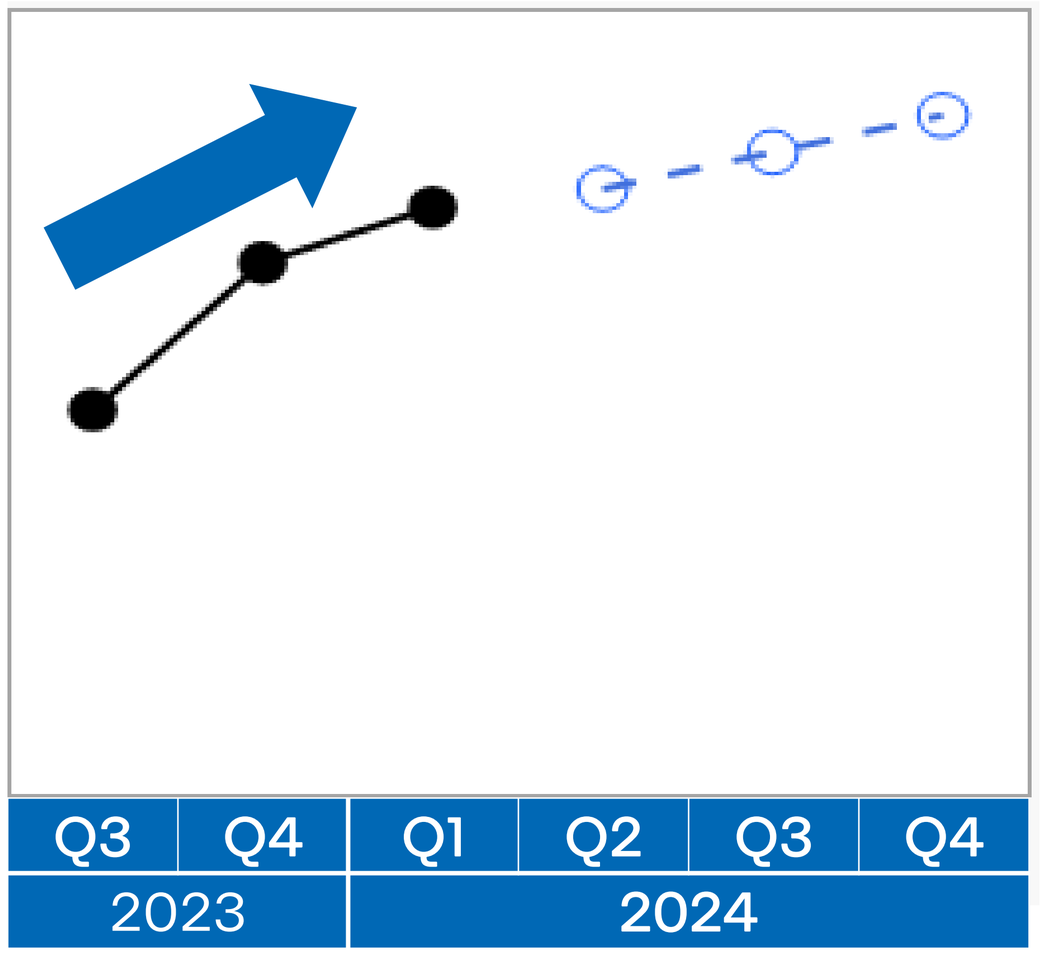
Milestone & KPI

EWS Gating	Event gating ahead 2 months
BEOL CIP	Yield +0.1%
iLLAD Tightening	Yield +0.1%
Device Tuning	Yield +0.2%
FEOL CIP	Yield +0.2%

Test Overkill Reduction



Yield Roadmap



Global External Manufacturing and Sourcing Poster Pop-Up 2024
Baker Lin | baker.lin@intel.com

Change Control Board Powering Intel's IDM 2.0

$+2.1B

Cost Affordability GEMS Contributed

Yield Improvement

1. Contributed $9.8M for cost saving and $2.8M for cost avoidance
2. Evaluated over 100 BKM from 4 foundries

Business Continuity

1. Contributed Revenue support of $2 Billion
2. Avoided revenue interruption for 10K+ wafers and 10+ products annually.

Reliability Enhancement

1. Further enhance wafer quality and reliability
2. Achieved 6.5% VBD improvement by BKM implementation

Excursion Prevention

1. Zero excursion to CCB change in 2022 and 2023

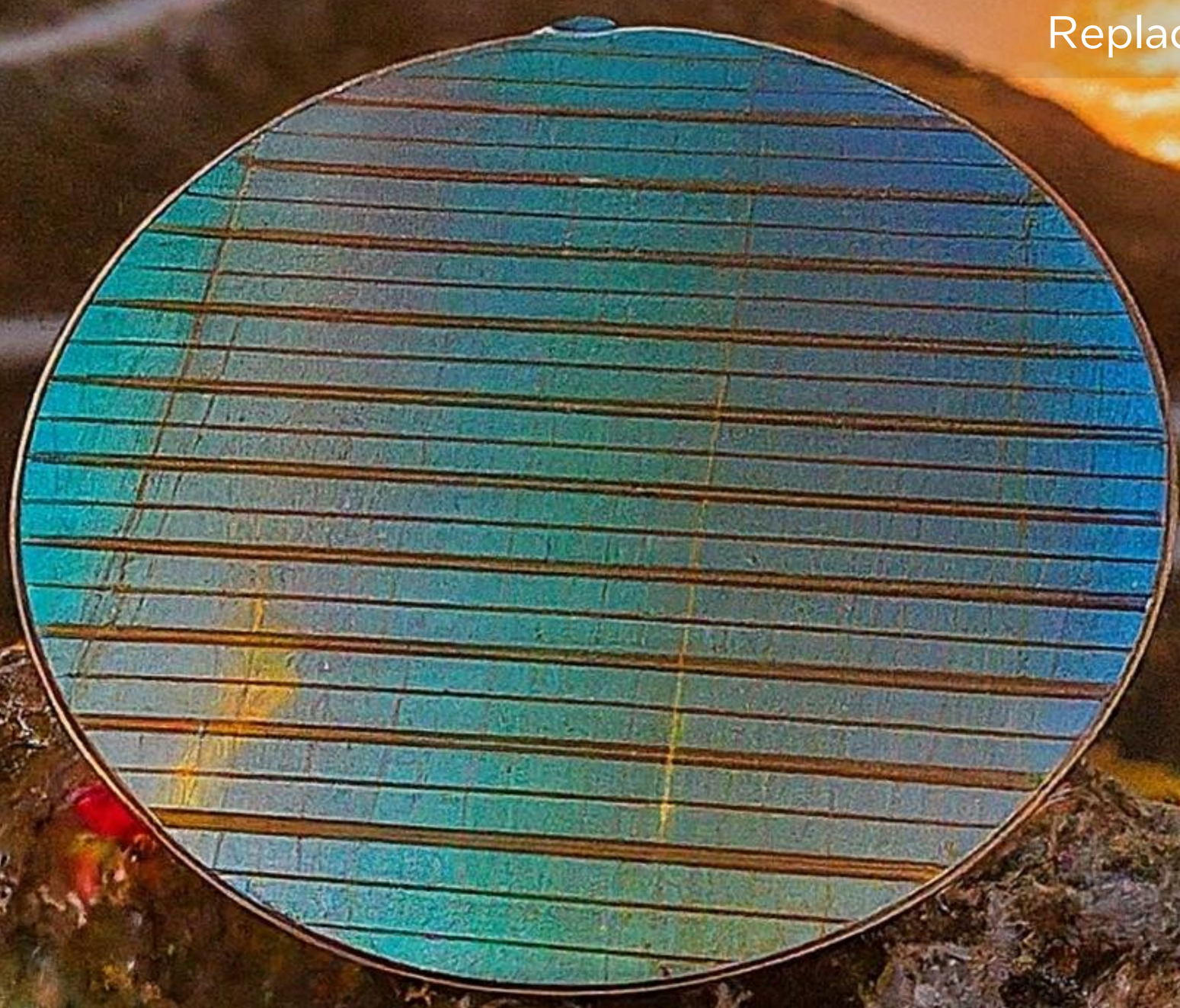
Global External Manufacturing and Sourcing Poster Pop-Up 2024
Lawrence Yu | lawrence.yu@intel.com

Long Road to the Victory
14nm PCH Foundry Excursion Management

Impacted
13,644 wafers

Data Driven
Pattern detection, DOEs,
Screening Development
Scrap Decision

Execution
Test/Shipping Management
Materials Disposition
Replacement & Credit



$18M Value saved
Potential 3Mu Recall avoided

Work accomplished by One Intel Team
GEMS EMP FM, MQE, EMS, QnR, F24/F28/CDAT/VNAT

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Global External Manufacturing and Sourcing Poster Pop-Up 2024
Tung-Wu Hsieh | tung-wu.hsieh@intel.com

Global External
Manufacturing & Sourcing

Wi-Fi 7
Yield +3%

$2.6B

+9.22%

WIRELESS

Outstanding Products

GEMS secures billions in revenue preservation and over **$10 million** in cost saving by foundries':

Sustainable Delivery

Second-source photoresist sustained business continuity plan and prevented **$2.6 billion** in cost losses.

Continuous Process Improvements

in Wi-Fi 6E with strategic Si gate height control, contributing **$1.82 million** cost avoidance from module yield enhancement.

Wi-Fi 7 executed defect reduction and device optimization, leading to **$11.76 million** cost saving from a 3% yield gain.

Capability

Affordability

Stability

Bluetooth

6 6E 7

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Global External Manufacturing and Sourcing Poster Pop-Up 2024

Jing Chen | jing4.chen@intel.com

Manufacturing Affordability

+50 Products Sustain

+90 Projects Acceleration

+131M Affordability Contribution

----One Intel---

Global External Manufacturing and Sourcing Poster Pop-Up 2024
Liao Chiahsin | chiahsin.liao@intel.com

PROPELLING 28NM PRODUCTION YIELD TO GLORY

Achieved cost savings of $6.9 million through collaboration with BU and Foundry

+$6.9 Million

One Intel

Synergized with BU to achieve remarkable yield improvement

FXL	HDB
+$4.0M	+$1.4M
Yield +2.8%	Yield +33.0%

Quality

Engineered foundry CIPs to elevate product quality

MPR & HDB
+$0.3M
Yield +0.8%

Customer First

Investigated device window and strategically prioritized to fulfill customer demand

CLF
+$1.2M

Civen Hong | civen.hong@intel.com

EARLY WARNING SYSTEM IN HVM

Monitoring overall exceeds 400 diverse items to early detect abnormality including inline/device performance/testing automatically daily.

PCM
- BSL Drift & Variation
- Excursion abnormal (Lot/Wafer/Site)

Datalog
- BSL Drift & Variation
- WiW Uniformity

Performance
- RO performance monitoring

Yield
- Yield P90&P10 monitor
- Field related index

Diagnosis
- FMA for Logic
- Signature analysis for ARR

EWS pre-warned 30+ cases successfully for MTL in 2024

Achievement	2024 Goal
Automation System	Execute in ARL/LNL
Daily Warning	Accuracy reinforcement
Trigger rate Monitoring	

Global External Manufacturing and Sourcing Poster Pop-Up 2024
Chris Chen | chris1.chen@intel.com

Excellence in Foundry Excursions Castaway

Contributors: EMP_FM and GSMQR

85%↓

MRB/DRB reduction from 2017-2023

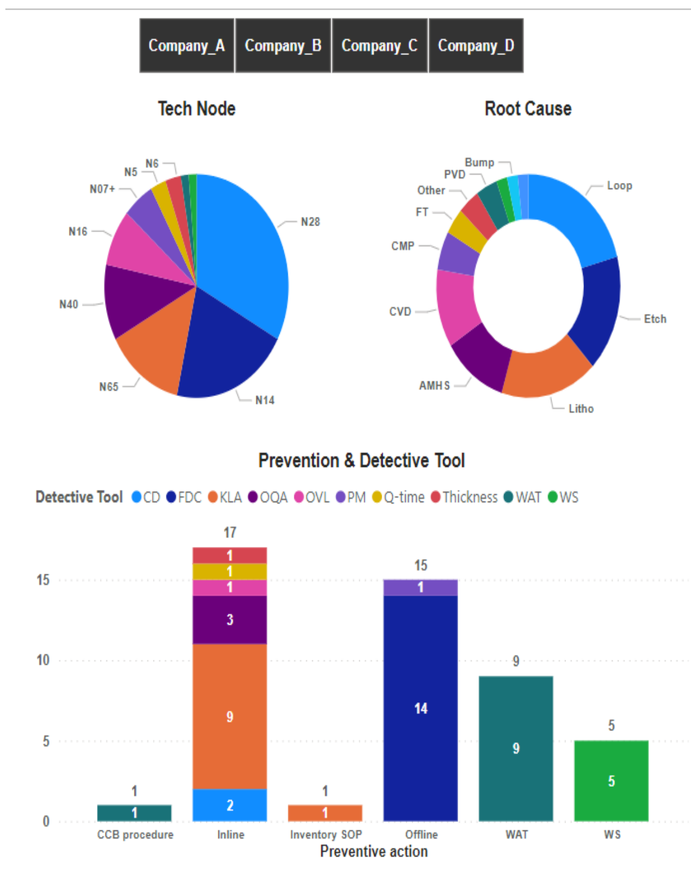
Event Prevention Review

Event Library

Cost Affordability

Efficient preventive action review

Web-view event library cross suppliers



Quarter	File Name
21Q4	001_Company_C_N65_AMHS Defect Issue_Timmy
21Q4	003_Company_A_N28_Asher Tool-A line type defect_Christine
21Q4	007_Company_D_N65_AMHS robot tool issue_Eric
21Q4	008_Company_C_N65 Litho wafer edge scum issue_Timmy
21Q4	009_Company_C_N28_Wafer Center HV Loss_Christine
21Q4	010_Company_A_N28_IMP flood gun abnormal issue_VincentL
21Q4	012_Company_B_Etch Tool Scratch Issue_Tung-Wu
22Q1	013_Company_D_N40_OQA Frontside Discoloration_Janice
22Q1	014_Company_A_N28_OQA Circle Scratch Defect Summary_Tyler
22Q1	015_Company_D_N28_WS_HBin1_Degradation_Analysis_Eric
22Q1	016_Company_D_N65_Abnormal Bondpad_Eric
22Q1	017_Company_B_N14_Ash tool scratch issue_Sharon
22Q2	020_Company_A_N7_Poly CD induced edge WFM defect low yield_William
22Q2	021_Company_A_N16_Bin81 and 82 Yield flunctuation_Lawrence
22Q2	022_Company_C_N65_CUSPUT Particle Issue_Timmy
22Q2	023_Company_A_N16_Wafer edge low yield_Lawrence
22Q2	024_Company_C_N28_DARC tool down notification_Christine
22Q2	025_Company_C_N65_Metal Damage Defect Issue_Timmy
22Q2	028_Company_A_N28_SEAL SiN dep. Tool A nozzle broken_Christine
22Q2	029_Company_B_N14_eSiGe_Chamber induce M1 shift_Sharon
22Q2	030_Company_A_N16_HBIN3+4 CIP_Lawrence
22Q3	033_Company_A_N65_Litho tool reopen induce defect Bin Yield loss_VincentLin
22Q3	034_Company_A_N28_Device MOM cap issue_Vicky
22Q3	035_Company_B_N14_PC to eSiGe short_Sharon
22Q3	036_Company_A_N7_DLCP to SICC performance_William
22Q3	037_Company_C_N65_STI bridge defect_Timmy
22Q3	038_Company_C_N28_STI SiN_Emb Defect issue_Cristine
22Q3	040_Company_D_N65_CA RIE Block etch inline pre-alert_Baker

Leads to save invisible cost affordability

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Torrid Fast Cycle Time

Expedited >6,000 days for >430 NPI lots without extra cost
(average pull-in 2 weeks/lot)

Relationship
Local Connections
Influences

Intelligence
Local Channels
Negotiations

$105M
Pull-in Value in 2023

Talent
50+ Years' Work
Local Foundry Experiences

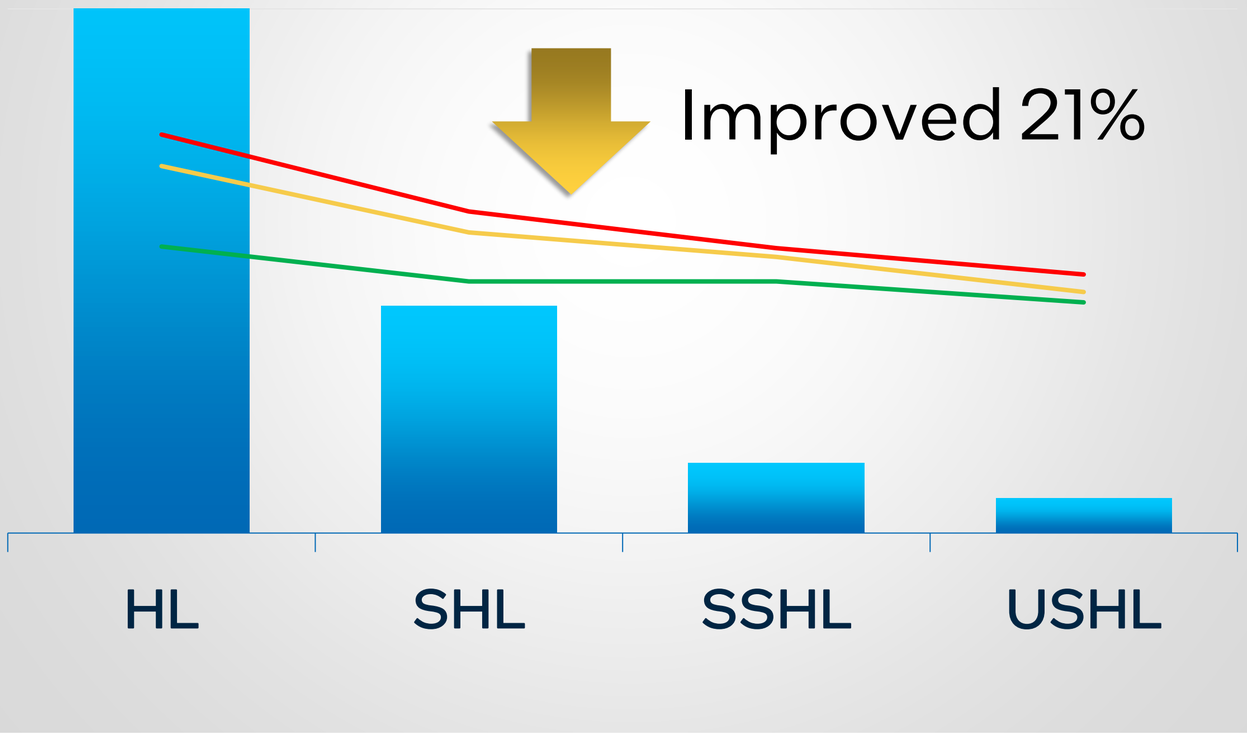
Execution
Local Fab & HQ Planning
Collaborations

NPI Wafers Pull-in

Meteor Lake	173 lots, 17 days	Time-to-market
Lunar Lake	36 lots, 10 days	
Arrow Lake	53 lots, 22 days	

Pull-in Value YoY +$70M

TPT Goal Improved & Further Pull-in



Winston Tsai | winston.tsai@intel.com

Packaging Idea to Production

External Packaging End to End Solution to Enable IDM2.0

Take Full Advantage of Global Ecosystem

Advanced Packaging Enablement

IDM 2.0 Enabler

Diverse Packaging Product Development & Production

Enhance Intel Foundry Packaging Portfolio

NPI Project Summary

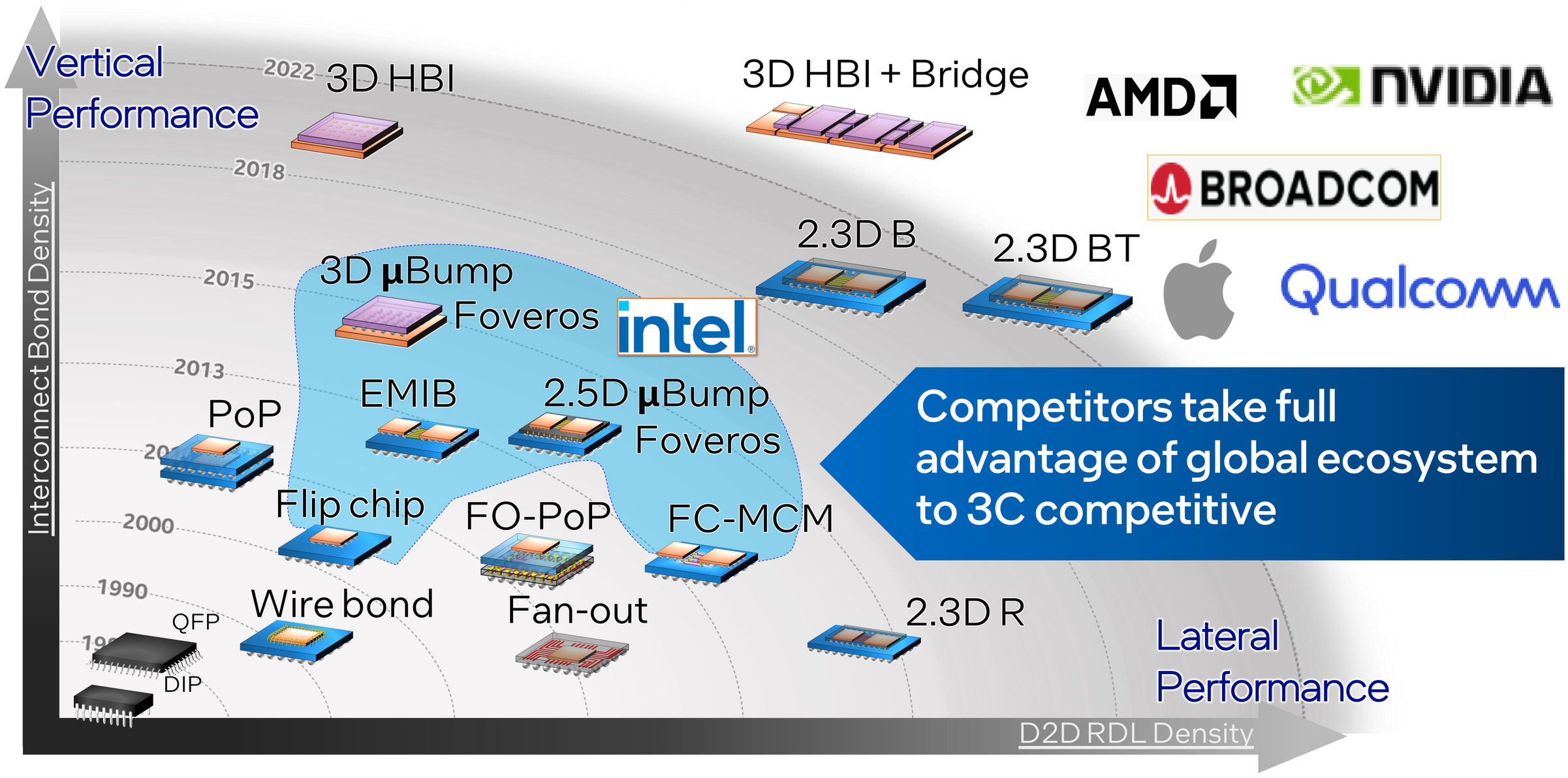
19 PRODUCTS

8 BU/DIVISIONS

9 PACKAGE ARCHITECTURES

8 OSAT SITES/FACTORIES

External Packaging Landscape vs. Intel's



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External Packaging Technology Enablement

Advanced packaging solutions with external partners
- Shorter Time-to-Market at lower cost -

Advanced Packaging
Variety of packaging options
2.3D BT
3D u-bump (15um pitch)

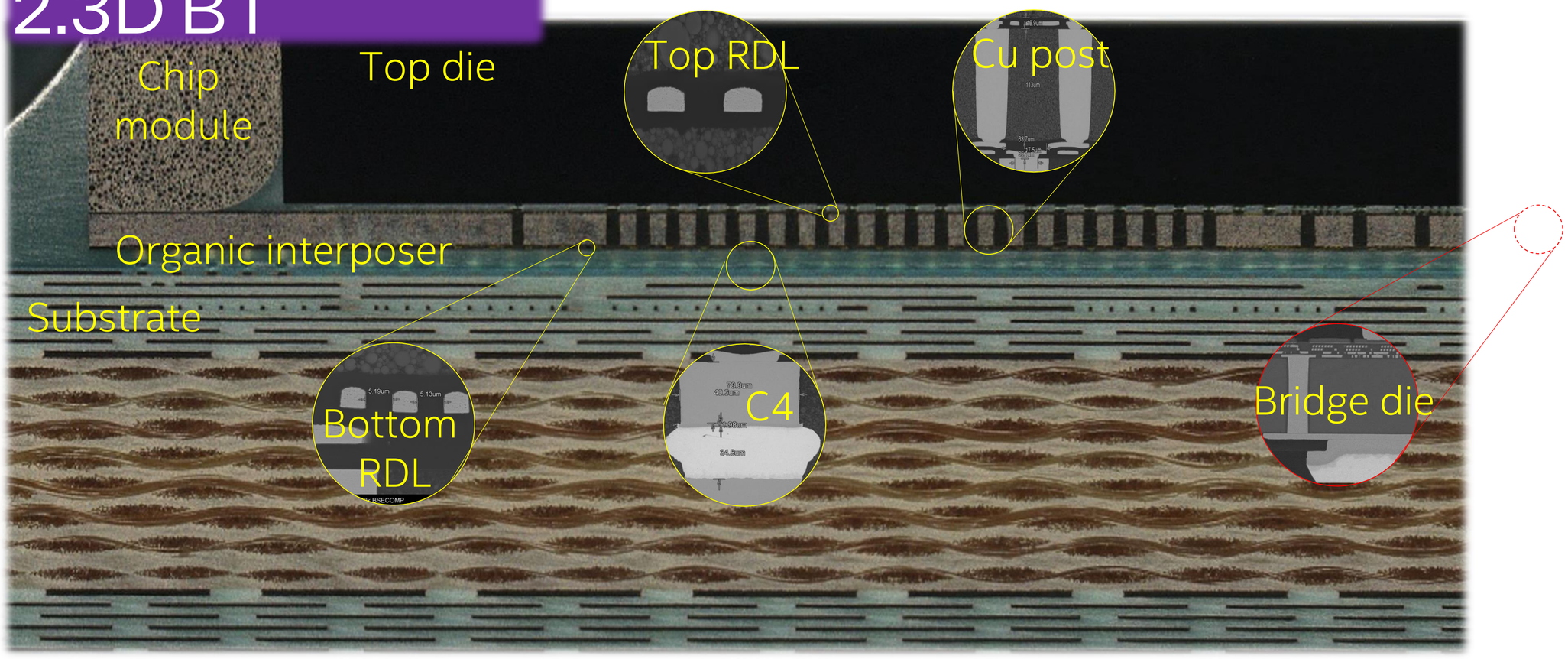
Silicon Integration
Silicon from multiple sources
Variety of silicon nodes
At various OSATs

25%
Shorter Develop Time

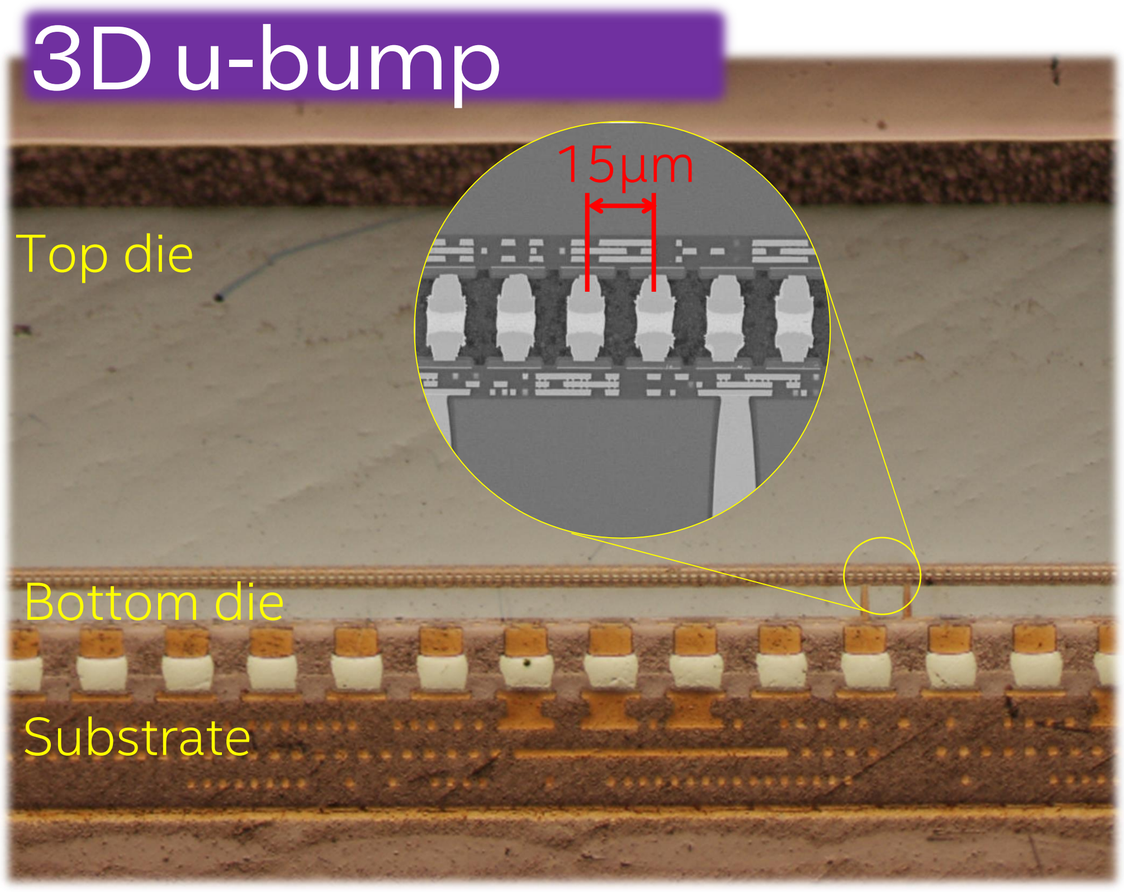
Co-design Flow
Assembly design kit (PDK)

Virtual DOE
Reducing DOEs by 50%
Reducing cycle time by >17 weeks

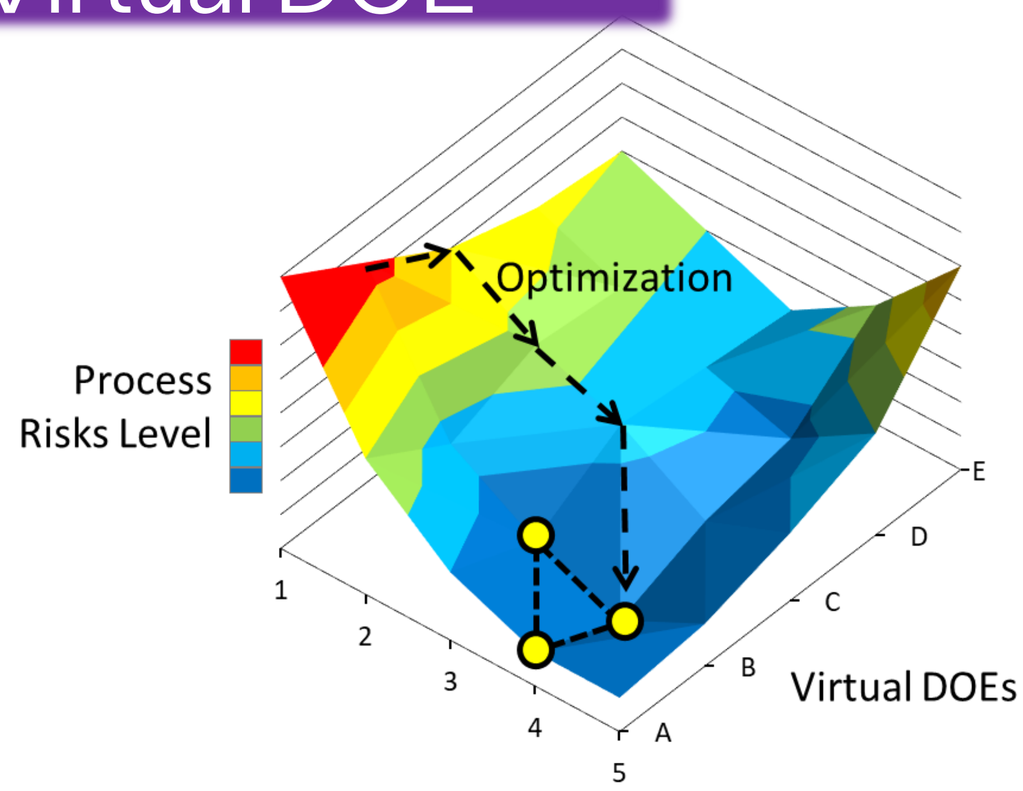
2.3D BT



3D u-bump



Virtual DOE



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PC Renaissance -

First Intel 47 TOPS AI PC - LNL is coming

Performance
Implemented 9 Process Device CIPs to Boost Performance
- Fmax +3% (+150MHz)
- Vmin -30 mV
- SMP +5%

Quality
Optimized Process and Testing
Stable Array (1σ Vmin<10mV)
Diagnostic De-bug flow
Tighten In-line control with CP/CPK monitoring

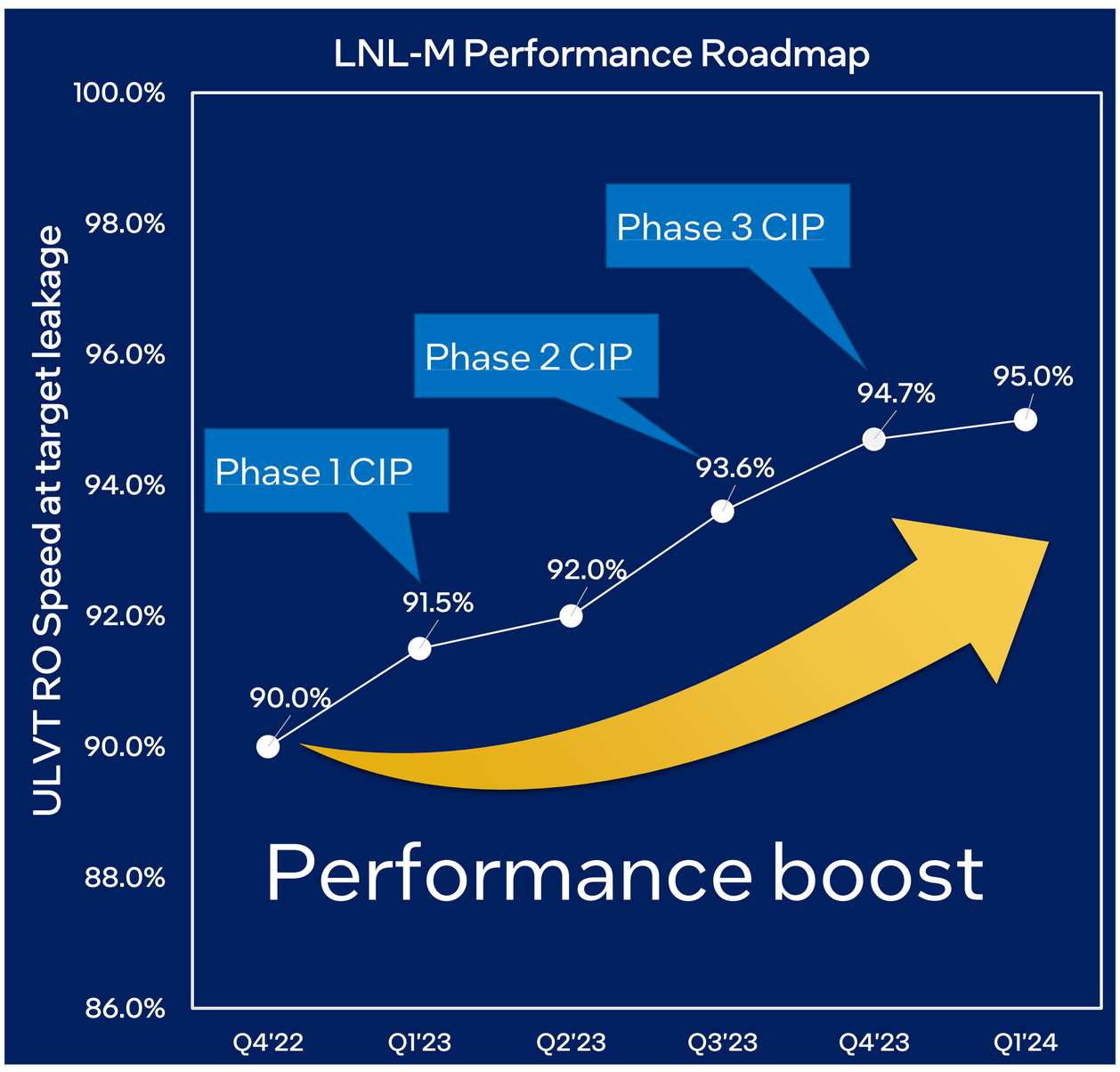
> $6B

Additional Revenue Due to the Superior Performance

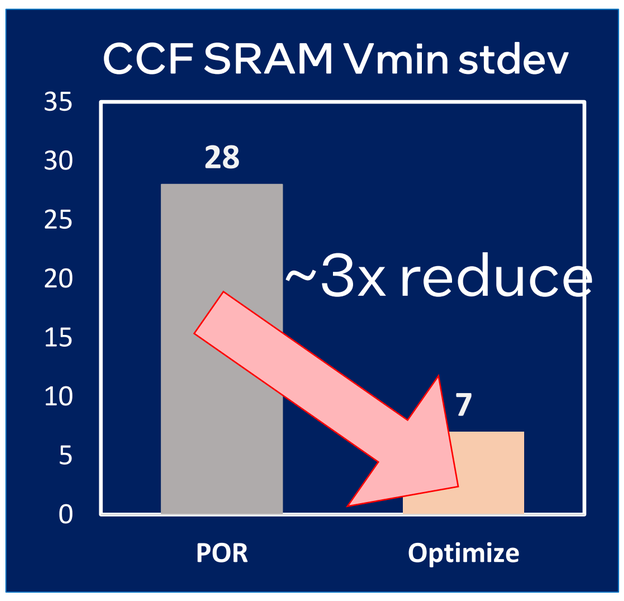
Low Leakage
Reduce 20% stand-by power consumption meeting battery lifetime spec.

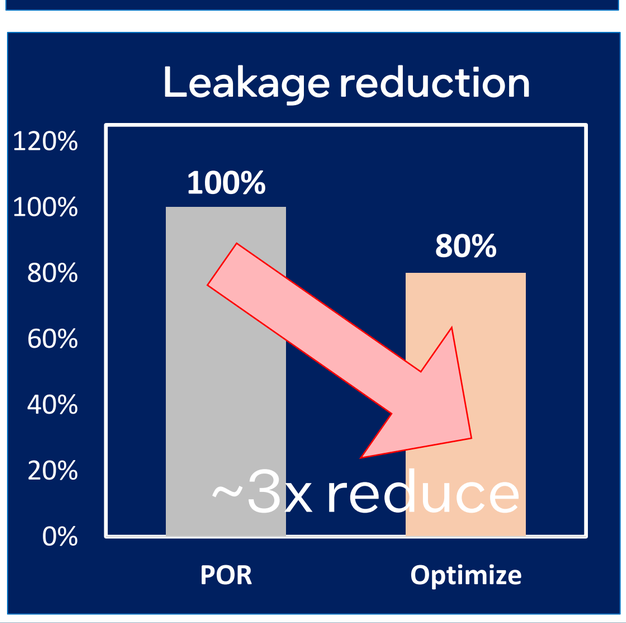
ESG Value
Lower power consumption is estimated to potential carbon emission reduction by 146000tons annually.

Performance



Quality





ESG Value

Potential yearly 146000 tons CO_2 reduction

Equivalent to 5000 soccer field areas of trees to absorb!

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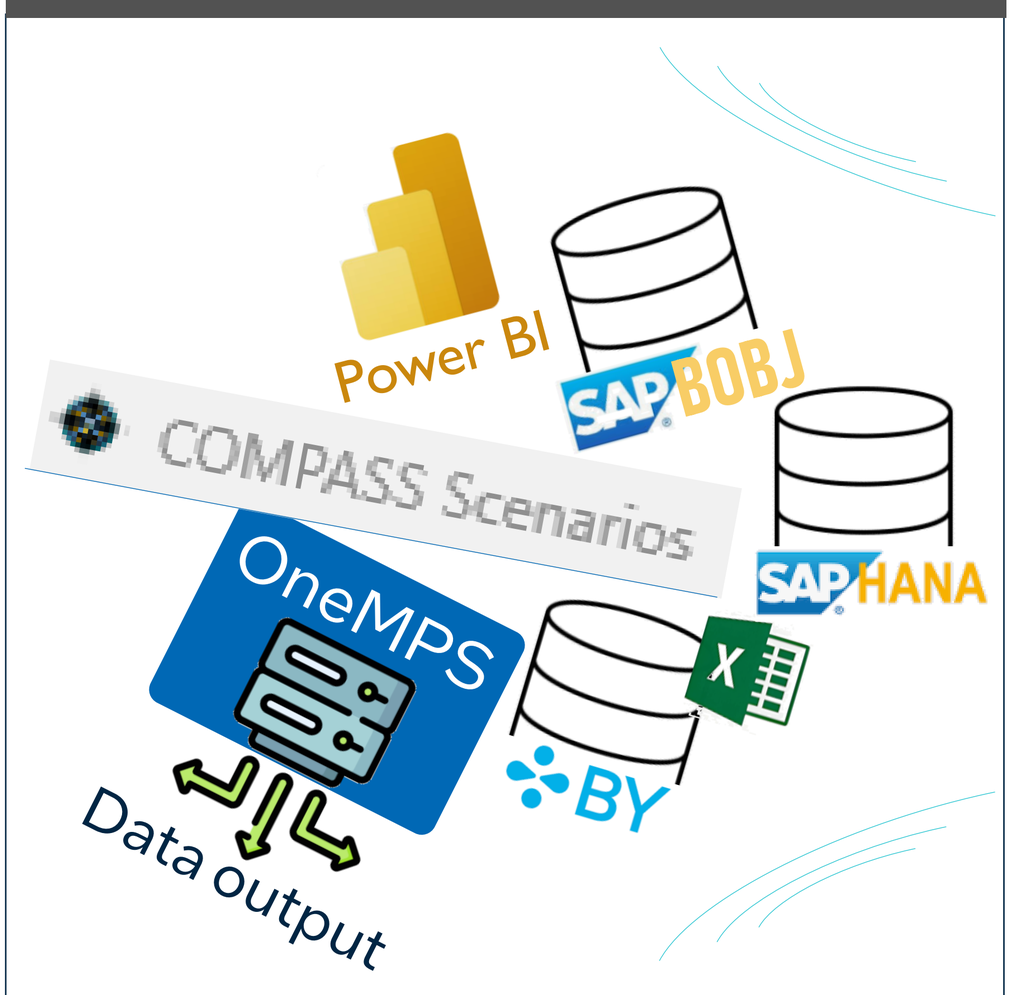
Capacity Reporting *evolved*

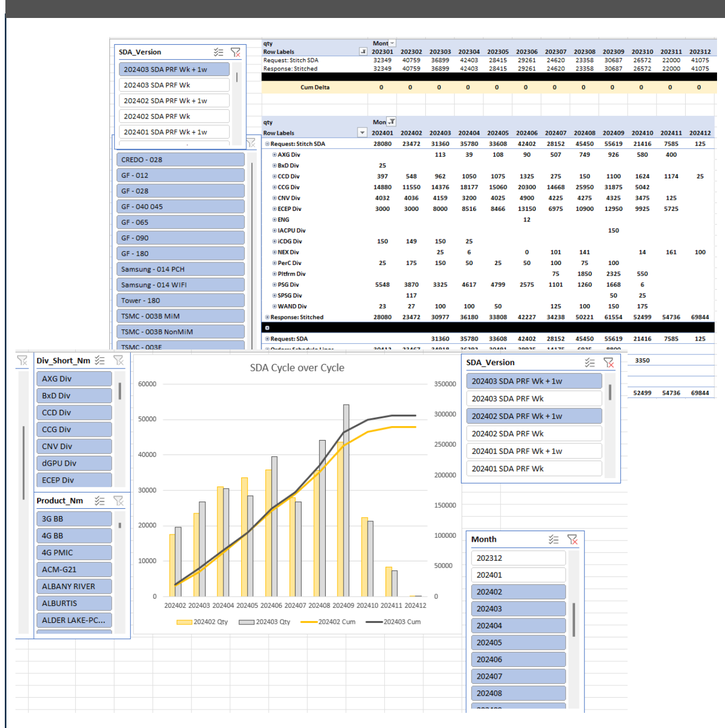
The Foundry Capacity Report is a keystone record which centralizes critical data for external foundry planning

Data in…



…Stitch Engine…

…*Information* out



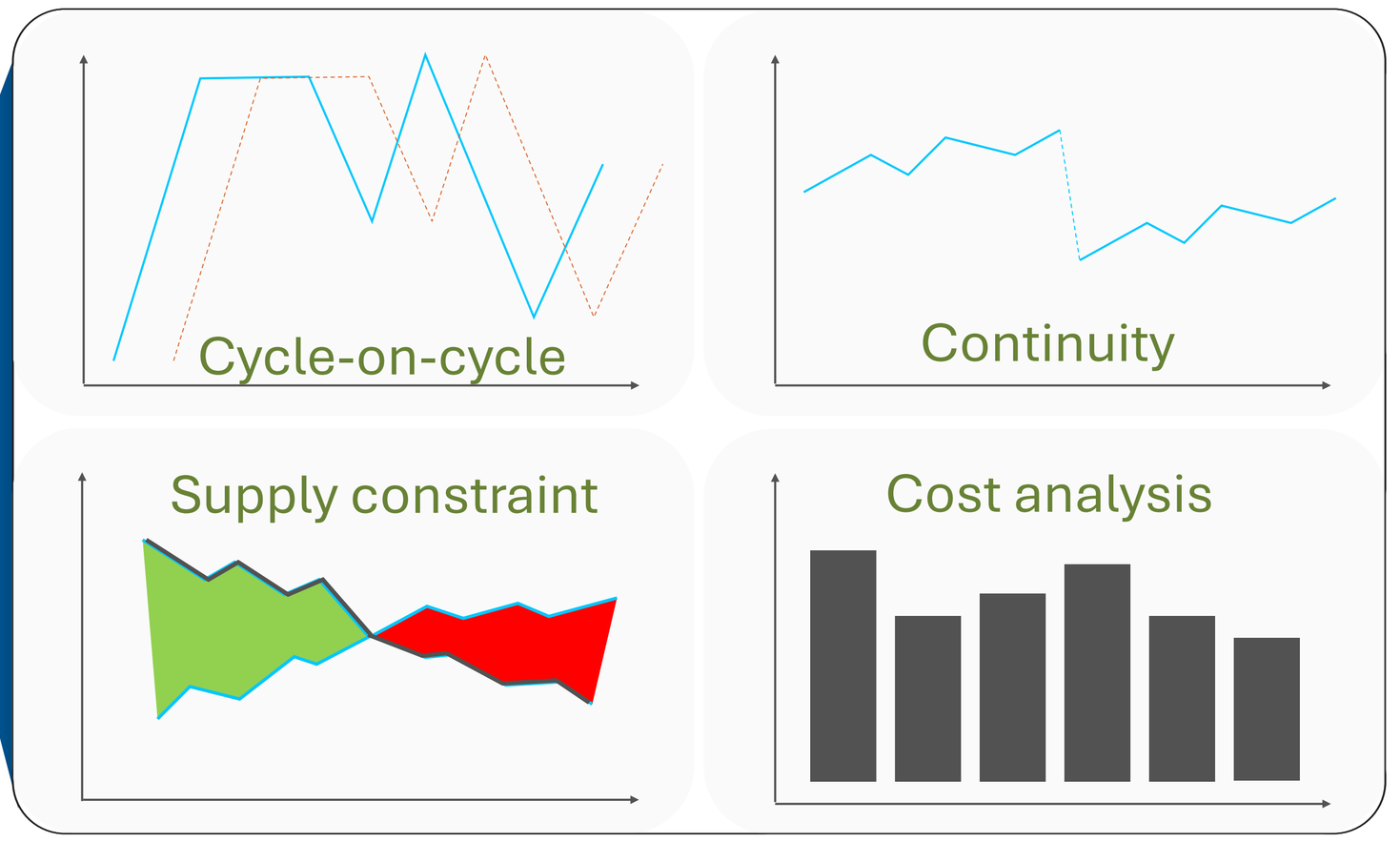
- *24-month wafer demand*
- *Supplier Capacity Response*
- *Orders, Shipments, Commits*

Comprehensive

Single Source of Truth

Enabling Analytics

and the backbone of other supply planning reports and analysis among user base



Reporting evolution

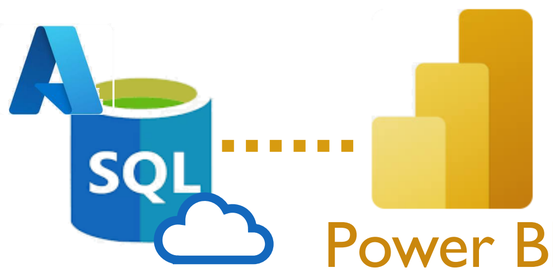
2023 AUTOMATE

Massive automation upgrade

4x update freq.; 95% time savings

Longer horizon, higher accuracy

2024 ENTERPRISE



Shared DB structure

Custom PBI views

Auto-scheduled runs

2024+ SCALE

Additional data sources

Integration with a full suite of KPIs, dashboards

With contributions from:
John Pete Sachin Rastogi
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