JEDEC

Global Standards for the Microelectronics Industry

Jedec Memory for Automotive LPDDRx & UFS

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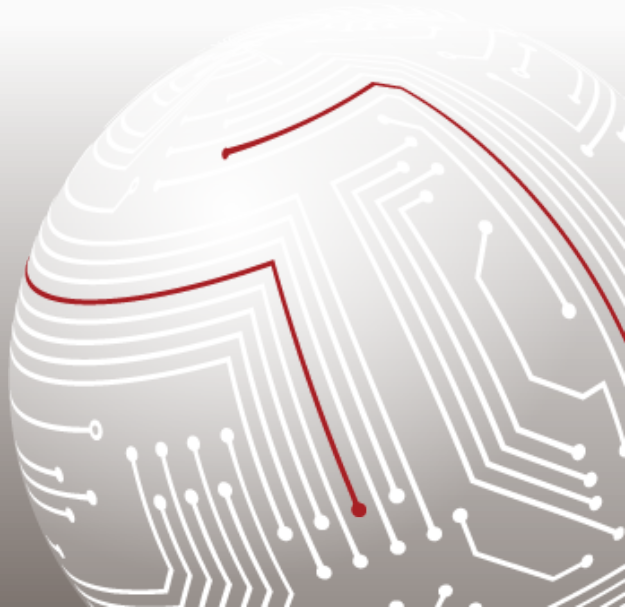
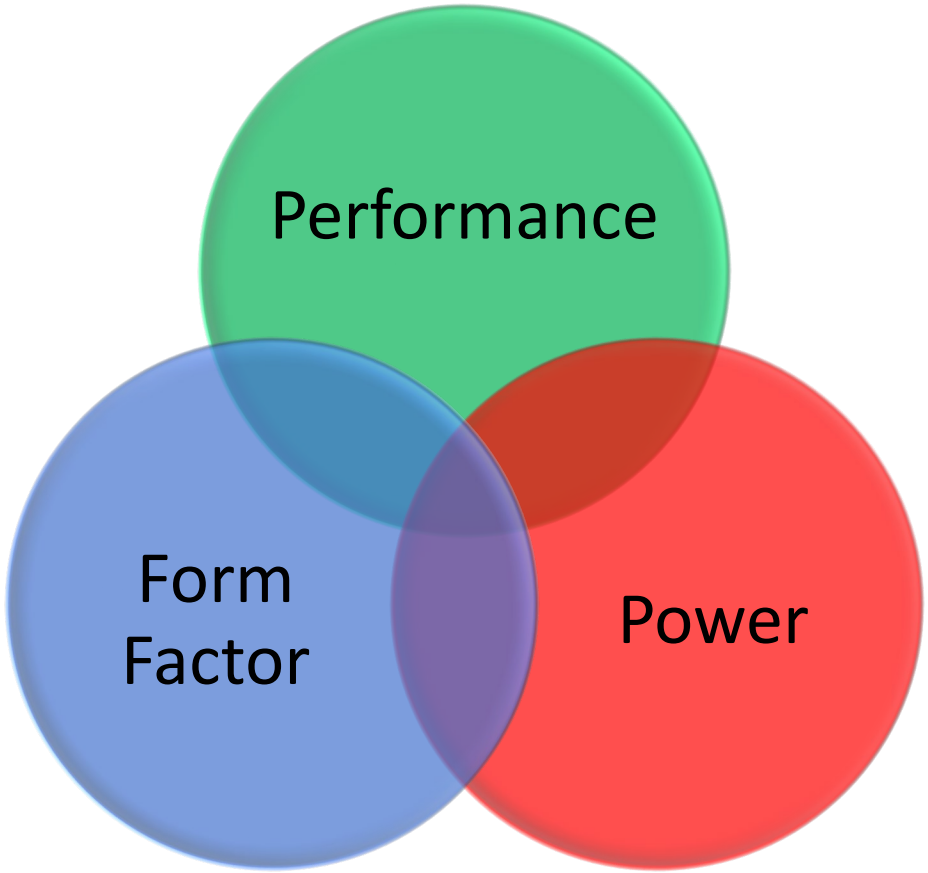
Qualcomm Inc



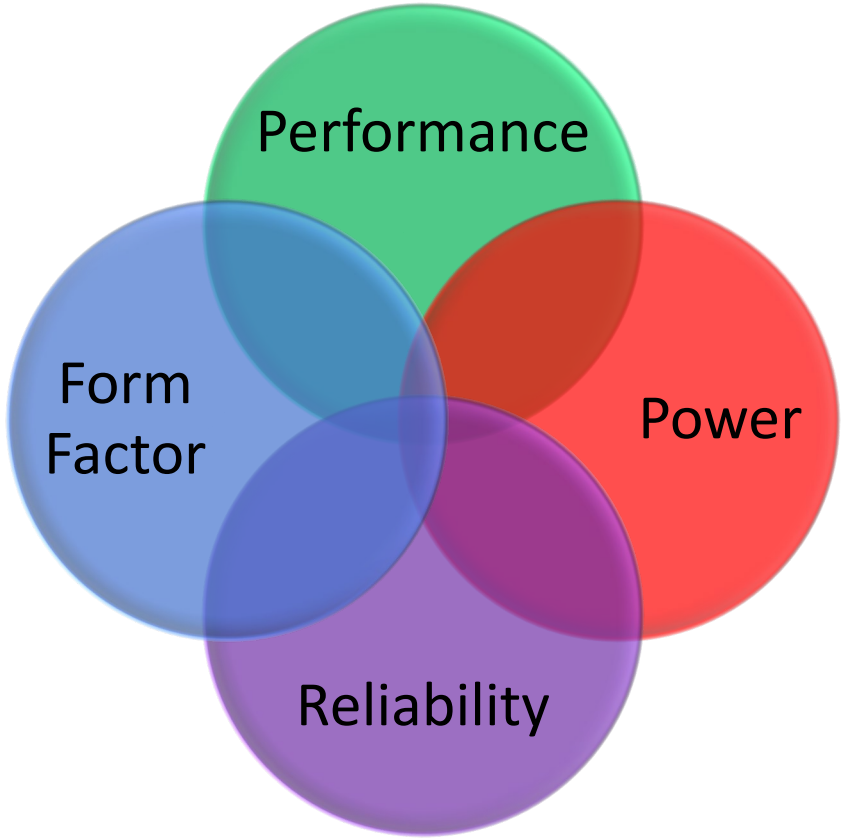
Memory Trends & Direction

- Jedec memory trends have always been about Performance, Power efficiency, and smaller form factor
- Jedec continue to address growing opportunities – compute, IoT, XR, etc.
- Automotive market brings new challenges

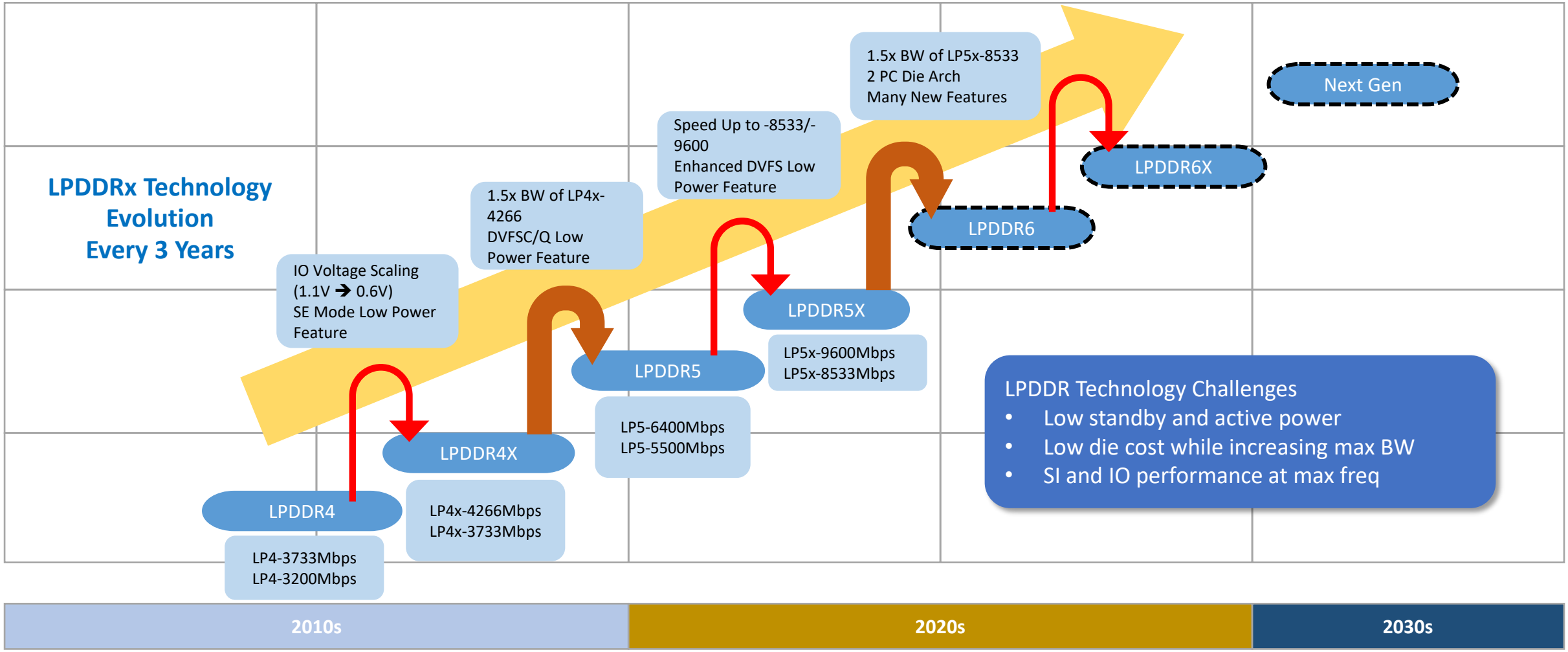


Automotive Memory Challenges

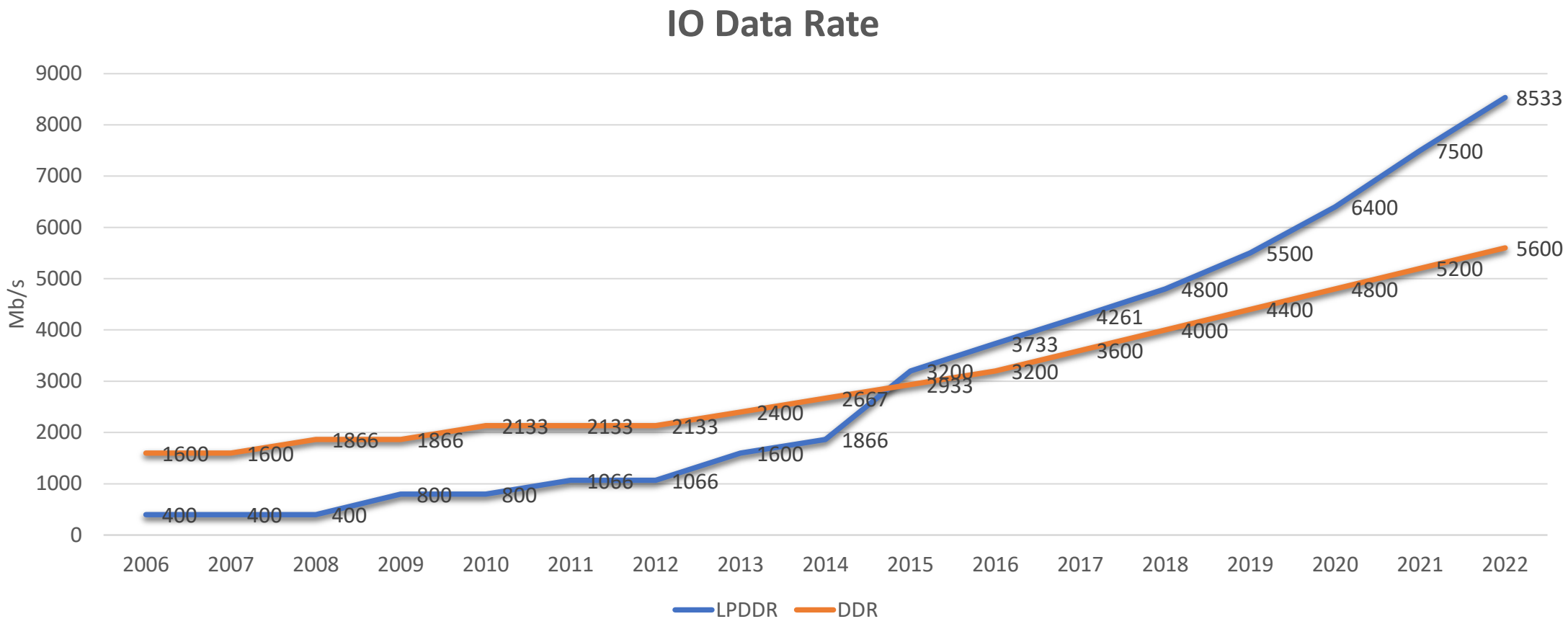
- LPDDRx performance & power efficiency are attractive, even for automotive market
  - LPDDR4x performance
  - Low latency
- But there are challenges for LPDDRx in the automotive market
  1. Data Reliability
  2. Improving Boot time



LPDDRx Technology Trends

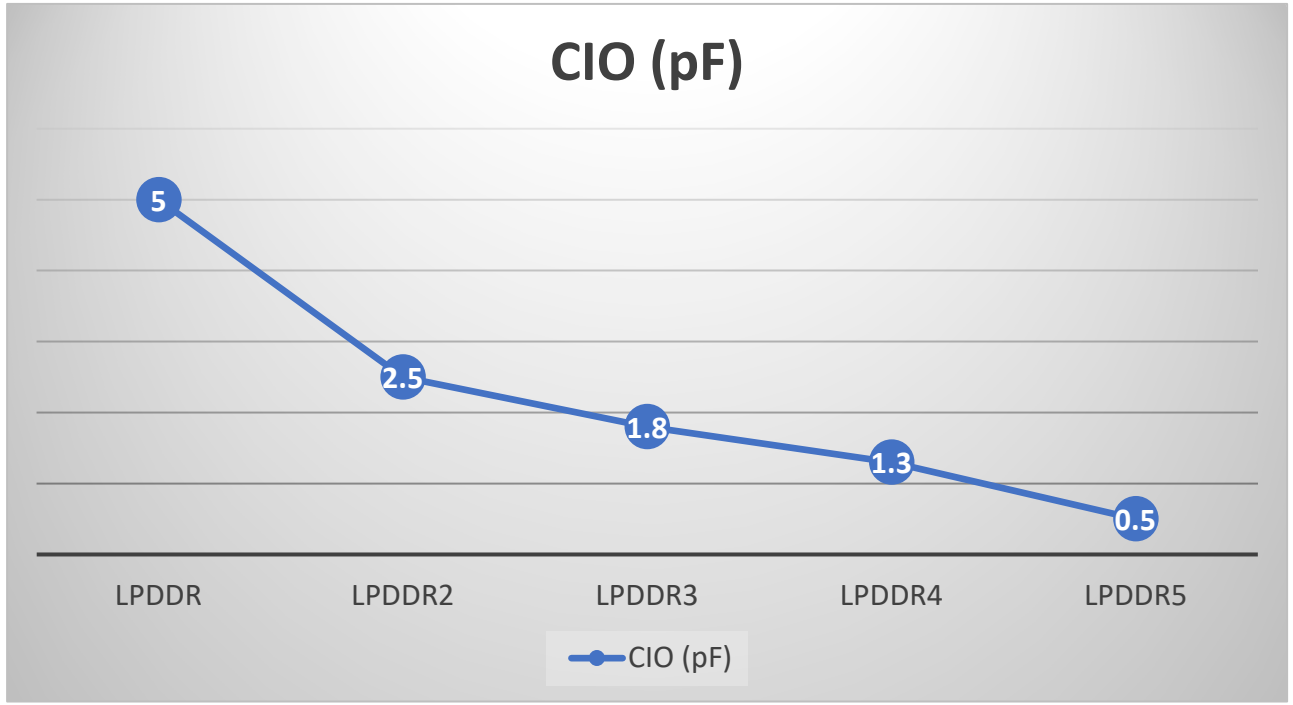


LPDDRx & DDRx IO Data Rate

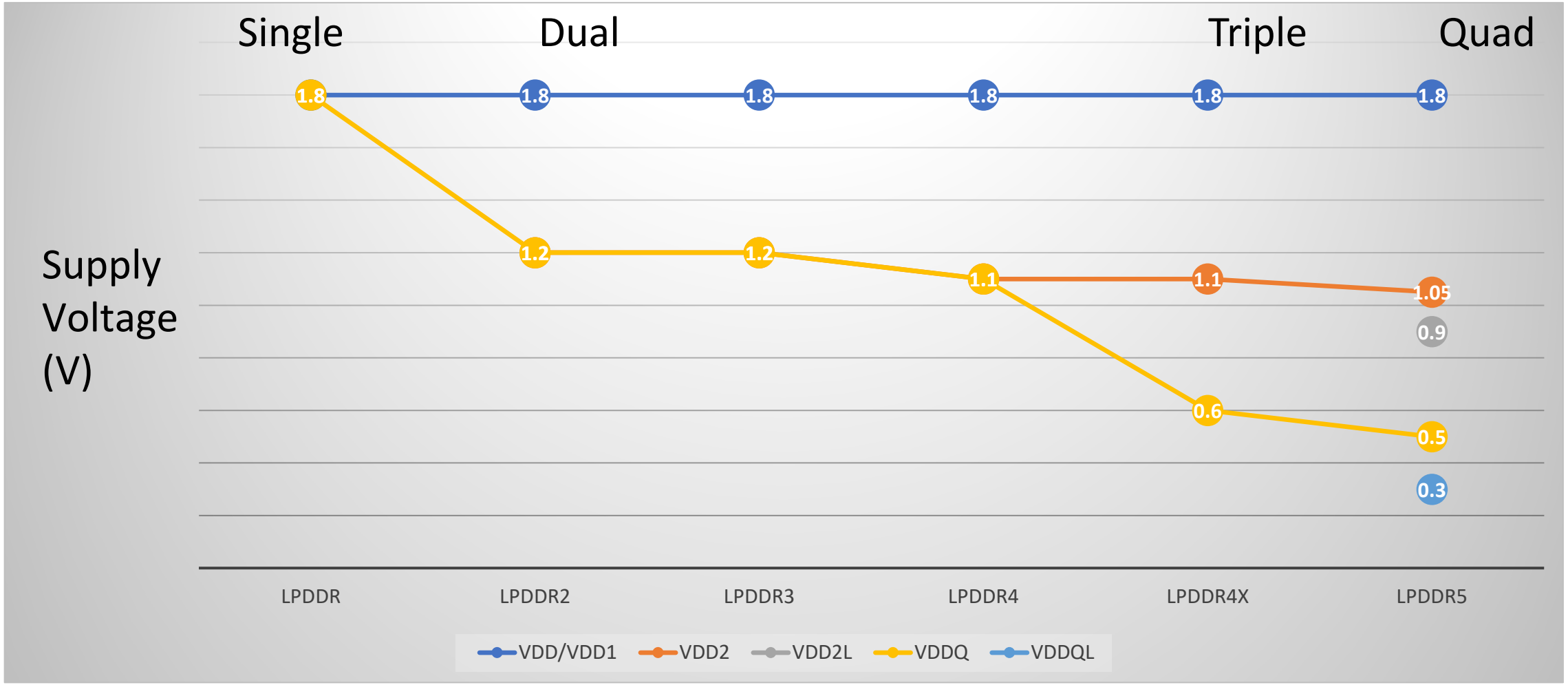


LPDDRx Channel Improvement

- CIO reduction
  - CIO is essential parameter for both eye opening and Channel power
  - Challenge is ESD & pin leakage
- Channel power considerations
  - Channel power consumption is reduced
    - Lower VDDQ
    - Channel load reduction
  - Large power consumption
    - Tx Pre-driver
      - Optimize Driver strength



LPDDRx - Supply Voltages

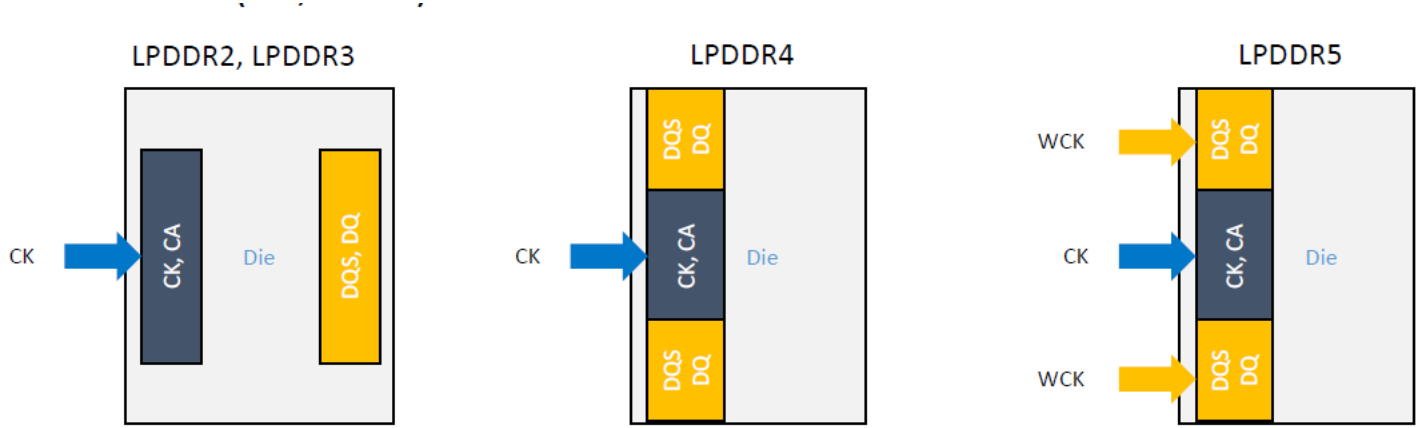


LPDDRx - Supply Voltages & DVFSC

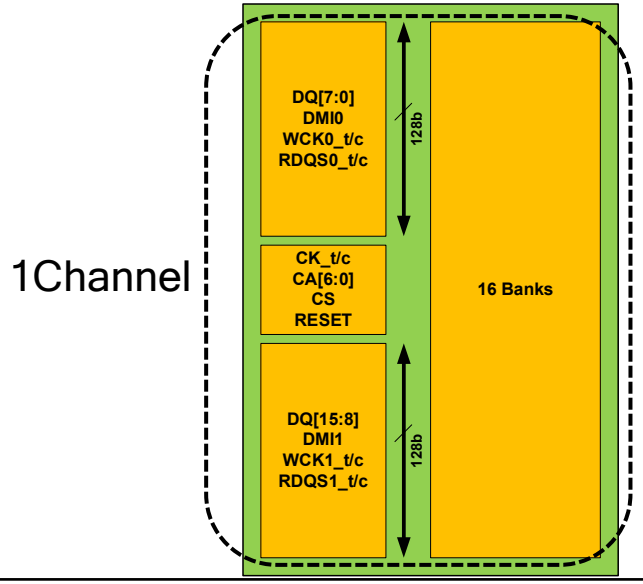
- DRAM power reduction by using lower power supply for low frequency operation
- Two DVFS schemes defined
  1. DVFSQ - Interface voltage (VDDQ/VDDQL)
     - Low voltage can be applied during un-terminated operation.
       - DRAM and SOC can use same receiver mask spec. LPDDR5 use VDDQ=0.5V and VDDQL=0.3V.
       - This help to reduce mobile system DOU power.
       - Even during VDDQ transition LPDDR system can continue to work with limited frequency operation.
  2. DVFSC - DRAM peripheral (VDD2L)
     - VDD1=1.8V and VDD2H=1.05V is essential for DRAM memory cell operation.
     - Adding power rail for peripheral circuits power reduction, VDD2L=1.05V/0.9V
       - Higher voltage supply for high-speed operation
       - Lower voltage supply for low-speed operation
       - Extending lower voltage supply region step by step

LPDDRx - Clocking Architecture Improvement

- LPDDR2/3/4 uses single clock
- To improve timing, LPDDR5 introduce forwarded clock, differential
- WCK operates at twice or quardruple the frequency of CMD/Address clock



LPDDR5/5x - Summary

	LPDDR5/5x
Die Diagram	
Max BW per Die	17GB/s (1Ch X16)
IO Speed	8533Mbps or higher (X16 NRZ)
Data Clock Freq	4266MHz or higher
CA Bus, Speed	CA[0:6], 2133MT/s (DDR)
Bank Architecture	1 Channel, 16Bank (4BG/4Banks)
Access Data Size, Page Size	32Byte per Ch, 2KByte
PDN	VDD1, VDD2H, VDD2L, VDDQ
Features	DVFSC, DVFSQ, SE Mode, RFM, Link ECC

LPDDRx, What's Next?!

LPDDR6 – High Level Goals

- Doubling of LPDDR5x bandwidth
- Improved low-power schemes
- Improved idd4 reduction
- One standard to comprehend all speeds and features
- Improvement of low-rank performance (e.g. more banks, better core params)
- Improved clocking architecture
- Evolutionary packaging technologies
- Improved Data Integrity
  - RFM solutions
  - On-die ECC, Link ECC, Link CRC

Reliability – Die

- On Die ECC
  - LPDDR are on-Die ECC capable spec is defined : Masked write command constraint is longer than others.
    - On-Die ECC scheme is vendor's specific
    - Because of limited resource, LPDDR doesn't have on-Die ECC transparency function.
  - Diversity of application requesting new reliability features
- Row Hammer mitigation
  - Row Hammer is one of hot topics in DRAM reliability
  - Trends of RH mitigation
    - DRAM internally manage RH mitigation implicitly
    - DRAM ask SOC to co-work mitigating RH by counting active CMD : RFM
      - Adding RH target level programmability. Adding SOC direct mitigation CMD : ARFM and DRFM
    - Under discussion on "SOC controlled RH mitigation"

Reliability – System

- Assumption
  - LPDDR PKG configuration is x32 or x64 DQ and multi rank capable.
  - This configuration is difficult to configure parity bit by system
- Link protection
  - High transfer rate interface may increase random communication error
  - LPDDR need to have feature of link protection
    - LPDDR5 has link ECC feature : SECDED link protection coding.
    - Parity bit is not stored in cell but create/check only communication
- System ECC better than in-line ECC
  - To configure system ECC using LPDDR, in-line ECC scheme is commonly used.
    - There are some issues on this scheme difficult to use all memory density on parity.
    - Degrade channel performance
- LPDDRx TG considering effective system ECC feature, and its impacts

LPDDR-NVM

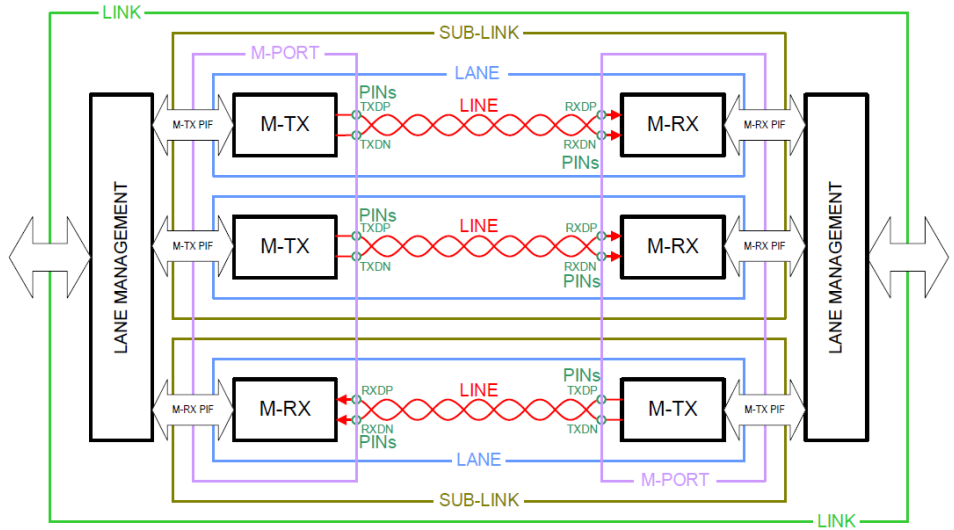
JEDEC LPDDR-NVM

- **<u>Current Automotive ecosystems</u> use-cases**
  - xSPI-NOR – is the default NVM in certain use cases due to its reliability, endurance, and PE cycle
    - READ performance limited to ~200MB/s
    - Mission critical, isolated use cases
- **Automotive memory requirements**
  - Data Reliability: data integrity, endurance, and PE cycles
  - Boot time improvement => Increase read Performance
- **LPDDR-NVM TG was created in Q4/2022. Opportunity to address boot time**
  - Executable memory (NOR) on LPDDRx bus. xSPI still available for write
  - LPDDR4x Read performance – min 800MT/s. *(lower latency, pipelined accesses)*
  - LPDDR4 interface flexibility *(single/dual channel, x8/x16, differential/single-ended)*
  - Adoption of standardized (LPDDR) bus transactions; but simplified for NVM
- **XiP architecture support. One interface for both LPDDR, XiP/NVM memory**
- **LPDDR-NVM participation are welcome**

UFS4.0

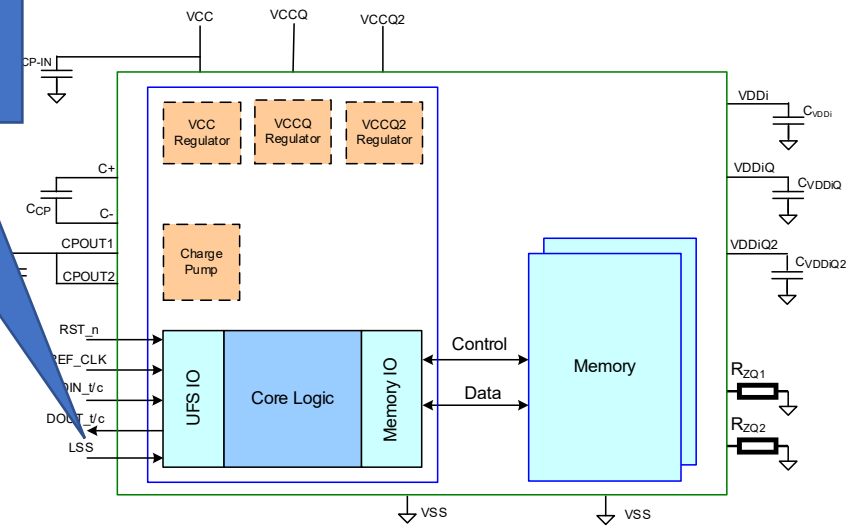
UFS 4.0: HighSpeed-Gear5

- MIPI M-PHY 5.0 and UniPro 2.0 deliver 23.32 Gbps per lane to satisfy the storage ecosystem's growing data rate requirements
- Data rates have been optimized for target applications, simplifying Phased Lock Loop (PLL) implementation and eliminating design complexity.
- High-speed startup reduces latency for earlier flash memory access on power up.
- Eye monitor - visualizes signal health, enhancing debug functionality.
- New attributes for equalization and other electrical updates to HS-G5 improve the suitability of M-PHY for ultra-high data rate applications.

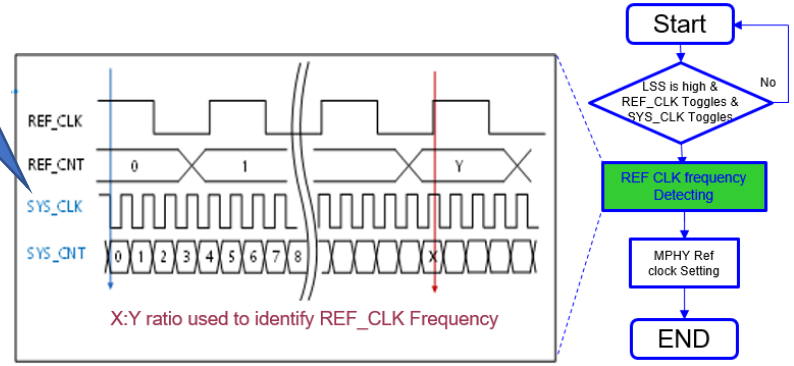


UFS4.0: HighSpeed LinkStartup

1. Signal on device to select startup mode



2. UFS device detects REF_CLK



3. SoC can be designed to configure UniPro and M-PHY Reset Mode

High-speed startup allows the interface to operate directly in Highspeed Gear1 instead of the default PWM mode

UFS4.0: Electrical Improvements

- VCC=2.5V only, 3.3V removed
- Higher REF_CLK frequencies for HS-G5 operations
  - 38.4Mhz & 52Mhz
- Improved Jitter and Noise definitions

Parameter	Symbol	Nominal		Unit	Notes
Frequency	f_{ref}	19.2, 26.0, 38.4, 52.0		MHz	1
Parameter	Symbol	Min	Max	Unit	Notes
Frequency Error	f_{ERROR}	-150	+150	ppm	
Input High Voltage	V_{IH}	0.65 * VCCQ		V	2
Input Low Voltage	V_{IL}		0.35 * VCCQ	V	2
Input Clock Rise Time	t_{IRISE}		2	ns	3
Input Clock Fall Time	t_{IFALL}		2	ns	3
Duty Cycle	t_{DC}	45	55	%	4
Random Jitter (f_{ref} = 19.2)	RJ_{RMS}		5.9	ps	5
Random Jitter (f_{ref} = 26.0)			4.6		
Random Jitter (f_{ref} = 38.4)			3.5		
Random Jitter (f_{ref} = 52.0)			2.8		
Deterministic Jitter	$DJ_{\delta\delta}$		15	ps	6
Input Impedance	RL_{RX}	100		kΩ	7
	CL_{RX}		5	pF	

NOTE 1 HS-BURST rates A and B are achieved with integer multipliers of f_{ref}.

NOTE 2 Figure 6.4 shows the input levels $V_{IL,MAX}$ to $V_{IH,MIN}$.

NOTE 3 Clock rise time and clock fall time shall be measured from 20% to 80% of the window defined by $V_{IL,MAX}$ to $V_{IH,MIN}$, see Figure 6.4.

NOTE 4 Clock duty cycle shall be measured at the crossings of the REF_CLK signal with the midpoint V_{MID}, defined as: $V_{MID} = (V_{IL,MAX} + V_{IH,MIN}) / 2$, see Figure 6.4.

NOTE 5 The RJRMS magnitudes are based on the phase noise parameters of previous versions of

this standard and replace them. RJRMS is computed with the integration range from 50 kHz to the

Nyquist frequency of the reference clock.

NOTE 6 Reference Clock frequencies of 19.2 MHz and 26.0 MHz cannot be used for HS-G5 and

above, because the corresponding RJRMS values are beyond the allowable limit for HS-G5

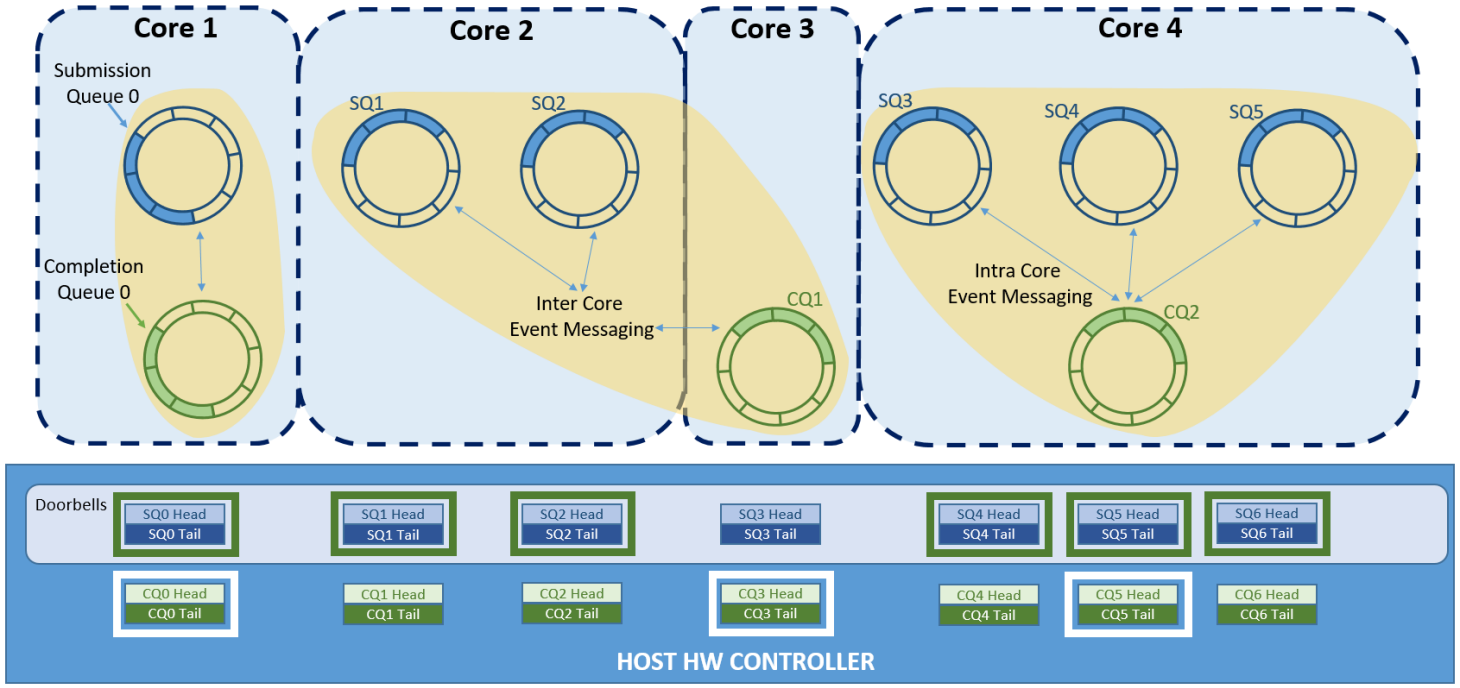
operation. The frequency of the reference clock shall be 38.4 MHz or 52.0 MHz for HS-G5 and above

operation.

NOTE 7 RL_{RX} and CL_{RX} include Rx package and Rx input impedance.

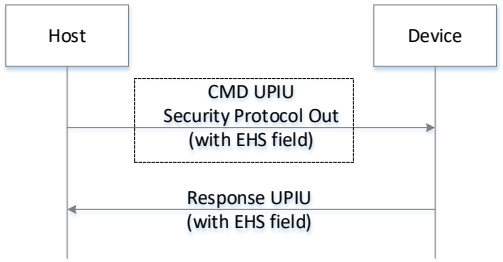
UFS4.0: Multi-Circular Queue

- Legacy mechanism: UTP Transfer Request List DoorBell Register (UTRLDBR)
  - Max 32 commands with contention between threads and cores
- New mechanism: MCQ
  - Max 32 queues each for submission and completion with host assignability



UFS4.0: Advanced RPMB, Improved Bandwidth

- Fewer messages, decrease per-operation latency
- Payload size: 4kB native vs. legacy 256B
- Built on SCSI's Extended Header Segments to simplify RPMB protocol



COMMAND UPIU

0	1	2	3
xx00 0001b	Flags	LUN	Task Tag

4		5	6	7	
IID	Command Set Type	Reserved	Reserved	EXT_IID	Reserved

8	9	10 (MSB)	11 (LSB)
Total EHS length (02h)	Reserved	Data Segment Length (0000h)	

12 (MSB)	13	14	15 (LSB)
Expected Data Transfer Length			

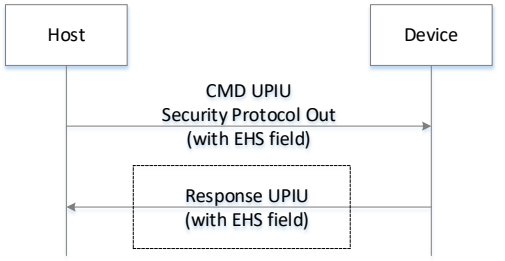
Bit / Byte	7	6	5	4	3	2	1	0
0	OPERATION CODE (B5h)							
1	SECURITY PROTOCOL							
2	SECURITY PROTOCOL SPECIFIC							
3	(Region Info)							
4	INC_512=0	Reserved						
5	Reserved							
6	(MSB)	TRANSFER LENGTH = 0						
9								(LSB)
10	Reserved							
11	CONTROL = 00h							

28	29	30	31
CDB[12]=00h	CDB[13]=00h	CDB[14]=00h	CDB[15]=00h

EHS field

0~3	EHS Header	
4~5	(Req./Resp. Message Type)	0001h
6~21	(Nonce)	0..00h
22~25	(Write Counter)	0...0h
26~27	(Address / LUN)	0000h
28~29	(Block Count)	0000h
30~31	(Result)	0000h
32~63	(MAC / Key)	Key

Header E2ECRC (omit if HD=0)



RESPONSE UPIU

0	1	2	3
xx10 0001b	Flags	LUN	Task Tag

4		5		6	7
IID	Command Set Type	EXT_IID	Reserved	Response	Status

8	9	10 (MSB)	11 (LSB)
Total EHS length (2)	Device Information	Data Segment Length	

12 (MSB)	13	14	15 (LSB)
Residual Transfer Count			

16	17	18	19
Reserved			

20	21	22	23
Reserved			

24	25	26	27
Reserved			

28	29	30	31
Reserved			

EHS field(2)

0~3	EHS Header	
4~5	(Req./Resp. Message Type)	0100h
6~21	(Nonce)	0..00h
22~25	(Write Counter)	0..00h
26~27	(Address / LUN)	0000h
28~29	(Block Count)	0000h
30~31	(Result)	Result Code
32~63	(MAC / Key)	0...00h

Header E2ECRC (omit if HD=0)

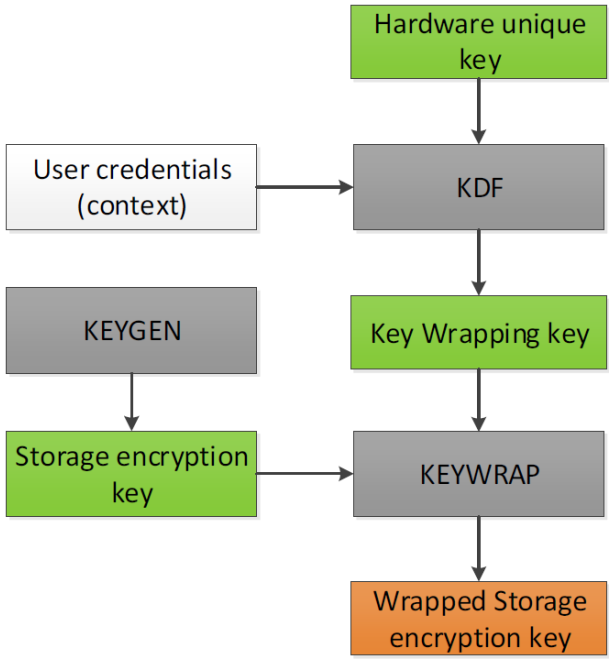
K (MSB)	K+1 (LSB)	K+2	K+3
Sense Data Length		Sense Data[0]	Sense Data[1]
...	...	...	...
K+16	K+17	K+18	K+19
Sense Data[14]	Sense Data[15]	Sense Data[16]	Sense Data[17]

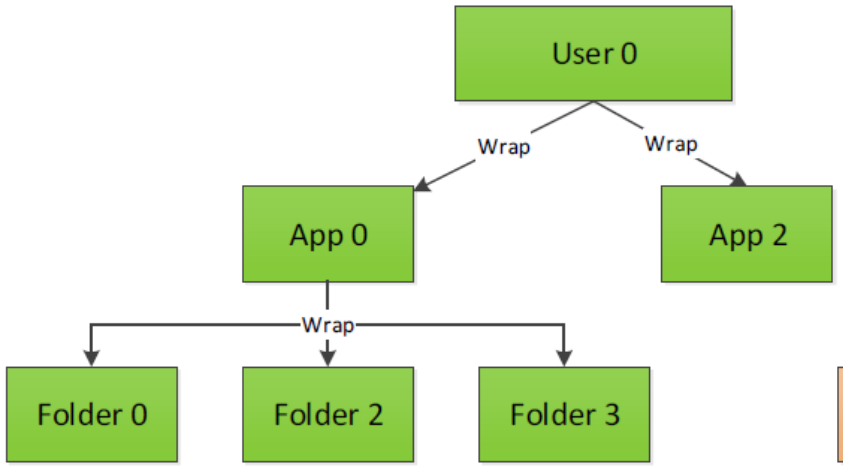
Data E2ECRC (omit if DD=0)

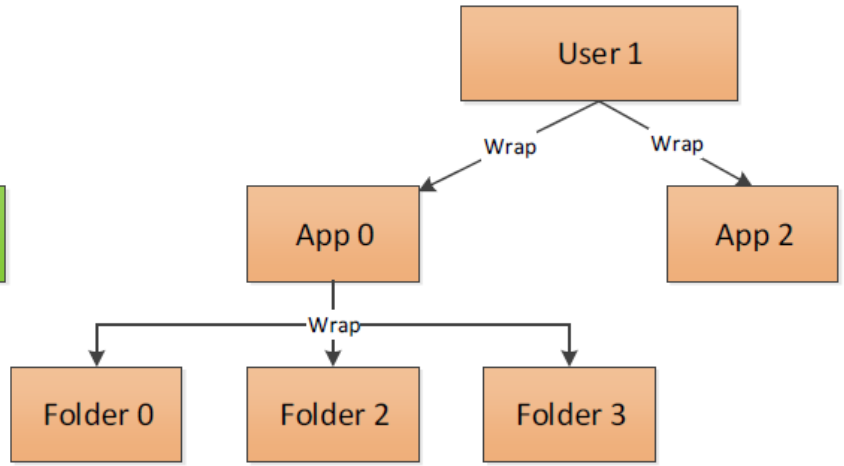
Note 1 K=32 if HD=0 and EHS field is not included
K=96 if HD=0 and EHS field is included
Note 2 EHS field shall not be sent when SPI/SPO command terminated with CHECK CONDITION status. In this case, the Total EHS length is 0h.

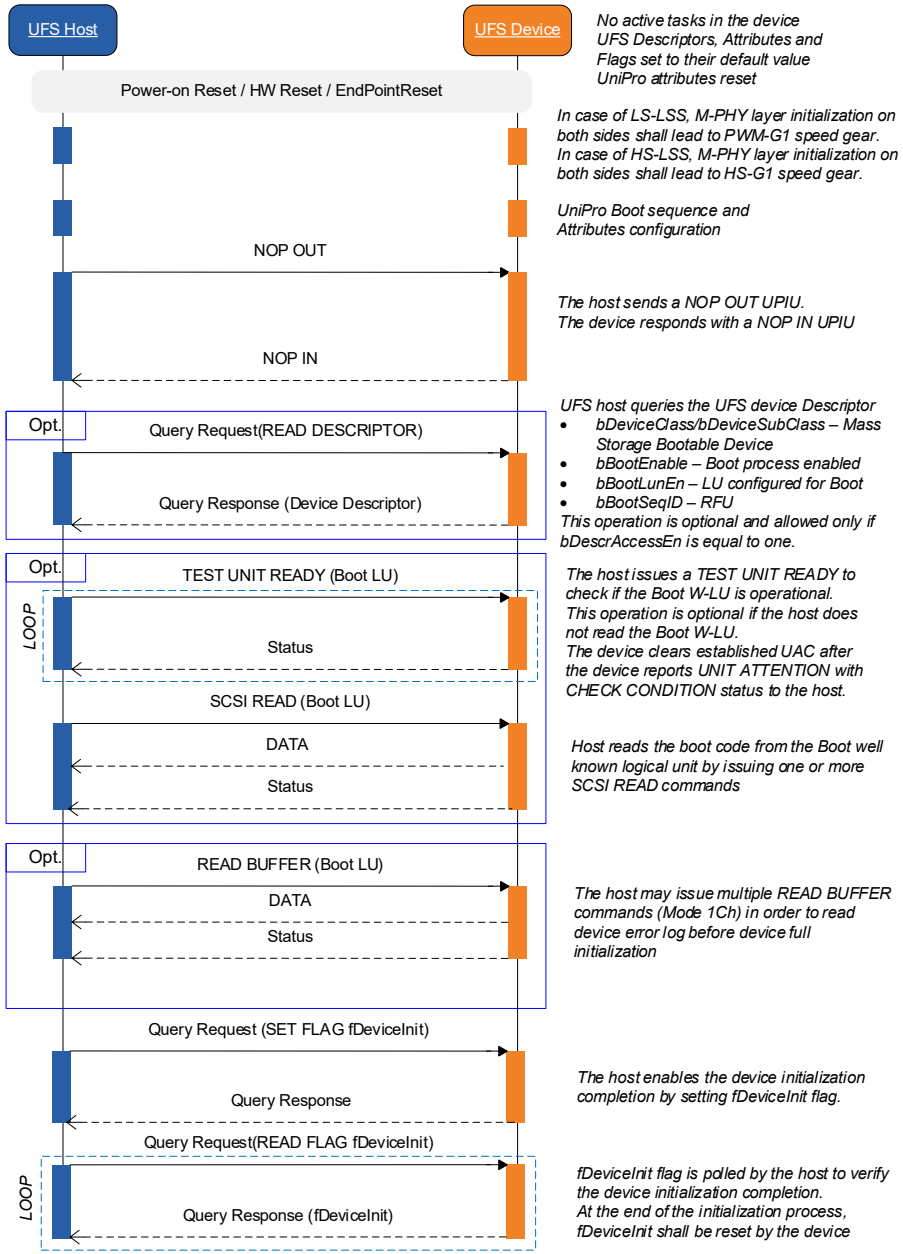
UFS4.0: RPMB Purge

- Removal of overwritten RPMB data for high-security applications
- Enables cryptographic erase by erasing keys securely (NIST SP 800-88)
- Makes use of Android and other OS encryption capability









UFS4.0: Boot-time Error Log Access and Timestamps

- Early debug ability enables easy integration
- A READ BUFFER command can retrieve the Device Error Log, as soon as BOOT phase
- Hosts may configure qTimestamp to synchronize Device and Host time

Next-Gen UFS

- UFS4.1 & addendums – Minor revision, targeting SW or FW updates
  - Zoned Storage, as an addendum
  - Improvement to WriteBooster
  - Improvement to UFSHCI
    - Update to Completion Queue to include EXT_IID, IID, LUN, and TaskTag. Minimize SW overhead
  - Host Initiated Defragmentation
  - SoC Buffer. Buffer defined for SoC use at power-up
  - Additional notifications for other device exceptions
  - Introduce new, smaller packaging - 9x13mm
  - Minor editorial updates
- UFS5.0 targets
  - Double the data rate. Targeting new MIPI M-PHY Gear6 & Unipro3.0
  - Address new requirement from markets like automotive, AI, XR, etc.
  - Challenges – power, new signaling, encoding, BER, data reliability, etc.

UFS Performance Trend