DTTC 2024

Enabling IDM 2.0 and AI through product development engineering leadership

DTTC 2024 Schedule

3 Virtual Days: July 15-17, 2024

72 Presented Papers | 12 Invited Technical Talks

Keynotes | Meet the Fellows | Birds of a Feather

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Day 1: Monday, July 15, 2024

Time (PST, AM)	Design	Validation	Systems	Test	Software	Design
7:05-8:00	Keynote: Pat Gelsinger					
8:05-8:10	Paper Presentation Intro (5 Min)					
Invited Talks 8:10-8:45	System level approach to next generation data center architectures	Quality Bots and leveraging QIRI-LLM Gen AI to enhance analytics	Scaling Gaudi 2 & Gaudi 3 designs	Embracing IDM2.0: A Mindset shift to Affordable Innovation & Accountability for Scale	Bringing AI to the Web Platform	What's Next in Computing. GPU / CPU Accelerators...
Paper Presentations 8:45-10:00	A 0.9pJ/b 100-128Gb/s DAC based transmitter in Intel 18A technology	Trinity: Automatic Test Stimulus Generation Integrating Real-World Software	Enhancing Memory Error Mitigation: AI-Driven RAS Action Optimization in BMC	Intel Cold Transformation - a Mindset Change for IDM 2.0	Efficient LLM Inference on CPUs	MaRS: Machine-Readable Specification in IP Architecture, Design and Validation and its Application to DMR and Beyond
	Intel-4 standard design rule BCAM cell high Vmin post-Si learnings	Shift-Left IPSD Development via Co-Validation in Pre-Silicon RTL Model	Sub-channel Re-grouping for Package Optimization for DDR5 Memory for RDIMM/MRDIMM	Breakthrough stress strategy in DieSort: HOT HVQK Single Stress Location	Coral Fast: A Breakthrough Abstraction Technique for Speeding Up Pre-Silicon Software Performance Tuning	Spec Generator: Parallel SoC Assembly Tool
	Enhanced SRAM Power Analysis: Methodologies and Insights for improved Design Efficiency	Regression Data Slicer - a Leap Towards Efficient Regressions	Magnetic Inductor Solutions for FIVR - Achieving 92.8% peak efficiency for 1.75 V to 0.75 V Conversion	CTT Power Modeling and Flat Power Technology	Making PyTorch Eager Mode Performant on Intel Gaudi2	Reconfigurable FP8/FP16 Floating-Point Fused Dot-Product
10:15-10:20	Paper Presentation Intro (5 Min)					
	Design	Validation	Systems	Test	Software	Validation
Paper Presentations 10:20-11:35	AI-Assisted Defect-Aware Timing-Yield Optimization of IP Blocks	Newtonian and MaRS in Automating Validation	Proactive ICCmax Management: A Deterministic Approach to Optimal Power Delivery in Open Ecosystem Chiplet-Based Server SoCs	HVM per-part Vpower-grid Methodology Enhancement and Power Performance Optimization with the new Adaptive Clock Modulation (ACM)...	Studying Games using SPLIT - Simics Pass-through Long Instruction Trace	Architecting Early Boot Debug provisions for Granite Rapids-D
	Multi-objective Optimization of FIVR Compensator using Evolutionary Algorithms	Artificial Intelligence Solution in Power Performance Validation and Development	Revolutionary Power-Signal Co-design to Enable Higher TDP on Xeon Platforms	Scan ATPG Learnings from Meteor Lake SoC	Kairos - Advancing Analysis, Projection and Pathfinding Capabilities for AI and HPC Applications	Persistent Fuse Override journey to transition from SPR PoC to an official POR Xeon's DMR SoC CPU feature
	Synthesized Array Power Optimization	Fusion-Compiler and PhysRTL-Gen Based Mapping Flow for Power Estimation in Atom CPU	Soft processors Applications in Validation Platforms - Hardware/Software Co-Design Advantages	Navigating Scan Extest Journey: Insights and Lessons from Intel4	Optimizing Transformer Networks for execution on Intel NPU	Valhalla: Fine-tuned Large Language Model (LLM) based tool for validation test generation and execution
11:35-11:40	Wrap and Closing Remarks (5 min) End 11:40					

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Day 2: Tuesday, July 16, 2024

Time (PST, AM)	Design	Validation	Systems	Test	Software	Security
7:05-8:00	Keynote: Michelle Johnston Holthaus & Justin Hotard					
8:05-8:10	Paper Presentation Intro (5 Min)					
Invited Talks 8:10-8:45	AI tools for design	Reimagining Validation beyond Si	Aurora: The Exascale SuperComputer	Envisioning Tomorrow: Convergence of AI and Human Ingenuity for Smart Product Dev.	Client AI Usages, Strategy and Roadmap	Architectual Innovations for Confidential AI and AI for Security
Paper Presentations 8:45 - 10:00	SAAF: Streamlined Access Approval Flow -- Methodology and Application to Support End to End IP Security	Scalable active visual perception for automation of memory matrix validation tasks via synthetic data generation	Two-Phase Jet Impingement Liquid Cooling: Experimental evaluation using the Sahara Active Thermal Test Chip	QIRI Gen AI, FERRET-QBots powered Manufacturing Data Analytics	UHGM: Unified Device Manager for Heterogeneous GPUs	Carystus: Secure & High-Performance RISC-V Core
	Streamlining Die Ring Creation and Integration with Dragon and AboveFC Utilities	The Role and Impact of Python UEFI in Silicon, Firmware and Platform Validation across Intel and Tech Industry	3D Heat Pipe Solution for DIMM Liquid Cooling	Concurrent Test Scheduling and Assistive Technologies	AIPP: AI Power Predictor for Single DUT for Digital Regression Efficiency	Ultimate Memory Safety by Fusing Cryptography with Tag Checking
	Enabling a High-Quality, Industry 1st, PowerVia Auto Place and Route TFM on ArrowLake-P	Speech Platform Evaluation Toolset (SPET) a comprehensive audio quality evaluation framework forIntel Evo certification	SuperCoverage: AI-Guided Full Coverage of Thermal and Power Analysis for SoC Design	Innovative HVM MRC in DDR PHY: A Game-Changer for Faster time to market	Boosting Productivity and Quality: Modernization of SHC Toolkit for Enhancing Outgoing SDE detection on Xeon Fleet	TM-AI, an Artificial Intelligence assistant for generating Threat Modeling mitigation strategy.
10:15-10:20	Paper Presentation Intro (5 Min)					
	Design	Validation	Design	Test	Software	Validation
Paper Presentations 10:20-11:35	Pre-Si Vmin Optimization Workflow Paving Way for Improving Product Performance per Watt	MOSAIC: A Fully Automated Tool for Platform Security Research	From Client to Server - Two Layer Coherent Fabric	Sapphire Rapids: Tribulations and Resolutions for Bin99/"Mousebite" Issues	CPU Microarchitectural Performance Analysis of SVT-AV1 Encoder	ProtoFlex: Integrated RISC-V Pre-Silicon Suite
	Innovations to Mitigate Late discovery of Layout Dependent Effects in Project Execution	The Crucial Role of Power Delivery in Unraveling Systemic High-Speed IO Errors	Disaggregation Architecture Modeling for Optimized New Product Design (DiAMOND)	Improvements to MBIST Solution with Advanced Algorithms and Test Coverage for Advanced Memories	Enhancing End-User Experience through Telemetry: Development and Impact of Intel Platform Analytics	Root Cause Analysis Method and Tools for KPI-based Performance Validation with SoC RTL Emulator
	Co-Optimizing Base-Die and Top-Die IR/RV Convergence using 3DIC methodology for CWF	PCI Express Equalizers Optimization by Machine Learning Techniques in Post-silicon Validation	Pushing the System Performance Boundary: Achieving Memory Speed Overclocking on Non-OC SoC SKU	Design and Validation of a Diamond-Based Thermal Solution for Singulated Die Sort/Test	Improving Server Projections: Using Machine-Learned Memory Models to Improve Performance Validation During Pre-Si Design	Pioneering Software Formal Verification Methodology on Intel Primecode Firmware
11:35-11:40	Wrap and Closing Remarks (5 min) End 11:40					

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Day 3: Wednesday, July 17, 2024

Time (PST, AM)	Design	Validation	Systems	Test	Software	Security
7:05-8:00	Keynote: Navid Shahriari					
Birds of a Feather Sessions 8:05-9:45	Inter-Chiplets Synchronous Clocking – Challenges and Solutions	Strategy to accomplish Windows OS boots in Pre-silicon for x86 cores validation	Enabling Hot-Swappable NVMe Storage in Client Products	The Future of Test Interconnects in IDM 2.0	HW/BIOS co-validation: Effectively validate product configurations in HW and FW pre-silicon validation environments	Strengthening the Foundation through Architectural Security Hardening
10:00-11:30	Meet the Fellows					
11:30-11:40	Wrap and Closing Remarks (10 min)					

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