

[Technical Paper]

# Investigation on Microstructure and Resistivity in Cu-TSVs for 3D Packaging

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## Abstract

The resistivity of Cu-TSVs (through silicon vias) substantially affects the performance of system LSIs. Hence, it is very important to evaluate the resistivity of Cu-TSV precisely.

Researchers and engineers have been concerned about the possibility that many impurities from additives and plating solutions were incorporated into Cu-TSV during plating and these impurities would precipitate along the grain boundaries, leading to great variation in grain sizes from tens of nm to several  $\mu\text{m}$ , resulting in a resistivity increase after annealing. However, the precise resistivity has not always been published. In order to obtain accurate resistivity, we have developed a new TEG (test element group) pattern and its manufacturing process. Using TEGs, we obtained  $4.13 \times 10^{-8} \Omega\cdot\text{m}$  as the resistivity of one Cu-TSV. We discussed the mechanism for the high-resistivity of Cu-TSV based on measurements of grain size scattering using X-ray diffraction, EBSD (electron back scatter diffraction) and Cs-corrected STEM (scanning transmission electron microscope) observation.

**Keywords:** Cu-TSV, Resistivity, Microstructure, Cu Electroplating, Three-dimensional Packaging

## 1. Introduction

LSI (large scale integration) has undergone evolution through research and development toward miniaturization and higher integration densities, but it is foreseeable that the miniaturization of LSI circuits will shortly hit a physical limit. As a consequence, “More than Moore,” which is based on diversification methodology not dependent on Moore’s Law, has been drawing attention in recent years. In addition, Okamoto[1] reviewed studies that have been carried out on evolution toward higher integration densities in three-dimensional terms that is not dependent on miniaturization but that is based on “More than Moore” for several reasons, including that the miniaturization of LSI circuits requires enormous capital investment. One example of evolution toward higher integration densities that has been studied is three-dimensional packaging that uses copper through silicon vias (hereinafter referred to as Cu-TSVs).[2–4]

Recently, three-dimensional packaging that uses Cu-TSV technology has been applied to electronic parts for use in

portable terminal devices (e.g., smartphones) and other similar devices. These electronic parts are required to accommodate processing of a large volume of information and to provide high-speed data transmission. To meet these requirements, the wiring resistivity attributable to Cu-TSVs must be reduced. However, only a few reports on Cu-TSV resistivity have been made,[5, 6] and it has been difficult to perform high-accuracy measurements on Cu-TSVs alone. For example, the measured resistivity using a daisy chain pattern includes interconnect resistivity which ties up with Cu-TSVs,[5–7] and bump resistivity is also included in the measured resistivity for single and double-layer patterns.[8] Furthermore, it is impossible to remove resistivity due to bypass current from the measured resistivity in the case of resistivity measurement using Kelvin patterns.[9] Several reports on Cu-TSV resistance measurements have been made to date. However, none of the reported resistance values are those of Cu-TSVs alone; all the reported resistance values include resistance attributable to devices around Cu-TSVs (e.g., wiring resistance,

bump resistance). In other words, it has been difficult to determine a resistance value attributable to Cu-TSVs alone.

To deal with this challenge, we independently developed a new TEG (test element group) for resistivity evaluation and measured Cu-TSV resistivity using the TEG. Moreover, we analyzed the microstructure inside the Cu-TSVs using STEM and EBSD, thereby clarifying the relationship between the resistivity and microstructure of the Cu-TSVs.

## 2. Experimental Method

### 2.1 Method of sample formation

Samples for electric resistance measurements were made using an 8-inch wafer. Figure 1 shows a process flow of sample fabrication. First, via holes were formed in a Si wafer by dry etching using the Bosch process. The depth of the formed via holes was set to  $110\ \mu\text{m}$  given that their diameter was  $10\ \mu\text{m}$ . Next, a  $500\ \text{nm}$  TEOS (tetraethyl orthosilicate) oxide film was formed by CVD (chemical vapor deposition), and then a  $200\ \text{nm}$  Ti barrier film and an  $800\ \text{nm}$  Cu seed film were sequentially formed by sputtering (Fig. 1 (a)). Subsequently, a  $10\ \mu\text{m}$  Cu electroplating film was formed using the high-speed fluid flowing method,[10, 11] and heat treatment with a  $\text{H}_2$  atmosphere was done at  $250^\circ\text{C}$  for 30 min to accelerate crystal growth (Fig. 1 (b)). The conditions for the aforementioned Cu electroplating were set as follows: electroplating method, pulse electrolysis (ON, 350 ms; OFF, 350 ms); current density,  $5\ \text{mA}/\text{cm}^2$ ; plating solution flow speed,  $5.0\ \text{m/s}$ . The Cu plating solution and additives used for sample formation were commercially available products.

Next, CMP (chemical mechanical polishing) was carried out for the Cu electroplating film and Ti barrier film

formed on the wafer surface to remove the Cu and Ti films (Fig. 1 (c)). Subsequently, a  $50\ \text{nm}$  Ti barrier film and a  $1.0\ \mu\text{m}$  Al-0.5 wt%Cu film were formed, and then Al pads were formed through photoresist and Al-0.5 wt%Cu/Ti dry etching processes (Fig. 1 (d)). The final step involved fabricating the back-side electrode as follows. The Si wafer back surface was ground so that the Cu-TSVs bottom surfaces were exposed; the thickness of residual Si was  $80\ \mu\text{m}$ . Then, the sputtering method was used to get a  $50\ \text{nm}$  Ti barrier film and a  $200\ \text{nm}$  Au film to serve as the back-side electrode (Fig. 1(e)). In this way, samples were fabricated to allow conduction between Al pads on the wafer surface.

Figure 2 shows the appearance of the TEG chip embedded in the samples that had been made by the process of Fig.1. The chip was  $20\ \text{mm} \times 20\ \text{mm}$  and the Cu-TSVs had three different diameters ( $5$ ,  $10$  and  $20\ \mu\text{m}$ ) and a depth of  $80\ \mu\text{m}$ . Cu-TSVs were formed right under each Al pad such that any number of Cu-TSVs within the 1–100 range could be selected at the time of resistance measurements. In addition, the inter-Al pad distance was varied from  $360$  to  $2,160\ \mu\text{m}$  to allow resistance measurements to be made with different distances.

### 2.2 Measurement method of Cu-TSV resistivity

The Cu-TSV resistivity was measured using the four-point probe method. Figure 3 shows a schematic conceptual diagram of how to measure the resistance of Cu-TSVs using our new TEG. Figure 3 (a) shows the new TEG cross section and Fig. 3 (b) shows circuit diagrams of Fig. 3 (a). In this research, the number of Cu-TSV is fixed as 81. The procedure for the Cu-TSV resistance measurements was as follows. First, the resistance of the Cu-TSVs was measured between Al pad 0 and Al pad 1 through I-V measurements. The resistance obtained is the summation of  $R_a$  of the Cu-TSVs right below Al pad 0,  $R_{b1}$  right below

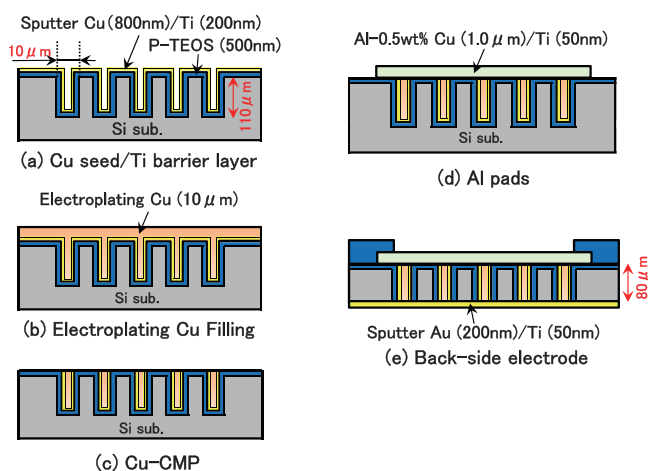


Fig. 1 Schematic diagram of the fabrication process of the sample.

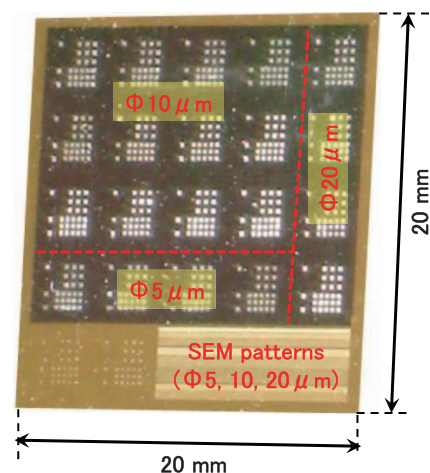


Fig. 2 Appearance of a TEG (test element group) chip.

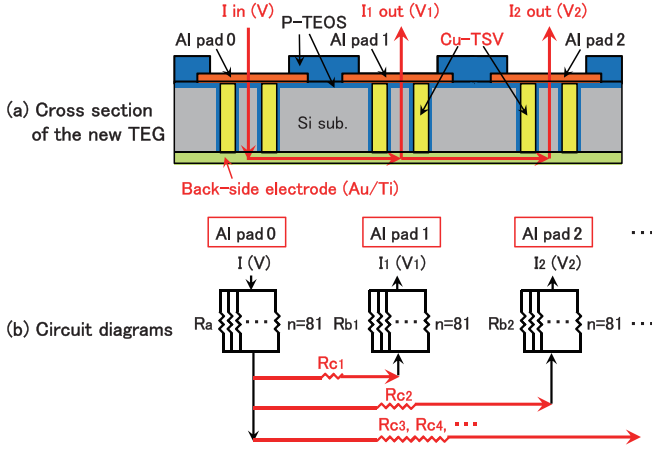


Fig. 3 Conceptual schematic diagrams of how to measure the resistance of Cu-TSVs using the new TEG.

Al pad 1, and  $R_{c1}$  of the back-side electrode. Then, I-V measurements are also made between Al pad 0 and Al pad 2. The measured resistance in this case is the total value of  $R_a$ ,  $R_{b2}$ , and  $R_{c2}$  of the back-side electrode. Here,  $R_a$  equal  $R_{b1}$ , because their total number of Cu-TSVs is 81. Hence, the resistance difference between Al pad 0 and Al pad 1, and Al pad 0 and Al pad 2 should be attributed to the difference between back-side metal resistances  $R_{c1}$  and  $R_{c2}$ . In a similar way, the total resistance between Al pad 0 and Al pad 3 also reflects the resistance difference between back-side electrodes  $R_{c1}$  and  $R_{c3}$ . Hence it follows that the resistance difference due to the difference of the back-side metal length can be got by measuring the resistance of the different pad distances. If we plot measured resistance as a function of distance between Al pads, we can calculate resistance of the Cu-TSVs when extrapolating Al pad distance to 0. This means that a Cu-TSV resistance value exclusive of the resistance attributable to the back-side electrode (Au/Ti) can be derived.

In addition, the resistance value attributable to the Al pads, based on calculation, is less than 0.2% of the resistance value per Cu-TSV, and it would therefore be negligible. Further, resistance of Al pad (Al/Ti) derived  $0.832 \mu\Omega$  from the size in Al pad and each film thickness by approximation (1).

$$\begin{aligned} R_{\text{Al pad}} &= R_{\text{Al}} + R_{\text{Ti}} \\ &= (2.65 \times 10^4 \mu\Omega \cdot \mu\text{m} \times (1.0/(240)^2 \mu\text{m}^{-1})) \\ &\quad + (4.27 \times 10^5 \mu\Omega \cdot \mu\text{m} \times (0.05/(240)^2 \mu\text{m}^{-1})) \end{aligned} \quad (1)$$

Hence, the Cu-TSV resistance value exclusive of the resistance attributable to the Al pads and back-side electrode (Au/Ti) can be derived. With respect to this Cu-TSV resistance value, we can calculate Cu-TSV resistivity from

the number and dimensions (diameter and depth) of the TSVs.

### 2.3 Evaluation method

Measurements of resistance values were taken per inter-Al pad distance using the four-point probe method. In addition, evaluations of the microstructure inside the Cu-TSVs were performed as follows. A three-dimensional evaluation of voids inside the TSVs was done using high-resolution, three-dimensional X-ray CT images obtained with the TDM1000H-Su (Yamato Scientific Co., Ltd.), and evaluations of Cu crystal orientation and grain size were done by EBSD. Moreover, the distribution of fine crystal grain sizes of not more than 200 nm was evaluated using XRD (X-ray diffraction), as reported in the literature.

To evaluate the ability to embed Cu in TSVs, we carried out the following observations. First, cross-sectional observations were made with a STEM (model HD-2700, Hitachi High-Technologies). Then EDX (energy dispersive X-ray spectroscopy) was used in combination with an Octane T Ultra W 100 mm<sup>2</sup> SDD (silicon drift detector; AMETEK, Inc.) to observe the areas within the cross section that indicated flaws in order to determine precipitate composition.

## 3. Results and Discussion

### 3.1 Cu-TSV resistivity

We devised a resistance measurement method and a measurement pattern with the objective of taking more accurate measurements of Cu-TSV resistance, then we performed Cu-TSV resistance measurements in a rigorous manner and calculated Cu-TSV resistivity.

The prototyped 8-inch wafer was divided into chips, as shown in Fig. 2, to measure Cu-TSV resistance, as shown in Fig. 3. Figure 4 shows the results of three Cu-TSV resistance measurements that we made using different inter-Al pad distances, i.e., 360, 1,080 and 2,160  $\mu\text{m}$ . The TSVs of the resistance measurement pattern were 10  $\mu\text{m}$  in diameter and 80  $\mu\text{m}$  in depth. TSVs were formed right under the Al pads so that any number of TSVs within the 1 to 100 range could be selected. The evaluation presented in Fig. 4 used 81 TSVs. Approximation (1) was derived from these measurement results:

$$Y = 23.236X + 0.485 \quad (2)$$

where Y represents Cu-TSV resistance ( $\Omega$ ) and X represents inter-Al pad distance ( $\mu\text{m}$ ).

From approximation (2), we calculated a value of 0.485  $\Omega$  as the Cu-TSV resistance assuming the inter-Al pad dis-

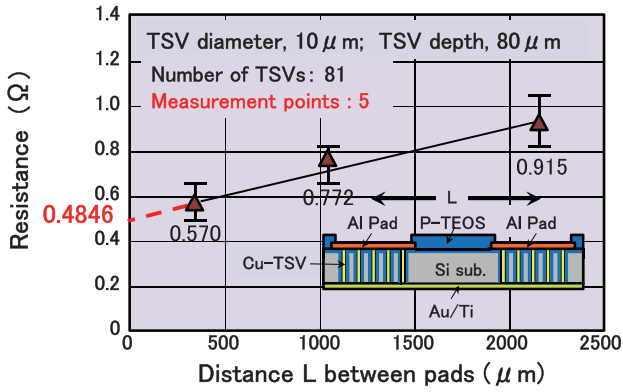


Fig. 4 Total resistance of Cu-TSV as a function of distance between pads.

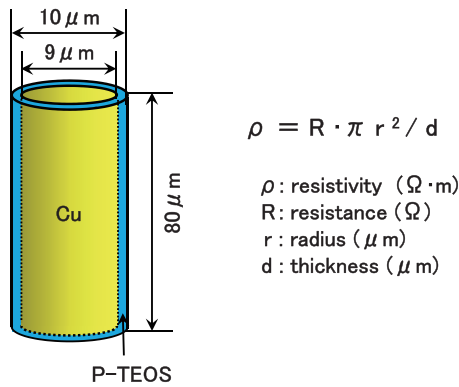


Fig. 5 Schematic illustration of Cu-TSV and calculation formula of Cu resistivity of a TSV.

tance was zero ( $X = 0$ ). In addition, a value of  $0.570 \Omega$  was calculated as the Cu-TSV resistance assuming the inter-Al pad distance was  $360 \mu\text{m}$ . From these results, a value of  $0.0854 \Omega$  was calculated as the Cu-TSV resistance exclusive of the resistance attributable to the back-side electrode (Au/Ti). Because the number of TSVs right under each Al pad was 81 and the pattern where two sets of 81 parallel Cu-TSVs were arranged in series was adopted, we calculated a value of  $5.27 \times 10^{-4} \Omega$  as resistance per Cu-TSV.

The calculated Cu-TSV resistance value was then substituted into the formula shown in Fig. 5, and the Cu-TSV resistivity of  $4.13 \times 10^{-8} \Omega\cdot\text{m}$  was calculated. **Further, this Cu-TSV resistivity was calculated from the design value of the new TEG.** This resistivity was approximately 2.47 times higher than the Cu bulk resistivity ( $1.67 \times 10^{-8} \Omega\cdot\text{m}$ ). In order to identify contributors to this high resistivity, we examined the crystallinity of the Cu-TSVs next.

### 3.2 Crystallinity of the Cu-TSVs

As the Cu-TSV resistivity calculated in Sec. 3.1 (i.e.,  $4.13 \times 10^{-8} \Omega\cdot\text{m}$ ) was higher than the Cu bulk resistivity as well as the LSI wiring resistance,[12–14] we evaluated the crystallinity of the Cu-TSVs to identify contributors to get

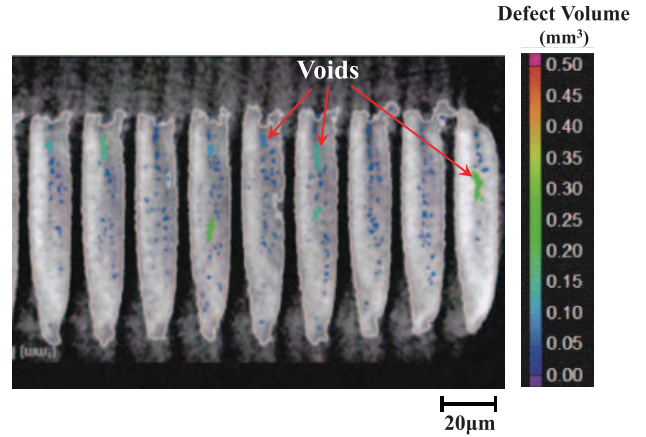


Fig. 6 Three-dimensional images of Cu-TSVs obtained by X-ray computed tomography scan (Diameter of Cu-TSV,  $10 \mu\text{m}$ ; Depth of Cu-TSV,  $80 \mu\text{m}$ ).

such a high Cu-TSV resistivity. The evaluation results are described in the following subsections.

#### 3.2.1 Evaluation of voids inside the Cu-TSVs

With the aim of identifying contributors to the high Cu-TSV resistivity, we evaluated the Cu-TSVs using high-resolution, three-dimensional X-ray CT images. As illustrated in Fig. 6, voids were irregularly located inside the Cu-TSVs. Many of the voids detected in each TSV were located in the region from the center to the top of the TSV. However, the void ratio was only 1.92 %, and this fact suggested that the possibility of these voids having contributed to the high resistivity was low.

#### 3.2.2 Crystallinity of the Cu-TSVs

Figure 7 shows the inverse pole figure pattern of a Cu-TSV obtained by EBSD. We confirmed that many Cu crystal grains with a diameter of  $2 \mu\text{m}$  or more and many fine Cu crystal grains were present together. These results are consistent with those reported by Kadota, *et al.*[15, 16] In addition, the distribution of Cu crystal grain sizes derived from these measurement results is shown in Fig. 8. We found that approximately 40% of Cu crystal grains had a diameter less than about 170 nm, as the figure indicates. This means that EBSD cannot clarify grain distributions when the diameters are less than 170 nm. Hence, we used XRD analysis for a detailed evaluation of these small Cu-TSV crystal grain sizes based on the report fact that XRD is a highly accurate measurement method for grain sizes less than 100 nm.[17] Figure 9 plots results that were obtained, indicating that the average crystal grain size of the Cu-TSVs was 65 nm, as well as that 27% of the Cu crystal grains had a diameter of 50 nm or less while 13% had a diameter of 40 nm or less. As the size of these fine crystal grains was approximately the same as the mean free path



(39 nm), electron scattering was considered to be one of the contributors to the high Cu-TSV resistivity.

In addition, we could explain the contributor to the Cu crystal grain size reductions as follows. Because the flow speed of the plating solution used to form the electroplating film was set as high as 5.0 m/s, the leveling agent component of the plating solution was excessively supplied to the top of each TSV.[16] On the other hand, the speed of Cu film growth was lower at the top of the TSV because the effect of bottom-up filling on Cu film growth was smaller at the top of the TSV than in the inner part of the TSV. The excessive supply of the plating solution and the

lower speed of Cu film growth had a synergy effect, causing the leveling agent component to be easily introduced into the Cu film.

Hence, a larger size of Cu crystal grains at the top of each TSV could be effectively achieved by reducing the flow speed of the plating solution and thereby suppressing excessive supply of the leveling agent component in the process of Cu film formation, and this would be one of the methods for lowering Cu-TSV resistivity.

### 3.2.3 Cross-sectional observation of the Cu-TSVs and analysis of the precipitates

As mentioned in 3.2.2, we supposed the fine Cu crystal grains were a contributor to the high Cu-TSV resistivity, and we carefully observed cross sections of the Cu-TSVs using STEM.

Figure 10 shows STEM micrographs of the Cu-TSV. The bright field STEM image of the upper Cu-TSV in Fig. 10 (a) indicated that the numbers of impurities generated at the top and on the side wall of each TSV were larger, and that the sizes of the Cu crystal grains at the top and on the side wall of each TSV were smaller, compared to Cu crystal grains in the central part of the TSV. Furthermore, the dimension in the vertical direction of each TSV, i.e., the direction of electric current, was larger than the TSV width which suggested that the Cu grain boundaries near the top and side wall of the TSV contributed to the high Cu-TSV resistivity.

Figure 10 (b) is an enlargement of the area surrounded by the yellow square in Fig. 10 (a). The Cu crystalline structure was evaluated in detail. We found that there were many impurities of 0.1  $\mu\text{m}$  or less in size along the Cu grain boundaries. These impurities were thought to have suppressed Cu crystal growth and thus a localized transition took place along the grain boundaries during the 30 min heat treatment at 250°C. We also supposed that with an increase in these impurities, the distribution of fine Cu crystals was more extensive. Thus, such an increase contributed to the rise in Cu-TSV resistivity.

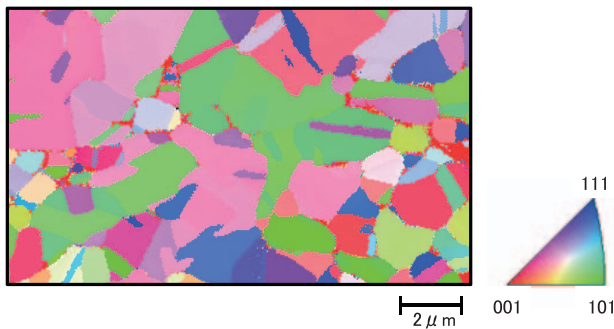


Fig. 7 Inverse pole figure pattern of Cu-TSV obtained by EBSD.

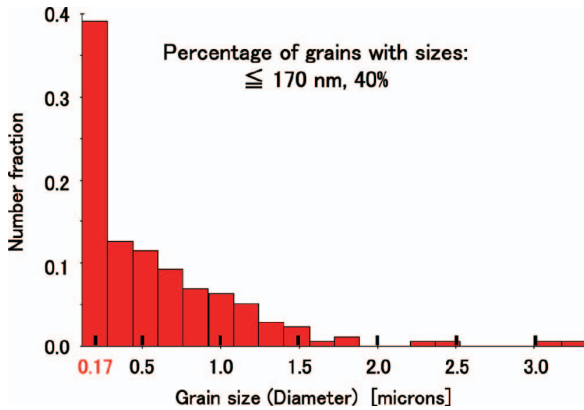


Fig. 8 Grain size distributions in the Cu-TSV by EBSD.

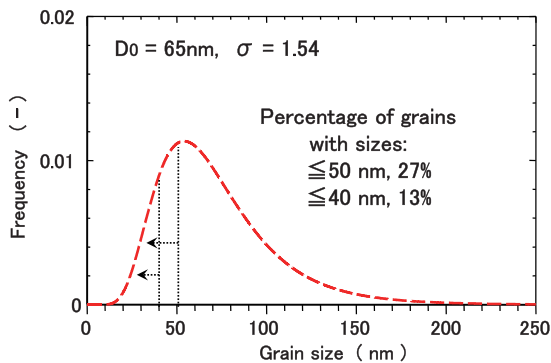


Fig. 9 Grain size distributions in the Cu-TSV by X-ray diffraction.

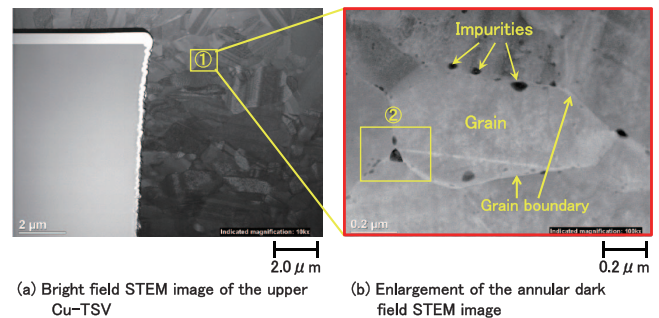


Fig. 10 STEM micrographs of Cu-TSV.

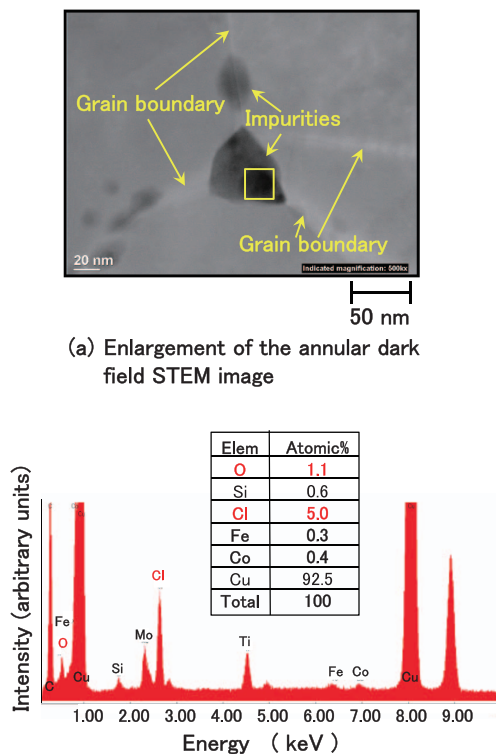


Fig. 11 Analyses of impurities by EDX.

Figure 11 (a) shows an annular dark field STEM image that provides an enlarged view of area ② in Fig. 10 (b). As shown in Fig. 11 (a), precipitates of approximately 70 nm in size were found along the Cu grain boundaries. Composition analysis was conducted on the interiors of these impurities using EDX, and the impurities Cl, O, Fe, and Co were detected (Fig. 11 (b)). Of the detected impurities, the ratios of Cl and O were particularly high (Cl, 5.0at %; O, 1.1at %). This suggested that Cl and O combined also with non-Cu metallic atoms, such as Fe or Co, as reported by Nagano, *et al.*[18]

#### 4. Conclusion

In this research, we designed a new pattern for Cu-TSV resistivity measurements and then used the pattern to derive Cu-TSV resistivity, one of the critical issues about Cu-TSVs for three-dimensional packaging. In addition, we evaluated the relationship between the derived Cu-TSV resistivity and Cu microstructure using EBSD, XRD, STEM and EDX. The conclusions of our study were as follows.

- (1) For TSVs 10  $\mu\text{m}$  in diameter and 80  $\mu\text{m}$  in depth, a Cu-TSV resistivity of  $4.13 \times 10^{-8} \Omega\cdot\text{m}$  was derived.
- (2) EBSD and XRD analyses yielded results indicating that 27% of the Cu crystal grains of the Cu-TSVs had a diameter of 50 nm or less while 13% had a diame-

ter of 40 nm or less. These fine Cu crystal grains were considered to have contributed to the high resistivity of  $4.13 \times 10^{-8} \Omega\cdot\text{m}$ .

- (3) STEM and EDX analyses revealed that precipitates had been generated near the top and side wall of each TSV at a higher frequency. The analyses also indicated that these precipitates were located along grain boundaries in Cu-TSVs and that they contained large proportions of Cl and O impurities.
- (4) Precipitates near the top and side wall of each TSV were supposed to have suppressed Cu crystal growth during heat treatment (250°C, 30 min) to cause reductions in crystal grain sizes. In addition, the precipitates were thought to have undergone a localized transition along the grain boundaries during the heat treatment and that was an underlying cause of the rise in Cu-TSV resistivity.

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