Global Standard for the Microelectronics Industry

LPDDR6
A Deep Dive Into the JEDEC Press Release

Mobile / Client / AI Computing Forum

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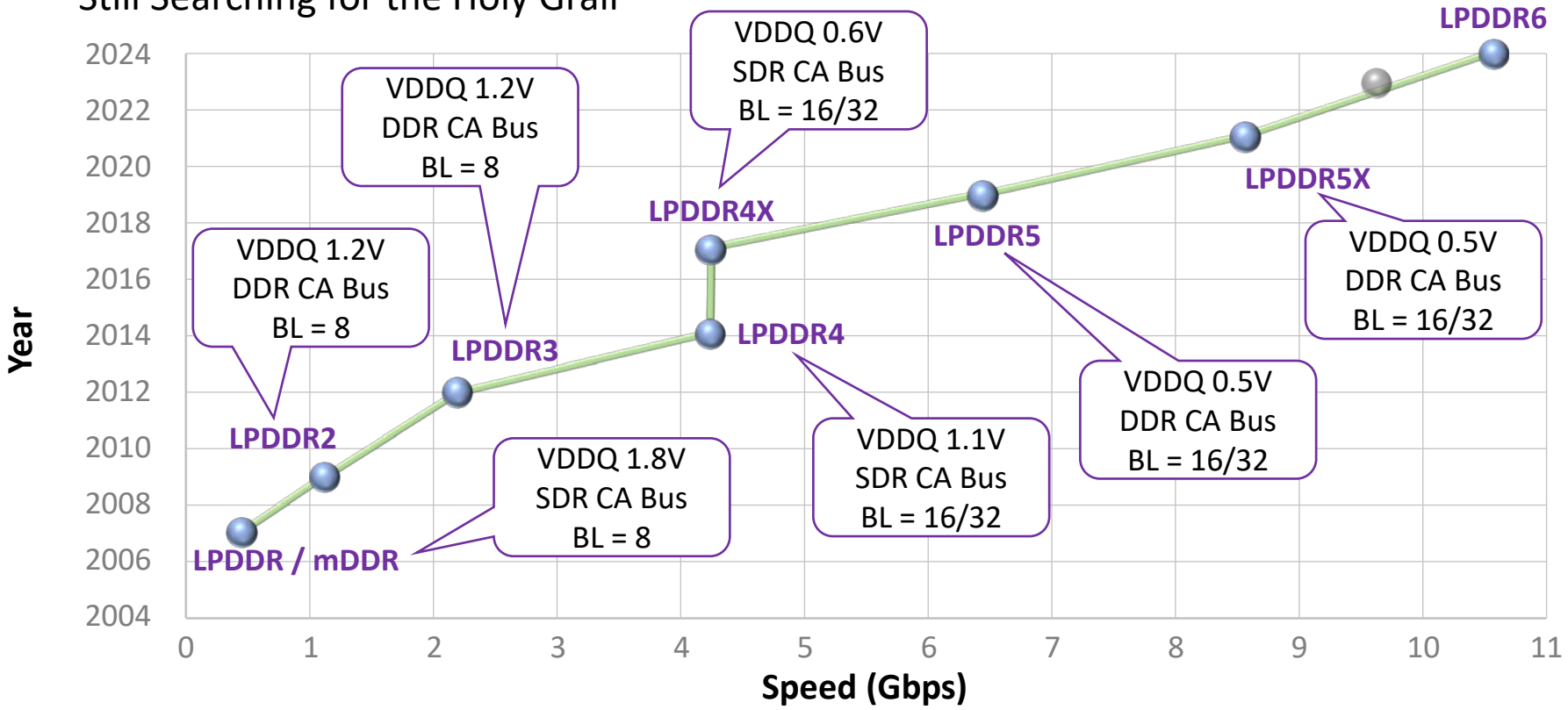
The JEDEC Timeline

Still Searching for the Holy Grail



JEDEC Plans to Update Popular Standard for Low Power Memory

JEDEC's JC-42.6 Subcommittee for Low Power Memories is developing the next generation of its popular LPDDR memory standard: LPDDR6. To significantly boost memory speed and efficiency for a variety of uses including mobile devices and AI, development plans for LPDDR6 include a focus on:

Increasing Bandwidth: To support AI applications and HPC use cases, various high frequency enablers are being considered
Lowering Power Usage: LPDDR6 will continue to reduce power as compared to the prior version of the standard
Enhanced RAS (Reliability, Availability and Serviceability) to improve security and performance

As with all JEDEC standards development activities, industry participation is welcome. Learn more about membership and join today.

JEDEC standards are subject to change during and after the development process, including disapproval by the JEDEC Board of Directors.

DISCLAIMER

The contents of this presentation are believed to be accurate[1] at the time of presenting; however, the LPDDR6 standard is not yet finalized and may still undergo significant changes. If you are not a JEDEC member please maintain a close relationship with your silicon provider and memory vendor(s) to ensure you have the latest information when planning for use of LPDDR6. If you are a JEDEC member – please pay attention to the LPDDR6 related task groups for the most up-to-date information.

1 : Based on JEDEC ballots as of March 2024 JC 42.6 committee meeting

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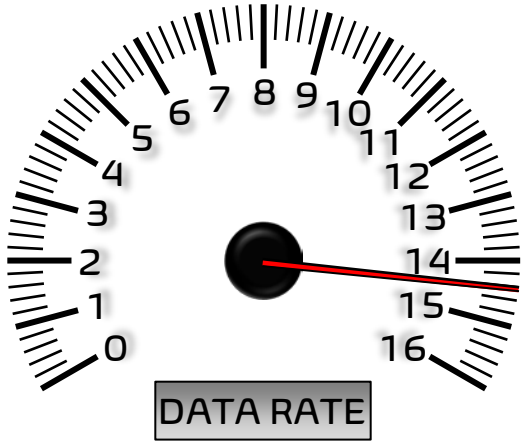
LPDDR6 – Increasing Bandwidth

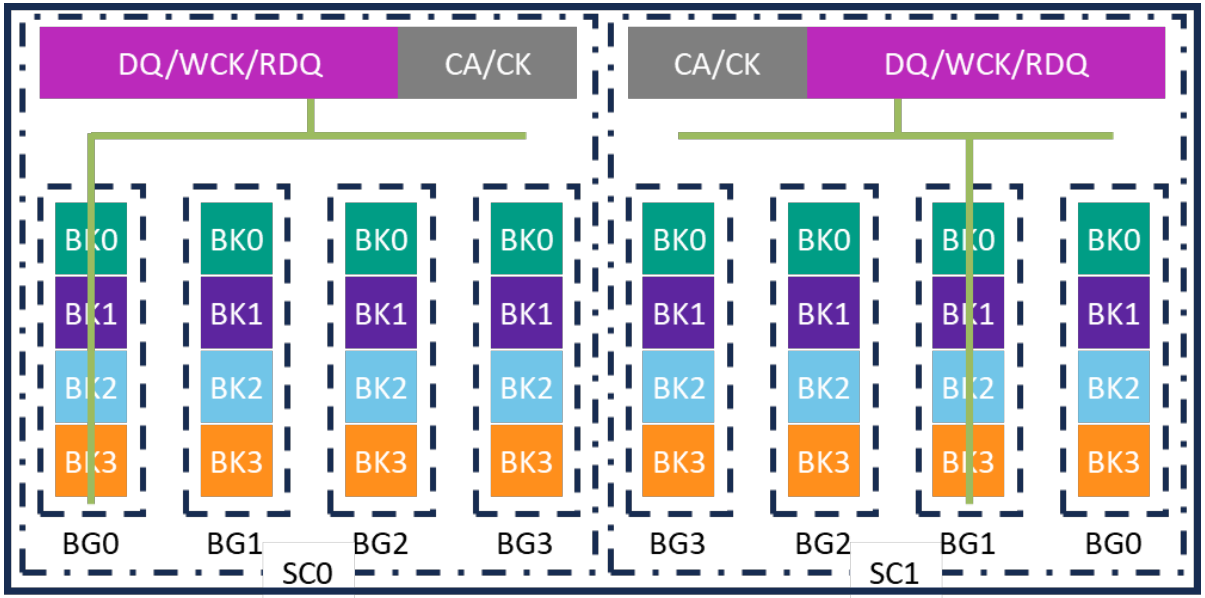
Bandwidth = Data Rate * Data Width

- Standard LPDDR5X bandwidth per channel
  - 8533 Mbps * 2 Bytes = 17.1 GBps
  - 9600 Mbps * 2 Bytes = 19.2 GBps
- LPDDR6 Introductory data rate – 10.667 Gbps
  - LPDDR6 Highest defined data rate – 14.4 Gbps
- LPDDR6 channel width – 24 bits
  - Composed of two 12 bit sub channels
- LPDDR6 introductory bandwidth – 32 GBps
  - Is it really almost double the LPDDR5X standard?
  - Or over 50% more than actual LPDDR5X-9600 devices?



LPDDR6 – Channel View

24-bit channels – what's inside?



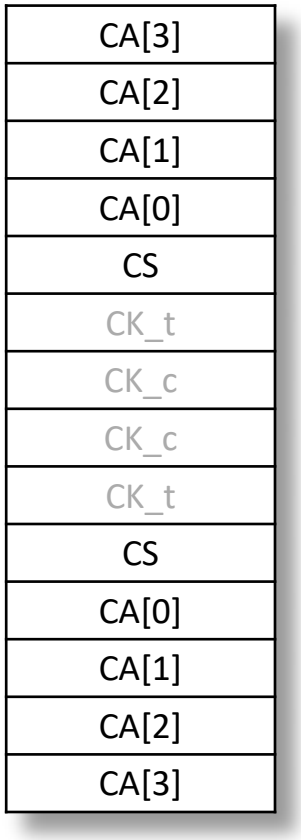
- 24-bit channels
- Two 12-bit sub channels
- CA and data per sub channel
- Four bank groups per sub channel
- Four banks per bank group

LPDDR6 – Command Interface

Something new

- LPDDR5X per channel
  - 7 Command and Address pins
  - 1 (or 2) Chip Select(s)
  - 2 CK (differential, with single ended mode support)

- LPDDR6 per channel
  - 8 Command and Address pins
    - 4 per sub channel
  - 2 (or 4) Chip Selects
    - 1 (or 2) per sub channel
  - **TBD** CK (differential, with single ended mode support)
    - Independent or Shared between sub channels???



LPDDR6 – Non CA Signals

Sub channel focus with some commonality

- Common signals per channel
  - ALERT (New!)
  - RESET_n
  - ZQ
- Sub channel based signals
  - WCK (differential, with single ended mode support)
  - RDQS (differential, with single ended and strobeless support)
  - DQ[11:0]
- Missing compared with LPDDR5X?
  - DMI

SC[0]	SC[1]
ALERT	DQ[11]
ZQ	DQ[10]
DQ[0]	DQ[9]
DQ[1]	DQ[8]
DQ[2]	DQ[7]
DQ[3]	DQ[6]
DQ[4]	DQ[5]
RDQS_t	WCK_c
RDQS_c	WCK_t
WCK_t	RDQS_c
WCK_c	RDQS_t
DQ[5]	DQ[4]
DQ[6]	DQ[3]
DQ[7]	DQ[2]
DQ[8]	DQ[1]
DQ[9]	DQ[0]
DQ[10]	RESET_n
DQ[11]	

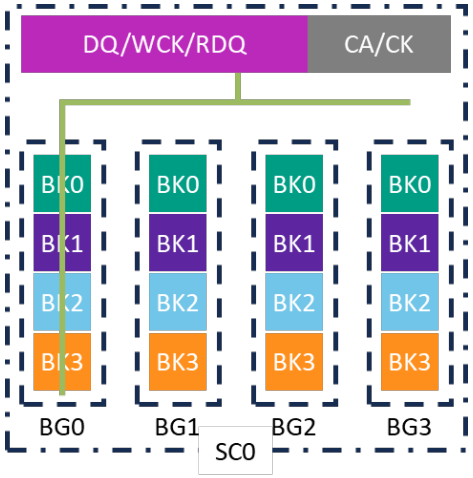
LPDDR6 – Sub Channel View

- Command & Address
  - 4 CA Pins, 1 (or 2) CS, **TBD** CK differential pair
- Data
  - 12 DQ, WCK & RDQS differential pair

12 Data pins?

That’s not very power-of-two-ish…

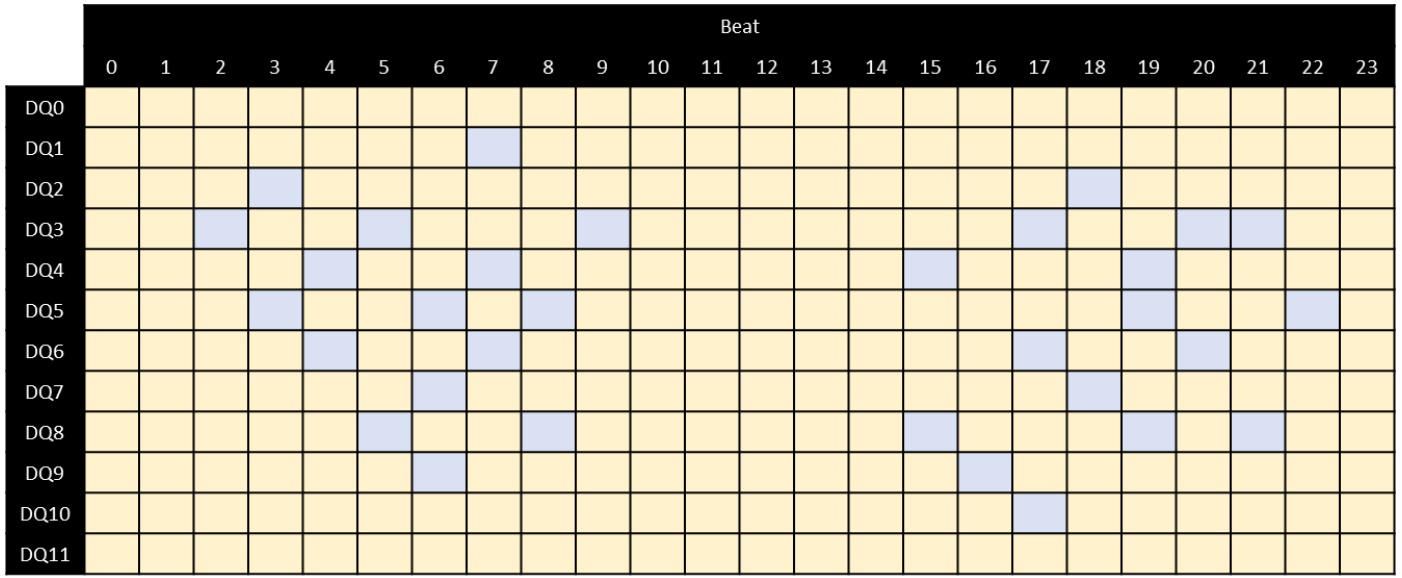
New burst length incoming!



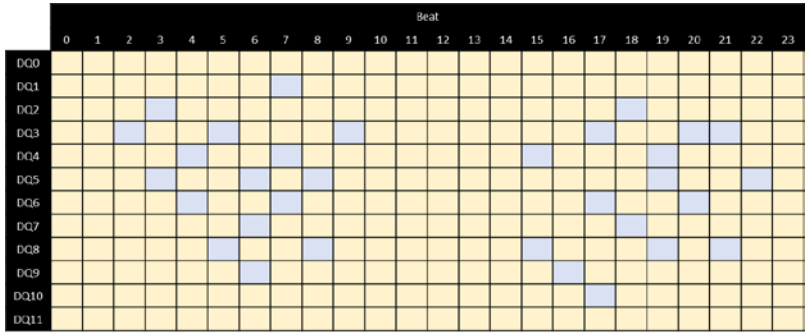
BL = 24!

12 DQ and BL 24?

- Math says a standard memory sub channel data packet is 288 bits
- We all like cache line sized chunks (256 bits / 512 bits)



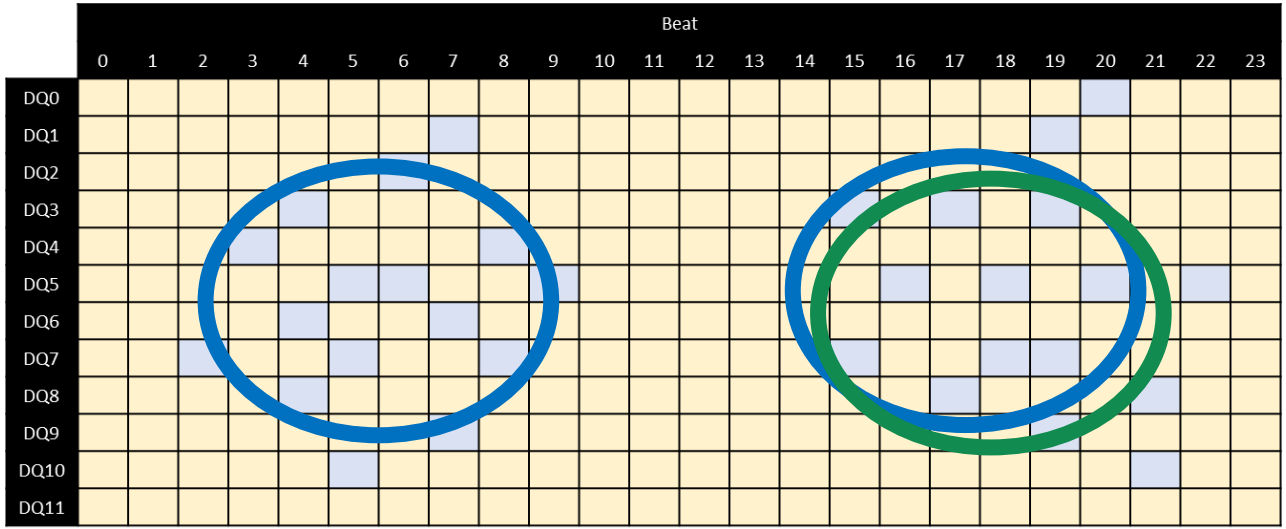
Back to Bandwidth



- Each memory access contains
  - 256 bits of data
  - 32 bits of – *not data*

- What is the effective bandwidth?
  - 10.667 Gbps * 256 bits data / 288 bits transferred * 24 bits / 8 bits/Byte
  - 28.5 GBps initially
  - 38.4 GBps eventually (14.4 Gbps) – double that of LPDDR5X-9600!

What about those 32 extra bits per sub channel?



RAS! **Low Power!**

LPDDR6 – The *Not Data* Bits

Metadata (16 bits) – M[15:0]

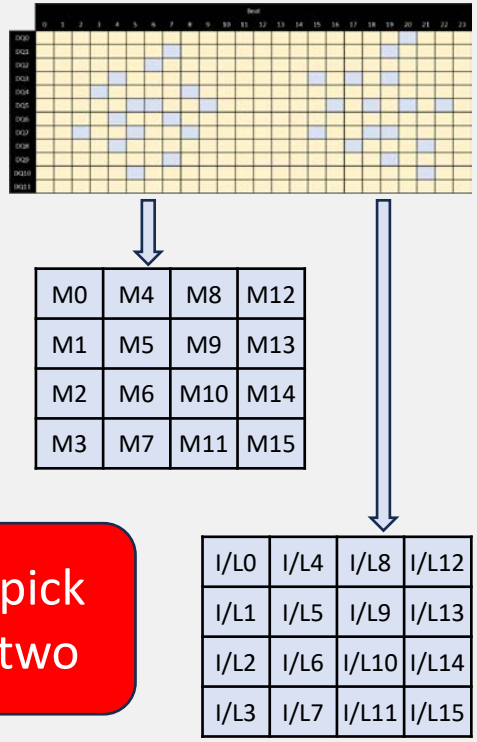
- Host ECC/EDC
- Memory tagging
- Whatever your heart desires…

RAS Focused (16 bits) – L[15:0]

- Link Protection

Low Power Focused (16 bits) – I[15:0]

- DBI



Sadly, you must pick only one of the two

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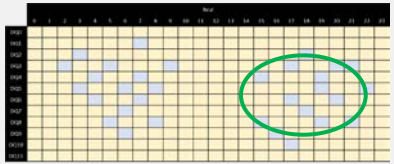
LPDDR6 – DBI

Data Bus Inversion (DC)



DBI (DC) is one option for the *not data* bits

No ballot specifically mentions Read DBI – but stay tuned…

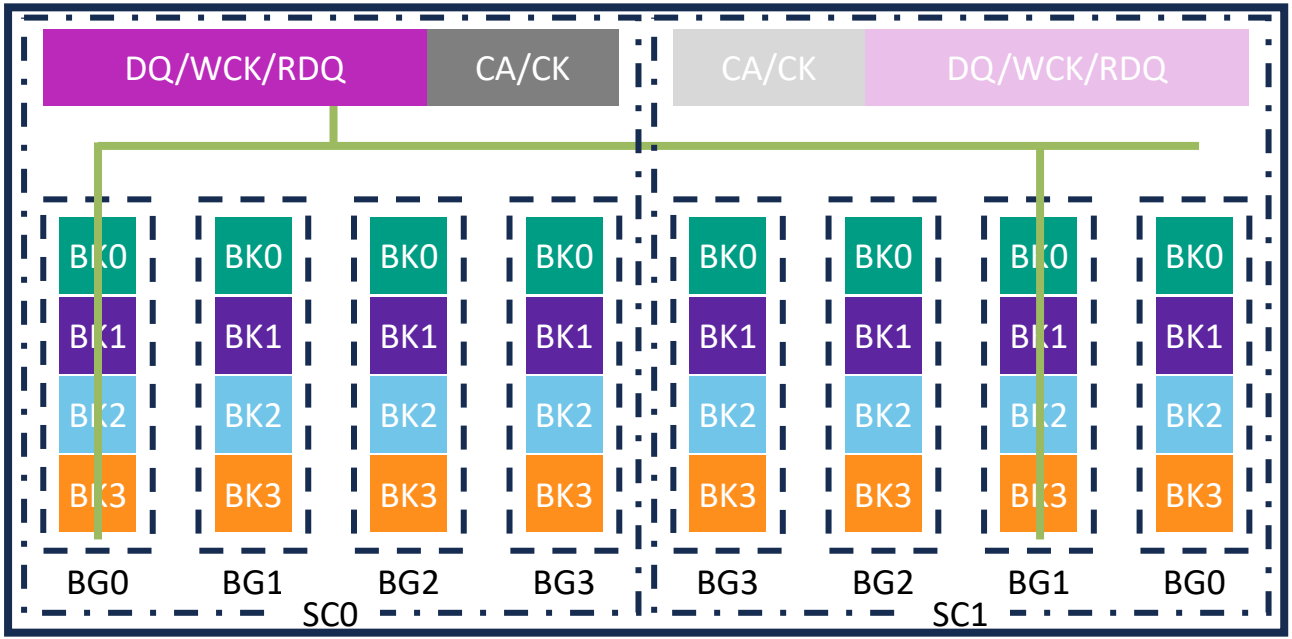
Write DBI has two options (MR programmable)

1. I[x] bit defines whether to XOR the bytes with 16'h0000 or 16'hFFFF
2. I[x] bit points to one of two 8-bit MRs which contain the value to be used in the XOR with the bytes

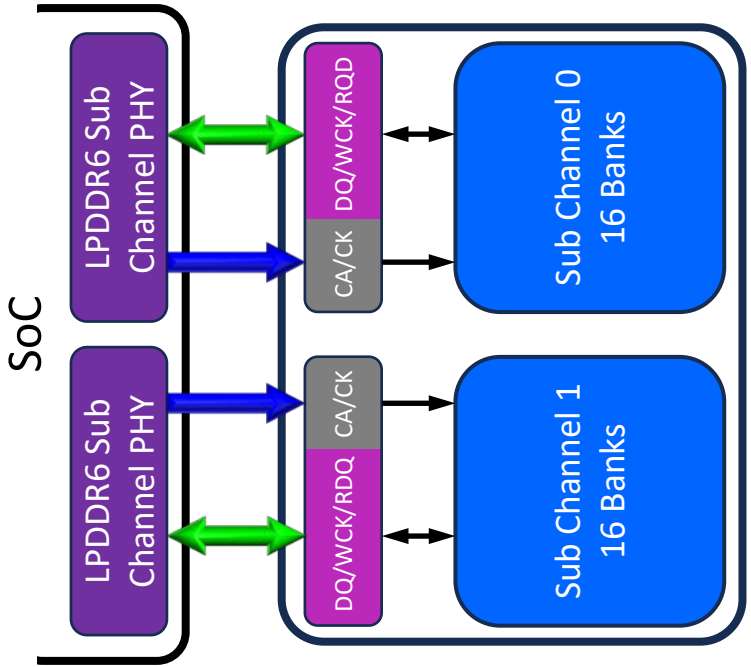
DBI Bit	Data Bits
DBI 0 (I0)	D[15:0]
DBI 1 (I1)	D[31:16]
DBI2 (I2)	D[47:32]
DBI3 (I3)	D[63:48]
DBI 4 (I4)	D[79:64]
DBI 5 (I5)	D[95:80]
DBI 5 (I6)	D[111:96]
DBI 7 (I7)	D[127:112]
DBI 8 (I8)	D[143:128]
DBI 9 (I9)	D[159:144]
DBI 10 (I10)	D[175:160]
DBI 11 (I11)	D[191:176]
DBI 12 (I12)	D[207:192]
DBI 13 (I13)	D[223:208]
DBI 14 (I14)	D[239:224]
DBI 15 (I15)	D[255:240]

LPDDR6 – Efficiency Mode

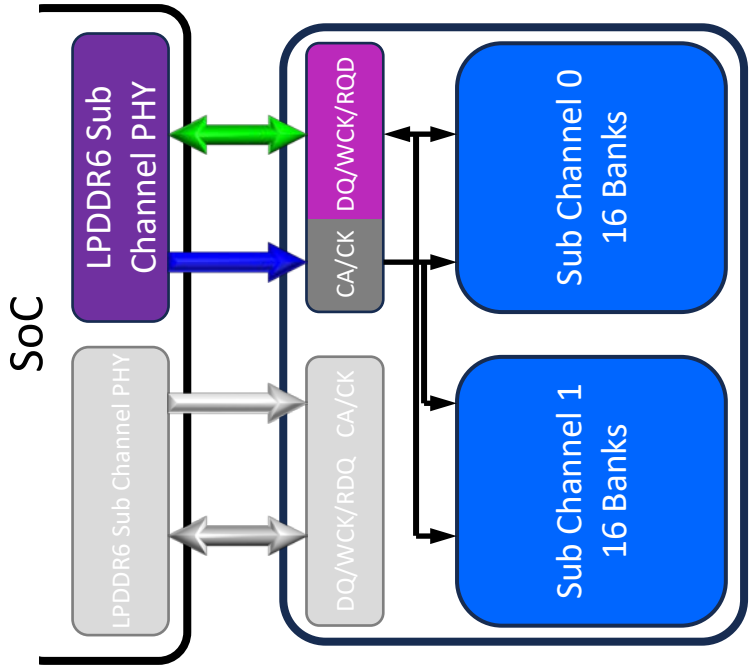
Lower Power!



LPDDR6 – Efficiency Mode



High Performance Mode



Low Power “Efficiency” Mode

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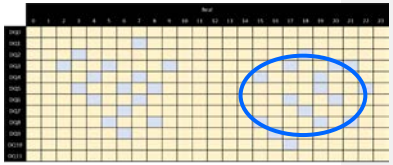
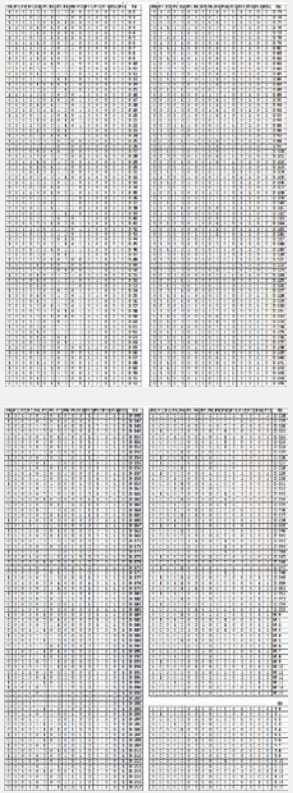
LPDDR6 – Link Protection

The other *not data* bits option



H-Matrix



Programmable Protection Options

	SBE Correct (ECC) SBE Detect (EDC)	DBE Detect	MBE Detect
None	Using DBI Instead?		
Write ECC	100%	100%	≥ 99.5%
Write EDC	100%	100%	≥ 99.998%
Read ECC	100%	100%	≥ 99.5%
Read EDC	100%	100%	≥ 99.998%

Read link errors are obvious to the host …

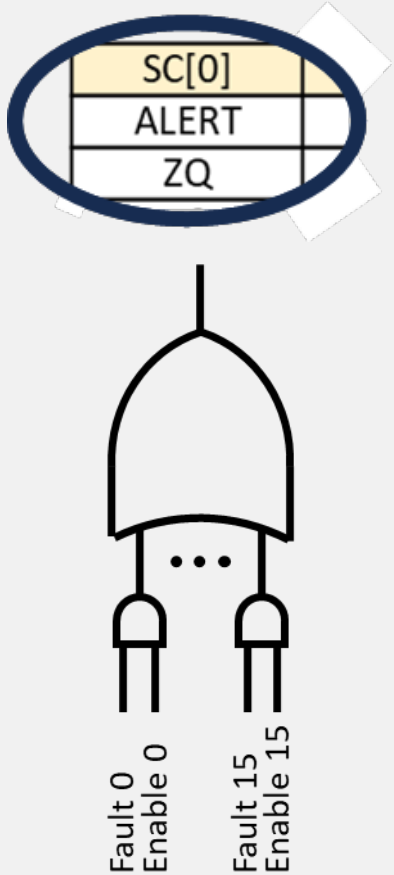
… But how does it know about write link errors???

LPDDR6 – Error Reporting

New Signal – New Functionality!

ALERT

- Fabulous new signal – provides a mechanism for LPDDR6 devices to signal faults to the host
- High Z when inactive so multiple ALERT device outputs can be connected to a single host input
- The device can register up to 15 different faults via four Fault Registers
- Faults such as Write ECC/EDC errors can be masked or reported on a real time basis



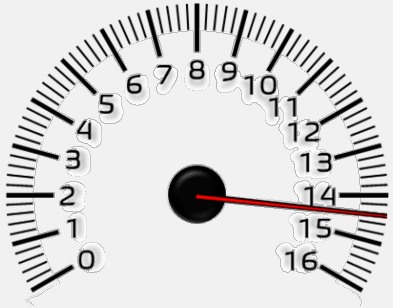
LPDDR6 – PRAC

From April 17, 2024 JEDEC Press Release regarding JESD79-5C DDR5 SDRAM Standard

JESD79-5C introduces an innovative solution to improve DRAM data integrity called Per-Row Activation Counting (PRAC). PRAC precisely counts DRAM activations on a wordline granularity. When PRAC-enabled DRAM detects an excessive number of activations, it alerts the system to pause traffic and to designate time for mitigative measures. These interrelated actions underpin PRAC's ability to provide a fundamentally accurate and predictable approach for addressing data integrity challenges through close coordination between the DRAM and the system.

Summary

Bandwidth



- 10+ Gbps data rates
- 24 bit channels
- 28.5 GBps initially
- 38.4 GBps defined

Low Power

- DBI
- Efficiency mode

RAS

- Metadata
- Link protection
- PRAC

Thank you!