# DERCHANG KAU

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## SUMMARY

Intel Fellow in semiconductor technology research and development. Expertise in heterogenous technology integration for high-performance computing, high-bandwidth interconnect and memory subsystems. Proven track record of driving innovation and delivering cutting-edge solutions. Adept at leading cross-functional teams and collaborating with industry partners to advance semiconductor technologies.

## EXPERIENCE

### June 26, 1995 – present, Intel Corporation, Santa Clara, CA, USA

***Jul 2021 – Present*** **| Intel Fellow, Director of Technology Pathfinding**
**Corporate Planning Group / Foundry Technology Engineering**
***Strategic*** Technology Roadmap Development and supply chain engagement with cross-functional leadership
***Innovative*** heterogenous integration of Logic, Memory, Power, Signaling and Packaging technologies
***Leading*** high bandwidth low power memory solutions cross the span from data center to client compute

***Jan 2017 – Jun 2021*** **| Intel fellow, Director of 3D-XPoint Memory Technology**
**Nonvolatile Memory Solution Group / Technology Development**
***Avid*** inventor leading R&D of technology and design teams exploring novel memory architecture
***Developed*** the strategic direction to build persistent memory using atomistic memory & switching devices
***Leadership*** and vision achieving breakthrough advances for Intel's leadership in Storage Class Memory

***Apr 2005 – Dec 2016*** **| Senior Principal Engineer, Director of Disruptive Memory Technology**
**Nonvolatile Memory Solution Group / Technology Development**
***Guided*** the foundational research of Phase Change Memory and Ovonic Threshold Switch technologies
***Championed*** the Product life cycle transition from initial concepts to the successful inception of Intel's first-generation 3D-XPoint memory product, a.k.a. Optane™ memory, in one decade

***Apr 2003 – Mar 2005*** **| Principal Engineer, Group Lead of NOR Flash Technology**
**Flash Product Group / Technology Development**
***Led*** 65nm Self-Align Contact (SAC) NOR Flash memory MLC device and architecture design
(SAC NOR Flash is commonly recognized as the de facto last generation NOR flash technology, which is still running in mainstream production.)

***Apr 2000 – Mar 2003*** **| Senior Staff Engineer, SOC Technology Development Lead**
**California Tech Development and Manufacturing / Process Integration**
***Technologist*** and architect for 90nm Mixed Signal and Embedded Flash Technology
***Managed*** Design Collateral enabling global collaboration cross US, Europe and Israel design teams
***Delivered*** world leading AFE and baseband processor used by Blackberry
***Demonstrated*** the first Intel CMOS GSM radio and drove digital radio initiative

***Jun 1995 – Mar 2000*** **| Staff Engineer, Transistor Architect and Design**
**California Tech Development and Manufacturing / Process Integration**
***Delivered*** transistors family in ¼μm NOR Flash Technology deployment for automotive application
***Awarded*** Intel IAA for Self-Aligned Floating Gate Technology of 130nm NOR Flash
***Invented*** dual gate oxide process for logic transistors and high voltage transistors

**June 1, 1987 – June 23, 1995, Digital Equipment Corporation, Hudson, MA, USA**

**Individual contributor with 3 levels of career advances**

***Device** Engineer:* Extensive Hands-On Experience in device design, layout and characterization
***Circuit** Designer:* SRAM Cell and Array Design and Characterization
***Process** Module Engineer:* including clean, diffusion, implant, PVD, Silicide, Salicide and dry/wet etch
***Process** Integration Engineer*: front-end integration processes and yield improvement strategies
***Expertise** and Innovations in Ion Implantation:* Avid inventor with deep knowledge in high-energy ion implantation beam line design, large-angle ion implant device design, and gate oxide hardening
***Transistors** Architect*: 0.75µm CMOS technology used in the Alpha-AXP CPU

## EDUCATION

**MSEE, Solid State Physics, The Ohio State University, Columbus, OH, USA**

**BSEE, Electronic Engineering, Chung Yuan University, Chung-li, Taiwan**

**Graduation with Honor, member of The Phi Tau Phi Scholastic Honor Society**

## PUBLICATION

**Multiply charged, channeled, ion implantation**, p668, Proceeding of the tenth International Conference on Ion Implant Technology, Catania, Italy, June, 1994

**Process optimization for large angle tilt implant**, p967, Proceeding of the tenth International Conference on Ion Implant Technology, Catania, Italy, June, 1994

**Implanted doping profile engineering design for manufacturability**, IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop (ASMC), Nov, 1994, **DOI:** 10.1109/ASMC.1994.588173

**Role of hydrogen anneal in thin gate oxide for multi-metal-layer CMOS process**, The 38th IEEE International Reliability Physics Symposium, Apr, 2000, **DOI:** 10.1109/RELPHY.2000.843912

**Enabling high-performance mixed-signal system-on-a-chip (SoC) in high performance logic CMOS technology**, 2002 Symposium on VLSI Circuits, Jun 2002, **DOI:** 10.1109/VLSIC.2002.1015074

**A Self-Aligned Contact Architecture with W-Gate for NOR Flash Technology Scaling**, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Apr, 2007, **DOI:** 10.1109/VTSA.2007.378934

**Fundamental drift of parameters in chalcogenide phase change memory**, *J. Appl. Phys.* 102, 124503 (2007), https://doi.org/10.1063/1.2825650

**The Role of Interfaces in Damascene Phase-Change Memory**, International Electron Devices Meeting. Dec, 2007. **DOI:** 10.1109/IEDM.2007.4418936

**Evidence of field induced nucleation in phase change memory**, *Appl. Phys. Lett.* 92, 173501 (2008), https://doi.org/10.1063/1.2917583

**Temporal Changes of Parameters in Phase Change Memory**, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Apr, 2008, **DOI:** 10.1109/VTSA.2008.4530836

**Phase change memory parameters: Effects of atomic transformations**, the 9th Annual Non-Volatile Memory Technology Symposium, Nov, 2008, **DOI:** 10.1109/NVMT.2008.4731187

**A stackable cross point Phase Change Memory**, International Electron Devices Meeting. Dec, 2009. **DOI:** 10.1109/IEDM.2009.5424263

**Phase Change Memory with Chalcogenide Selector (PCMS): Characteristic Behaviors, Physical Models and Key Material Properties**, Materials Research Society symposia proceedings, Aug, 2010. DOI: 10.1557/PROC-1250-G14-01-H07-01

**A Survey of Cross Point Phase Change Memory Technologies,** International Conference on Solid State Devices and Materials, Tokyo, Sep, 2010, pp1098-1099, https://doi.org/10.7567/SSDM.2010.E-8-1 and AVS 58th Annual International Symposium, Oct, 2011 https://www2.avs.org/symposium2011/Papers/Paper_EM2-MoA6.html

**Universal glass dynamics in PCM nano-glasses**, Materials Research Society symposia proceedings, Jan, 2011. **DOI:** 10.1557/PROC-1072-G02-09

**The Pursuit of Atomistic Switching and Cross Point Memory**, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Apr, 2021, **DOI:** 10.1109/VLSI-TSA51926.2021.9440112

## PATENT

DerChang Kau contributed to 120+ IP disclosures primarily in the field of memory technologies and integrated circuits. Here are a few notable examples

- **Integrated Circuit Structures with Stacked Electrostatic Discharge (ESD) for Backside Power Delivery** - This patent involves structures that include a device layer with a front side and a backside, incorporating a silicon substrate with a diode and/or bipolar junction transistor.
- **Bipolar Decoder for Crosspoint Memory** - This patent describes a memory device with a memory array and address lines, featuring decoder circuitry to apply various biases to the memory cells.
- **Apparatuses and Methods for Concurrently Accessing Multiple Partitions of a Non-Volatile Memory** - This patent covers methods for performing multithread, concurrent access of different partitions of a memory array.
- **Self-Aligned Cross-Point Phase Change Memory-Switch Array** - This patent relates to a memory device, specifically a self-aligned cross-point phase change memory-switch array.
- **Stacked Two-Level Backend Memory** - This patent involves integrated circuit devices with stacked two-level backend memory, enhancing memory cell density and functionality.

### List of patents

| # | Patent number | Title | Date |
|---|---|---|---|
| 1 | US-11900998 | Bipolar decoder for crosspoint memory | 02/13/24 |
| 2 | US-11768603 | Apparatuses and methods for concurrently accessing multiple partitions of a non-volatile memory | 09/26/23 |
| 3 | US-11563055 | Self-aligned cross-point phase change memory-switch array | 01/24/23 |
| 4 | US-11354040 | Apparatuses and methods for concurrently accessing multiple partitions of a non-volatile memory | 06/07/22 |

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| 5 | US-11276465 | Device, system and method to float a decoder for deselected address lines in a three-dimensional crosspoint memory architecture | 03/15/22 |
| 6 | US-11114143 | Bipolar decoder for crosspoint memory cells | 09/07/21 |
| 7 | US-11010061 | Scalable bandwidth non-volatile memory | 05/18/21 |
| 8 | US-10877352 | Semiconductor photonic devices using phase change materials | 12/29/20 |
| 9 | US-10783965 | Apparatuses and methods including memory access in cross point memory | 09/22/20 |
| 10 | US-10719237 | Apparatuses and methods for concurrently accessing multiple partitions of a non-volatile memory | 07/21/20 |
| 11 | US-10692930 | Self-aligned cross-point phase change memory-switch array | 06/23/20 |
| 12 | US-10475853 | Replacement materials processes for forming cross point memory | 11/12/19 |
| 13 | US-10431270 | Apparatuses for modulating threshold voltages of memory cells | 10/01/19 |
| 14 | US-10331360 | Scalable bandwidth non-volatile memory | 06/25/19 |
| 15 | US-10304534 | Apparatuses and methods including memory access in cross point memory | 05/28/19 |
| 16 | US-10163507 | Apparatuses and methods including memory access in cross point memory | 12/25/18 |
| 17 | US-10163982 | Multi-deck memory device with inverted deck | 12/25/18 |
| 18 | US-10090050 | Apparatuses and methods including memory access in cross point memory | 10/02/18 |
| 19 | US-10050084 | Replacement materials processes for forming cross point memory | 08/14/18 |
| 20 | US-9905296 | Apparatuses and methods including memory access in cross point memory | 02/27/18 |
| 21 | US-9905280 | Methods and apparatuses for modulating threshold voltages of memory cells | 02/27/18 |
| 22 | US-9747978 | Reference architecture in a cross-point memory | 08/29/17 |
| 23 | US-9734907 | Apparatuses and methods including memory access in cross point memory | 08/15/17 |
| 24 | US-9698344 | Dielectric thin film on electrodes for resistance change memory devices | 07/04/17 |
| 25 | US-9659997 | Replacement materials processes for forming cross point memory | 05/23/17 |

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| 26 | US-9653127 | Methods and apparatuses for modulating threshold voltages of memory cells | 05/16/17 |
| 27 | US-9613698 | Set and reset operation in phase change memory and associated techniques and configurations | 04/04/17 |
| 28 | US-9590012 | Self-aligned cross-point phase change memory-switch array | 03/07/17 |
| 29 | US-9576659 | Apparatuses and methods including memory access in cross point memory | 02/21/17 |
| 30 | US-9368554 | Apparatuses and methods including memory access in cross point memory | 06/14/16 |
| 31 | US-9368205 | Set and reset operation in phase change memory and associated techniques and configurations | 06/14/16 |
| 32 | US-9306165 | Replacement materials processes for forming cross point memory | 04/05/16 |
| 33 | US-9287498 | Dielectric thin film on electrodes for resistance change memory devices | 03/15/16 |
| 34 | US-9245926 | Apparatuses and methods including memory access in cross point memory | 01/26/16 |
| 35 | US-9142271 | Reference architecture in a cross-point memory | 09/22/15 |
| 36 | US-8909849 | Pipeline architecture for scalable performance on memory | 12/09/14 |
| 37 | US-8765581 | Self-aligned cross-point phase change memory-switch array | 07/01/14 |
| 38 | US-8730755 | Single transistor driver for address lines in a phase change memory and switch (PCMS) array | 05/20/14 |
| 39 | US-8649212 | Method, apparatus and system to determine access information for a phase change memory | 02/11/14 |
| 40 | US-8605531 | Fast verify for phase change memory with switch | 12/10/13 |
| 41 | US-8462577 | Single transistor driver for address lines in a phase change memory and switch (PCMS) array | 06/11/13 |
| 42 | US-8404514 | Fabricating current-confining structures in phase change memory switch cells | 03/26/13 |
| 43 | US-8385100 | Energy-efficient set write of phase change memory with switch | 02/26/13 |
| 44 | US-8374022 | Programming phase change memories using ovonic threshold switches | 02/12/13 |
| 45 | US-8289762 | Double-pulse write for phase change memory | 10/16/12 |
| 46 | US-8278641 | Fabricating current-confining structures in phase change memory switch cells | 10/02/12 |

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| 47 | US-8184469 | Stored multi-bit data characterized by multiple-dimensional memory states | 05/22/12 |
| 48 | US-8081506 | Amorphous semiconductor threshold switch volatile memory cell | 12/20/11 |
| 49 | US-8049197 | Self-aligned nano-cross-point phase change memory | 11/01/11 |
| 50 | US-7986549 | Apparatus and method for refreshing or toggling a phase-change memory cell | 07/26/11 |
| 51 | US-7764477 | Electrostatic discharge protection circuit including ovonic threshold switches | 07/27/10 |
| 52 | US-7751226 | Reading phase change memories with select devices | 07/06/10 |
| 53 | US-7547597 | Direct alignment scheme between multiple lithography layers | 06/16/09 |
| 54 | US-7087943 | Direct alignment scheme between multiple lithography layers | 08/08/06 |
| 55 | US-6911695 | Transistor having insulating spacers on gate sidewalls to reduce overlap between the gate and doped extension regions of the source and drain | 06/28/05 |

## REFERENCE UPON REQUESTS